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APPLIED PHYSICS REVIEWS

Silicon carbide: A unique platform for metal-oxide-semiconductor physics

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A sustainable energy future requires power electronics that can enable significantly higher efficiencies in the generation, distribution, and usage of electrical energy. Silicon carbide (4H-SiC) is one of the most technologically advanced wide bandgap semiconductor that can outperform conventional silicon in terms of power handling, maximum operating temperature, and power conversion efficiency in power modules. While SiC Schottky diode is a mature technology, SiC power Metal Oxide Semiconductor Field Effect Transistors are relatively novel and there is large room for performance improvement. Specifically, major initiatives are under way to improve the inversion channel mobility and gate oxide stability in order to further reduce the on-resistance and enhance the gate reliability. Both problems relate to the defects near the SiO_2/SiC interface, which have been the focus of intensive studies for more than a decade. Here we review research on the SiC MOS physics and technology, including its brief history, the state-of-art, and the latest progress in this field. We focus on the two main scientific problems, namely, low channel mobility and bias temperature instability. The possible mechanisms behind these issues are discussed at the device physics level as well as the atomic scale, with the support of published physical analysis and theoretical studies results. Some of the most exciting recent progress in interface engineering for improving the channel mobility and fundamental understanding of channel transport is reviewed.
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I. INTRODUCTION TO SiC SEMICONDUCTOR TECHNOLOGY

Silicon carbide (SiC) is a wide-bandgap semiconductor considered to be one of the major enabling materials for advanced high power and high temperature electronics applications. In addition to its wide bandgap, SiC also has a high critical electric field strength and a high saturation drift velocity, making it able to sustain higher voltages with lower conduction loss. Device fabrication is also attractive since

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SiC can be doped both n- and p-type with relative ease, and a native oxide can be formed. With recent improvements, SiC-based electronics are now superior for power conversion than current silicon-based electronics, especially for high-temperature, high-power, and high-frequency applications.[1] In addition, SiC has also been successfully employed in microwave devices,[2] UV photodiodes, and light emitting diodes.[3] In addition, SiC has been used in special applications in harsh environments requiring higher temperatures (300–600 °C) and/or higher radiation hardness.[4,5] Besides applications as an active semiconductor, SiC is routinely used as templates for heteroepitaxy of nitride materials for optoelectronics. SiC has also been intensively studied as the substrate for synthesis of graphene via Si sublimation.[6] In this regard, it has been recently reported that graphene with a non-zero bandgap can be formed from nitrogen-seeded SiC,[7] which may provide a promising path to large-area semiconducting graphene for fabrication of graphene devices using wafer-scale processing techniques.

A. SiC material properties

Silicon carbide has more than 200 polytypes, divided into three basic crystallographic categories: cubic (C), hexagonal (H), and rhombohedral (R). The electronic properties of SiC vary significantly with polytype. The 4H-SiC polytype is currently preferred for power electronics due to the advances in 4H-SiC growth technology and its attractive electronic properties over other available wafer-scale polytypes. For instance, compared to 6H-SiC, 4H-SiC has a larger band gap and a higher intrinsic carrier mobility.[8] 4H-SiC crystal growth and epitaxy technologies have matured rapidly, and large diameter wafers (6 in.) are currently available. For the rest of the paper, our discussion will be restricted to 4H-SiC, unless otherwise noted.

For unipolar power devices such as Schottky diodes or metal oxide semiconductor field effect transistors (MOSFETs), for a certain rated breakdown voltage (BV), the ideal on-resistance of the device depends on the semiconductor material's dielectric constant (ε_S), the carrier mobility (μ), and the critical electric field (E_c) at the onset of breakdown, i.e.,[9]

$$\boldsymbol{R_{on}} = \frac{4\boldsymbol{BV}^2}{\varepsilon_S \boldsymbol{\mu} \boldsymbol{E}_c^3}, \tag{1}$$

where ($\varepsilon_S \mu E_c^3$) is called the Baliga figure of merit (BFOM), which is commonly used to qualitatively compare the expected performance of semiconductors for power applications.[9] This quantity represents the ideal resistance of a power (vertical) Schottky diode and is a measure of the ideal performance of any semiconductor material for unipolar power electronic devices. Table I summarizes the Relative-to-Si BFOM's of various materials. It can be seen from the table that wide bandgap semiconductors have a significantly higher BFOM compared to Si and GaAs due to their higher critical electric field as a result of higher band-gap. Besides lower on-resistance, SiC has other advantages over Si that are not directly expressed in the BFOM. The larger bandgap

TABLE I. The bandgap (E_g) dielectric constant (ε_S), electron mobility ($\boldsymbol{\mu_n}$), critical electric field ($\boldsymbol{E_c}$), and relative-to-Si BFOM's of various materials. The electron mobility for 4H-SiC is in [0001] direction.[10–12]

Material	4H-SiC	GaN	β-Ga_2O_3	Diamond	GaAs	Si
E_g (eV)	3.26	3.4	4.7–4.9	5.5	1.4	1.1
ε_S	9.7	9.0	10	5.5	13.1	11.8
μ_n (cm^2/V s)	900	900	300	1 900	8500	1430
E_c(MV/cm)	3.0	3.3	8	10	0.4	0.3
Relative BFOM	517	852	3371	22 937	16	1

results in significantly reduced minority carrier generation under high voltage and temperature, which in turn leads to lower leakage currents during the off-state of the power device. SiC also has a higher thermal conductivity (3×) and a higher saturation carrier velocity (2×) compared to Si, which enables high current density and high frequency operation. In addition, SiC is the only wide band gap semiconductor that has SiO_2 as the native oxide, making it a leading candidate for the development of next-generation, energy efficient, power MOSFET.

For SiC, the traditional bulk (substrate) growth techniques are based on physical vapor transport. Crystals are grown through the sublimation of a SiC source placed in the hot zone (2100–2400 °C) of the furnace and the subsequent mass transport of the vapor species to the seed crystal located in a cooler region of the furnace. These processes are difficult to control, particularly for large wafers. In order to produce defect free material with precise doping, controlled homoepitaxial techniques are necessary to grow device quality material on bulk substrates. Chemical vapor deposition (CVD) is presently the most widely used epitaxial technique for the growth of SiC device structures.[13,14] Both n-type and p-type doping are possible in SiC. Nitrogen is commonly used as a donor, and aluminum is the acceptor of choice. Phosphorous and boron can also be used as donors and acceptors, respectively.[13,14] Controlled doping of selective areas in SiC is implemented by ion implantation, followed by high-temperature annealing to activate the dopants and remove the implantation induced damage. Diffusion is not a suitable process here, due to low diffusion coefficients of the main dopants in SiC.[15]

One of the typical features of wide-band gap semiconductors, such as SiC compared to silicon, is the $>k_BT$ activation energies of common doping impurities at room temperature. This leads to incomplete impurity ionization which in addition to increasing substrate resistance, impacts device characteristics when the impurity quasi-Fermi level position changes. The inequivalent lattice sites for the same impurity species further complicate the situation. The detailed impact of these effects on device operation has been studied for SiC Schottky diodes[16] and MOSFETs,[17] and this factor needs to be taken into account during device design.

B. SiC power electronics technology

The unique material properties and the availability of specialized process technology have enabled the development of state-of-the-art SiC devices, especially for power

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electronics. In 2001, the first SiC power Schottky diodes operating in the voltage range between 300 V and 600 V were introduced to the market by Infineon.[18] In 2008, the first full SiC 1200 V/230 A power module that consists of a converter and an inverter, for use in electric and hybrid cars was introduced to the market by Honda and ROHM.[19] The 600 V SiC MOSFET was first produced in 2010 by ROHM,[20] followed by the 1200 V power MOSFET from Cree.[21] Today, there are more than a dozen major device manufacturers and developers in the SiC power electronics market across the world.[22]

The drivers for growth include higher switching frequencies, blocking voltages, operating temperatures, and radiation hardness. Key applications for SiC technologies include hybrid electric and all-electric vehicles, Photovoltaic (PV) inverters, power supplies and Uninterruptible Power Supply (UPS), industrial motor drives, traction, and wind turbine controls. The SiC power semiconductor market is projected to be more than $\$1.6 \times 10^9$ in 2022.[22] Currently, the main growth barriers of this technology are the relatively higher material and device costs compared to Si, novel application design inertia and reliability concerns. There has been continuous progress in reduction of defect densities, increase of wafer size, and lowering of wafers costs over the last decade. Since 2013, 6-in. diameter SiC wafers are in mass production, which is expected to have a significant positive impact on device cost.

The SiC power MOSFET has many inherent advantages over other types of switches for low and medium power applications. Compared to the SiC Junction Gate Field Effect Transistor (JFET) and Bipolar Junction Transistor (BJT), SiC MOSFETs have the highest industry acceptance due to simpler power circuit design and simpler gate driver circuits. MOSFETs are voltage controlled devices, unlike BJTs which are current controlled, and do not require any special voltage shape unlike in the case of JFET or very high peak current (BJT) for a fast turn-on and correct conduction operation. In addition, as a majority carrier device, MOSFET avoids the minority carrier storage time that exists in the bipolar power BJTs, enabling it to switch at much higher frequencies.

The first lateral SiC MOSFET was made on 3C-SiC by Kondo *et al.* in 1986.[23] A decade later, the first high-voltage double implanted power MOSFET (DMOSFET) was demonstrated by Shenoy *et al.* on 6H-SiC.[24] Research has led to rapid progress for 4H-SiC DMOSFETs in the last ten years. The schematic cross-section of a typical n-channel DMOSFET cell is shown in Figure 1. In order to obtain high current densities, many cells are connected in parallel in a single power switch die. For power applications, the device is usually designed for "normally off" operation, i.e., no current conduction takes place without the application of a positive gate voltage. In this "off-state," the depletion region formed at the p-well/n-type drift region junction (see figure) blocks the high drain to source bias (V_{DS}). When the applied gate voltage is higher than the threshold voltage, surface band-bending inverts the p-type region under the gate oxide and an electron conduction path or channel formation at the surface, and forming a conduction path from drain to source.

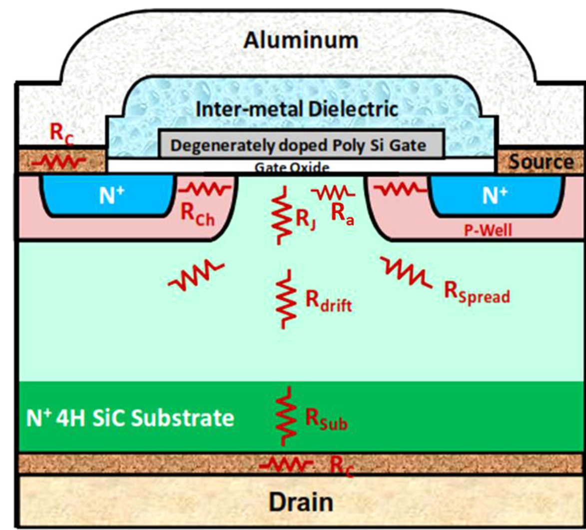

FIG. 1. Schematic of a DMOSFETs, resistances contributing to total ON-resistance. Reproduced with permission from Palmour *et al.*, "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV," in *IEEE 26th International Symposium on Power Semiconductor Devices & IC's* (*ISPSD*) (2014), pp. 79–82. Copyright 2014 IEEE.

The specific on-state resistance or total device resistance ($R_{ON,SP}$, in mΩ cm^2), is the typical parameter used to evaluate on-state power loss. This quantity is calculated from the slope of J_D-V_{DS} at a specified gate voltage. As shown in Figure 1, following the conduction path of the current from source electrode on the top to the drain electrode at the bottom, the various resistance components of $R_{ON,SP}$ can be identified as follows: (i) Contact resistances (R_C) in all source and drain electrodes; (ii) the channel resistance (R_{Ch}) that is limited by carriers' density and mobility; (iii) the accumulation layer resistance (R_a) in the n type surface region in series with the channel; (iv) the JFET resistance (R_J) of the internal junction gate field-effect transistor that is formed by the n type vertical conducting channel between the two adjacent p-wells; (v) the spreading resistance (R_{Spread}) as current spreads out horizontally to take advantage of the broader conducting path in the drift layer; (vi) the drift-layer resistance (R_{drift}) that is limited by its relatively low doping and large thickness to sustain the high blocking voltage; and (iv) the substrate resistance (R_{sub}) that mainly depends on the thickness of the heavily doped supporting substrate.

During the 1990s, a lot of progress was made in increasing the blocking voltage rating, but with little progress in reducing forward conducting resistance. The low mobility of inversion electrons in MOS channel due to severe electron trapping and scattering at the SiO_2/4H-SiC interface has been the main shortcoming of power MOSFETs. Unlike Si MOSFETs, post metallization anneals with H_2 do not reduce these interface traps (or defects) resulting in higher than ideal on-state resistance SiC devices.

The introduction of a post-oxidation annealing in nitric oxide (NO) was a huge breakthrough for reducing SiC channel resistance. NO annealing was first shown to improve the interface defect density (D_{it}) near the conduction band edge on 6H-SiC by Li *et al.* in 1997.[26] NO annealed MOSFETs

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initially showed a fivefold increase in inversion layer electron mobility and a corresponding reduction in channel resistance as first demonstrated by Chung *et al*. in 2001.[27] This important breakthrough is one of the most important milestones in the development and commercialization of SiC power MOSFETs. Since then, there has been tremendous progress with a further reduction of the on-state resistance and improved blocking performance. The measured specific on-resistance of various state-of-the-art DMOSFETs is shown in Figure 2 and compared to the ideal value at any blocking voltage.[25] The ideal $R_{ON,SP}$ for Si and SiC can be calculated using Eq. (1) recognizing that the blocking layer or drift layer resistance R_{drift} is lowest on-resistance possible in a DMOSFET, intrinsic to the semiconductor material. From the figure, we can see that SiC-based devices have significant advantage over Si-based devices, especially for blocking voltage ratings of 1000 V and higher. The practical device performance of SiC MOSFETs is close to the ideal limit at higher breakdown voltages above about 3 kV. In this regime, thick blocking layers are necessary and therefore R_{Drift} dominates R_{on}. However, at commercially relevant blocking voltage ratings of 600 V–1700 V, the experimental $R_{ON,SP}$ is significantly higher than the ideal, as the channel resistance forms a significant part of the total resistance. New channel engineering processes are therefore pivotal for further reduction of $R_{ON,SP}$ in this voltage range. In Sec. III, the channel resistance problem will be discussed in detail.

In the power switching market, the competing silicon technologies are Si super-junction (SJ) MOSFETs for low voltage ratings (600 V) and insulated gate bipolar transistors (IGBTs) for high voltage ratings (6.5 kV). In the 1200 V range, the SiC MOSFET can offer 50% lower R_{ON}, lower leakage current, and weaker temperature dependence. In the latter case, due to the superior SiC material properties and its unipolar characteristics, the SiC MOSFET can exhibit very high frequency switching performance, resulting in significant reductions in switching losses.[25]

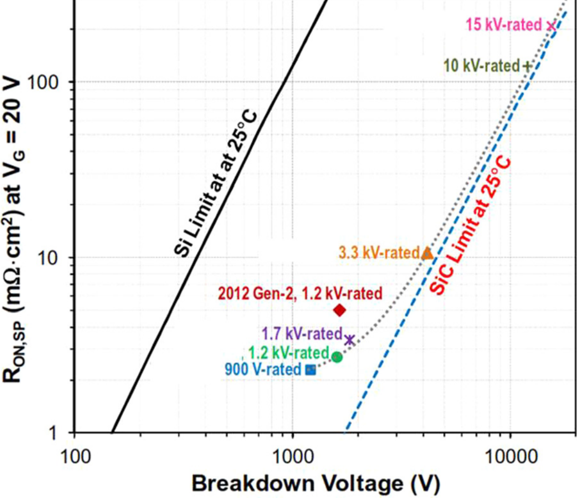

FIG. 2. Examples of state-of-the-art 4H-SiC power MOSFET performance. Specific on-resistance, $R_{ON,SP}$ in mΩ·cm^2, of the SiC DMOSFETs measured at gate bias of 20 V as a function of breakdown voltage at 25 °C. Reproduced with permission from Palmour *et al*., "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV," in *IEEE 26th International Symposium on Power Semiconductor Devices & IC's* (*ISPSD*) (2014), pp. 79–82. Copyright 2014 IEEE.

II. SiC/SiO$_2$ INTERFACE

The nanoscale chemistry of the SiC-oxide interface is intricately connected to the channel transport in SiC MOSFETs. Various research papers have been devoted to the theoretical and analytical study of SiC/SiO$_2$ interface properties. Here, we summarize the present understanding of the nature of interfacial defects and reactions with nitric oxide, which are currently the most established process for interface defect passivation.

A. Theory of oxidation

Many features of the oxidation process are well understood. In general terms, the oxidation of SiC is similar to the oxidation of pure Si.[28–30] In pure Si, the density mismatch of Si across the interface is mainly relieved by the oxygen mediated Si (2×1) reconstruction of the Si (100) surface.[31,32] Reconstructions at the SiC-oxide interface are more subtle. Also, in oxides grown on SiC, there is no detectable carbon found in the gate oxide. The release of excess carbon occurs during oxidation, mainly as molecular CO species. The dominant microscopic aspects of oxidation have been elucidated by theoretical studies employing density functional calculations using realistic interface models.[33–41]

In Figure 3, we illustrate the oxidation of a new layer of SiC at an abrupt SiC-oxide interface using three panels. Panel (a) shows an O_2 molecule approaching the interface through the growing oxide. Panel (b) shows that, at the interface, O–O bonds readily break apart to form the stronger Si–O–C bonds. In panel (c), carbon is removed from SiC as a CO molecule leaving behind an oxygen passivated carbon vacancy (V_CO_2) with only Si–O–Si bonds. In the process of growing the oxide and emitting carbon, several metastable defect structures have been identified but they are not shown in Figure 3.[33,35] Such defects are continuously generated and annihilated during the oxidation of SiC.

B. Review of interfacial and near–interfacial Defects

After the oxidation process terminates, there remains a concentration of kinetically stable defects formed at and near the SiC-Oxide interface.[36,41,42] The identification of the remaining defects is challenging because the interface structure is highly disordered and the concentration of the important electrically active defects is relatively small. For instance, electrically active interface defects in SiC MOS have a concentration of $\sim 10^{-12}$ cm^{-2}, which corresponds to one defect per 1000 SiC units. The problem is important because a small concentration of defects can dramatically affect the current transport in the device.

As previously mentioned, carbon is removed from the growing interface mainly as CO molecules. However, research suggests that small concentrations of carbons inject into the SiC channel, forming split interstitial defects.[42] These electrically active defects may be one source limiting the mobility of SiC MOS transistors. Medium energy ion

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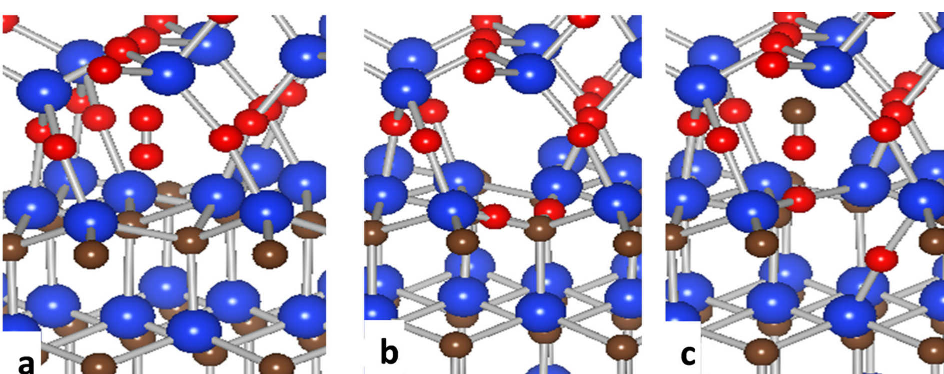

FIG. 3. The oxidation of SiC is illustrated with ball-and-stick models. Blue balls are silicon atoms, brown balls are carbon atoms, and red balls are oxygen. Panel (a) shows an O_2 molecule approaching the SiC-Oxide interface. Panel (b) shows O_2 breaking apart at interface to form stronger Si–O and C–O bonds. Panel (c) shows the structure after a CO molecule is emitted leaving behind a V_CO_2 complex in SiC.

scattering studies indicate that any excess C has a surface concentration less than $1.8 \times 10^{14}\,\mathrm{cm}^{-2}$ from the oxide surface down to a few monolayers beneath the SiC/SiO_2 interface,[43] although fewer electrically active defects may be required to reduce mobility. Modic *et al.*[44] explored the relation between carbon release and its electrical effect. To minimize thermal oxidation that consumes SiC and releases carbon, the standard NO annealing (which includes partial-pressure oxidation from NO decomposition at high temperature) was replaced by a nitrogen plasma processing for interface passivation; and instead of thermally grown thick gate oxide at 1150 °C, SiO_2 film deposited at low temperature was used. Electrical tests indicated that the D_{it} is lower than that obtained by NO annealing, but mobility was not improved.[44] This implies that interstitial C released from oxidation at 1150–1175 °C may not be the limiting factor for mobility. However, the concentration of C interstitials was not directly measured and could be higher than presumed. For instance, thermal oxidation was still used to grow the first 15 nm oxide at interface before the plasma treatment which may have released sufficient amount of C interstitials. This effect may also be conditional upon temperature. At higher temperature, e.g., 1300 °C and above, C may play a different and perhaps a bigger role, as discussed below in Sec. IV D.

Another important mobility limiting defect is the unpassivated carbon vacancy in SiC. Figure 3(c) illustrates an oxygen passivated carbon vacancy. Unpassivated carbon vacancies are present in SiC MOS directly at the SiC-Oxide interface. Equivalently, these defects are oxygen vacancies in the oxide just above the SiC channel. Regardless of the naming convention, the strained Si-Si bonds of the defect at the SiC/oxide interface are spectroscopically similar to the E'(delta) defect observed by electron spin resonance (ESR) in Si MOS.[45] E' defects have also been observed in radiation damaged oxides on SiC.[46] It is important to recognize that the V_CO_2 complex shown in Figure 3(c) is electrically inactive and represents a proper SiO_2 bonding unit. However, the density of Si in the V_CO_2 complex shown is close to double the density of Si in the oxide. Therefore, strain builds up in the growing interface and point defect formation becomes an energetically favorable mechanism for relieving strain. Si vacancies in SiC would naturally relieve the cross-interface Si bond density strain. Indeed, near interfacial Si vacancies have been observed with ESR.[45]

A very important class of interface defects is the so-called near interface traps (NITs) which are found in both Si and SiC MOS.[47] These traps are found in the oxide very near the interface and are responsible for the high concentration of neutral defect states within <0.2 eV of the SiC conduction band.[47–49] Since most SiC MOSFETs are n-channel (carriers are electrons), these NITs are particularly important for limiting the mobility of typical SiC MOSFETs. Reduction of NITs is strongly correlated with electron mobility improvements.[50] The NITs are intrinsic oxide traps since they occur in both Si and SiC MOS.[47,49] Comparing experiments with density functional calculations, new oxide defects have been proposed as the NIT electron trap candidates, including Si interstitials[51] and strained Si bonds.[52] Another candidate is the oxygen vacancy, which is well known to cause E' defects[53,54] and gate leakage[54–56] in Si MOS. Currently, there is no definitive microscopic model for NITs.

C. Nitridation of SiO_2/SiC interface

Since the discovery that NO annealing improves the SiC MOSFET performance, there have been numerous efforts to explain the atomic scale mechanisms. Macroscopically, experiments show (see Figure 4) that for channel field-effect mobility values up to about 50 cm^2/V s, the mobility is

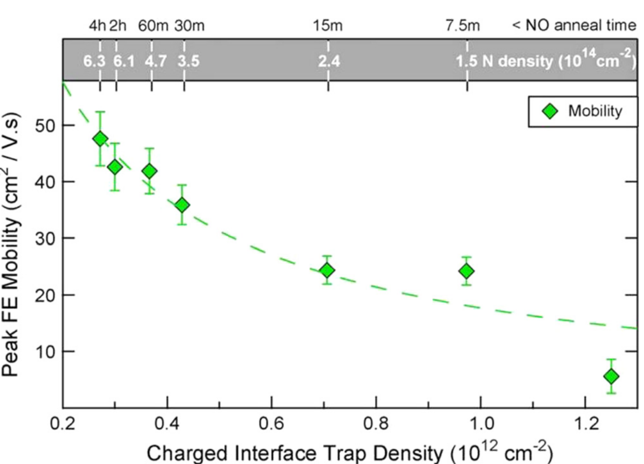

FIG. 4. Peak field-effect mobility is plotted as a function of various NO annealing times (upper horizontal axis), which yield distinct densities of charged interface states (lower axis) in the ON-state of the MOSFETs. The N density at the interface is measured by SIMS. Reproduced with permission from Rozen *et al.*, IEEE Trans. Electron Devices **58**(11), 3808–3811 (2011). Copyright 2011 IEEE.

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limited by electron trapping in interface states near the conduction band edge. The introduction of N at the interface via an NO annealing reduces D_{it} and increases mobility. These changes are monotonic with the concentration of interfacial N varied by annealing time.[57] However, depending on crystal faces and annealing temperature, N content always saturates at levels that are less than a monolayer.[58] Simultaneous high-low frequency capacitance-voltage (hi-lo CV) was used to extract the D_{it} in these studies. As will be discussed more in Sec. IV G, this technique is not able to detect the trapping by the "fast states,"[59] thus the observed values are lower than the actual values. Nevertheless, the relative correlation between D_{it} and N as well as mobility is still valid.

Deep Level Transient Spectroscopy (DLTS) can detect both traps near the insulator/semiconductor interface and in the bulk semiconductor. DLTS spectra taken in constant capacitance mode (CCDLTS) as shown in Figure 5(a) indicate that NO annealing significantly reduces the two overlapping broad trap distributions centered at $E_C - 0.15$ eV (O1) and $E_C - 0.39$ eV (O2), which exist in the as-oxidized interface (i.e., without nitridation). In Figure 5(b), the density of the traps from CCDLTS measurements is plotted as a function of the NO-annealing time, with the corresponding interfacial nitrogen areal density plotted as well. The data clearly show that the decrease in trap density is correlated to the increase in interfacial N. Notice that the interfacial N density is two orders of magnitude larger than the decrease in D_{It},[60] which indicate that: (i) not all nitrogen atoms are involved in passivation of dangling bonds or (ii) the near-interfacial oxide is converted to a ultra-thin oxy-nitride layer.

During NO annealing, the NO molecular bond breaks creating a free oxygen that results in further growth of the oxide, creating a new interface. XPS experiments indicate that, after NO annealing or other nitridation processes, N is mainly bonded within less than a nanometer of the interface forming an oxynitride interlayer between SiC and the amorphous oxide.[40,61] While the majority of nitrogen atoms bond to three silicon atoms, a few percent of the N atoms may be in other bonding environments.[40] Indeed, ESR experiments indicate that annealing oxidized SiC in NO results in $\sim 10^{12}\,cm^{-3}$ N atoms substituting for C in the SiC channel.[62,63]

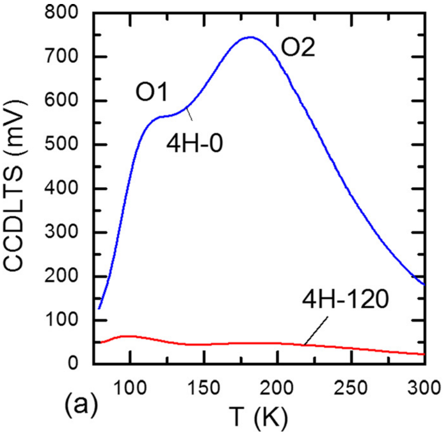
The theoretical understanding of interfacial nitridation in SiC MOSFETs has been developed over several years.[48,50,64] Early experiments indicated the main effect of NO annealing was to reduce near-interfacial oxide traps.[46] Later, NO anneals were also observed to reduce carbon related defects on the SiC side of the oxide-channel interface.[50] Subsequent research has confirmed these early results.[64,65] Theoretical calculations have elucidated the passivation of threefold-coordinated carbon atoms by nitrogen.[64] The reduction of NITs by NO has also been recently explained in terms of the counter doping effect.[48] This latter point will be discussed more in Sec. V B. Although significant progress has been made toward understanding the microscopic behavior of N within the MOS structure, a complete theory is not yet established.

III. PRESENT CHALLENGES—MOBILITY AND STABILITY

From the technological perspective, the wide spread adoption of SiC power MOSFETs has been hindered by high device costs, application design inertia, and proof of reliability. The two main technical challenges related to the MOS interface, which can have a significant impact on device cost, are (a) obtaining higher channel mobility and (b) improving the stability of the device under operating conditions. These interconnected issues are discussed in detail below.

A. Higher mobility

In a power MOSFET, for a given blocking voltage, it is desirable to have the minimal on-resistance, to reduce the conduction loss in the on-state. As mentioned in Sec. I B, the specific on-state resistance $R_{ON,SP} = R_{Ch} + R_a + R_J + R_{Spread} + R_{drift} + R_{sub} + R_C$, where, in principle, only R_{drift} scales with blocking voltage (Eq. (1)). At high voltage ratings, R_{drift} is large, and the current technology has successfully approached the theoretical limit $R_{ON,SP} \approx R_{drift}$, which is limited by the fundamental material properties of SiC. However, at ratings less than around 1700 V, R_{Drift} becomes comparable to other components and R_{Ch} becomes the limiting factor (see Figure 2). In the power electronics market, this voltage range consists of critical applications such as automotive/HEV, PV inverters, and power supplies and UPS. Therefore, there is a strong demand for higher mobility devices beyond the present NO annealed MOSFETs, especially to expand



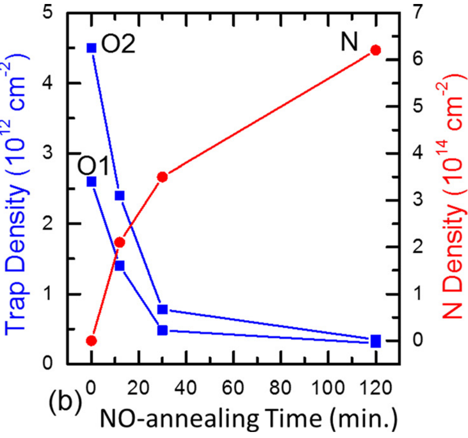


FIG. 5. (a) Saturated CCDLTS spectra for as-oxidized and NO-annealed 4H-SiC capacitors showing two broad peaks corresponding to near-interface oxide traps. The emission rate is $465.1\,s^{-1}$. (b) Interfacial N density and near-interface oxide trap density plotted vs. NO-annealing time. From P. M. Mooney and A. F. Basile, *Micro and Nanoelectronics: Emerging Device Challenges and Solution*. Copyright 2014 CRC Press, Taylor and Francis Group. Reproduced with permission from IEEE.

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SiC MOSFETs into the <600 V market. And undoubtedly, the new high mobility devices must also have excellent stability, to be practically beneficial.

In addition to reach the ideal R_{ON}, a better mobility can benefit many other design aspects for SiC MOSFETs. For instance, to reach the same drain current, the gate can be driven with a smaller voltage, resulting in smaller oxide electric fields. This improves both threshold stability and oxide reliability, as both are strongly dependent on the oxide electric field. In addition, in the current technology, shrinking the channel length is the main method to improve the channel resistance. However, this gives rise to the detrimental "short-channel effects,"[66] i.e., the punch-through behavior and the degradation of threshold voltage and the deterioration of sub-threshold characteristics. All of these problems can be mitigated by a higher mobility device structure, as longer channel length could be afforded, for the same channel resistance.

For developments of more complex MOS power device structures, other requirements besides high inversion channel mobility are needed. The IGBT is a hybrid MOS–bipolar power devices structure.[9] The cross section of a fabricated 4H-SiC n-IGBT is shown in Figure 6. Its bipolar operation enables drift layer conductivity modulation, resulting in lower conduction losses. The MOS structure brings in voltage-controlled gate that significantly simplifies the gate drive circuit, as well as a higher operating junction temperature due to the unipolar device's positive temperature coefficient for on-resistance. Therefore, the high voltage 4H-SiC IGBTs are desirable and are expected to play an important role in future high-power compact energy conversion and power grid systems, especially at blocking voltage ratings higher than 10 kV.[67] The carrier lifetime in lightly doped epi layers that are often hundreds of microns thick is a critical property, which determines the performance of bipolar devices. Therefore, to ensure optimal performance on both MOS and bipolar sides, the MOS interface passivation must have minimal negative impact to minority carrier life-times, in addition to provide excellent channel mobility and reliability. Such requirements may be relevant even for DMOSFETs, which has a parasitic "body diode" at the junction of p well and n drift layer in Figure 1, reversely placed between drain and source. Use of this diode is often not recommended due to its high and increasing forward drop over time. If this conduction degradation can be eliminated, the intrinsic body diodes can replace the external Schottky Barrier Diode (SBD) in inverters/converters modules with the switching characteristics maintained and lower cost.[68] To achieve long carrier lifetimes for effective conductivity modulation, identification of lifetime killers and their reduction are essential. The $Z_{1/2}$ center is a C vacancy defect (0.67 eV below conduction band edge)[69] that has been identified as one of the lifetime killers in n-type epi, which can be healed by thermal oxidation in oxygen.[70] However, oxidation in O_2, N_2O, or NO that are routinely used in SiC MOSFET fabrications is also found to generate other deep levels in the bulk epi layers: such as the so-called ON1 ($E_C - 0.84$ eV) and ON2 ($E_C - 1.1$ eV) centers.[71] Although the relation of these ON1,2 defects to lifetime is still not clear, these new defects illustrate that some processing steps may have unexpected effects.

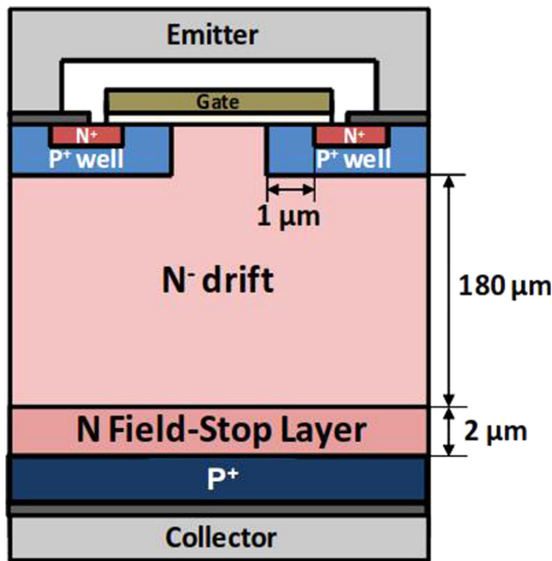

FIG. 6. Cross section of 4H-SiC n-IGBT. Reproduced with permission from E. V. Brunt *et al.*, "22 kV, 1 cm^2, 4H-SiC n-IGBTs with improved conductivity modulation," in *IEEE 26th International Symposium on Power Semiconductor Devices & IC's* (*ISPSD*) (2014), pp. 358–361. Copyright 2014 IEEE.

B. Gate stability

Even with the successful introduction of SiC power MOSFETs into the commercial market, several key reliability issues have not been fully resolved.[72] The bias and temperature-induced instability (BTI) of threshold voltage (V_{th}) is one major reliability problem. Typically, in SiC MOS devices, a positive-bias stress shifts V_{th} to more positive values, while a negative-bias stress shifts V_{th} negatively. The net V_{th} shift, or ΔV_{th}, measured after stressing the device with both gate voltage polarities in succession is typically used as a measure of overall BTI.[72,73] However, it is often useful to further define the shifts by individual polarity, namely, NBTI and PBTI for positive and negative BTI, respectively, as their individual magnitudes and importance to a device's functionality may vary. Although different types of interfacial charge are present either in the insulating gate oxide or at its interface with the SiC conduction channel—including interface traps and mobile ions—the primary defects attributed to the instability effects are the near-interfacial oxide traps.[73] The nature of these related defects is further discussed in Sec. V C. As noted before, current commercial power MOSFETs are generally annealed in NO. Using ΔV_{th} as the measure, it has been determined that NO annealing improves threshold voltage instability compared to as-oxidized devices.[74] However, experimental studies have shown that nitridation dramatically improves PBTI while at the same time degrades NBTI, although the net shift is still smaller than devices without NO passivation. In other words, electron trapping is decreased and hole trapping is increased with interfacial nitridation.[46,75] Normally off or enhancement mode operation is one of the most desirable features for a practical power switch. Excessive and

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uncontrolled NBTI may cause a device to become normally on, which may lead to catastrophic power system failure. Therefore, the fundamental issue of hole trapping in NO annealed oxide needs to be resolved.

Candidate engineered interfaces that yield "beyond NO" mobility need to be evaluated for BTI. The threshold voltage instability of Phosphorus OxyChloride ($POCl_3$) annealed MOSFETs has recently been reported by Yano *et al*.[76] Higher mobility in conjunction with reduced shifts was observed compared to NO annealed devices, which is extremely encouraging. To find a competitive replacement for NO, BTI studies for other high mobility candidates are needed as well.

In addition, a large V_{th} of about ~5 V is needed in power switches to avoid accidental turn-on by drive circuit noise. Due to NBTI, an even larger V_{th} is needed to leave a margin for safe operation. Therefore, higher channel p-body doping (~10^{17} cm^{-3}) is typically used to increase V_{th}. The result is a significant reduction of inversion channel mobility,[77] which in turn increases the channel resistance and the specific on-resistance of the device. As a consequence, to achieve the rated high currents, larger SiC dies areas are needed, which leads to higher costs. Some of these issues can be alleviated if NBTI can be eliminated, which may significantly enhance device performance and cost reduction.

IV. RECENT PROGRESS 2010–2014

Recently, there has been encouraging research in SiC MOS processes beyond the standard NO interface treatment. The most promising channel engineering processes include introduction of interfacial layers with trace impurities, surface counter-doping, and higher temperature oxidations. Alternative non-polar crystal faces instead of the conventional polar Si-face are also attracting more attention due to their inherently high mobility. Such alternate faces are particularly important for trench MOSFET applications. Here, we briefly summarize the recent results of the channel engineering efforts. The possible underlying transport mechanisms for the improved mobility in each case are discussed in Sec. V B.

A. Phosphorus

High inversion layer mobility of ~75–100 cm^2/V s and lower D_{it} compared to NO annealing were achieved by Okamoto *et al*. by annealing thermally grown SiO_2 in $POCl_3$.[78] Subsequently, similar results were also reported by Sharma *et al*. using a SiP_2O_7 planar diffusion source (PDS).[79] Unfortunately, severe negative threshold voltage shift after positive bias, at elevated temperature, was observed. This is because P_2O_5 converts the SiO_2 layer to PhosphoSilicate Glass (PSG)—a polar material that introduces voltage instabilities which negate the benefits of lower interface trap density and higher mobility. In order to solve this problem, a stacked gate oxide structure consisting of a thin PSG interfacial layer (~1 nm) and a deposited oxide was proposed.[80] This led to a significant improvement in voltage stability while also maintaining high peak field effect mobilities, up to 72 cm^2/V s.

B. Metals in the oxide

The (initially unintentional) addition of sodium (Na) in the gate oxide has been found to yield an exceptionally high peak field effect mobility of about 170 cm^2/V s.[80] While the mobility is impressive, the devices suffer from the mobile ion effect, i.e., the sodium ions move within the gate oxide at typical operating temperatures and gate biases. Recently, Lichtenwalner *et al*. expanded the search to both group I and II metals, as shown in Figure 7.[81] They found that a thin barium (Ba) layer (~1 nm) deposited onto SiC, before oxide deposition and annealing can yield a peak field effect mobility of ~85 cm^2/V s on Si-face, without any noticeable mobile ion effect. In another study, Yang *et al*. demonstrated a peak field effect mobility of 133 cm^2/V s and high threshold voltage using an interfacial lanthanum silicate and top SiO_2 stack deposited by atomic layer deposition.[82] More recently, Okamoto *et al*. used a boron nitride planar diffusion source to introduce a high concentration (more than 10^{20} cm^{-3}) of boron atoms into the bulk oxide and interface of Si−face SiC, although N was inevitably also introduced to the interface as well, at a concentration of 10^{19} cm^{-3} near the interface. This treatment resulted in a reduced D_{it} and a peak field-effect mobility of ~100 cm^2/V s.[83] The effect was attributed to the passivation of interface states near the conduction band-edge of 4H-SiC by boron.

C. Surface/interfacial counter doping

Surface counter-doping refers to doping the surface of the MOSFET p-body with n-type dopants. We need to differentiate interfacial counter-doping discussed here from the bulk counter-doping, i.e., buried channel devices. The main difference is the depth of the counter doping layer which consequently leads to the distinct transport mechanisms. Buried channels are typically hundreds of nm deep into the semiconductor substrate. The resulting mobility can be high since transport of bulk carriers does not involve scattering from the interface.[84] However, the threshold voltage is typically negative and hard to control, making them undesirable

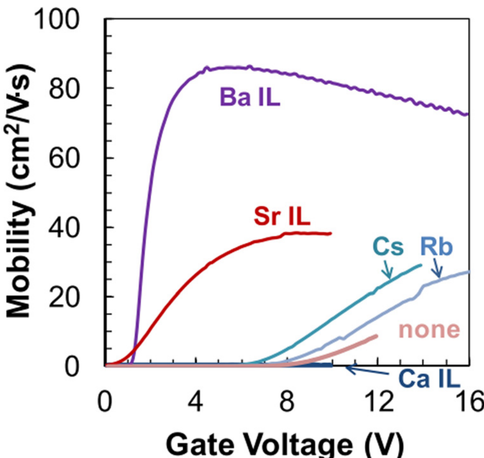

FIG. 7. Field-effect mobility with Rb, Cs, Ca, Sr, or Ba interface layers, compared to an unpassivated thermal oxide (labeled "none"). Reproduced with permission from Appl. Phys. Lett. **105**, 182107 (2014). Copyright 2014 AIP Publishing LLC.

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for power applications. In contrast, the interfacial counter doping depth is smaller, typically tens of nm or less, which is less than Debye length, and ideally involves a delta function doping profile. In principle, any group V element incorporated into SiC and activated should act as a donor and form a counter doped channel.

By using an antimony (Sb) doped layer with a depth of about ∼10 nm and forming the gate oxide with NO annealing, Modic *et al*. recently reported high channel mobility greater than 100 $cm^2/V\ s$ with a threshold voltage of about 1 V.[85] The Sb provides two advantages. First, the large Sb ion size helps to achieve the preferred delta function shaped doping profile via ion implantation, which can provide high mobility with least threshold voltage loss. The mechanism of such interfacial counter doping will be discussed more in Sec. V B 1. Second, Sb helps to distinguish the counter doping effect from the defect passivation effects, since Sb does not result in interface passivation unlike nitrogen and phosphorous. The significance of this work will be discussed in Sec. V B 2.

D. Interface improvement by high temperature thermal oxidation only

The mobility enhancement methods mentioned so far involve the addition of other elements to the SiO_2-SiC near-interface region. It has long been a goal to directly grow a defect-free interface without post-oxidation treatments. This effort traced back to 2006 when Kurimoto *et al*. reported that the interface trap density has a dependence on the thermal oxidation temperature.[86] Recently, there have been two major breakthroughs. By raising the oxidation temperature to above 1400 °C, Kikuchi and Kita observed a low D_{it}.[87] In another study, a channel mobility of 40 $cm^2/V\ s$ was reported by Thomas *et al*.[88] using an oxidation temperature of 1500 °C, but the device was normally on. The reduction of carbon precipitation at high temperature was speculated to be the mechanism causing the improvement.[88] However, carrier lifetime studies suggest that high temperature oxidation enhances interstitial C injection into SiC, which could potentially result in higher amount of scattering centers as well as traps in the SiC inversion channel.[72] More work is needed to establish the underlying mechanisms for mobility improvement using very high temperature oxidations.

E. Alternative crystal faces

Historically, the (0001) Si-face of 4H-SiC has been the most commonly used since it is commercially available in wafer form. However, there are other faces that could be used, including the polar $(000\bar{1})$ C-face and other non-polar faces, e.g., the $(11\bar{2}0)$ a-face and the $(1\bar{1}00)$ m-face, as illustrated in Figure 8. The surface atomic structure varies from face to face. While Si atoms terminate the Si-face SiC, the C-face is terminated by C atoms, and the non-polar faces, as the name suggests, have equal number of Si and C atoms. These different surface structures have unique properties that are distinct and often advantageous compared to the Si-face. The advantages include higher oxidation rates, and for

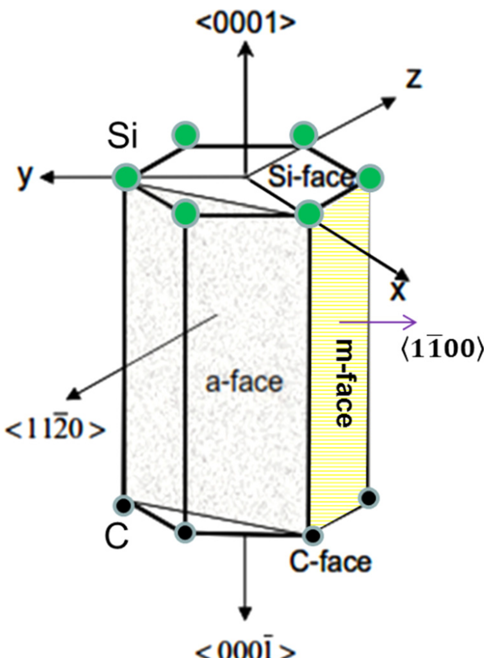

FIG. 8. Crystal faces in 4H-SiC. The Si-face is terminated by Si atoms (large green balls) and C-face by C atoms (small black balls). Non-polar faces, e.g., a-face and m-face, have equal number of Si and C atoms.

resulting devices: higher channel mobilities and higher threshold voltages.

Figure 9 shows that at 1150 °C, the C-face has the highest oxidation rate among the three SiC faces, closely followed by the a-face. The Si-face has the lowest rate, by a significant amount. For a typical oxide thickness of 50 nm, it takes more than 12 h to grow oxide on the Si-face, and less than 1 h for the other two faces.[89] Shen *et al*.[29] attributed the lower oxidation rate of SiC than Si to the different dominant oxidants. According to this work, the majority diffusing species in the oxide, i.e., O_2 molecules, is the dominant oxidant for pure Si. However, SiC has a smaller lattice constant so the interfacial oxide layer on the Si-face of SiC is denser than the oxide on top of Si (100). This dense oxide

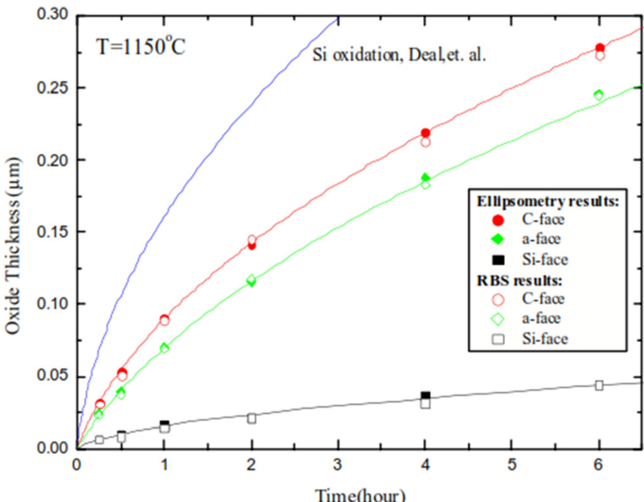

FIG. 9. a-face, Si-face, and C-face dry oxidation curves at 1150 °C, the solid symbols are ellipsometer results, and the opened symbols are Rutherford backscattering spectrometry (RBS) results.[89]

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filters out O_2 but allows through trace amounts of atomic oxygen resulting in a very low oxidation rate. The C-face of SiC has a high concentration of dangling bonds which are difficult to passivate during the oxidation of C-face SiC. The result is a high interface defect concentration that in turn enables molecular oxygen to be an effective oxidant again. This explains the higher oxidation rate of C-face SiC.

The significantly higher channel mobility on non-Si face devices has made them an alternative solution to the low mobility of the dominant Si-face devices. In 1999, Yano *et al.* reported $>25\,cm^2/V$ s field effect mobility on a-face, compared to the value of $<10\,cm^2/V$ s on Si-face devices, with the same wet oxidation and H_2 anneal.[90] Following that, many treatments and other faces have been evaluated, and record mobilities have been reported. On a-face, Senzaki *et al.* reported a peak mobility of $110\,cm^2/V$ s with hydrogen post oxidation annealing process,[91] and Endo *et al.* reported an even higher mobility with wet annealing.[92] Applying the NO annealing to $(03\bar{3}\bar{8})$ face, Hiyoshi *et al.* reported a channel mobility of $80\,cm^2/V$ s.[93]

In addition to high mobilities, the comparisons between Si-face and the alternative faces, with the same treatments, offer a unique way to better understand the underlying mechanisms. Recently, using an NO based process for the fabrication of a-face and m-face devices, Kimoto *et al.* reported a high channel mobility of $118\,cm^2/V$ s.[95] It has been suggested that the reason for the higher mobility in the non-polar face MOSFETs is the significantly lower "fast" interface trap density compared to the Si-face. ("Fast states" will be discussed in detail in Sec. IV G.) Liu *et al.* treated the a-face interface with phosphorus at 1000 °C and achieved a channel mobility of $125\,cm^2/V$ s, compared to $80\,cm^2/V$ s on Si-face, as shown in Figure 10.[94] However, the companion physical characterization intriguingly showed that the interfacial phosphorus coverage is actually lower on the a-face than on the Si-face, with similar bonding configurations. This, together with similar D_{it}, results inspired the concept of interfacial counter doping which was later experimentally verified and developed. The counter doping effect is discussed further in Sec. V B 1.

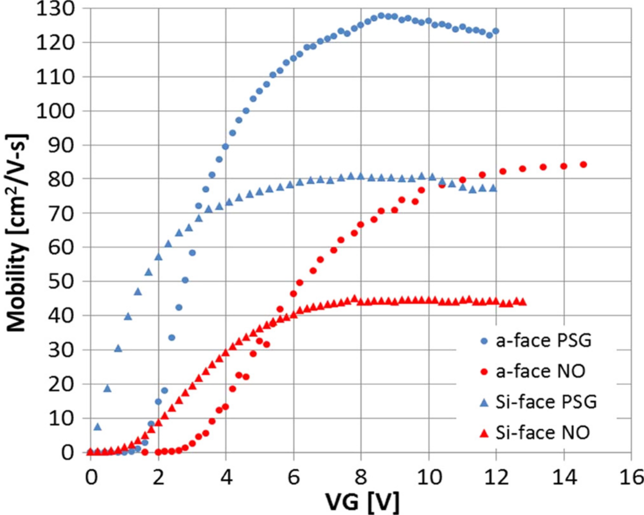

FIG. 10. Field effect mobility of n-channel MOSFETs made on (circles) a-face and (triangles) Si-face, with (blue filled) PSG and (red filled) NO anneal, respectively. Reproduced with permission from Liu *et al.*, IEEE Electron Device Lett. **34**(2), 181–183 (2013). Copyright 2013 IEEE.

Comparisons between C-face and Si-face also provide interesting insights into the interface treatment mechanisms. The dry oxidation and/or NO annealing that works reasonably well on Si-face and non-polar faces are less efficient on C-face both in terms of reducing interface trap density and improving mobility.[65] On the other hand, Okamoto *et al.* have shown that wet-oxidation can achieve better D_{it} and mobility in both n- and p-channels, and annealing in H_2 in addition to a wet re-oxidation (water) can further improve the n-channel mobility to as high as $90\,cm^2/V$ s on C-face.[96–98] However, these treatments have not worked very well on Si-face. Umeda *et al.* studied the differences between Si-face and C-face MOS interfaces using electrically detected magnetic resonance (EDMR) technique and found that there are different types and different amounts of interface defects on each interface.[99] Water absorption studies have recently confirmed that a substantial amount water related components were absorbed at the C-face/oxide interface.[100]

The dependence of the interfacial electrical properties on crystal faces is clearly illustrated by Yoshioka *et al.*,[101] as shown in Figure 11. Gate oxide processing by pyrogenic oxidation or nitridation yields distinctly different D_{it} and mobility on the three faces. The crystal face dependence of D_{it} in interfaces formed by pyrogenic oxidation can be explained by the corresponding strong face dependence of water absorption. Liu *et al.*[102] showed that oxides formed on the C- and a-faces absorb an order of magnitude more hydrogen at the interface than the Si-face, after water exposure to the oxide structure. This trend is consistent with the good D_{it} and mobility on C- and a-face but not on Si-face, after pyrogenic oxidation, as illustrated in Figure 11.

In most of the aforementioned reports, the non-polar face devices also have a higher threshold voltage, compared to Si-face which is extremely attractive for power devices. Along with the high oxidation rate and high mobility, the

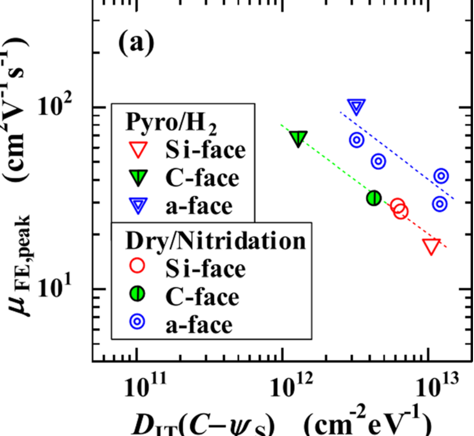

FIG. 11. Correlation between peak field-effect mobility in the ⊥[0001] direction evaluated using MOSFETs and D_{it} (C-ψ_s) at E_C-$E_T = 0.2$ eV evaluated using MOS capacitors. Reproduced with permission from Appl. Phys. Lett. **104**(8), 083516 (2014). Copyright 2014 AIP Publishing LLC.

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alternative faces are attractive candidates for SiC MOSFET applications. Of course, more work needs to be done on the materials development, oxide reliability, and stability for these crystal faces before devices derived from alternate faces can be competitive with the Si-face devices. Currently, research on the alternate crystal faces mainly rely on custom made materials since these crystal faces are not available commercially. However, understanding and engineering the MOS properties of the non-polar faces are extremely important for the development of next-generation SiC trench power MOSFETs, since these devices naturally employ a variety of faces.

F. Trench MOSFET

The trench MOSFET (or U MOSFET), shown in Figure 12, is a very desirable device design for next-generation SiC power MOSFETs. In these devices, the MOS inversion channel forms on the trench side-walls, nominally etched along non-polar crystal faces. Fundamentally, this device structure can carry higher current density compared to the DMOSFET due to the absence of the "JFET region" (refer to R_J in Figure 1) leading to smaller cell-pitches.[103] In addition, it can also take an advantage of higher mobility on the non-polar faces, as mentioned in Sec. IV E. The studies on planar epitaxial layers mentioned above set the limit on performance, as non-polar faces created by Reactive-ion etching (RIE) processes are typically not as good as epitaxial surfaces. Nevertheless, UMOSFETs formed by RIE with high mobilities have been reported.[104–106] Moreover, practical power trench MOSFETs have been demonstrated with superior current density when compared to DMOSFETs.[95]

It is very important to understand the nature of residual damage caused by RIE, as well as the damage recovery

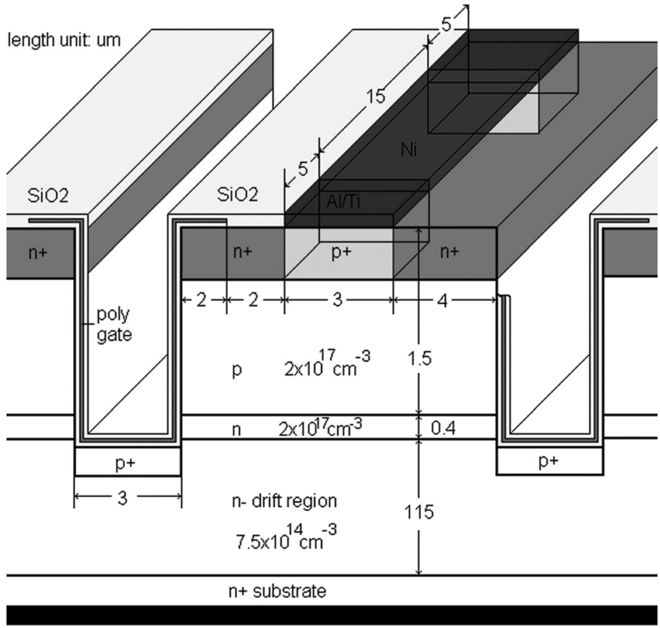

FIG. 12. Schematic cross section of the 4H-SiC trench MOSFET. Reproduced with permission from Sui *et al.*, IEEE Electron Device Lett. **26**(4), 255–257 (2005). Copyright 2005 IEEE.[107]

processes. In one of the first high power (100 A/cm^2, 5 kV) UMOSFET studies, atomic force microscopy (AFM) showed severe roughness on the sidewall after RIE. The roughness was not substantially reduced after sacrificial oxidation.[108] A H_2 etching process with hydrogen gas flow at $\sim$1400 °C has been shown to be effective for obtaining smoother surface morphology after RIE.[109] Residual point defects in SiC epitaxial layers before and after RIE post-annealing have also been studied by Kawahara *et al.*[110]

In a recent study, the effects of RIE processing on SiC a-face MOSFETs and their recovery by H_2 etching were established by combining electrical and physical analysis. It was demonstrated that RIE introduces severe surface roughness and causes serious damage to the surface crystal structure. Thermal oxidation consumes most of the damage in the near surface epitaxial region. However, surface roughness remains and causes a large negative flat band voltage and early oxide breakdown. The field effect mobility in the RIE processed MOSFET is very low, which is likely limited by the high defect density and the large surface roughness. An H_2 etch results in recovery of the surface flatness and improves the device performance. Capacitance-voltage measurements indicate higher D_{it} than without RIE. DLTS has confirmed the higher D_{it} at the interface and identifies three types of residual defects in the epitaxial layer. Most importantly, the MOSFET channel mobility is substantially recovered to a value only slightly lower than devices without RIE. This study suggests that proper processing of a-face trench walls can produce high channel mobility in UMOSFETs.[111]

G. Electrical characterization of the SiC-SiO_2 interface

There are various techniques to measure the interface trap density (D_{it}), most of which are based on measuring the A.C. admittance of simple MOS capacitor structures. Some of the popular methods for MOS capacitor characterization are simultaneous quasi-static and high-frequency capacitance and conductance measurements on MOS capacitors, charge pumping and sub-threshold current measurements on MOSFETs.[112] For characterization of traps near the band-edge, which is most relevant for SiC, the simultaneous high-low frequency CV technique has been the most popular.

The sum of the semiconductor capacitance and the interface-state capacitance ($C_D + C_{IT}$) can be measured from a MOS capacitor. From C_{IT}, one can calculate D_{it}. To isolate the value of C_{IT}, the high-low method probes the capacitor with two different frequencies, the quasi-static and the high frequency (0.1 or 1 MHz). There are three assumptions: (1) C_D remains the same for all frequencies; (2) the quasi-static is slow enough to let all traps of different time constants to response, i.e., measuring ($C_D + C_{IT}$); and (3) the high frequency is too high for any traps to response, as a result, measuring only C_D. Therefore, by comparing the results measured by these two frequencies, C_{IT} and D_{it} can be calculated.[113]

However, as shown in Figure 13, Yoshioka *et al.*[59] found that the measured capacitances are still dependent on the frequencies that are higher than the "high frequency"

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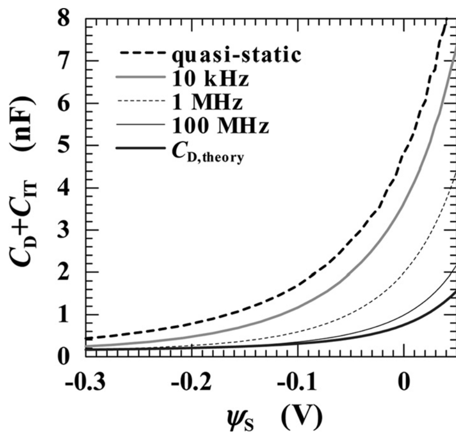

FIG. 13. $C_D + C_{IT}$ (semiconductor capacitance and the interface-state capacitance) versus surface potential (ψ_s) at various frequencies for an n-type Si-face SiC MOS capacitor, with dry oxidation at 1300 °C, without post-oxidation anneal. Reproduced with permission from J. Appl. Phys. **111**(1), 5 (2012). Copyright 2012 AIP Publishing LLC.

(0.1 or 1 MHz) typically used in high-low method. Assuming C_D remains the same for all frequencies, the measured capacitance by "high frequency" apparently includes not only C_D but also some interface-states that are fast enough to response to the probing frequencies. As a result, by subtracting the capacitance values of these two frequencies, the high-low D_{it} fails to include those fast states and underestimates the density of traps.[59] To solve this problem, Yoshioka *et al*. proposed to replace the high frequency capacitance with a theoretically calculated capacitance $C_{D,theory}$ that does not contain any interface states. And this so-called "C–ψ_s" technique can monitor the very fast interface states that are missed by the conventional method.[59]

Applying this technique, it was reported that nitridation generates large amount of very fast interface states for Si-face SiC,[114] but much less for the (11$\bar{2}$0) and (1$\bar{1}$00) faces.[115] The monotonic correlation between the field-effect mobility and C-ψ_s N_{it} (integrated D_{it}) across (0001), (11$\bar{2}$0), and (1$\bar{1}$00) faces has also been demonstrated in one report.[115] However, this correlation was not observed in another student where the (0001), (000$\bar{1}$), and (11$\bar{2}$0) faces were compared.[101] The reason for such variation is discussed more in Sec. V A 2.

One critical limitation of both the high-low technique and C-ψ_s method is that uniform doping profile is assumed for the calculation of surface potential. However, as discussed in Secs. IV C and V B 1, many interface treatments introduce an interfacial counter-doping layer. As a result, doping profiles near the interface become complex and non-uniform. This factor may severely affect the calculation surface potential required to extract the D_{it} as a function of energy in the SiC band-gap. Therefore, an analysis technique that can account for such doping profile complexity will be very desirable.

In addition to the C-ψ_s method that can evaluate the total density of interface states, including fast states, a new conductance method has been introduced to characterize the properties of these states. Since the response frequency of interface states is lowered with decreasing temperature, Yoshioka *et al*. studied the interface state peaks near the conduction band edge by a low temperature conductance method. In this method, the defect density was evaluated from G_{PIT}/ω against frequency, where G_{PIT} is the interface state conductance extracted from the measured impedance, while the defect energy level was evaluated by an Arrhenius analysis.[116]

V. FUNDAMENTAL ASPECTS OF THE PROBLEMS

To overcome the channel mobility and stability problems, it is important to understand the underlying fundamental mechanisms. The recent encouraging progress with novel interface engineering, high mobilities, and better characterization techniques provides more information that could be put together to establish the mechanisms related to the mobility and stability problems. There are two general questions related to mobility: (a) What are the channel mobility limiting factors on 4H-SiC? and (b) What are the mobility improvement mechanisms?

A. Mobility limiting factors

To tackle the questions related to mobility, we first briefly review the established channel mobility limiting factors for Si MOSFETs with thick gate oxides. As depicted in Figure 14, there are three major mechanisms that limit the mobility: coulomb scattering, phonon scattering, and roughness scattering, with the total mobility given by their reciprocal sum based on Matthiesen's rule

$$\mu_{Inv}^{-1} = \mu_C^{-1} + \mu_{Ph}^{-1} + \mu_{Sr}^{-1}. \quad (2)$$

Each mechanism becomes the limiting factor in different regimes and each has a unique dependence on temperature. The mobility is also strongly dependent on the transverse effective field, E_{eff}, which is perpendicular to the plane of inversion channel. E_{eff} is defined as

$$E_{eff} = (Q_{inv}/\gamma + Q_B)/\epsilon_s, \quad (3)$$

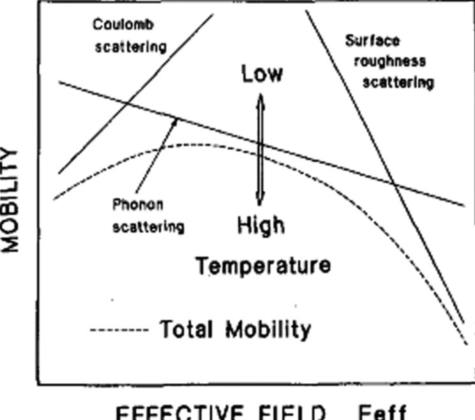

FIG. 14. Schematic of major scattering mechanisms in universal mobility curve on n-channel Si MOSFET. Reproduced with permission from Takagi *et al*., IEEE Trans. Electron Devices **41**(12), 2357–2362 (1994). Copyright 1994 IEEE.

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where Q_{inv} is inversion carrier charge density, Q_B is the depletion region charge density, and the empirical factor γ is 2 for electrons and 3 for holes, based on experimental data.[117] The mobility dependence on E_{eff} and temperature in Si MOSFETs is schematically depicted in Figure 14, also known as the "universal mobility" curve.

According to the "universal mobility" model of Si MOSFETs, Coulomb scattering from traps and ionized impurities is dominant when channel carrier concentration is low, which typically occurs at low effective field. In this case, mobility increases with decreasing scattering centers (N_{it}) and increasing temperature and carrier concentration. This is typically modeled by the following relation: $\mu_c \propto N_{it}^{-1} \times T \times n_s{}^{\xi}$.[117] As the inversion carrier concentration gets high enough to screen the coulomb scattering centers, corresponding to the medium effective field, phonon scattering begins to dominate. In this regime, the mobility decreases with temperature and effective field or carrier concentration. In this regime, the phonon mobility is semi-empirically modeled by the relation: $\mu_{Ph} \propto E_{eff}^{-\alpha} \times T^{-\beta}$.[117] As the effective field gets even stronger, the width of the inversion channel decreases to ~1 nm, and as the electron distribution gets squeezed closer to the interface, surface roughness scattering becomes dominant, and mobility decreases with effective field quickly, where the surface roughness mobility $\mu_{Sr} \propto E_{eff}^{-\gamma}$.[117]

Practically, there are several ways to measure and extract values of μ_{inv}. Here, we will discuss the following mobilities (i) *effective mobility* (μ_{eff}), (ii) *field effect mobility* (μ_{FE}), and (iii) *Hall effect mobility* (μ_{Hall}). The μ_{eff} is derived from source-drain conductance measurements[118]

$$\mu_{eff} = \frac{(L/W)}{C_{ox}(V_G - V_T)} \left(\frac{dI_D}{dV_D} \right) \bigg|_{V_D \to 0}, \tag{4}$$

where L and W are the length and width of channel, Cox is the gate capacitance per unit area, I_D is drain current, V_G and V_D are the voltages on the gate and drain electrodes, and V_T is threshold voltage.

The μ_{FE} is obtained from the drain-gate transconductance[118]

$$\mu_{FE} = \frac{(L/W)}{C_{ox} V_D} \left(\frac{dI_D}{dV_G} \right) \bigg|_{V_D \to 0}. \tag{5}$$

The μ_{Hall} is the most accurate mobility value, because it is calculated from the sheet resistance R_s and the inversion sheet charge density N_{inv}, both of which are measured separately[112]

$$\mu_{Hall} = \frac{1}{qN_{inv}R_s}. \tag{6}$$

However, one drawback of Hall measurements lies in the more complex device fabrication.

Comparing the three methods, the μ_{eff} and μ_{FE} yield similar peak mobility, while μ_{FE} underestimates mobility at higher field.[118] And from Figure 15, we can see that both μ_{eff} and μ_{FE} underestimate the peak mobility compared to μ_{Hall}.[119]

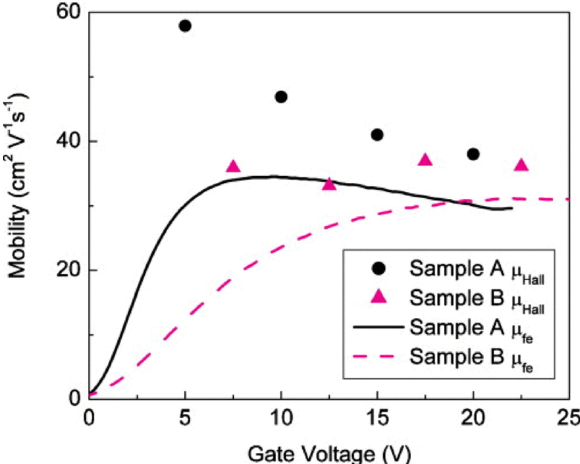

FIG. 15. Field-effect mobility and Hall mobility for samples with NO annealing at 1175 °C for sample A and 1300 °C for sample B. Reproduced with permission from J. Appl. Phys. **108**(5), 054509 (2010). Copyright 2010 AIP Publishing LLC.

1. Coulomb scattering/temperature dependence

In the state-of-the-art Si-face 4H-SiC MOSFETs with nitrided gate oxides, loss of carriers by trapping does not play a significant role in the current reduction under heavy inversion conditions, as indicated in Figure 16. Rather, it is the low carrier mobility that limits the channel current.[119] This is contrary to interfaces without nitridation where the transport is completely dominated by trapping. Coulomb scattering at low field and surface roughness scattering at high field are believed to limit surface mobility for a wide range of temperatures. Consistent with Coulomb scattering, the peak mobility of NO annealed devices increases with temperature,[120,121] as shown in Figure 17. At temperatures above about 100 °C, the mobility starts decreasing gradually with temperature as phonon scattering dominates Coulomb scattering at these higher temperatures.

2. Phonon scattering/temperature dependence

As summarized in Table II, it has been observed that the high mobility interfaces (>50 cm^2/V s) collectively have the negative mobility temperature dependency, which is the signature of phonon scattering. However, there are other high mobility reports where the temperature dependency information is missing. More studies are needed to firmly establish temperature dependence of the mobility for the novel interface engineering processes.

The evolution of the temperature dependence is perfectly captured by Yang *et al.*, in their lanthanum silicate work that was mentioned in the last section. As Figure 18 shows, an oxide deposited using atomic layer deposition yields a low mobility interface, presumably due to high D_{it}. As a result, the mobility increases with temperature, which is a signature of coulomb scattering, as mentioned earlier. On the other hand, for the lanthanum silicate interfaces, very high mobilities are observed which has a distinctly opposite temperature dependence, indicating phonon scattering. The interesting intermediate case is shown in green diamonds symbols. It appears to have a negative but relatively weak

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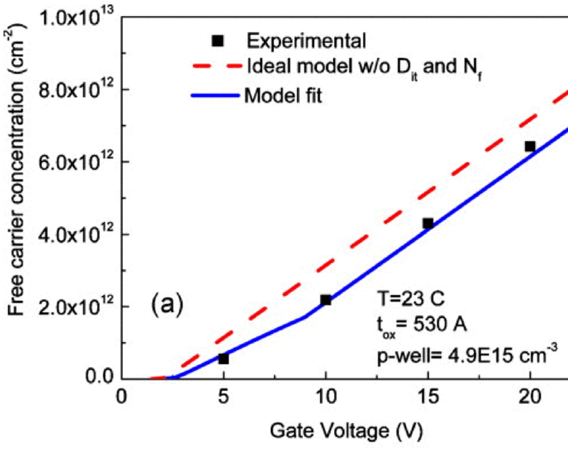

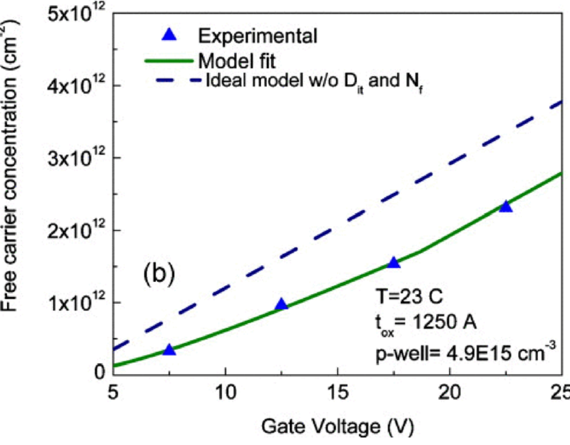

FIG. 16. Free carrier concentration as a function of gate voltage for NO annealed sample. Points represent Hall measurements, dashed line is ideal charge-sheet model, and solid line represents model fit to the data. Reproduced with permission from J. Appl. Phys. **108**(5), 054509 (2010). Copyright 2010 AIP Publishing LLC.

temperature dependence. This is an indication of combined effect of both coulomb and phonon scattering.

The temperature dependency power factor-β in Table II, which varies with processing, is always lower than that in the

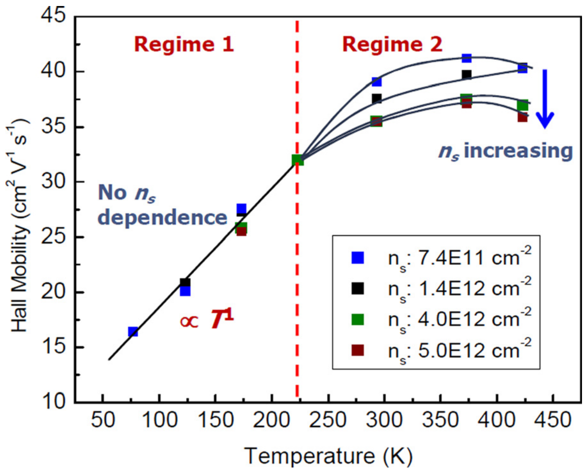

FIG. 17. Temperature dependence of NO annealed sample field effect mobility for different channel electron sheet densities. Reproduced with permission from Dhar *et al.*, *Silicon Carbide and Related Materials 2011, Pts. 1 and 2*. Copyright 2012 Trans Tech Publications, Inc.[122]

TABLE II. Peak field-effect mobility (μ_{pk}) temperature (T in unit K) dependence, $\mu_{pk} \propto T^{-\beta}$.

Crystal face	Process	μ_{pk} (cm^2/V s)	p-well doping (cm^{-3})	$-\beta$	References
(0001)	$LaSiO_x$	130	NA	**−0.9** to **−2.8**	82
(0001)	Sb + NO	110	6×10^{15}	**−0.8** to **−1.6**	85
(0001)	$POCl_3$	108	1×10^{17}	**−0.7** to **−1.5**	123
(0001)	Ba	85	5×10^{15}	**−1**	81
$(03\bar{3}\bar{8})$	NO	90	3×10^{16}	**−1.5**	93

bulk SiC semiconductor, −2.1 for 4H-SiC. A similar situation exists for Si, where the power factor is −1.5 in inversion channel and −2.4 in the bulk Si.

A phonon scattering limited mobility is not contradictory to its positive correlation with the total amount of interface traps, N_{it}. Only after N_{it} is significantly reduced, the coulomb scattering mobility component μ_C^{-1} becomes small enough, resulting in either the phonon scattering μ_{Ph}^{-1} or roughness scattering component μ_{Sr}^{-1} to be the new limiting factor. In such a regime, further improvement of N_{it} may no longer affect the peak mobility. This is in agreement with the scattered mobility-N_{it} relations in literature, as mentioned above in Sec. IV G. Nevertheless, lower N_{it} may be beneficial to bias temperature induced instability, by reducing the near-interface states from which trapped carriers can tunnel into the oxide traps.

3. Surface roughness/effective field dependence

As in the case of Si MOSFETs, the reduction of mobility at high transverse field for SiC has also been attributed to surface roughness scattering. Figure 19 shows the field-effect mobility as a function of gate voltage for different channel engineering schemes; the details of which are provided in the figure caption. Interestingly, despite various interface treatments, the mobility of the various devices converges at high field. Notice that such channel mobility value (μ) corresponds to the electron mean free path (λ_m) of less than 1 nm, calculated by[124]

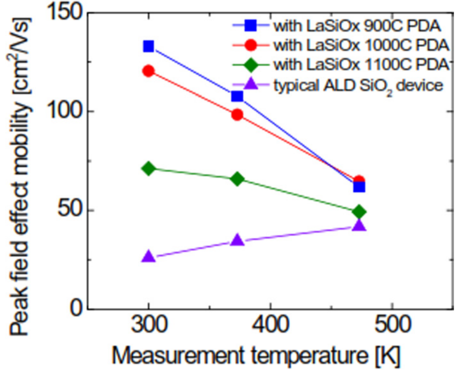

FIG. 18. Peak Mobility-temperature dependence in MOSFETs with different interface conditions. Reproduced with permission from Yang *et al.*, "Effect of post deposition annealing for high mobility 4H-SiC MOSFET utilizing lanthanum silicate and atomic layer deposited SiO2," in the 2nd IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA) (2014). Copyright 2014 IEEE.

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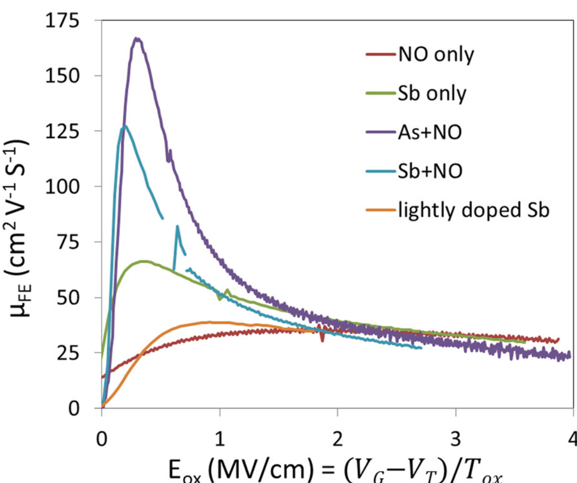

FIG. 19. Field effect mobility with various interface treatments, including NO post-oxidation annealing, thin counter-doped channel layers with Sb (lightly and heavily doped), As only, and As or Sb in combination with NO. The mobility is tested at room temperature with high gate field.[125]

$$\lambda_m = \frac{m^* v_{th}}{q} \mu, \tag{7}$$

where the effective mass of an electron in SiC $m^* = 2.73 \times 10^{-31}$ kg ($0.3\,m_e$), the thermal velocity $v_{th} = 2 \times 10^7$ cm/s, and the charge of an electron $q = 1.60 \times 10^{-19}$ C. Conventional AFM scan spatial resolutions are typically limited to the order of nanometers; therefore, it is difficult to correlate mobility to the surface roughness measured by this technique.

High-resolution transmission electron microscopy (HRTEM) is a very powerful tool for this purpose. From the 3D atomic structure of the vicinal interface image in Figure 20, one can clearly see that the vicinal surface is not as flat as the ideal case. Steps of the vicinal interface are not always straight. In contrast, kinks are very common and widely distributed on the steps, protruding in and out of the terraces. This observed interface roughness could be responsible for limiting the mobility at high effective field range.[126]

B. Mobility improvement mechanisms

The atomic scale mechanisms for the various interface treatments for mobility enhancement share common features. As discussed in Sec. II, the interface trap density is caused by defects that exist in the near interface region, including at the oxide and SiC epitaxial layer. Generally speaking, there are two ways to reduce the trap density. One way is to physically annihilate those defects, either by optimized defect-free interface formation processes or by chemical passivation of the defects after interface formation. The resulting defect density, electrical trap density, and mobility are all improved from a MOSFET perspective. It is believed that one of the major roles of nitrogen at the SiO_2/SiC interface is to directly passivate the interface defects, i.e., nitrogen chemically bonds with atoms which causes the formation of bonding and anti-bonding states that are removed from the band gap. Another way to improve device performance is to leave the defects physically intact at the interface, yet indirectly

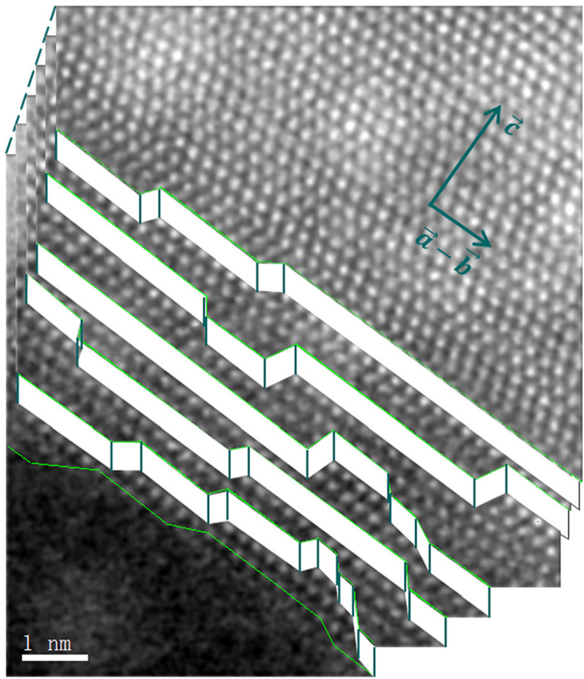

FIG. 20. A 3D atomic structure of the vicinal interface was reconstructed from the through focal Z-contrast image series. The interface structure consists of six frames. In each frame, the SiO_2, at the lower left corner, was set to be transparent, and the edges of the steps are highlighted with green lines. The focus increment was 40 Å, and the steps of the vicinal interface appeared sequentially with every changed focus. Reproduced with permission from Liu *et al.*, J. Vac. Sci. Technol., A **32**(6), 060603 (2014). Copyright 2014 IEEE.

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annihilate their detrimental electrical effects to the inversion channel. The resulting defect density remains the same; however, N_{it} and mobility are both improved. Interfacial counter doping, discussed below, is such a mechanism and is mainly responsible for improvement of channel transport in many recent cases.

1. Interfacial counter doping

In Sec. IV C, we made a distinction between interfacial counter-doping (shown in Figure 21(a)) discussed here from bulk counter-doping (i.e., buried channel devices). As mentioned earlier, for buried channel devices, the threshold voltage is typically negative. In contrast, interfacial counter doping results in positive threshold voltages. Results from 2D device simulations in Figure 21(b) show that for a fixed total counter doping charge is 1×10^{12} cm^{-2}. As the counter doping layer depth decreases, its effect on threshold voltages shift diminishes.

Energy-band diagrams of an n-channel MOSFET with counter doping are shown in Figure 22. The thin counter doping layer can be easily depleted by the adjacent p-well without gate bias, resulting in normally off devices. In inversion mode, the positive charges in the n-type depletion layer will cancel part of the negative electrical field built up by the negative charges in the p-well depletion region, reducing the slope of the potential drop toward the interface, effectively raising the surface potential [see Figure 22(a)]. As gate voltage V_G increases to produce strong inversion, the thin n-type layer is also filled by electrons and becomes neutral, which,

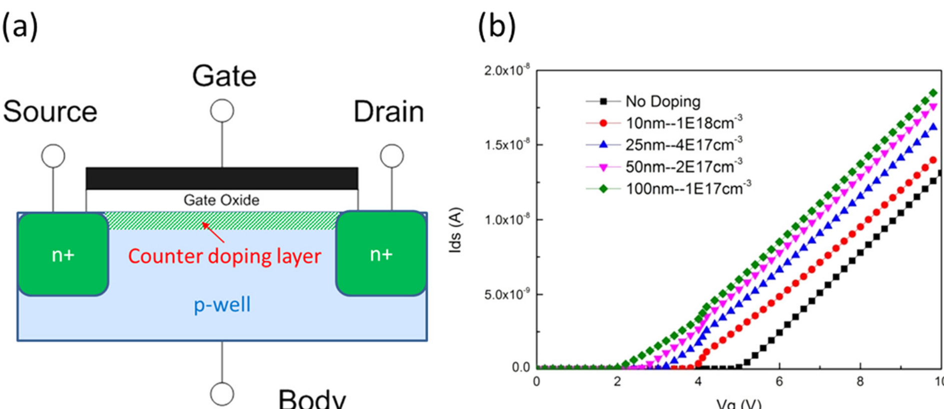

FIG. 21. (a) The cross-section of an n-channel MOSFET with interfacial counter doping layer. (b) Simulated threshold voltage dependence on counter-doping layer depth, where total counter doping charge is fixed to $1 \times 10^{12}\,cm^{-2}$.

in turn, widens the bottom of the conducting channel [see Figure 22(b)]. As a result, for the same inversion electron density, the electric field is lower, relieving surface roughness scattering and resulting in better mobility. Moreover, at any V_G, particularly in the low field range, there are more electrons, leading to higher screening, which also improves mobility.[94]

2. Group-V interfacial counter doping

Interestingly, the nitrogen and phosphorus treatments that passivate interface traps also result in interfacial counter-doping of SiC. The concept of interfacial counter doping, against conventional bulk counter doping, was used by Liu *et al*.[97] to explain the high mobility of MOSFETs fabricated on the $(11\bar{2}0)$ face using phosphorus and nitrogen interface passivation. It was suggested that in addition to passivating the interface defects, phosphorus and nitrogen diffuse a few nm into the SiC layer and act as native donors as well. This hypothesis was soon experimentally verified by Fiorenza *et al.*[127] They applied Scanning Capacitance Microscopy (SCM) to measure the doping profile on the cross section of n-type Si-face 4H-SiC—oxide samples, with and without N and P anneal (1000–1150 °C), as illustrated by Figure 23. The carrier concentration profile reveals that the peak donor concentration is $N_D = 5 \times 10^{17}\,cm^{-3}$ for N sample and $N_D = 4.5 \times 10^{18}\,cm^{-3}$ for P, compared to the initial n−type substrate doping of $N_D = 5 \times 10^{15}\,cm^{-3}$. The paper also estimates the N and P doped interfacial region thicknesses to be 5.1 and 1.7 nm, respectively. Around the same time, Tuttle *et al.* invoked the same effect to explain the observed reduction in the NITs in the presence of interfacial sodium, potassium, nitrogen, and phosphorous. They show that the NIT energy levels are lowered by the impurities and thus become inaccessible to the experimental measurements.[48] The magnitude of the interface counter doping effect of N and P for non-polar faces is still unknown, although it is expected to be larger than that for the Si-face SiC.[97]

We now know that the interfacial N and P can both passivate the defects and cause interfacial counter doping. To better understand the interfacial counter doping effects on MOSFET operation, it is necessary to separate it from defect passivation effects. Modic *et al.* showed that Antimony (Sb) is the ideal candidate for this purpose. As a group V element, it acts as electron donor, giving rise to counter doping. On the other hand, it does not show noticeable passivation effects on the defects, probably due to the large atomic size.[85]

In this report, it was reported that at low temperatures of ∼70 K, Sb donors freeze out, which results in a temperature dependence that can turn the counter doping effect on and off. Figure 24(a) shows the case of "Sb" only without additional interface passivation. The close to zero mobility indicates that the interface is unpassivated, and the counter-doping effect is absent. At higher temperatures, the Sb interfacial counter doping effect becomes active which results in higher mobility transport. The peak mobility remains the same when temperature is raised above room temperature. This indicates that coulomb scattering and phonon scattering are both active at this point. Figure 24(b) shows the case of

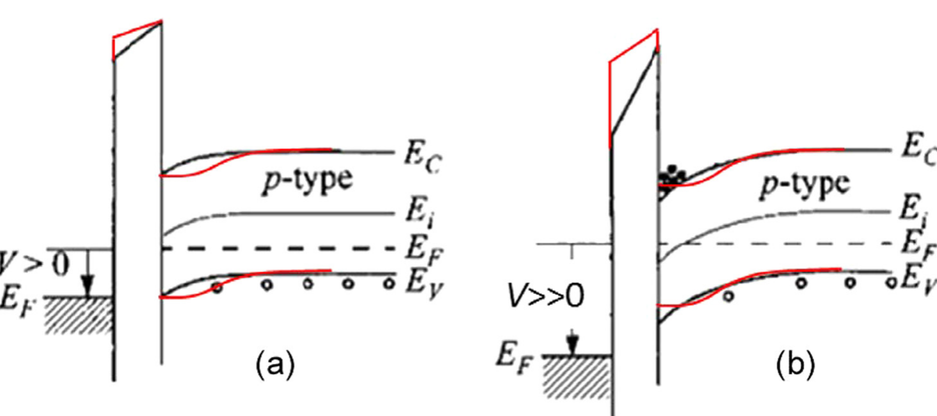

FIG. 22. Energy-band diagrams of an n-channel MOSFET, in (a) depletion and (b) strong inversion, where the standard enhancement mode structure is illustrated in black and the n-type counter-doping effect is highlighted in red. Reproduced with permission from Liu *et al.*, IEEE Electron Device Lett. **34**(2), 181–183 (2013). Copyright 2013 IEEE.

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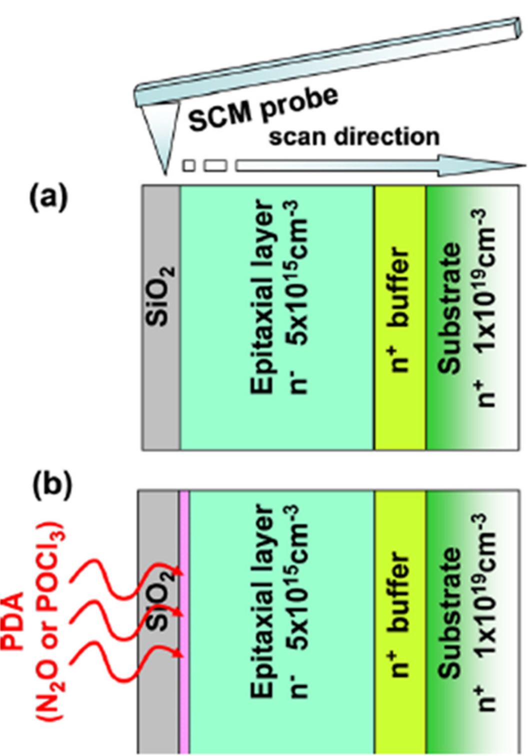

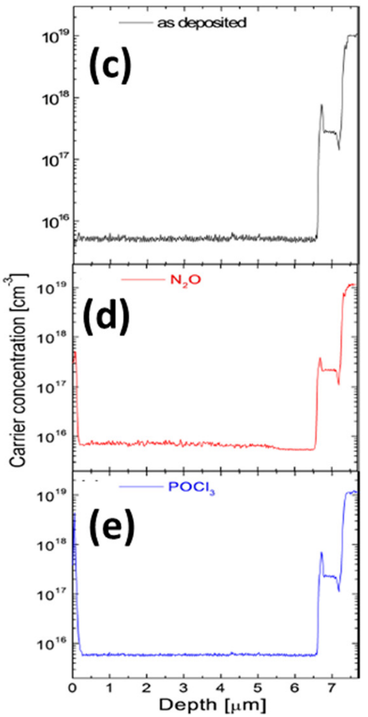

FIG. 23. Schematic of scanning capacitance microscopy on reference sample (a) and samples with P or N treatments (b). Measured carrier concentration profiles of reference, with N and P treatments are shown in (c)–(e), respectively. Reproduced with permission from Appl. Phys. Lett. **103**(15), 153508 (2013). Copyright 2013 AIP Publishing LLC.

"Sb + NO," where in addition to Sb counter-doping, the oxide was also annealed in NO. Nitridation passivates the interface, yet incompletely, since NO channel mobility is coulomb scattering limited. The combination of interfacial counter doping and NO defect passivation results in even higher mobility. The negative temperature coefficient of mobility indicates that phonon scattering limits the mobility. This implies that interfacial counter doping further reduces coulomb scattering, without physical defect passivation resulting in higher mobility at lower fields. The most likely reasons for this effect are: (i) A wider channel consistent with the counter-doping profile that results in a free carriers located further away from the Coulomb scattering sites at the interface and (ii) higher electron density at lower transverse fields which could result in effective screening from Coulomb scattering.

The peak mobility range reported for this experiment and the temperature dependencies match the values reported in the lanthanum silicate interface channel very well (see Figure 18). This indicates that there might be a universal behavior for the peak mobility temperature dependence, consistent with surface phonon scattering.[82]

The counter doping mainly affects mobility at low field when carrier density is low. As mentioned earlier, it reduces coulomb scattering but it has little effect on surface roughness scattering. This is most likely because the inversion carrier density at high fields overwhelms the counter doping carrier density, minimizing its effects. This is evident in Figure 19, where the counter doping does not make a difference to mobility at high field.

3. Metal counter doping

As mentioned in Sec. IV B, certain metals at the SiO_2/SiC interface give rise to very high mobility and low D_{it}, e.g., Na in group I, Ba in group II, and its immediate neighbor La the first element of transition metals. For Na, the theoretical study of Tuttle *et al.* has shown that its Coulombic potential results in ultrashallow donor states in the near interface SiC channel.[128,129] As a result, the sodium at the interface actually forms an interfacial counter doping layer with

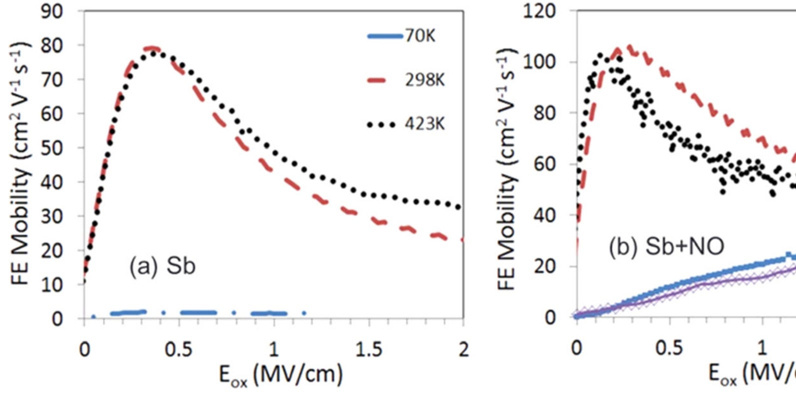

FIG. 24. Temperature dependence of field-effect mobility for 4H-SiC using the (a) "Sb" and (b) "Sb + NO" process. Reproduced with permission from Modic *et al.*, IEEE Electron Device Lett. **35**(9), 894–896 (2014). Copyright 2014 IEEE.

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all its benefits to channel transport as discussed in the last section, similarly for N and P.

It is yet to be confirmed for the case of Ba and La, whether these metals result in counter-doping. Nevertheless, it is possible that they behave similarly as Na, as they are all known to have a low ionization energy.

C. BTI

BTI is a major reliability issue in both Si and SiC MOSFETs. In Si MOSFETs, the release of hydrogen from passivated interfacial Si dangling bonds under BTI stress can lead to interface trap buildup and oxide-trap charge. In high-quality SiC MOSFETs, hydrogen is relatively ineffective in passivating interfacial defects. Therefore, one might expect that BTI in SiC-based structures may be caused by altogether different mechanisms than in Si MOS devices. It is particularly important to understand the instability mechanisms for MOS structures after nitridation since NO annealing is a primary process for commercial power MOSFETs. Figure 25 shows trapped charged density versus electron or hole injection as a function of NO annealing.[43] As mentioned in Sec. III B, in addition to reducing the interface state density and improving mobility, nitridation of the SiO_2/SiC interface also yields immunity to electron injection but increases hole trapping.

A near-interface SiO_xN_y transition layer theory was proposed by Rozen *et al.* to explain the nitridation induced hole trapping phenomena.[75] The first-principle calculations performed in supercells representing amorphous SiO_2 indicated that N atoms and NO molecules could insert in Si–Si suboxide bonds and Si–O–Si bridges leading to an oxygen protrusion. In the latter case, it would correspond to nitrogen converting a perfect oxide into an oxynitride. The binding of nitrogen in SiO_2 is expected to induce a lone-pair state close to the valence band edge of 4H-SiC. This level is predicted to act as a hole trap, which could be the origin of the enhanced hole trapping after nitridation, as illustrated in Figure 26. These two N related bridges may be precursor defects leading to the ESR signal observed by Campbell *et al.* after hole capture.[130,131]

Sequential switched-bias stressing on NO annealed MOS capacitors shows reversible degradation for *n*-type substrates and monotonically increasing degradation for *p*-type.[132] This cannot be explained by the SiO_xN_y transition layer theory, as it has been demonstrated that trapped holes are released from N-related defects at the interface of NO-annealed SiC MOS structures at 125 °C.[42] This indicates that there may be more than one atomic mechanism that is operational during BTI.

Shen *et al.* found that the conventional O vacancy can explain degradation under both stress voltage polarities, as illustrated in Figure 27.[132] The neutral O vacancies can transform from a dimer to a puckered configuration upon hole capture; capture of a second hole further stabilizes the puckered configuration. The neutral O vacancy level rises from its initial level to far above the SiC valence band edge after the capture of one or two holes. In contrast, no significant structural change happens when the O vacancy captures an electron.

In addition, the measured effective-activation energies for BTI in 4H-SiC metal-oxide-semiconductor capacitors, for *p*-type and *n*-type substrates, coincide closely with the ionization energies of the respective dopants. This suggests that dopant ionization may also play an important role in BTI from room temperature to 150 °C. Moreover, temperature induced barrier lowering and trap-creation may contribute to BTI in SiC at higher temperatures as well.[132]

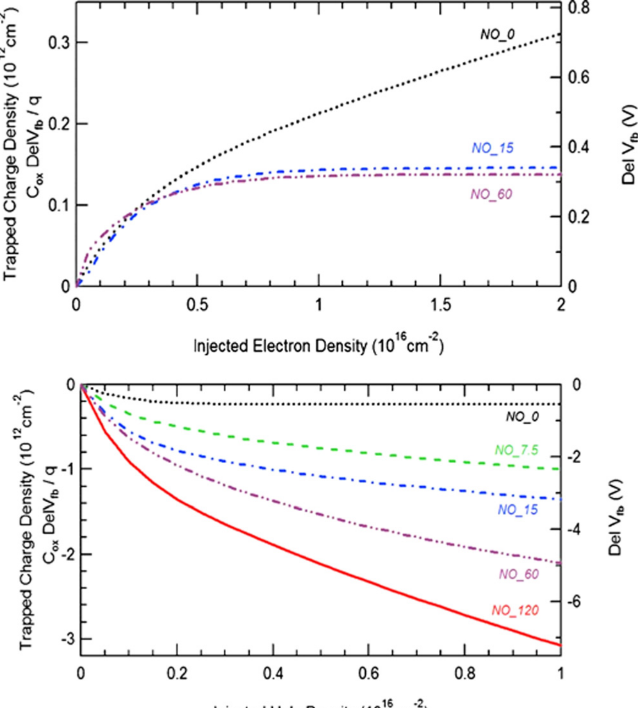

FIG. 25. Effective trapped charge upon electron (top panel) or hole (bottom panel) injections in oxides annealed for various times in NO.[46] Reproduced with permission from J. Appl. Phys. **105**(12), 124506 (2009). Copyright 2009 AIP Publishing LLC.

VI. SUMMARY

In this paper, we reviewed the current status of SiC power MOSFET technology and highlighted the most critical

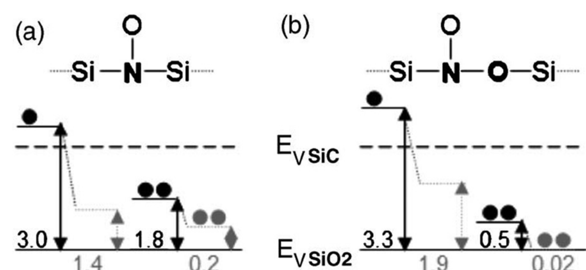

FIG. 26. Configurations resulting from N and NO incorporation in SiO_2. The energy of the corresponding levels are noted in electron-volts. Before trapping (labeled in black), they each have a singly occupied level and a doubly occupied level. The capture of a hole leads to a lowering of the energy states (labeled in gray). The calculated energy levels are adjusted using the experimental value ≈2.9 eV for the valence band offset between 4H-SiC and amorphous SiO_2.[75] Reproduced with permission from J. Appl. Phys. **103**(12), 124513 (2008). Copyright 2008 AIP Publishing LLC.

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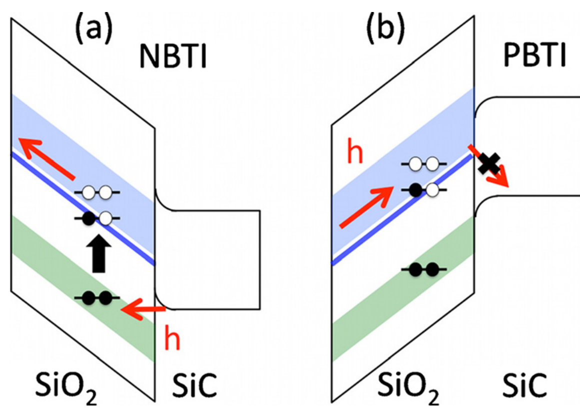

FIG. 27. Schematic diagram for switched-bias stress in p-substrate SiC MOS capacitors. (a) Injection of holes during the initial positive Bias Temperature Stress (BTS). Electronic energy levels are shown for the neutral dimer O vacancy $V_O{}^0$ (lower band, green), and the puckered VO+ (middle line, dark blue) and $V_O{}^{2+}$ (upper band, light blue) configurations. Upon hole capture, the O vacancy undergoes a structural transformation (puckering) that shifts electronic levels far above the SiC valence band. (b) Drift of trapped holes during the positive BTS after the initial negative stress. Since the electronic levels of the holes are far above the SiC valence band, the holes pile up at the oxide side of the interface and cannot enter the SiC substrate. Reproduced with permission from Appl. Phys. Lett. **98**(6), 063507 (2011). Copyright 2011 AIP Publishing LLC.

directions for advancements. Following a brief overview of the SiC technology history, we summarized the current understanding of the theoretical aspects of SiC oxidation, defect formation, and interface nitridation, from the MOS channel transport point of view. We pointed out that the two main challenges for further SiC power MOSFET development are the low channel mobility and gate threshold voltage instability. The recent progress and underlying fundamental aspects of these problems have been discussed in detail, including mobility limiting factors, mobility improvement mechanisms, and the bias temperature instability theory. The new advances in mobility and stability have not only improved the performances but also open new ways to understand the underlying physical mechanisms. There is still room for further improvements and many of the fundamental questions remain open. It is our hope that this review paper can be a timely and helpful orientation for researchers that have an interest SiC MOSFET research. There is no doubt that the next generation SiC/SiO_2 interface treatments with higher inversion channel mobility and better gate threshold voltage stability will unleash the full potential of SiC power MOSFETs. And such advancements can bring forth the new era of power electronics for a more sustainable energy future.

ACKNOWLEDGMENTS

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