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Review

Review of Silicon Carbide Processing for Power MOSFET

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Abstract: Owing to the superior properties of silicon carbide (SiC), such as higher breakdown voltage, higher thermal conductivity, higher operating frequency, higher operating temperature, and higher saturation drift velocity, SiC has attracted much attention from researchers and the industry for decades. With the advances in material science and processing technology, many power applications such as new smart energy vehicles, power converters, inverters, and power supplies are being realized using SiC power devices. In particular, SiC MOSFETs are generally chosen to be used as a power device due to their ability to achieve lower on-resistance, reduced switching losses, and high switching speeds than the silicon counterpart and have been commercialized extensively in recent years. A general review of the critical processing steps for manufacturing SiC MOSFETs, types of SiC MOSFETs, and power applications based on SiC power devices are covered in this paper. Additionally, the reliability issues of SiC power MOSFET are also briefly summarized.

Keywords: silicon carbide (SiC); silicon (Si); power devices; SiC MOSFETs; on-resistance; breakdown voltage

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1. Introduction

The development of power electronics technology has always been towards achieving higher power density, higher efficiency, and integrating many systems [1,2]. Power semiconductor devices (power devices) play an important role in this development. Power devices are used for controlling electric energy precisely, with high efficiency and reliability from the source to load, depending on the load demand. Over the last 50 years, the advancements of power devices have been primarily due to Si-based power devices. However, due to limitations of the intrinsic physical properties of Si, devices based on Si cannot be used for future power devices. Hence, researchers have aimed to find alternative materials for replacing Si in power devices [3]. The introduction of wide-bandgap (WBG) semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) materials have been a revolutionary development in the field of power devices [3,4]. The superior material properties of WBG materials, such as higher dielectric strength, higher saturation drift velocity, and the ability to operate in harsh environments, make the materials favorable for power devices [5]. GaN-based devices are mainly used for high-frequency applications, while SiC-based devices are used for high voltage power applications. The larger critical electric field, higher thermal conductivity, and higher breakdown voltage enable SiC-based

devices to operate at higher current density, higher temperature, and higher blocking voltage [4,6–8]. Hence, SiC-based power components have been a topic for extensive research for high voltage/power applications for more than a decade. Moreover, SiC is more mature in terms of the quality of the crystal [9], the existence of large wafers [10], and is readily available in the market [11]. In addition, the material cost of SiC is much lesser than that of GaN [12], and the processing lines of SiC-based devices have great compatibility with that of Si-based devices.

1.1. SiC Materials Properties

SiC was discovered by professor Jons Jakob Berzelius in 1823 at the Karolinska Institute in Stockholm [13]. SiC exists in different crystalline structures, depending on the stacking sequence, and this phenomenon is known as polytypism, where each structure is known as a polytype of SiC. Hence, SiC is a classical polytypic substance existing in more than 250 polytypes [14,15]. The most common research polytypes for SiC devices are 6H-SiC, 4H-SIC, and 3C-SiC. The crystal structures of 4H, 6H, and 3C SiC polytypes are shown in Figure 1 [16]. Among the polytypes, 6H-SiC and 4H-SiC are the most preferred polytypes, especially for device production, as they can make a large wafer and are also commercially available. For high power, high temperature, and high-frequency device applications, 4H-SiC is the most used and established-material due to its high electron mobility [17,18], higher bandgap, higher critical electric field [19], and shallower ionization energy of dopant [20], along with the availability of the single crystalline wafer. In addition, 4H-SiC does not exhibit anisotropy electron mobility, whereas 6H-SiC does [21]. Hence, 4H-SiC has been developed exclusively and is also more readily available [9,22].

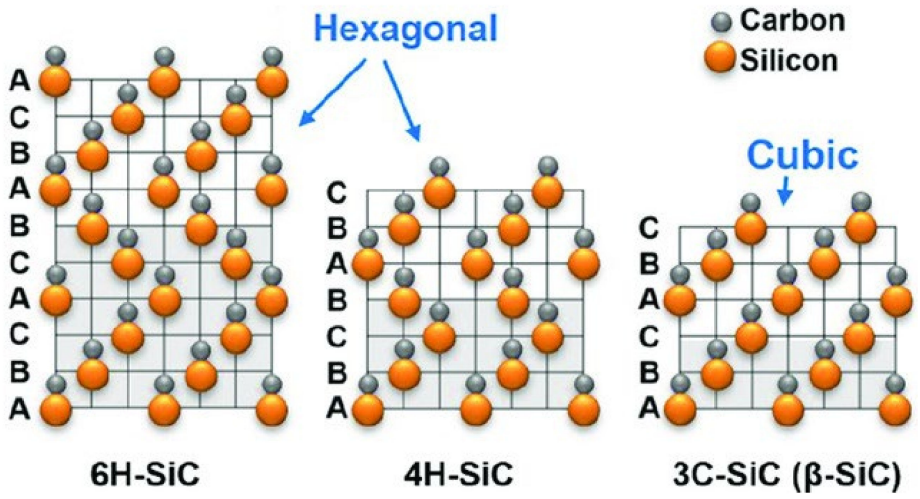


Figure 1. The staking sequences of SiC polytypes: 4H-SiC, 6H-SiC, and 3C-SiC [16].

The comparison of three polytypes of SiC with Si is given in Table 1 [20]. Each polytype exhibits different electronics properties, and the bandgap energy of polytypes are larger than that of Si and remains the same at 1000 K [20]. Moreover, the intrinsic carrier concentration of the polytypes is much lower than that of the Si, which makes SiC a suitable candidate for high-temperature applications. This is because, at high temperatures, the material properties undergo changes such as decreasing the energy bandgap and increasing carrier concentration, which affect the device performance [23]. Therefore, a WBG material with a low intrinsic carrier concentration is preferred for high-temperature power applications. In addition, the high thermal conductivity of SiC allows the transfer of heat more efficiently than the other semiconductors, which further enhances the performance of the device [24]. For semi-insulating SiC with low impurity, a very high thermal conductivity of about 500 W/m-K was achieved [25].

Table 1. Comparison of material parameters of polytypes of SiC and Si [20].

Material Parameters	4H	6H	3C	Si
Energy bandgap at 300 K (eV)	3.26	3.03	2.3	1.12
Lattice constant at 300 K (A)	3.076	3.081	4.349	3.84
Critical electric field (V/cm)	2.2×10^6	2.5×10^6	2×10^6	2.5×10^5
Saturated electron drift velocity (cm/s)	2×10^7	2×10^7	2.5×10^7	1.0×10^7
Thermal conductivity ($W/cm^{-1}K^{-1}$)	3.0–3.8	3.0–3.8	3–4	1.5
Intrinsic carrier concentration (cm^{-3})	10^{-7}	10^{-5}	10	10^{10}
Electron Mobility at $N_D = 10^{16}$ (cm^2/V-s) (‖c-axis)	900	60	750	1400

Moreover, the higher critical electric field of SiC, at least by one order magnitude than Si, helps SiC devices to have a thinner and highly doped drift region for the same breakdown voltage, which further reduces the specific on-resistance ($R_{on,\,sp}$). Thus, a smaller die size can be achieved [26]. The outstanding chemical properties of SiC, such as higher melting temperature (2800 °C), higher chemical inertness, and higher radiation resistance [27], along with its impressive mechanical properties, especially the hardness (2480 kg/mm^2) and high wear resistance value (9.15) [28], make SiC an excellent candidate for use in high temperature and harsh environmental conditions, ranging from highly erosive to highly corrosive environments. Along with the abovementioned properties of SiC, some other characteristics of SiC that are also useful in power devices include the ability to grow homoepitaxially without mismatch, achieving both p- and n-type conductivity by doping, the availability of large substrates, and the ability to grow oxide film thermally on both Si and C faces [29].

1.2. SiC Power Devices

A semiconductor device is said to be a power device if it is used as a rectifier or a switch in power electronics. Power devices are the heart of the power electronics system. Power devices were first introduced in 1950 [30]. Since then, many Si power devices have been introduced, namely, bipolar power transistor (BPT or BIT), insulated gate bipolar transistor (IGBT), gate turn-off thyristor (GTO), static induction transistor (SIT), and power MOSFET. However, despite achieving numerous advancements, Si power devices had reached their performance limitation. The groundbreaking developments in power devices are due to the introduction of WBG-based power devices due to the excellent material properties of WBG materials, as mentioned above. Most of the SiC-based power rectifiers and power switches for high voltage applications are designed as vertical devices based on semi-conducting substrates. In contrast, some other SiC-based high-power RF devices, such as metal-semiconductor field-effect transistors (MESFETs), are designed as a horizontal device and are generally based on a semi-insulating substrate [31,32].

The main advantages of SiC power devices over Si power devices are as follows [33]: First, improved voltage capability. The breakdown voltage of SiC SBDs is able to achieve around 1700 V, which is much higher than that of 200 V Si-based SBDs. Chips based on a SiC diode were able to obtain a breakdown voltage of about 20 kV, which is almost equivalent to that of a high-pressure Si stack. The breakdown voltage of SiC MOSFETs is about 10 kV, whereas it is 1 kV for the Si MOSFETs. Moreover, the complexity, as well as the size of SiC devices, can be reduced drastically compared to that of Si devices as the total parallel and series components of SiC devices can be minimized to 1/10th times of Si devices, thus increasing the reliability of SiC devices. Second, the outstanding switching performance of SiC devices. On comparing with Si devices, SiC devices have a negligible reverse recovery rate at the same voltage level. Hence, SiC devices are preferred for high-frequency operations, i.e., tens of MHz. Third, generally, the SiC devices tend to have a positive temperature coefficient when compared with Si devices and can achieve a larger

current by using parallel chips. Therefore, designing a device with a higher voltage, the higher current becomes much more convenient.

Among the power devices, the power MOSFET is one of the most common power devices due to its fast switching speed, low gate drive power, as well as the capability of withstanding both high current and voltage applications simultaneously without any destructive failure [34]. On comparing SiC-based power MOSFET and Si-based power MOSFET, SiC power MOSFET can achieve a $R_{on, sp}$ much lower than that of the Si counterpart, which helps in achieving a smaller parasitic capacitance as well as higher switching speed [35]. Therefore, a power device based on SiC can achieve lower conduction and switching loss for a large range of blocking voltages [36]. In addition, the major advantage of SiC MOSFET over Si MOSFET is that as the temperature rises from 25 to 135 °C, the on-resistance of SiC MOSFET is increased by 20%, whereas it increased by 250% for Si MOSFET [37].

SiC power MOSFETs have made tremendous progress since the first SiC device appeared in 2001 [35]. The evolution of the commercialization of SiC power devices is shown in Figure 2 [38]. Currently, the main suppliers of SiC power devices are Cree/Wolfspeed, Microsemi, Infineon, GeneSiC, ST, Mitsubishi, and ROHM [39]. Additionally, according to Yole, a research organization of the market, these companies together share 80% of the SiC power semiconductor market. The most common commercially available SiC power devices include SiC Schottky diodes, SiC JFETs, SiC BJTs, and SiC MOSFETs [35]. At present, some of the highest voltage/current rated SiC-based commercially available devices are (a) SiC Schottky diodes with a rating of 1.7 kV/25 A, (b) discrete SiC MOSFETs with 1.7 kV/72 A, (c) SiC MOSFET modules with 1.7 kV/225 A from CREE/Wolfspeed, and (d) SiC BJT modules with 1.7 kV/160 A from GeneSiC [39]. The SiC device that is commercially available for high temperatures is the 210 °C SiC BJTs with a voltage/current rating of 600 V/20 A from GeneSIC.

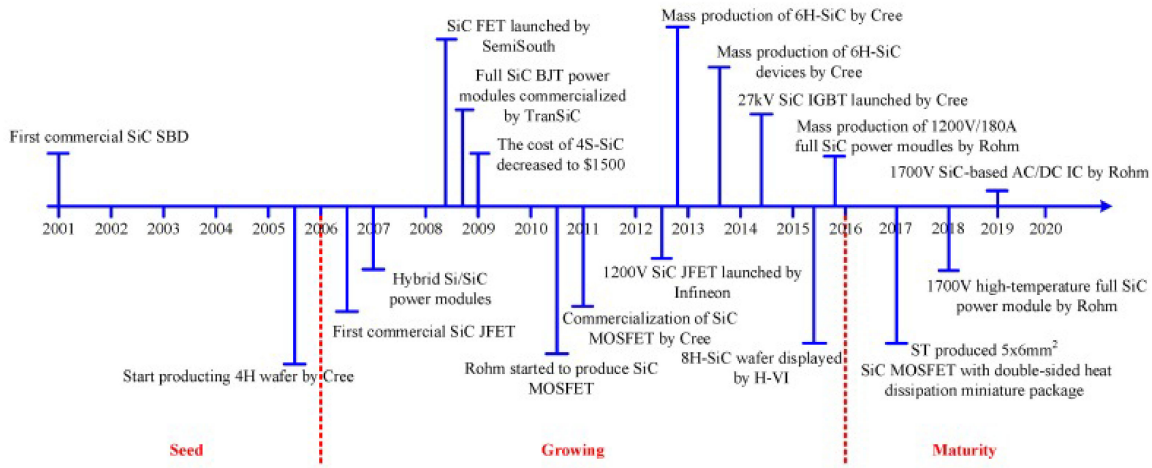


Figure 2. The development of SiC-based devices over the year [38].

The benchmark plot of various SiC power devices on breakdown voltage (BV) and $R_{on, sp}$ of the various SiC power devices is shown in Figure 3. This plot represents the intrinsic capability of the device or FOM from the conduction point of view. The data of the SiC devices were collected from different articles [3,40–81]. From the plot, it is observed that most of the SiC power devices are able to perform beyond the limits of Si, indicating the advantages of the SiC power devices over Si counterparts. Though SiC devices are not far from reaching their limit, there is still plenty of room for some of the SiC devices to improve their performances. Additionally, due to the strong conductivity modulation of SiC GTOs and PIN diodes, these devices are able to surpass the SiC limit. On comparing theoretical limits of SiC and GaN, GaN limits show a better trade-off between the breakdown voltage and on-resistance. However, GaN-based devices are mainly employed for high-speed

lower voltage applications, and, due to lower thermal conductivity than SiC, SiC-based devices are preferred for high-temperature applications.

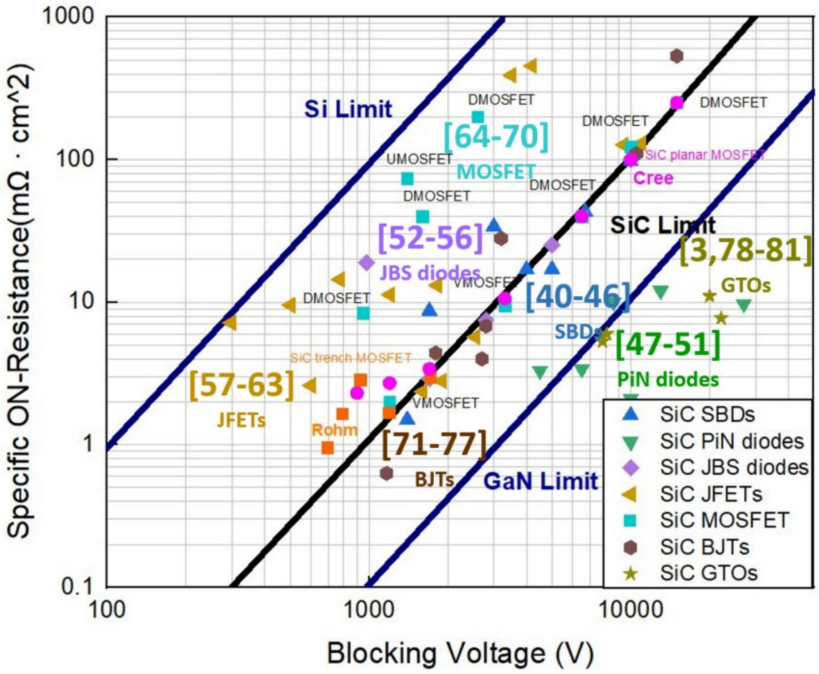


Figure 3. The benchmarking plot on specific on-resistance and breakdown voltage for various SiC power devices [3,40–81].

1.3. SiC Applications

The high-performance capabilities of SiC power devices provide a significant improvement in the existing systems, enabling new power applications. In addition, the outstanding material and chemical properties of SiC, namely, high thermal conductivity, high breakdown electric field, low intrinsic carrier concentration, and high chemical inertness, make SiC-based devices favorable devices for implementing in high-temperature electronics as well as in thermal sensors that can also be used in harsh environments [82]. Moreover, the lower on-resistance and the lower output capacitance of SiC MOSFET makes it an appropriate choice to be used in switching designs such as three-phase inverters, digital power supplies, and also for electronic AC-to-DC or DC-to-DC converters [31]. In addition, the reduced switching losses of SiC devices also improve the switching frequencies of the converters. Hence, SiC power devices play an important role in high-performance power device applications.

At present, SiC-based converters are used in solar inverters [83,84], EV/HEV drivers (e.g., SiC MOSFETs at Tesla Model 3 EVs) [85–87], railway traction inverters [88], high voltage applications [89], and uninterrupted power supplies (UPSs) [90]. The cost of a solar inverter was reduced by 20% of the power by using SiC diodes and SiC JFETs [91]. Figure 4 illustrates the classification of various types of applications based on Si and WBG devices [5]. As seen in the figure, Si devices are used for lower power and lower frequency applications, while GaN-based devices are used for lower voltage and lower power high-frequency applications such as data centers and consumer systems; SiC devices are used for higher power, higher voltage switching power applications such as trains, electric vehicles and their battery chargers, and industrial automation.

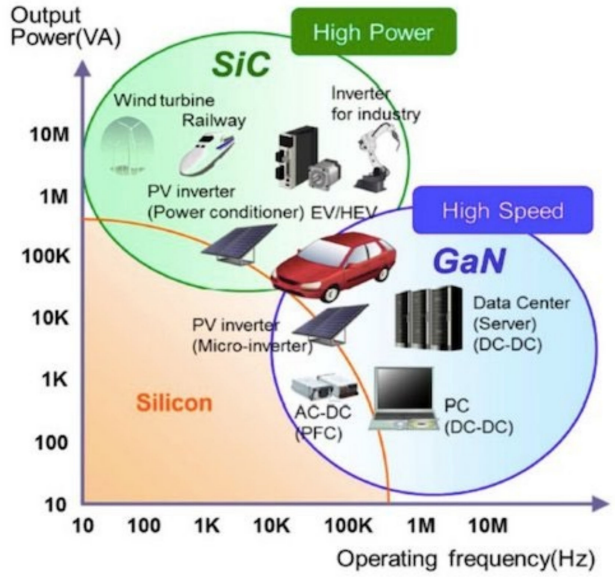


Figure 4. Applications based on WBG materials. Image used courtesy of Georgia Tech.

SiC power devices also provide significant help in the rising demand for photovoltaic energy. The photovoltaic energy source needs fast switching, low loss, high power, and a reliable device that improves efficiency, reliability, and power density. The desired performances have been achieved by implementing SiC power devices [92]. SiC power devices are also used for developing power modules. The SiC power modules were able to achieve a voltage/ampere rating range from 1.2 kV–3.3 kV/70 A–800 A, which is suitable for electric vehicle applications (EVs) such as onboard chargers, DC-DC power converters, and motor drives [93]. Smart EVs are an advanced class of vehicles that can reduce the emission of carbon dioxide up to 43% compared with diesel-based vehicles [94]. A 1.2 kV SiC MOSFETs developed by Wolfspeed's was able to replace the IGBT transistors used in the circuit topologies of the EVs battery charging system; the new system was able to manage a wide range of voltage, ranging from 200 to 800 V. Moreover, the new system was able to reduce power losses by 40%, increase power density by 50%, and also manage the bidirectional charging or discharging process [95].

This paper reviews the critical process steps of the fabrication process for SiC power devices, which include substrate formation, epitaxy layer, ion implantation, and oxidation. The most common types of SiC power MOSFETs, such as planar and trench MOSFET and superjunction MOSFET, are also discussed. Finally, the review is concluded by briefly discussing the reliability issues of SiC MOSFETs.

2. SiC Critical Step

One of the most important steps that play an important role in improving the performance of SiC power devices is the device fabrication process flow. SiC power devices tend to show better performance when it is used as n-channels rather than p-channels; to achieve even more enhanced performance, the device needs to be grown epitaxially on low-resistivity p-type substrates. However, at present, the commercially available p-type 4H-SiC substrate has relatively high resistivity (~2.5 Ω·cm), which is about two orders of magnitude higher than that of the n-type substrate [96]. The advantages of n-channel SiC devices weaken if the high resistivity p-type substrate is used. Hence, due to the present issue of the nonavailability of p-type substrates with low resistivity, reverse growth is studied by growing layers on commercial n+ substrates to enhance the performance [97].

To further improve the performance of the device, the trench design process of the device is also considered. The trench structure has been widely used in Si-MOSFETs, and it has also attracted much attention in SiC-MOSFETs. Trench SiC MOSFET exhibited no degradation in both the on-resistance of differential body diodes and the on-resistance

of the device even after continuous current stress of 500 h [98]. Moreover, the trench SiC MOSFET exhibits lower on-resistance than the conventional design as the trench design does not have JFET regions [99].

In the fabrication process steps of the trench MOSFET, the implantation of the p-base step and the trench formation step can be interchanged, i.e., by performing p base implantation first and then making trench structure, as in [100], or making the trench first and then the p-base implantation, as in [101]. The fabrication process flow by performing trench first is shown in Figure 5. The process step is as follows: first, the n- drift region is epitaxially grown on n+ substrate; then, the trenched gate region, after the structure is trenched by implantation by using Al or N, is done to make the p-base region; subsequently, p+ implantation is done to form the shielding region, and then n+ implantation is performed for defining the source and drain regions. After the implantation steps, the resulted structure is then exposed to high temperatures for thermal oxidation to form gate oxide after annealing, and then the gate electrode, source metal, and drain metal are deposited. Finally, the structure is coated with a polyimide layer as a protective passivation layer. To improve the performance of the device by reducing the number of defects present in the SiC substrate and epitaxial layer, various methods of ion implantations and thermal oxidation processes are employed [96,97].

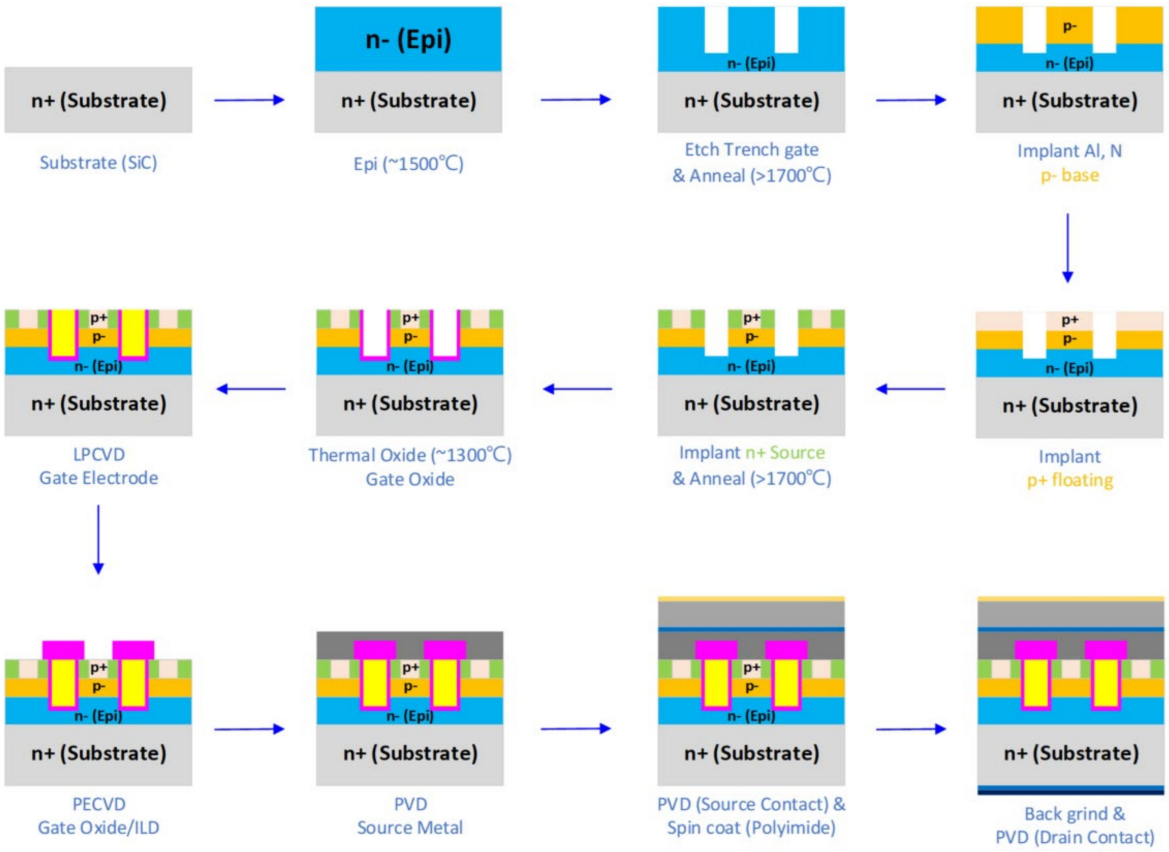


Figure 5. SiC MOSFET process flow.

The performance, reliability, and stability of the SiC devices also depend on the quality of the SiC wafers [102,103], and the yield of the SiC components indirectly affects the cost of manufacturing. The total defects of SiC wafers are mainly intrinsic material defects and structural defects caused by epitaxial growth. These defects act as recombination centers and reduce the carrier lifetime of the thick drift region significantly. Different optimization process parameters, such as C+ ion implantation/annealing, thermal oxidation/annealing, or trench design, could reduce these defects to a very low level of about 10^{11} cm^{-3} [104].

To reduce the interface trap density for further improving the device performances, a thin insulator with a high dielectric constant and a large bandgap was deposited by atomic layer deposition (ALD) technology [105–109]. Several ALD materials such as Al_2O_3, AlN, and ZrO_2 have also exhibited the ability to improve the properties of power electronic components significantly [110–112]. However, although many efforts have been made to reduce these defects, they still exist and greatly affect the carrier lifetime. In addition, the trade-off between target defects and new defects caused by post-growth and the contradiction between C-plane and Si-plane epitaxial growth further hinder its commercialization. Therefore, the supply of large-size and high-quality materials and the epitaxial growth process with low defect density are the keys to the commercialization of SiC devices.

2.1. SiC Substrate

The semiconductor SiC is widely known for its appearance in various stable crystal polytypes. The crystal structure differs from the different stacking order to the Si-C double layer, where each Si is surrounded by four C atoms, as shown in Figure 1. Physically, it is mainly a large bandgap and good thermal conductivity material, as shown in Table 1. A general growth process of SiC is done by the physical vapor transport (PVT) method. The sketch of a typical PVT growth method is shown in Figure 6a [113]. The SiC source is placed on the graphite crucible, and the apparatus is surrounded by insulation materials. The temperature field is mainly determined by the crucible and the surrounding isolation parts, which are in the case of a long coil. The growth method is done at a high temperature of about 2000 °C or more. It shows as a feasible design to susceptor of the electromagnet heating power and inductive heating in PVT growth technology. It reaches a low background doping level in a high vacuum range of 10^{-6} to 10^{-7} mbar.

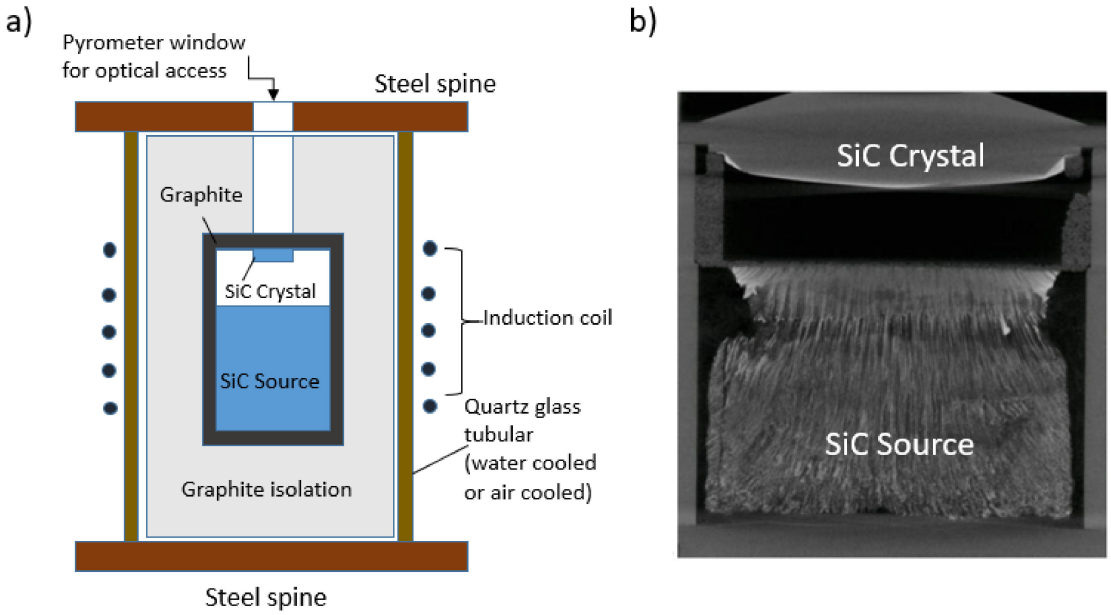


Figure 6. (**a**) A sketch of the PVT growth method for SiC boules and (**b**) 2D visualization of the PVT growth to image the great details about the morphology and the crystal growth interface and conditions [113].

The X-ray imaging in 2D [114–116] and 3D illustrations [117,118] are shown in Figures 6b and 7. This application indicates that the in-situ visualization of the PVT growth process is available. Employing the in-situ X-ray diffraction to analyze the visualization of polymorphic transformation [119] and the curvature of the lattice plane [113] have been demonstrated during the crystal growth.

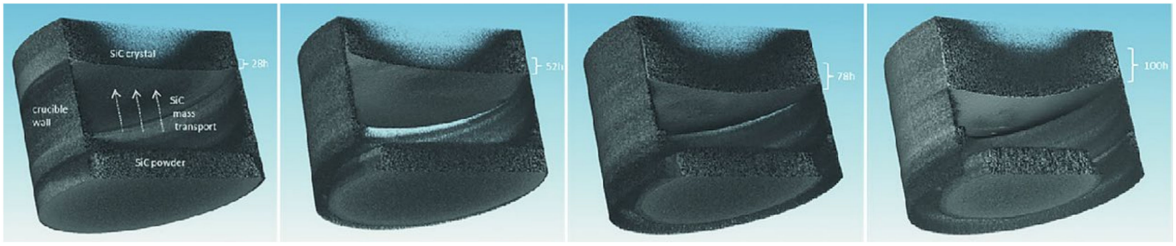


Figure 7. 3D in situ x-ray visualization of the PVT growth process using computed tomography: detailed visualization of the crystal's growth interface [113].

Furthermore, a wafering process includes grinding the crystal to a specific size and fabricating a flat plane in the direction of the substrate. The multiple-wire saw is usually used for wafer dicing. A stainless-steel wire and diamond-based slurry are used for abrasive materials. On the other hand, diamond-coated steel wire and laser cutting are also available in new wafering technologies. However, the new technologies require further technological development. To achieve a smooth and mirror-like wafer surface, three process steps are required, such as (1) grinding the diced wafer, (2) polishing with diamond slurry to obtain an optically perfect surface, and (3) chemical mechanical polishing (CMP) to fabricate a wafer-level SiC substrate for the next power device process.

2.2. SiC Epitaxy

Homoepitaxial growth was researched on commercially 4° off-axis 4H-SiC (0001) Si-face substrates using a horizontal hot-wall chemical vapor deposition reactor; its reactive source included SiH_4, C_3H_8, and H_2 [120]. First, H_2 etching in the epitaxial chamber was generally done at 1650 °C for 25~35 min before the SiC epitaxy. The pressure during H_2 etching was around 3.5–5.5 kPa. Typical growth was at 1600–1650 °C, and the SiH_4 flow rate was varied from 1 to 30 sccm in H_2 carrier gas flow at a fixed rate of 10 slm. Figure 8a shows the SiH_4-flow-rate dependence on the growth rate at a moderate C/Si ratio (C/Si = 1.2) in source gases [121,122]. The growth rate increased through the SiH_4 flow rate, and it reached 85 µm/h at a SiH_4 flow rate of 30 sccm. Figure 8b shows a smooth surface in 150 mm-diameter 4H-SiC epitaxy at a 77 µm/h growth rate [123].

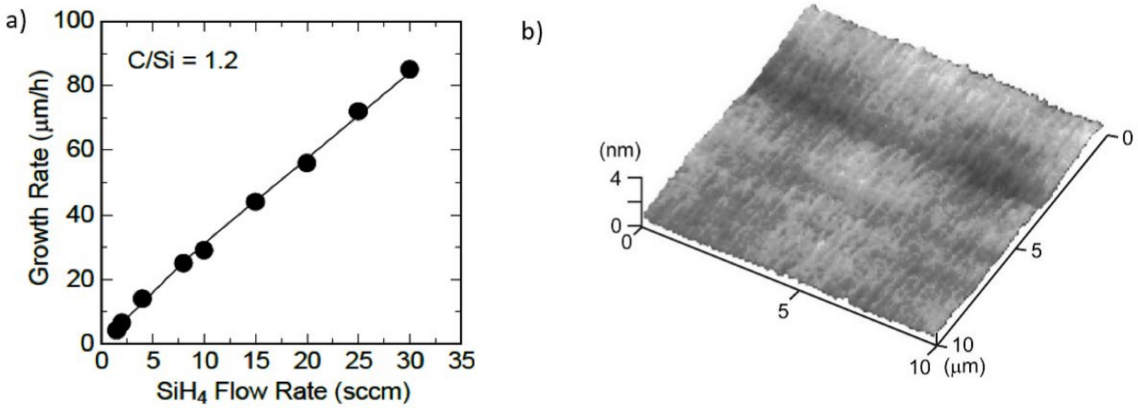


Figure 8. (**a**) SiH_4-flow-rate dependence of the growth rate at a C/Si ratio (C/Si = 1.2) in the homoepitaxial growth of 4H-SiC(0001) [121,122]. (**b**) AFM results from a 150 mm-diameter 4H-SiC epitaxy grown at 77 µm/h [123].

Furthermore, both SiH_4 and C_3H_8 flow rates increase with a moderate or high C/Si ratio, and the doping concentration will decrease. In comparison, the amount of excess carbon increases with the total source gas flow rate, and the epitaxial growth rate increases on the growing surface [121,122]. It induces suppression of nitrogen incorporation at high flow rates of SiH_4 and C_3H_8, and the effect results from the increase in effective C/Si ratios [124]. It shows a good epitaxial surface that almost exhibits the less disordered

bunching in growth processes, which also reaches the RMS roughness of 0.21 nm in Figure 8b [123]. Therefore, the bigger C/Si ratio also brings surface roughness and impacts p-type conductivity. However, it is usually made in the 3C-triangular defects and various SFs confirmed in 4H-SiC epilayers. The different types of SFs could be identified as different formation mechanisms, as illustrated in Figure 9 [123].

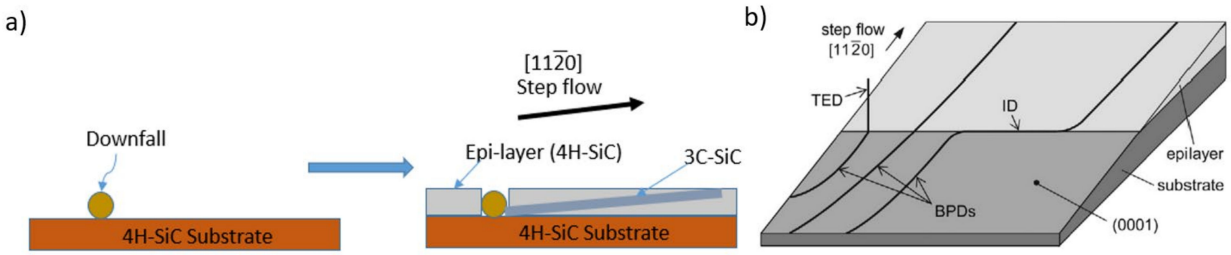


Figure 9. (**a**) Schematic illustration of the formation of downfall and (**b**) 3C-triangular defects and BPD propagation in 4H-SiC epitaxial growth [123].

2.3. Ion Implant

Ion implantation is an important process for manufacturing almost all types of SiC devices. A wide range of doping control of n-type and p-type conductivity can be achieved by ion implantation. Since the diffusion coefficient of the dopants in SiC is very small, most of the diffused impurities during implantation can be ignored during the post-implantation annealing process. However, if the damage to the crystal lattice during implantation is close to the amorphous state, it is difficult to restore the crystal lattice. Therefore, high temperature (~500 °C) implantation is usually used, especially when the implant dose is very high. Additionally, it is necessary to perform post-implantation annealing at a very high temperature (>1700 °C) to achieve lattice recovery and a high electrical activation rate. This high-temperature annealing may cause inconsistent silicon evaporation and a rough surface. Figure 10a shows the dependence of the electrical activation rate on the annealing temperature of SiC implanted with nitrogen (N) or phosphorus (P); the implantation is done at room temperature (RT) [125]. The activation rate below the annealing temperature of 1300°C is very small (<10%), and high-temperature annealing at 1600~1700°C is required to obtain a nearly perfect activation rate (>95%).

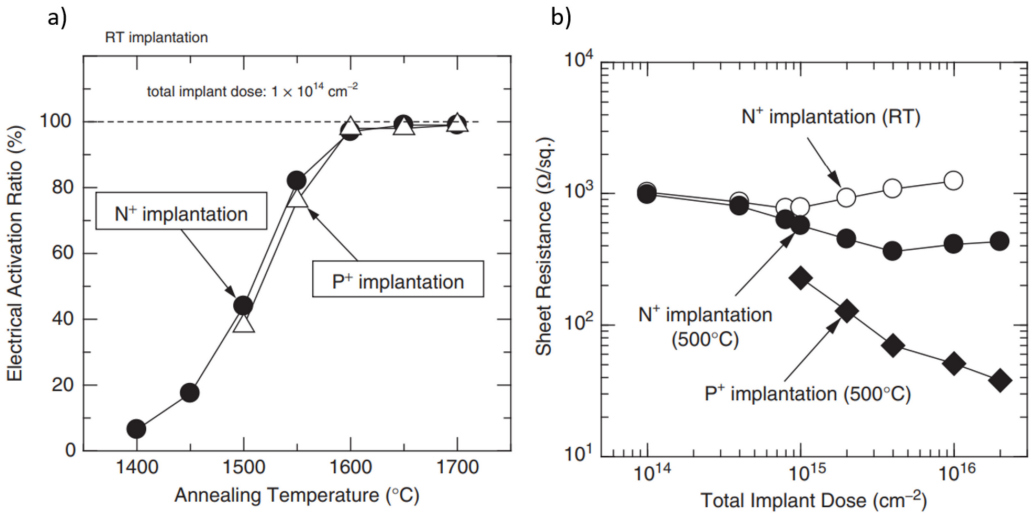


Figure 10. (**a**) Annealing-temperature dependence of the electrical activation ratio in nitrogen- (N) or phosphorus (P)-implanted SiC. (**b**) Sheet resistance versus the total implant dose for N- or P-implanted SiC annealed at 1700 °C for 30 min [125]. Copyright © 2022 John Wiley & Sons, Singapore Pte. Ltd.

Figure 10b shows the relationship between the sheet resistance of N- or P- implanted SiC annealed at 1700 °C for 30 min and the total implant dose. When the implant dose is relatively low (<3 × 10^{14} cm^{-2}), there is no significant difference in the sheet resistance of the N+ implant type, regardless of the implant temperature (RT or 500 °C) [125]. In the case of RT implantation, the sheet resistance at the implant dose is about 0.7–1 × 10^{15} cm^{-2}, and it increases with the further increase of the implant dose. In this high-dose region, the lattice damage caused by room temperature implantation is very serious. After activation annealing, the implanted area contains high-density stacking faults and 3C-SiC crystal grains. On the other hand, it was observed that the sheet resistance decreases as the thermal implantation dose increases. The maximum sheet resistance of the nitrogen-implanted area is almost saturated at 300 Ω/sq., which may be limited by the relatively low solubility of N atoms in SiC. The sheet resistance can be further reduced to 30–50 Ω/sq by thermally injecting P. This process is possible due to the higher solubility limit of P.

2.4. Oxidation

Like Si, SiC also has the ability to produce high-quality SiO_2 through thermal oxidation. Hence, to form gate dielectric, thermal oxidation is performed on SiC. However, the presence of carbon atoms in SiC exhibits a significant difference to that of the oxide quality achieved from Si technology [126]. Although the interface of oxide and the epilayer of SiC MOSFET continues to improve, the quality and the understanding of the factors that control the quality is still far from a satisfactory level. The behavior of SiC power MOSFETs mainly depends on the characteristics of the SiO_2/4H-SiC MOS system, i.e., the amount of slow near-interface oxide traps (NIOTs) present inside the oxide layer, bulk traps, interface state density (D_{it}) distribution, and the modification of the 4H-SiC area near the SiO_2 interface by MOS systems. The brief location of NIOTs and D_{it} is shown in Figure 11 [127]. D_{it} is present near the edge of the valence band or conduction band at the SiO2/4H-SiC interface, and NIOTs are present inside the gate insulator.

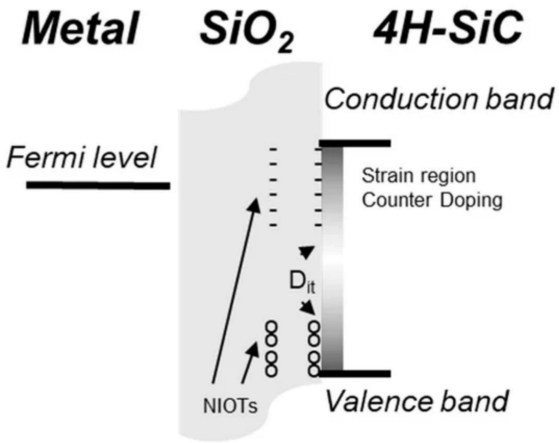


Figure 11. Graphical representation of the location of oxide traps and interface traps present at the interface of SiO2/4H-SiC [127].

The other important problem of SiC-MOS devices is the poor reliability of the gate oxide layer, such as the low dielectric breakdown field and threshold voltage instability. However, due to the recent advancement in technology and equipment, different SiO_2 passivation processes can be used to improve the trench mobility of the gate oxide layer of SiC devices. The passivation process can be achieved by thermal annealing in a chamber filled with nitrogen (N_2O or NO) [128,129]. The comparison of measured doping concentration and the D_{it} of various nitrogen-based annealing processes, based on some literature on 4H-SiC devices, is shown in Table 2 [130–134]. These data were fabricated on epitaxial layers or ion-implanted layers or MOS capacitors under nitrogen-filled conditions. Most of the annealing temperature of the passivation layer falls within the range of 1100–1400 °C.

Table 2. Summary of p-type doping concentration and interface state density (Dit) data of gate oxide in 4H-SiC devices.

Process	Temperature (°C)	N_A (cm^{-3})	D_{it} (cm^{-2} eV^{-1})	Ref.
NO	1250	1.3×10^{15}	2×10^{14}	[130]
NO	1250	2.3×10^{15}	8×10^{13}	[130]
NO	1250	2.7×10^{15}	6×10^{13}	[130]
NO	1175	8×10^{15} epi	N.A.	[131]
N_2O	1150	10^{17} imp	$3.6–7.2 \times 10^{11}$	[132]
N_2O	1300	1×10^{16} epi	4×10^{11}	[133]
N_2O	1410	5×10^{15} epi	10^{12}	[134]

3. SiC MOSFETs

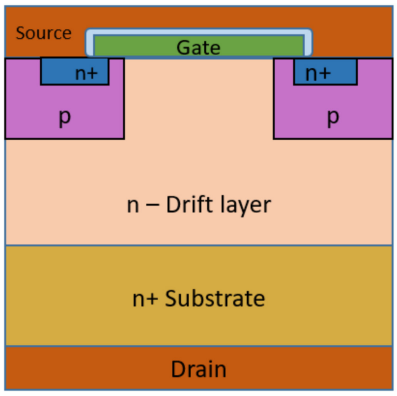
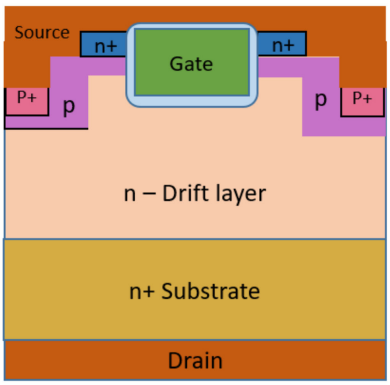
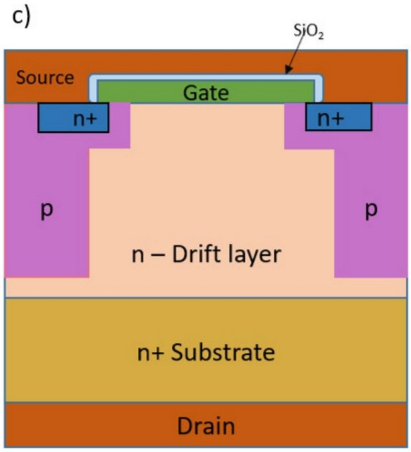
Since the beginning, MOSFETs have been the most successful devices and are mainly employed for switching operations in power converters [135]. The structure of SiC power MOSFETs is similar to that of Si MOSFETs with an insulated gate structure. SiC power MOSFETs can operate over a wide range of blocking voltage, with lower conduction and switching loss, as the device has less on-resistance than the Si counterpart and is much smaller [136]. The main advantage of SiC power MOSFETs is that the SiC power MOSFET combines the excellent material properties of SiC, which enhances the performance of the device. However, the SiC power MOSFET suffers from the carbon cluster introduction at the gate oxygen interface, which increases D_{it} at the gate–oxide interface, and thus, the channel resistance increases.

SiC Power MOSFETs are classified into different types depending on the structural modification of the gate and the drift region. The classification of the device is illustrated in Table 3. The two basic types of SiC MOSFET structures based on the gate modification are planar MOSFETs (DMOSFETs) and trench MOSFETs (UMOSFETs) [99], as shown in images (a) and (b) in Table 3, respectively. The planar types are further classified into conventional and super junction MOSFETs (SJ MOSFETs), as shown in image (c) in Table 3. A detailed discussion on the types of SiC MOSFETs can be found in the following sections.

3.1. Planar and Trench MOSFETs

The planar MOSFETs (or DMOSFETs), as shown in image (a) in Table 3, are a double diffusion MOS structure where the channel is formed by a double diffusion process and has the ability to withstand high voltage [137]. However, the performance of the device is affected by the poor channel mobility due to the scattering process at the interface of the 4H-SiC/insulator. This scattering causes a significant reduction in mobility at the interface when compared with that of the bulk. Moreover, the presence of parasitic junction FET resistance increases the conduction loss during the forward condition [138]. A 4H-SiC Planar MOSFET with a blocking voltage of 2.3 kV was proposed in [139]. The device has an acceptable gate oxide electric field with a gate oxide thickness of 27 nm. The device was fabricated using a commercial foundry. The device exhibits an improvement in $R_{on,\,sp,}$ and a high-frequency figure of merit (FOM) by 1.3 times when a 15 V is applied at the gate. However, the device suffers from gate voltage overshoot failure due to the thin gate oxide. A 4H-SiC Planar MOSFET with multiple floating guard-rings for edges termination was developed; the device can achieve a blocking voltage of 2.4 kV and a specific on-resistance of about 42 mΩ cm^2 [140]. The fabricated device exhibits a mobility of 22 cm^2/V.s in the channel and has a threshold voltage of about 8.5 V.

Table 3. Basic classification of SiC MOSFETs based on gate and drift structure.

Drift \ Gate	Planar	Trench
Conventional	a) 	b) 
Superjunction	c) 	

To minimize the conduction and switching loss in the planar MOSFET, the trench MOSFET or UMOSFET was developed for power application. The structure of trench MOSFET is shown in image (b) in Table 3; it has a vertical gate channel in U groove shape and a channel form at the sidewalls of the trench. This structure improved the channel migration rate and was able to eliminate the parasitic JFET resistance [141]. In addition, the on-resistance of the trench SiC MOSFET is half the planar SiC MOSFET. Hence, the trench SiC MOSFET design is preferred for power devices [98,142].

The first trench MOSFET was first introduced in 1992 by Palmour et al. [143]. In 1994, a trench MOSFET with a breakdown voltage of 150 V and $R_{on,\,sp}$ of about 3.3 mΩ cm^2 was demonstrated [144]. However, the device suffers from low mobility in the inversion layer due to the presence of a high electric field at the trench corner in the oxide, which restricts the breakdown voltage of the device. A 1.2 kV trench gate SiC MOSFET with a low switching loss was developed by Fiji Electric [145]. The proposed device exhibits a 48% reduction in on-resistance, with a higher threshold voltage than the conventional SiC planar MOSFET. A 4H-SiC Planar MOSFET with a blocking voltage of 2.3 kV was proposed [139]. The device has an acceptable gate oxide electric field, with a gate oxide thickness of 27 nm. The device was fabricated using a commercial foundry. The device exhibits an improvement in the specific on-resistance and high-frequency figure of merit by 1.3 times when the applied gate bias is 15 V. However, the device suffers from gate voltage overshoot failure due to the thinner gate oxide.

A 4H-SiC Planar MOSFET with multiple floating guard-rings for terminating the edges was developed; the device can achieve a blocking voltage of 2.4 kV and a specific on-resistance of about 42 mΩ cm^2 [140]. The fabricated device exhibits a mobility of 22 cm^2/V.s in the channel and has an 8.5 V threshold voltage. Purdue University introduced a trench MOSFET with a blocking voltage of 5 kV, with protection in the trench oxide and an extension in the junction termination [140,146]. A 4H-SiC planar MOSFET with the highest blocking voltage of about 10 kV was reported in [147].

The major issue of the common single trench is the concentration of the electric field at the bottom of the gate trench, which imposes a reliability issue to the device under long-term use. Additionally, it also suffers from the degradation of the switching performance and also the degradation of breakdown voltage due to the high value of gate-drain capacitance. To overcome the immature breakdown and reliability problem of the oxide, a double trench SiC MOSFET (DT MOS) was developed; it distributes the electric field concentration on the gate oxide into the source region [99,148,149]. The structure has a p+ shielding region to distribute the high gate oxide electric field to the source and drain p+ regions, which help in improving the breakdown voltage of the device [150]. The p+ shielding also improves the switching performance of the device by reducing the gate and drain charge coupling effect [151].

For high power switching applications, to increase the switching speed with lesser switching losses, a smaller value of reverse transfer capacitance (C_{GD}) and lower gate-drain charge (Q_{GD}) is necessary. A split-gate double trench MOSFET (SG-MOSFET) was proposed, with a better high-frequency FOM ($R_{on,\,sp} \times Q_{GD}$) than the DT MOS [152,153]. The structure has a separate upper and lower gate terminal; the upper gate terminal is connected to the gate voltage and is lower than the source voltage. The area under the active channel is reduced, which enhances the switching performance by reducing the gate-drain capacitance. Central implant MOSFET (CI MOSFET) is another type of structure demonstrated by Wolfspeed; it exhibits lower C_{GD} and Q_{GD} [154]. In power inverter applications, to reduce the SiC Chip area, SiC MOSFETs are used with free-wheeling diodes (FWD), namely, parasitic body PiN diodes. However, these diodes result in bipolar degradation and increase on-state power dissipation [155]. To overcome these issues, a different variety of embedded parallel Schottky barrier diodes (SBDs) with SiC MOSFETs has been proposed [156–162].

3.2. Superjunction MOSFETs

Superjunction (SJ) is a technique utilized widely to overcome the $R_{on,\,sp}$xA limitation in Si devices [163]. A superjunction MOSFET (SJ MOSFET) structure has alternating p and n layers in the drift region, as shown in image (c) in Table 3. The structure is formed by penetrating p+ columns into the n-epitaxial layer and follows the charge compensation principle, which helps in distributing the electric field uniformly inside the drift region [164]. As a result, the performance of the SJ MOSFET surpasses the conventional MOSFET performance. The main benefit of SJ MOSFETs is the linear relationship between $R_{on,\,sp}$ and the breakdown voltage (BV) [165], whereas for conventional MOSFETs (planar), the relationship is $R_{sp,\,on} \propto BV_{2.4–2.6}$ [166]. Moreover, SJ can reduce the $R_{on,\,sp}$ of the device without compromising the BV voltage of the device [163].

The structure of SJ MOSFETs can be grown by trench filling or by multi epitaxial growth. The epitaxial growth of SJ by trench filling is shown in Figure 12a and by multi epitaxial growth in Figure 12b. The trench filling epitaxial growth process is done by dry etching at the beginning to form a deep trench, and then, on the trench surface, an epitaxial layer is grown in the trench [167,168]. The multi-epitaxial growth method is a fabrication method that is used to achieve a certain thickness of drift-layer by combining epitaxial growth and the ion implantation method of fabrication [166]. The fabrication process of the SJ structure was first introduced by R. Kosugi et al. [169]. The measured breakdown voltage and $R_{on,\,sp}$ of the fabricated pn-pillar structure were 1545 V and 1.06 mΩ cm^2, respectively; the structure has a 5.5-µm-thick pn-pillar structure, grown using multiple

epitaxial growth method. The breakdown voltage and specific on-resistance achieved are almost the same as that of the theoretical limit of SiC. In addition, SiC-based SJ structures have been exhibited to show a reduction in on-resistance by 140 times and have a smaller pillar charge imbalance effect than the Si SJ structures [170].

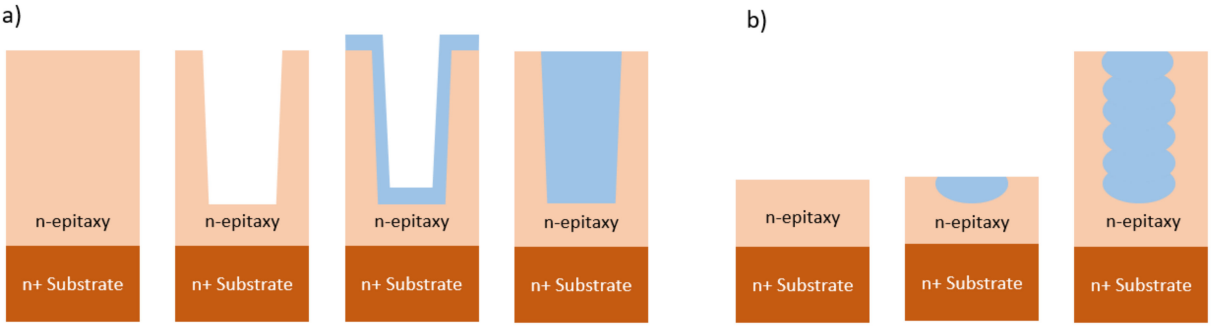


Figure 12. (**a**) Trench-filling epitaxial growth and (**b**) multi-epitaxial growth.

SiC SJ MOSFETs have also exhibited an excellent Baliga's figure of merit (FOM) ($BV^2/R_{on,sp}$) when compared with other SiC devices [171]. Simple analytical models for predicting the on-resistance and breakdown voltage of SiC SJ MOSFETs were proposed in [172,173]. Furthermore, SiC SJ MOSFETs exhibited a lower charge imbalance effect when compared with Si SJ MOSFETs in the drift region [170]. To achieve a better trade-off between the BV and $R_{on,sp}$, many researchers aimed to obtain the desired result by modifying the doping profile or the structure of the device. A SiC SJ MOSFET with a variation in the vertical doping profile (VVD) was proposed [164]; the device exhibits a better trade-off between the on-resistance and BV. The proposed device also shows the best results in both Baliga's and conventional FOM. A SiC SJ V-groove trench MOSFET with a breakdown voltage of 820 V and an on-resistance of 0.97 mΩ cm^2 was reported by Masuda et al. [174]. A SiC SJ V-groove trench MOSFET with a smaller on-resistance of 0.63 mΩ cm^2 and a breakdown voltage of 1170 V was demonstrated in [73]. The proposed device has a lower on-resistance than the SiC MOSFETs with a breakdown voltage of over 600 V.

A class of 1.2 kV SiC SJ MOSFETs, with an extremely low value of $R_{on,sp}$xA, a higher value of withstanding the short-circuit capability, and a significantly lower value of reverse recovery loss, was demonstrated in [73,175–177]. A DC-FSJ MOSFET (different concentration floating super junction MOSFET) was proposed [178], and the device was able to achieve a breakdown voltage of more than 3.3 kV, along with reduced $R_{on,sp}$. The $R_{on,sp}$ of the proposed structure was 25% less than conventional vertical MOSFET under the same conditions. The structure was fabricated by implementing multiple epitaxial growths with floating p-type structures and different concentrations of epitaxial layers. The BFOM of the device increased by 18% from FSJ MOSFETs and by 27% from vertical MOSFETs. A SiC SJ MOSFET with a very high breakdown voltage of 3.3 kV and a low $R_{on,sp}$ of 3.3 mΩ cm^2 at 27 °C and 6.2 mΩ cm^2 at 175 °C was developed in [179]. The proposed devices were able to exceed the theoretical limit of the unipolar SiC device.

Although SiC power devices have come a long way in improving their performances and satisfying the increasing demands, it is noteworthy to mention one of the key technical challenges faced, i.e., the reduction of electric field on the surface or at the edges of the device. The reduction of the electric field becomes more challenging with device miniaturization. Some in-plane edge termination techniques have been demonstrated for SiC power devices, which have a similar concept to that of Si power devices. The techniques include field plates [180,181], mesa structures [182], junction termination expansion (JTE) [183–185], floating field rings (FFR) [186,187], ramp structures [188,189], ion implantation, and hybrid solutions [37,190–193]. Edge terminations are generally used at the device periphery so that it supports the maximum amount of the bulk breakdown value [194]. Hence, robust and reliable edge terminations are one of the most important requirements that help in achieving the full SiC technology potential.

4. Device Reliability

SiC devices show great potential in the field of power electronics because of their high power handling capacity. SiC semiconductor materials account for the largest investment share in microelectronic design center and foundry R&D [31]. However, (D_{it}) in the SiC-SiO_2 system reduces the potential barrier between SiC and SiO2, thus resulting in increased carrier injection in the oxide. The stability of the SiC and SiO_2 interface is yet to reach that of the Si and SiO_2 stability due to the inherited small conduction band offset [195,196]. Microtubules, dislocations, grain boundaries, and epitaxial defects in SiC wafers and epitaxial layers have also been shown to reduce the critical breakdown electric field, leading to higher leakage currents and reduced device on-state performance [195,197,198]. Hence, reliability studies of SiC devices have become a focus of research, with increasing applications [195,199–201]. The substrate material, structure designs, and process technology affect the reliability of the device material.

The die-level failure mechanisms of SiC power MOSFET are mainly time-dependent dielectric breakdown (TDDB), accelerated life test high-temperature reverse bias (ALT-HTRB), neutron-induced device breakdown, and avalanche breakdown [202]. TDDB occurs during the on-state mode; it happens when there is a wear-out of gate-oxide. ALT-HTRB is also based on the wear-out of gate-oxide. The ALT-HTRB occurs when the wear-out is due to the high electric field in the oxide layer of the JFET region, which is linked to the high drain bias. The neutron-induced device breakdown occurs due to exposure to the neutron, which causes random failures, and the failure worsens if the device is at a higher elevation on the earth. The avalanche breakdown is caused by high electric field stresses [203,204]. The most potential reliability issues of SiC MOSFETs are threshold voltage degradation [205], gate-oxide degradation [206], and body diode degradation [207].

4.1. Threshold Voltage Degradation

Threshold voltage degradation occurs due to the instability of the threshold voltage. According to [208], the oxide trap charging and its activation are the two main reasons behind the instability of threshold voltage. The density of the defects present in the device depends on the processing technology. The oxide trap charging occurs through the direct tunneling mechanism, which results in the shifting of the threshold voltage of the device at room temperature [205,209]. The threshold voltage is shifted to the negative side due to the presence of oxide traps with a positive charge, which results from the tunneling of electrons from the oxide, and it is shifted on the positive side when the positive oxide traps are neutralized by the electrons tunneling back into the oxide; this process of tunneling of electrons is generally an ad infinitum process [209].

If the negative shift is large, then there is an increase in blocking state leakage current, which will result in device failure if the increase in leakage current is very large. Similarly, if the positive shift is very large, then there will be an increase in the on-resistance of the device. The dependency of the stability of threshold voltage on the NO annealing, which is done after post-oxidation, has been observed [205,209,210]. The activation energy of the trap is observed to be about 1.1 to 1.2 eV [209,211]; hence, there is an increase in instability of the threshold voltage of the device when it is exposed to high temperature (above 100 °C) bias for an extended time period.

4.2. Gate Oxide Degradation

The degradation of the oxide layer is also a major issue regarding the reliability of SiC MOSFETs as the device has a thin layer of oxide [212]. The oxide layer of the SiC MOSFET is small when compared with the Si MOSFET when trying to achieve a reasonable value of threshold voltage and transconductance [213,214]. Additionally, the lower tunneling barrier between SiC and SiO_2, i.e., 2.7 eV, makes the hopping of electrons from SiC to the oxide layer much easier [215].

The reliability of the gate oxide layer of SiC MOSFETs compared to Si devices can be discussed in three ways: (a) SiC MOSFETs have a lower inversion channel migration

rate [195]. As a result, a higher electric field is required to achieve a smaller channel resistance. Hence, there exists a trade-off between smaller on-resistance and better gate oxide reliability, (b) a higher density of interface states [195,216] that appear at the SiC-SiO2 interface reduces the barrier height, which results in the injection of more mobile hot carriers into the oxide from the doped SiC. Hence, the non-equilibrium nature of the carriers induces dislocations in the gate oxide, and (c) the smaller conduction band offset between the SiC and SiO_2 [217] introduces a higher Fowler-Nordheim tunneling current at a similar gate field and temperature. Therefore, the probability of time-dependent dielectric breakdown (TDDB) is higher. The relatively poor quality of the SiC and SiO_2 interface is the main restraining factor for the extrinsic reliability. The presence of a high concentration carbon cluster makes the interface very rough, which further enhances the introduction of the traps and defects on the interface as well as near interface regions [218,219].

There are two types of stresses that contribute to the degradation of the gate oxide layer, namely, high electric field stress and high-temperature stress [220]. An additional oxide trap near the interface is activated at high temperature and high electric field stress, which contributes to the trapping process [209]. The region of high electric field stress of UMOSFETs and DMOSFETs is shown in Figure 13 [195]. In UMOSFETs, an extremely high electric field is located in the oxide at the bottom of the trench [221]; the field concentration is more severe at the trench bottom and corner than at the lateral of the trench as the bottom of the trench is extended underneath the PN junction blocking voltage. In terms of controlling the electric field in the gate oxide, DMOSFET is the most promising SiC power MOSFET structure. The most widely studied indicators of gate oxide degradation include the Miller plateau time length [222], Miller plateau voltage amplitude [222,223], threshold voltage [209], drain leakage current, gate leakage current [224], and through-state resistance [222].

4.3. Body Diode Degradation

MOSFETs have a failure mode known as body diode degradation. This mode is a condition where forward current flows through the body diode of the MOSFET increase, and the resultant recombination energy of the electron-hole pair causes a defect called a "stacking defect", affecting the current path, which causes an increase in on-resistance and forward voltage of the body diode. The location of the body diode of the MOSFET is shown in Figure 14. The most prominent defect in SiC is the micropipe defect, where a hole through the top and bottom surface of the wafer is generated by lattice stacking misalignment. In addition to micropipes, there are many material defects. These defects can be broadly classified into wafer-level defects and epitaxial defects. Typically, SiC wafer defects are the nucleation point for epitaxial defects. Closed-core helical dislocation is an ordered crystalline defect, which is like a microtubule, and might continue to grow into the epitaxial layer depending on the epitaxial growth method. These defects can cause a decrease in the carrier life of the epitaxial layer [225].

The root cause of stacking faults at forward voltage is due to the expansion of base-plane dislocations (BPD) during forward conduction [226–228]. The coincident electrons and holes provide energy for the BPD to expand into a triangular stacking fault in the drift region [229]. The extended BPD penetrates through the epitaxial layer, creating a barrier for the conduction of multiple carriers, resulting in reduced carrier mobility [230]. The formation of these stacking faults increases the forward voltage and $R_{on,\,sp}$ [207,231]. Although the threshold voltage remains constant in the post-stressed state, a gradual increase in state leakage is observed, and the electronic state generated by the expanding BPD acts as a charge generator. Hence, the expanding BPD acts as a charge generation center in the drift region [207].

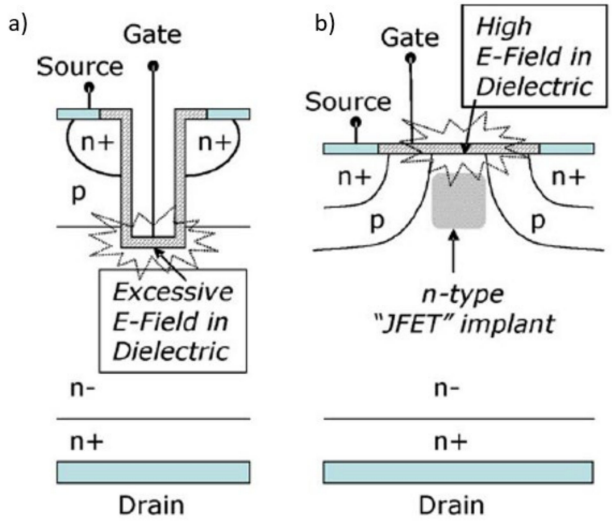


Figure 13. High electric field stress of (**a**) UMOSFETs and (**b**) DMOSFETs [195].

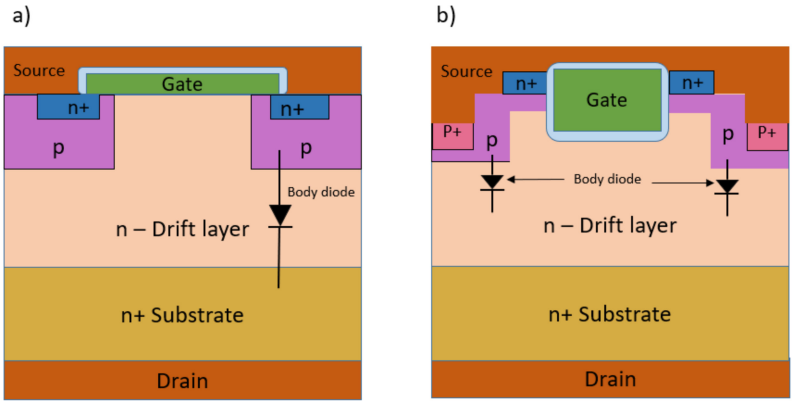


Figure 14. The location of body diode in (**a**) DMOSFETs and (**b**) UMOSFETs.

5. Conclusions

SiC power devices are widely used in power applications and have been researched extensively in various industries and academics. Along with the inherited superior material properties of SiC, SiC-based devices are able to be used in high speed, high voltage, and high-temperature operations. Hence, SiC power devices are employed in power converters, high-efficiency power inverters, and also in smart electric vehicles. This paper provides an extensive discussion about SiC materials, types of SiC power MOSFETs, their critical process steps, such as substrate growth, epitaxy layer, and ion implantation, and the impacts of critical process steps in improving the performance of the device. In addition, the reliability and failure mechanisms are also discussed. SiC power devices show great potential in achieving highly effective high-performance power applications.

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