Springer

Handbook of Semiconductor Devices

Rudan
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Springer Handbook of Semiconductor Devices

With 1335 Figures and 71 Tables

Springer

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Foreword by Chihiro Hamaguchi

The first semiconductor device, named "point-contact transistor," was demonstrated on the 17th of December 1947 by John Bardeen, Walter Brattain, and William Shockley at Bell Laboratories. About a month later (January 1948), Shockley invented the "junction transistor." The first demonstration of a radio receiver made with point-contact transistors was performed in December 1947. The design of solid-state devices for electrical amplification was organized at Bell Laboratories under the guidance of Shockley, who was also interested in a new device to control surface electrons with a metal gate. A FET-like transistor had already been patented in the USA by Julius Edgar Lilienfeld in January 1930; the idea was not realized because of the high density of surface states in silicon. The difficulty was resolved by using an oxide surface layer processed in high-temperature vapor atmosphere, as proposed by C. Frosch in 1954; the deposition of a metal gate on the oxide layer was achieved by J. Attala and D. Kahng at Bell Laboratories in 1959. First, PNP and NPN junction transistors were commercialized and used to design solid-state circuits; however, the Si-MOSFET, invented afterwards, revealed its superiority over the junction transistor, in view of designing and manufacturing digital circuits.

So many people were involved in the early development of integrated circuits (ICs); among them, Jack Kilby of Texas Instruments (hybrid integrated circuit, 1958) and Robert Noyce at Fairchild Semiconductor (monolithic integrated circuit, 1959) played a very important role in the opening of IC technologies. The advancement of IC technology is well explained by Moore's law: "the number of transistors in a chip of integrated circuits doubles every two years." Moore's expectation expresses quite well the history of ICs from 1970 till 2020. This advancement has been supported by many new technologies, materials, processes, circuit-design strategies, and others. Starting from the simple planar technology, structures are now more complex and three dimensional. The technological revolution in the field of the semiconductor devices radically changed many aspects of the social organization (communications, economy, transportation, and all the primary necessities of everyday life), so that in the present time, human beings find it difficult to survive without ICs.

Semiconductor-device operations are based on fundamental electrical and optical properties of the materials, as anyone can easily agree about just by leafing through this *Springer Handbook of Semiconductor Devices*. The knowledge of energy band structures is essential for understanding any device operation. In other words, energy band calculations provide knowledge on electronic and optical properties of semiconductors. Many semiconductor properties are well understood on the basis of the effective masses of electrons in the conduction band and holes in the valence bands, in addition to the (direct or indirect) band gap. Pioneer data from cyclotron resonance experiments in Ge and Si were interpreted by the theory based on $k \cdot p$ perturbation method by G. Dresselhaus, C. F. Kip, and C. Kittel in 1955, and revealed the many-valley structure of the conduction band and the spin-orbit splitting of the valence bands in these elemental semiconductors. The energy band calculation in the full Brillouin zone for 14 semiconductors of the diamond and zinc-blende structures was reported for the first time by M. L. Cohen and T. K. Bergstresser in 1966 by means of the pseudopotential method. More advanced theoretical approaches have been reported afterwards, and some of them are dealt with in this handbook.

This *Springer Handbook of Semiconductor Devices* provides a quite useful framework suitable to guide the interested reader across a massive amount of information, and achieves an almost complete review of the basic and advanced knowledge of semiconductor devices. The editors planned to cover the present status and future development of semiconductor devices, including physics, structures, processing, designing, and simulation. Part I is concerned with the technological aspects of semiconductor devices, and deals with the manufacturing of semiconductor memory devices together with the technology of processing, measuring parameters, advanced lithography, and dielectric materials. In addition, FinFETs and advanced technologies for future materials and devices are discussed. Part II deals with basic semiconductor devices and applications, including Si-based devices such as MOS devices, MOSFETs, capacitors, and CCDs. Part II also deals with the topics of sensors, semiconductor lasers, and solar cells. Part III deals with new-generation devices and architectures, such as resonant-tunneling devices, bioelectronics, spin-based devices, quantum-computing devices, and other innovative structures. Part IV is devoted to device modeling and process simulation, where both classical device-simulation tools and more advanced methods are described in detail.

Even though many kinds of semiconductor devices are still designed and produced, and new and advanced devices are expected to appear in the future, this handbook can be considered a milestone reference, since it covers a large spectrum of devices and surveys their structures and properties in depth. The editors selected the topics cleverly, and the contributors are specialized and outstanding scientists from all over the world. Therefore, on the basis of my experience in this field, I consider this *Springer Handbook of Semiconductor Devices* the most important guide book for researchers, in industries and academic institutes, as well as graduate students. I congratulate the editors and all the authors for bringing such an excellent handbook to publication.

Professor Emeritus at Osaka University
IEEE Life Fellow
March 2021

Chihiro Hamaguci, Ph. D.

Foreword by Herman Maes

I was born in the year 1947, the blessed year so to speak of the revolutionary invention of the point-contact transistor by Shockley, Bardeen, and Brattain. Perhaps this explains my fascination to this day for semiconductors, the physics, the devices, and the technology, in that order. I had the pleasure to admire this first "transistor" at the Bell Labs in Murray Hill, New Jersey. I moreover have had the privilege to meet John Bardeen and attend a few of his classes during my postdoctoral research stay at University of Illinois Champaign-Urbana in 1974–1975. I even had a brief, accidental encounter with William Shockley in 1974. I graduated as an electronic engineer at the Katholieke Universiteit Leuven, Belgium, in 1971 at a time when the semiconductor industry had in fact only just come out of the starting blocks. Intel just launched its Intel 4004, the first processor-on-chip consisting of 2,300 transistors. We were still within the first phase of the semiconductor saga, a few years after Gordon Moore had reported his findings on the evolution in size of the first integrated circuits (IC) and launched his predictions, later known as Moore's Law. Only on the basis of a few data points, Moore concluded and predicted that the number of transistors in ICs on a chip would double every year with innovations in lithography as the main driving force to enable transistor scaling. How more visionary could a man be? And exactly these kinds of bold statements have been so typical and have, as we experienced, in fact been driving the development of this fascinating semiconductor technology field over the past nearly 65 years. This is commonly referred to as self-fulfilling prophecy.

During our engineering training in the late 1960s, a somewhat older professor, close to retirement, actually strongly doubted whether those semiconductors would eventually break through and therefore still spent a lot of attention to the usefulness, properties, and application of vacuum tubes. Fortunately for us, there was this other, young, dynamic, visionary professor, Roger Van Overstraeten (the founder of imec in 1984), who had obtained his

Ph.D. from Stanford University and who had returned a few years earlier to our university. He was so enthusiastic and inspiring about the latest developments and opportunities of semiconductor science and technology that he could convince many of us to fully engage ourselves in that direction. My fascination was aroused and from then gradually turned into passion and hunger for knowledge. So, we started to look for suited books. In these early years, appropriate textbooks were still scarce. The books that were being produced mostly focused on specific technological and solid-state physics issues. I personally remember a few of these while in college, the SEEQ series on the bipolar transistor, Andy Grove's *Physics and Technology of Semiconductor Devices*, and of course Simon Sze's standard work *Physics of Semiconductor Devices*, which saw its first edition in 1969. Over the past 50 years, numerous new handbooks have become available, many of them covering in detail specific disciplines or aspects of the strongly expanding field of semiconductor devices. However, at this early stage there was a need of books providing a broad-scope and balanced mixture of state-of-the-art, prospect, insight and context of all inherent aspects of semiconductor technology, devices and applications, offering high level treatments with more than mere encyclopedic knowledge, with attention to interdisciplinary aspects and to the mutual support of the various disciplines: such books, in fact, remained rather scarce.

After about 45 years in the twentieth century and 20 years in this twenty-first century, the industrialized world has been marked by extremely rapid technological (r)evolutions. We witnessed the incredible and far-reaching developments of the semiconductor industry with growing amazement and disbelief, even to those who were involved in the process from the first rank. This was largely due to the extremely successful scaling endeavors by research and industry. The Intel 4004 processor that we referred to earlier was realized in the 10 μm technology node, today we have reached the 5 nm node (a feature size scaling by 2,000), allowing fabrication of chips with over 50 billion transistors! Semiconductor technology today is a very mature, established industrial discipline. The entire semiconductor market is close to 500B$ and expected to further grow year after year, with even a doubling in 10 years' time. This industrial progress went hand in hand with (and was also steered by) profound societal changes in its most diverse aspects and led us into the Information Age. Semiconductor devices, ICs, and products played an undeniably prominent role in these tremendous transitions. They are now used in every corner of our "digital" society and are taking an increasingly crucial and essential role in almost all economic sectors, information technology, multimedia, communication, automation, robotics, transport, medical and health sector, games, education, environment, energy, cryptography, smart buildings, and smart cities.

But we are today on the verge of a new disruptive landslide. The transition from the Information Age to the Digital Age is taking place, with expected revolutions in the interfaces for speech recognition, augmented reality, virtual reality, and artificial intelligence, just to name a few. Our businesses and the economy will have to realize that this transition will not come gradually, in small steps. After all, a characteristic of a revolution is that the change comes abruptly and is accompanied by breaking with the past. And if we had thought to have reached the pinnacle of technologically possible developments, we realize that many even more far-reaching technological breakthroughs will be needed in the future.

The semiconductor industry is facing a new era in which device scaling and cost reduction will no longer continue to proceed on the path followed for the past few decades. Further advanced nodes, even when feasible, may no longer bring the desired cost benefit. Moreover, R&D investments in new lithography solutions and devices below 5 nm nodes are rising substantially. Therefore, the insatiable and ever-increasing demand in the digital era forces the industry to come up with ever more innovative and sophisticated technology solutions to bridge the gap and improve cost/performance while at the same time adding more functionality through integration. The so-called More-than-Moore devices (including

MEMS and sensors, CMOS Image Sensors, power devices, THz devices) represent this new functional diversification of technologies, combining performance, integration, and cost not merely limited to CMOS scaling. Their role is expected to become more and more predominant. Semiconductor device and technology engineers and scientists will therefore have to continue the quest for ingeniously new electronic devices and functionalities. We are in fact on the cusp of big changes.

More than ever, semiconductor researchers, scientists, and engineers will have to maintain the widest possible view of these rapidly evolving fields. They need to be constantly and continuously curious, interested, amazed, fascinated, and triggered by the evolution and the developments in their own fields but also in the domains adjacent but often complementary to their own specialization. They therefore need to acquire thorough yet easy-to-digest, appropriate, timely, and reliable knowledge on the state of the art but also on the newest developments and trends in these domains. And above all, they count on obtaining this information from specialists and experts in these fields.

A handbook is a book capable of being conveniently carried as a type of ready reference work, providing information, facts, insights, and instructions on a particular field, subject, or technique, designed to be easily consulted and providing useful, quick, but solid and reliable answers in a certain area. It covers and offers scientific basics, fundamentals, methods of research, general principles, functional links, and review of established or potential applications. Moreover, even in rapidly expanding fields, the information and content need to be sufficiently timeless.

Springer Handbooks respond to such needs fully and successfully. They strive to provide and maintain the highest standards of references in well-selected fields and key areas of physical and applied sciences and technology. They are intended for practitioners in academia and industry, as well as graduate students. They are allowing fast yet comprehensive review and easy retrieval of reliable key information.

It is Springer Handbooks' tradition to come up *at the right time* with new, well-considered initiatives for launching appropriate reference books. Recent examples have been the handbooks on nanotechnology, robotics, mechanical engineering, and automation.

Today certainly is the right time to launch this Springer Handbook on semiconductor devices, considering the transition to the even more challenging post-scaling era.

Conceiving and realizing such a handbook is a daring, challenging, and ambitious endeavor. It is a major undertaking and requires vision, significant organizational skills, and commitment. One also needs to have a network of experts who look up to the editor.

This Springer Handbook on semiconductor devices you have in hand fully meets the strict requirements and high-level standards of the Springer Handbook series. It provides comprehensive coverage of numerous technological and fabrication aspects of advanced semiconductor devices, focusing not only on advanced "traditional" structures but also on ingeniously new and often futuristic, beyond CMOS, and More-than-Moore concepts for many applications. Rightly so, strong attention was paid to the indispensable advanced modeling and simulation methods for predictive and supporting purposes, as well as an outlook toward near or far future needs. This handbook is not the first one covering semiconductor technology and device disciplines, and it will undoubtedly not be the last one. But the differentiator, the USP of this handbook according to me, is this mixture of broad scope, thoroughness of treatment with still sufficient accessibility, the wide range of concepts for many applications, and the foresight. And, worth noting, all chapters have been written by international experts, innovators, and leaders in their field. The reasoned interpretations of developments in each area are commendable and often unique. The editors did a wonderful and tremendous job in not only selecting the 45 rightful and relevant topics but also in inviting the right specialists to treat these topics and share their expertise and experience with the knowledge-hungry reader.

This has resulted in an extensive, voluminous yet digestible standard work that deserves to be on the shelf of graduate students of nanoelectronics, and researchers in academia and industry who are active or intend to be active in this field and who are looking for in-depth, up-to-date information. Finally, also practicing scientists and engineers who want to expand their know-how in adjacent fields will strongly benefit from this book.

I would like to congratulate the editors and all the authors for their excellent contributions, one by one, bringing this ambitious and formidable challenge to a successful conclusion.

Professor Emeritus Katholieke Universiteit Leuven, Belgium Herman E. Maes, Ph.D.
Former Senior VP imec, Leuven, Belgium
March 2021

Preface

No other class of materials than semiconductors, since the early identification of their electrical, optical, and thermal properties at the beginning of the nineteenth century, has been so deeply investigated and used to design all kinds of devices. The first theoretical models about the physics of semiconductors, based on quantum-mechanical grounds, fueled the design of solid-state diodes and transistors; these, in turn, have opened new horizons to electronics, computer science, and sensors, and have greatly impacted the global market with annual revenues of the order of 500 billion US dollars in the present days.

In turn, semiconductor companies pushed ahead the search of new semiconductor materials and structures suited for specific applications, and urged academia and the industry's R&D toward the elaboration of more and more powerful simulation tools to inquire about the effects of miniaturization, interfaces, and doping on device performance and reliability, or to benchmark specific semiconductor properties before investing resources in expensive innovations of the production lines.

All the above justify the effort of putting together, in this *Springer Handbook of Semiconductor Devices*, many cross-disciplinary competences about present-day and near-future semiconductor devices, namely modern concepts in solid-state physics, material science, growth and process technology, device design, and advanced simulation strategies.

When we speak about semiconductor devices, what we consider "future" is very often already "present time" somewhere in the world. Thus, this handbook not only includes the most recent progress in research and technology of conventional semiconductor devices and sensors but enlarges its view to include some specific topics related to new materials and designs, presently at the frontier between science and technology, nonetheless suitable to be employed in the next-generation semiconductor-technology challenges.

The handbook is organized in four parts: 1. Technological Aspects; 2. Basic Devices and Applications; 3. New-Generation Devices and Architectures; 4 Modeling. Almost 100 leading scientists from both academia and industry were invited to contribute to the 45 chapters of the handbook, which has been conceived for professionals and practitioners, material scientists, physicists, and electrical engineers working at universities, industrial R&D, and production. Each chapter is self-contained and refers to related topics treated in other chapters when necessary, so that the reader interested in a specific subject can easily identify a personal path through the massive contents of the handbook.

We are very grateful to all the authors who joined this ambitious enterprise, to the referees who generously contributed to improve the quality of the final outcome, to Springer's editors who patiently followed our work step by step, and, last but not least, to Prof. Chihiro Hamaguchi (Osaka University) and Prof. Herman Maes (KU Leuven and imec) for providing forewords based on their long-term experience in the field of semiconductor science and technology.

May 2021 M.R., R.B., S.R.

Contents

Part I Technological Aspects 1

1 CMOS Manufacturing Processes 3
Aaron Douglas Lilak and Patrick H. Keys

2 Semiconductor Memory Technologies 37
Paolo Fantini, Giorgio Servalli, and Paolo Tessariol

3 BCD Process Technologies 67
Giuseppe Croce, Antonio Andreini, Paola Galbiati, and Claudio Diazzi

4 Measuring Techniques for the Semiconductor's Parameters 117
Alessandra Alberti, Filippo Giannazzo, Francesco La Via, Salvatore Lombardo, Antonio M. Mio, Giuseppe Nicotra, Stefania M. S. Privitera, Riccardo Reitano, Fabrizio Roccaforte, Corrado Spinella, and Emanuele Rimini

5 Interconnect Processing: Integration, Dielectrics, Metals 169
Shyng-Tsong Chen, Nicholas A. Lanzillo, Son Van Nguyen, Takeshi Nogami, and Andrew H. Simon

6 Wet Chemical Processes for BEOL Technology 219
Cornelius Brown Peethala, James J. Kelly, Donald F. Canaperi, Mahadevaiyer Krishnan, and Takeshi Nogami

7 From FinFET to Nanosheets and Beyond 259
Nadine Collaert

8 Advanced Lithography 279
Alberto Roncaglia

9 Advanced Technologies for Future Materials and Devices 309
Francis Balestra

Part II Basic Devices and Applications 329

10 MOS Capacitors, MOS Transistors, and Charge-Transfer Devices 331
Massimo Rudan, Susanna Reggiani, and Giorgio Baccarani

11 Electrostatic Doping and Devices 371
Raymond J. E. Hueting and Gaurav Gupta

12 Planar MOSFETs and Their Application to IC Design 391
Salim El Ghouli and Denis Rideau

13 Silicon Power Devices 423
Noriyuki Iwamuro

14 Silicon Carbide Power Devices 491
B. Jayant Baliga

15 GaN-Based Lateral and Vertical Devices 525
Matteo Meneghini, Srabanti Chowdhury, Joff Derluyn, Farid Medjdoub, Dong Ji, Jaeyi Chun, Riad Kabouche, Carlo De Santi, Enrico Zanoni, and Gaudenzio Meneghesso

16 Bipolar Transistors and Silicon Diodes 579
Jean-Michel Sallèse and Farzan Jazaeri

17 Memory Challenges 603
Carlo Cagli and Luca Perniola

18 Silicon Sensors 635
Benedetto Vigna, Ernesto Lasalandra, Sarah Zerbini, and Mario Aleo

19 Solar Cells 699
Stephen M. Goodnick and Christiana Honsberg

20 X-Ray Detectors 747
Safa Kasap and Zahangir Kabir

21 Photodetectors Based on Emerging Materials 777
Jiantong Li and Mikael Östling

22 Terahertz Electronic Devices 807
Frédéric Aniel, Gregory Auton, David Cumming, Michael Feiginov, Sebastian Gebert, Tomás González, Chong Li, Alvydas Lisauskas, Hugues Marinchio, Javier Mateos, Christophe Palermo, Aimin Song, Jeanne Treuttel, Luca Varani, and Nicolas Zerounian

23 Semiconductor Lasers 851
Martin R. Hofmann and Stephan W. Koch

Part III New-Generation Devices and Architectures 865

24 Heterojunction Tunnel Field-Effect Transistors 867
Paolo Paletti and Alan Seabaugh

25 Carbon-Based Field-Effect Transistors 905
Zhenxing Wang, Daniel Neumaier, and Max Christian Lemme

26 Negative Capacitors and Applications 931
Muhammad Ashraful Alam, Nicolò Zagni, Atanu Kumar Saha, Niharika Thakuria, Sandeep Thirumala, and Sumeet Kumar Gupta

27 Flexible Electronics and Bioelectronics Devices 959
Chen Jiang, Xiang Cheng, Hanbin Ma, and Arokia Nathan

28 Biodegradable Electronics 1019
Giovanni Antonio Salvatore, Lan Yin, and Fanqi Dai

29 Resistive-Switching Memories 1043
Peng Huang, Yudi Zhao, and Jinfeng Kang

30 Phase-Change Memories 1093
Enrico Piccinini and Carlo Jacoboni

31 Spin-Based Devices for Digital Applications 1123
Viktor Sverdlov and Siegfried Selberherr

32 Memristive/CMOS Devices for Neuromorphic Applications 1167
Valerio Milo, Gerardo Malavena, Christian Monzio Compagnoni, and Daniele Ielmini

33 Nanoelectronic Systems for Quantum Computing 1201
David K. Ferry

Part IV Modeling 1231

34 Compact/SPICE Modeling 1233
Wladek Grabinski and Daniel Tomaszewski

35 Process Simulation 1259
Jürgen Lorenz and Peter Pichler

36 A Digital Twin for MEMS and NEMS 1303
Jan G. Korvink, Kirill V. Poletkin, Yongbo Deng, and Lihong Feng

37 Macroscopic Transport Models for Classical Device Simulation 1335
Johann Cervenka, Robert Kosik, Markus Jech, Martin Vasicek, Markus Gritsch, Siegfried Selberherr, and Tibor Grasser

38 Grid Generation and Algebraic Solvers 1383
Aurelio Giancarlo Mauri, Benedetta Morini, Simona Perotto, and Fiorella Sgallari

39 Spherical Harmonics Expansion and Multi-Scale Modeling 1413
Bernd Meinerzhagen and Christoph Jungemann

40 Charge Transport Models for Amorphous Chalcogenides 1451
Rossella Brunetti and Massimo Rudan

41 Application of the $k \cdot p$ Method to Device Simulation 1491
Antonio Gnudi, Elena Gnani, Susanna Reggiani, and Giorgio Baccarani

42 *Ab initio* Methods for Electronic Transport in Semiconductors and Nanostructures 1515
Massimo V. Fischetti, William G. Vandenberghe, Maarten L. Van de Put, Gautam Gaddemane, and Jingtian Fang

43 Quantum Transport in the Phase Space, the Wigner Equation 1559
Jean Michel Sellier and Philippe Dollfus

44 The Nonequilibrium Green Function (NEGF) Method 1583
Kerem Y. Camsari, Shuvro Chowdhury, and Supriyo Datta

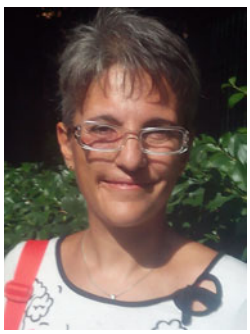
45 Tight-Binding Models, Their Applications to Device Modeling, and Deployment to a Global Community 1601
Gerhard Klimeck and Timothy Boykin

Index 1641

About the Editors

Massimo Rudan received a degree in electrical engineering in 1973 and a degree in physics in 1976, both from the University of Bologna, Italy. His research interests are in the field of physics of carrier transport and numerical analysis of semiconductor devices and solid-state sensors. In 1986, he became a visiting scientist, on a one-year assignment, at the IBM Thomas J. Watson Research Center at Yorktown Heights, NY, studying the discretization techniques for the Boltzmann transport equation. In 1990 he became Full Professor of Electronics, and in 2021 Professor Emeritus, at the University of Bologna. An IEEE Life Fellow, and a recipient of the 1998 Körber Foundation Award, Massimo Rudan has coordinated several research projects funded by the European Commission, international companies and foundations, the National Council of Research, and the National Ministry of University and Research.

Rossella Brunetti received her master's degree cum laude in physics in 1981 and her Ph.D. degree in physics from the University of Modena, Italy, in 1987. Since 2002, Rossella Brunetti is Associate Professor of Condensed Matter Physics in the Department of Physics, Informatics and Mathematics at the same university. Her research activity has mainly been focused on charge transport, in both semi-classical and quantum conditions, in semiconductor structures and devices. Rossella Brunetti is experienced in a variety of numerical techniques (mainly the Monte Carlo, Molecular Dynamics, and Hydrodynamic Methods) which have been applied to validate theoretical models against experiments and to predict new effects. In the past few years, Rossella Brunetti focused her research on transport properties of chalcogenide materials in view of their applications in the field of emerging memory devices.



Susanna Reggiani received her Ph.D. degree in electrical engineering from the University of Bologna in 2001. Since 2001, she is with the Department of Electronics and the Advanced Research Center for Electronic Systems (ARCES) at the same university. Her scientific activity has been devoted to the physics, modeling, and characterization of electron devices, with special emphasis on transport models in semiconductors. She has been involved in projects dealing with TCAD analysis of power MOSFETs, modeling and characterization of hot-carrier stress degradation and reliability of wide-bandgap semiconductors, and modeling of package influences on high-voltage ICs. In 2020, she became full professor in the School of Engineering at the University of Bologna.

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Part I

Technological Aspects

CMOS Manufacturing Processes

1

Aaron Douglas Lilak and Patrick H. Keys

Contents

1.1 Introduction . . . 3

1.2 CMOS FinFET Process . . . 4

1.3 Ion Implantation . . . 4
1.3.1 Beam Line Ion Implant . . . 4
1.3.2 Ion Stopping . . . 5
1.3.3 Amorphization and Channeling . . . 5
1.3.4 Impact of Implant Process Knobs upon Resultant Distributions of Implanted Ions and Implant Damage . . . 8
1.3.5 Consideration for Implant into Nonplanar Surfaces . . . 10
1.3.6 Plasma Implant . . . 10
1.3.7 Implant Sputtering and Backscattering . . . 11
1.3.8 Implant Ion Beam Mixing . . . 12

1.4 Thermal Annealing . . . 12
1.4.1 Annealing Methods . . . 12
1.4.2 Diffusion . . . 14
1.4.3 Dopant Activation/Clustering/Deactivation . . . 16
1.4.4 Semiconductor Recrystallization . . . 17
1.4.5 Simulators . . . 17
1.4.6 Oxidation . . . 17
1.4.7 Solid Source Diffusion . . . 17

1.5 Deposition . . . 17
1.5.1 Deposition Methods . . . 17

1.6 Etch . . . 19
1.6.1 Wet Etch . . . 19
1.6.2 Dry Etch . . . 20
1.6.3 Chemical Mechanical Polish or Chemical Mechanical Planarization . . . 20
1.6.4 Etch Selectivity . . . 20
1.6.5 Atomic Layer Etch . . . 21
1.6.6 The Coloring Problem . . . 21

1.7 Lithography . . . 21
1.7.1 Fundamental Lithographic Process . . . 22
1.7.2 Lithographic Constraints Due to Light Source . . . 22
1.7.3 The Role of the Stepper/Scanner and Impact to Feature Resolution . . . 23
1.7.4 The Role of Resist in Lithographic Process . . . 23
1.7.5 Lithographic Enhancement Techniques . . . 23
1.7.6 Multiple Patterning Approaches . . . 24
1.7.7 Post-optical Lithographic Techniques . . . 27

1.8 Metalization and Contact Formation . . . 29
1.8.1 Silicide Contact to Transistor . . . 29
1.8.2 Interconnect Stack . . . 30
1.8.3 Damascene Metal Processes . . . 31
1.8.4 CMOS Process Technology Development through Nontraditional Techniques . . . 31
1.8.5 Substrate Engineering and Hybrid CMOS Integration . . . 32
1.8.6 Stress Engineering . . . 34

1.9 Summary . . . 35

References . . . 35

Abstract

In this chapter, we will discuss the common fabrication processes and methods utilized in the fabrication of CMOS devices. This discussion will include doping techniques such as ion implantation and diffusion along with a discussion of etch, deposition, and lithography techniques used to pattern and fabricate devices at the nanometer scale. This chapter will conclude with a survey of foreseeable changes which are emerging in regard to semiconductor manufacturing processes.

Keywords

Semiconductor processing · TCAD · Etch · Deposition · Lithography · CMOS · Ion implantation · Stress engineering · Oxidation

1.1 Introduction

Over the last 70 years, transistors have progressed from being manufactured by hand out of chunk of germanium, gold foil, and glue at Bell Labs to the integrated devices which

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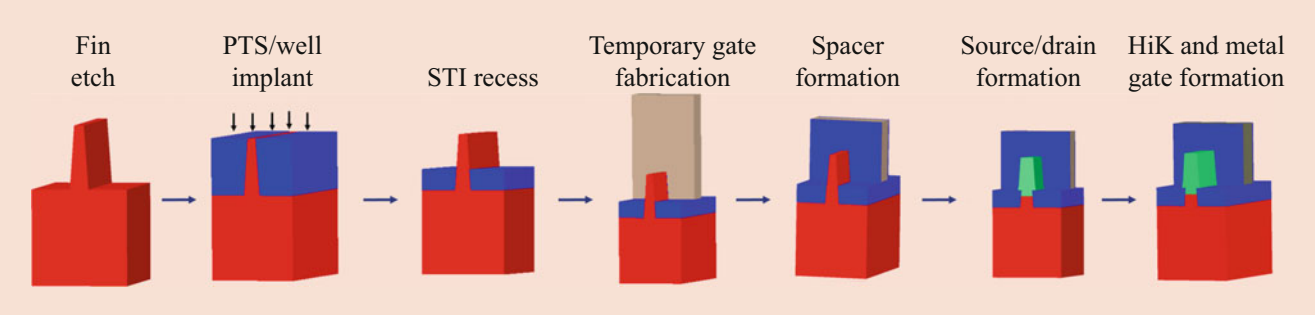


Fig. 1.1 Example process steps of a FinFET transistor fabrication flow using a variety of process techniques

have densities measured in the billions/cm^2 and emerge from multi-billion dollar facilities that look more like hospitals than factories. This chapter will discuss the manufacturing processes used to create these devices at such scale and quantity.

This discussion will begin with an introduction to doping and activation techniques including ion implant and diffusion. As semiconductor assemblies are built in a layer-by-layer manner by adding and subtracting materials and dopants, the tools used for deposition, etch, and lithography will be described. Finally, a discussion of foreseeable process-related trends will conclude this chapter.

1.2 CMOS FinFET Process

The fabrication of transistors is more an art than it is a science; however, these fabrication processes do tend to follow a similar series of operations. While there are embodiments and numerous variations of these steps and operations and resultant geometries; a (much) simplified block process flow for fabrication of a FinFET transistor through front-end fabrication is shown in Fig. 1.1. The operations and flow variations required to implement these processing steps and those required to add electrical interconnections in the back-end fabrication are described within this chapter.

1.3 Ion Implantation

Ion implantation is a means of material modification used in semiconductor fabrication. This material modification may be done for purposes of introducing doping, creating regions of damage, removal of material or cleaning of a surface, modification of etch properties of a material, or for purposes of intermixing a material surface in order to modify a subsequent deposition process. Ion implantation is utilized in both front-end and back-end processes. Ion implantation tools are broadly categorized as either beam line or plasma immersion tools.

1.3.1 Beam Line Ion Implant

Beam line ion implantation tools used in modern CMOS fabrication can trace an origin to the ion implantation device patented by William Shockley in [31] . In his patent "Forming Semiconductive Devices by Ionic Bombardment," Shockley first illustrates how atoms of one material may be ionized from a gas phase, accelerated to a known energy with an applied voltage, and then implanted into a semiconductor wafer.

In Shockley's original patent, a gas containing a dopant specie, for example, boron trifluoride, is allowed to flow into the assembly through tubing indicated as (22) in Fig. 1.2. Atoms of this gas are ionized and accelerated through use of an applied voltage between a cathode (32) and an anode (31). A wafer (25) is placed on the holder assembly (26) and conductive base (48, 49). By manipulating the flow rate of gas and arc used to ionize the particles, a beam current may be adjusted. This current may be measured as it exits the conductive base in the implanter and is a measure of the number of implanted charges and hence related to the number of implanted impurity ions. By adjusting the voltage applied between the cathode and anode, the energy of each implanted ion may be manipulated in order to change the range and distribution of the implanted ions. The ions may be introduced at a tilt or rotation by manipulating the orientation of the wafer holder assembly.

Modern ion implantation tools like in Fig. 1.3 have evolved from this basic configuration of Shockley, but share the same fundamental concepts. Mass selection is accomplished through passing the ion beam through a magnetic field and series of apertures. Additional magnets and computerized control enable the shaping of the ion beam, and the beam can be rastered across the wafer. Single-wafer tools have evolved into batch process tools which mount wafers on a rotating assembly and can process

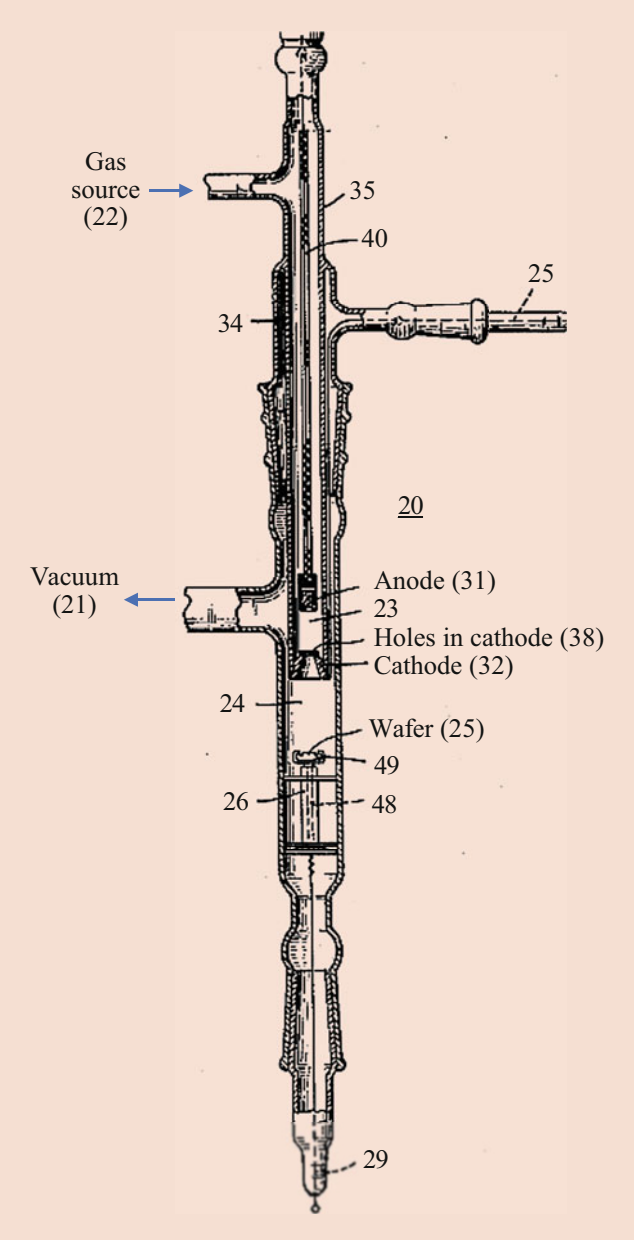


Fig. 1.2 The ion implanter assembly proposed in Shockley's original patent for an ionic bombardment apparatus. Most of the functional elements of this crude device are in place in modern ion implanters

multiple wafers simultaneously. Wafer temperature can now be adjusted during the implant process, and specialized tools have been developed for high-current, high-voltage, and other applications.

While ion implantation was initially largely integrated in CMOS processes for the purposes of introducing doping, it has since evolved as a means of material modification. Particularly in the BEOL metallization and contact processes, beam line implant continues to find new applications. A representative list of implant species from the periodic table is shown in Fig. 1.4.

1.3.2 Ion Stopping

An implanted ion interacts with both the electrons and atoms in a target material and loses kinetic energy at a rate of dE/dx in a process referred to as stopping. Nuclear stopping involves interactions with the atoms of the target material, and electronic stopping involves interactions with the electrons of the target material, and the total stopping is represented by the sum of the two components. Several derived and empirical relationships have been proposed to express these nuclear and electronic stopping components. These stopping powers may be simulated with the aid of a computer program such as SRIM as shown for silicon in Fig. 1.5.

1.3.3 Amorphization and Channeling

For a single-crystal semiconductor material, the stopping power of the crystal to the implanted ion can vary significantly as the orientation of the beam relative to the crystal surface is changed. Ion implanters enable this orientation adjustment through tilt of either the ion beam or surface of the wafer relative to the ion beam and through rotation of the wafer relative to the ion beam. Ions which experience a relatively lower stopping power are referred to as being channeled. Channeling is common for low-dose implants such as V_t adjust or well implants or for implants of lower-mass species such as boron.

Plots such as that of Fig. 1.6 indicate a very significant implant beam orientation dependence to the resultant implant profile. A fluctuation of less than a degree in tilt or rotation or slight fluctuation in wafer orientation can result in a significant difference in a channeled tail. This effect can result in a fabrication process with very high sensitivity to implant beam orientation or with significant process fluctuation. One approach to alleviate this sensitivity is to intentionally implant highly channeled implants such as boron wells (P-well) in an off-channel orientation such as 7 degrees tilt or 7 degrees tilt/22 degrees rotation for a (100) orientated silicon crystal where possible. This effect is shown in Monte Carlo simulation in Fig. 1.7.

Amorphization refers to the process of accumulating damage within an ordered crystalline or polycrystalline material until the atomic positioning within the crystal becomes randomized. A randomized crystal will not experience channeling on ions. Ion implantation is a common means used for amorphizing semiconductor crystals due to ability to adjust the depth of amorphization through the use of ion energy, the ability to determine the area of amorphization through the use of lithography to pattern implant blocking layers, and the ability to adjust the amount of implant damage through the use of implant dose (see Fig. 1.8).

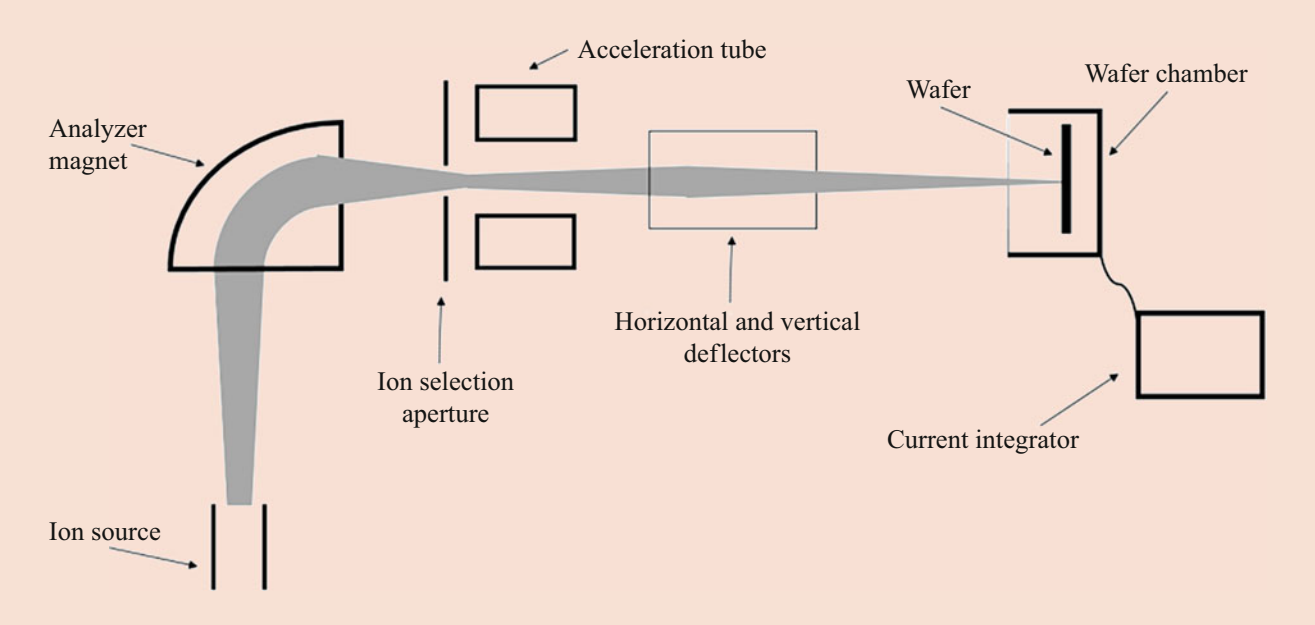


Fig. 1.3 A schematic of a modern ion implanter

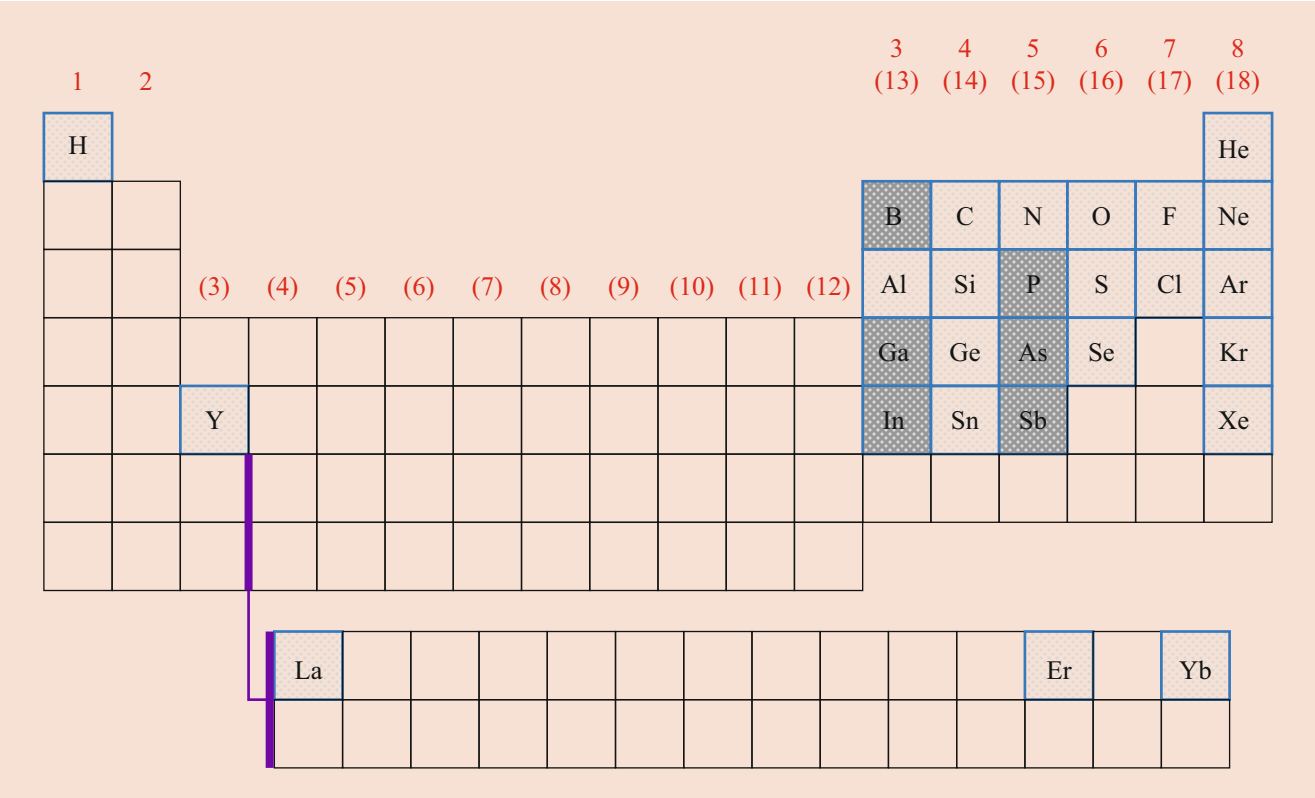


Fig. 1.4 Periodic table showing a partial list of beam line implant species regularly available for CMOS processing. The darker shaded atoms comprise a historical list of the silicon dopant species and the lighter shaded atoms reflect those which are commonly used for material modification purposes. This list continues to expand

Ion = Silicon [14], mass = 27.977 amu

Target density = 2.3212E+00 g/cm^3 = 4.9770E+22 atoms/cm^3
======== Target composition ==========

Atom name	Atom numb	Atomic percent	Mass percent
Si	14	100.00	100.00

==========

Bragg correction = 0.00%
Stopping units = MeV / (mg/cm^2)
See bottom of table for other stopping units

Ion energy	d*E*/d*x* elec.	d*E*/d*x* nuclear	Projected range	Longitudinal straggling	Lateral straggling
10.00 keV	4.592E–01	1.687E+00	174 A	87 A	63 A
11.00 keV	4.816E–01	1.695E+00	188 A	93 A	68 A
12.00 keV	5.031E–01	1.701E+00	201 A	99 A	72 A
13.00 keV	5.236E–01	1.704E+00	215 A	105 A	76 A
14.00 keV	5.434E–01	1.706E+00	229 A	110 A	80 A
15.00 keV	5.624E–01	1.705E+00	242 A	116 A	84 A
16.00 keV	5.809E–01	1.704E+00	256 A	121 A	88 A
17.00 keV	5.988E–01	1.702E+00	269 A	127 A	92 A
18.00 keV	6.161E–01	1.699E+00	283 A	132 A	96 A
20.00 keV	6.494E–01	1.690E+00	310 A	143 A	103 A

Fig. 1.5 SRIM simulation of stopping components for a silicon implant into a silicon substrate

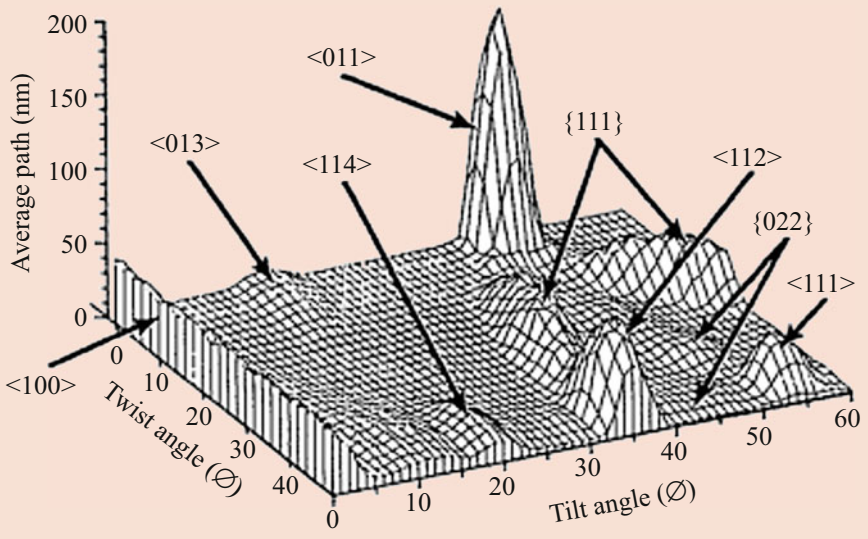


Fig. 1.6 Monte Carlo simulation results of 5 keV B-11 ions implanted into (100) oriented silicon as a function of tilt and twist of the wafer. Regions of this plot reflecting a low average path indicate implant into a randomized crystal orientation, while those which experience longer implant average path lengths reflect crystal orientations which present a highly ordered atomic cross section to the ion implant beam

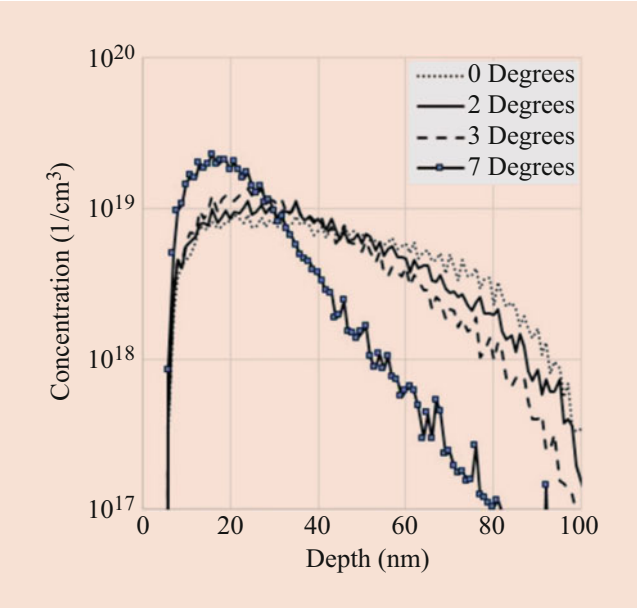


Fig. 1.7 Monte Carlo simulation of 3 keV boron implant at 5e13/cm^2 dose implanted into a (100) orientated silicon wafer. A slight variation in tilt angle toward (110) results in a substantial reduction in channeling tail of the implant

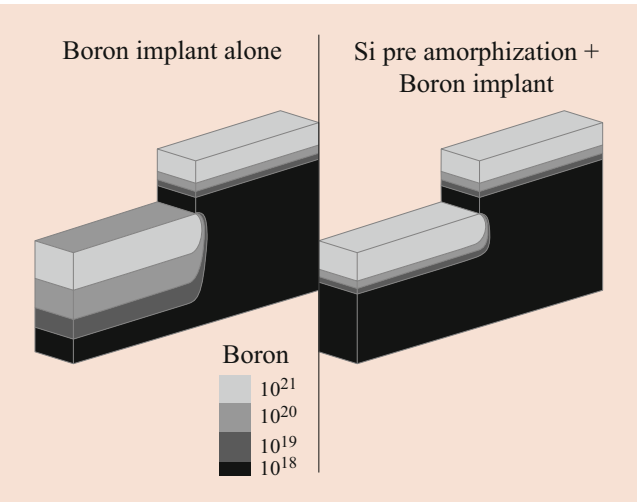


Fig. 1.8 Simulation showing the impact of a pre-amorphizing implant upon a subsequent non-amorphizing boron implant. In both cases, the boron implant is identical. In addition to a much more abrupt vertical implant profile, the lateral profile is also several nm more abrupt for the process which includes a pre-amorphizing implant

Amorphization may be accomplished by the same implants which are used to induce doping. This process is referred to as self-amorphization. For a group IV semiconductor crystal such as Si or Ge, self-amorphization commonly occurs with higher mass implanted species such as In, Sb, As, or P. Self-amorphization with lighter atoms such as B may be achieved through the use of cluster species such as BF2. In a region which is self-amorphized, the damaged location and ion positioning will largely overlap. It is common in a self-amorphized material to see a strong dependence between the implanted dose and measured projected range of the implant with the lightest dose self-amorphizing implants experiencing a longer projected range due to channeling which occurs before the self-amorphization process is completed.

Amorphization may also be accomplished through the use of a separate non-doping or co-implant specie. For a group IV semiconductor, amorphization without introducing doping is commonly achieved through the use of an implant specie from group IV such as Si, Ge, or Sn or through the use of an implant of a noble gas specie such as Ar, Kr, or Xe or through the use of species such as F or cluster implant species which do not contain a dopant atom. In a separately amorphized or pre-amorphized region, the damage and ion profiles need not overlap.

In addition to amorphization, another means of minimizing channeling is through the use of an amorphous capping layer placed above a crystalline semiconductor region. In this case, the amorphous capping layer serves to randomize the ion trajectories before they reach the semiconductor.

Amorphization and implant damage are important effects in that they significantly impact the channeled tail of an implanted ion distribution. This can manifest as a shallower vertical or more abrupt lateral junction. For this reason, CMOS processes which involve tip extension implants, source/drain implants, or source/drain contact implants may involve an implant of a non-doping specie performed prior to the implant of a doping specie. This implant may or may not be (separately) amorphizing and serves to confine the implanted doping laterally which may lead to improved device short channel effects, reduced device V_t, and higher channel mobility.

1.3.4 Impact of Implant Process Knobs upon Resultant Distributions of Implanted Ions and Implant Damage

The electrical behavior and characteristics of a transistor are heavily impacted by the placement and concentration of dopant atoms. Integration and optimization of a transistor fabrication process requires a thorough understanding of the positioning of both damage and ion, as well as an understanding of how processes downstream from the implant operation are impacted by the results of a prior implant operation. Such understanding is normally gained through the use of TCAD tools and the models upon which these tools are based. The principal outputs of these simulations are the ion profile and the crystal damage profile. These quantities may then be utilized in TCAD models to create profiles of excess damage which may drive dopant diffusion, grow and nucleate extended defects such as {311}'s and end-of-range

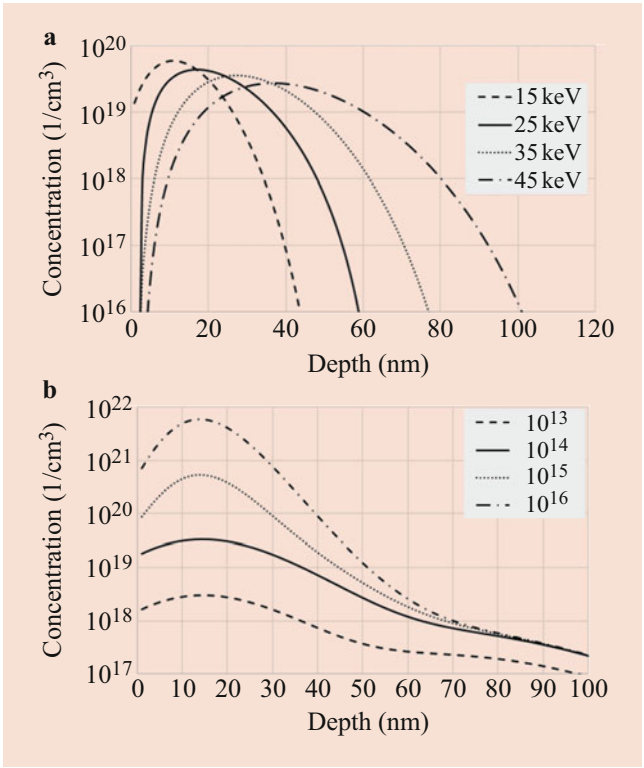


Fig. 1.9 (**a**) Simulation of arsenic implant at 15/25/35/45 keV at fixed 1e14/cm^2 dose into a randomized (100) Si crystal. As energy of the implant is increased, the resultant profile is deeper and broader. (**b**) simulation of 10 keV phosphorus implant into an undamaged (100) Si crystal. As the dose is increased, the fraction of channeled ions is decreased which results in a profile shape change

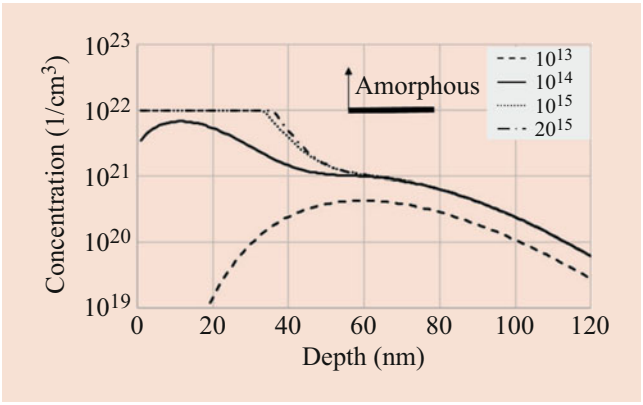


Fig. 1.10 Simulated cascade damage resultant from a 10 keV phosphorus implant into (100) Si at doses of 1e13 to 2e15/cm^2. The 1e15 and 2e15/cm^2 implants will result in an amorphous layer being formed in the structure. As implant dose is increased, the peak cascade damage also increases until amorphization is reached. Increasing dose further will lead to an increase in the depth of amorphization

(EOR) loops, lead to dopant deactivation or clustering, and initiate recrystallization of an amorphized layer. Therefore, it is critical to understand the impact of implant parameters upon these quantities.

The two most fundamental implant parameters are dosage/dose and implant energy. The implant dose is commonly measured in units of 1/cm^2 and represents the number of ions which are implanted per unit area as measured perpendicular to the ion beam. The measurement of implant dose perpendicular to the ion beam results in an effective dose reduction at wafer surface for an implant in which the wafer is tilted at time of implant and not orientated perpendicular to the ion beam.

Implant profiles for arsenic and phosphorus are shown in Fig. 1.9. As energy of the implant is increased, the resultant profile is deeper and broader. As the dose is increased, the fraction of channeled ions is decreased which results in a profile shape change. Both of these effects can be modeled with either Monte Carlo implant simulations or with continuum models which utilize shape functions (as shown in these figures).

The implant damage can also be modeled with TCAD tools, as demonstrated in Fig. 1.10. As would be expected, increasing the implant dose will lead to an increase in implant damage until amorphization is reached. In many TCAD implant models, amorphization is represented as a threshold function in which a region is amorphized if the damage exceeds a value. This damage is a measure of the quantity of vacancies which have been introduced to the crystal lattice due to collisions and recoil events and the interstitials which are created as the recoiled atoms come to rest. Computationally efficient models such as those of Hobler have been proposed to describe these effects and are commonly used in TCAD tools to describe implant damage. A measure of the vacancies injected from an implanted ion can also be determined through a Monte Carlo implant simulator such as MARLOWE or SRIM.

Until recently, most ion implants used in CMOS processes were performed at room temperature. Modern implant tools, however, now have the ability to perform the implant into either a heated or cooled substrate. An implant into a heated substrate will tend to dynamically heal implant damage during the implant, and heated implants have found applications for situations where amorphization must be avoided such as high-dose well implants for a bulk FinFET process. Conversely, cryogenic (or chilled) implants have found applications where abrupt amorphizations are desired such as for pre-amorphization implants done at contact formation.

For high-volume manufacturing, it is common to operate the implanter at the highest reasonable beam current (and hence the lowest time on the tool to achieve the desired dose); however, ion implanters can operate at different beam current levels, and this is a knob which is also used for process optimization at times. It has been shown experimentally that

implant-induced defects and their thermal dissolution can be modulated by the implanter beam current.

1.3.5 Consideration for Implant into Nonplanar Surfaces

A beam line ion implantation tool is a "line-of-sight" tool. During CMOS fabrication, it is common for there to be a height variation in the top surface to be implanted. As implants are tilted and rotated, this elevation change in top surface can lead to regions of the semiconductor wafer being blocked or partially blocked from the implant beam by another higher elevation feature located lateral to that exposed location within the line-of-sight of the implant beam as shown in Fig. 1.11. In modern CMOS fabrication, especially for FinFET processes, this effect often determines the tilt/rotation process window bounds for an implant process. To overcome this limitation, tilted and rotated implants are commonly performed in pairs at the same tilt (offset by 180 degrees of rotation) or in quadruples (offset by 90 degrees of rotation) depending upon the application. This shadowing effect also manifests as a nonuniformity in implant profiles which is introduced with irregular patterns.

Height variation in an implanted surface may also lead to proximal doping effects. The most familiar of these effects is a well-proximity V_t effect in which the threshold voltage of a device is dependent upon the distance from the well boundary. These effects are manifested as a lateral variation in implanted dose which is due to implanted ions scattering from a location higher in elevation on the wafer and being re-implanted elsewhere as shown in Figs. 1.12 and 1.13. This ion scattering can originate from either a topographical feature of the assembly (for instance, a fin or gate structure) or the blocking and resist layers used to mask off regions of a wafer for which implant is not intended.

1.3.6 Plasma Implant

A second category of ion implant tools used in CMOS fabrication are those which place a target wafer within a plasma source or sheath. These tools are referred to broadly as plasma immersion ion implantation (PIII) tools. Once placed within a plasma, the wafer is subjected to a DC bias or a pulsed voltage which serves to form an electric field between the target and the plasma and to draw out the charged particles which are implanted into the target. The plasma composition may be varied and both p-type and n-type implant options have been developed.

A main advantage of this technique results from alleviating the line-of-sight restriction present with a beam line ion

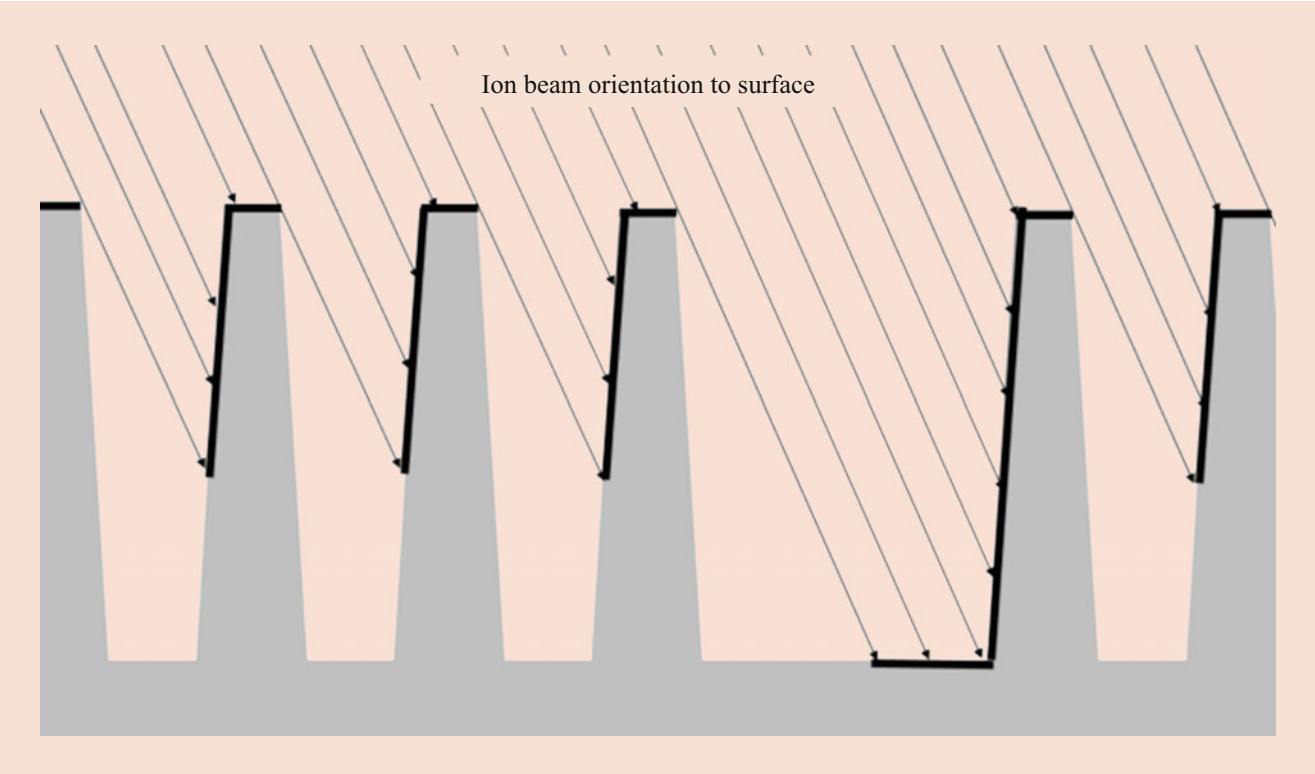


Fig. 1.11 A representation of shadowing which occurs with a tilted ion implant and a surface with height variation. Areas of the surface which are exposed to the implant beam have a dark top interface. This effect leads to a nonuniform doping profile across the array of fins or the grating pattern

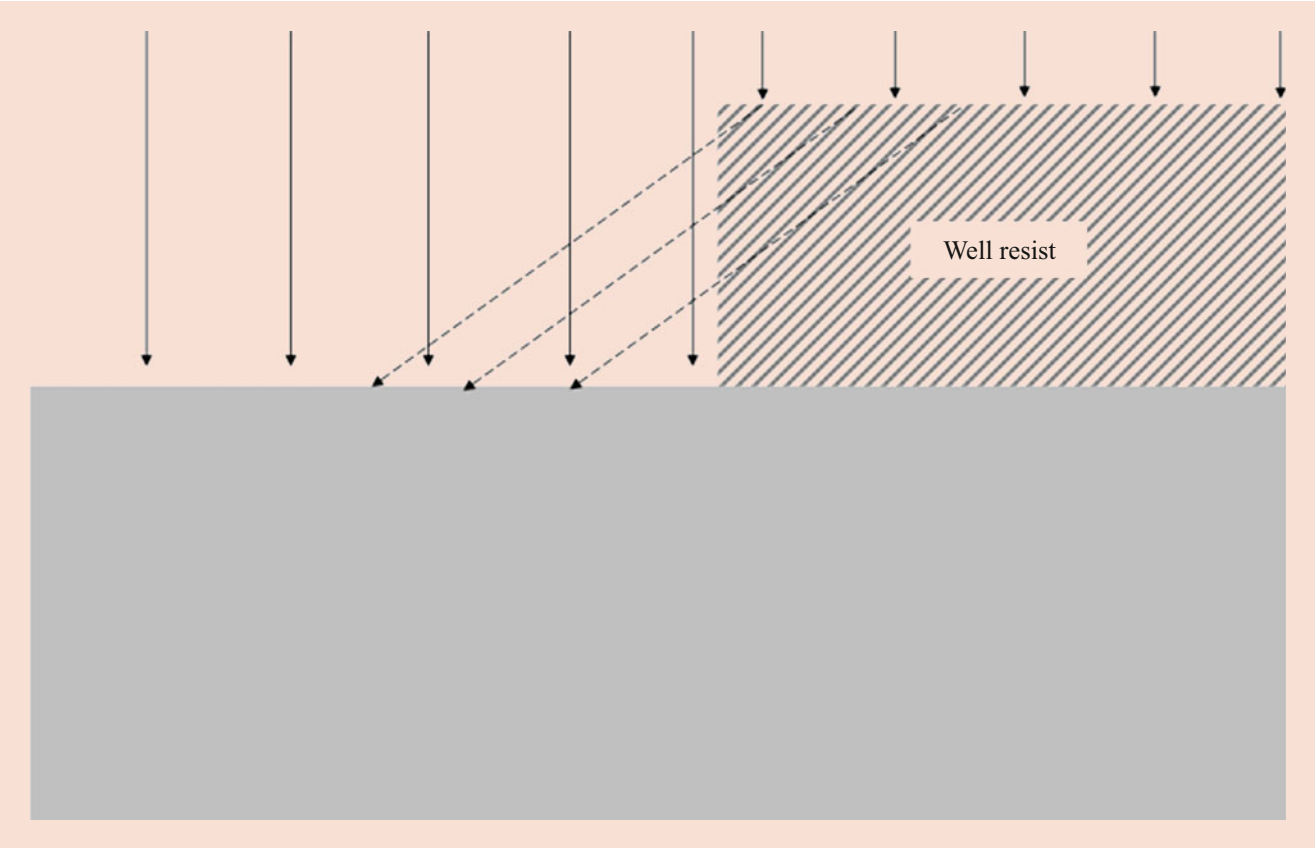


Fig. 1.12 Well proximity doping effect. Ions from the incoming ion beam (solid lines) are scattered (dashed lines) at a higher elevation within the well resist and are re-implanted at a lower elevation proximal on the wafer. The net dose of implanted ions becomes a function of distance to the well boundary and devices which are formed within the region where these scattering events occur may experience a layout-dependent performance variation

implant tool as the target wafer is immersed within the plasma sheath directly. In theory, this enables conformal dosing to be achieved on nonplanar target surfaces. In practice, some degree of non-conformality is present even with a plasma source ion implant. A second advantage of this technique is that it enables very high throughput or high doses to be achieved (to ~e18/cm^2). At these high doses, percent level concentrations of impurities may be introduced to a target. For this reason, many common applications of a plasma-source ion implant in CMOS manufacturing entail near-surface material transformation of a target from one material or phase to another.

Plasma implant does have several key disadvantages that have traditionally limited the applicability of the technique to niche applications. Chief among these limitations is that the implanted species consist of every specie present in the plasma. For instance, a plasma implant intended to introduce boron doping from a BF_3 plasma source may implant a soup of all permutations of B and F molecular and atomic species to the substrate. In addition to charged species in the plasma, neutral species are commonly injected into the plasma to improve conformity and may also be implanted through a recoil effect. These species will differ in mass which may yield an implant distribution profile with a longer tail than would a beam line implant, which presents a severe drawback if an abrupt implant profile is desired. In addition to implanting desired doping or impurity species, it is often necessary to implant high doses of unintended species as well when a plasma implant is used.

1.3.7 Implant Sputtering and Backscattering

In addition to damaging the crystalline structure of the target material, implanted ions may also eject material from the surface of the target or themselves be ejected or reflected. These processes, diagramed in Fig. 1.14, are referred to as implant sputtering and backscattering. Sputtering may be used advantageously in certain CMOS and memory processes such as non-selective surface clean operations, and backscattering is generally an unavoidable consequence of high-angle implant operations or implant operations into structures with topographical variation. In general, this sputtering process is most significant for higher mass implanted species with incidence at high angles relative to the localized surface implanted at high doses (>~ e15/cm^2). The efficacy

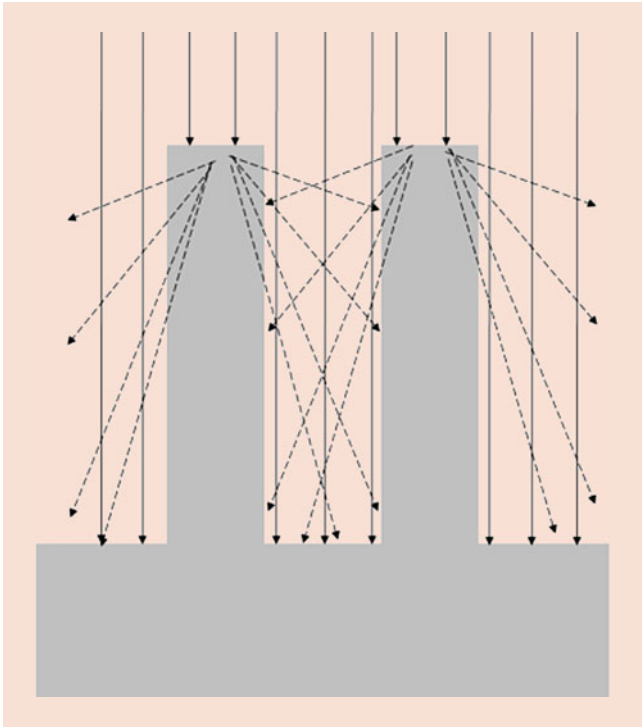


Fig. 1.13 Proximal doping resultant from normal incidence implant into a fin or grating structure. Even in instances where the sidewalls of the fin or grating structure are parallel to the original ion beam (solid lines), they are still implanted due to scattering events (dashed lines) which occur in adjacent fins or grating structures

of the sputtering process is specified by the sputtering yield which is a value representing the mean quantity of target atoms ejected for each incident implanted ion. The calculated sputtering yield from SRIM software is demonstrated in Fig. 1.15. For cases where the target material is not composed of a single atomic specie, the sputtering yield of each atomic component of the target may be determined, and in general, these quantities will differ. A common manifestation of sputtering for CMOS FinFET processes is that sharp corners are eroded and rounded with high-dose n-type implants (such would be present with a NMOS source/drain or contact implant). In addition to certain CMOS processes, the sputtering process also forms a basis for several analytical techniques such as SIMS (secondary ion mass spectrometry) profiling.

1.3.8 Implant Ion Beam Mixing

In certain CMOS processes, it is necessary to implant through a capping layer, a superlattice structure, or a stack of materials. This is particularly applicable to implants used for workfunction modulation in the gate stack of materials and implants used in contact processes. In these situations, the implant beam can recoil and mix the stacked or lattice layers together and blur the boundaries that once existed between the distinct regions or materials and introduce unintentional impurities or doping into the layers beneath. Figure 1.16 shows these events can be predicted with the aid of TCAD simulation tools or simulators such as SRIM.

1.4 Thermal Annealing

The process of annealing is used to influence the properties of the materials within semiconductor devices. It is commonly performed to control the location and electrical activation of dopants, setting the p-n junction locations. Alternatively, it can stabilize a material that has just been deposited or damaged from a previous process step like ion implantation or etching.

As shown in Table 1.1, different materials can withstand different temperatures and times. Silicon devices can be annealed in the range of 500 °C for hours to 800 °C for minutes and up to 1200 °C in the millisecond timeframe. Semiconductor materials with higher melting points such as SiC can sustain higher thermal budgets. Conversely, semiconductors with lower melting temperatures like Ge need to be annealed at a reduced thermal budget. Similarly, once the metals used for source, drain, or gate contacts are introduced into the semiconductor devices, annealing temperatures must be kept moderate, usually below 400 °C so as not to diffuse the metals or deactivate the dopants in neighboring semiconductor regions.

There is a strong correlation between cohesive energy of elements and their melting temperature, Fig. 1.17. Similarly, the self-diffusivity of materials has also been correlated to their cohesive energy. This can be used as a guide to understand the relative temperature ranges that different materials can tolerate.

1.4.1 Annealing Methods

Furnace annealing is a batch process in which multiple wafers are loaded into a heated quartz tube at atmospheric pressure with a flowing gas such as nitrogen, N_2, or forming gas, 5% H_2 in N_2, and maintained at the desired temperature for hours. Vertical tube furnaces have become more popular than the earlier favored horizontal tube furnaces. Examples of these are diagramed in Fig. 1.18, showing the differences.

Rapid Thermal Annealing

Rapid thermal annealing (RTA) uses an array of heat lamps to increase the temperature of the exposed wafers, enabling

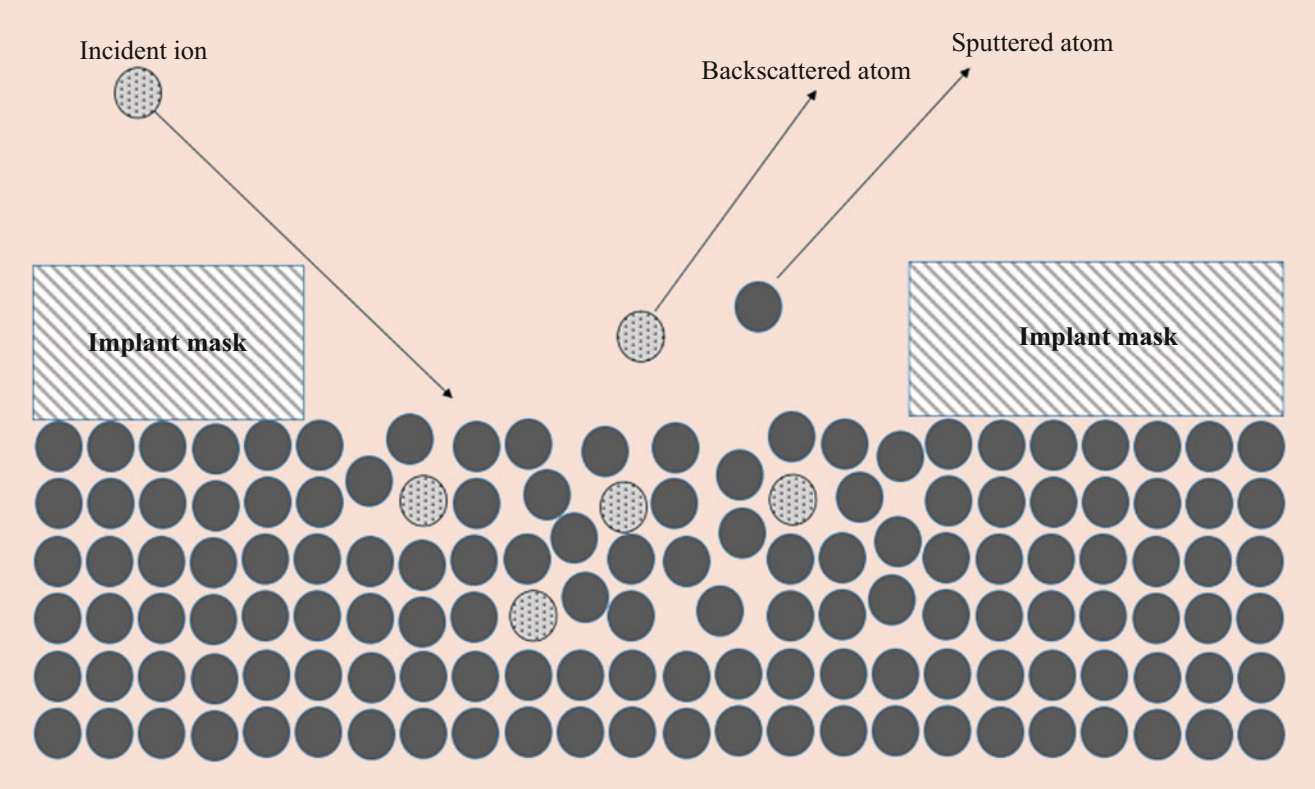
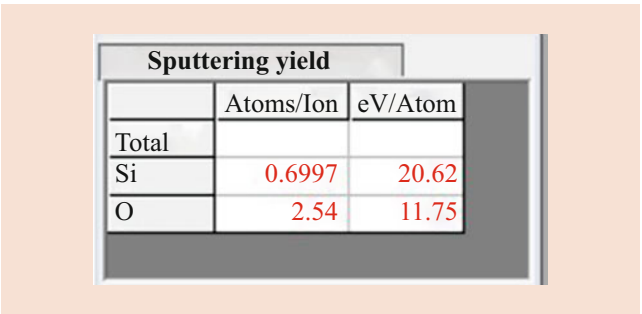


Fig. 1.14 The sputtering and backscattering process. An incident ion is implanted into a substrate and may induce lattice disorder, cause atoms of the surface to be ejected through a sputtering event, or be scattered themselves and ejected from the substrate in a backscattering event



Sputtering yield

	Atoms/Ion	eV/Atom
Total		
Si	0.6997	20.62
O	2.54	11.75

Fig. 1.15 Sputtering yield extraction from a Si implant into SiO_2 performed with SRIM. In this simulation, the incident ion was Si directed at a horizontal initial surface with a beam tilt of 45 degrees relative to the surface. For each implanted Si ion, on average ~0.7 Si substrate atoms and 2.54 O atoms are sputtered

faster ramp-up and cooling than furnace annealing. This method can bring the anneal time down to the range of seconds as opposed to hours [1]. The short dwell time at maximum temperature for the RTA process makes it ideal for minimizing the diffusion of implanted dopants, forming shallow channel to source/drain junctions, maintaining high dopant activation, oxidizing ultrathin gate dielectrics, and making contacts through silicide reactions with metals. Advanced methods use "spike anneals," wherein high temperature ramp rates are used for both heating and cooling, while also minimizing the dwell time at peak temperature. The extreme case of this is commonly referred to as "flash annealing" in which case a high-arc discharge lamp is used to expose the surface of the wafer to a millisecond flash of light resulting in thermal absorption and heating. The wafer itself acts as a heat sink, leading to rapid cooling of the surface after the flash exposure. Configuration like the one shown in Fig. 1.19 utilize two sets of lamps to provide RTA heating of the wafer backside and high temperature flash on the top surface of the wafer.

Laser Heating

Laser heating has also been used to anneal semiconductor materials. In this application, a laser is rastered across the surface of a wafer resulting in localized heating that can be as short as nanoseconds. The thermal profile can be compressed to high temperatures for ultrashort durations as shown in Fig. 1.20 to reduce thermal diffusion budget.

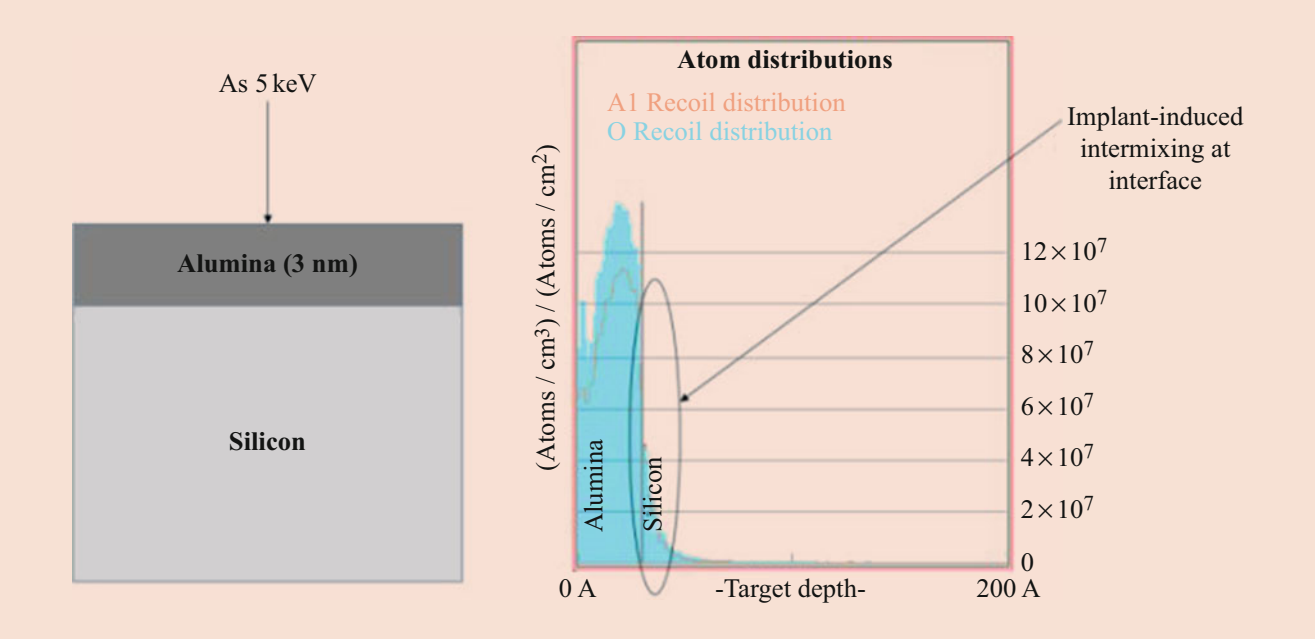


Fig. 1.16 An example of ion beam mixing which distorts the interface between a capping layer and the underlying materials. In this hypothetical example, aluminum and oxygen atoms are recoiled several nm into the underlying silicon material

Table 1.1 Material melting temperatures and cohesive energies

Material	Melting temperature (°C)	Cohesive energy (eV/atom)
SiC	>2730 (decomposes)	–
GaN	>2500	–
Si_3N_4	>1800 (decomposes)	–
SiO_2	>1600	–
Si	1415	4.63
SiGe	Varies between Ge and Si based on Ge%	–
Ge	937	3.85
GaAs	1238	–
InP	1062	–
W	3422	8.90
Ti	1668	4.85
Ni	1452	4.44
Cu	1083	3.49
Al	659	3.39

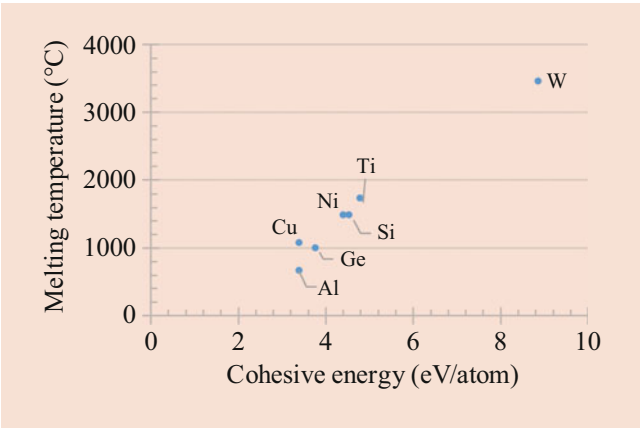


Fig. 1.17 The relationship between melting point of a material and the cohesive energy showing that materials with higher cohesive energy generally have higher melting points

1.4.2 Diffusion

The introduction of dopants must be done in a controlled manner to reliably set the electronic properties of different regions. During annealing, dopants can redistribute and diffuse into neighboring areas. Figure 1.21 shows a conventional P-N junction formed in-diffusion of P-type dopants from a surface.

Diffusion of dopants occurring at low dopant and point defect concentrations (<1 atomic percent) can assume dilute approximations. In this regime, Fick's laws of diffusion are valid and can be useful for describing dopant motion. Fick's first law relates the flux, J, of particles passing through a unit area per unit time to the concentration gradient, dC/dx, in proportion to the diffusion coefficient, D.

$$J = -D\, dC/dx \quad \text{(in 1 dimension, } x\text{)} \tag{1.1}$$

Combining the continuity equation $dJ/dx = -dC/dt$ with Fick's first law gives Fick's second law.

$$dC/dt = D\, d_2C/dx_2 \tag{1.2}$$

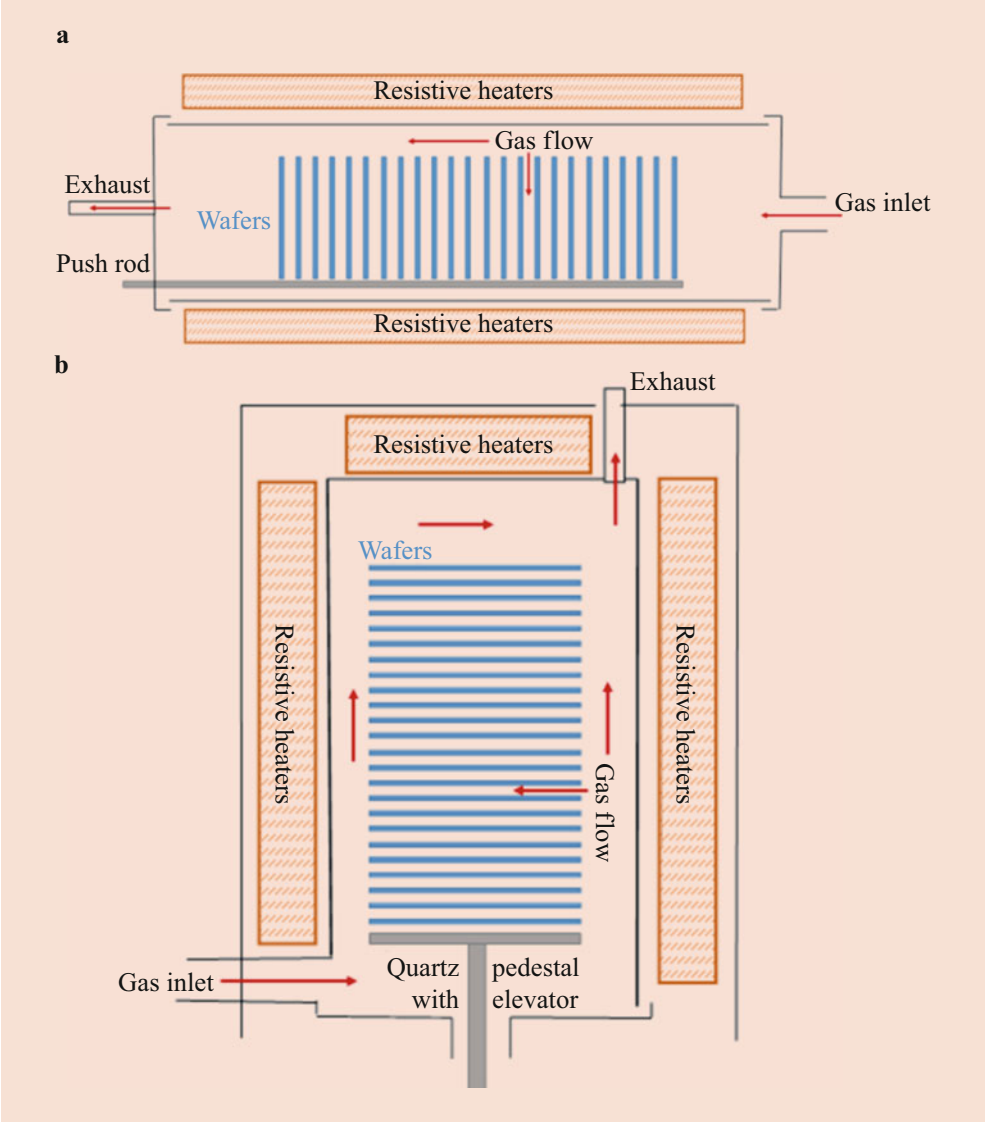


Fig. 1.18 Schematic of a horizontal (**a**) and vertical furnace (**b**) showing key functional elements

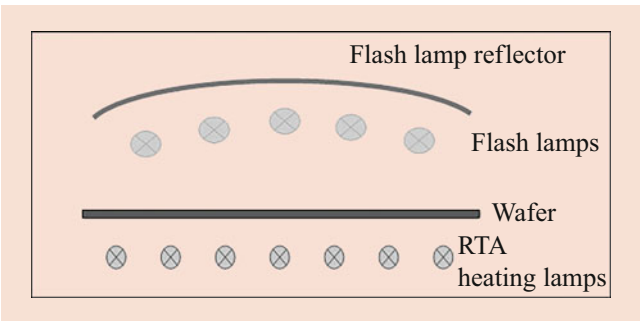


Fig. 1.19 Schematic of a flash chamber showing an array of lamps and reflector positioned about a wafer

The diffusion coefficient follows an Arrhenius dependence with an exponential prefactor, D_0, and an activation energy, E_a, for the thermally activated process.

$$D = D_0 \exp\ (-E_a/kT) \tag{1.3}$$

The presence of nonequilibrium concentrations of point defects can further be included to proportionally enhance the diffusion over the equilibrium, C^*, levels such as for the case of vacancies:

$$\mathrm{d}C/\mathrm{d}t = D_\mathrm{v}\ C_\mathrm{v}^*\ \mathrm{grad}\left(C_\mathrm{v}/C_\mathrm{v}^*\right) \tag{1.4}$$

As a simple analytic approximation for the case of junction formation by indiffusion, the junction depth, X_j, is estimated by the square root of the diffusivity, D, at a given temperature multiplied by the duration of the anneal, t.

$$X_\mathrm{j} = \mathrm{Sqrt}\,(Dt) \tag{1.5}$$

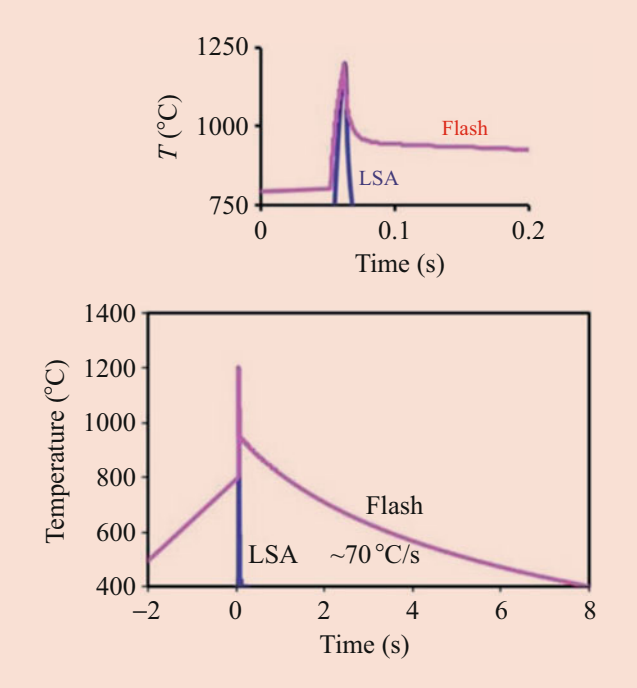


Fig. 1.20 Comparison of typical flash and laser anneal (LSA) time-temperature profiles showing the much faster transients involved in a laser anneal process

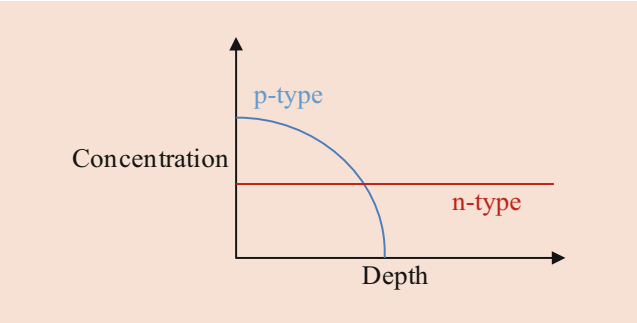


Fig. 1.21 An electrical junction is formed at the position where the active p-type doping concentration equals the active n-type doping concentration

Several dopants and impurities have been experimentally quantified for semiconductor materials such as silicon.

Grain Boundary and Interfacial Diffusion

The existence of grain boundaries in polycrystalline materials can provide a pathway for faster diffusion than their single crystalline counterparts as shown in Fig. 1.22. The density of grain boundaries, segregation, and the cohesiveness of the grain boundaries ultimately determine how much faster polycrystalline diffusion is. For metals, the diffusivity in grain boundaries can be orders of magnitude higher than bulk lattice diffusivities. Fisher proposed a model for GB diffusion that assigns an effective width to the highly diffusive grain

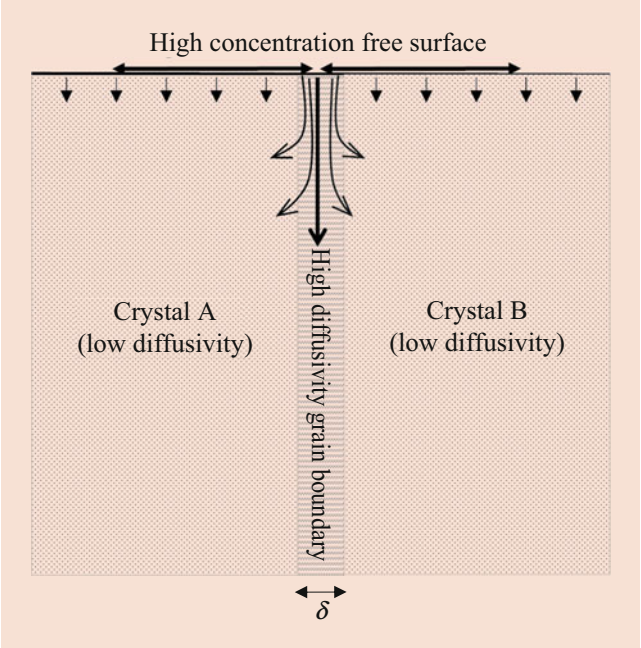


Fig. 1.22 Schematic showing enhanced diffusivity which may occur along a grain boundary

boundaries and extracted a value on the order of two atomic layers (about 5 angstroms). This type of diffusion can be important for semiconductor devices as electromigration is directly influenced by the diffusivity of atoms in interconnect lines.

1.4.3 Dopant Activation/Clustering/Deactivation

Dopant impurities in semiconductors such as boron, phosphorus, arsenic, and antimony in silicon can provide excess electrical carriers (electrons or holes), shifting the Fermi level of the material to be more n-type or p-type. To do so, these dopants typically reside on substitutional sites within the crystal lattice. However, when present in high concentrations, the dopants can begin to exceed soluble limits and form clusters or precipitate [6, 7, 26]. The critical concentration for equilibrium electrical solubility is a temperature-dependent property. Annealing at high temperatures increases the critical concentration allowing dopants to be captured in their metastable soluble state by quenching via a rapid cooling step. The quenching rate need to be fast enough, usually exceeding their diffusivity rate, so that dopants are kinetically limited from coming out of solution. However, further annealing at moderate temperatures can allow the dopants to deactivate as the system moves toward its lower temperature equilibrium state.

1.4.4 Semiconductor Recrystallization

Semiconductor materials that are in an amorphous state either from deposition or ion implantation can be recrystallized into polycrystalline or single crystal during thermal treatment. Solid-phase epitaxial recrystallization (SPER) is the heterogeneous recrystallization of an amorphous region in contact with an underlying single crystal material of similar type. The rate at which the amorphous region regrows and the crystalline quality of the regrown region has been shown to depend strongly on the surface orientation normal to the regrowth front, temperature, and doping/impurities within the amorphous layer [18–20].

1.4.5 Simulators

Computer software is now commonly used to simulate dopant diffusion through the solution of partial differential equations using finite element methods [22, 23]. These programs can be more generalized than the above analytical solutions allowing for a multitude of geometry effects and producing spatially varying diffusion contours. The diffusion models developed within them can include extensively more physics such as the interaction of dopants with point defects under intrinsic and extrinsic conditions along with varying temperature profiles and have become commonplace within the semiconductor industry [25, 28].

1.4.6 Oxidation

Annealing in a gas ambient can lead to the growth of new materials on the surface. For example, silicon exposed to an oxygen-rich ambient will form a silicon dioxide layer on the surface through the following chemical reaction:

$$\text{Si (solid)} + \text{O}_2 \text{ (gas)} \rightarrow \text{SiO}_2 \text{ (solid)} \qquad (1.6)$$

As the reaction proceeds, the rate of oxidation will slow down due to the diffusion of oxygen reactant through the formed SiO_2 layer to the silicon surface where the reaction can continue to form new oxide. Due to the difference in density of SiO_2 and the silicon that it replaces, there is a volumetric expansion of about 2.2× resulting in an intrinsic stress. The rate of oxidation was initially modeled by equating the flux of reactants for three primary mechanisms, resulting in a linear parabolic dependence of oxide thickness per time [4, 12]. Later models were added to improve the growth kinetics for low thicknesses typically under 200 angstroms [13]. Additional modifications can be made to account for changes in growth rate with dopant concentration and surface orientation [3].

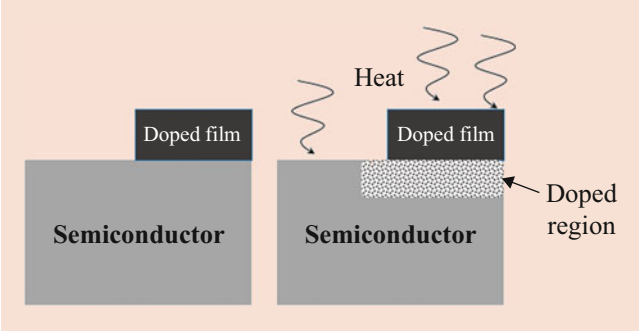


Fig. 1.23 An example of solid source doping. A doped film is deposited on a region of semiconductor, and the assembly is then subjected to thermal anneal. This anneal drives dopant species from the film to the semiconductor

1.4.7 Solid Source Diffusion

In addition to implanting dopant species or growing a doped epitaxial layer, another means that has historically been utilized to dope a semiconductor crystal is through the use of a solid source diffusion as in Fig. 1.23. In this technique, a material with a high concentration of doping atoms is deposited upon regions of the semiconductor which are desired to be doped. The wafer is then thermally annealed to diffuse dopant species from the deposited material into the semiconductor. Common material utilized for the doping source include borosilicate glass (BSG), phosphosilicate glass (PSG), and doped oxides. It was disclosed that this technique was utilized by Intel to dope under the fins as a punch through stopper doped layer.

1.5 Deposition

Materials deposition is an important step in the semiconductor device fabrication process. New layers can be deposited to epitaxially align with the exposed crystalline surface. Due to the dependence on exposed crystalline surfaces, epitaxial deposition can be a selective process that only grows in desired regions through balanced control of the absorption and desorption rates of the depositing atoms. Alternatively, non-epitaxial deposition of polycrystalline and amorphous layers can result in the conformal deposition across the entire exposed surface as shown in Fig. 1.24.

1.5.1 Deposition Methods

Physical vapor deposition (PVD) or sputter deposition is a physical process in which a target material is sputtered from a source onto a nearby wafer. The deposited material can be of very high purity and does not require a chemical reaction

for the deposition to take place. Typically, the target is an electrically grounded metal cathode in a vacuum chamber. Argon gas is introduced into the chamber, gets positively ionized, and is accelerated toward the cathode target. Though ion impacts with the target, metal atoms are displaced such that they deposit onto the surface of a nearby wafer.

In chemical vapor deposition (CVD) depositing atoms are delivered by gases flowing over the wafer surface in a heated chamber. When the transport gases are brought in contact with the wafer, chemical reaction occurs on the surface resulting in deposition of new material. The species contained in the gases can lead to deposition of thin semiconductor layers like silicon with controlled amounts of dopant or insulators like SiO_2.

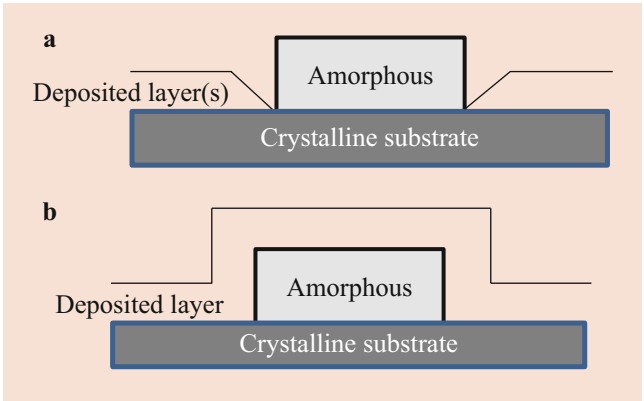


Fig. 1.24 Figure showing the resultant geometries created by a selective deposition seeded from a crystalline substrate (**a**) and a conformal deposition (**b**)

CVD is a heterogeneous reaction with three main steps: (1) chemical arrival, (2) surface reaction, (3) removal of by-products. More specifically, these steps can be broken down into their individual influences as shown in the heterogeneous model in Fig. 1.25.

The rate of deposition is controlled by the rate of arrival of reactants, the surface reaction rate, and the rate of removal of by-products. For typical CVD processes, it is desired to have the rate of arrival of the reactants be the rate-limiting step for epitaxial growth, resulting in the best crystal quality and process control. Plotting the deposition rate exponentially over temperature for a particular chemistry and reactor geometry will often make two distinct regimes observable as shown in Fig. 1.26. The kinetic regime occurs at lower temperatures when the surface reaction is the rate-limiting process. The mass transport controlled regime occurs at higher temperatures and is limited by the diffusion or rate of arrival of reactants.

The morphology of the deposited layer is controlled by the rate of arrival relative to the surface diffusion rate, with a faster arrival rate leading to more polycrystalline morphologies.

The quality of the epitaxial layer resulting from CVD deposition is highly dependent upon the cleanliness and crystal quality of the surface prior to epitaxial growth, the lattice mismatch between the crystal surface and the depositing film, the arrival rate relative to the surface diffusion rate, and the

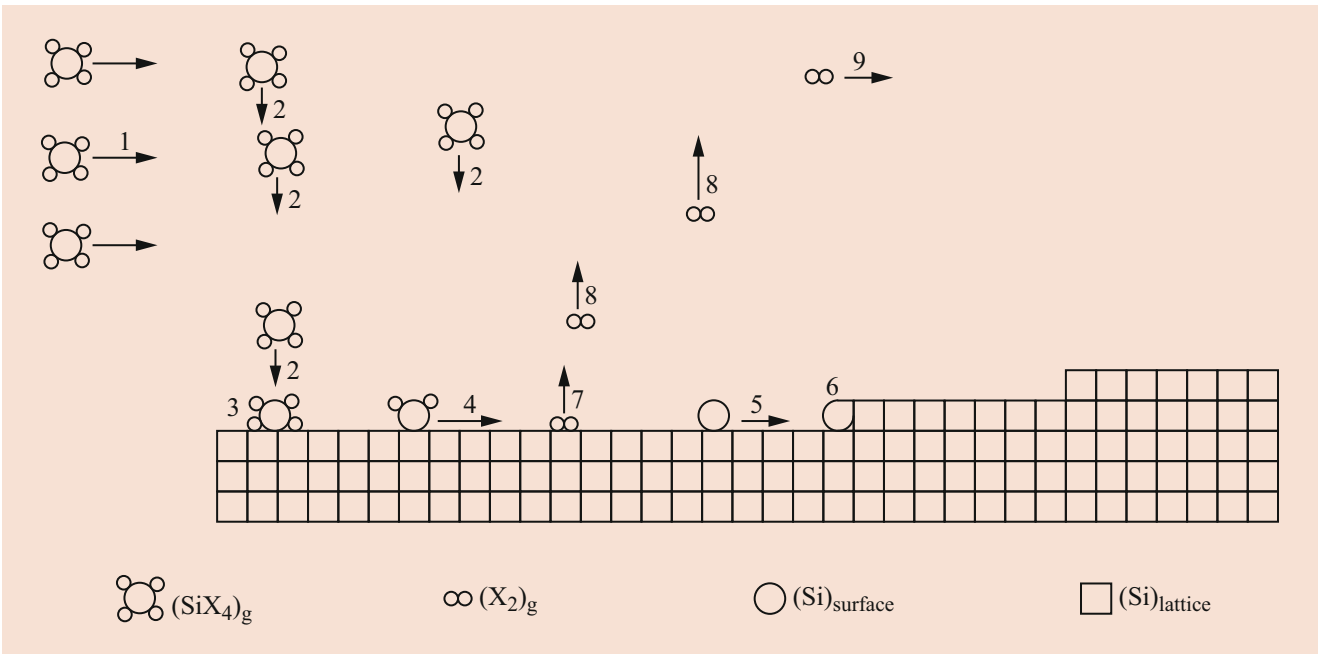


Fig. 1.25 Heterogeneous reaction model illustrating arrival (1, bulk transport of reactants; 2, diffusion of reactants to surface; 3, reactant absorption), surface reaction (4, chemical reaction; 5, surface diffusion; 6, incorporation into crystal), and by-product removal (7, by-product desorption; 8, by-product gas transport; 9, by-product bulk transport evacuation)

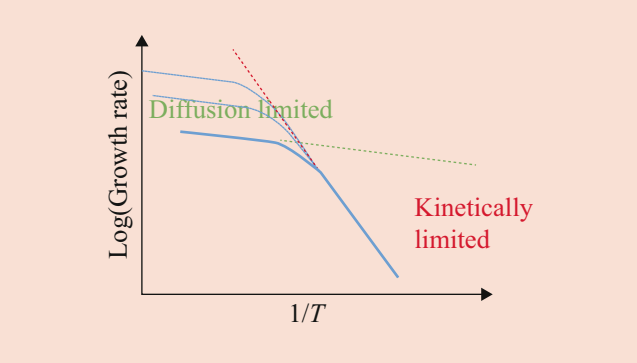


Fig. 1.26 Growth rate vs. reciprocal of temperature for a typical deposition process

nature of the lattice incorporation. Due to the differences in surface diffusivity and lattice incorporation for different surface crystal orientations, the growth rate and quality for different orientation can vary. Typically (111) surfaces will have slower deposition rates than (110) and (100) resulting in faceting for nonplanar surfaces and possible stacking fault formations.

Atomic Layer Deposition

A thin film deposition method that allows for conformal layers that are angstrom to nanometers in thickness is atomic layer deposition (ALD). This process is similar to CVD but relies on an alternating set of self-limiting chemical reactions on the surface of the wafer. For each step, the wafer is exposed to gas precursors until the surface reaction for a single atomic layer is carried out to completion. A second set of self-limiting precursors are then exposed to the new surface in order to build a new atomic layer on the first. The set of alternating chemical reaction exposures is called a cycle. Through the repeated sequence of these cycles, a thin film can be atomically deposited layer by layer. This method has proven to be very useful for the formation of high dielectric constant (Hi-K) gate insulators.

Molecular Beam Epitaxy.

Molecular Beam Epitaxy (MBE) is an atomic deposition process performed under ultrahigh vacuum (UHV) in a chamber like the one shown in Fig. 1.27. MBE can result in exceptionally high-quality epitaxial layers [2]. Ultrahigh purity sources of the depositing elements are heated in Knudsen effusion cells or electron beam evaporators directly across from a target deposition wafer. The targets are heated until they begin to sublime, releasing a low concentration of atoms for deposition. The released atoms will condense on the neighboring wafer surface. The temperature of the source will control the rate of material impinging on the substrate surface. The temperature of the substrate affects the rate of hopping or desorption occurring during the epitaxy process. Reflection high-energy electron diffraction (RHEED) is used

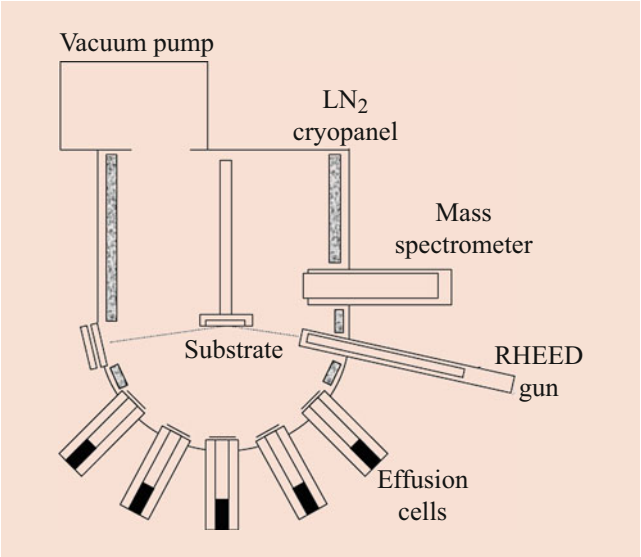


Fig. 1.27 Schematic of an MBE reactor

for in situ monitoring of the crystal quality and thickness of growth. Although MBE can deliver high-quality epitaxy, the throughput is too slow for high-volume manufacturing except in specialized cases. The sub-nanometer control and epitaxial quality afforded by MBE allow for band gap engineering and generation of delta-doped layers suitable for precise device dimensions.

1.6 Etch

Materials can be removed during the fabrication of semiconductor devices through the chemical process of etching. In this step, the materials are introduced to chemicals such as halides (F, Cl, Br, Xe) or acids to form a reaction at the exposed surfaces resulting in the controllable loss of material. Portions of the device can be covered with etch resistant materials to protect from the etchant, resulting in different device geometries. The primary methods of etching can be categorized into two approaches: (1) wet etching based on liquids and (2) dry etching based on gas or vapor phase chemistries.

1.6.1 Wet Etch

The mechanisms for wet chemical etching involve three essential steps: the reactants are transported by diffusion to the reacting surface, chemical reactions occur at the surface, and the by-products from the surface are removed by diffusion and evacuation. The etch rate, which is the amount of film removed by etching per unit time, is influenced by the concentration of the etchant in the solution, the agitation of

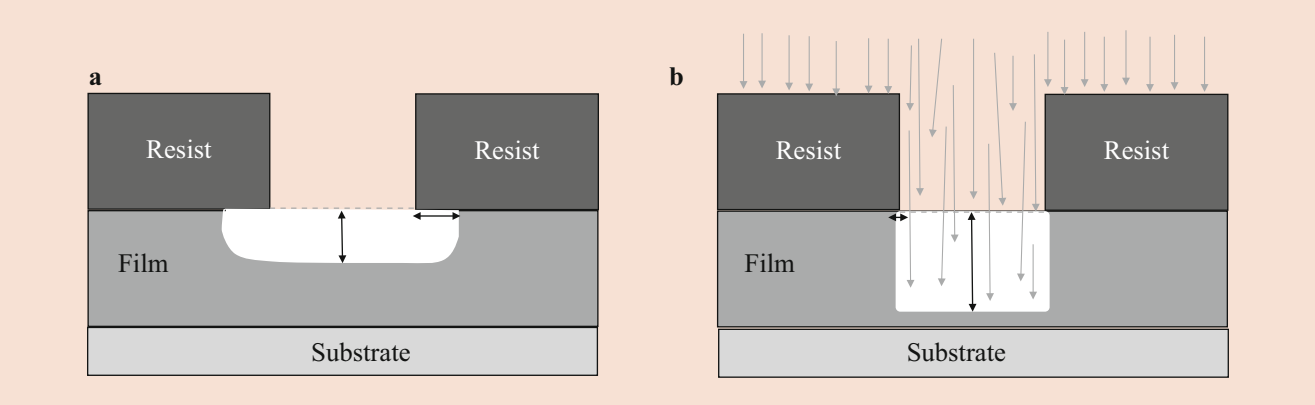


Fig. 1.28 Resultant etch profiles from an isotropic wet etch (**a**) and an anisotropic dry etch (**b**). The wet etch may undercut a masked feature and the dry etch acts in a vertical or line-of-sight fashion

the liquid, and the temperature of the etchant solution. Wet etching often results in isotropic removal (i.e., having the same lateral and vertical etch rates) of the etchable materials producing undercutting of masking material as shown in Fig. 1.28a. This can lead to a loss of resolution in the etched pattern. However, due to the reliance on chemical reaction, high selectivity between the etch rates of different materials can be achieved.

1.6.2 Dry Etch

Dry etch methods include plasma etching, reactive-ion etching (RIE), sputter etching, magnetically enhanced RIE (MERIE), reactive-ion-beam etching, and high-density plasma (HDP) etching. These dry etch methods have been developed to achieve high-fidelity transfer of mask patterns by producing highly anisotropic etch rates in which the lateral etch rate is almost zero relative to the vertical etch rate (Fig. 1.28b). This is done by applying a directional bias to the etchants often through the generation of plasma in a gas at low pressure. Positive ions bombard the surface at high speed giving more directionality to the etch process. Due to the physical nature (sputtering and bombardment) associated with dry etching, it can yield anisotropic profiles, but it is also associated with lower etch selectivity and severe bombardment-induced damage.

1.6.3 Chemical Mechanical Polish or Chemical Mechanical Planarization

Chemical mechanical polishing/planarization (CMP) is a process which has relatively recently been applied to semiconductor manufacturing. The introduction of this process somewhat coincides with the introduction of copper interconnects and the associated difficulty in etch removal of copper.

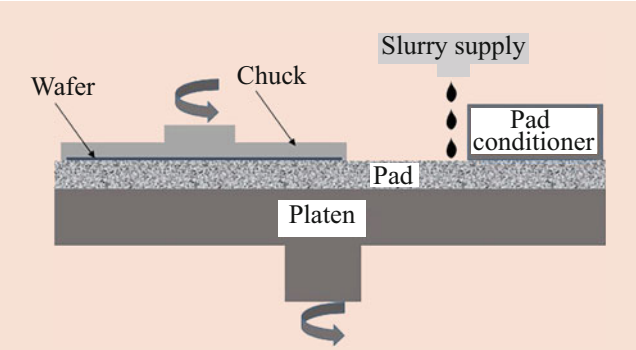


Fig. 1.29 A functional schematic of a CMP tool. A wafer is loaded onto the chuck in an inverted state. The chuck and/or platen may rotate as a slurry mixture is deposited upon the pad

Unlike other etch processes, CMP uses both chemical and abrasive methods to remove material as shown in Fig. 1.29. A slurry is utilized which can contain particulate to serve as abrasives and chemicals such as dilute HF. This slurry is deposited on a pad composed of a porous material which is mounted on a platen which may rotate. The wafer is mounted on a chuck which may then rotate in contact with the slurry and/or pad.

Since introduction, the CMP process has been incorporated into numerous front-end and especially back-end processes. The process is heavily reliant upon the slurry and pad characteristics, and these consumable items can represent a very significant cost to the manufacturing process. The CMP process is capable of angstrom-level control and can be end pointed through various techniques.

1.6.4 Etch Selectivity

In practice, it is difficult to find etch chemistries that can target a specific material and have non-zero etch rates in

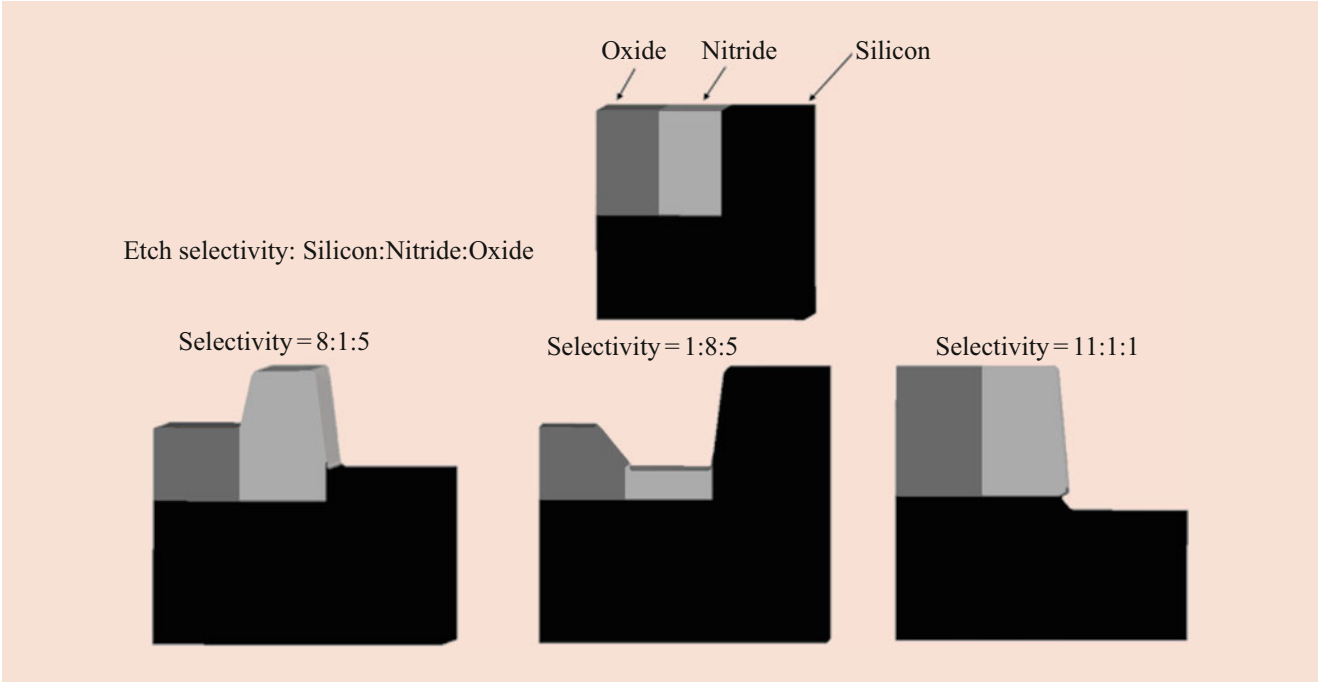


Fig. 1.30 An illustration of etch selectivity from a wet etchant. The selectivity is specified for silicon, nitride, and oxide materials and each material will etch a different amount during the same operation

all other materials. It is equally as difficult to find etch chemistries that etch all materials at the same non-zero rate. For this reason, etch processes are commonly classified by their etch selectivities to the different materials in the assembly, resulting in differences as shown in Fig. 1.30. This metric is fundamentally a measure of the ratio of etched material in one material to another.

It is also important to understand that semiconductor processes involve materials that may all informally be classified as the same material, but in actuality have far different properties. For instance, a thermal oxide will have different etch properties from a deposited oxide, and there may be a dozen of different recipes for deposited "oxides" which may all differ in etch rate and/or chemical composition. Experimentation is the key to determining an accurate sense of how an etch process will behave.

1.6.5 Atomic Layer Etch

Atomic layer etching (ALE) is a relatively new technique for etch operations in semiconductor processing. This technique has exhibited extremely high selectivities for certain applications with precise angstrom-level controllability. ALE relies upon alternating self-limiting reactions performed in a cyclical manner. Etches can be specified by the number of cycles. The process is becoming heavily utilized in R&D areas of semiconductor process development, and it is foreseeable that it will see some commercial adoption in the future.

1.6.6 The Coloring Problem

Semiconductor features are becoming so small that, in many cases, very high etch selectivities are required. Ideally, it would be possible to target etches that would remove a layer with infinite selectivity to all other materials present; however, this is not the case. Technology developers, instead, rely upon materials which have highly selective etches to all other common materials. Unfortunately, the list of these materials is quite short which limits the ability of technology designers to implement new features or requires them to utilize additional expensive patterning operations to protect some region of the semiconductor die from etchants. This problem is commonly referred to as a coloring problem.

1.7 Lithography

Lithography is the process by which patterning is introduced to semiconductor assemblies. When one refers to the process node, it is a reference that historically has some correlation to the smallest feature which can be lithographically imaged. While lithographic challenges in future technology nodes associated with the light source are perhaps the most documented and discussed, challenges exist in regard to resist chemistry, resist processing, mask formation, and optics as well. Therefore, it is vital to discuss these concepts in conjunction with each other and take a holistic approach to lithography technology.

1.7.1 Fundamental Lithographic Process

The fundamental goal of lithography for semiconductor processing is to pattern a region on a semiconductor assembly in a repeatable and prescribed manner (Fig. 1.31). In its most basic form, a semiconductor lithographic process entails the exposure of a light-sensitive chemical, commonly referred to as photoresist or simply resist, which is placed atop a semiconductor assembly. This exposure is performed through a patterned photomask which enables the transmittal of light in some regions and prevents it from others. In this manner, the pattern of the photomask is transferred to the resist on the semiconductor assembly like in Figs. 1.31 and 1.32.

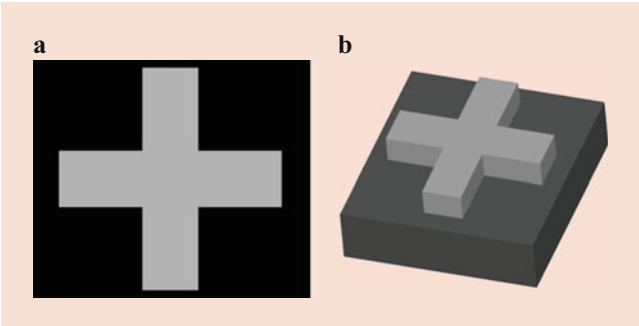


Fig. 1.31 (**a**) top down view of lithographic mask, (**b**) 3D view of patterned feature using a lithographic process with the same mask

1.7.2 Lithographic Constraints Due to Light Source

While this text is not going to go into great depth to explain the physics underlying light at the nanometer scale, a basic understanding of the role of the light source may be obtained by considering the Rayleigh criterion. Where R is the resolution provided by the light source, $k1$ is a parameter related to processing factors such as defects associated with the resist and the use of resolution enhancement techniques, λ is the wavelength of the light source, and NA is the numerical aperture of the projection lens.

$$R = \frac{k1 * \lambda}{\text{NA}} \tag{1.7}$$

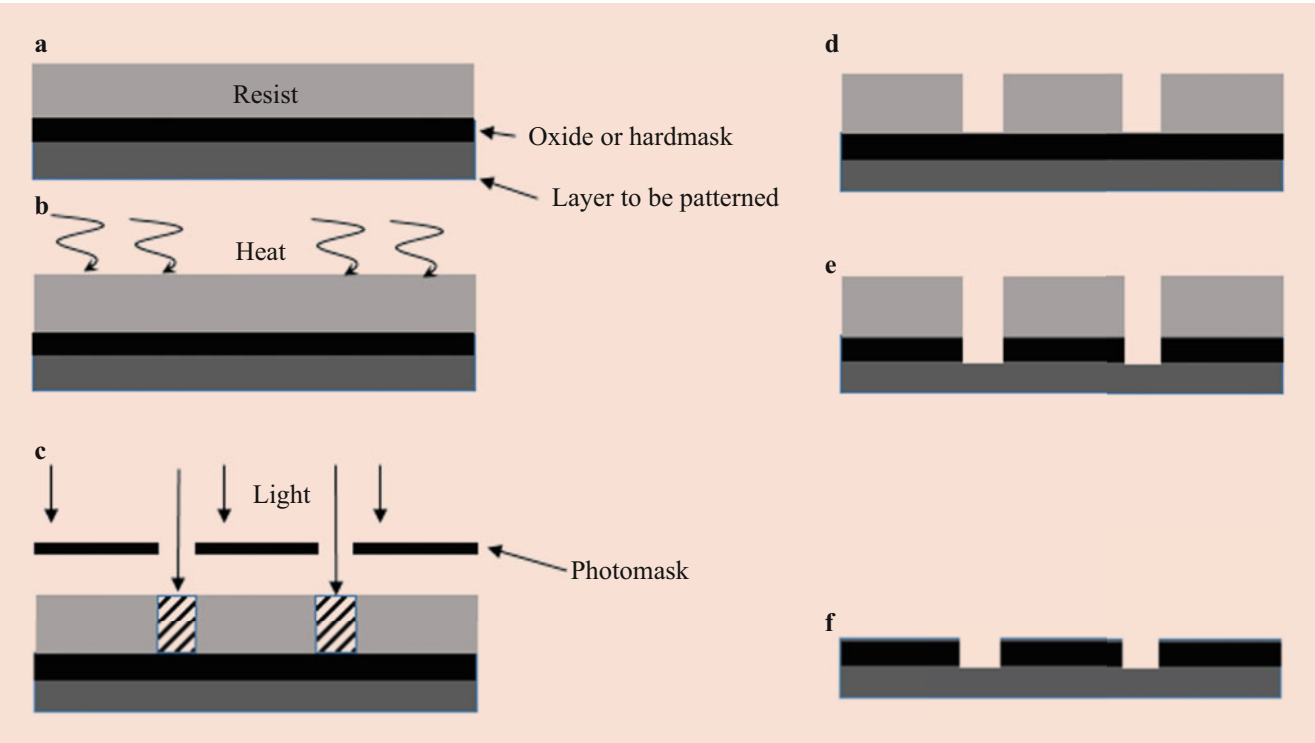


Fig. 1.32 Usage of photoresist in a lithographic process. (**a**) Photoresist is deposited on an assembly with typically a spin-on process. (**b**) The deposited resist is thermally baked to reduce defect-causing solvents from within it and to improve adhesion to the substrate. (**c**) The resist is exposed through a photomask to light; (**d**) the resist is subjected to an additional bake step and developed to remove either the exposed or unexposed resist; (**e**) the underlying structure may be processed (etch, implant, deposit, etc.); (**f**) the resist is stripped

This single equation explains both the industry focus on reducing the wavelength of the incident light and focus on providing high-quality optics for lithography operations.

1.7.3 The Role of the Stepper/Scanner and Impact to Feature Resolution

A stepper is a tool used in the lithographic processing of semiconductor wafers which provides the light to expose the photoresist on the wafer through a photomask. Stepper is an acronym for step-and-repeat camera which further indicates that it processes only part of the wafer at a given time, versus the entire wafer as was done in the early years of semiconductor manufacturing. Scanners are advanced versions of steppers that move the mask and wafer in opposing directions and can utilize smaller lenses. These are typically some of the most expensive tools in a fab.

The light source provided by the illumination system in the stepper has a characteristic wavelength determined by how the light was generated. Over the past roughly 30 years, the industry has moved from 436 nm g-line, to 365 nm i-line, to 248 nm krypton fluoride (KrF) laser, to 193 nm argon fluoride (ArF) laser as light sources have been unable to resolve increasingly small details required by advancing process nodes. By examining Rayleigh's criterion, and noticing that resolution is directly proportional to the wavelength of the light source, the reasoning behind this progression becomes apparent. Indeed, in 2018, we now find ourselves at the cusp of the next transition which is expected to be to a 13.5 nm EUV light source.

The numerical aperture of the projection lens is also an important part of Rayleigh's criterion and is representative of the ability of a lens to collect light. Namely, the resolution is inversely proportional to the numerical aperture and a lens with a higher numerical aperture will be able to resolve smaller features.

1.7.4 The Role of Resist in Lithographic Process

As previously explained, resist is a light-sensitive polymer which is used for photolithographic imaging. A resist can be classified as either negative or positive tone which reflects respectively whether the exposed or unexposed areas of the resist are polymerized and become more difficult to remove. In addition to tone, resists are characterized by the critical dimension they can image, the light wavelength and dosage required for exposure, and parameters related to how it spins on and adheres to the substrate. Resists which are suitable for one wavelength of light or one application may not be suitable for a different wavelength or application. For instance, finding low dose resists is one of main limiters to adoption of EUV.

1.7.5 Lithographic Enhancement Techniques

Phase Shift Mask

Phase shift masks (PSM) are photomasks that are designed to locally introduce a shift in the phase of the light which is transmitted through them. In a standard or binary mask, chrome or other opaque absorber materials are utilized to change only the intensity of the light which is transmitted through a transparent material of constant thickness. As features become smaller and closer in pitch, the diffractive effects of light transmitted through a binary mask increasingly prevent the resolution of small features. A phase shift mask operates differently by changing both the intensity of the transmitted light, like a binary mask, and also the phase of the transmitted light in localized regions where enhanced resolution is required.

To understand this physically, one must consider the phase angle of transmitted light. Light which is transmitted through quartz regions of differing thicknesses will emerge with different phase angles. Phase shift masks which rely upon this effect are commonly referred to as alternating phase shift masks (altPSM). Likewise, light which is transmitted through different materials or a stack of different materials may also undergo a phase shift relative to light which is transmitted through a single transparent material of the same thickness. Phase shift masks which rely upon this effect are commonly referred to as attenuated phase shift masks (attPSM) as shown in Fig. 1.33.

Optical Proximity Correction (OPC) and Inverse Lithography

OPC is a lithographic correction technique which compensates for diffraction effects and also for process-related effects which produce final patterned shapes which differ from those which appear on the mask as shown in Fig. 1.34. In-

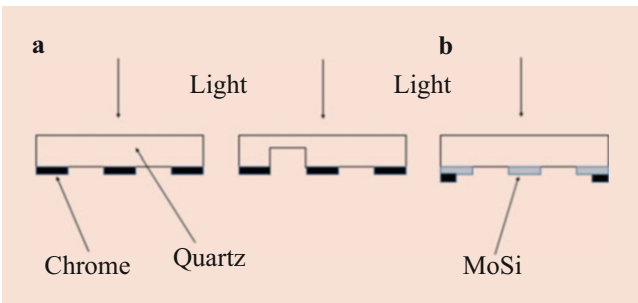


Fig. 1.33 Three types of photomasks. (**a**) A conventional or binary mask which relies upon light intensity only to pattern images. (middle) An alternating phase shift mask which changes the thickness of material through which light is transmitted to introduce a phase shift in the transmitted light. (**b**) An attenuated phase shift mask which utilizes a semitransparent material such as MoSi to induce a phase shift in the transmitted light

Fig. 1.34 A simple example of OPC correction. A rectangular shape is desired; however, an ellipsoidal shape is produced due to diffraction and processing effects. These effects can be partially compensated through the use of alternative shapes on the initial mask

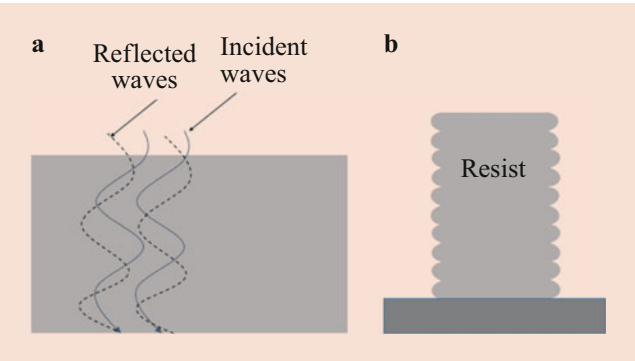


Fig. 1.35 (**a**) An example of reflected light created by exposure of photoresist without an antireflective coating (ARC) used. The ARC layer serves to absorb the light after it penetrates the resist and prevent or minimize the formation of reflected waves. (**b**) An example profile of a standing wave profile formed into the sidewall of an exposed resist feature

verse lithography (ILT) is the field associated with providing mask representations necessary to create desired features or solving the OPC problem in inverse. These fields are heavily reliant upon automated software tools such as those provided from EDA vendors. OPC correction and ILT are very time and computationally demanding and are being increasingly performed on more lithographic layers at each process node.

Antireflective Coatings

Antireflective coatings (ARCs) or bottom antireflective coatings (BARCs) are materials which are deposited in conjunction with a photoresist to minimize the reflection of light back into the unexposed resist. This serves to enhance the resolution of the lithography technique and minimizes the formation of standing wave patterns which may form from exposure to phase shifted light reflected from beneath the resist layer, demonstrated in Fig. 1.35.

1.7.6 Multiple Patterning Approaches

Single patterning 193 nm immersion lithography enables the formation of features to roughly 40 nm half-pitch. In order to enable continued scaling of device features in the absence of a viable EUV lithography solution for sub-30 nm process nodes, alternative means of forming sub-resolution features have been devised. Common techniques to accomplish this are pitch division, spacer-based approaches, and implant-based pitch division methods.

Pitch Division Methods

The most basic form of pitch division is to divide a desired pattern to be imaged, which contains sub-resolution features, into individual masks such that there are no features on any individual mask which are closer than the resolution limit of the lithography tool as shown in Fig. 1.36. This approach was the first one taken to image sub-resolution features for CMOS processing. Two similar approaches have been developed based upon this idea: litho-etch-litho-etch (LELE) and litho-freeze-litho-etch (LFLE) [5]. Both of these approaches add additional operations to achieve sub-resolution features. In particular, the lithography patterning is repeated in both processes and presents a challenge in terms of alignment or registration of these operations. These alignment challenges and increased count of processing operations are significant limiters to adoption of these techniques.

Litho-Etch-Litho-Etch (LELE) Pitch Division

LELE processes entail two litho operations and two etch operations to image a single layer. A common LELE process will begin with the deposition of two hardmask layers which are individually patterned to assemble the composite pattern. A process flow for this technique is shown in Fig. 1.37.

Litho-Freeze-Litho-Etch (LFLE) Pitch Division

LFLE is very similar to the LELE process in that it utilizes two lithographic operations, but it eliminates one etch process and requires only a single hardmask layer to be deposited. This operational count reduction is the chief advantage of this technique versus a LELE process. A LFLE process does require a specialized thermal or chemical freeze treatment to prevent shrinkage of the first patterned layer during the processing. A process diagram of this technique is shown in Fig. 1.38.

Triple Patterning and beyond

A logical extension to the LELE and LFLE approaches is to add additional lithography/freeze/etch operations. Triple patterning is a broad classification which encompasses

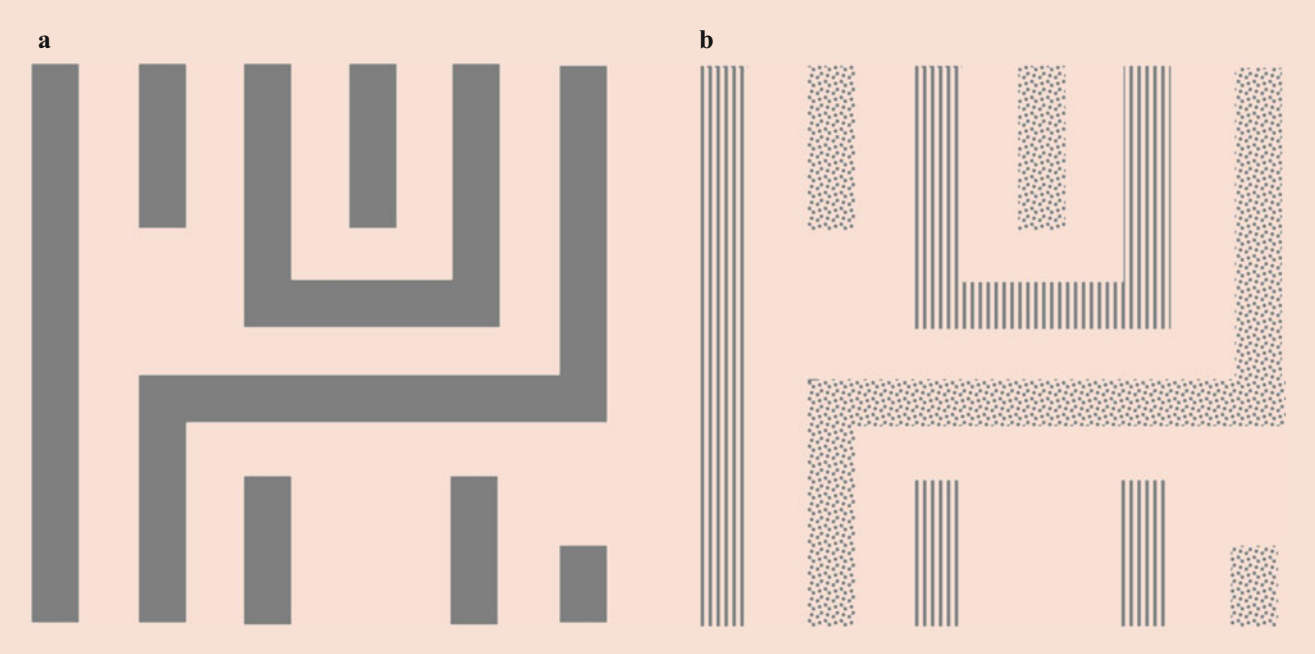


Fig. 1.36 Example of mask decomposition for a double patterning approach. The features of the pattern (**a**) are located closer than can be resolved with the lithography tool and the mask is decomposed into two separate masks (**b**)

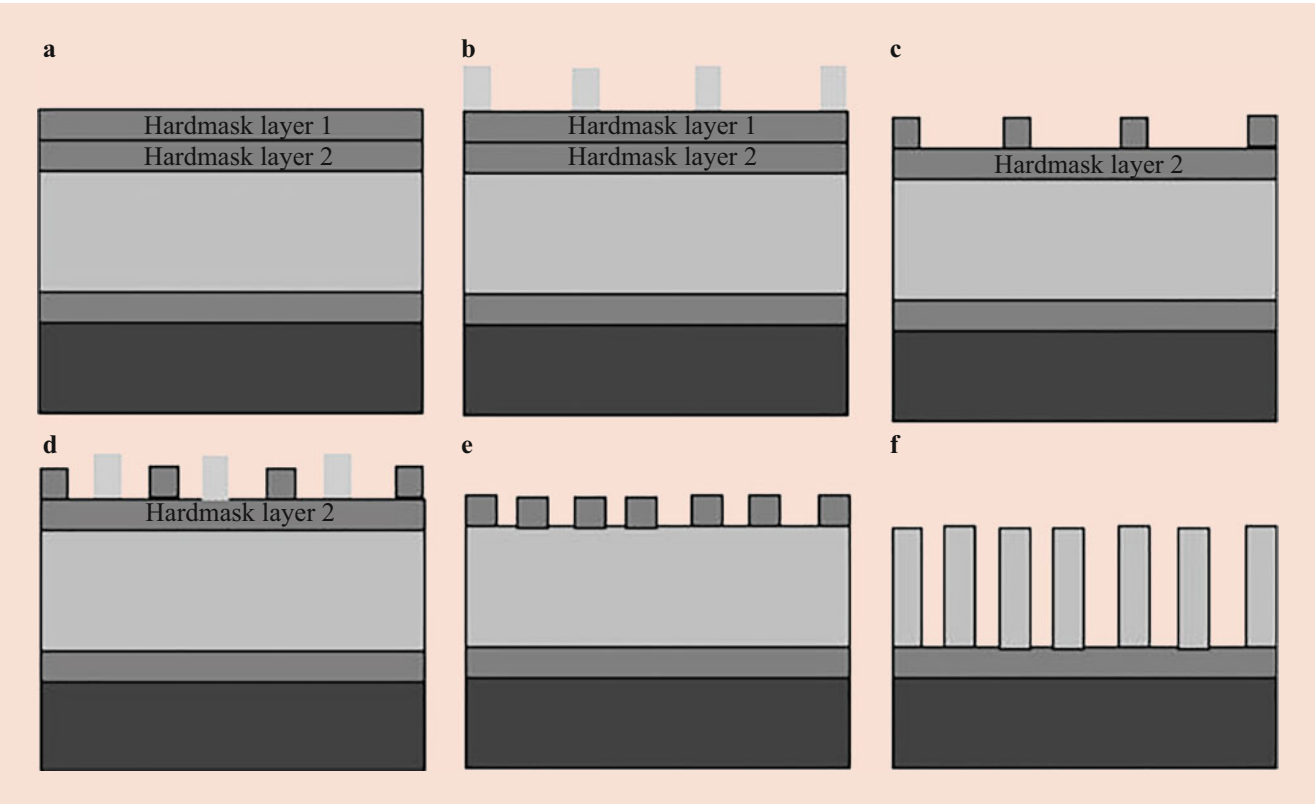


Fig. 1.37 Operational flow for a LELE patterning process. (**a**) Two hardmask layers are deposited atop the layer to be patterned. (**b**) A first pattern is lithographically printed. (**c**) The first lithographic pattern is used to pattern the first hardmask layer. (**d**) A second pattern is lithographically printed. (**e**) The second hardmask layer is patterned with the composite pattern from the first and second lithographic operations. (**f**) The layer is patterned

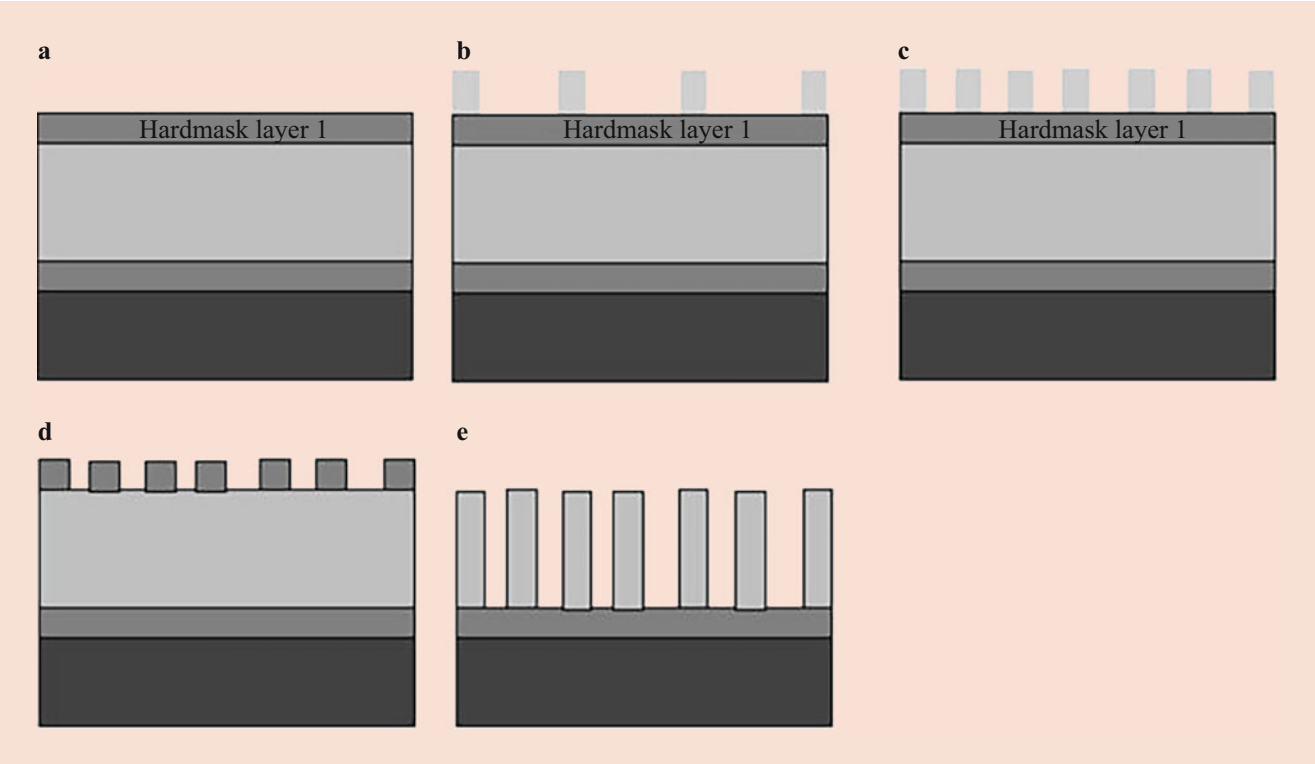


Fig. 1.38 An example LFLE process flow. (**a**) A hardmask layer is deposited atop a layer to be patterned; (**b**) a first lithographic set of patterns are printed; (**c**) the first resist features are frozen, a second resist is deposited, and a second set of lithographic patterns are printed; (**d**) the hardmask layer is etched with the lithographic patterns of both the first and second lithographic patterns; (**e**) the layer is etched

techniques utilizing three lithographic operations for imaging of a single layer. Techniques such as litho-etch-litho-etch-litho-etch (LELELE) have been proposed as EUV alternatives for sub-10 nm process nodes. As these processes are scaled to additional lithographic operations, the alignment problems become increasingly more severe, the process count increases, throughput decreases, and the challenges placed upon EDA software tools for mask decomposition become increasingly complex.

Spacer-Based Pitch Division

Deposition and etch processes have process control which is tighter than the resolution limit of 193 nm lithography. In a spacer-based pitch division process, an initial feature is imaged with a mask called a mandrel. Deposition and etch processes are then utilized to create spacers about this original feature which may then be utilized as masking layers to a subsequent etch process. This technique and variations are variously referred to as self-aligned double patterning (SADP), sidewall image transfer (SIT), pitch halving, or spacer patterning. Spacer-defined pitch division methods have a key advantage versus other pitch division approaches in that the divided pitch features are self-aligned to the mandrel features and are not prone to lithographic misregistration. A process flow for this technique is shown in Fig. 1.39.

The SADP process has been successfully utilized to form features at sub-20 nm half-pitch. The process of Fig. 1.39 is typically used with a trim mask to define the spacer features to be printed. Significantly, however, this SADP process entails far more operations than does a single exposure lithographic process which results in reduced throughput and increased processing cost. The burden of this process has been shifted from a lithography constraint to etch and deposition constraints, and etches of high selectivity are required. In addition to these processing constraints, it also becomes very difficult to form features which are bidirectional with SADP and layouts may require unidirectional features. Finally, SADP requires spacer features to be minimal size, whereas that constraint does not exist for other pitch division approaches.

Self-aligned quad patterning (SAQP) approaches have been derived from the SADP process. In these processes, a second spacer region is formed on a backbone of first spacer features. SAQP processes have been proposed as a means to achieve features at the 7 nm half-pitch process node. In practice, the line spacings of these spacer-defined patterning approaches are reliant upon the process control and variability of the spacer deposition and etch, and a degree of variability is introduced with each cycle of operations.

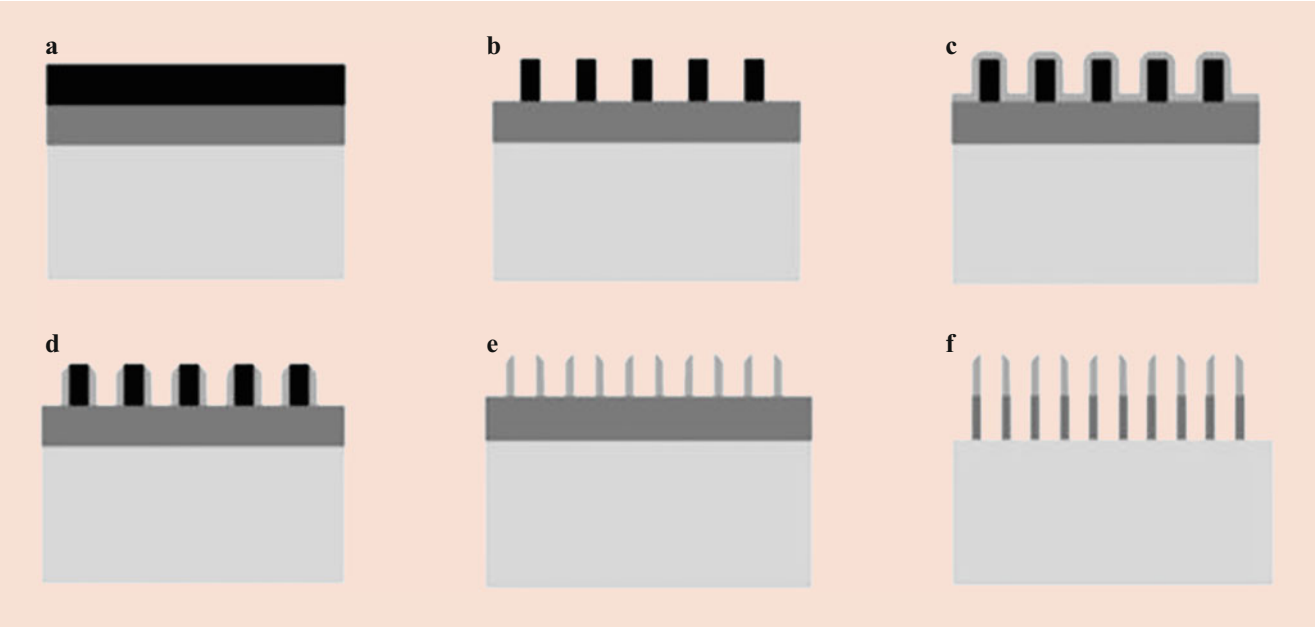


Fig. 1.39 An example of a SADP process. (**a**) Resist and lithography layers are deposited upon an assembly; (**b**) a mandrel mask is used to form a first patterned layer; (**c**) a conformal or isotropic deposition is utilized to deposit a layer about the surface containing the mandrel feature; (**d**) a dry etch is used to form spacer features on the sidewall of the mandrel feature; (**e**) the mandrel feature is removed with an etch which is highly selective to the spacer material; (**f**) a second dry etch is performed which utilizes the spacer features as a masking layer. By completing this process, the pitch between adjacent features can be effectively halved

Implant-Based Pitch Division

Another technique for pitch division uses a self-aligned tilted ion implant (TII) process to pattern and modulate the etch properties of an etch-block layer. This etch rate modulation may be driven by either a damage-based mechanism or an impurity-enhanced etch rate mechanism. Specifically, an argon implant has been demonstrated to modulate the etch properties of a silicon dioxide layer and is self-aligned through an ion beam shadowing process off of a mandrel feature which is controlled by the tilt of the ion beam relative to the wafer surface. An exemplar process flow of this technique is shown in Fig. 1.40.

The principal advantages of an implant-based pitch division process versus other multi-patterning approaches are the reduction in operational count and associated improved throughput. In practice, this technique has several challenges and has not seen widespread adoption. The most significant challenge associated with this technique is related to the implant profile which is neither laterally abrupt (due to lateral ion scatter) nor vertical (due to the ion beam tilt). The tilted ion implant also scatters at the corners of the masking layer to implant the entirety of the area between the patterns to some extent and will erode the corner of the masking layer at higher doses through a sputter process. Another concern with this technique is the etch selectivity of the masking layer is not binary to impurity concentration and typically not sufficiently high relative to the unimplanted region. This results in implant-defined mask features which are non-vertical and often possessing nonlinear sidewalls. These effects are shown in Fig. 1.41.

1.7.7 Post-optical Lithographic Techniques

A variety of techniques have been proposed as replacement for optical lithography utilizing 193 nm light sources. These include EUV, nanoimprint lithography, and direct self-assembly approaches. Each of these techniques have their merits; however, they all also currently have challenges associated with their adoption.

Extreme Ultraviolet Lithography (EUV)

EUV lithography is considered a key enabler for future device scaling and appears to be at the cusp of limited adoption for the sub-10 nm process nodes. This technology has been under development since the 1980s (at the time referred to as X-ray lithography), but adoption has been deferred in the face of numerous tool cost, uptime, mask, and resist problems. In addition, engineers have continuously pushed out the limits of 193 nm lithography using some of the resolution enhancement techniques previously mentioned. When EUV is adopted, it is likely to only be utilized for a few select tight-pitch layers such as those for local interconnect, with the remainder of the lithographic operations being performed on legacy tools.

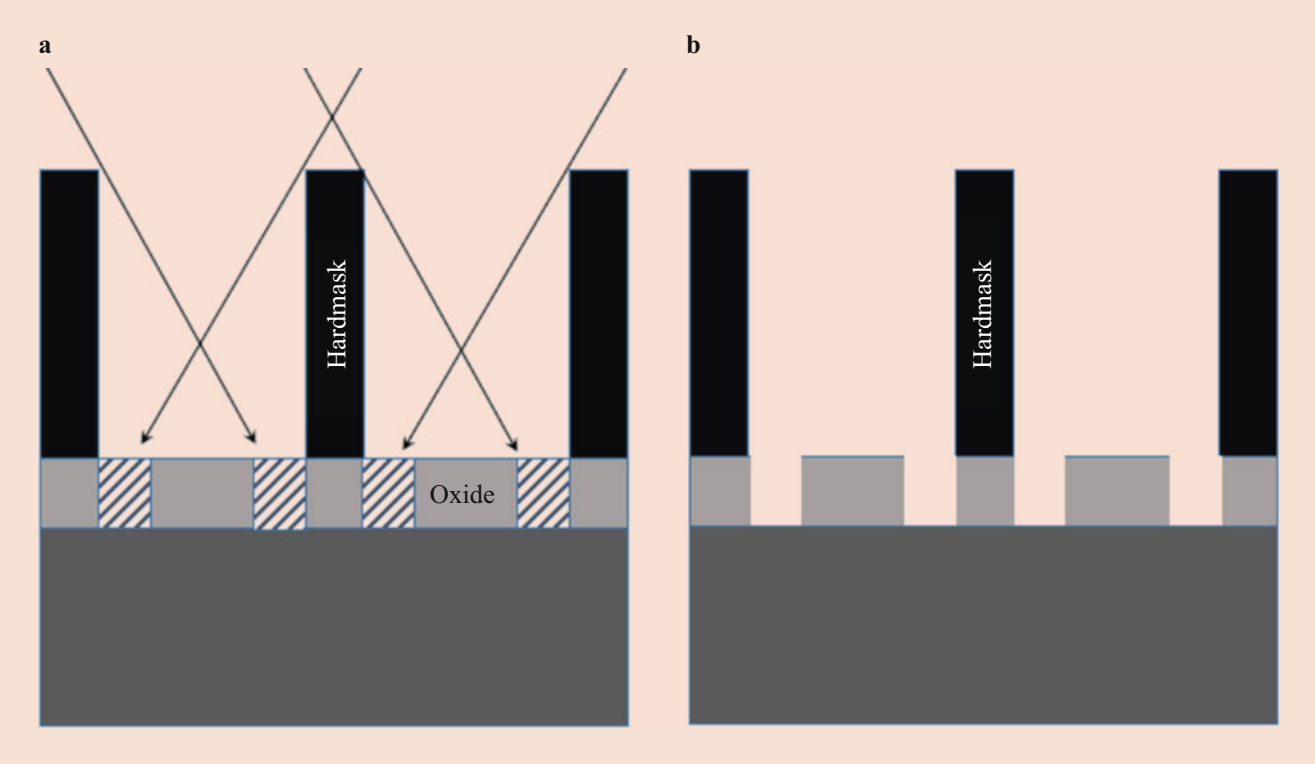


Fig. 1.40 Ion implant-based pitch division approach. (**a**) A hardmask or implant blocking layer is patterned at a loose pitch. These patterned features serve to enable shadowing of subsequent tilted implant operations. Two tilted ion implant operations are then performed at 180 degrees rotation to each other. (**b**) These implants are used to modulate the etch rate of an implanted layer which lead to preferential removal of the implanted region of that layer

Nanoimprint Lithography

Nanoimprint lithography (NIL) is a means of using a physical mold to imprint features into a resist layer or other polymer as shown in Fig. 1.42. This technique has been applied to NAND flash processing by Toshiba and has been proposed as an alternative to EUV for sub-10 nm technology nodes. NIL processes, in comparison to SADP/SAQP or pitch division approaches, utilize relatively simple equipment and are very cost efficient as they avoid the use of optical lithography tools. Variations to the NIL process pertain to whether the resist is cured with heat or with UV light and in regard to whether the contact operation displaces a resist layer or deposits a resist pattern. Tools have been developed for NIL which utilize either a wafer-scale imprint or a method which imprints a small area, moves to a new area, and repeats.

NIL technology does introduce a new set of integration issues related to the implant process. Specifically, adhesion between the template and resist is an issue. Adhesion can be minimized with the use of an anti-adhesion coating such as perfluorodecyltrichlorosilane (FDTS). In addition, the mechanical force to cause the imprint can lead to template wear; NIL is subject to gas bubble-related and density-related defects, and registration of the template to the target is an issue.

Direct Self-Assembly as Alternative Lithography

Almost every semiconductor company has investigated the directed self-assembly of a block copolymer (BCP) system as a means of nanolithography. The most common material system currently utilized is based upon the polystyrene-block-polymethylmethacrylate (PS-b-PMMA) system. DSA is not a stand-alone lithography solution; rather, it allows features patterned with an existing lithography solution to be self-aligned and/or pitch-divided.

DSA research focuses heavily on the ideas of chemoepitaxy and graphoepitaxy. In chemoepitaxy, brushes or molecules are grafted, or covalently bonded, to existing features on the target. These existing features would commonly be fabricated with a typical lithography/deposition/etch process. Graphoepitaxy then relies upon confinement created by the patterned features to self-assemble the block copolymer in a prescribed manner. This self-assembly is dictated by the phase diagram of the BCP system, the confinement, and the Flory-Huggins chi parameter. By altering the geometry, the ratio of the components in the BCP, or the chi value, it is possible to generate spheres, cylinders, gyroidal, or lamellae features in the self-assembled BCP. Selective chemical etches exist for the BCP components and

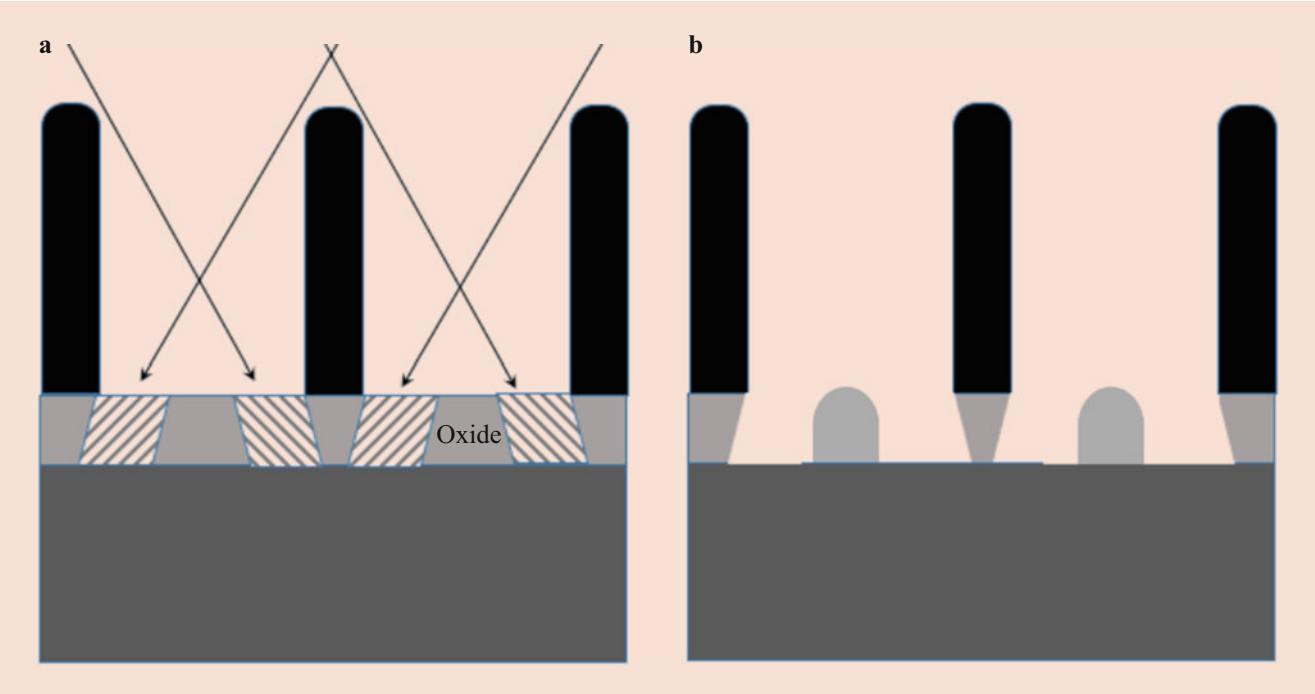


Fig. 1.41 Realistic implant and etch selectivity concerns are challenges to the integration of implant-based pitch division approaches. Ion implant as shown on the left does not result in vertical profiles. The corners of the masking features are rounded through a sputtering process and implant lateral straggle and implant scatter from the corners of the shadowing features into the nominally masked central region lead to rounded features being formed as shown on the right

various process flows have been proposed to utilize these behaviors for the formation of nanoscale features.

DSA does have numerous integration challenges. One main concern is in regard to finding a BCP system with sufficiently high chi value. Self-assembled geometries are also highly sensitive to defects or geometry fluctuations which can produce, in some cases, geometries and patterns that fluctuate dramatically both laterally and in the thickness dimension.

Electron Beam Lithography

Electron beam lithography is occasionally touted as a replacement for optical lithography. This process scans a focused electron beam onto a photoresist covered surface to pattern features. The chief advantage of e-beam lithography is that sub-10 nm resolution is possible. Indeed, e-beam lithography is used to pattern the masks used in other forms of optical lithography. However, this comes at a severe cost in throughput. A modern stepper or scanner can process hundreds of wafers per hour, while an e-beam tool would require many hours to expose a single wafer which makes these systems impractical for high-volume manufacturing (HVM) use. Attempts to productize these systems for HVM manufacturing have been undertaken in the past with very limited success.

1.8 Metalization and Contact Formation

Fabricated transistors require metal contacts and metal routing to form CMOS or VLSI circuitry. A modern CPU may contain more than 60 miles of metal wires within a package that is roughly the size of your thumbnail. This metal wiring distributes power, clock, and signal to form the VLSI circuitry through which CPUs and logic devices are formed. Metal routing in a traditional CMOS process utilizes a tiered metal system which begins with contact made to the transistor itself and terminates with contacts provided to the outside world through the package.

1.8.1 Silicide Contact to Transistor

A good contact to a transistor should provide a low barrier height to charge transport and be composed of a low resistivity metal. The contact should also be formed in a manner which does not deleteriously impact the already formed devices. These contacts may differ from NMOS to PMOS transistors as different metals may provide more optimal barrier heights; however, this comes at the cost of additional lithographic and other process operations.

Metal silicides are commonly utilized for contact to the source and drain regions of a silicon transistor. Silicide has

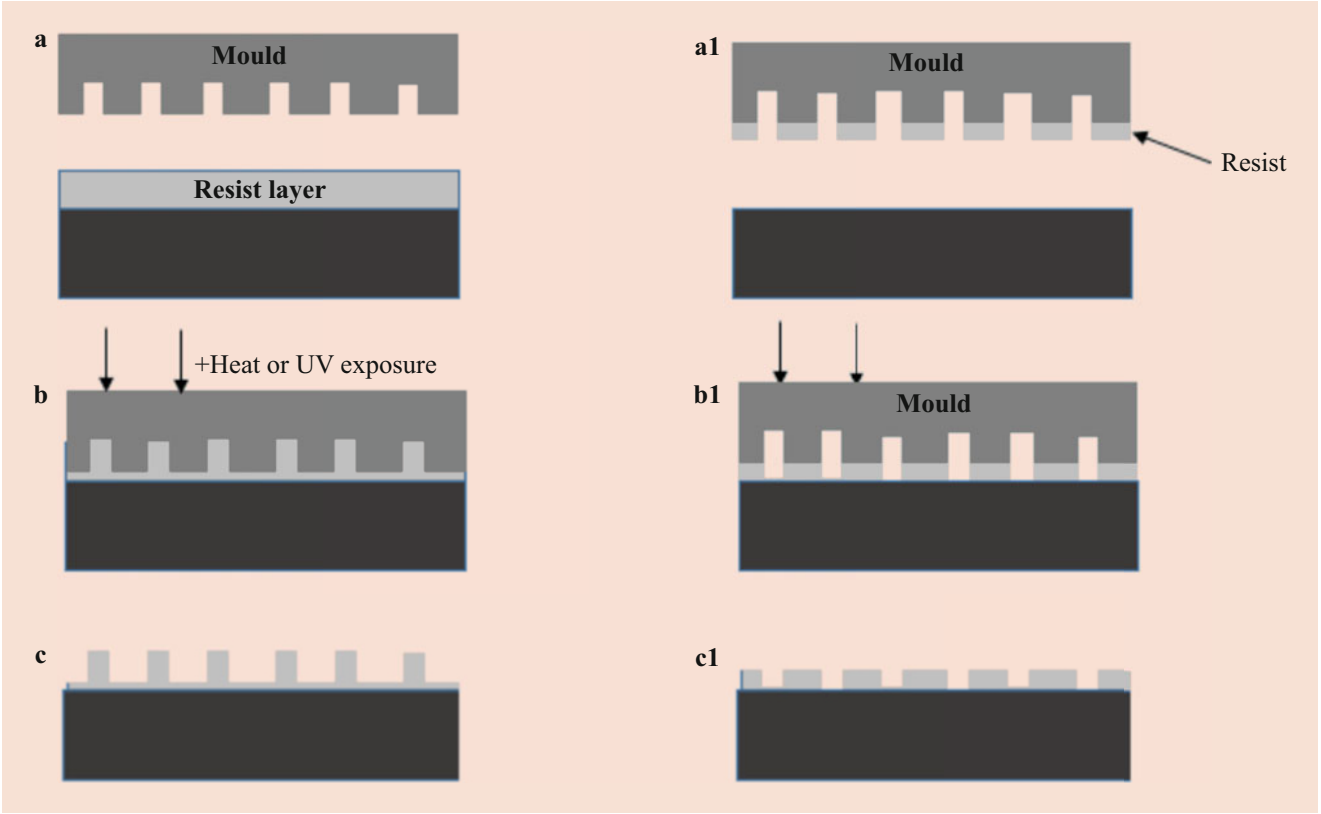


Fig. 1.42 Different NIL process flows. At the left are shown the steps in a UV or thermal NIL process. (**a**) A resist is deposited on a target wafer and planarized and a mold is prepared. (**b**) The mold is imprinted into the resist, and heat or UV light is applied to the assembly; (**c**) the mold is removed leaving the patterned resist. At the right is shown a nanocontact NIL process which is similar; (**a1**) resist is placed upon the features of a mold; (**b1**) the mold is contacted to the target; (**c1**) the mold is removed leaving the patterned features

also historically been utilized for contact to a polysilicon gate or for complete silicidation of a polysilicon gate (FUSI). A silicide is simply a compound formed by a metal and silicon atoms. Similarly, for a germanium-based transistor, a germanide could be formed. The process to form a silicide or germanide is as simple as depositing metal upon an exposed semiconductor surface and annealing the assembly, like it is shown in Fig. 1.43. The electrical barrier between the silicide and semiconductor may be further lowered by providing a high level of active doping adjacent to the silicide/semiconductor interface. This doping may be introduced by forming a contact to a highly doped and activated epitaxial layer or by implanting and activating dopant atoms about this interface. The area of the contact between the silicide and the semiconductor may also be increased to reduce the contact resistivity.

The silicide process does, however, have several technological impacts. Firstly, the contact resistance between the silicide and the semiconductor is not negligible and increasingly is becoming one of the major bottlenecks to CPU performance and power consumption. The resistance of the contact is, in part, determined by the phase of the silicide with different phases being more optimal. For instance, nickel deposited on silicon may form several different phases of silicide depending upon how it was annealed and factors concerning the metal deposition such as NiSi, Ni_2Si, and $NiSi_2$. Silicides formed with these contacts may differ in resistivity by a factor of nearly 2.5. A second concern is in regard to semiconductor voids which form in proximity to the silicided region. This concern is especially prevalent for silicide phases which are silicon rich. A third concern is the thermal processing required to form the desired silicide phase that must have a minimal impact upon the already formed device features, in particular, the gate stack and gate dielectric thickness. Finally, the silicide needs to be thermally stable to back-end metallization and packaging thermal processes.

1.8.2 Interconnect Stack

A complex CMOS process will utilize numerous layers of metal (Fig. 1.44). The first couple layers closest to the transistor are used for forming interconnect between transistors and are referred to as local interconnect. The upper layers are referred to as global interconnect and used for routing across the die. Vias are metal interconnects which connect metal from one level to another.

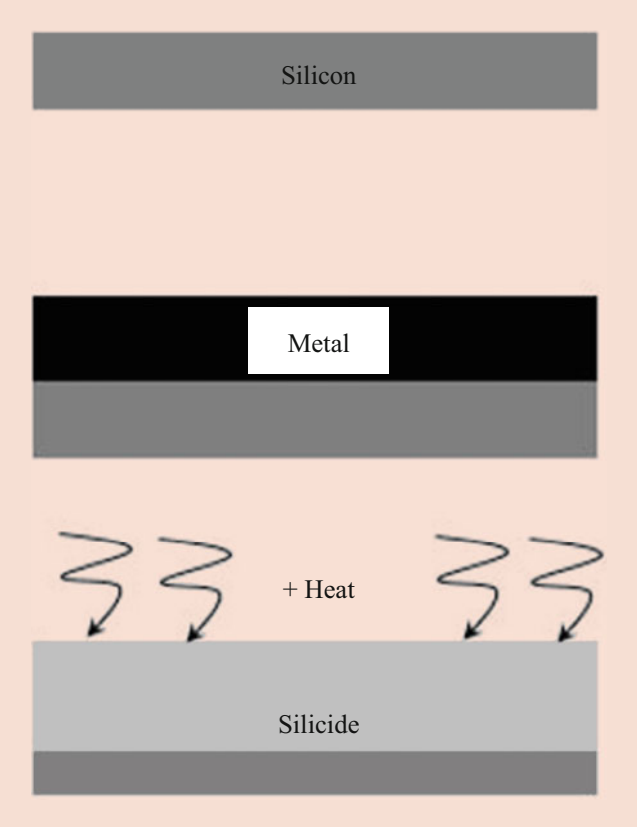


Fig. 1.43 A sample silicide process. A metal is deposited upon a silicon surface which is then thermally annealed to form the silicide

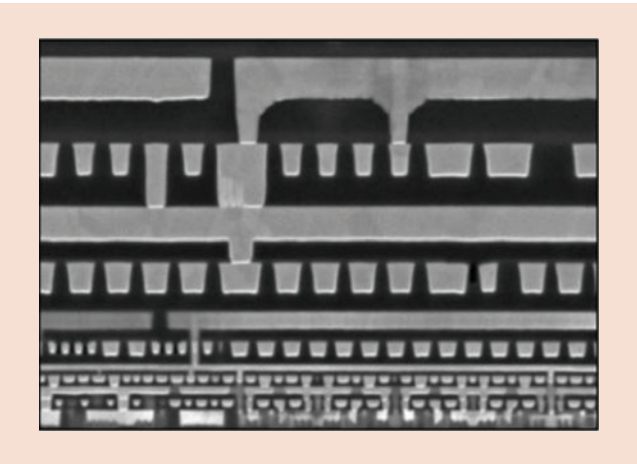


Fig. 1.44 Interconnect stack from 14 nm Intel process

Of critical concern are the local interconnects which are thinnest and spaced closest together. As devices continue to scale, the pitch and CD of these local interconnects also continue to scale. Historically, these metal layers were formed of aluminum. At the 180 nm process node, IBM transitioned from aluminum to copper interconnect as copper has lower resistivity and improved electromigration tolerance. The industry followed shortly thereafter.

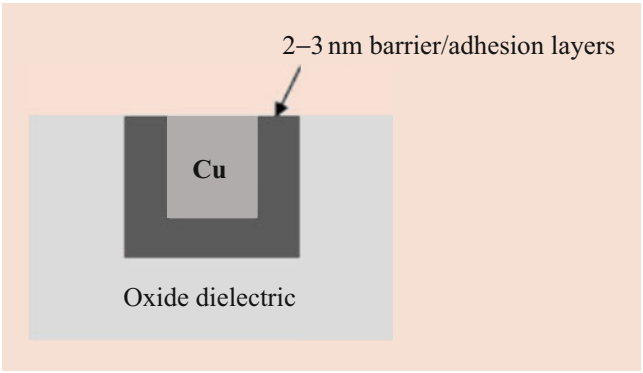


Fig. 1.45 Copper interconnect layers require barrier and adhesion layers of 2–3-nm thickness. As metal lines scale, an increasing fraction of the metal line volume is consumed by the barrier and adhesion layers

This transition to copper interconnect presented several challenges as copper has a high diffusivity in dielectric layers which necessitate the use of barrier and adhesion layers for copper metallization and dedicated toolsets to prevent contamination. In order to prevent the diffusion of copper into dielectrics, liners such as TiN at thicknesses of 2–3 nm have been implemented (Fig. 1.45). With the scaling of metal CD to sub-10 nm values, this liner requirement allows copper width of only 4–6 nm. Because of this barrier requirement, in large part, Intel has recently announced that cobalt interconnect will be utilized for some local interconnect layers in their 10 nm process.

1.8.3 Damascene Metal Processes

With the introduction of copper interconnects and continued scaling of metal line pitch, damascene metal processes have become typical as shown in Fig. 1.46. In a damascene process, the dielectric layer is patterned and etched, and then the liner and metal layers are deposited. The metal deposition is commonly done through an electroplating operation which deposits and excess of metal. The structure is then subjected to a chemical mechanical polish/planarization (CMP) operation to planarize and remove the excess metal. A dual damascene process is similar except both the metal lines, and vias are filled during the metal deposition step.

1.8.4 CMOS Process Technology Development through Nontraditional Techniques

Recent CMOS technology nodes have delivered performance and density gains not just through traditional scaling but also

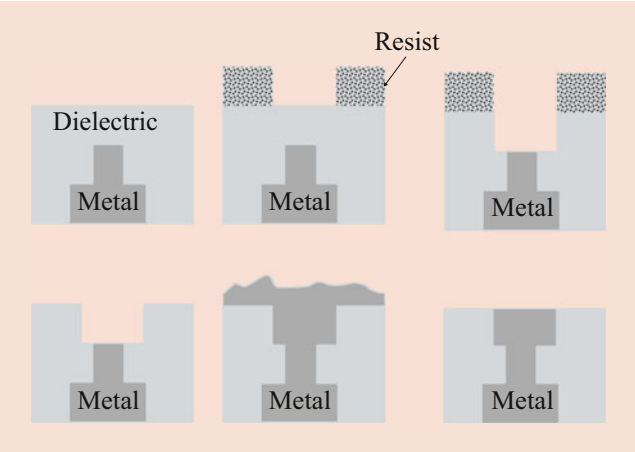


Fig. 1.46 An example of a damascene metal process. Instead of directly patterning the metal layer, the dielectric is patterned and filled, and then the resulting structure is subjected to a CMP operation. This figure does not show a liner layer; however, if a liner is required, it would be deposited prior to the metal layer

through the use of nontraditional techniques such as substrate engineering, hybrid semiconductor integration, stress engineering, different architecture, and gate stack engineering. It is expected that future process nodes will continue this trend, especially in the areas of architecture where numerous papers have been presented detailing gate-all-around architecture and vertical integration. It is important to understand the process-related implications of these techniques and understand how these ideas are being integrated into future technology nodes.

1.8.5 Substrate Engineering and Hybrid CMOS Integration

The integration of multiple semiconductor channel materials is a current major research area. By introducing different semiconductor crystals for the NMOS and PMOS regions of the die, the devices can potentially be optimized beyond what could be attained if they were both formed of the same crystal. Material properties such as carrier mobility, stress response, and band gap can be exploited to yield devices with both high electron and hole mobilities or devices which are more suitable for power/high voltage applications on die with other devices which are more suitable for low-power CMOS logic. The two major techniques for hybrid integration are epitaxially templated regrowth and wafer bonding.

Epitaxially Templated Regrowth Technique

Epitaxy has historically been a technique to introduce a dissimilar semiconductor grown from a seed of an original semiconductor. Epitaxially templated regrowth (ERG) or aspect ratio trapping (ART) is a technique which utilizes

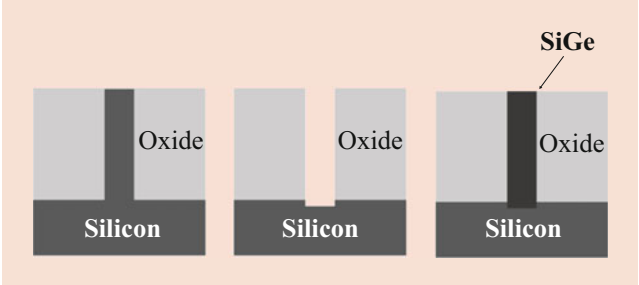


Fig. 1.47 An example of the ART/ERG technique of heterogeneous integration of multiple semiconductor systems on a single CMOS wafer. A fin, or other structure, is selectively etched to form a mold within a dielectric layer. An epitaxial layer is then formed from the seed left in the semiconductor layer with a second semiconductor that is lattice matched or nearly lattice matched to the seed material

epitaxy to form a new semiconductor region within a mold formed of a different material or insulator. This technique can be utilized to fabricate new device features at the same pitch and approximately the same aspect ratio as the material used to form the mold. As current CMOS technology is largely Si-based, these processes are of great interest as they provide a means to introduce already patterned III-V or Ge/SiGe single-crystal regions to an existing die patterned with silicon features.

An example process of an ERG/ART process is shown in Fig. 1.47 fabricated upon a silicon substrate. This process first entails the formation of silicon fin features which are surrounded by a dielectric material such as silicon dioxide. The fins are then selectively etched leaving the oxide behind to act as a mold and a silicon seed region remaining at bottom of the mold. The structure is then subjected to epitaxial process which grows a new fin within the mold comprising a different semiconductor crystal.

The ART/ERG process does have several drawbacks, however. Chief among these is the presence of crystal defects which may be nucleated at the interface between the epitaxial and substrate material. These defects are particularly problematic as they will continue in the epitaxial material until they are terminated at an interface. These defects are caused by lattice mismatch and strain energy introduced between the two semiconductor materials and become more severe as the lattice parameters become more dissimilar. For this reason, careful consideration is given to semiconductor materials for both the substrate and epitaxial layer, and the use of grading layers or seed layers prior to the deposition of the main epitaxial region is common.

Some defects from ART/ERG are unavoidable, however. By introducing taller fins formed within a deeper mold, the defects which run perpendicular to the fin length direction can normally be terminated and removed; however, the defects which run in the length direction of the fin cannot be trapped or terminated. If a device is then fabricated of a fin

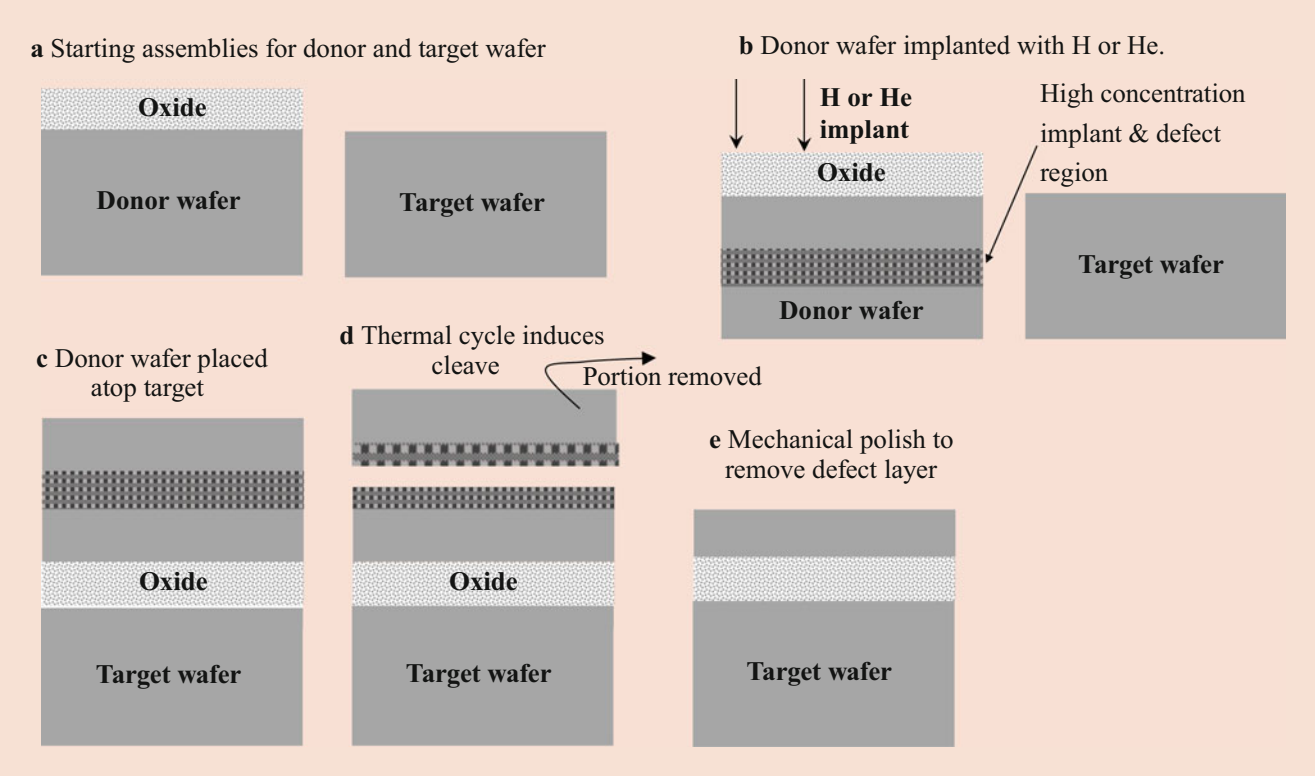


Fig. 1.48 An example of a layer transfer process using oxide bonding. There are several variants of this technique including various semiconductors, bonding layers, etch stops, and anneal sequences. This technique can result in the transfer of a relatively defect-free crystalline layer of a second semiconductor material atop a first semiconductor material

with such a defect running across a p-n junction or near the channel region of a device, an electrical leakage path will ensue which will degrade performance of the device and potentially render it unusable.

Wafer Bonding Technique

Wafer bonding is a technique used to introduce a blanket second semiconductor region atop a first semiconductor region. Unlike ART/ERG, these material systems do not have constraints on lattice parameters, and the second semiconductor layer may be introduced relatively free of crystal defects. However, this process results in the introduction of a second vertical layer or strata of semiconductor crystal. The semiconductor layers are separated by a dielectric layer which is used to bond them together and can also serve as electrical isolation between devices fabricated on the upper device strata from the lower device strata. As this technique involves the introduction of a vertical stack of semiconductors, it is of great interest to research areas involved with the vertical stacking of devices such as the complementary FET (CFET) process from IMEC.

There are several different methods of wafer bonding. In a common implementation, a donor wafer is processed with an oxide (or other bonding layer) deposition and a high-dose (5e16/cm^2–2e17/cm^2) H or He ion implant to form a region of percent level H/He atomic impurity concentration. The donor wafer is then placed oxide side down upon a second wafer and subjected to a series of anneal steps which serve to bond the oxide (or other bonding layer) to the second wafer and also to condense the H/He impurities into a narrow band of bubbles which then expand in volume and shear off a region of the donor wafer at a depth prescribed by the energy of the ion implant process. The transferred layer may then be polished to remove any defects associated with the implant process, and in some instances an epi etch-stop layer may be introduced into the donor material to facilitate this etch. The donor wafer may also be polished and reused many times for this process. This process is shown in Fig. 1.48. This process may be repeated multiple times to form many device strata.

Semiconductor-on-Insulator Formation

Variants of the previously mentioned layer transfer process have been commercially used to produce semiconductor-on-insulator (SOI) substrates. An alternative process uses direct ion implantation of oxygen into a silicon substrate and is referred to as separation by ion implantation of oxygen or SIMOX as shown in Fig. 1.49. This process demands very high doses of oxygen implanted at high energies and a significant anneal step. Variations of this process have been proposed for localized oxidation on a CMOS wafer.

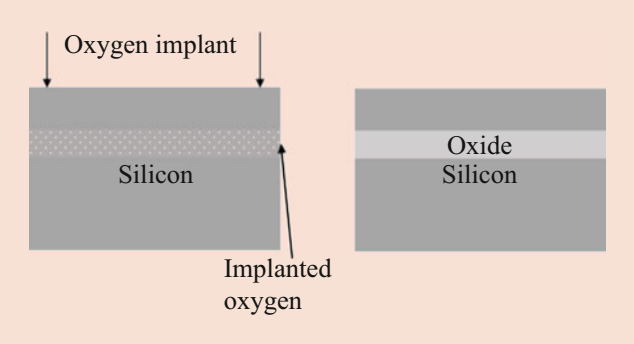


Fig. 1.49 An example of a SIMOX process. Oxygen is implanted at high doses and high energies into a silicon substrate to form a buried oxygen-rich layer. The structure is then annealed to form a buried oxide layer

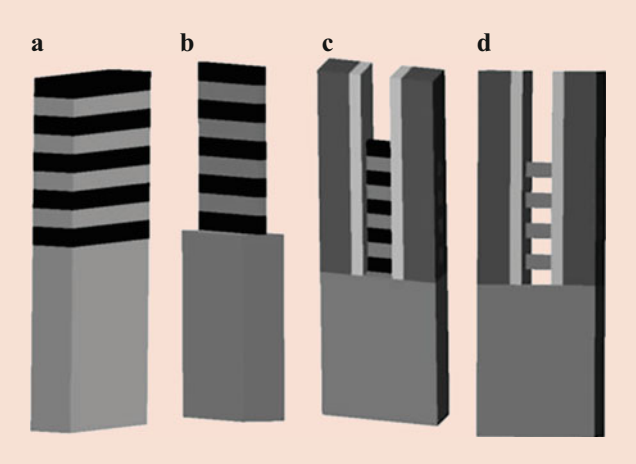


Fig. 1.50 A common process for the formation of a GAA transistor. (**a**) A series of alternating epitaxial layers are deposited upon a wafer with materials with high etch selectivity to each other (Si and SiGe are common); (**b**) fins are formed from this stack of epitaxial layers and a device is fabricated as would be done for a replacement gate process; (**c**) the sacrificial gate material is removed exposing the channel; (**d**) the sacrificial material is removed from the channel with a wet etch exposing the entire periphery of the nanowires. This step is done while the nanowires are stabilized by the source/drain and gate spacer. From this state, the processing is completed as normal with gate dielectric deposition and gate stack formation

Transistor Architecture Advances

The introduction of the FinFET or trigate device by Intel in 2011, with their 22 nm technology node process, was the first instance of a 3D transistor technology developed for high-volume manufacturing. Various industrial and research papers have indicated that the next architectural change is likely to be a transition to a gate-all-around (GAA) transistor. In addition, there have been several recent research papers looking at the vertical integration of transistors themselves. The two main approaches proposed for this are monolithic stacking and complementary FET (CFET) processes.

Gate-All-Around Transistor Structure Formation

The most common proposed process in literature for formation of a GAA transistor structure utilizes a series of epitaxially deposited layers on a blanket structure and a gate-last process. A fin is fabricated from this lattice structure, and the gate region is exposed with the source/drain region stabilized or a spacer in place as a stabilizer. A selective etch process is then utilized to remove one set of layers from the lattice structure in the gate region. From this structure, the gate dielectric can be deposited around the entire periphery of the individual wires, and a gate stack can be deposited atop that. This process is shown in Fig. 1.50.

Vertical Integration of Multi-Strata CMOS

Recently there has been a significant amount of research into means of placing transistors in a vertically stacked arrangement as a means to provide a new scaling vector. The two main approaches are a sequential monolithic stack such as used by LETI with their CoolCube™ architecture and the CFET approach from IMEC. Each of these approaches offer advantages and disadvantages.

The sequential monolithic stacked architectures such as CoolCube™ offer, perhaps, the simplest means to achieve 3D scaling. However, a sequential process comes at the cost of repeating virtually every operation in the front-end of the process which may minimize the cost savings. The density scaling provided by this approach, also, appears to be partially offset by the area required for inter-strata local interconnects. One of the main concerns with this approach is that the thermal processes of the second strata would deleteriously impact the electrical properties of the already formed devices and the development of a low-temperature process for the devices of the second device strata is a key enabler.

The CFET approach from IMEC utilizes a fin-over-fin monolithic approach with buried power rails. The proposed process for fabrication of this device places heavy emphasis on fill depositions and etch-back processes. This approach resolves several of the challenges associated with the CoolCube™ including challenges associated with local interconnects and enables a higher temperature process for the devices on the second device strata.

1.8.6 Stress Engineering

With the 90 nm process node, Intel was the first to utilize strain as a performance enhancer for a high-volume manufacturing CMOS process. In this process Intel utilized strain from a lattice mismatched epitaxial source/drain on the PMOS device (Fig. 1.51) and from a stressed cap layer on

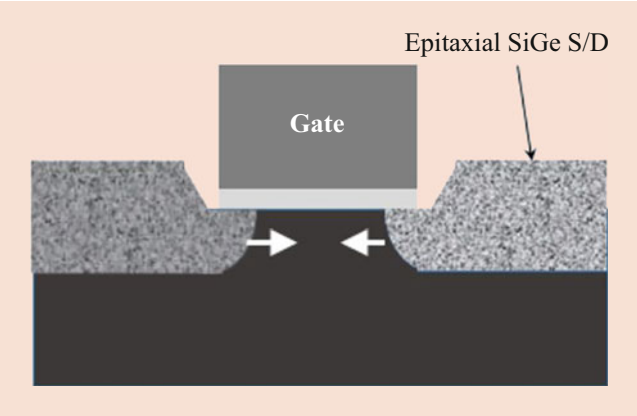


Fig. 1.51 An example of an epitaxial stressor inserted as a source/drain material for a PMOS transistor. The SiGe region has a larger lattice constant than the silicon region it is seeded from, and this serves to introduce a beneficial compressive stress within the PMOS channel

the NMOS device. Since this time, numerous other methods of introducing strain have been investigated including stress from dopants, dielectrics, and metals. It is likely that all future technology nodes utilizing silicon or other column IV semiconductors will utilize strain in some fashion, and it is important that these effects be considered when designing a process technology.

When considering stress in a transistor, the nuances of a process become of upmost importance. For instance, the same metal or film may be deposited with one of many different recipes, all of which will have a different stress associated with them. Stress effects may also diminish over distance from a free surface or geometry change; this can give a position-dependent stress response.

1.9 Summary

This chapter has introduced, at a very simplistic level, the fundamental processing operations utilized in the fabrication of CMOS integrated circuits and a brief introduction to foreseeable future trends in this field. Through these processes, it is possible to create nanometer-scale transistors and assemblies with the high degree of repeatability necessary for high-volume manufacturing.

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Semiconductor Memory Technologies

2

Paolo Fantini, Giorgio Servalli, and Paolo Tessariol

Contents

2.1 Introduction . . . 38
2.2 Semiconductor Memories Taxonomy . . . 38
2.3 Volatile Memory . . . 41
2.4 SRAM Cell and Basic Operating Principles . . . 41
2.5 SRAM Scaling . . . 42
2.6 DRAM Cell, Array, and Basic Operating Principles . . . 45
2.7 DRAM Technology Evolution . . . 46
2.8 DRAM Capacitor Scaling . . . 48
2.9 DRAM Access Transistor Scaling . . . 49
2.10 DRAM Product Evolution . . . 50
2.11 Nonvolatile Memory: The Flash Memories . . . 51
2.12 Floating Gate MOSFET Devices . . . 51
2.13 Flash Memory MOSFET Devices . . . 53
2.14 Charge Storage Solutions . . . 54
2.15 Charge Injection/Extraction Mechanisms: Programming/Erase Operations . . . 55
2.16 NOR Flash Array, Operations, and Reliability Aspects . . . 55
2.16.1 NOR Flash Applications and Roadmap . . . 57
2.17 NAND Flash Array, Operations, and Reliability Aspects . . . 57
2.18 NAND Flash Roadmap . . . 60
2.19 Emerging Memories: An Insight on Phase-Change Memories . . . 60
2.20 In-Memory Computing and Neuromorphic Applications . . . 64
References . . . 66

Abstract

The aim of this chapter of the *Handbook of Semiconductor Devices* is to provide an overview on semiconductor-based memory technologies. A preliminary introduction will contextualize the topic considering the actual scenario of the memory ecosystem. Then, the chapter will describe the main volatile memory technologies, in terms of fundamental operating principles and memory array organization. In the following, the principles, the applications, and the roadmap of the main nonvolatile memory technology will be presented. A subsequent section will illustrate the phase-change memory (PCM) technology as example of emerging memory technology among various flavors that will be cited. The chapter will close with a forward looking considering the potential opportunities of emerging memory technologies in the field on in-memory computing and neuromorphic applications.

Keywords

Memory technologies · Semiconductor devices · Emerging memories · DRAM · Flash · NAND · PCM · In-memory computing

2.1 Introduction

The ability to generate, store, and share information is indubitably a sign of civilization. In fact, these abilities strongly grew up over the millennia and centuries of the human history. Since the Rosetta Stone period, the oldest memory device that the human invented thousands of years ago,

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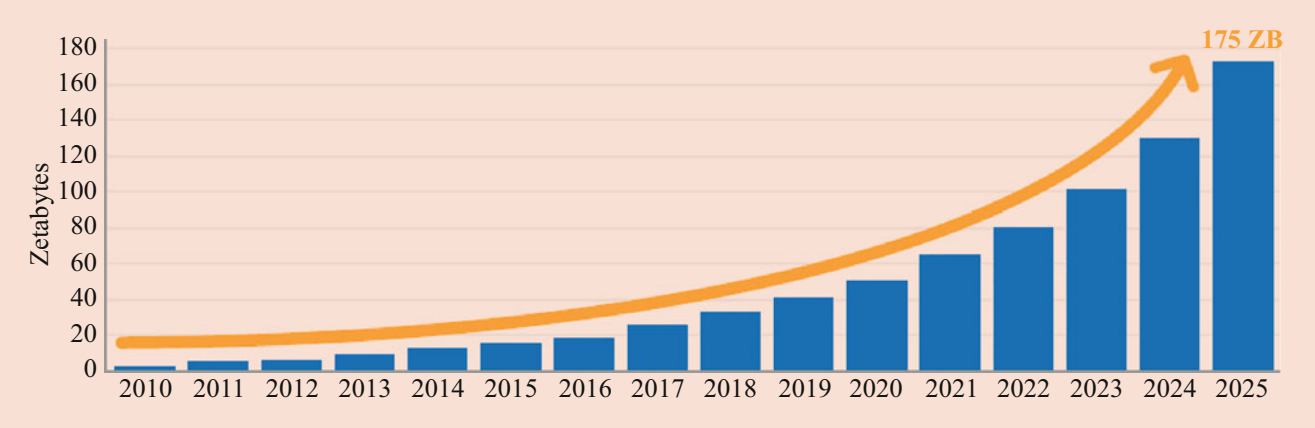

Fig. 2.1 Trend of Global DataSphere, from D. Reinsel, et al., "Data Age 2025", IDC White Paper (2018) [1]. (Source: Data Age 2025, sponsored by Seagate with data from IDC Global DataSphere, Nov 2018)

the information and data that man has created and that, thanks to the amazing retention time of some writing and imaging generation techniques, arrived up to us progressively increased. Coming closer to nowadays, the miniaturization of the digital computers that started ~40–50 years ago marked a dramatic exponential increase of data production and storing that does not show any hint to slow down. On the contrary, it is predicted to explode in the next years, asking more and more support to the semiconductor memory technology (see Fig. 2.1). Already actually, there are more than 2.5 exabytes of data created each day, and this trend is accelerating with the pervasion of the Internet of Things (IoT). We also would like to recall that the term Google is born from a misspelling of Googol, coined in mathematics to represent an incredibly high number 10^100, roughly corresponding to the total number of particles in our universe. This scenario depicts a context where semiconductor memories are occupying a more and more important role in the semiconductor technologies.

The aim of this chapter of the *Handbook of Semiconductor Devices* is to illustrate the actual scenario of semiconductor memory technologies; the chapter is organized as follows:

- The first section will provide a general introduction to sketch the classes of memory technologies in terms of volatile, nonvolatile, and emerging memories, their fundamental features, and applications.
- The second section will be a dig into the volatile memory technologies;
- the third section will be dedicated to explain the principles, the applications, and roadmap of the actual nonvolatile memory technology.
- The fourth section will deepen the phase-change memory (PCM) technology among the various flavors of emerging technologies, illustrating the device physics and architecture together with the main issues of PCM technology to challenge conventional nonvolatile memory solutions.
- The last section will be dedicated to the potential opportunities of the memory technologies in the field on in-memory computing and neuromorphic applications.

2.2 Semiconductor Memories Taxonomy

Semiconductor memory has always been an indispensable component and backbone of modern electronic systems. All familiar computing platforms ranging from handheld devices to large supercomputers use storage systems for storing data temporarily or permanently. Figure 2.2 reports in a tree structure the various typologies of semiconductor memories that can store data in the form of binary information (bits). It shows that a storage unit is distinguished into two main categories:

1. Volatile memory: it loses its data, when the power is switched off.
2. Nonvolatile memory: it is a permanent storage and does not lose any data when the power is switched off.

Two types of volatile memories, both invented more than 50 years ago, are listed: DRAM and SRAM. The class of nonvolatile memories is more expanded, including EPROM, EEPROM, flash, and ROM. In this variety, the present chapter will describe in detail the flash memories, as significant nonvolatile memory technology that serves today an actual computer system together with DRAM and SRAM.

They have been in fact circled in the scheme of Fig. 2.2 as objects of the description of their working principle and applications in the following of the chapter.

Since the functionality and performance of today's computing systems are more and more dependent on the characteristics of the memory subsystem, another memory taxonomy with respect to this usage can be illustrated. In this context, the solid-state memory system that currently serves

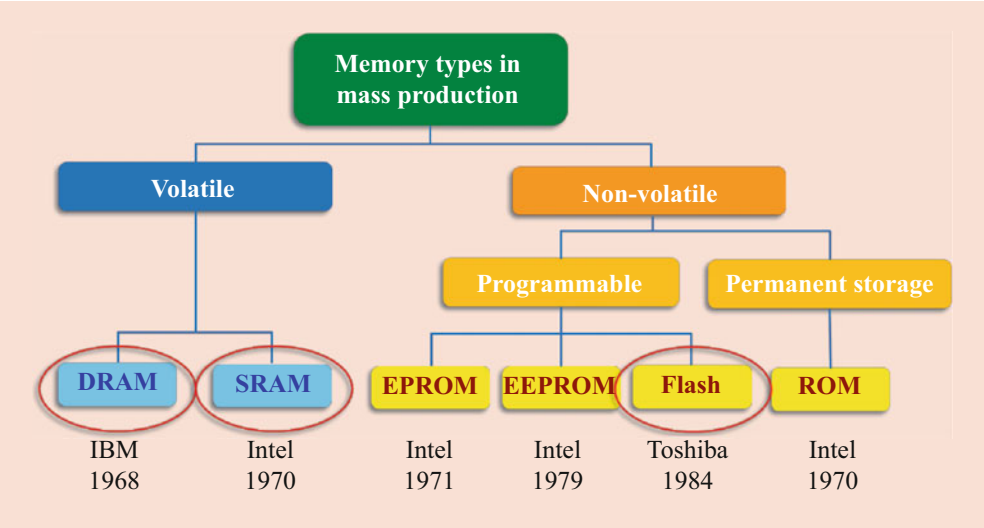

Fig. 2.2 Types of semiconductor memories that reached the mass production. The circled types of memory are the main memories that serve today an actual computer system and that will be described in the present chapter

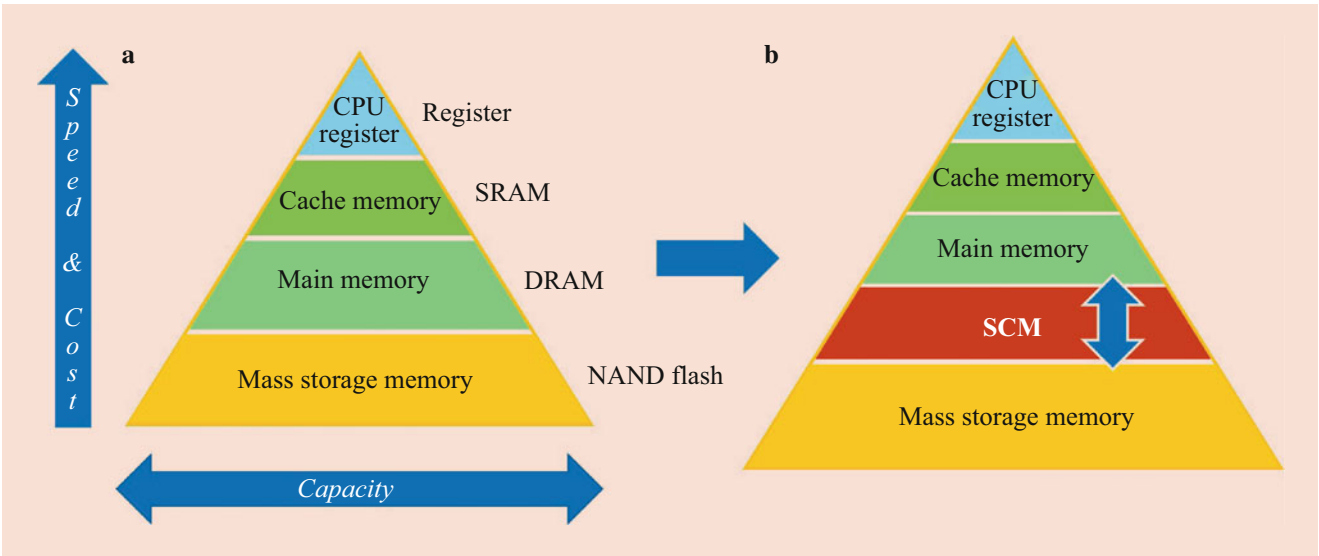

Fig. 2.3 (**a**) Memory hierarchy organized according capacity, cost, and speed parameters. (**b**) The same hierarchic scheme with the addition, between the gap in capacity, cost, and speed of DRAM and flash of the storage class memory (SCM) as new memory system. SCM represents the ideal realm for the emerging memory technology as it will be discussed in the chapter

the CPU is organized according a hierarchy based on these three parameters, the response time, the capacity, and the cost as reported in Fig. 2.3, exploiting the shape of a segmented pyramid, where the extension of the portions of the pyramid are related with the memory capacity and the vertical position has to deal with the memory speed and cost that typically move together.

The parameter that defines the speed of memory is the latency, defined as the time taken to transfer a block of data either from main memory or caches. The latency is thus the time the CPU waits to obtain the data. The types of memory that in Fig. 2.3 are at the basis and the vertex of the pyramid show, respectively, complementary features: at the basis, there is the NAND memory technology that is slow but nonvolatile and cheap and serves as the main solid-state storage memory. Close to the vertex of the pyramid, there are SRAM and DRAM that are fast, answering to the CPU with very low latency time, thus serving as the main working memory, but volatile. Since neither DRAM nor NAND is ideal for the needs of the system, the concept of "universal" memory was introduced in the early 2000s, combining the best of DRAM with the best of NAND features. This concept alludes to a potential new memory that could possibly replace several of the existing nonvolatile memory technologies such as NAND flash and even replace some current volatile memory technologies such as DRAM

Table 2.1 Taxonomy of NAND and DRAM as a function of their attributes

Attributes	NAND	DRAM
Nonvolatile	Yes	No
Scaling to	1× nm	1× nm
Power	~flash	High
Write bandwidth	10+ MB/s	100+ MB/s
Read latency	15–50 us	20–80 ns
Endurance	10^4–10^5	Unlimited

with a nonvolatile but equally high-performance memory, opening up new memory and chip design concepts. Indeed, nowadays this dream has been abandoned with the awareness that both the memory systems and the market are not in favor to give away to any performance of DRAM and NAND and the bundle in a single memory device of all the advantages of DRAM and NAND, simultaneously, is not realistic. In addition, physiology indicates that the human memory shows, from neurological basis, as a heterogeneous entity with complementary features, including the short-time memory (like DRAM, short both for latency and retention) and the long-time memory (like NAND, long both for latency and retention): this supports the idea that a heterogeneous memory ecosystem is the right direction to efficiently serve a modern computer system.

However, the gap in performance between DRAM and NAND spans several orders of magnitude on many key technology parameters illustrated in Table 2.1: the scalability, the programming power, the write bandwidth, the time latency, and the endurance over the programming cycling.

In particular, a part the volatility that has been recalled, there are two value propositions that are both, someway related with the velocity: the bandwidth and the latency. However, they indicate, specifically, different aspects of memory performance related with the concept of velocity. Nevertheless in synoptic Table 2.1, bandwidth is reported for write and latency for read, and they can be referred to as both write and read operation. But while latency refers to the transfer time needed to read or write a block of data, the bandwidth represents the amount of data that can be read or written within a unit of time (in other words, it measures the throughput of memory). An acute paper written by D. Patterson in 2004 [2] explains very well as bandwidth was more significantly helped by the technology scaling according with Moore's law, enabling more devices per unit of area that can operate in parallel. At variance, latency that is the fundamental measure of the speed of memory is more difficult to be improved. And this led to a chronic imbalance between bandwidth and latency with the technology scaling. D. Patterson reports in his paper this illuminating exergue by an Anonymous: "There is an old network saying: Bandwidth problems can be cured with money. Latency problems are harder because the speed of light is fixed—you can't bribe God." This has been true for temporary memory devices closer to the CPU, at the vertex of the pyramid of Fig. 2.3, like the cache and the DRAM that directly serve processors for computing operations. But it has been also more dramatically true for permanent memory of which, for many years, the hard disk drive (HDD) was the embodiment. In fact, the mechanical movement of the head in a specific sector of the HD platter necessary for any read or write operation was inherently slow, thus the HDD performance did not improve so much when, at variance, the performances of the CPU strongly improved over the technology roadmap. Hence, few years later, at IEDM 2009, Al Fazio by Intel [3] underlined the need to improve the latency of permanent memories to better serve the computing systems, where most memory accesses are nonsequential. The introduction of NAND technology to build solid-state disks (SSDs) that replaced the HDD represented a significant step forward in this direction. But there is room to do more. In fact, coming back to Table 2.1 and looking at the application requirements, the so large gap between DRAM and NAND (several orders of magnitude!) required, in the last years, the definition of a new type of memory. Such a new memory system is referred to as storage class memory (SCM) [4]. The goal for a SCM is to complement the existing memory hierarchy and operate at a performance and cost between that of NAND flash and DRAM as sketched in Fig. 2.3b. It represents a big opportunity for *any* emerging memory with properties in between DRAM and NAND, both in terms of latency (access time <10 ms) and cost (cost <1$/GB). Being so wide the SCM gap, two spaces exist for a SCM to enter in the market: a storage-type SCM, which operates as a faster, higher endurance NAND flash, whose primary driver is the cost, and a memory-type SCM, which is similar to DRAM with the added nonvolatility benefit, whose primary focus is on write speed and read latency. Close to the end of the chapter the phase-change memory will be presented also in terms of its potential ability to cover SCM applications.

2.3 Volatile Memory

In 1945, John von Neumann wrote a paper, titled *The First Draft of a Report on the EDVAC* [5], with a detailed description of a "very high speed automatic digital computing system." This paper is recognized as the foundation of modern computer architecture, in which the data and the program codes are both stored in the computer's memory in the same address space. The von Neumann architecture was widely used since the late 1940s and is still the standard architecture for most computers. The use of memory in digital computers to store both sequences of instructions and data was a breakthrough to which von Neumann made major contributions. Figure 2.4 reports the von Neumann computer architecture scheme.

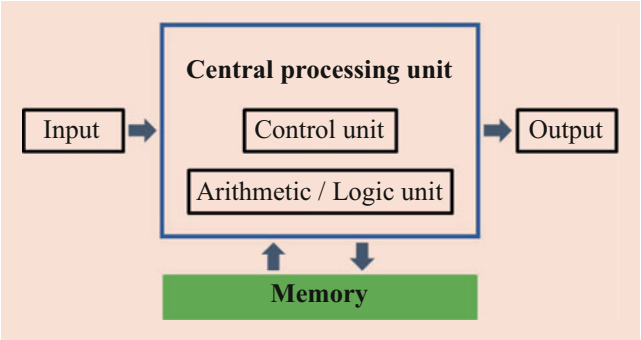

Fig. 2.4 Scheme of von Neumann architecture for a computing system with memory

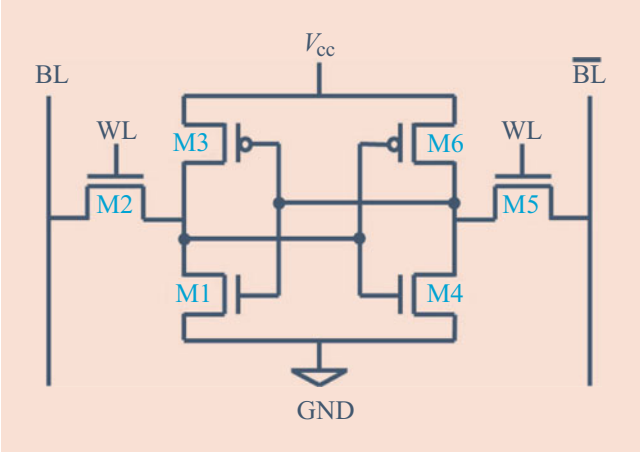

Fig. 2.5 6T SRAM cell schematic

In all modern computers and in most of high-performance electronic systems, the role of memory is played by two kind of devices: SRAM (static random access memory) and DRAM (dynamic random access memory). Both are volatile memory, which means that they retain data only if power is supplied to the devices.

SRAM is a type of semiconductor memory that uses bistable latching circuitry to store each bit of data in a single cell which is composed by several CMOS transistors. SRAM devices provide the fastest access to data and are typically used for computer cache memory and as part of the random access memory digital-to-analog converter on a video card. Once data are written in a SRAM cell, retention is guaranteed as long as power is supplied, without need for a periodic refresh of the information.

DRAM is a type of semiconductor memory that stores each bit of data in a cell composed by a capacitor and a transistor (the so-called 1T1C cell). Binary information is stored as positive or negative charge in the capacitor, and the transistor is used to access the capacitor. A DRAM cell will lose its information in a fraction of a second because of leakage, so a periodic refresh operation is needed to retain the data while the system is active. A DRAM cell is much smaller than SRAM and allows to reach very high densities at a much cheaper cost: this is the reason why DRAM is used as main memory instead of SRAM, despite the added complexity and power needed by refresh management.

2.4 SRAM Cell and Basic Operating Principles

The integrated bipolar SRAM was invented by Robert H. Norman at Fairchild Semiconductor in 1963 [6], becoming an alternative to magnetic-core memory. It was followed by the development of MOSFET SRAM, requiring six MOS transistors for each bit of data, invented by John Schmidt at Fairchild in 1964. Commercial use of SRAM began in 1965, when IBM introduced the SP95 memory chip for its System/360 Model 95, the first family of computer designed to cover a complete range of applications. Since early development, CMOS technology has been recognized as superior for SRAM application with respect to bipolar since it reduces power and allows to reduce cell size.

The SRAM memory cell works thanks to cross-coupled connection of inverters: SRAM uses bistable latching circuitry to store each bit. The basic SRAM cell is built with six transistors, with two back-to-back connected inverters: the output of each inverter is connected to the input of the other one forming a latch. Access to the cell occurs through a wordline and through two bitlines which use complementary voltage signals.

The working principle of a SRAM cell is briefly explained referring to Fig. 2.5.

When the wordline (WL) is at 0 V, the access transistors M2 and M5 are in off state, and the data is held in the latch. To write the cell, WL is raised to V_{cc} while the data (V_{cc} or 0 V) is applied to the bitline (BL) and the complementary data is applied to the complementary bitline BLB: in this way the latch is forced to move in the direction of the applied voltages, and the charges in the latch are overwritten with the new values. To have a good write capability, a high pull-up ratio is needed, that is, a high ratio between the current driven by transistor M2 with respect to the current of transistor M3 (and equivalently of M5 respect to M3).

To read the cell, the WL is raised again to V_{cc} and the charge of the latch can flow through the bitlines to reach the sense circuit, which is a simple differential amplifier. The stability of read requires a high cell ratio, meaning a high ratio between the current driven by transistor M1 with respect to the current of transistor M2 (and equivalently of M4 respect to M5): in this way the cell is less exposed to disturb issues during read.

Alternative SRAM cells with eight or ten transistors are used to allow multiple access to the same SRAM cell simultaneously, providing a memory with higher data bandwidth, at the cost of layout size, lower speed, and higher power consumption.

SRAM cell are built with the same MOSFET devices of logic processors and is the only memory architecture whose speed is comparable to the one of logic ports. For this reason, despite having a large cell area, SRAM is still today the main type of semiconductor memory, used as cache integrated into processor chips (Chap. ► 12).

2.5 SRAM Scaling

Because of the complexity of 6T circuit and the need to connect each cell to an array with common wordlines and bitlines, the area of a single SRAM cell is quite large with respect to the minimum lithographic feature λ that can be printed, as reported in Fig. 2.6

In the first generations of CMOS technologies, SRAM cell is scaled following general technology rules, using devices with dimensions balanced to optimize performances. In the most recent generations of microprocessors, which use several levels of cache to improve performances and parallel processing, SRAM arrays occupy a large fraction of the area of the whole chip: for this reason, cell SRAM scaling is a primary technology parameter, and the size of high-density 6T SRAM cell is often used as the key metric for pure logic technology density.

To allow length scaling with a proper control of short-channel effects, the conventional CMOS transistors based on SiO_2 oxide have been progressively replaced by devices with stress engineered junctions and then by high K metal gate transistor from 45 nm on. Scaling involves not only dimensions but also voltages: V_{cc} reduction is a key element to allow device scaling and to reduce the power consumption at chip level, and this is again a critical factor for cell stability.

SRAM cell uses devices with minimum width and length and for this reason is more exposed to process-induced variations in device size, threshold voltage variability due to dopant fluctuations, and mismatch issues: all these problems reduce the cell working window, its stability, and finally its yield.

The scaling of SRAM arrays involves not only the scaling of the transistors of each cell, but also the improvement of the layout of the 6T cell to make it scalable-friendly. The traditional layout of a SRAM cell as in Fig. 2.6 was realized in a way to optimize some array characteristics, sharing horizontal routing for the wordlines, and vertical routing for the bitlines, power, and ground, but the shape of all the lines is complex.

From 65 nm on, the layout of SRAM cell has been modified to what is called “thin cell” or “wide cell,” shown

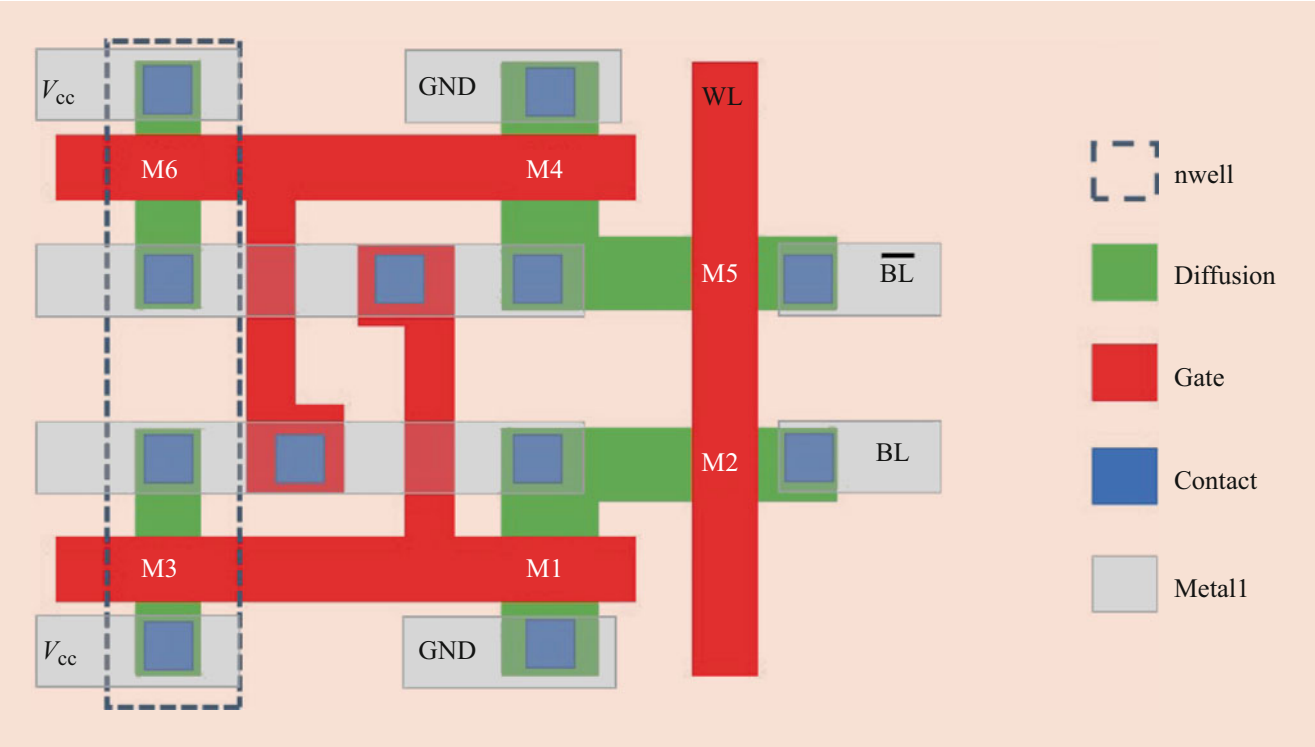

Fig. 2.6 Example of 6T SRAM cell layout; connections above metal1 are not shown

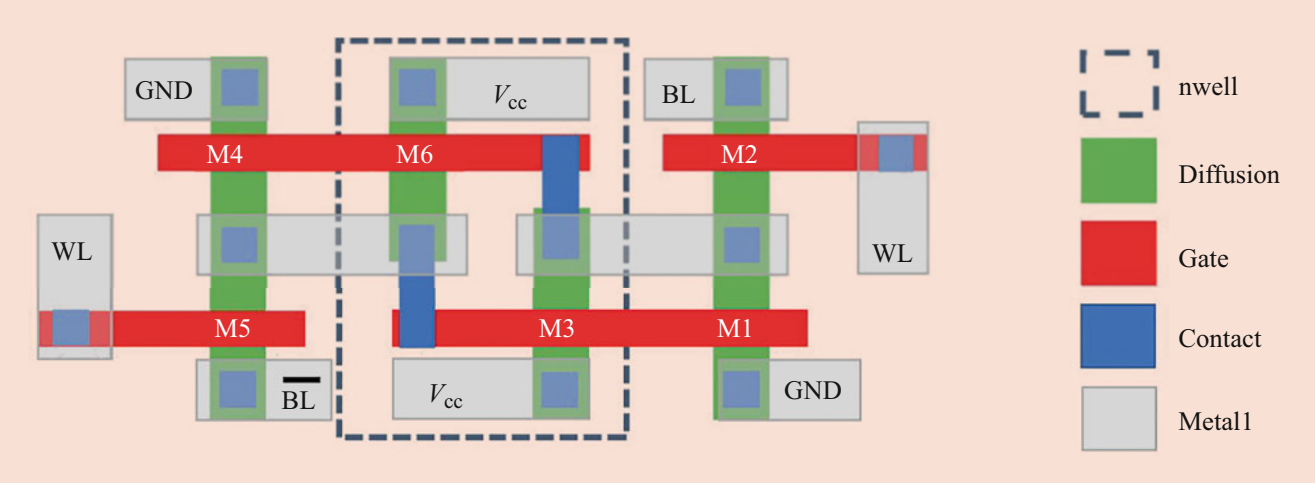

Fig. 2.7 Example of the "thin" 6T SRAM cell layout; connections above metal1 are not shown

in Fig. 2.7, where bending of diffusions and gate lines are avoided, transistors are all oriented in one direction, and bitline capacitances are minimized: this modification helps not only to improve the cell performances in terms of transistor matching and low capacitance but also to simplify lithography and patterning steps, allowing to scale the area of the cell thanks to the scaling of the active devices and to the tightening of the spacings and of the process tolerances.

The introduction of patterning-friendly layout at all levels, including the very tight contact and metal interconnections, allowed to extend the use of 193 nm lithography and 193 nm immersion lithography well beyond the optical resolution limits, thanks to self-aligned multiple patterning solutions. Scaling of 6T SRAM cells over various technology nodes are schematically shown in Fig. 2.8, as from [7–11]. Self-aligned quadruple patterning solution is used for 10 nm state-of-the-art technology. EUV lithography is expected to be introduced at 7 nm node.

From 22 nm technology on, planar MOSFETs are replaced by FinFET (Fig. 2.9), invented in 1988 in Hitachi's labs [12]. Differently from planar devices, FinFETs have several advantages for scaled and low-voltage applications: short-channel effects and subthreshold current are much better controlled thanks to the fact that the gate surrounds the channel; better gate control allows to use devices with very low threshold, which is fundamental to reduce voltages, and enables low channel doping, which further improves performances and uniformity among devices.

At the same time, FinFET devices limit the flexibility in the design of SRAM cells, since the width of each transistor in the SRAM can be only an integer multiple of the width of a single fin; this constraint, together with the reduction of the supply voltage, is critical with respect to the working window of the cell and has been addressed with a dedicated management of voltages in the SRAM array [13].

Table 2.2 6T SRAM cell scaling for Intel processors technologies

Date	Technology node (nm)	SRAM cell size (μm^2)	V_{cc} (V)
1993	500	44	3.30
1995	350	21	2.50
1997	250	10.6	1.80
1999	180	5.59	1.60
2001	130	2.09	1.40
2003	90	1	1.20
2005	65	0.57	1.20
2007	45	0.346	1.00
2009	32	0.148	0.75
2011	22	0.092	0.75
2014	14	0.0499	0.70
2019	10	0.0312	0.70

Thanks to all these solutions, SRAM cell area has been continuously scaled in the last 25 years, following up to 2009 the fast pace dictated by Moore's law (number of transistors per unit area doubles every 2 years); from 2009, the scaling is continuing with a lower speed. Table 2.2 shows the scaling path for SRAM 6T used in Intel processors from 1993 onward [14].

Alternative SRAM cell architectures have been developed to reduce cell area with respect to 6T standard: for example, a 4T 2R SRAM cell can be built, substituting p-channel transistors M3 and M6 of Fig. 2.5 with two highly resistive resistors.

4T 2R SRAM cells have been widely used in standalone SRAM market in the past, but this architecture has been abandoned in the most recent technologies because of added technology complexity (need to integrate extra layers for polysilicon resistors in high-performance logic technology) and because of worse performance at low-voltage operation (increase off current flowing in the resistors and poor mem-

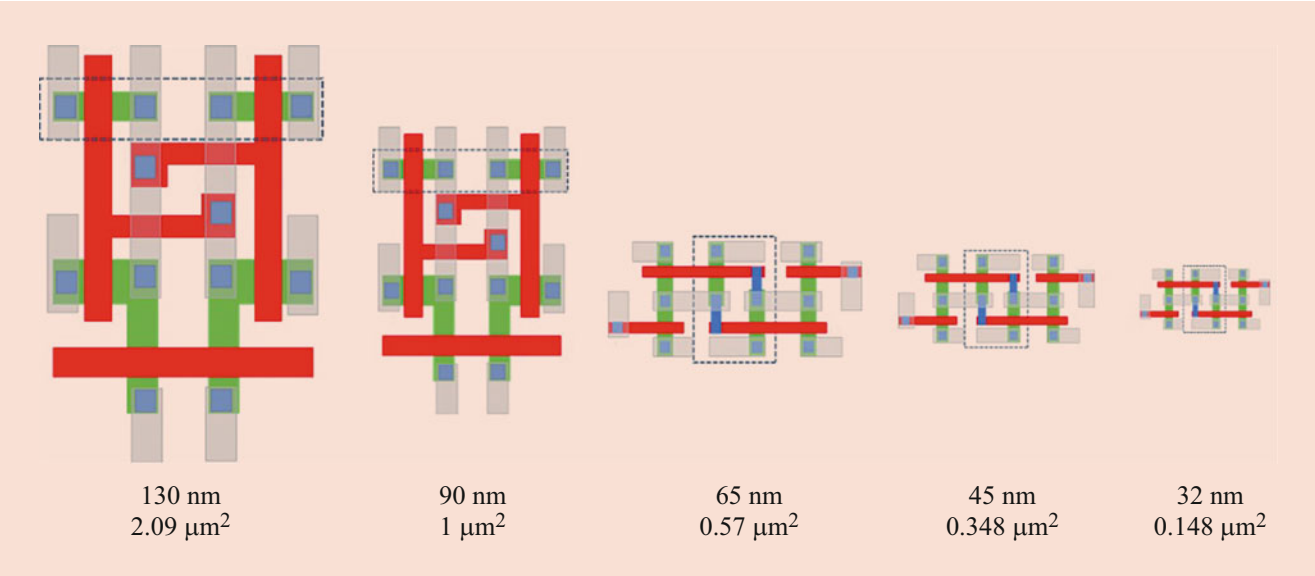

Fig. 2.8 Scaling of SRAM cells, showing the transition to thin 6T cell from 65 nm technology on

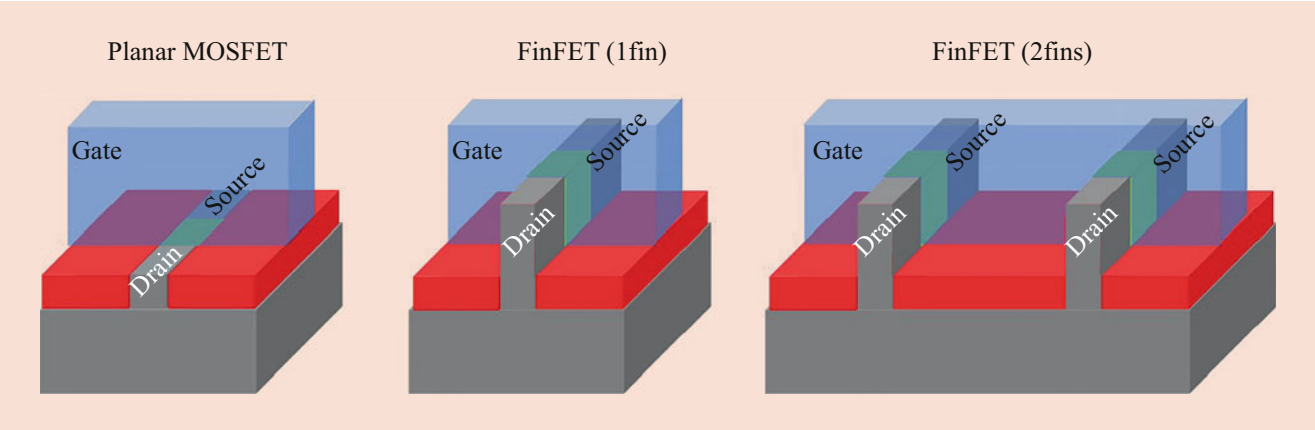

Fig. 2.9 Conventional planar MOSFET vs FinFET devices with one or two fins

ory cell stability because of low static noise margin below 1.8 V) [15].

2.6 DRAM Cell, Array, and Basic Operating Principles

DRAM was invented at IBM by Robert Dennard in 1966 [16]: while he was working on field-effect transistors, he had the idea to store binary data in a capacitor, as positive or negative charges, with a very fast programming and reading speed. But Dennard had to face the problem of leakage out of the capacitor, so that the information could be lost in few milliseconds. For this reason, he proposed and developed a solution where a single MOSFET device could read the charge and put it back thousands of times per second, in the so-called "refresh" operation. This single access transistor would then be responsible for each bit of information, thus reducing the size of the whole cell dramatically with respect to SRAM cells just developed. The constant refreshing of the charge on each capacitor is why Dennard's chip is referred to as "dynamic" RAM. The ultimate effect of Dennard's invention was that a single chip can hold a billion or more RAM cells in modern computers.

In 1970, the newly formed Intel company publicly released its first DRAM, the famous 1103 1 Kbit chip, which by 1972 was the best-selling semiconductor memory chip in the world, definitely defeating magnetic-core type memory which was bigger, costlier, and more power-consuming.

Today DRAM is still based on the original concept, but the evolution of the technology in 50 years has been dramatic, as we can see in Table 2.3, that compares some of the most relevant characteristics of a 1973 4 K DRAM to 2015 8 Gb DRAM chips.

A DRAM 1T-1C memory cell is formed with one transistor and one capacitor (Fig. 2.10a). The capacitor, with capacitance C, holds binary information in the form of stored charge Q, while the transistor, called access transistor, operates as a switch between the capacitor and the digitline that connects the cell to the sensing circuitry. One of the terminals of the capacitor is called plate, and it is a common node biased at $V_{cc}/2$. The other terminal can be biased to V_{cc} or to 0 through the access transistor, storing a positive or negative charge $Q = \pm V_{cc}/2{*}C$ corresponding to logic state 1 or logic state 0.

A DRAM device is composed by an array of 1T-1C cells (Fig. 2.10b), organized in wordlines (rows) and digitlines (columns). Each digitline consists of a multitude of DRAM cells and is highly capacitive because of the quantity of cells connected and because of the proximity to other features: digitline capacitance is a key parameter for DRAM design. The gate terminal of the access transistor is connected to a wordline, common to a multitude of cells and physically orthogonal to the digitlines.

Reading a DRAM is a differential operation, involving pairs of digitlines (see Fig. 2.11). To read data from a DRAM array, first all the digitlines are equilibrated to $V_{cc}/2$ with the wordlines off. Then a single wordline is raised to a voltage called V_{ccp}, which is higher than V_{cc} plus the threshold voltage of the access transistor. At this moment, all the capacitors connected to the selected wordline begin to discharge, each of one sharing its own charge to its digitline, whose voltage consequently increases in case of stored 1 or decreases in case of stored 0, generating a small signal (typically less than 200 mV). The value of this signal is a function of the cell capacitance C, of the stored charge Q, and of the digitline capacitance C_{digit}:

$$V_{signal} = \frac{Q}{C + C_{digit}} = V_{cc} \cdot C / \left(C + C_{digit}\right)$$

The small signal of each cell is sensed with an amplifier connected to each digitline, which compares the signal with a reference voltage coming from a paired digitline which has no selected wordline. This sensing circuit amplifies the small signal to a digital V_{cc} or 0 V value.

During the read operation, the charge on each selected cell is lost: it's a destructive read. Since the selected wordlines remain at high voltage during the reading process, the amplified signal is written back from the sensing circuit into the cell capacitors, restoring the charge on the selected capacitors. When the reading operation is completed, the wordline is turned off, trapping the fresh charge in the cell.

Write operation in a DRAM is similar to the sensing and restoring steps which happen in read, except that a separate circuitry determines the data that will be placed into the cells: the voltage of each digitline is forced to V_{cc} or 0 V by the write drivers and then a wordline is turned on to V_{ccp} to charge or discharge the capacitor of each cell.

As already underlined, the DRAM capacitor loses its charge is a short time, because of leakage current of the access transistor. To keep the information, a periodic refresh

Table 2.3 Comparison of early DRAM features to recent devices

	MOSTEK1973	Micron2015
Density	4 Kbit	8 Gbit
V_{cc}	12 V	1.2 V
Minimum lithography feature	8 μm	17 nm
Cell area	1280 um^2	2555 nm^2
Clock rate	3 MHz	1600 MHz

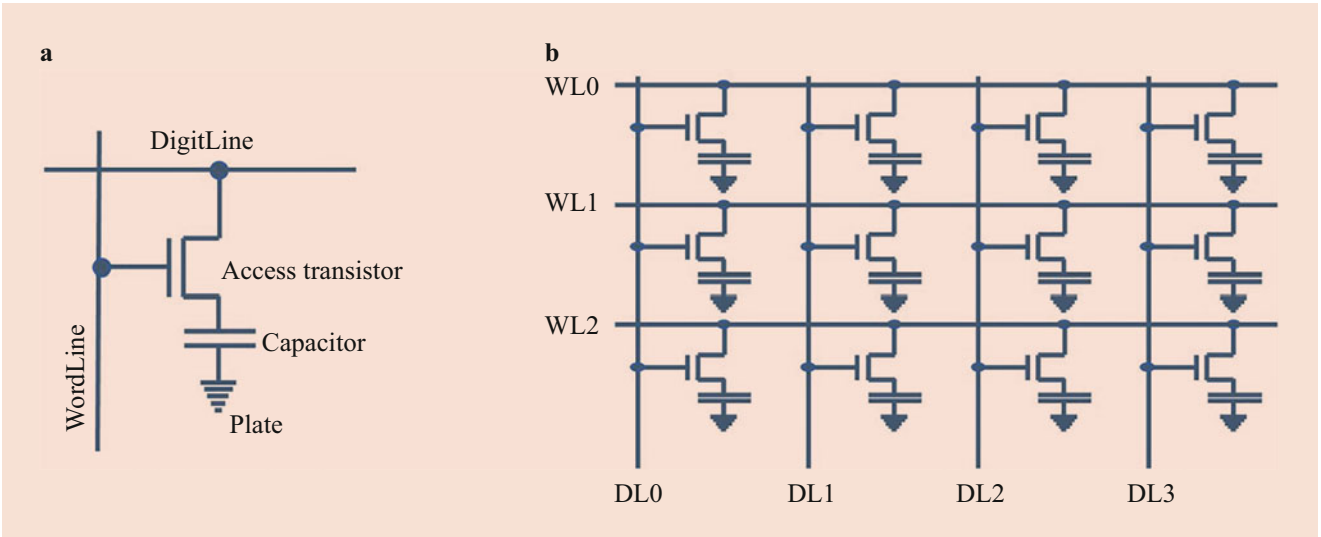

Fig. 2.10 (**a**) Schematics of 1T-1C DRAM memory cell and (**b**) of DRAM array organization

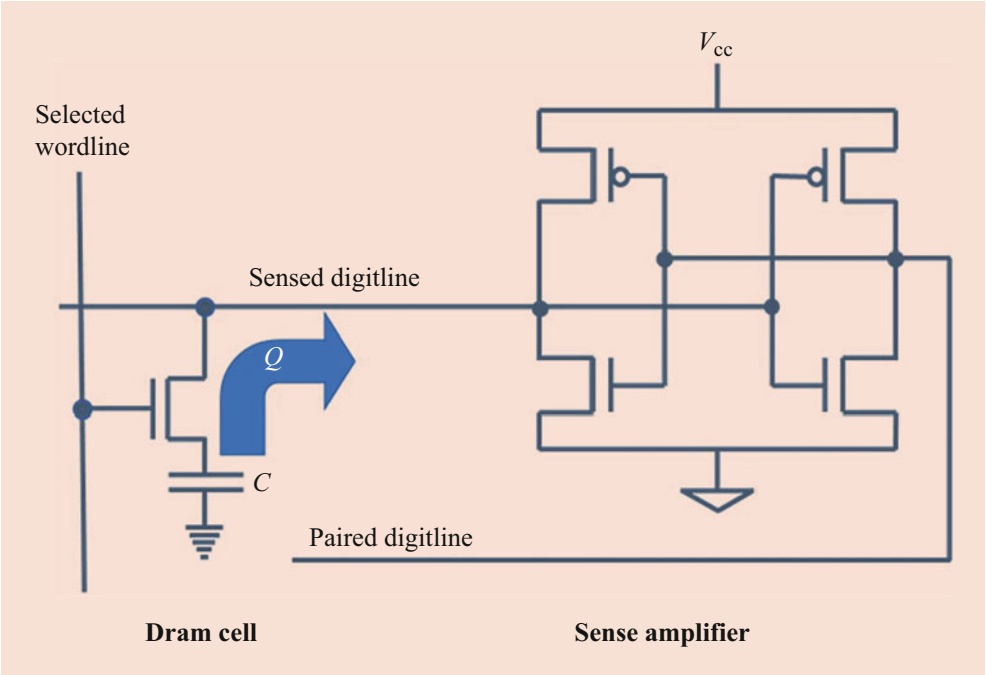

Fig. 2.11 Differential sensing of a DRAM cell

operation is needed on each single cell every few ms, typically between 64 ms and 32 ms in the recent devices. The refresh operation works like a read operation, which restores the full charge on each single capacitor.

2.7 DRAM Technology Evolution

The evolution of DRAM technology followed Moore's law from the early 1970s up to 2015, scaling the array features from 8um down to 20 nm in 45 years. Cell area scaling was executed in parallel with cost reduction, power reduction (mainly through operating voltage scaling), density increase, and performance increase, introducing huge technology and design innovations on the same basic device concept developed by Dennard.

We can observe a reduction of scaling rate in the last 5 years (see Fig. 2.12), because of the increasing challenges in cell area reduction, but DRAM unique features are hard to be replaced in a short term by other technologies, in particular considering its fast switching speed (~10 ns), its small switching energy (~2 fJ/cell), its unlimited cycling endurance, and its small cell area with simple 1T-1C structure.

DRAM technology scaling involves all the key elements of array: capacitor, access transistor, WL and DL resistances and capacitances, and CMOS circuitry performances.

Also the integration of these devices into an efficient array is an impressive accomplishment of DRAM technology: beside lithographic and patterning evolution, which is tracked by the minimum feature λ, the layout of DRAM cell improved from $20\lambda^2$ in the early 1990s to $6\lambda^2$ today, as shown in Fig. 2.13, with the possibility to move to $4\lambda^2$ area [17].

This improvement in the cell form factor has been realized moving the integration from a conventional planar approach derived from CMOS technology to a dedicated 3D approach which leverages on the integration in the vertical direction, using the space below the silicon surface and the one above it.

In the next paragraphs, we will focus on the dramatic evolution of the key devices of the cell: the capacitor and the access transistor.

2.8 DRAM Capacitor Scaling

At a first approximation, digitline capacitance is constant with scaling, since the reduction of the distances between adjacent digitlines is compensated by the reduction of digitline lengths. Since the signal of the cell is related directly to the ratio between the charge stored in the capacitor and the digitline capacitance, also the capacitance of the single DRAM must be kept approximately constant to have a good signal. It means that the capacitance per cell area needs to be increased, node by node, working on all the directions: increasing the dielectric constant of the capacitor, reducing the dielectric thickness, and increasing the effective area of the capacitor, all with the constraints of dielectric leakage control to have a tolerable refresh rate.

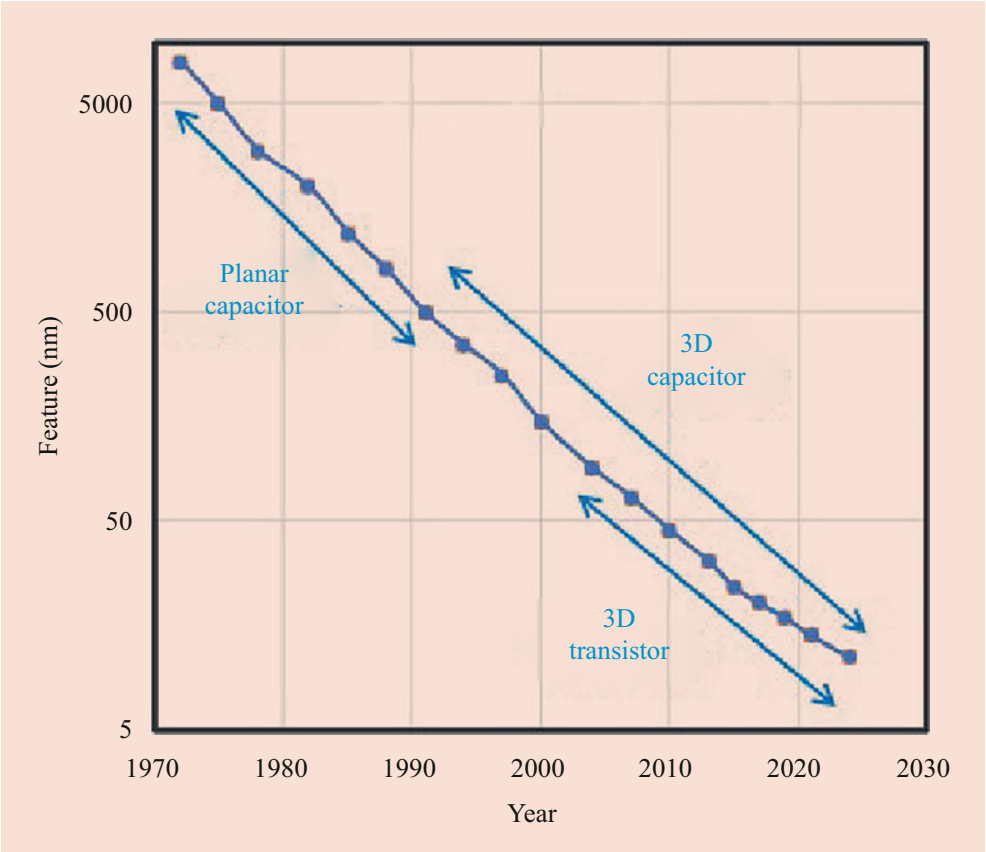

Fig. 2.12 Scaling of DRAM technology expressed in terms of minimum feature λ. (Source: Various publications & IRTS)

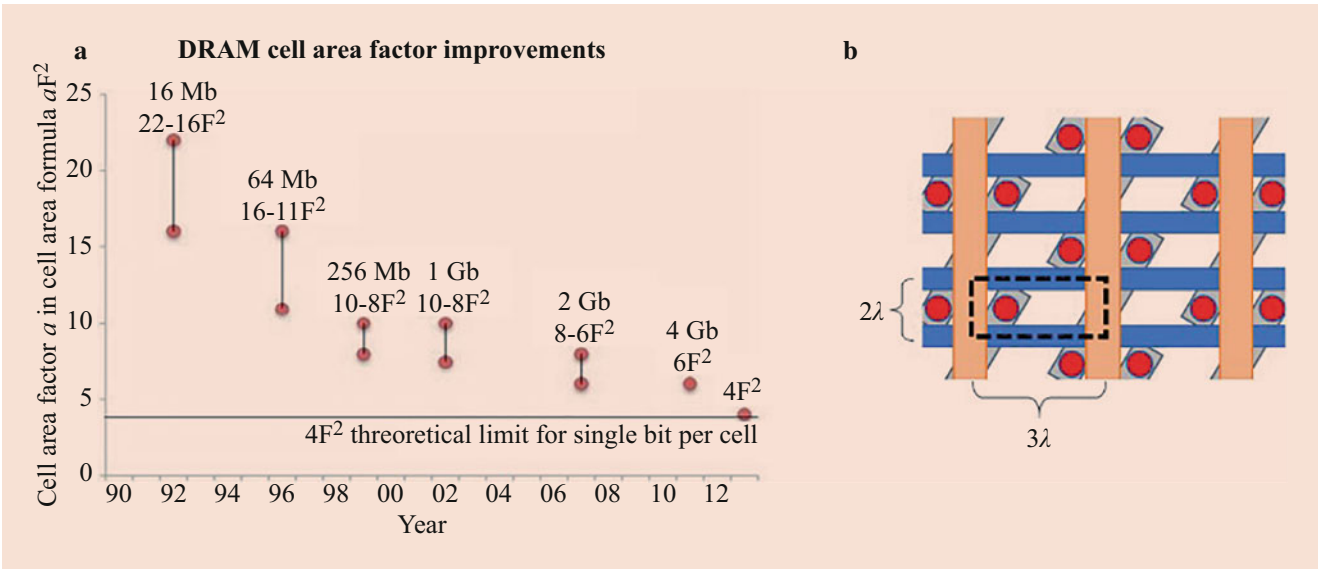

Fig. 2.13 (**a**) Scaling of DRAM technology expressed in terms of minimum feature λ and (**b**) compact layout of a state-of-the-art $6\lambda^2$ DRAM cell

The first DRAM cell was built with a pure planar process, with a SIS (semiconductor-insulator-semiconductor) capacitor built with SiO_2 dielectric between a polysilicon gate and highly doped substrate, placed beside the access transistor.

To increase the effective area of the capacitor, the shape of the cell changed from planar to a progressive increase of aspect ratios, to distribute the cell capacitor area along the vertical direction instead of the horizontal one. So, the capac-

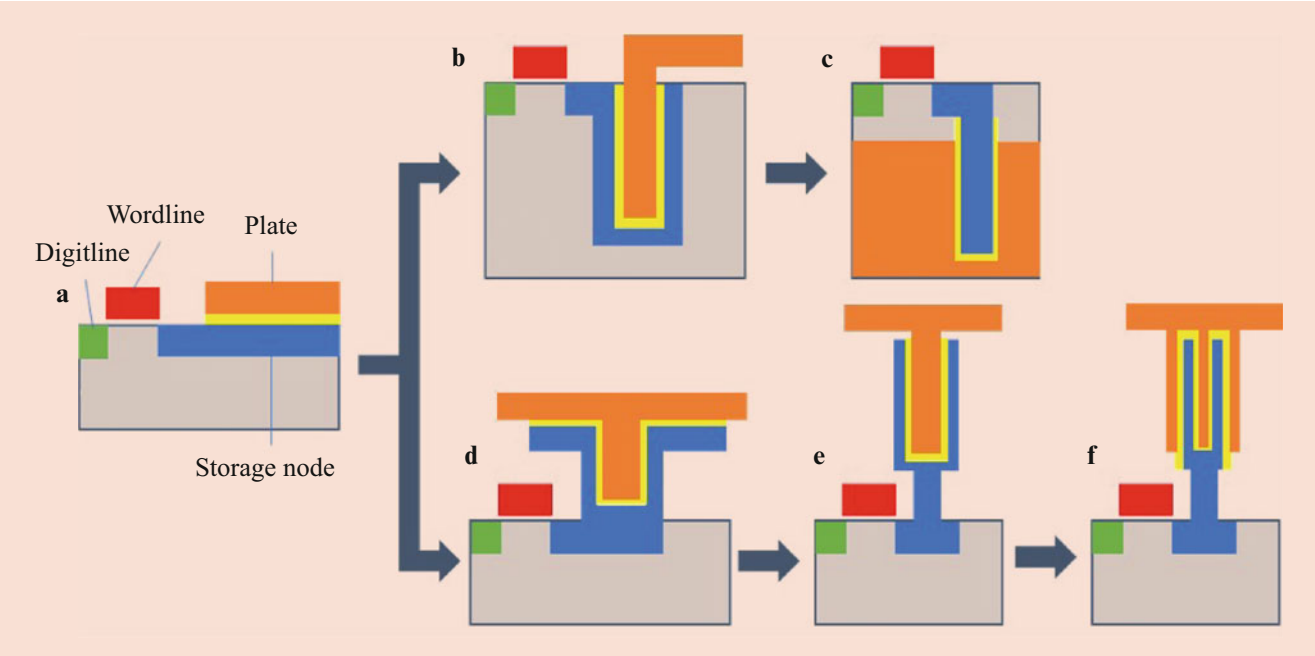

Fig. 2.14 Evolution of DRAM cell capacitor, from planar device (**a**) to 3D integrated device in the substrate like trench capacitor (**b**) and substrate-plate capacitor (**c**) or over the access device like stack capacitor (**d**), container cylindrical capacitor (**e**), and container dual-sided cylindrical capacitors (**f**)

itor, once integrated directly over silicon surface, then moved below the substrate or on top of it, as shown in Fig. 2.14. More examples of capacitor solutions for high-density DRAM can be found in literature, in references [18, 19].

The state of the art of the DRAM technology today is a cell with a tall cylindrical capacitor, called container, stacked over the silicon surface like in Fig. 2.14e. In the last 15 years, the diameter of the container decreased from 150 nm to 20 nm, and the aspect ratio of the container, that is, the ratio of its height to its diameter, grew from 10 to 35, challenging not only lithography but all the process technologies and process controls: etch, cleaning, thin metal, and dielectric film depositions [20]. To increase the capacitance of each cell without increasing too much the aspect ratio of the container, most advanced array uses dual-sided capacitors, like in Fig. 2.14f.

Starting from SiO_2 SIS, the technology evolved using MIM (metal-insulator-metal) and introducing insulators with increased dielectric constant: $Hf2O_3$, Al_2O_3, and ZrO_2. The dielectric in the capacitor is today composed by a thin ZAZ (ZrO_2-Al_2O_3-ZrO_2) dielectric between TiN electrodes [21], whose dielectric constant is more than 10 times higher than the one of SiO_2 and that guarantee a limited leakage. Metal and dielectric films are deposited in the container using atomic layer deposition technologies to obtain very uniform characteristics in structures with such high aspect ratios.

2.9 DRAM Access Transistor Scaling

DRAM access transistor needs to have a low off current to reduce charge dissipation from the cell; it needs to drive at least 1uA on current to charge the capacitor in few ns (current requirement does not change with technology node, since cell capacitance does not scale) and needs to be integrated in the cell available in an effective way, considering the array organization.

Up to ~100 nm technology node, the access transistors were built as planar devices, with improvement in the engineering of the junction to reduce short-channel effects. In the following nodes, the reduction of the length of the transistors was not achievable with a limited Ioff, so the device has been progressively recessed into the Si substrate, as in Fig. 2.15, creating a U-shaped channel whose length is higher than the physical size of the gate and introducing the so-called RAD (recessed access device) technology [22]. Then, to improve channel control and wordline resistance, metal gate substituted conventional polysilicon gate.

Today the state of the art of DRAM technology in a 6F2 cell is based on a BRAD access transistor (buried-recessed access device), where the whole metal gate is recessed below the silicon surface and is completely isolated from the surface, to give space to the contacts for the digitlines and for the cell capacitors. Wordlines are in contact with the surface

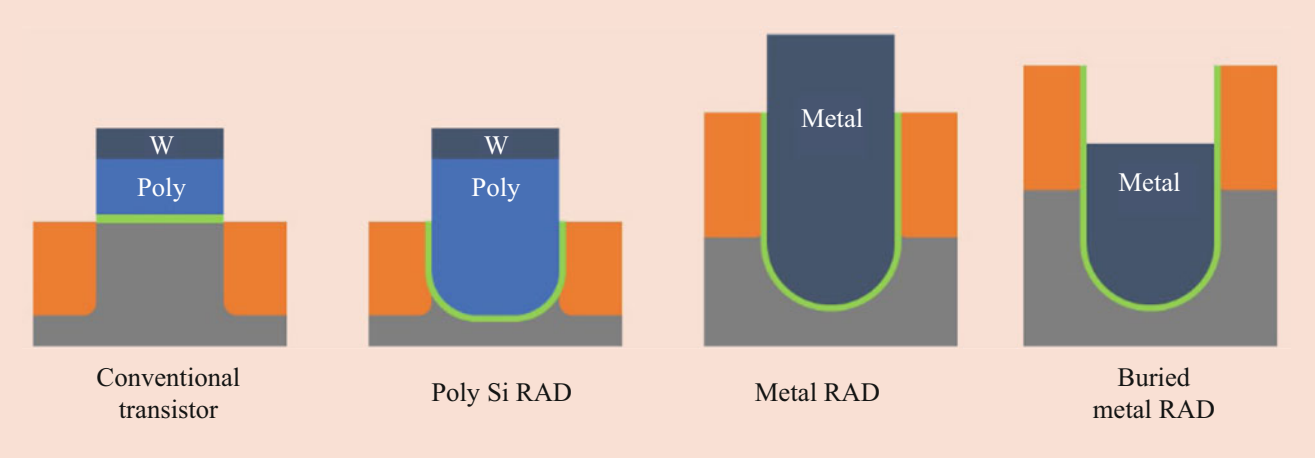

Fig. 2.15 Access transistor scaling; in the buried metal, RAD gate is completely recessed and the surface of the wafer is used for cell contacts

of the silicon and with the standard periphery just at the edge of the array.

2.10 DRAM Product Evolution

In parallel with technology evolution, also DRAM product design evolved to increase memory density, improve performances, and reduce power.

The first-generation DRAM worked in asynchronous mode, but in 1992 the first SDRAM device (synchronous DRAM) was presented, which has the advantage of accepting sequences of commands in a pipeline before the completion of running commands and the possibility of using contemporaneously many different memory blocks of the same chip. All DRAM today are SDRAM.

At single cell level, the performances of DRAM technology did not improve much in the last years: the latency is approximately constant, in the range of few tens of nanoseconds, limited by array resistances and DRAM capacitor. The most relevant improvement in DRAM chip performances has been obtained increasing the bandwidth, with wide data paths and internal pipelining.

From 2000, the new concept of DDR SDRAM (double data rate SDRAM) became a standard in the market: with the same clock frequency, the bandwidth of a DDR memory is doubled with respect to a std. SDRAM because data are transferred both on the rising and the falling edges of the clock signal, thanks to a strict control of the internal timings of the device.

From the introduction of DDR devices, the evolution of the following DRAM generations has been in terms of clock frequency and operating voltage, reaching a transfer rate of ~20 GB/s in DDR4 (Table 2.4).

Other architectural solutions to increase performances are the increase of I/O count and the 3D die stacking with TSV (through silicon vias) interconnects [23] and/or interposers: HBM (high bandwidth memory) [24] and HBC (hybrid memory cube) [25] are two solutions in the market, providing improved bandwidth for graphical and network applications (see Fig. 2.16).

2.11 Nonvolatile Memory: The Flash Memories

In 1967 D. Khang and S.M. Sze at Bell Laboratories proposed the concept of floating gate MOS transistor [26] that paved the way for one of the most successful solid-state integrated electronic device based on charge storage: the flash memory. Capitalizing this concept, Intel developed in 1971 a 2048-bit user-erasable EPROM memory (erasable programmable read-only memory) that could be reused multiple times by erasing the pattern with ultraviolet light [27]. Generations of UV EPROMs with multimillion bits of storage from Intel and others found wide application for storing and modifying program codes as firmware in microprocessor-based system designs.

Few years later, Eli Harari, working at Hughes Microelectronics from 1976 to 1978, demonstrated that a thin oxide floating gate could be an electrically erasable PROM (EEPROM), thus eliminating the need for external UV erasure [28]. George Perlegos employed the thin oxide technique for Intel's first EEPROM in 1978. A couple of years later, in 1980, Fujio Masuoka at Toshiba modified the EEPROM architecture to increase the speed of programming, appropriately naming it "flash" [29]. Professor Fujio Masuoka's ideas allowed overcoming the electrical and architectural limita-

Table 2.4 DRAM generations

DDR SDRAM standard	Internal rate (MHz)	Bus clock (MHz)	Data rate (MT/s)	Transfer rate (GB/s)	Voltage (V)
SDRAM	100–166	100–166	100–166	0.8–1.3	3.3
DDR	133–200	133–200	266–400	2.1–3.2	2.5
DDR2	133–200	266–400	533–800	4.2–6.4	1.8
DDR3	133–200	533–800	1066–1600	8.5–14.9	1.35/1.5
DDR4	133–200	1066–1600	2133–3200	17–21.3	1.2

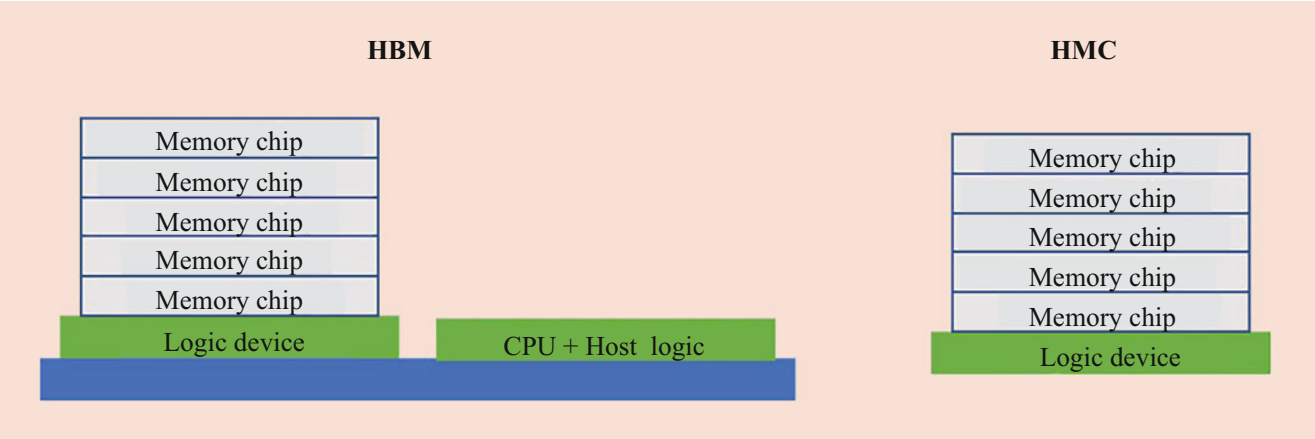

Fig. 2.16 HBM and HMC with stacked DRAM memory chips

tions of the early implementations of the charge storage-based memories such as EPROM or EEPROM by means of a simple memory cell transistor (1T = 1 cell) with particular array arrangements in order to allow parallel operations over a large group of cells and achieve higher array efficiency. Masuoka's research group presented the cell matrix architecture called NOR flash in 1984 [30] and then, in 1987, a second cell matrix architecture called NAND flash [31] that several years later would have been the fundamental technology block for USB flash memory stick and solid-state disks (SSD). Toshiba introduced its commercial flash products in 1987 followed by Intel in 1988. From then on, flash memory has found widespread use in such personal device applications as mobile phones, cameras, and GPS navigation systems.

Other matrix and architectural variations have been proposed (see Table 2.5); however, the original NOR and NAND flash remained the dominant solutions, and today NAND flash is the industrial standard for widely used solid-state storage systems, for instance, in SSDs and SD cards.

In the last 30 years, driven by the CMOS scaling roadmap, flash memory devices experienced a spectacular scaling, and nowadays, thanks to the transition from planar to the 3D integration, a single monolithic chip of NAND flash could reach logical density above 500 Gb/cm^2 [32] with a total memory density of 1 Tb = 128 GB [33].

Even if the technological challenges necessary for further density increase are huge, this scaling path is expected to continue since the global market for flash is growing with impressive CAGR (compounded average growth rate), boosted by the hunger of memories in more and more pervasive technologies such as smartphones, cloud computing, and IoT.

2.12 Floating Gate MOSFET Devices

A flash cell is basically a MOS transistor with the addition of a floating conductive electrode sandwiched between the channel and the gate node. Being the added element to the simpler MOSFET structure a conductive layer completely surrounded by dielectrics, it is coherently called floating gate (FG).

The device physics describing the FG MOS transistor can be therefore obtained from the conventional MOS transistor equations by replacing the MOS gate voltage with the FG voltage and transforming the device parameters, such as threshold voltage V_T and the conductivity factor β to values measured with respect to the control gate. In such a device, the gate node, above the FG, allows controlling the electrical behavior of the "transistor," but through the capacitive coupling with the FG node [34].

The gate of the FG MOS device is thus named control gate (CG), while the FG acts as storing electrode in the cell structure, being electrically isolated. In fact, the charge injected and stored in the FG modulates the "apparent" threshold voltage (i.e., the V_T seen from the CG) of the cell transistor. Figure 2.17 sketches the equivalent electrical model of the floating gate (FG) MOSFET device that can be useful for describing its operating principle. Being C_{FG}, C_S,

Table 2.5 Flash memory array architectures: in bold the market dominant solutions

Array architectures								
Cells in series		Cells in parallel						
NAND		AND	Virtual ground			Common ground		
Planar	**Vertical (3D)**		AMG (Alternate metal ground)	NROM	Triple poly split gate	DiNOR (Divided bitline NOR)	EEPROM	**Standard NOR**

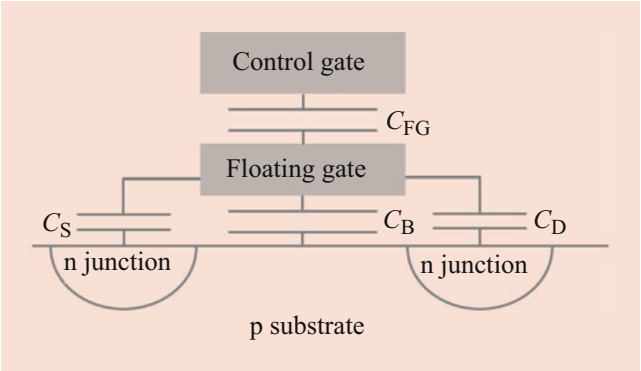

Fig. 2.17 Capacitive model of FG MOSFET

C_D, and C_B the capacitances between the FG and the control gate, source, drain, and substrate regions, respectively, the potential of the FG due to capacitive coupling can be written as:

$$V_{FG} = \frac{C_{FG}}{C_{TOT}} \cdot V_{CG} + \frac{C_S}{C_{TOT}} \cdot V_S + \frac{C_D}{C_{TOT}} \cdot V_D + \frac{C_B}{C_{TOT}} \cdot V_B + \frac{Q_{FG}}{C_{TOT}} \tag{2.1}$$

where:

$$C_{TOT} = C_{FG} + C_S + C_D + C_B \tag{2.2}$$

The capacitive ratio C_{FG}/C_{TOT} is often called α_G and represents the coupling factor between the control gate and the floating gate. α_S, α_D, and α_B are, consequently, the other coupling ratios.

Assuming both source and body at 0 V, Eq. 2.1 can be simplified as:

$$V_{FG} = \alpha_G \cdot V_{CG} + \alpha_D \cdot V_D + \frac{Q_{FG}}{C_{TOT}} \tag{2.3}$$

Then, defining V_T^{FG} as the potential that must be applied to FG to reach the inversion of the surface population (MOS threshold definition), the potential to be applied to the control gate to realize this condition, V_T^{CG}, can be found by using Eq. 2.3 that leads to:

$$V_T^{CG} = \frac{1}{\alpha_G} \cdot V_T^{FG} - \frac{Q_{FG}}{C_{FG}} \tag{2.4}$$

Since V_T^{FG}, α_G, and C_{FG} are in a good approximation constant, for a given technology, depending only from constructional parameters, then Eq. 2.4 ties the dependence of FG MOS threshold with the amount of charge stored in the floating gate.

2.13 Flash Memory MOSFET Devices

The description of the floating gate MOS device leads straightforwardly to the FG memory cell or flash memory. We just saw that under certain conditions, the threshold voltage V_T of a MOS transistor depends linearly from the amount of charge stored in the gate capacitor system. For an n-channel enrichment MOSFET, the general form of this dependence, from Eq. 2.4, can be written as:

$$V_T^{CG} = A - \frac{Q_{FG}}{C_{FG}} \tag{2.5}$$

where A is a constant depending on constructional parameters of the transistor and C_{FG} is the capacitance of gate system [34]. Thus, negative charge increases the threshold, while positive charge in the FG decreases it. The digitalization of this dependence in two or more discrete threshold states is the base of flash memories.

General convention assigns logical state 1 at non-charged state (erased cell) and logical state 0 at the charged state (programmed cell), as in Fig. 2.18.

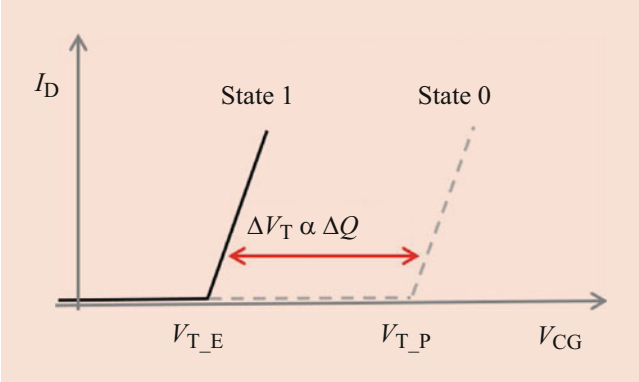

Fig. 2.18 Shift of ideal MOS I_D-V_G transcharacteristic due to negative charge injection in the gate/substrate capacitor system

Standard flash cells can displace the threshold over several volts; however, the size of the working window is limited by fundamental phenomena, mainly by the maximum electric field that can be sustained by the dielectric layers.

Considering the intrinsic variability of the threshold voltages over a large collection of cells, the minimum separation between logical states (also known as read window budget, RWB) is dictated by the width of the statistical distributions of the thresholds of the erased and programmed cells. The precise control of the placement of the V_T of the cell for both state 0 and state 1 is achieved thanks to engineered program and erase algorithms [35]. These programming algorithms tighten the width of threshold distributions and enable the placement of additional V_T distributions in between the erased and the programmed cell, thus offering the opportunity to store more than one logical bit in one physical cell.

In Fig. 2.19, an ideal representation of the threshold distributions over a large cell collection (block of cells) for single bit technology (SLC = single-level cell) and 2-bits technology (MLC = multilevel cell) is reported.

The actual state of the art of multibit technology features up to 4 bits per cells in the most advanced NAND flash products [36, 37], which means that 16 different distributions are placed in the V_T accessible range.

The overall separation of logical states represented by the RWB quantity measures the reliability of the data storage and becomes more and more critical with the increase of the number of distributions (number of bits per cell), considering the already mentioned constraint to not enlarge over a certain limit the total program to erase window (max threshold displacement).

In current flash memory technologies, especially NAND flash, in which the reading operation is naturally performed in parallel over a large cell collection, the decoding of logical states relies on error correction code (ECC) techniques to overcome RWB and reliability limitations [38].

For NAND flash, the large dimension of the page, which is the portion of array read in parallel, allows to use many bits of ECC without significative penalties. Instead, random read access and single bit granularity in NOR flash are preventing the use of many ECC bits due to an unacceptable degradation of random read performances.

2.14 Charge Storage Solutions

In flash memories, the "memory effect," thus the digitalization of threshold states, is achieved by adding a net amount of electrical charge in the floating gate. In addition, the capability to retain this stored charge for a long time (years at max operative temperature) even when the gate bias is not present, makes this memory device nonvolatile.

Indeed, the floating gate technology is not the unique solution to achieve a charge storage element above the channel of a MOS transistor. Two solutions are widely adopted as industrial standards to store charge above the channel able to modulate the threshold of the transistor:

1. Adding a conductive electrode in between control gate and channel, creating the FG technology extensively described in the previous paragraph. To enhance charge retention and the device performance, the insulation structure between floating and control gates is often made by stacking multiple dielectric layers, alternating silicon oxide (O) and silicon nitride (N), giving rise to the ONO dielectric.
2. Embedding materials and interfaces, inherently dielectrics, able to trap charges, into the gate oxide of the MOS transistor. A common solution for this is the use of silicon nitride-based films: for this reason, this kind of devices is often called SONOS (silicon-oxide-nitride-oxide-silicon) or MONOS (where M stands for metal) [39].

Figure 2.20a, b show the ideal cross sections of a generic SONOS and generic FG devices (n-MOS based) with the typical stack and industry standard materials.

From the physical point of view, the capability to retain a net charge is related to the electronic bands structure of the stack built by metals, dielectrics, and semiconductor materials.

In FG cell, the conduction band offset between the conductive polysilicon electrode and the surrounding silicon oxide-based materials is 3.1 eV at room temperature, approximately. This is the energy barrier preventing that free electrons, stored in the FG, are emitted in the conduction band of surrounding material and thus lost toward substrate or control gate.

The charge trap-based cell, like the SONOS cell, has more complex retention mechanism: it relies into the potential

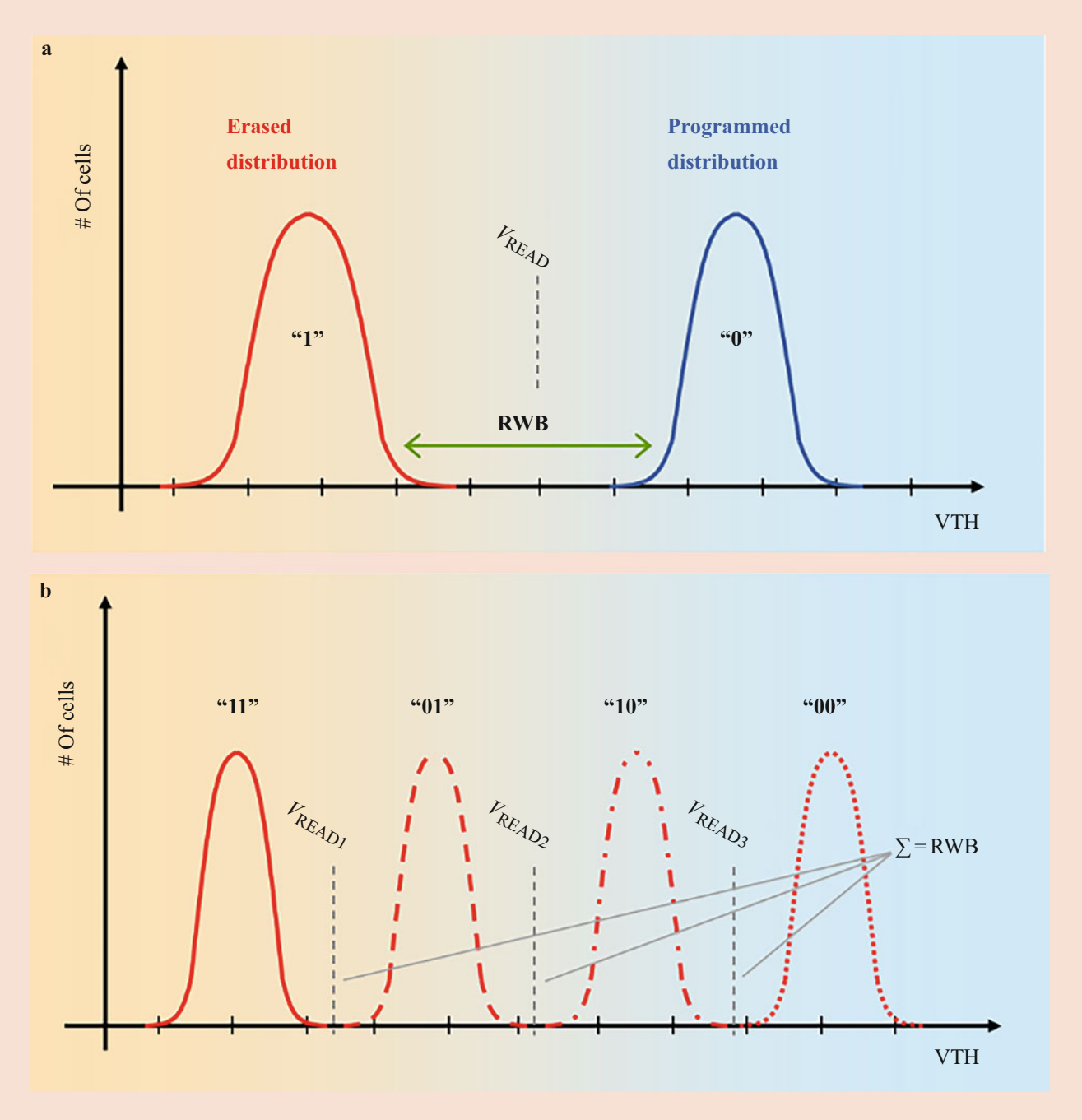

Fig. 2.19 (**a**) Ideal threshold voltage distributions for SLC and (**b**) MLC technologies

wells where the charge is stored in localized states into the trapping material, generally defects of crystalline lattice. This potential well can be ideally described as the depth of the energetic level of the trap in the forbidden gap of the dielectric trapping material. For commonly used silicon nitride-based material, this depth lies in the $1 \div 2$ eV energy range. However, the emission of a trapped charge toward external electrodes is a multistep phenomenon (Poole-Frenkel and band to band emissions), whose activation energy can differ from the energetic depth of trap level.

2.15 Charge Injection/Extraction Mechanisms: Programming/Erase Operations

Once we have in place the charge storage system inside the gate to substrate capacitor (either charge trap or FG systems), then the problem is to change the charge in a tightly controlled way, that is, let the charge flow through a dielectric: it could be a single layer or a composite stack

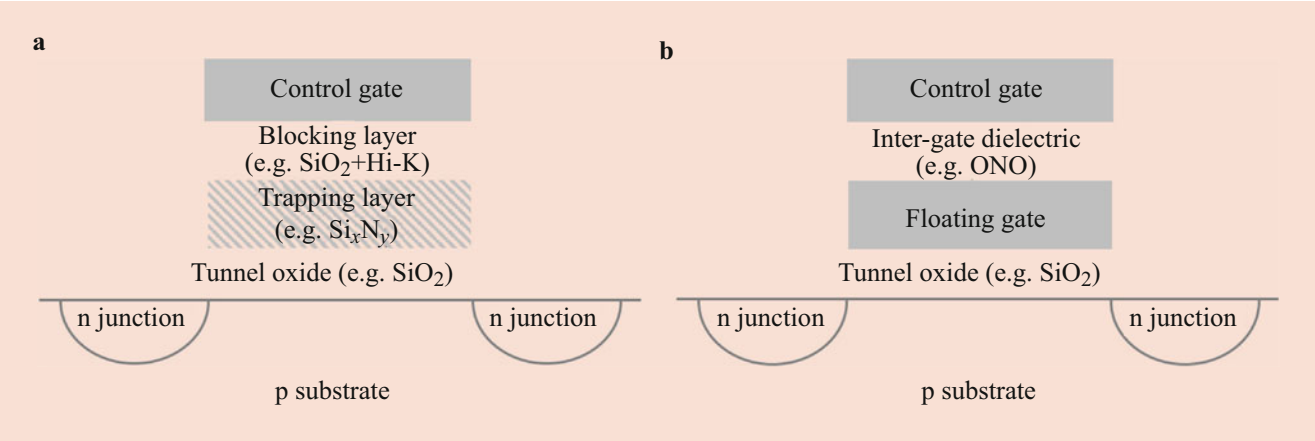

Fig. 2.20 Ideal cross sections of (**a**) a generic SONOS and (**b**) a generic FG device (n-MOS based)

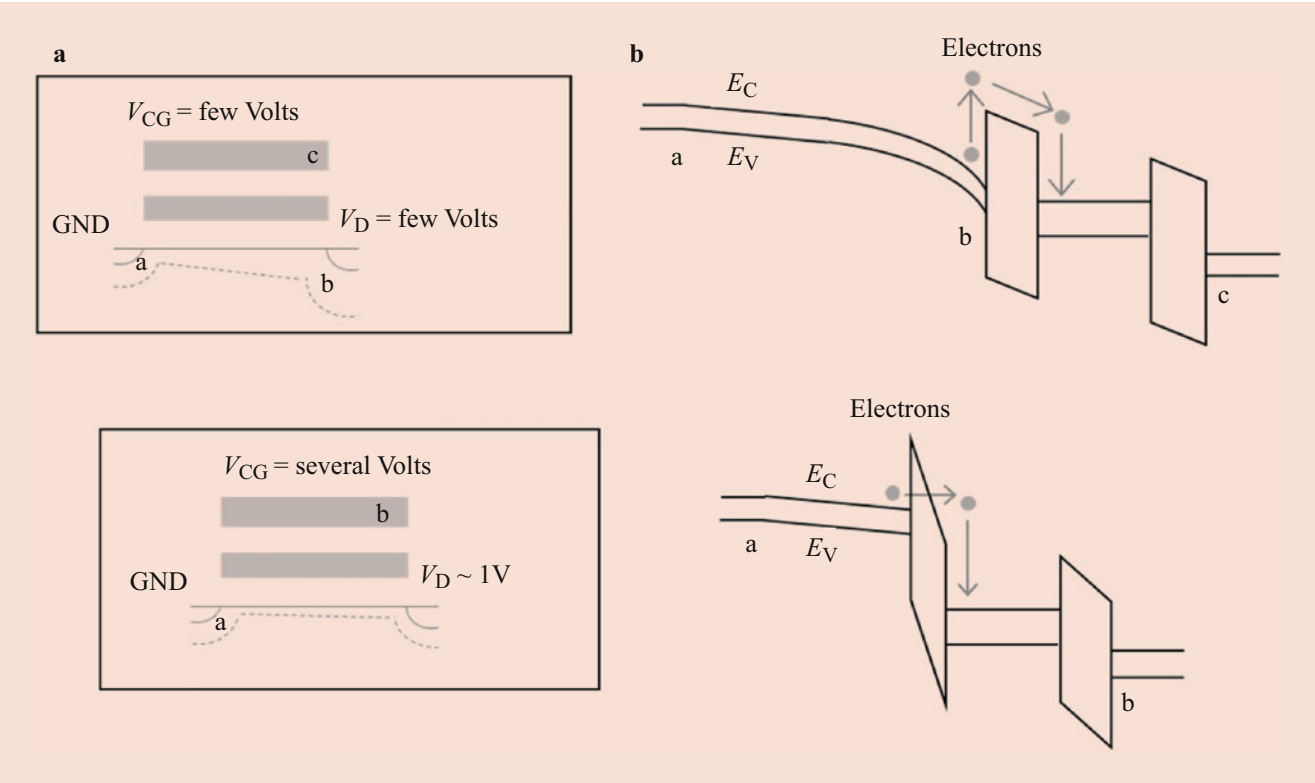

Fig. 2.21 (**a**) Biasing scheme and schematic energy band diagram related with the electron injection processes: by hot-carrier and by (**b**) Fowler-Nordheim tunneling

when the so-called band engineered (BE-tunnel) solutions are required [40].

Generally flash memories use two alternative mechanisms to make this charge transfer possible:

1. Hot-carrier emission and injection: they could be electrons or holes.
2. Quantum tunneling across a triangular energy barrier, also known as Fowler-Nordheim tunneling: it could be either for electrons injection or electrons extraction (flash memory cell is probably the most common man-made object relying on quantum mechanical effect: a real triumph of modern physics).

Figure 2.21 shows schematically the band energy diagram of a generic FG n-channel MOSFET system promoting an electron injection in the FG by using hot-carrier or Fowler-Nordheim tunneling.

Both mechanisms are strongly modulated by geometrical and constructional parameters of the device, such as doping, material features, thicknesses, and cell shape. It is important to notice that high energy carriers generated in both mechanisms are also source of spurious effects potentially leading to device degradation and limiting the total number of program and erase cycles that a flash memory device can experience in its lifetime.

NOR flash relies on hot-carrier injection for programming phase, while tunneling is used for erasing. NAND flash uses tunneling either for programming and erasing phases.

2.16 NOR Flash Array, Operations, and Reliability Aspects

NOR flash memory cells (generally FG MOS transistors) are connected as in Fig. 2.22 to form a memory array.

In this structure, every cell shares its source and drain contact (bitline – BL) with another cell whose control gates are connected to a different terminal (called wordline – WL). The NOR array can provide random access both for read and write operation.

Read operation is executed sensing the I_{DS} of cell (bitline current) and comparing it with a reference current. From a logic perspective, the array resembles a NOR gate where the inputs are the wordlines of cells connected in parallel to the BL. With this configuration, when one of the WL is brought high, the corresponding cell acts to pull the output BL low, analogously to the logical operation of a NOR gate.

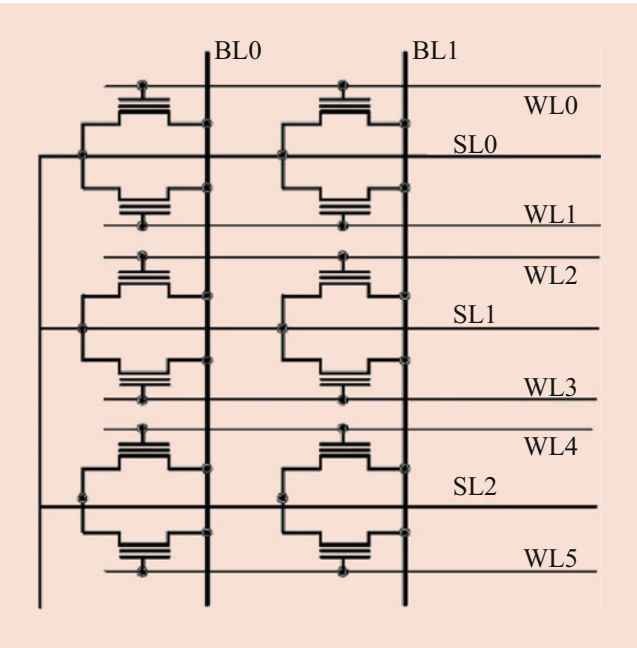

Fig. 2.22 NOR flash array section of 12 cells: 2 bitlines and 6 wordlines

In NOR flash cell, the programming or writing operation is performed by using hot electrons injection: these hot-carriers are generated by a high drain to source voltage (~5 V) and the increased probability for "lucky" electrons injection in the floating gate is granted by a vertical electrical field generated by an appropriate gate to source voltage. This mechanism is quite inefficient because of the large amount of I_{DS} required to generate a high enough number of "lucky" electrons. To avoid excessive power consumption, the maximum program parallelism is low: only few cells can be programmed at the same time.

The erase operation employs the Fowler-Nordheim (FN) tunnel effect by applying a high electric field across the cell stack (gate to source in the early version of the NOR cell, then gate to body in the more recent versions where triple well architecture is available). This high electric field bends the energy band structure enhancing the probability of electrons to tunnel through the oxide, thus extracting them from the FG. Being FN current very low, the erase operation can be performed in parallel over large sections of memory array (block erase) overcoming the intrinsic slowness of erase operation.

Figure 2.23 shows the TEM cross sections of industry standard NOR cells along with two orthogonal directions: (a) parallel to the WL; (b) parallel to the BL.

In particular, Fig. 2.23a shows two cells with shared control gates, but separate floating gates; while Fig. 2.23b shows two cells with shared bitline and drain contact but separate control and floating gates.

For NOR flash products, the data retention must guarantee up to 10 years at 65–85 °C and the dominant wear out mechanism for charge loss and gain occurs through electrons trapping in the tunnel oxide of the cell. This results in leakage through the insulator and the dielectric damage primarily induced by the ERASE/WRITE operations of a cell. Therefore, the maximum number of program and erase (P/E) operations is limited: typically, up to ~100 K cycles of program and erase.

2.16.1 NOR Flash Applications and Roadmap

NOR flash memory is used as primary storage for firmware such as the BIOS for PCs or set top box systems, because of the supported execute in place (XIP) capability granted by the random access for read and write operations.

In the early stage of mobile phones and digital cameras era, NOR flash has been used also as primary mass memory device in removable media (compact flash, MMC); however, the limitation of scalability and the high process cost due to

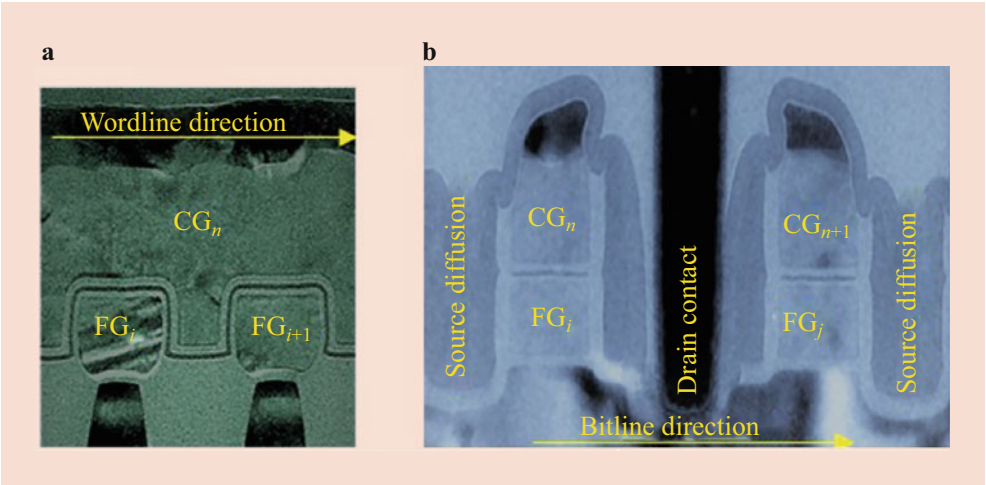

Fig. 2.23 NOR cell TEM sections: along WL direction (**a**) and BL direction (**b**)

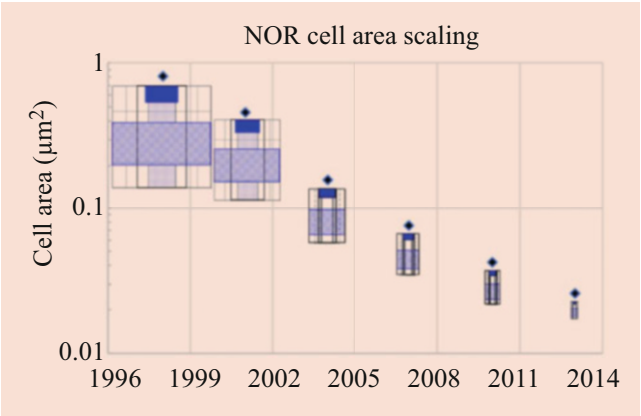

Fig. 2.24 Cell area reduction over 20-year roadmap of NOR flash cell

the need to integrate a drain contact (BL contact) every two cells prevented the diffusion of NOR flash in favor of NAND flash, which offers significative advantages in density and cost per bit as it will be illustrated in the following.

The technology effort for NOR cell scaling and thus for density increase is shown in Fig. 2.24; it practically ended after the first decade of 2000 with the introduction of the 45 nm node cell and 2 bits per cell (MLC) technology, but the market for NOR flash devices is in any case still growing driven by industrial, IoT, and automotive applications.

2.17 NAND Flash Array, Operations, and Reliability Aspects

In the quest for cheaper solid-state mass memory solutions, NAND flash became the solution of choice among all the invented array architectures and for all the high-volume memory manufacturers, thanks to the fact that NAND flash has the highest array efficiency and it can consequently reach density of memory not achievable with other flash architecture or by any other nonvolatile solid-state technologies.

In the array of NAND flash, the cells, which can be floating gate or charge trap-based MOS, are connected in series to form elements called strings as in Fig. 2.25. The number of cells tied in a single string varies according with the technology: e.g., up to 128 cells as for ultimate planar technologies. The string is then connected to the common source and to a single bitline (BL) by selector devices. The drain selector (DSL) connects the string to the bitline, while the source selector (SSL) connects the string to the common source. The selectors are generally MOS transistors or additional cells, not used to store data, integrated in the string with a similar technology process used for the cell formation.

Putting a large number of cells in series helps in diluting the overhead to array efficiency due to the presence of selector devices, but it must deal with electrical drawbacks, such as increased disturbs and higher series resistance, in particular for 3D NAND where the cell substrate is polycrystalline silicon.

In planar NAND technologies, the cell area approaches the ideal $4\lambda^2$, where λ is the minimum half pitch definable by lithography by means of advanced multiple patterning technologies. The transition to 3D architectures gives the possibility to move beyond this limit by stacking more cells on the same footprint and then to effectively decouple the density increase roadmap from the lithography node and patterning capability. In simple words, the transition to 3D architecture occurred arranging in vertical the NAND string and then moving out of the plane the integration Scheme [41]. 3D NAND architectures featuring this vertical channel and horizontal WLs are today the industry standard, and their simplified basic scheme is sketched in Fig. 2.26 [42–44].

NAND array is organized in pages, blocks, and planes. The page is the collection of cells sharing the same wordline

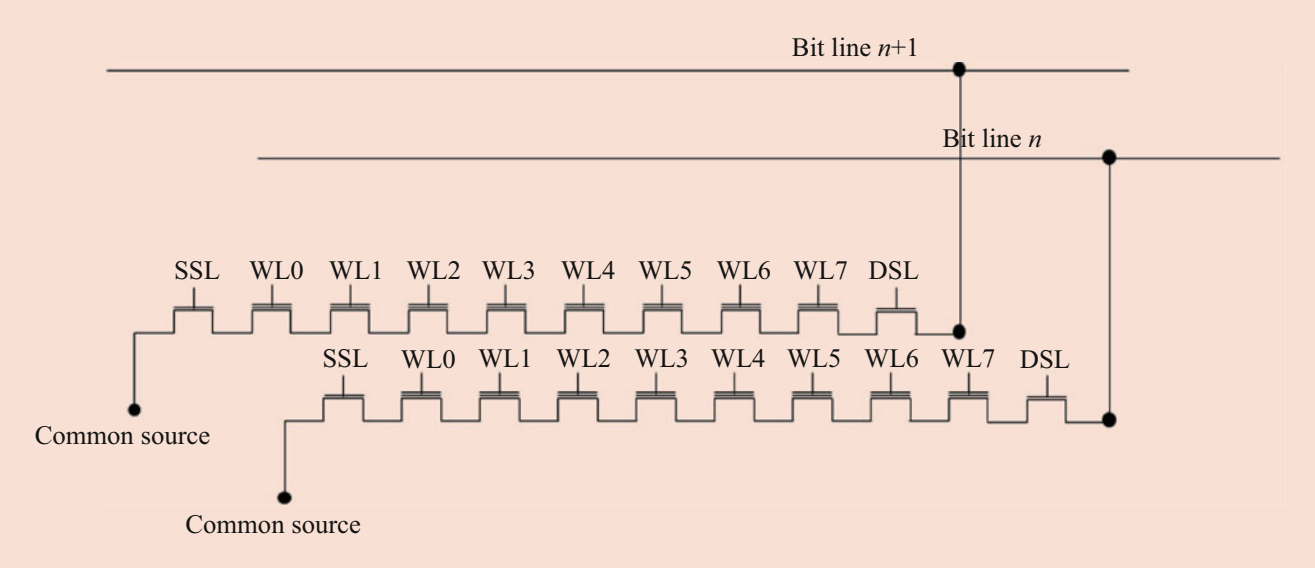

Fig. 2.25 Planar NAND array schematic showing two strings (BLn and BLn + 1) with 8 WLs

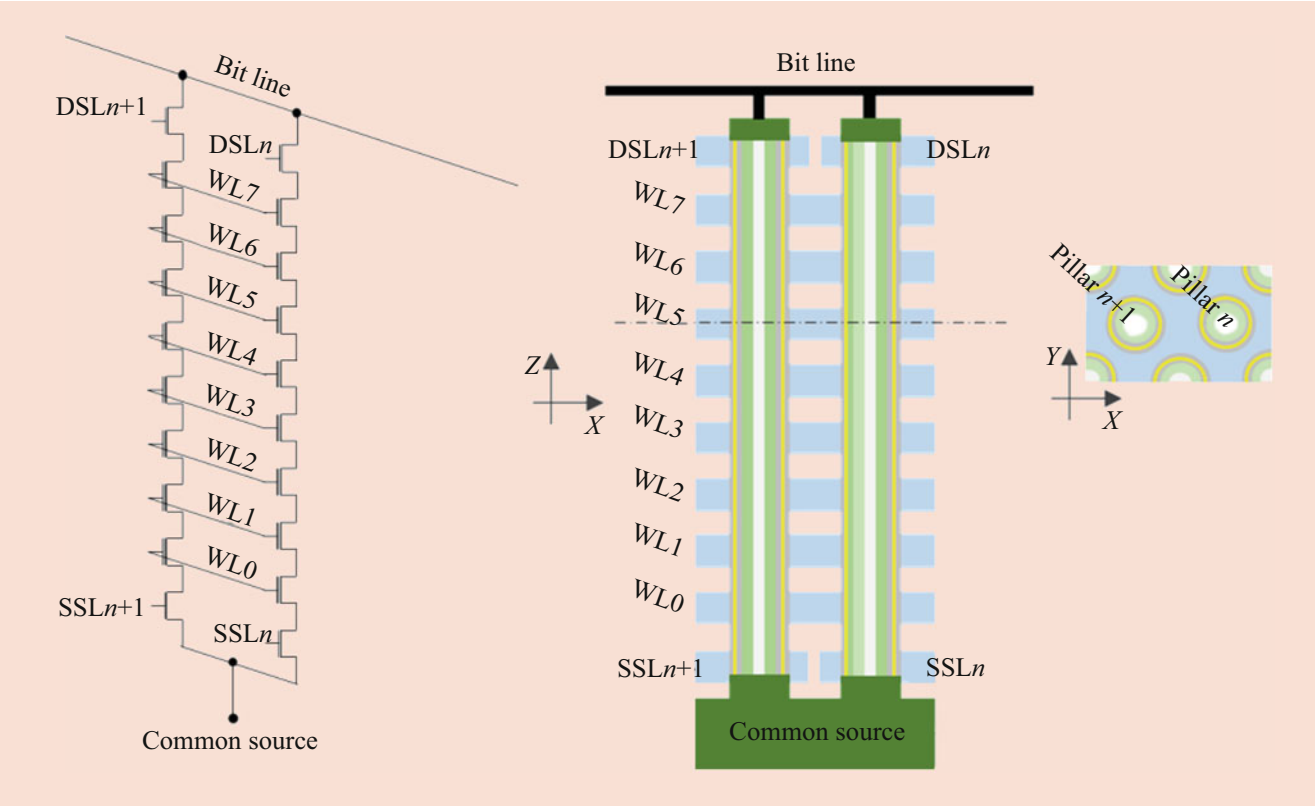

Fig. 2.26 3D NAND array schematic and pictorial sections showing two strings/pillars (vertical channel) and eight horizontal WLs

(WL) across a number of bitlines, spanning a dimension from 2 KB to 16 KB. The page defines the array section which can be read and programmed in parallel. For parallel reading, a large bank of sense amplifiers (called page buffer) is connected to the bitline system. Sense amplifier is a complex circuit mixing analog and digital parts.

During the read operation, by turning on both DSL and SSL, the current can flow through the string to the BL. Sense amplifier senses such a current, discriminating the threshold state of addressed cell identified by its WL (page index), and it digitalizes the information by storing it in one or, in case of multibit technology, more register latches which form

the data cache. The remaining cells belonging to the same string are turned on, regardless their threshold state, with a sufficiently high gate bias called pass voltage. Once the data from the page are stored in the data cache, then the output is obtained by serializing the page into data path to I/Os (typically by bytes).

The products of page size by the number of cells in NAND string define an array section called block. It is a collection of pages, and for a planar NAND, it has a physical density up to 16 Mb, while in 3D NAND it is generally bigger, from 32 to 64 Mb, thanks to an additional level of decoding due to drain selector. Block is the smallest array section that can be erased.

NAND flash uses the tunneling effect (see Fig. 2.21) for both program and erase operation. To program a cell, its WL is brought to a high voltage (more than 20 V) while its channel is kept low by turning on the DSL and keeping the BL to ~0 V. For the other cells sharing the same WL but located in different strings, the programming operation is inhibited by putting their channels in floating condition: in this way, the floating channel is coupled with WL potential, thus limiting the electric field across tunnel oxide and preventing tunneling current.

As said before, the tunneling mechanism requires a very low current, and then it is ideal for the high parallelism required by NAND page operations.

However, the propagation into the array of high voltage necessary for effective tunneling is creating electrical constraints, power dissipation, and reliability concerns. The typical page programming time is a function of the number of bits per cell, and it can span between 200 μs (SLC) and 2 ms (QLC). The overall energy necessary to program a bit is again function of number of bits per cell, array architecture, and technology parameters: for a MLC planar technology, it could be around 1000 pJ/bit [45].

While for planar NAND, the cell structure is similar to what described in the general section (Fig. 2.20a, b), for industry standard 3D NAND, the cell has a cylindrical geometry being formed by the intersection of WL plane wrapping all around the polycrystalline silicon pillar acting as substrate (see Fig. 2.27).

2.18 NAND Flash Roadmap

NAND flash devices are today the cheapest solution for solid-state mass memory systems. They are widely used for solid-state drive and memory cards such as microSDs. Until 2013, all the commercial NAND flash have been made using planar architecture in which roadmap is dictated by the scaling of planar transistors: definition of active areas, definition of gate, and interconnections. Scaled planar NAND flash devices use immersion lithography and double patterning techniques such as SADP (self-aligned double patterning)

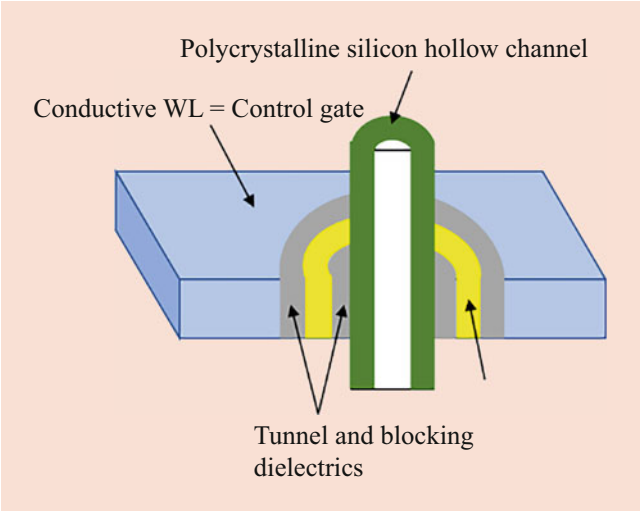

Fig. 2.27 Ideal semicircular cross section of the 3D NAND pillar and gate all around cell

to reach cell dimension well below 20 nm [46]. From 2013 the transition to 3D NAND flash architecture boosted the density to a new level. First industrial 3D NAND flash was fabricated by Samsung and featured 24 layers [47], but soon the transition to 32, 48, 64, and 96 layers happened [48–50]. Now, the race is going on and 128-layer technology has been announced by major industry players [51] while 176-layer outlook seems the next step [52]. TLC (triple-level cell) is the standard for 3D NAND; however, we have already seen makers able to deliver QLC devices at 64 layers [53]. Currently the highest density for a monolithic 3D NAND flash is 1 Tb, but this limit is expected to be outperformed soon [54].

2.19 Emerging Memories: An Insight on Phase-Change Memories

The previous two parts of the chapter have been dedicated to the main volatile and nonvolatile memory technologies nowadays present in a computer system. This section of the chapter will describe the phase-change memory (PCM) technology, classified as an emerging nonvolatile memory technology (see Fig. 2.28 reporting a map of emerging memories). Most of emerging memories are non-charge based, at variance with respect to the DRAM and flash concepts, previously discussed. In particular, ferroelectric memory (Fe-RAM) is based on the physical movement of atoms in response to an external field, which happens to be extremely fast, settling in about 1 ns. It is a random access memory similar, in construction, to DRAM but using a ferroelectric layer instead of a dielectric layer to achieve nonvolatility [55]. Floating-body RAM is one transistor memory cell used as a storage element, by modulating the threshold of the transistor

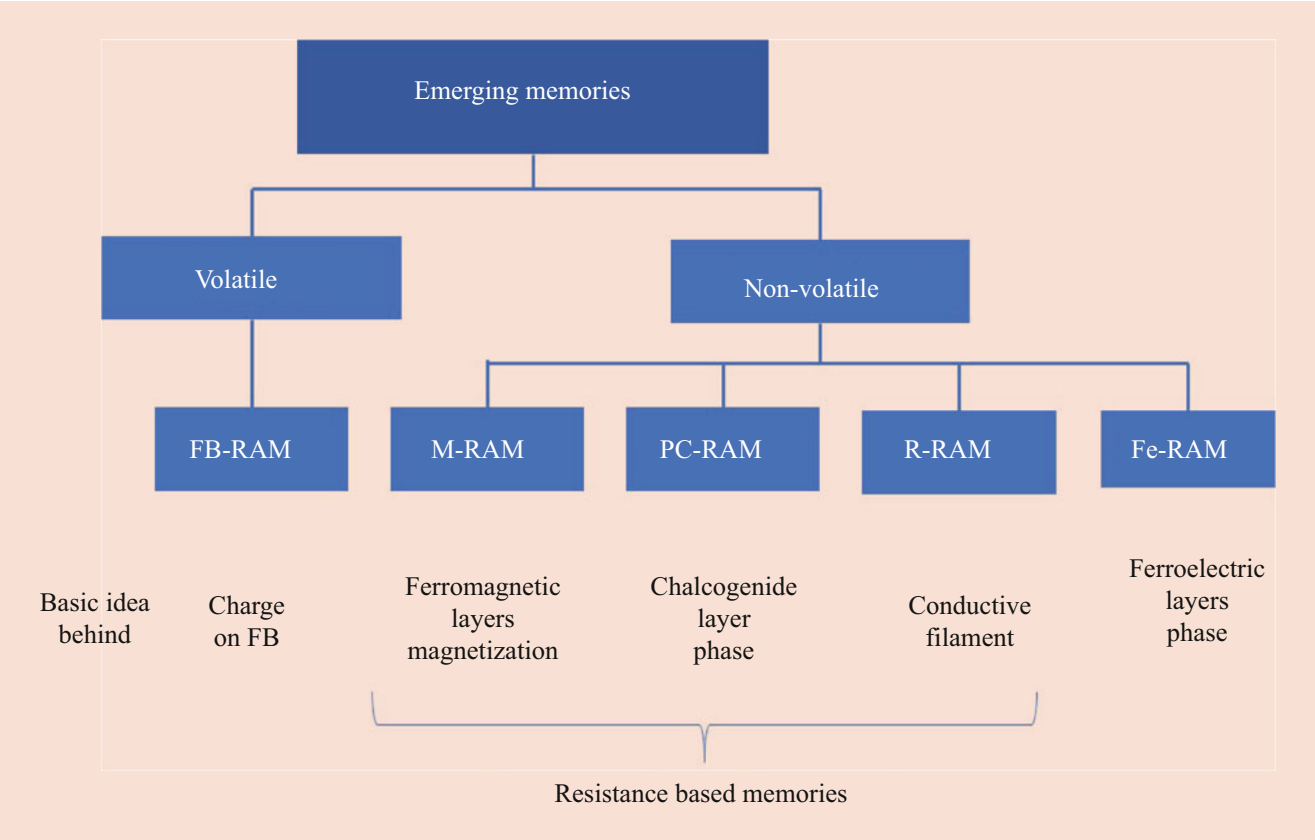

Fig. 2.28 Main proposals of emerging memories that can potentially complement the features of the DRAM and NAND previously described

via hole accumulation or depletion in the floating body region [56]. It was also proposed as potential candidate to replace the DRAM or even the 6T SRAM. The other proposed emerging memory concepts address the development of two-terminal devices that differentiate each other on the basis of the switching mechanism that controls the toggle between a high resistance state (HRS) and the low resistance state (LRS). The transition between the two states can be triggered by an electrical stimulus (i.e., voltage or current pulse). STT-MRAM relies on the parallel configuration (defining LRS) and anti-parallel configuration (HRS) of two ferromagnetic layers separated by a thin tunneling dielectric layer [57]; RRAM relies on the formation (LRS) and rupture (HRS) of conductive filaments within insulating layers sandwiched between two electrodes [58] (Chap ▶ 29).

PCM is the object of the present section. The physics at the basis of this technology and how the new physics might apply to build more efficient memory device will be described; at the same time, the opportunities and challenges to complement the previously described existing memories will be addressed.

The working principle of the PCM technology lies on the peculiar property of some chalcogenide alloys to reversibly toggle between the amorphous and the crystalline phase, thus the name phase change. The structural phase change also produces pronounced contrasts in the physical properties between the two phases. The optical contrast between the amorphous and crystalline phase makes these chalcogenide materials suitable for technological applications in the field of optical media and memories. The amorphous and crystalline phases also present a strong electric contrast: being the disordered amorphous network insulating, while the crystalline phase is conductive (Chap. ▶ 40). The abrupt resistivity change between the two phases (~3 orders of magnitude!) can be employed as the basis of electrically programmable and readable data storage. Hereto, the idea at the basis of the phase-change memory (PCM) is to *electrically* induce the phase transition of a chalcogenide-based thin film and to measure the device resistance as logic state of the cell. Since both states are stable, no energy is required to keep data stored, and PCM results in an inherently nonvolatile memory (NVM) technology. The best chalcogenide alloys for PCM applications belong to the class of GeSbTe compounds which follow a pseudo-binary composition (between GeTe and Sb_2Te_3, also including the GeTe and Sb_2Te_3 corners). Among them, the $Ge_2Sb_2Te_5$ (usually referred as GST) is the mostly used since it provides a good compromise between the speed of transformation from the disordered to the crystalline structure and the stability of the amorphous phase able to meet retention product requirements like 10 years at 85 °C.

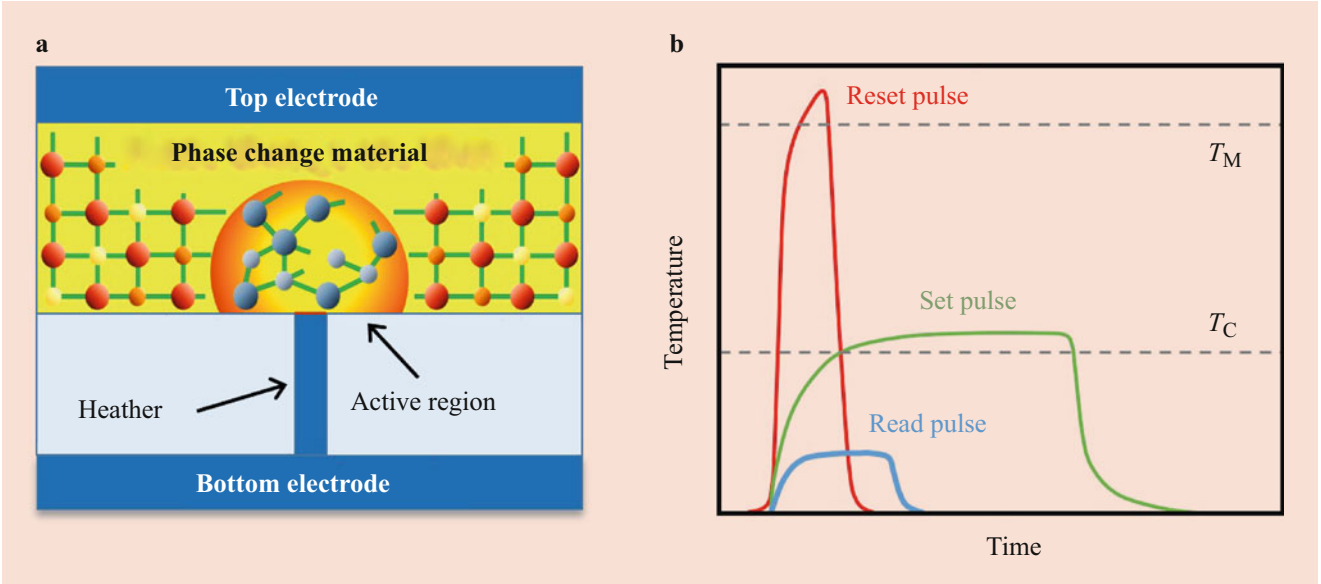

Fig. 2.29 (**a**) Sketch of the prototypical mushroom-like PCM cell where the current crowding through the small heater-phase-change material contact gives rise to the active area of the cell with mushroom boundary. (**b**) Temperature-time scheme of the pulses used to program the PCM cell in the reset and set states and to readout the state of the cell. Electrical pulses change the temperature in the active region of the cell, accordingly

The PCM cell architecture is essentially a resistor constituted by a thin film of chalcogenide material with a low-field resistance that changes by orders of magnitudes, depending on the phase state of the chalcogenide alloy in a possibly thinner layer than the total film thickness that is called active region of the cell. A prototypical architectural example of a PCM device is shown in Fig. 2.29a: it's called mushroom-type because of the shape of the active region coupled with the heater.

The switching between the two states of the active region is temperature activated. The glassy state of the material in the active region can crystallize when it reaches a critical temperature (T_c) and crystal nucleation and growth can occur (set operation). To bring the chalcogenide alloy back to the amorphous state (reset operation), the temperature must be increased above the melting point of hundreds of °C and then very quickly quenched down to prevent any ability of the glass to crystallize, leaving the cell in the amorphous state (Fig. 2.29b). The very small heater/phase-change contact area that characterizes this kind of PCM architecture is the key feature to develop a sufficient Joule heating effect to locally reach both the critical temperatures, T_c and T_M, thanks to the current crowding.

Figure 2.30 illustrates the electrical characteristics of the PCM cell. Depending on the chalcogenide material phase, the memory device features one of the two electrical characteristics depicted in Fig. 2.30a. The crystalline phase behaves as a resistor with a slope mainly dominated by the heater resistance itself. The amorphous phase shows an S-shaped negative differential resistance (SNDR) that starts from a high resistive off-state and collapses, with a decreased bias on the cell, into a high conductive on-state through the so-called threshold switching effect [59]. Figure 2.30b shows a typical programming curve of a PCM cell where the x-axis reports the programming current intensity of squared pulses of 100 ns duration and the *y*-axis the measured resistance as a function of the programming stimulus.

Both types of state transitions are shown in the figure. For the reset to set transition, the cell was always prepared in the reset state (correspondingly to $R \approx 1.5$ MΩ) prior to the application of the programming pulse. In this case, the programmed resistance steeply decreases for programming currents greater than 100 μA, due to the crystallization of amorphous chalcogenide film in the active region. The figure also shows the opposite (set-to-reset) transition, where the cell is prepared in the low-resistance crystalline state ($R \approx 3$ kΩ). Here, the cell resistance remains unchanged for moderately small programming currents and then abruptly increases for current values greater than 500 μA. This current value marks the chalcogenide melting temperature within the active region. In fact, rapid cooling of the melted chalcogenide along the falling edge of the program pulse results in a final amorphous phase, increasing the cell resistance. Note that the falling edge is a critical parameter in the set-to-reset transition: if the falling edge is not fast enough, the melted glass may re-crystallize leading to a final state with lower resistance. As already noticed, since both the crystalline and the amorphous state are stable, the two phases could be used to store binary information in a nonvolatile memory device, where the bit "1" corresponds to the conductive state and

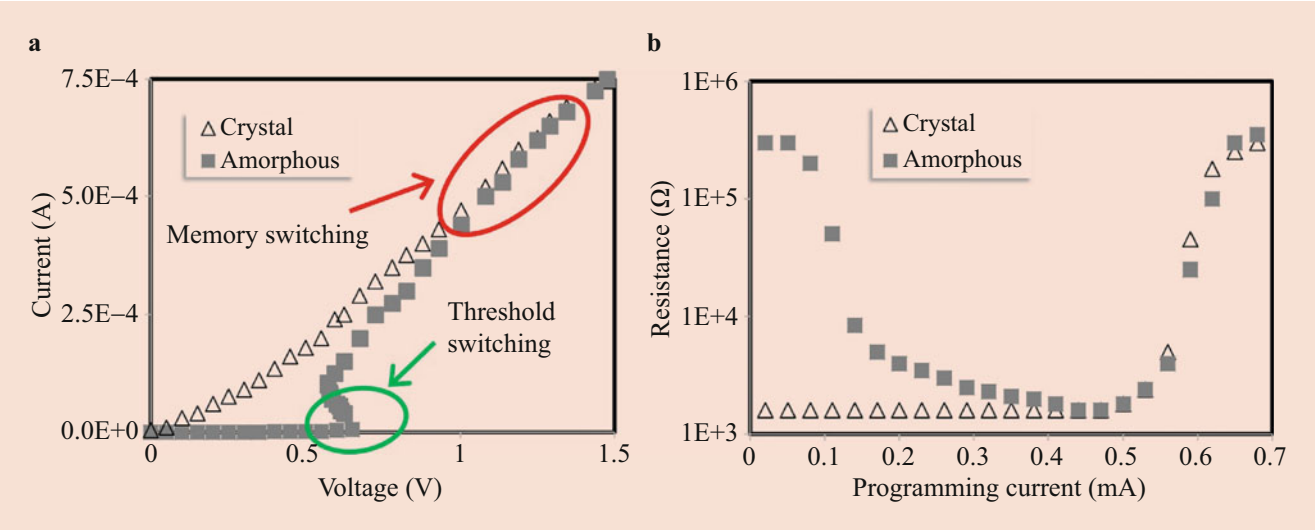

Fig. 2.30 (**a**) Current-voltage characteristics of the PCM cell with the chalcogenide alloy in the crystalline and amorphous phase and in (**b**) the R-I "U-shaped" programming curve of a PCM cell together with the R-I programming curve starting from the set state

the bit "0" to the insulating one. This electrically induced structural and electronic change has been thus named memory switching. It is worth noting that the threshold switching effect is required to get the memory switching mechanism but not vice versa. In fact, an amorphous chalcogenide has to be driven in a highly conductive electrical state through threshold switching to get the transition temperatures without enormous electrical fields [59, 60].

The minimization of the reset programming current, in addition to the power consumption control, addresses many performance implications enabling the PCM technology: the thermal cross-talk between adjacent cells, the need of a selector device able to drive high current in the programming on-state and to inhibit the current flow in the off-state, the *IR* drop management with large memory arrays, and the cell endurance with programming cycling. Several PCM architectures have been proposed to minimize the reset current.

Schematically, the various PCM cell architectures reported in literature can be classified into two main categories with their specific advantages and weakness, according to the taxonomy and philosophy:

- Built-in heater architecture where a dedicated element, hence named "heater," generates the heating necessary for the phase transition inside the PCM cell.
- Self-heating architecture that relies on the Joule heating generated inside the chalcogenide itself to increase the temperature and promote the phase transition.

The above presented mushroom-type PCM cell is the prototype of the first class that has been realized following different process embodiments and seize features [61–64]. In ref. [64], the synopsis of the process integration of one of them, the so-called "wall structure," that demonstrated its manufacturability at the 45 nm technology node as a 1 Gb PCM product operating at 1.8 V and exploiting a reset current as low as 200 μA can be found. At variance, an example of self-heating based cell in its extremely scaled version where the PCM cell constitutes the conformal connection between carbon nanotube electrodes with few nanometers diameter size is reported in ref. [65]. This is an academic work that demonstrated both the phase transition on the nanometer scaled device and the reset current scalability as low as 5 μA.

In addition to architectural approaches, mostly related to the programming current minimization, a lot of efforts have been devoted to other areas of improvement of the PCM to sublimate its performances, mainly by means of these three vectors:

- The thermal engineering in which guidelines can be found in ref. [66].
- Phase-change material optimization about which some refs can be found in [67–69].
- The minimization of the drift issue enabling the management of multilevel PCM as addressed in ref. [70].

It is worth to mention that, in 2009, PCM technology demonstrated the maturity to enter into the market through a 1Gb PCM product fabricated at the 45 nm technology node [71]. At that time, the feature set and main market focus for this product were the replacement of NOR flash memory in cellular phones. The product specifications were superior to NOR flash and ~10 millions of these devices were used in phones: it is believed that still today this represents the largest volume of bits ever shipped of a non-charge based solid-state memory device.

However, the choice of targeting the NOR cellular market may not have been the best choice. With the advent of smartphones, the cellular phone architecture started to rapidly move from a NOR-based "execute in place" architecture to a NAND+DRAM-based "store and download" architecture. This transition was driven by the rapid increase in storage required by the smart phone which was enabled by the rapid increase in density supplied by NAND. The NOR flash market in cellular phones dramatically decreased over the past 12 years and thus the PCM opportunity in this segment. Ultimately the cost of the technology was too high for the value delivered, and, while the technology was successful in manufacturability, endurance, and performance, the density was not high enough (meaning the cost structure not low enough) to be consistent with the feature set. The technology was not capable of delivering an "overwhelming compelling value" adequate to get the systems to make the changes required for its option. Definitively, this is the challenge for any emerging memory: since current system hardware and software architectures are heavily entrenched with many years of evolved development built into them in order to exploit the capabilities and mitigate the deficiencies of the existing DRAM and NAND memories, any emerging memory, such as PCM, must offer an "overwhelming compelling value" over conventional memories to motivate the entire ecosystem to adopt it and to eventually achieve success in the market. As mentioned in the semiconductor memories taxonomy at the beginning of this chapter, the storage class memory (SCM) applications represent the target of emerging memories. While from the side of performances like speed, power-consumption, and endurance, the PCM technology is demonstrating to be a top contender in the arena of SCM, the cost structure needs to be torn down. The 3D structure integration can reduce the cost of PCM devices. A cross-point stacked solution combining a PCM with an ovonic threshold switching as selector has been proposed in 2009 [72]. An emerging memory called 3D XPoint™ technology, without any details released by producers [73], but on which TechInsights reported that storage and selector elements are chalcogenide-based glasses [74], is entering to the market with a 128 Gb product at 20 nm lithographic node, showing the possibility for a new SCM.

2.20 In-Memory Computing and Neuromorphic Applications

The incipit of the volatile memory section of the present chapter recalled the von Neumann architecture introduced and used since the late 1940s and still the architectural principle for most computers (Chap. ▶ 32). In this architecture, there is a strict separation between the computation unit and memory. Thus, all data is stored in memory and then transported to the calculation engine back and forth. Data and instructions for the processing unit use the same data bus, leading to the so-called von Neumann bottleneck. Definitively, shuttling around all this data carries with it a significant power and performance price. Just think that in highly data-centric computing, most of the energy is consumed not in computation but in transferring data to and from the memory [75]. So, although the astounding progress through Moore's scaling law made possible demonstrations of truly remarkable tasks of artificial intelligence (AI), these results are achieved at the expense of an energy consumption that is orders of magnitude higher than the one of the human brain. Thus, radically new approaches, in some way emulating the human mind, are essential for creating a more efficient next-generation information technology.

Let's again have a look to biology: we already recalled as the human memory shows as a heterogeneous entity with complementary features, thus addressing the storage class memory as an opportunity, more favorable than the research of a universal memory. And in comparison to the separation of memory and logic of the von Neumann paradigm, biology figures out a better way: doing the compute in memory.

So a new frontier for memory technologies and systems lies in the development of a new computational memory paradigm where certain computational tasks are performed in the memory itself by exploiting the physical attributes and state dynamics of the memory devices. Conventional computation done in the CPU logic unit executes advanced operations through a sequence of elementary Boolean logic operations among bits. It has been quite recently demonstrated as emerging memories belonging to the class of memristive devices can emulate logic gates capable to carry out these functions [76].

Again, digital computers address the solution of problems such as linear systems by using a large number of computing steps by using the Boolean algebra, calling for possible most efficient ways to solve these kinds of algebraic problems. In this scenario, the nonvolatile memory (NVM) crossbar arrays represent a natural framework where, by construction, the matrix-vector multiplication (MVM) can be performed. Some ideas for the solution of algebraic problems with cross-point resistive arrays starting from the ability to execute MVM computations have been recently demonstrated [77, 78]. Figure 2.31 sketches a cross-point circuit for solving a linear system and mapping the elements of matrix A at the basis of the matrix formula: $Ax = b$, where b is a known vector (in this example the input currents) and x is the unknown vector [79].

In addition, an amazing feature of the human brain lies in its cognitive functions that are possible thanks to the learning and memory processes of a nervous systems. In neuroscience, the basis of the brain learning is found to be related to the process that modulates the connection strength of the

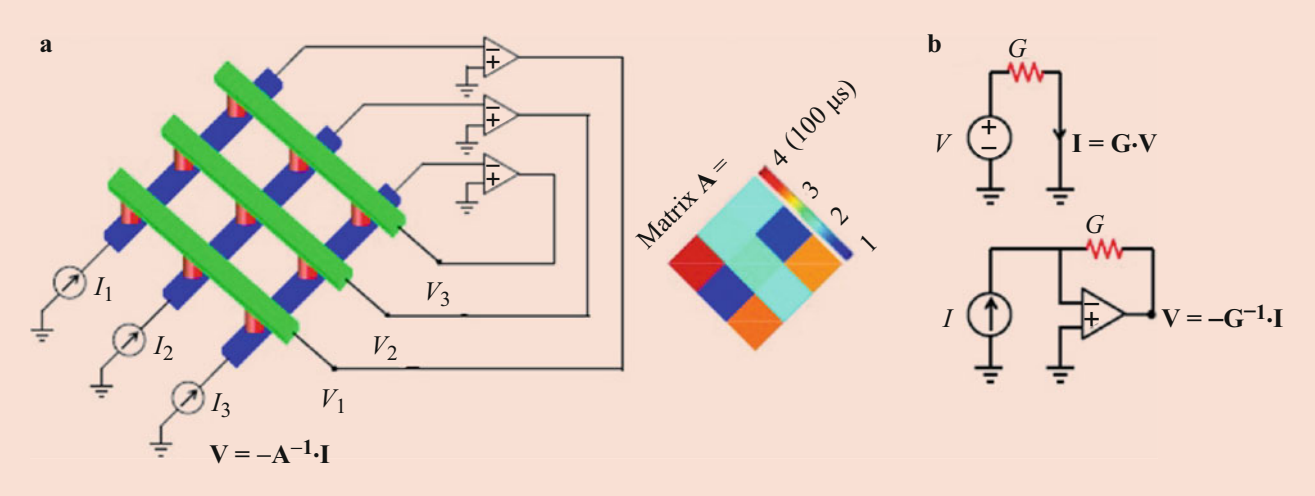

Fig. 2.31 (**a**) Cross-point circuit for solving a linear system or inverting a positive matrix. RRAM elements (red cylinders) are located at the cross-point positions between rows (blue bars) and columns (green bars). Conductance values mapping the elements of matrix *A* are also reported in figure a. (**b**) Circuits to calculate a scalar product $I = G{\cdot}V$ by Ohm's law and to calculate a scalar division $V = -I/G$ by a transimpedance amplifier

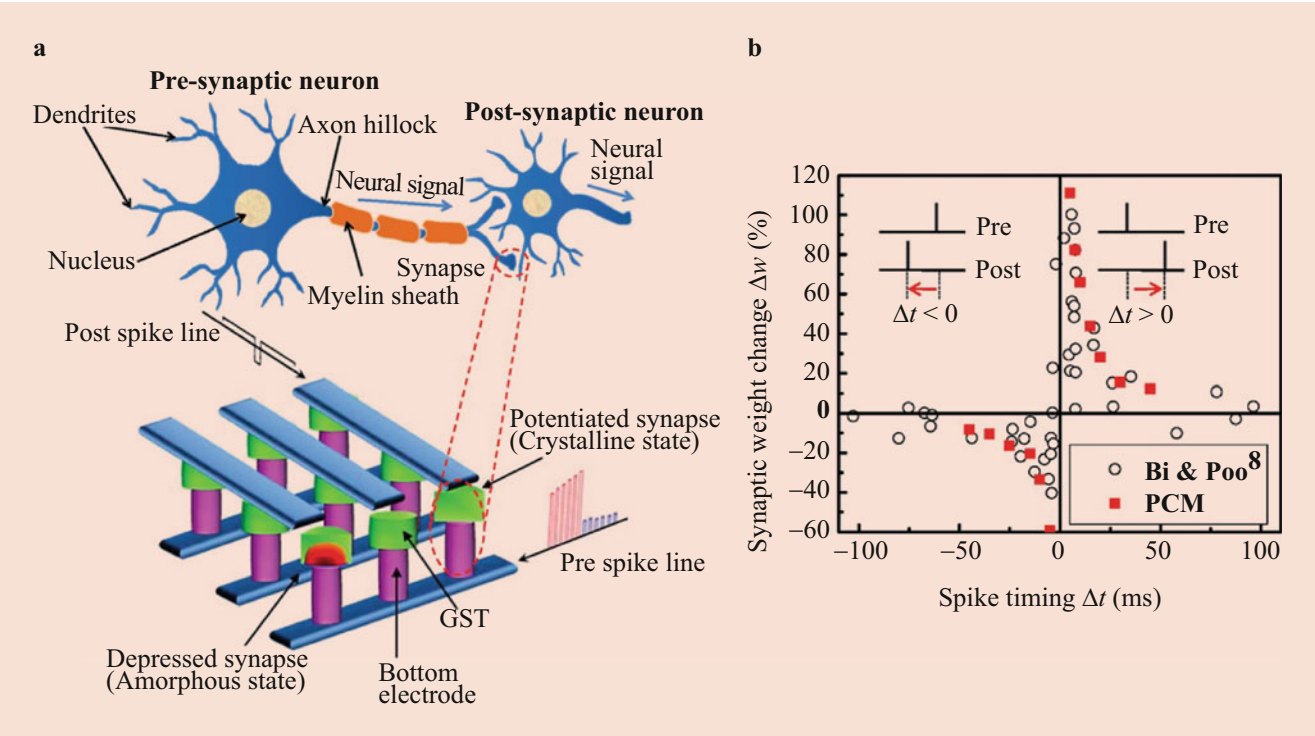

Fig. 2.32 (**a**) Schematic structure of biological pre-, post-, and synaptic connection. Bioinspired interconnection scheme of PCM synapses lies between post-spike and pre-spike electrodes; (**b**) synaptic weight change as a function of the relative timing of pre- and post-spikes implemented through PCM cells [80]. The good comparison with biological data demonstrates the ability to mimic the STDP behavior with PCM-based artificial synapses

synapse linking two neurons (referred to as synaptic weight). In particular, the spike-time-dependent plasticity (STDP) is a form of synaptic plasticity that updates the synaptic weight on the relative timing between pre-synaptic and post-synaptic spikes (see Fig. 2.9a). As it is shown in Fig. 2.32a, if pre-synaptic spike fires before the post-synaptic spike, long-term potentiation (LTP) will occur. Long-term depression (LTD) occurs when firing order is reversed.

Definitively, an electronic analog of a biological synapse needs the ability to exhibit STDP in order to mimic the synapse functionality. It has been shown that many emerging memory devices can really reproduce the synapse plasticity, fitting the biological behavior of synapses. An example of this is shown in Fig. 2.32b, where STDP is carried out by a PCM cell [80, 81]. In this context, IBM is strongly working employing phase-change memories that offer multiple advantages such as scalability, reliability, endurance, and multiple programming resistance levels giving them a suitable candidate for implementing large-scale synaptic systems.

In summary, dense crossbar arrays of emerging memory devices represent an opportunity to emulate the non-von Neumann human brain computing paradigm with high degree of connectivity (any given neurons having as many as 10,000 inputs from other neurons) through adaptive elements (synapses). This structure enables the massive parallelism and energy-efficient operation found in the human brain [82]. Nonvolatile memory (NVM) crossbar arrays to few nanometer dimensions are a promising path to build computing systems able to overcome the so-called "von Neumann bottleneck," performing the computation in the memory elements while they remain in place, thus avoiding the redundant load-and-store operations as the human brain suggests.

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BCD Process Technologies

3

Giuseppe Croce, Antonio Andreini, Paola Galbiati, and Claudio Diazzi

Contents

3.1 Introduction . . . 68
3.2 BCD Technology Platform Differentiation from Isolation Scheme . . . 69
3.3 BCD Technology Architecture . . . 73
3.3.1 Buried Layers and Epitaxial Growth . . . 74
3.3.2 Deep Trench Isolation . . . 75
3.3.3 Key Technology Features and Module Description . . . 75
3.3.4 Latest ST Technology Platforms . . . 82
3.4 New Technology Enablers for Application Evolution . . . 83
3.4.1 Increase Digital Processing Capability: Lithography, Logic, and Memories . . . 83
3.4.2 Power and HV Evolution: Device Architecture . . . 87
3.4.3 High Current and Energy Capability . . . 103
3.4.4 Passive Technology Modules for High Precision, Analog, and High Voltage Applications . . . 107
3.5 Next BCD Development Challenges . . . 109
3.6 Conclusions . . . 114
References . . . 115

Abstract

This chapter provides an overview of BCD (Bipolar CMOS DMOS) process technologies which are devoted to realize smart power ICs for different applications in the automotive, industrial, computer peripherals, and personal electronics domains.

After an initial overview of the possible isolation schemes and their reflection on the BCD platform differentiation, a description of the BCD technology architecture, compared to more standard CMOS processes, is presented.

Focus is then given on the technology enablers which are driving the innovation in order to meet the evolution of the applications.

The increase of digital processing capability and the need for embedded nonvolatile memories enabled by the minimum lithography reduction and by new emerging memory technologies are first discussed.

Then the requirements for more efficient and robust high voltage and high current power stages and the demands coming from analog functions are described showing power component architectures and innovations in the metal and dielectric layers which need to withstand very high currents and thermomechanical stresses.

The section on new technology enablers ends up with the presentation of passive modules to address specific analog and high voltage applications.

Finally, the future trends and challenges for BCD technology development are summarized.

Keywords

Smart power · BCD · DMOS · Power IC · RESURF · Safe operating area (SOA) · Galvanic isolation · DTI · Thick metalization

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3.1 Introduction

The name BCD has been created in the mid-1980s to classify that family of mixed processes which allow to integrate into a single-chip bipolar, CMOS (complementary MOS), and DMOS (double diffused MOS) transistors to realize power IC class called smart power ICs (Fig. 3.1) [1].

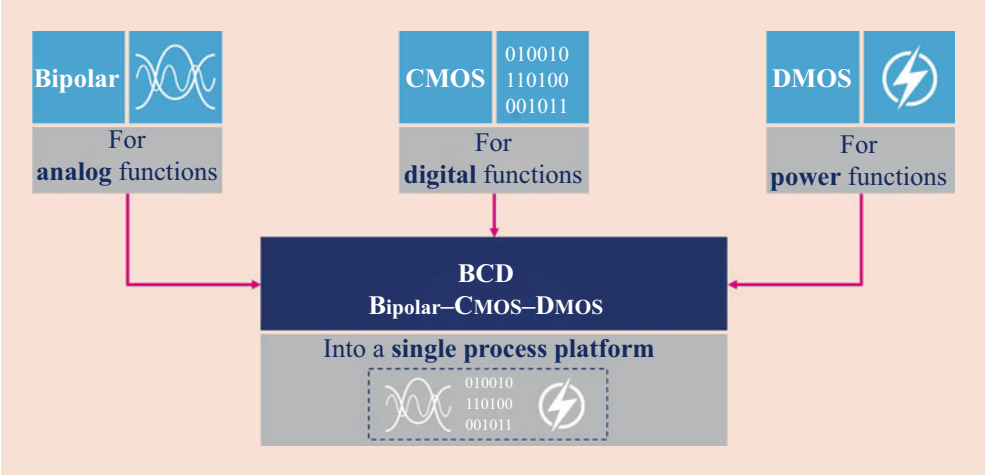

Fig. 3.1 Merging in one single BCD technology of bipolar, CMOS, and DMOS transistors

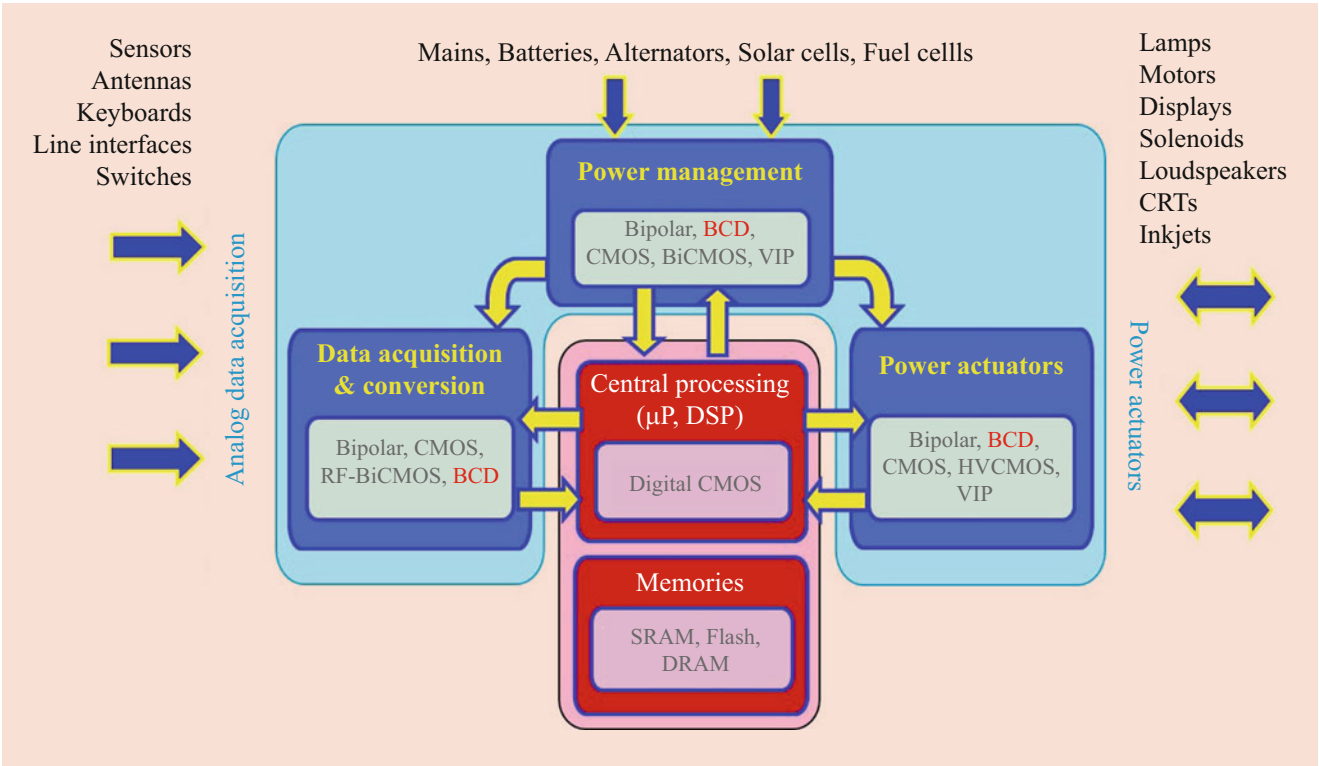

Fig. 3.2 Generic electronic system description highlighting the different functions addressed by BCD technology power ICs

This kind of technologies increased drastically the complexity of control circuits that could be integrated and led to a new way of approaching system integration, enabling:

- Higher energy efficiency solutions.
- Improved system reliability.
- Reduced electromagnetic interference.
- Smaller footprint of the final application.

Thanks to the BCD process technology features, the usage of this platform for power IC realization has been growing during the years since it has been possible to integrate in a cost-effective way many different functions in the same chip.

Today it is possible to state that any electronic system in any application field is requiring one or more power ICs realized in a specific BCD process technology to address (Fig. 3.2) some specific actions such as the following:

- Data acquisition securing, for example, system battery voltage accurate measurement, current and motion sensors output signals conditioning, or interface specific communication bus (LIN, CAN, FlexRay in the automotive application).

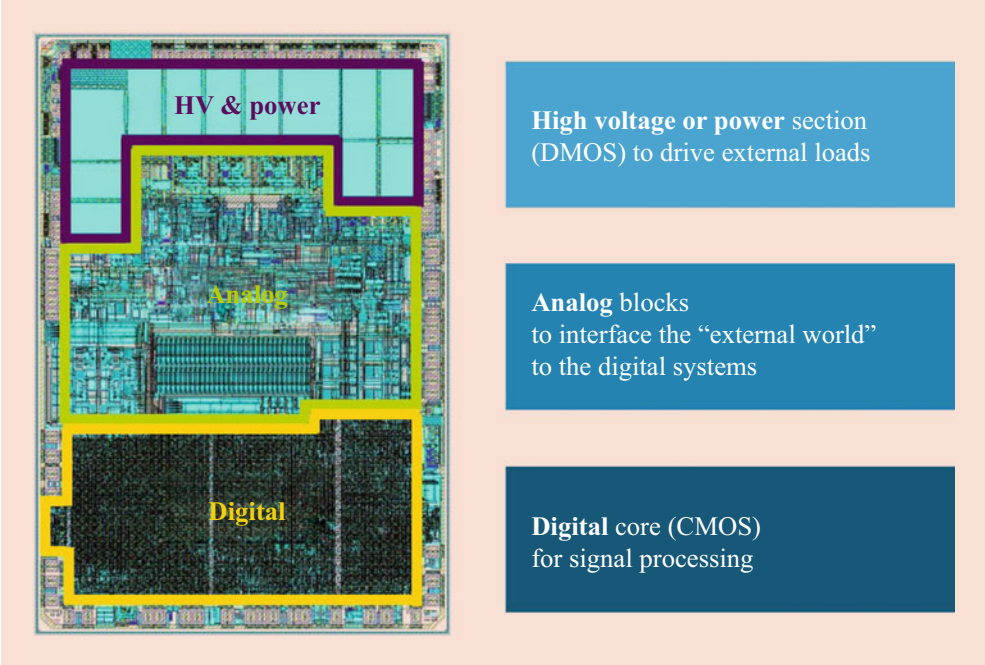

Fig. 3.3 Typical BCD power ICs embedding digital core, analog stages, and power section

- Power management securing the supply voltage and current to specific complex ASIC (application-specific integrated circuit – microcontrollers, memories) realized in advanced technology node.
- Actuation to drive many different loads such as electrical motors, gasoline car injectors, audio loudspeakers, or external large power discrete devices when loads are requiring higher power level.

In Fig. 3.3 a typical BCD power IC product is reported highlighting the three main integrated blocks for digital processing, analog signal conditioning, and power stages.

Given the very wide spectrum of application addressed with many different specific requirements, the integrated functions on BCD power ICs are driven by the overall electronic system cost and performance requirements. For this reason, the evolution of BCD technology roadmap during the years is following multiple paths (Fig. 3.4) to enable the right level of function integration on a single chip securing the application performance requirements with the minimum system cost level.

In the following paragraphs, the main enablers driving BCD technology evolution will be addressed.

This chapter describes the evolution of smart power technologies for automotive, industrial, and consumer applications that is going both in the direction of microlithography reduction; of improved power device performances, increasing voltage and current capabilities; and of additional tailored modules and analog features (Fig. 3.5).

Advanced technology nodes down to 40 nm with embedded nonvolatile memory solutions are today announced enabling added intelligence for monitoring and control.

Voltage capability is provided up to 2000 V and even on-die galvanic isolation up to 10 kV can be realized.

High current (tens A), severe energy dissipation requirements, extended life, and temperature range can be satisfied thanks to the availability of novel metallization schemes and packaging solutions.

3.2 BCD Technology Platform Differentiation from Isolation Scheme

In BCD technology, multiple devices are integrated in the same chip to realize the different functions. Electrical isolation among the different active and passive elementary components plays a key role in the final product performance. This is particularly true given the very demanding application constraints such as high junction temperature, high current switching power devices, and accurate analog stages.

Different solutions are adopted to achieve the appropriate isolation performance (see Fig. 3.6).

- Junction Isolation (JI)

  Today it is the most common solution given the lower integration cost. Isolation among devices is obtained through reverse biased P-N junctions (Fig. 3.7). Larger silicon area is required to withstand the voltage between adjacent high-doped deep n layers: reduced lateral diffusions and introduction of specific P-type bottom layers are required to mitigate the extra size. Since parasitic stray substrate bipolars are triggered during product operations, area consuming active protections are needed to mitigate cross talk among different devices.

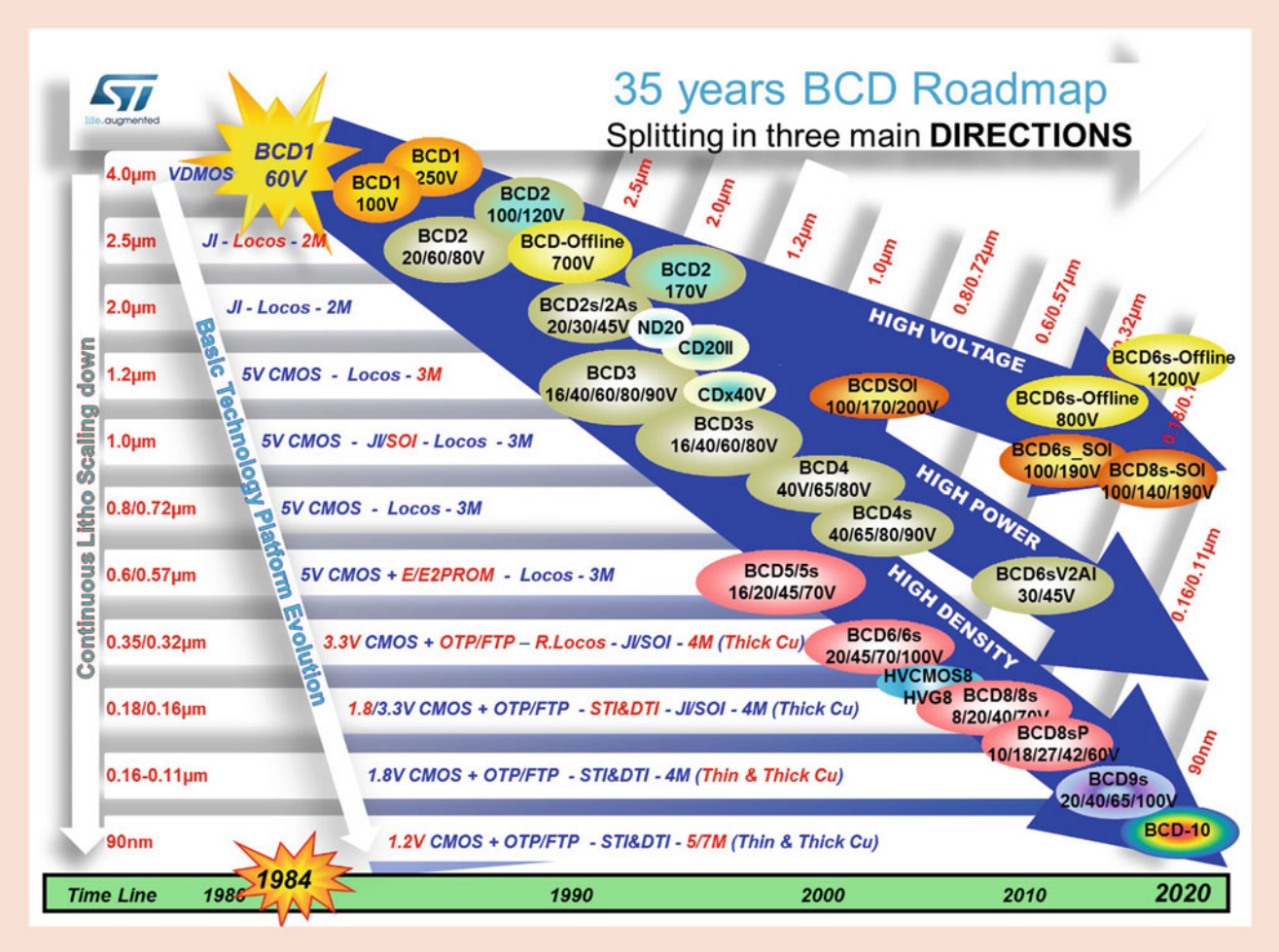

Fig. 3.4 ST BCD technology roadmap

- Deep Trench Isolation (DTI)

  Two adjacent devices are laterally isolated by a thick oxide in a deep trench in silicon (Fig. 3.8). This solution leads to a meaningful isolation area reduction (Fig. 3.9) increasing with higher rating voltage.

  The lateral contribution to intrinsic PNP parasitic bipolar (see Fig. 3.10) is inhibited by the deep trench limiting the amount of current injected in the substrate during the power operations. At the same time, deep trench is also limiting the lateral NPN bipolar gain reducing the electrons equivalent diffusion length in the substrate (see Fig. 3.11). Overall this is leading to a meaningful area gain and improved latch-up immunity.

  Together with the oxide isolation layer, many solutions have been presented introducing a highly conductive film (highly doped boron polysilicon or tungsten plugs) to secure a good ground connection to the substrate [2–4].

  The main drawback of this solution is the increased cost coming from the integration of different layers and process steps.

- Full Dielectric Isolation (Silicon on Insulator, SOI)

  This is the most effective solution to eradicate any parasitic effect among different devices securing an area effective electrical isolation (Fig. 3.12). Starting from silicon-on-insulator substrate, N-type silicon regions are separated laterally by oxide filled trench. To minimize cross talk among adjacent pockets in some implementation, a grounded silicon region is placed between two trenches. Increased thermal resistance and high starting material cost are limiting the adoption of this solution to a reduced number of applications usually requiring larger voltage (above 150 V) or demanding performance such as large negative voltage management, high power efficiency, or high junction temperature.

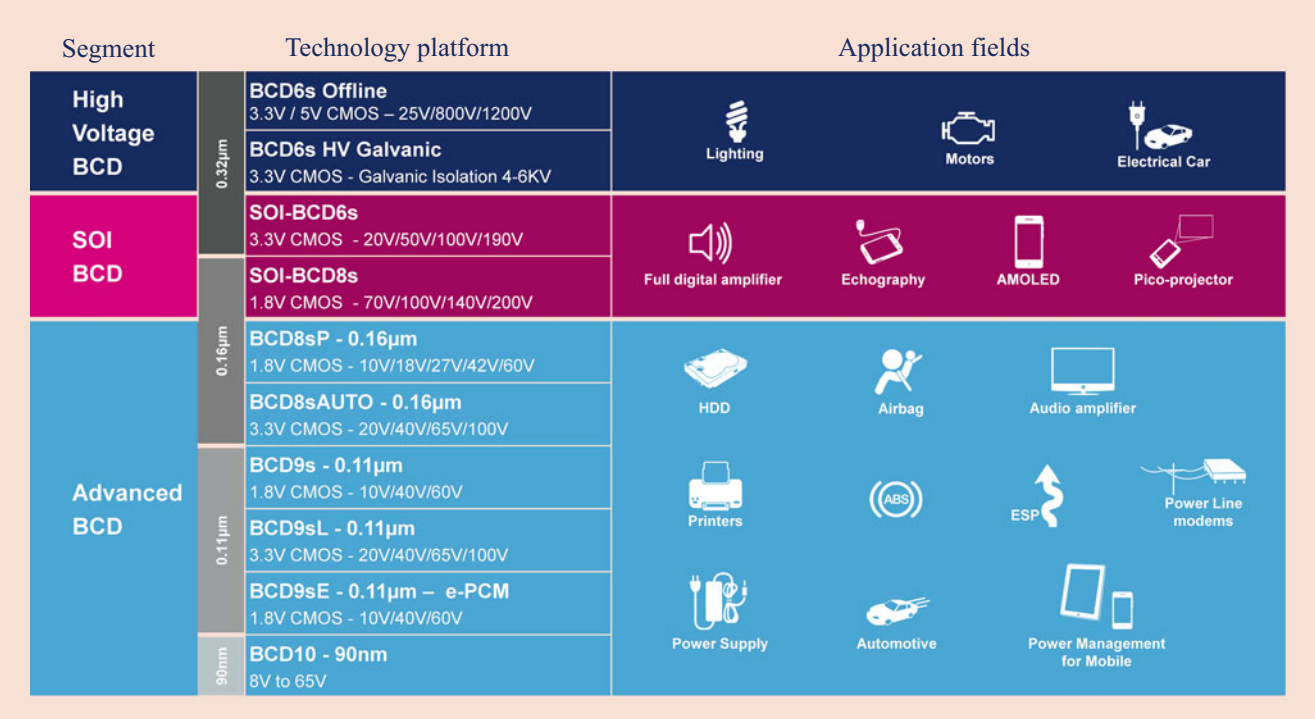

Fig. 3.5 STM BCD technology segmentation

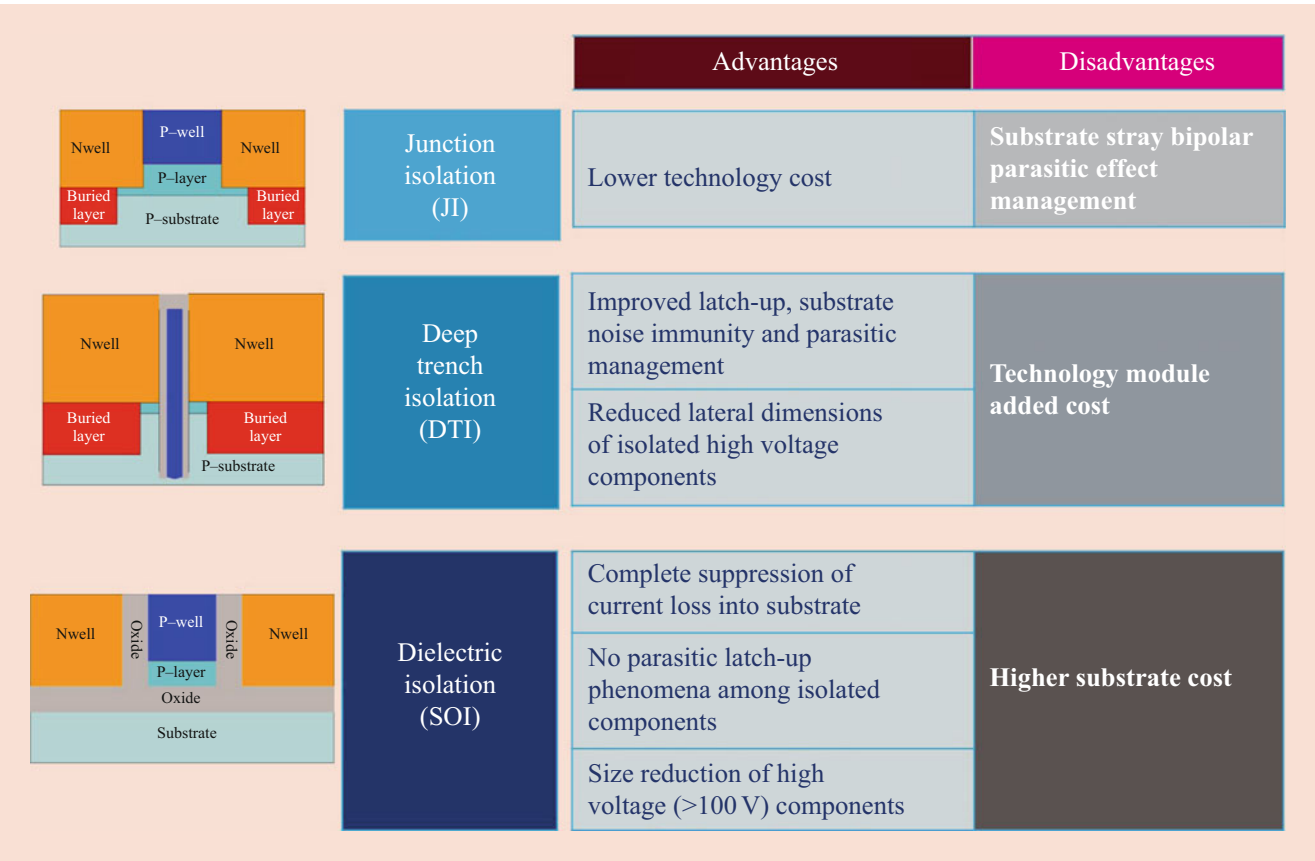

Fig. 3.6 BCD technology isolation architectures

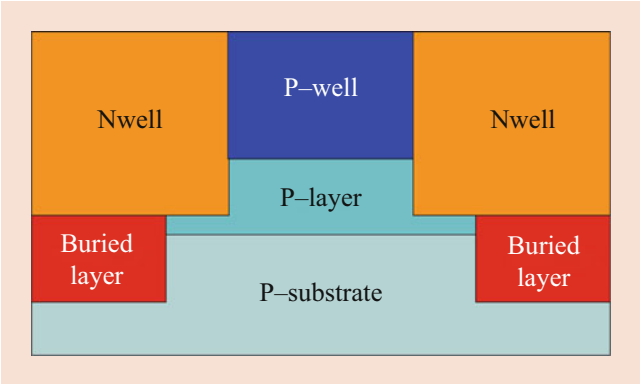

Fig. 3.7 Junction isolation schematic cross section. Two adjacent N-type regions separated by P-type silicon area

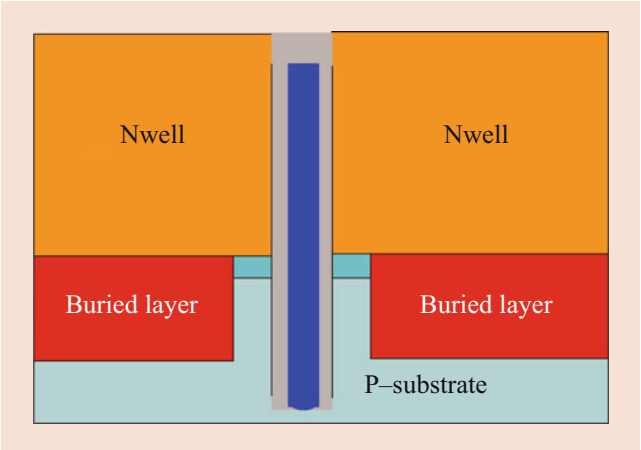

Fig. 3.8 Deep trench isolation architecture schematic cross section. Two adjacent N-type regions separated by a deep trench filled with a dielectric. In some implementation, a conductive layer may be added (blue region)

3.3 BCD Technology Architecture

The typical BCD technology architecture is shown in Fig. 3.13 in one of the latest implementation.

The most advanced BCD nodes are conceived following a process scheme as depicted in Fig. 3.14, which is realized adding some basic bricks to a typical CMOS flow:

- Buried layers and epitaxial growth.
- Scheme of isolation among components.
- Dedicated wells and implants for high voltage and power components.
- Steps for embedding of nonvolatile memories, both conventional and emerging types.
- Specific schemes of power metal levels.

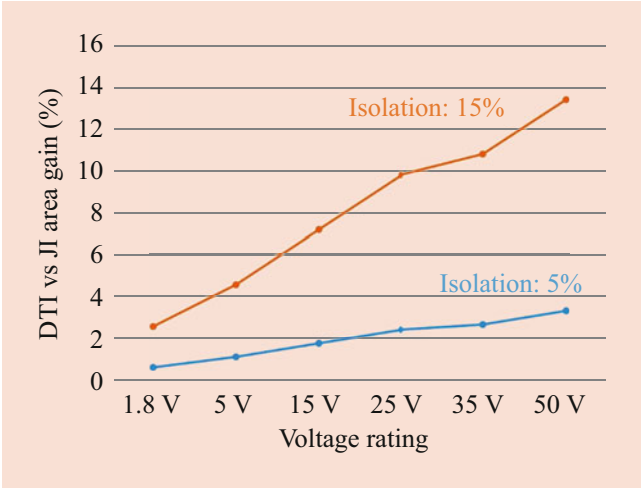

Fig. 3.9 Deep trench isolation area gain vs junction isolation for different rating voltage. Different curves refer to different amount of isolation in the circuitry. (Reference: ST proprietary BCD technology)

3.3.1 Buried Layers and Epitaxial Growth

Heavily doped N-type buried layers are historically introduced in BCD technology.

The original purpose of these layers has been to provide a low resistive path to collect the drain current of vertical power DMOS transistors bringing it to the die surface through heavily N-doped sinker diffusions.

The other N-buried layer functions are to reduce parasitic current injection into the substrate, to secure high voltage vertical isolation and to act as collector region in NPN bipolar transistors (Fig. 3.11). In this way the CMOS logic blocks are protected from collecting parasitic current injected in the substrate by the switching of power transistors, and therefore they are immune from disturbances coming from the power sections of the smart power IC.

In present BCD technology integrating lateral power DMOS transistor architecture, the drain current collecting function described above is no more required.

P-type buried layers can be added in the flow to enhance lateral isolation between components, as part of a junction isolation scheme.

Following buried layer implantations, lightly doped epitaxial layer is grown in order to build then all active and passive devices.

Its thickness and resistivity are key parameters to define the voltage capability: thin and low resistivity layers are commonly used for low voltage (<60 V) applications, while thicker and higher resistivity layers are adopted for higher voltage.

Different flavors of epi doping can be found in the microelectronic industry:

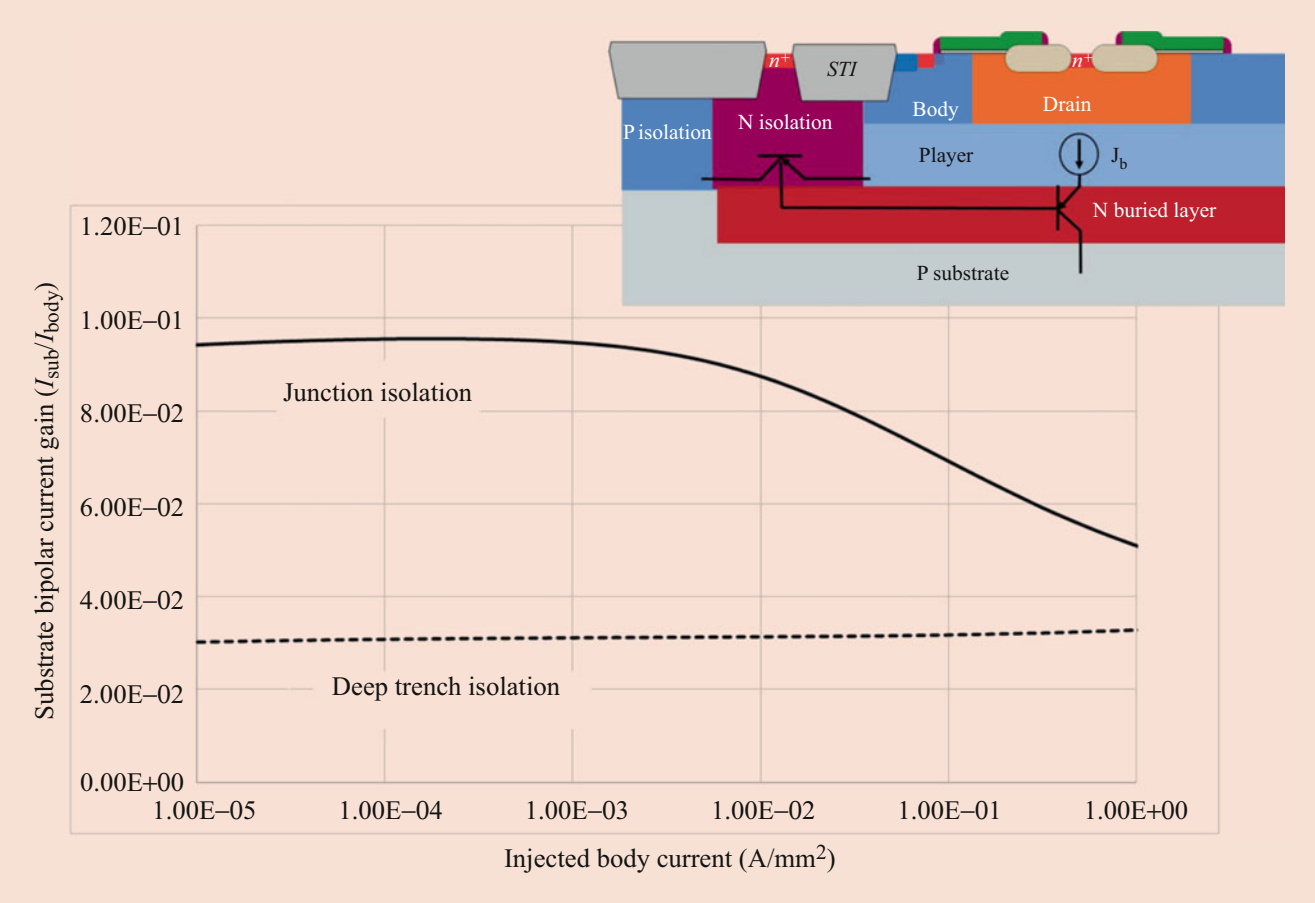

Fig. 3.10 Parasitic PNP bipolar gain (I_{sub}/I_{source}) as a function of the injected current density for JI and DTI. The maximum gain is observed in the lower current range due to the maximum lateral contribution. (Reference: ST proprietary BCD technology)

- P-type epitaxial layer secures compatibility with CMOS platforms, where this kind of doping is the common standard for this technology.

  The main drawback of this choice is the realization of high voltage components requiring thick epi since dedicated deep N-type layers should be added to connect N-type doped buried layer.
- N-type epitaxial layer enables an easier integration of high voltage components, but it may require dedicated implants for CMOS compatibility. Furthermore, P-type buried layers become mandatory with this option to provide N-type buried layer isolation between adjacent devices.

3.3.2 Deep Trench Isolation

Following epitaxial growth, in a possible integration scheme, deep trench isolation module is implemented.

First, a deep silicon etch is executed: depth and width are normally depending on the voltage requirements.

Following the silicon etch, thick oxide is realized to create the isolation layer. The filling may be completed by a dedicated poly layer that can act as stress relief and/or as a conductive plug contacting the substrate by removing the oxide at the trench bottom (Fig. 3.15). Recently, a BCD platform solution with two integrated trenches has been presented: one trench was suited for isolation and is filled with an oxide and an air gap, while the second one used to establish an electrical connection to the substrate is filled with a metallic layer (tungsten plug) realized at contact level [4].

3.3.3 Key Technology Features and Module Description

Following the process steps dedicated to the component isolation, BCD architectures are based on CMOS technology platforms with a modular approach to enable large process customization.

Thick oxide (*field oxide*) is deposited in order to suppress unwanted surface leakage currents among components, and the active areas are defined, adopting the concepts ported from CMOS technology baseline, depending on the specific lithographic node.

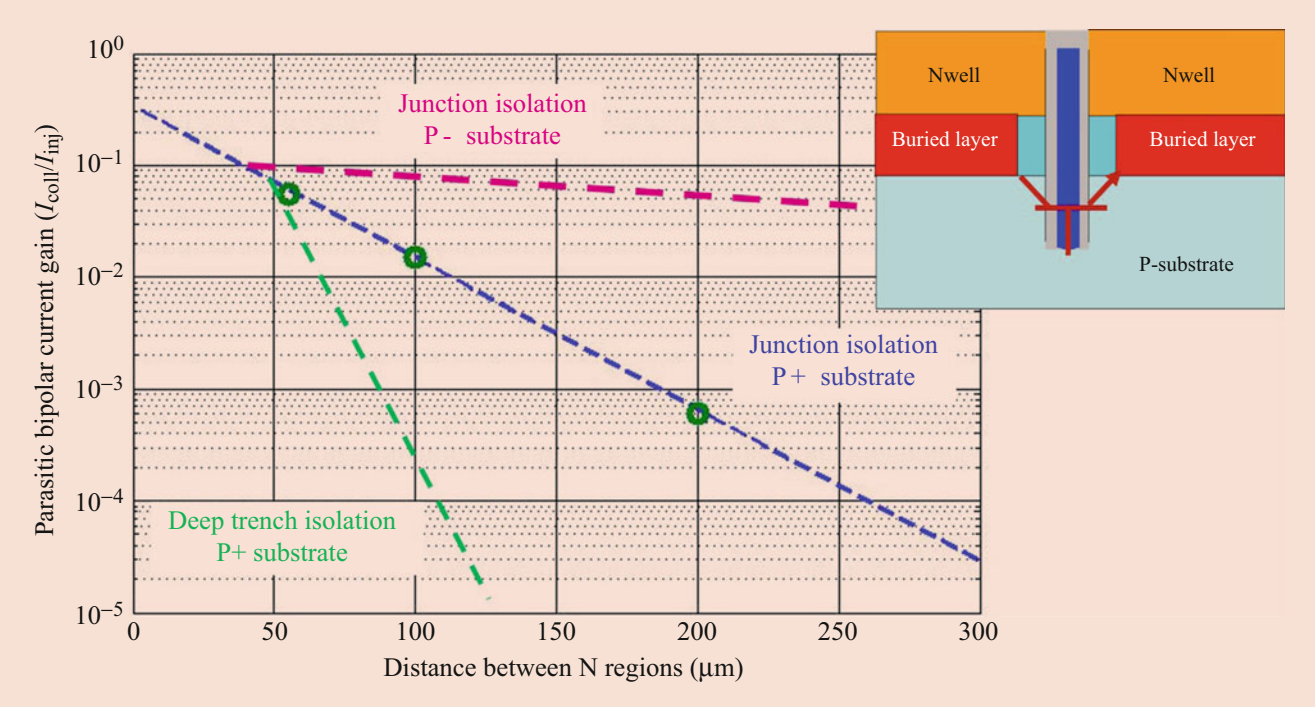

Fig. 3.11 Lateral NPN current gain ($I_{collected}/I_{injected}$) as a function of the distance between power and collecting device. Different substrate and DTI impact on electrons diffusion length is evident

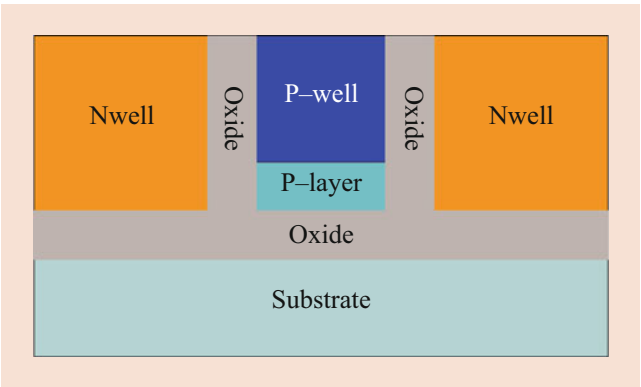

Fig. 3.12 SOI isolation architecture schematic cross section. Two adjacent N-type regions separated by oxide layer

Down to 250 nm node, the active area definition is realized with the well-known LOCOS (local oxidation of silicon) approach which is based on the selective growth of a thick oxide (field oxide) on a silicon surface masked by a patterned silicon nitride [1]. With this approach, a semi-recessed field oxide can be obtained, depending on the different specific techniques (simple LOCOS or poly-buffered LOCOS), but the transition between the thick oxide and the active area (*bird's beak,* see Fig. 3.16) has a non-negligible size. The thick oxide *bird's beak* shape is due to collateral oxide growth on the thin interface stress-relieving oxide layer placed between nitride and the silicon to reduce dislocation growth. Bird's beak shape and geometry depend on the thickness ratio between thin oxide and nitride layers.

As bird's beak inhibits pitch CMOS scalability (width and space), STI technique for active areas definition has been introduced to overcome this limitation.

Moving to minimum lithographic features smaller than 250 nm, a different scheme is used in order to reduce the size of the CMOS components: this scheme is called shallow trench isolation (STI), which is the preferred solution to increase the CMOS packing density, as it avoids the LOCOS bird's beak and realizes narrower isolation regions [5]. A trench etch is performed in silicon using an oxide-nitride hard mask, followed by an initial thin oxidation ("liner") and completed with a dielectric (silicon oxide) deposition providing adequate gap filling properties. The excess oxide is then removed with a chemical mechanical polishing (CMP) step obtaining a planarization of the wafer surface. STI geometrical top corner shape plays a key role to minimize the stress generated reducing the current kink in the CMOS sub-threshold region (Fig. 3.17).

The STI scheme permits to reduce the size of CMOS components as its horizontal size is significantly contained compared to the previous scheme (LOCOS) and because of the planarization of the wafer surface, resulting in finer dimension and pitch for the critical layers which are defined later on in the process flow, namely, the polysilicon layer for the CMOS gates and the contacts.

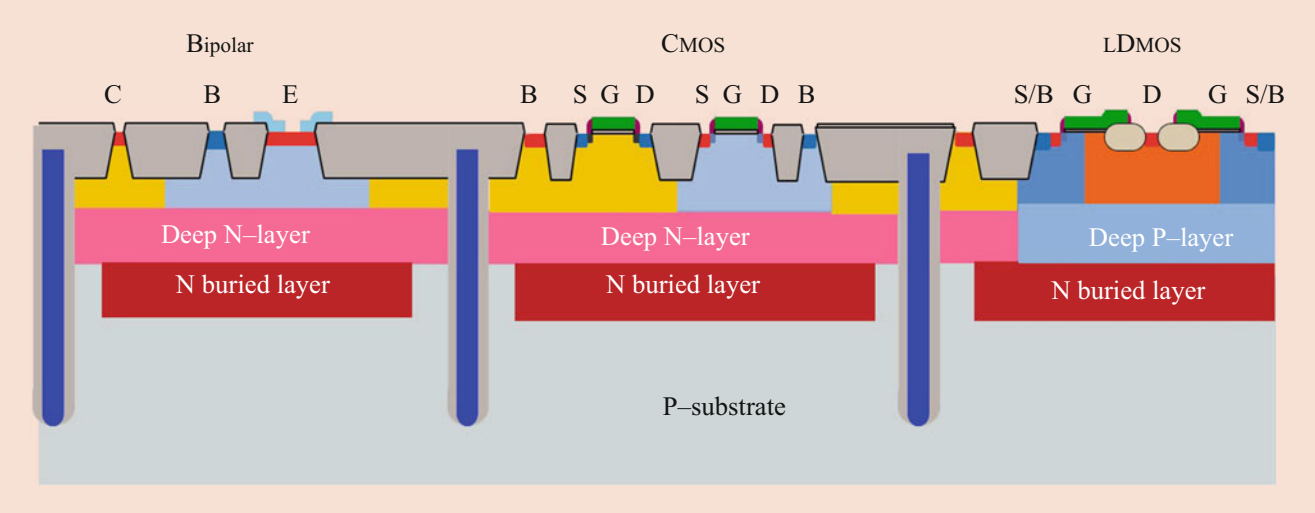

Fig. 3.13 BCD technology architecture

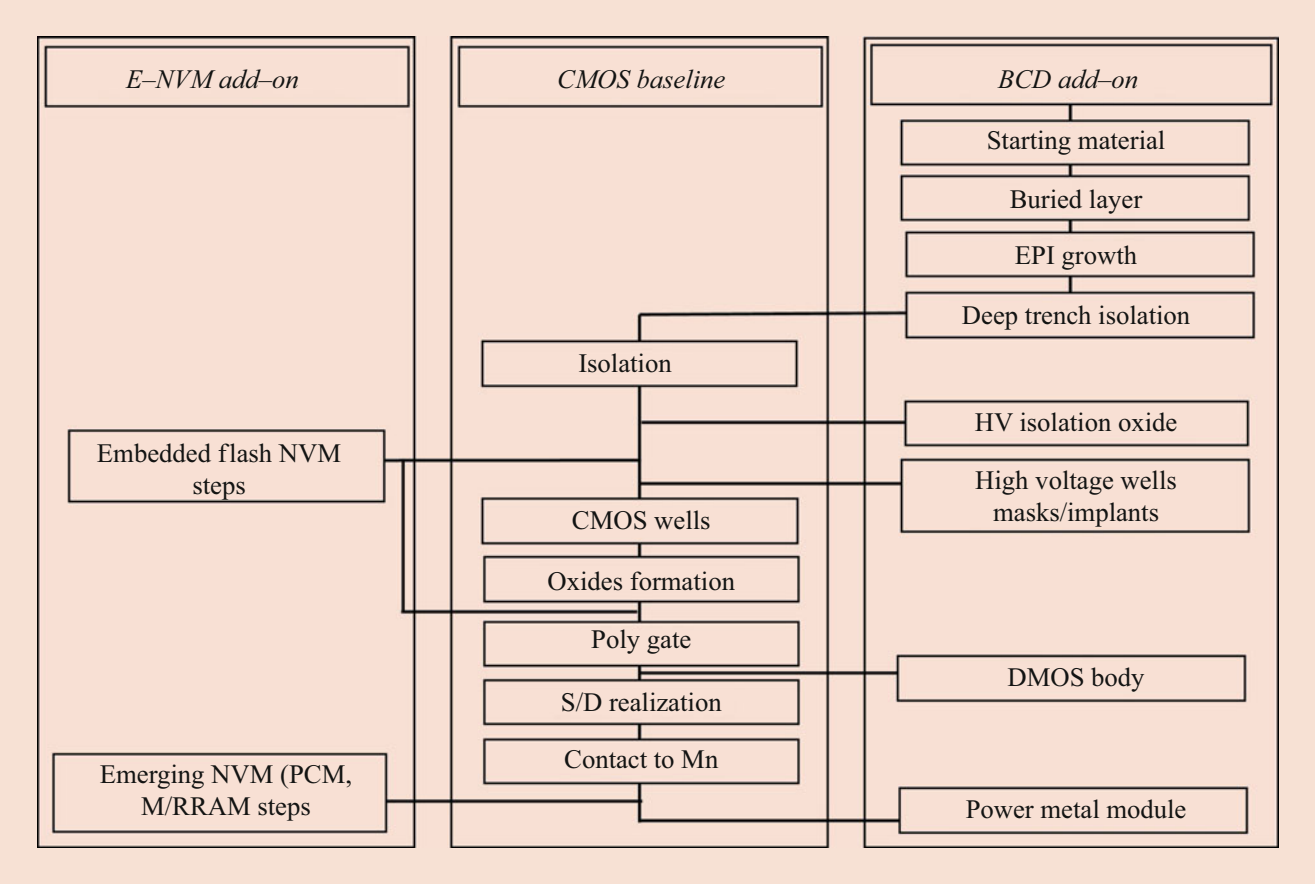

Fig. 3.14 BCD technology process flow

In a 160 nm BCD technology by ST (BCD8sP), in addition to STI for the isolation of the CMOS logic, a LOCOS scheme is present for the LDMOS power transistor blocks in order to optimize the device key performance parameters ($R_{on} \times A$, BV_{dss}), as it will be explained in more detail in Sect. 3.4.2. Therefore this BCD technology integrates two types of isolation: STI for the CMOS logic and LOCOS for the LDMOS power transistor blocks (Fig. 3.18).

After active area definition, the process flow continues with more specific construction steps aiming at the real-

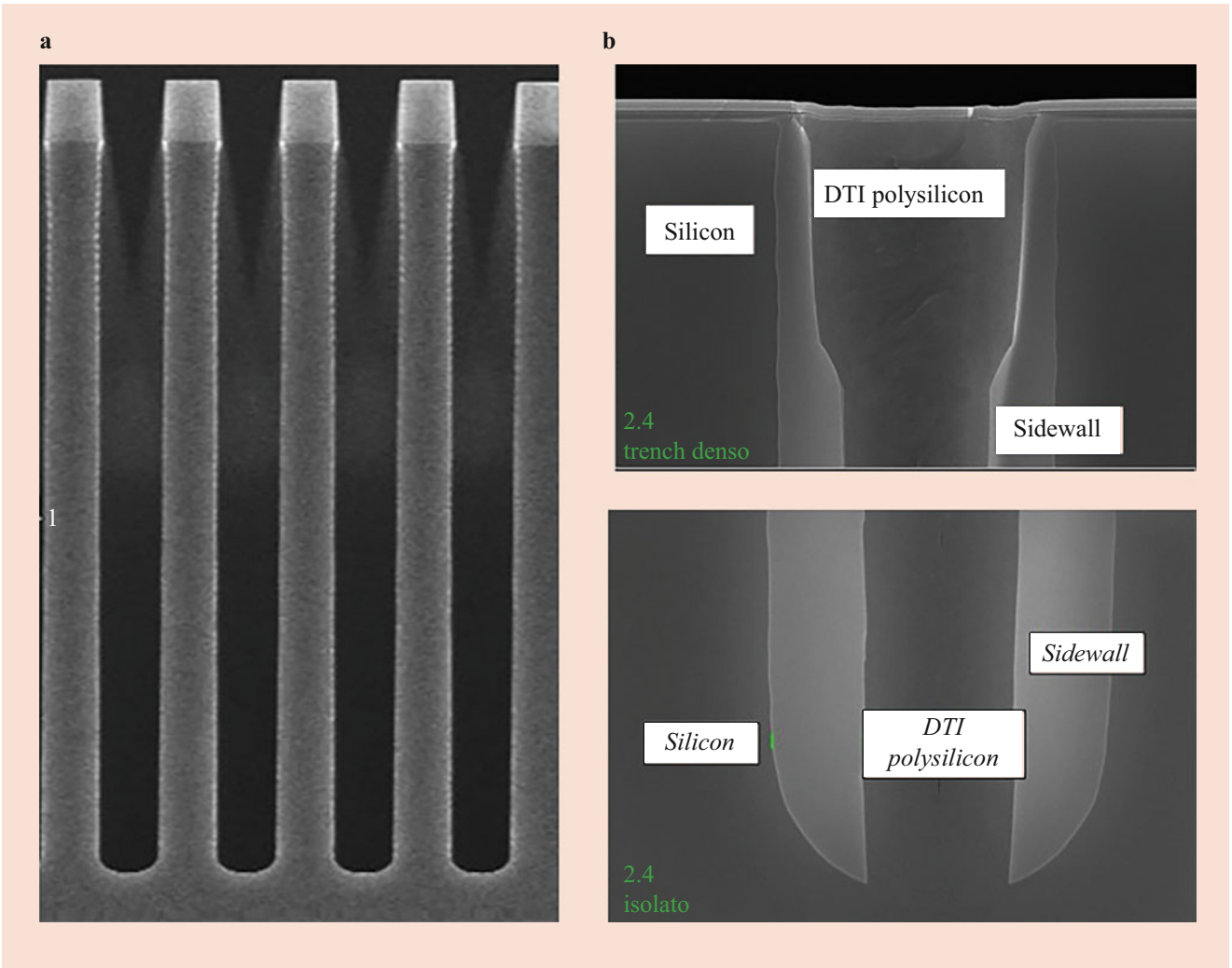

Fig. 3.15 Deep trench isolation module. Trench silicon etch (**a**), top and bottom details after oxide and poly filling (**b**)

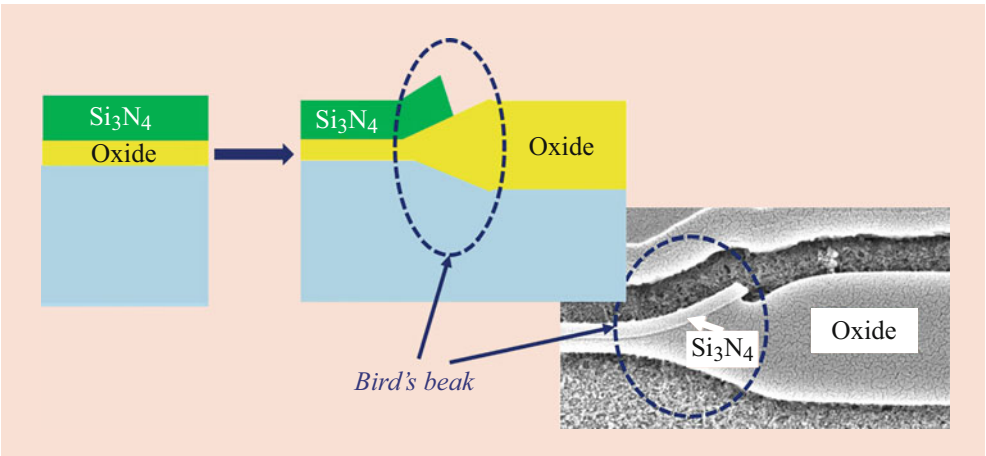

Fig. 3.16 Bird's beak schematic process and cross section

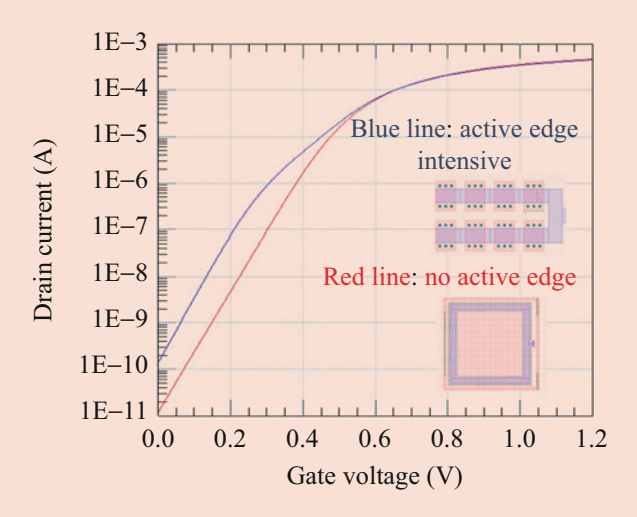

Fig. 3.17 Low voltage CMOS sub-threshold characteristic comparing an edge intensive transistor (blue line) vs a circular shape one without active edge (red line). The kink in the curve highlights a premature parasitic turn on at the active edge

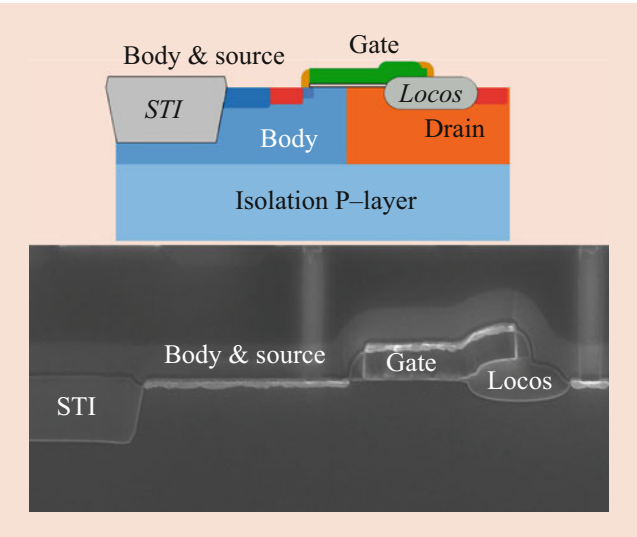

Fig. 3.18 160 nm BCD technology by ST (BCD8sP) integrating three types of isolations (STI, LOCOS, DTI)

ization of components and at the achievement of their performances: body layers for CMOS and high voltage MOS and DMOS components, specific wells, and deep layers to optimize components high voltage and isolation capability.

Multiple implants are today required to realize CMOS body region. Implant conditions are determined to fix the required threshold voltage values, short channel effects immunity and to guarantee latch-up robustness. For high voltage devices body formation, additional requirements must be taken into account: larger voltage capability and robustness against the activation of the parasitic NPN (Fig. 3.19).This implies more stringent constraints to the implant conditions

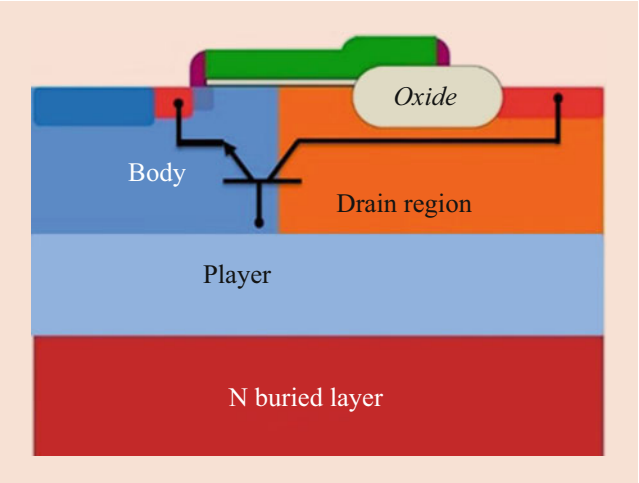

Fig. 3.19 Parasitic NPN in HV MOS transistor

for these layers, and therefore the re-use of the CMOS wells is not always the most appropriate solution requiring specific added implants for optimal component performance.

In addition to the well dedicated to body regions, N-type and P-type layers are introduced in the flow to realize the high voltage NMOS and PMOS components drain drift region.

High blocking voltage for components at minimum penalty for the active performances is driving the layers engineering: to this purpose the *Resurf* [6] principle has been progressively used not only in very high voltage application but also to realize components for a voltage operation <100 V. RESURF concept was introduced in the late 1970s: thanks to the simultaneous electrostatic effect of lateral and vertical diodes biased in reverse mode, very high breakdown voltages were recorded. A detailed description of this principle and on the advantages brought in the high voltage device design and performance is reported later in the chapter (Sect. 3.4.2). It's worth to mention that the adoption of this basic principle and its further refinements (single and double Resurf effect) imposes clear constraints on the final charge dose in silicon for the layers to be formed.

The dedicated deep layers enable to increase the versatility of the use of high voltage components, as they can be used to suppress the injection of parasitic current into the substrate when the drain terminals are forced to a negative biasing compared to the substrate ground potential, as it will be explained in more details in Sect. 3.4.2.

The gate oxide is then grown inside the active areas: multiple gate oxides are widely used. First oxidation step grows a thick gate oxide for high voltage MOS components, followed by the CMOS gate oxidation with a thinner thickness, which depends on the specific CMOS node. The thick gate oxide is adopted also to realize a higher

voltage rated CMOS (typically 5 V), needed for pins I/O, analog stages implementation, and for memory programming operation.

Ported from the most advanced CMOS process flow, gate oxide nitridation is introduced in order to cope with the need to avoid penetration in the channel surface region under thin gate oxide of the high energy boron implants for polysilicon doping and source-drain formation. Analog MOS performances (low-frequency noise) and threshold voltage stability of PMOS due to NBTI (negative bias temperature Instability) effect [7] are the drawbacks of such introduction. The NBTI is a degradation mechanism due to positive charge buildup in gate oxide and at Si/SiO_2 interface, which affects PMOS performances when stressed at negative gate voltage and at high temperature condition. The degradation is electric field dependent; it involves all relevant PMOS electrical parameters, in particular the threshold voltage (increasing in absolute value) and the drain current (decreasing in absolute value), and it is associated to the capture emission of semiconductor charge carriers on localized electronic states and to the weakening of Si-H bonds, which can be considered as oxide and/or interfacial defects.

According to the modular approach of BCD process flow, additional steps can be inserted at this stage to implement nonvolatile memory (NVM) cells: oxidation for tunnel oxide and possible second polysilicon level for dual-poly flash/EEPROM memories are the most peculiar steps of this module. When single poly EPROM or EEPROM are implemented, a single poly gate layer scheme on differential gate oxide is adopted (Fig. 3.20).

After the polysilicon layer deposition and patterning for the MOS gates, in many BCD platforms another peculiar step could be introduced: the body layer for the DMOS components. The layer is implanted self-aligned to the patterned polysilicon with conditions and thermal treatments to be defined in order to obtain the DMOS channel region as a difference between the body lateral junction length and the subsequent source implant lateral profile length. This way the DMOS channel length is independent of the technology minimum processable lithography [8].

The DMOS body formation evolved significantly in the last 20 years starting from implantation followed by prolonged high temperature diffusion step to solutions more compatible with advanced CMOS technologies with finer lithography and thinner gate oxides. The newer solution is based on a large angle tilt implantation performed without adding to the process flow any specific thermal treatment (Fig. 3.21). It was presented [9] that a 45° tilt angle implant gives the best trade-off between lateral and vertical body junction depth.

The subsequent process steps up to the formation of the metallization lines (*back end of line – BEOL*) are based on the advanced CMOS process flow of the equivalent lithographic node.

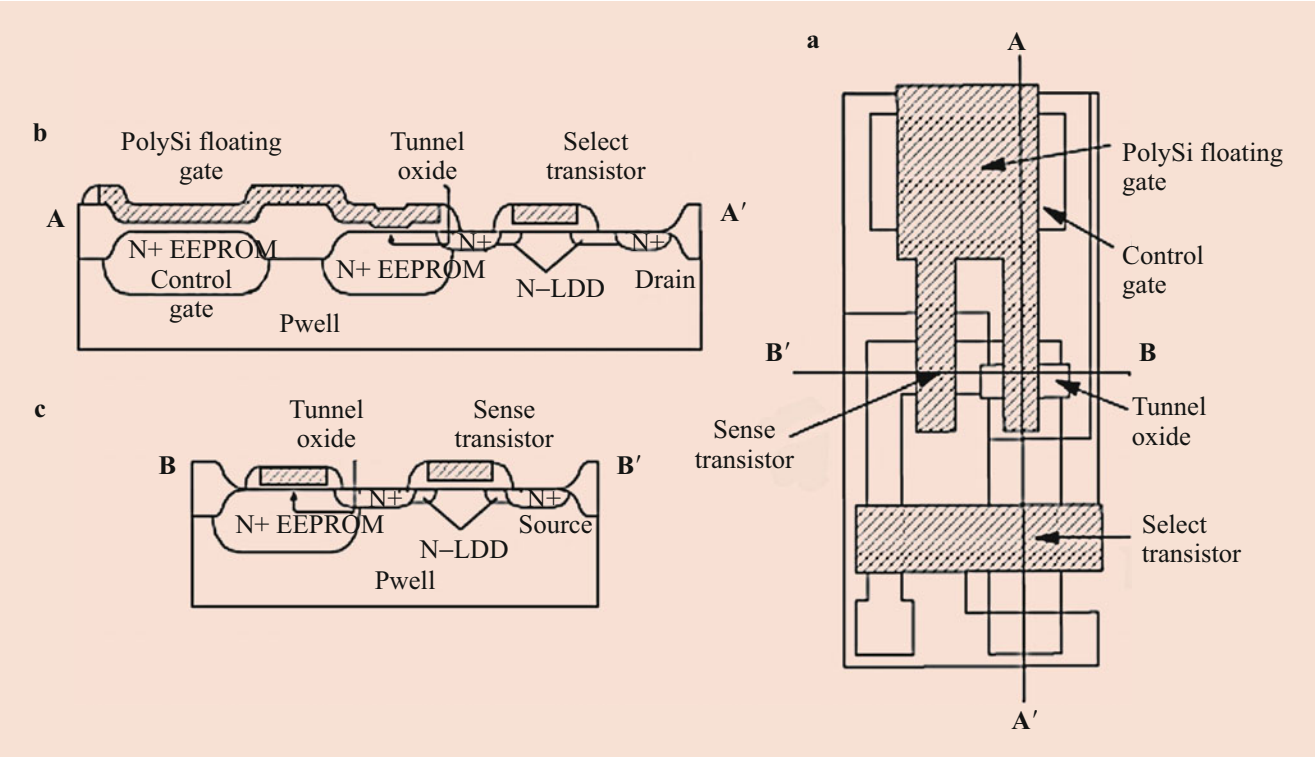

Fig. 3.20 Single poly EEPROM cell structure. (**a**) Top view. (**b**) Section along A-A′ line. (**c**) Section along B-B′ line

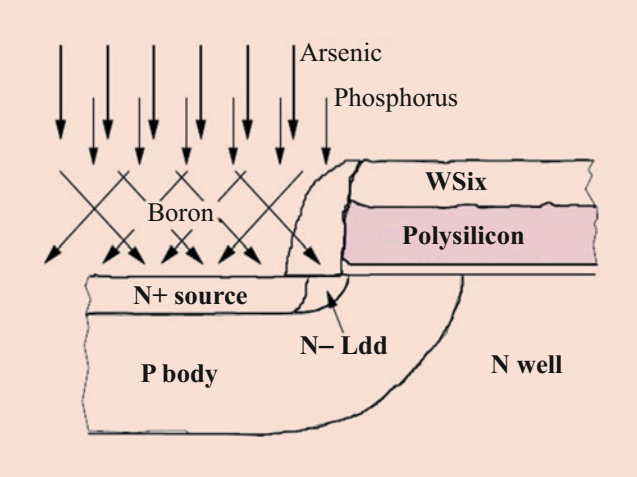

Fig. 3.21 Large angle tilt implant for DMOS body formation

Also the thin metal levels used in BCD technologies followed the advanced CMOS roadmap, evolving from aluminum down to 160 nm to damascene copper for 130 nm and below. The evolution to thin copper metal system provides an additional advantage in BCD technology enabling higher robustness under thermomechanical stress induced by high energy pulses of the power MOS section, as it will be shown in Sect. 3.4.3.

However, some peculiar requirements of BCD application force to introduce modifications to the BEOL scheme adopted in CMOS technology. The specific requirements to be fulfilled are related to the needed high voltage and high current capability, which have an impact on the thickness and materials to be used for the inter-metal dielectric layers, to provide the required isolation among metal lines, and for the metal lines, to guarantee the reliability against electromigration phenomena. Electromigration is a phenomenon of mass transport inside interconnections stressed with high current densities. The mass transport creates voids or hillocks. The voids can give rise to increased interconnection resistance or eventually evolve in open circuit after long stress time.

Emerging memories described in Sect. 3.4.1 are conceived to be added in the BEOL with the advantage to be modular and to not affect the architecture of the active components implementation. Their integration in the BEOL requires to add dedicated steps, as stacked contacts, specific and unconventional materials for programming and storage elements.

An additional aspect to be considered is the BEOL thermomechanical robustness against the stress related to the assembly steps, in particular in case of active components placed under wire bonding or bumping structures.

Very specific to BCD technology is the top metal level (*power metal*) due the multiple functions needed to be accomplished:

- High current capability.
- Low resistance.
- High electromigration robustness.
- Heat dissipation during power pulses.
- Mechanical stiffness for wire bonding with large diameter wires of different materials (Au, Cu, Al, Ag).

Historically the solution adopted by the silicon manufacturers has been based on a thick aluminum layer, with thickness in the range of 3–5 μm.

To improve the performances, thick copper metallization was introduced starting since the late 1990s [10–13].

The first presented solutions disclosed a realization scheme based on the so-called *patterned* copper approach, capable to grow thicknesses in the range of 10–20 μm [14, 15].

The process starts with the deposition of a barrier layer (usually realized with TiW alloy) and of a copper thin layer to be used as a seed for the successive growth (Fig. 3.22). A thick photo-resist layer is then span on the wafer surface and patterned to open the areas where the copper will have to grow. An electroplating technique is used to grow the copper at the required thickness, followed by the photo-resist removal and by a copper seed and barrier etch. In this way, the process is completed and the different metal lines are defined.

The patterned approach is common to the copper redistribution layer (*RDL*) solutions adopted for chip scale package (*CSP*) and has the flexibility to grow different copper thickness in function of the application requirements.

The drawback is the large copper line pitch (width + space) that limits the routing capability of this metal level: typical pitch values are in the range of 20–30 μm, depending on the copper thickness.

A different approach has been therefore developed based on the advanced VLSI CMOS BEOL scheme: damascene thick copper processes providing a thickness up to 5 μm are feasible and enable a top metal line pitch in the range of few μm, giving therefore great advantage in the routing density for power buses, compared to the patterned scheme.

Depending on the selected type of the top metal scheme architecture, several and diversified approaches can be found for the front-side finishing of the wafer in order to provide suitable solutions for the electrical connection to the package and for protecting the die from the external environment.

Smart power products peculiarity must be considered: loads sinking high current requiring large bonding wires connections, assembly in stressing packages for power dissipation and applications in harsh ambient conditions.

In case of applications in packages using wire connections, the top thick aluminum layer or an aluminum layer capping the copper top metal in the bonding area are the simplest solutions, the latter ported from CMOS technology (Fig. 3.23).

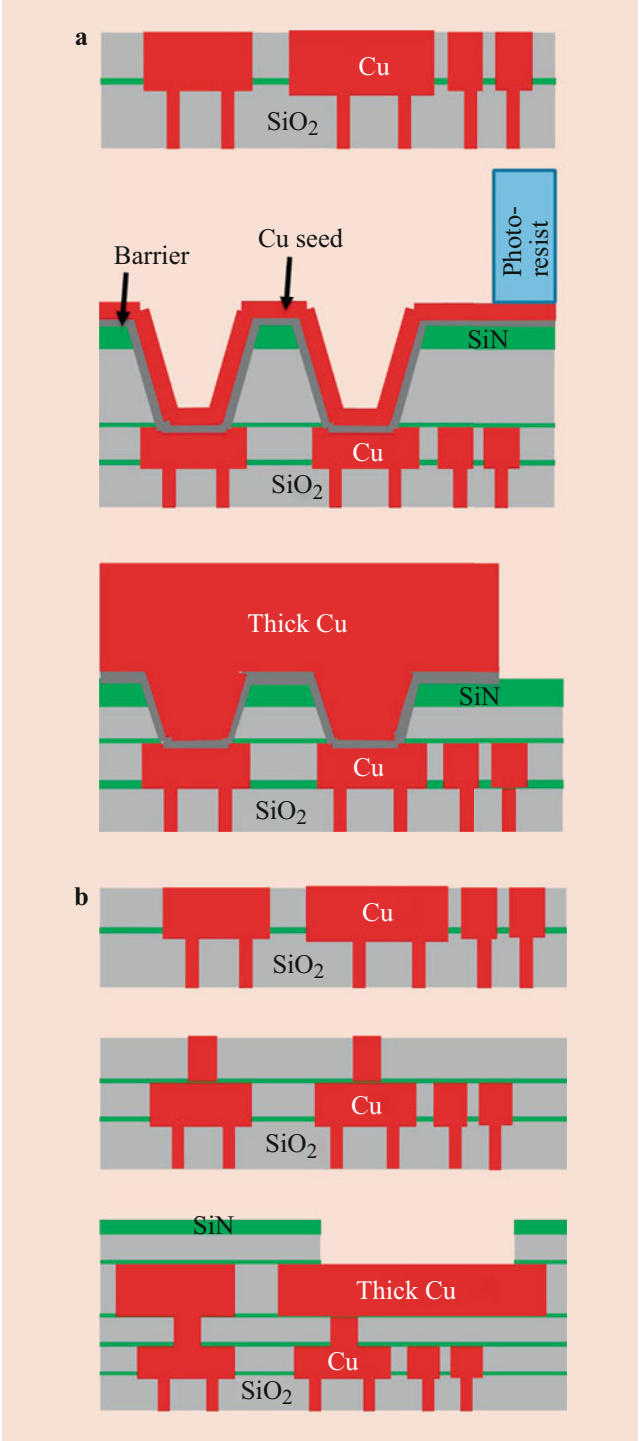

Fig. 3.22 Thick Cu process flows. (**a**) Patterned Cu. (**b**) Damascene Cu

An alternative more robust structure can be realized with a different metal layer stack composed by nickel, palladium, and gold, grown over the aluminum or copper bonding area by electroplating or by electro-less plating techniques [16]. This layer stack is generally called over pad metallization (OPM, Fig. 3.24).

The protection of the die from the external environment is provided by the deposition of final inorganic layers (*passivation*), preferably realized with silicon nitride which has superior sealing properties against moisture absorption, and of organic polymeric coating layers (*polyimides*) to planarize the die top surface and to act as buffer layers against the thermomechanical stress induced by the packaging materials.

In case of the patterned thick copper scheme, where the top metal is grown over the final passivation, a metallic coating solution can be adopted, realized with nickel and palladium (and gold) grown by electro-less plating and encapsulating the thick copper strips (Fig. 3.25). This solution permits to provide both mechanical protection during wire bonding for the underlying structures and to inhibit copper corrosion from the external environment.

3.3.4 Latest ST Technology Platforms

BCD technologies offer a wide possibility of integration capability. They allow to cover more and more single-chip solutions and the integration of digital CMOS, analog, and power stages in very flexible configurations (low side power, high side power, half/full bridge, etc.).

As an example, this paragraph describes the key characteristics and electrical features of BCD9s (110 nm), a proprietary STMicroelectronics technology specially conceived for power applications, with voltage rating ranging from 20 to 100 V.

Due to the flexibility and modularity, the technology can be applied to power management, industrial, and automotive applications.

The technology is modular and allows the best trade-off among performances/application needs/cost; masks can be added according to the application and the required voltage ratings.

In the basic process option, the technology features a voltage rating up to 40 V, with two gate oxides:

- 12 nm gate oxide for 5 V analog CMOS and for the gates of the high voltage power components which are optimized for a very low on resistance
- 3.5 nm gate oxide for 1.8 V digital CMOS with ~500 kTransistors/mm^2 gate density, which is suitable for digital intensive applications.

The voltage rating of the high voltage and power components can be increased up to 60 V, 80 V, and 100 V adding dedicated doped wells and adopting specific component architecture.

The technology is conceived with a deep N+ buried layer for robust and safe driving of inductive loads.

The metallization scheme implements a full copper solution that includes four metal levels, three thin damascene

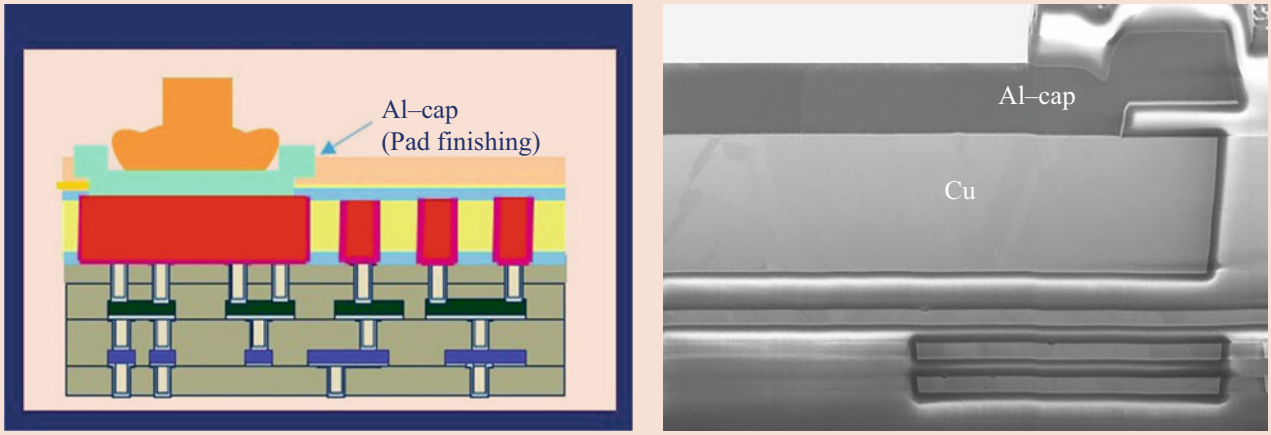

Fig. 3.23 Damascene thick copper + aluminum cap wire bonding pad

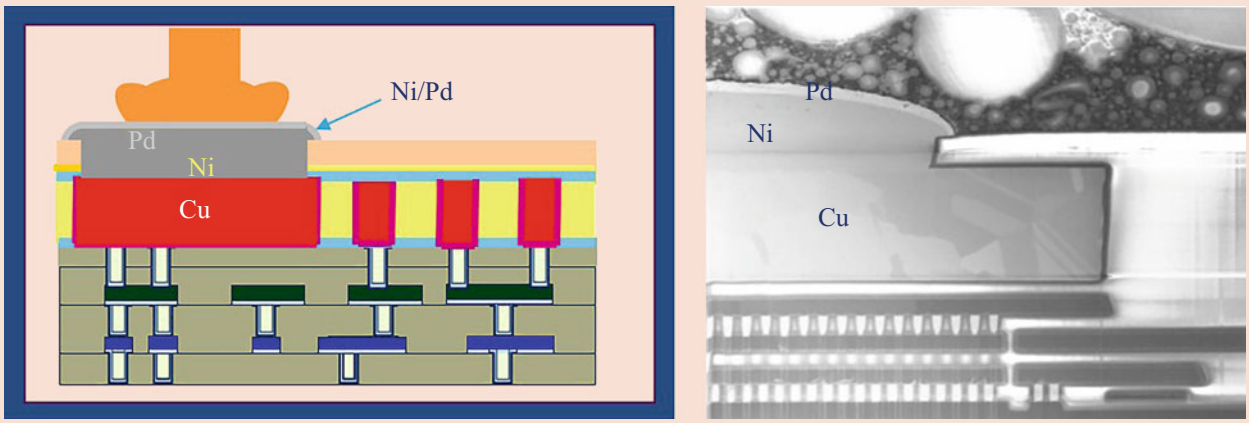

Fig. 3.24 Damascene thick copper + over pad metallization (OPM)

copper metals for signal routing, and one thick copper metal for power routing.

The technology architecture allows, for all the high voltage classes available, low side and high side configuration; hence it is possible to implement in a single-chip half bridges and full bridges topology (Fig. 3.26).

Table 3.1 summarizes the main technology options.

3.4 New Technology Enablers for Application Evolution

In the following paragraphs, the main enablers driving BCD technology evolution will be addressed.

Initially, the path toward denser BCD technology nodes will be presented highlighting the benefits associated to the introduction of some key CMOS technology modules and the widening of applications enabled by nonvolatile memory architectures.

Power and high voltage device architecture evolution is then widely described focusing on the key enablers to boost continuous performance improvement. Thanks to the achieved performances, on latest generations larger current and energy levels have to be handled requiring specific solutions for power metallization and assembly.

Finally, passive technology modules for high precision, analog, and high voltage applications will be described as additional enablers for function differentiation.

3.4.1 Increase Digital Processing Capability: Lithography, Logic, and Memories

Since its origin, BCD technology has followed with some delay the evolution of CMOS roadmap securing a continuous scaling of logic blocks offering increased capability for digital processing. This trend was originally straightforward: new

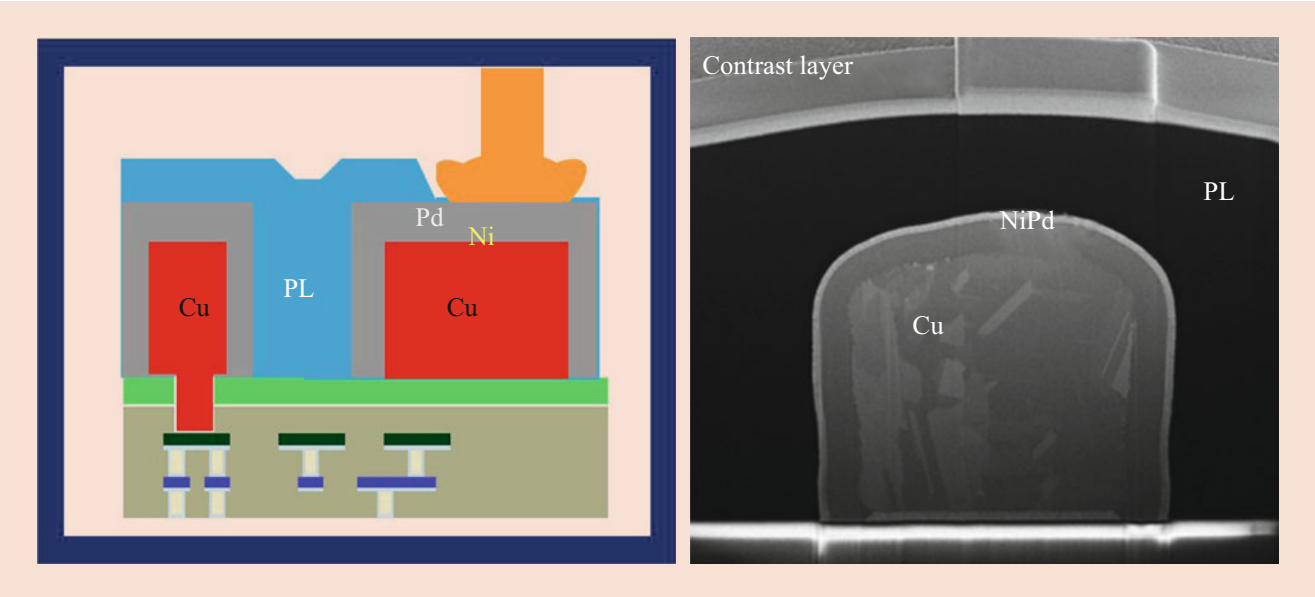

Fig. 3.25 Patterned thick copper + metallic coating

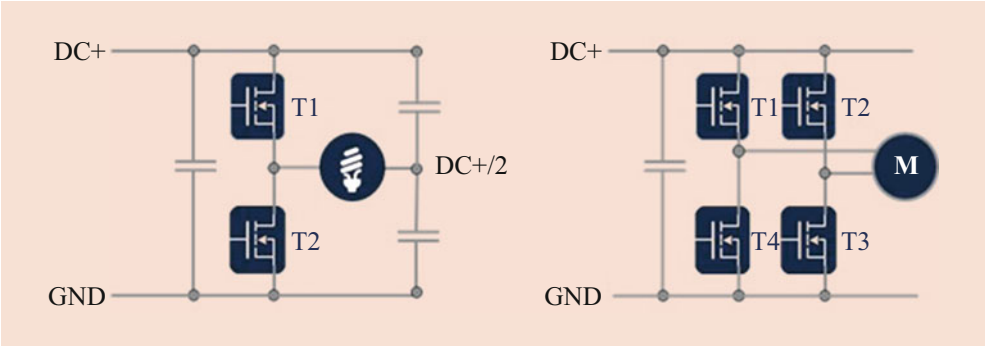

Fig. 3.26 Half bridge and full bridge topologies. Examples of lamp ballast and motor driver applications

BCD process generation was built starting from the CMOS baseline (Fig. 3.14) and the geometrical rules scaling coming from the new lithography node was bringing an overall area (and cost) reduction of all the integrated functions. On top of this reduction of area coming from the new generation, the introduction of some new features in the CMOS evolution enables the improvement of analog and power stages realization:

- Epitaxial substrate (P-/P+) offers the possibility to improve the isolation among the functions thanks to the low resistive substrate bulk.
- Reduced CMOS isolation spacing thanks to LOCOS evolution and STI integration allows the reduction of the high voltage devices drain region extension improving specific R_{on} [17].
- High energy implantation enables the possibility to introduce deep N-/P-type buried layers from the surface offering improved vertical isolation without dedicated epi growth.
- Thinner gate oxide and specific polysilicon layers improve CMOS analog key parameters (noise, matching) offering the possibility to realize precise stage without the need of high-performance bipolar devices.
- Self-aligned silicide (SALICIDE) module used to reduce CMOS access resistance offers the possibility to minimize source to body shared contact area in power devices.

In the early 2000s, 250/350 nm BCD process technology was announced by many integrated device manufacturer (IDM) players [18, 19], and at the same time 130/90 nm technologies were announced as latest CMOS technology platform [20, 21].

During the last 15 years, the speed of CMOS evolution has not changed significantly (new generation every 2 years) driven by high-performance and low power computing re-

Table 3.1 BCD9s (110 nm) main technology features

BCD9s (110 nm) main technology features		
Base options	CMOS	1.8 V CMOS Digital density ~ 130 kTransistors/mm^2
	Low voltage	5 V NPN, 5 V Zener 5 V poly capacitor Polysilicon resistors (600 **Ω** /square) FTP EEPROM
	Medium voltage	18 V isolated PNP 18 V Nch, 27 V Nch. 18 V Pch, 25 V Pch 30 V metal/metal capacitor
	High voltage	40 V NDMOS; 40 V diode 32 V Pch, 48 V Pch
	Metal levels	3 thin Cu metal layers: M1 pitch 0.3 μm, M2/M3 pitch 0.38 μm 1 thick Cu power metal: Thickness 10 μm, pitch 30 μm
High voltage options		60 V NDMOS, 80 V NDMOS,100 V NDMOS 60 V PMOS
R_{on} × area		40 V: 24 m**Ω** × mm^2
		60 V: 65 mΩ × mm^2
		80 V: 100 m**Ω** × mm^2
		100 V: 160 m**Ω** × mm^2

quirements sustained by new emerging applications (smart phone, data centers, communication infrastructure).

BCD technology evolution toward advanced CMOS nodes has been slowed down since the integration cost has increased significantly and the POWER IC applications' needs for digital capability have not increased at the same pace.

More recently the natural cost reduction of the manufacturing assets used for the advanced CMOS ASIC is enabling new BCD technology platforms (90/55/40 nm) offering a cost-effective solution for some applications requiring the integration of microcontrollers in a power IC.

Digital power management for mobile application processor, intelligent motor drivers for automotive and industrial markets, high efficient audio amplifier for car radio and mobile phone, mobile wireless charging systems, and novel USB power delivery systems are some key applications requiring high integration level including state-of-the-art microcontroller together with the possibility to drive low to medium power external loads.

Microcontroller is normally requiring a nonvolatile memory solution to store execution code and data. The need for a cost-effective nonvolatile memory solution has triggered the integration of different options depending on the product need in terms of programmability (number of write/erase cycles) and size.

- Dense One-Time Programmable (OTP) or Few-Time Programmable (FTP) Memory

  Low added mask solutions enabling dense one-time programmable (OTP) or few-time programmable (FTP) memory are obtained minimizing the number of extra process steps in the flow. Single poly memory cells are widely used for FTP solutions [22]: electrons are stored in a floating gate normally realized using same poly layer used for CMOS gate over the thicker gate oxide available in the process (the one required for I/O realization). This solution is widely used since no dedicated process steps are required. Different solutions [23] have been recently presented to overcome the potential charge retention challenge for latest technology platforms given the I/O MOS voltage rating scaling and consequent gate oxide thickness reduction (≤50 A).

  Anti-fuse/fuse approaches are widely used for OTP realization.

  Anti-fuse-based memory uses an insulating layer as storage element: process gate oxide is the most popular solution. In the natural nonprogrammed state, the electrical conductance is very low. Gate oxide breakdown is the physical mechanism used for programming: a voltage pulse is applied to induce the dielectric breakdown with the consequent irreversible increase of the electrical conductance. Thanks to the gate oxide scaling, this solution has recently gained a lot of traction since the programming voltage requirement has become compatible with the existing CMOS voltage capability: gate oxide breakdown voltage (V_{bd}) has become lower than CMOS drain to body junction breakdown (BV_{dss}) simplifying the programming circuitry.

  Electric fuse-based memory is using process conductive layers as storage elements. Silicide poly or metal layers are widely used: in the natural not programmed state, the layer electrical conductance is high. The physical mechanism used for programming is the atom migration induced by an electrical pulse (electromigration):

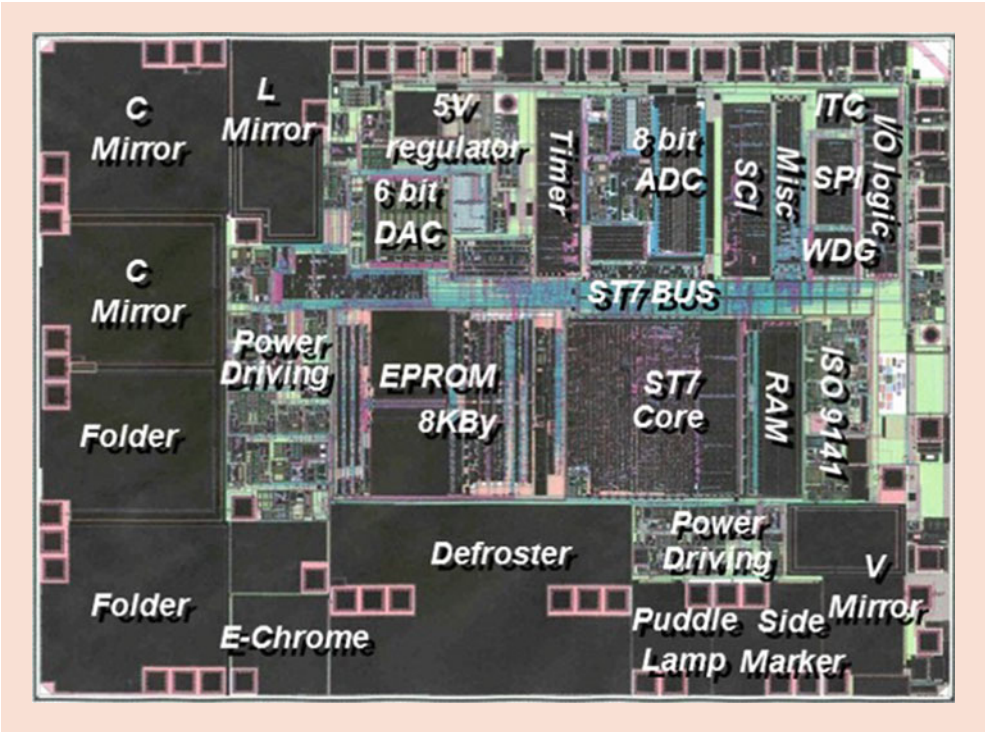

Fig. 3.27 Single-chip solution embedding microcontroller with embedded NMV (BCD5 technology)

the memory is programmed by applying a current pulse leading to an irreversible conductance drop. One of the key challenges of these fuse solutions is the applied power pulse control to avoid local melting inducing physical damage to the involved layers (conductor and surrounding insulating layers) that may lead to some potential conductance instability during the product lifetime. Recently a fuse solution based on silicide material migration assisted by the local electrical current/temperature during the programming pulse has been presented [24]: this solution should secure a wide conductance variation in the silicided poly layer without any physical damage creation.

The solutions described for OTP and FTP realization are not requiring specific process steps, and therefore they are offering a cost-effective solution to embed nonvolatile memory array up to 32/64 kBytes with a maximum number of write/erase cycles in the 1 k (1000) range for FTP memory.

- Nonvolatile Memory (NVM) Based on Dense Floating Gate Transistors

  This solution has been widely shared and used by many players. In Fig. 3.27 a picture of a complete system on chip (SOC) realized on an older technology node by STM is reported. EEPROM (128 Bytes) and EPROM (8 Bytes) were integrated to serve as microcontroller memory in a complete motor driver chip serving automotive market. More recently, Infineon announced dense NOR flash integration in its proprietary 130 nm BCD generation [2] targeting single-chip solution embedding high-performance microcontroller with power drivers for automotive applications (window lift, power seats, sun roof, etc.). RENESAS announced the integration of 1T MONOS flash cell in an advanced 90 nm BCD technology [4] addressing array up to 512 kBytes [25].

  Other players have recently announced dense flash memory capability in their latest BCD technology platform such as Global Foundries (split-gate SST solution on 130 nm BCD [26]) and ROHM (dual poly NOR flash on 130 nm BCD [27]).

  Integration of a dense and high-performance flash-based NVM is offering a mature solution requiring the introduction of specific process steps: tunnel oxide, dual poly, constraints on high voltage circuitry for memory programming/erasing, and specific needs of sealing layers for data retention.

  These extra steps are increasing the wafer cost putting some integration challenges especially in more advanced nodes because their impact on baseline CMOS performances could be meaningful, requiring potential redesign of libraries/IPs or additional process steps/modules that are making the integration cost even larger.

- Nonvolatile Memory (NVM) Based on Different Storage Mechanism

  In the last decade, different storage mechanisms have been investigated to offer an alternative solution to flash NVM allowing better performance (power, speed, density) and lower integration cost. Resistive RAM (ReRAM),

magnetic RAM (MRAM), and phase-change memories (PCM) are today gaining a lot of traction for advanced CMOS embedded solution thanks to the achieved performance and to their integration scheme. Indeed, they are integrated in BEOL of the process after the formation of the transistors having an almost negligible impact on the devices' performance. At the same time, they are not requiring large voltage for the programming operations and therefore no specific high voltage devices are needed.

One of the major challenges for these novel memory solutions is the data retention at high temperature exposure such as the product soldering in the final application board and the operative junction temperature peak typical of power ICs.

Resistive RAM memory [28] is realized with a metal/oxide/metal capacitors using resistive switching as physical mechanism for its operations. Memory operation is secured by the creation of a conductive path between the two electrodes by specific voltage pulse (forming). Once this path is created, switching among two stable states (high resistive/low resistive) is controlled by proper program/erase voltage signals. The choice of the materials for the realization of the electrodes and the insulator is key for the onset of the memory effect. Recently Adesto [29] has shown the evolution of a specific ReRAM flavor (conductive bridge RAM) to automotive compliant thermal profile with a specific error correction code scheme guaranteeing 20 years of data retention at 150 °C.

In a magnetic RAM memory (MRAM) [30], the storage element is realized by a magneto tunnel junction (MTJ): two magnetic layers are separated by an insulator. The electrical resistance of such structure depends on the relative magnetization directions of the magnetic layers: its value is low when magnetization directions are parallel while it is high when they are anti-parallel. The magnetization of one of the two deposited layers is fixed, while the second layer magnetic state is free to be changed (programmed) using different physical principles. One of the first used mechanism for programming is the generation of a magnetic field induced by an electrical current flowing in a conductor realized with a standard level of metal. A second widely used solution, spin-transfer torque MRAM, is using the electron current spin flowing through the MTJ to change the magnetization polarity: in this case the electrical current value and direction determine the switching direction (0 ➔ 1 or 1 ➔ 0). The realization of the storage element is quite complex since it is requiring many different layers for the realization of the MTJ that has to be properly engineered to comply with specific reliability requirements for memory operation. Recently Intel announced MRAM capability reaching good data retention up to 200 °C [31] and Qualcomm/TDK has shown MRAM integrated CMOS platform for Internet of Things (*IoT*) application [32].

Among all the different solutions, PCM-based NVM seems to be the only one compliant simultaneously with automotive high temperature operative requirements (data retention of several years at 150 °C) and able to guarantee code integrity after soldering reflow thermal profile (260 °C peak temperature) [33].

PCM can be integrated in a typical BCD flow after contact formation (Fig. 3.28). A chalcogenide ternary alloy, $Ge_xSb_yTe_z$ (GST), is used as a storage element and a thin metallic layer is used as a heater. The data storage is secured by the presence of two stable states in the storage element: amorphous state associated with

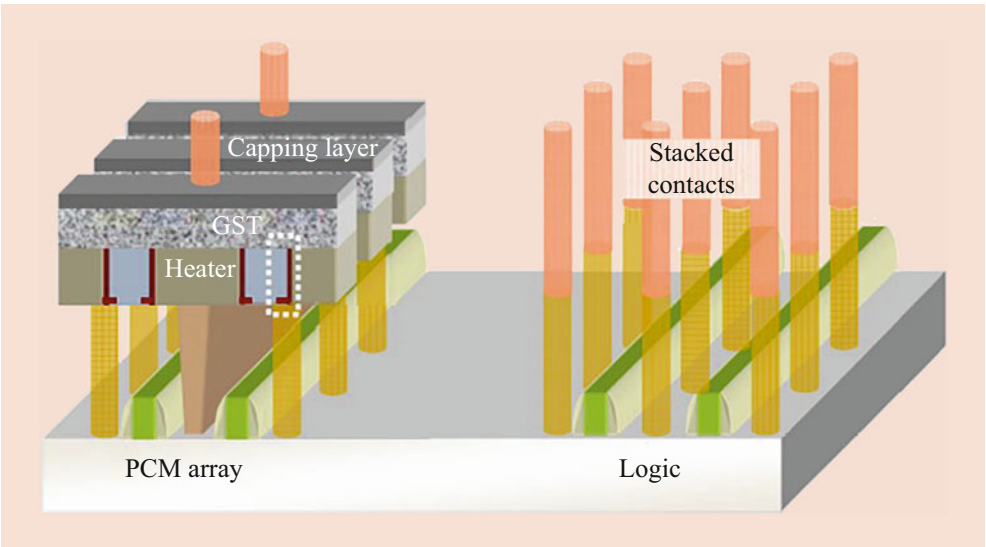

Fig. 3.28 Phase-change memory integration scheme section

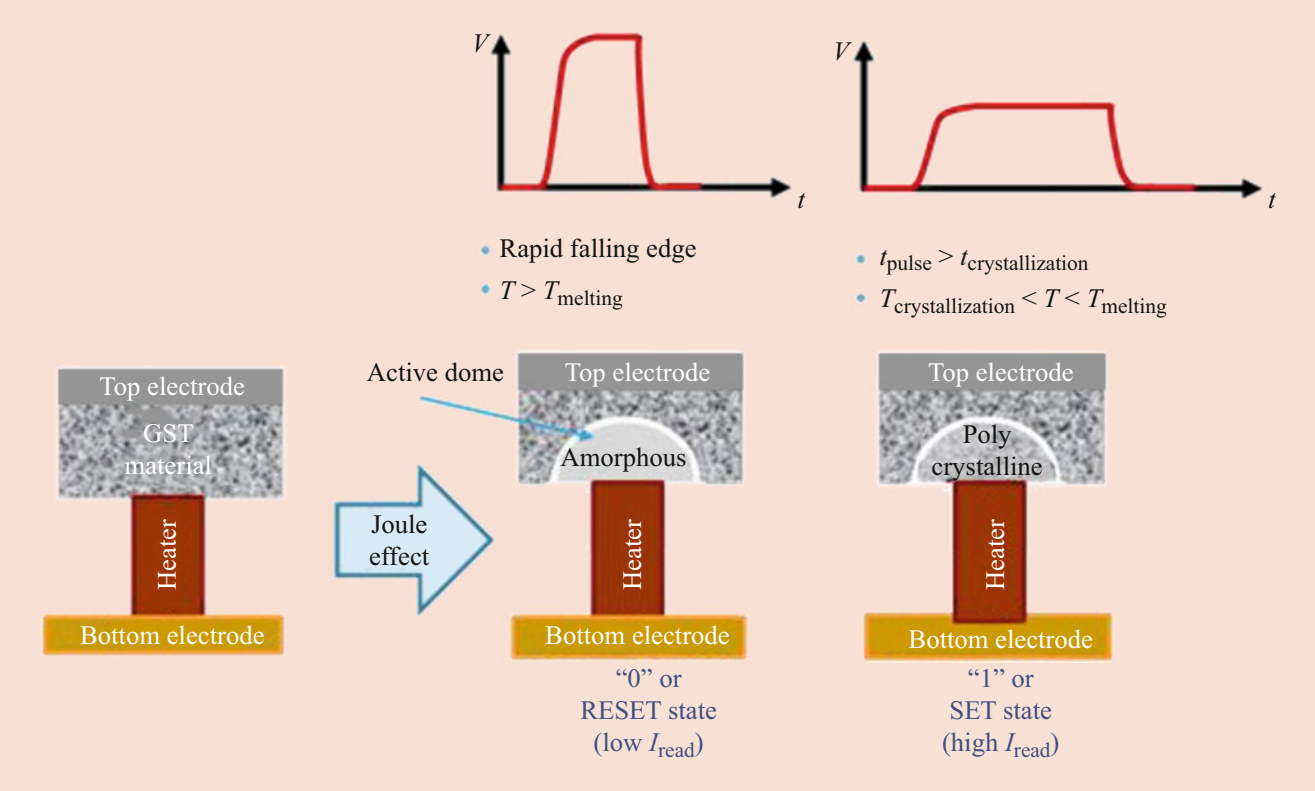

Fig. 3.29 Schematic representation of logic state 0 and logic state 1 in PCM cell

high electrical resistance (state 0) and a crystalline one with a low resistance (state 1). The switching between the states is realized with a tailored thermal pulse generated by the programming current flowing throw the heater. Baseline LV CMOS transistor is used as selector in the array realization (one resistor – one transistor).

Figure 3.29 shows a schematic representation of the PCM cell stack, with the top electrode, GST material, heater, and bottom electrode. In the active dome of the GST, an amorphous or crystalline status is generated depending on the local temperature reached as a consequence of the electrical pulse applied.

PCM is therefore able to secure a cost-effective approach to integrate a high-performance NVM scalable for future generations and compliant with the harsh BCD technology product temperature profile.

This integrated solution offers the possibility to embed in the same die all the functions needed to realize fully integrated system-on-chip IC (Fig. 3.30).

In Figure 3.31 a complete motor control system is shown in its evolution: from the simplest architecture (one full bridge in BCD1) to the full system integration (two full bridges, six external power drivers, ARM CortexM4 with 32 kBytes NVM based on PCM) in a smaller silicon area.

All these development activities currently running on quite advanced CMOS nodes (40 nm and below) may bring alternative competitive NVM options portable in the future on advanced BCD technology enabling the integration of more complex system on chip.

3.4.2 Power and HV Evolution: Device Architecture

Power devices are key elements of any smart power ICs: since the very early stage, they have been widely used to act as switch between supply and external loads. DMOS transistors have been integrated replacing bipolar devices thanks to their capability to deliver larger power to the external world given the wider safe operating area (no second breakdown) and reduced driving current consumption.

Originally vertical DMOS structure (Fig. 3.32) was integrated leveraging the power discrete structures and the availability of some key modules (high-doped buried layer and sinker) from bipolar technology. This integration scheme was built on N-type epi layer acting as drain extension to withstand the voltage: thickness and doping/resistivity were fixed by the highest voltage devices penalizing the performance of the lower voltage one. At the same time, a passive

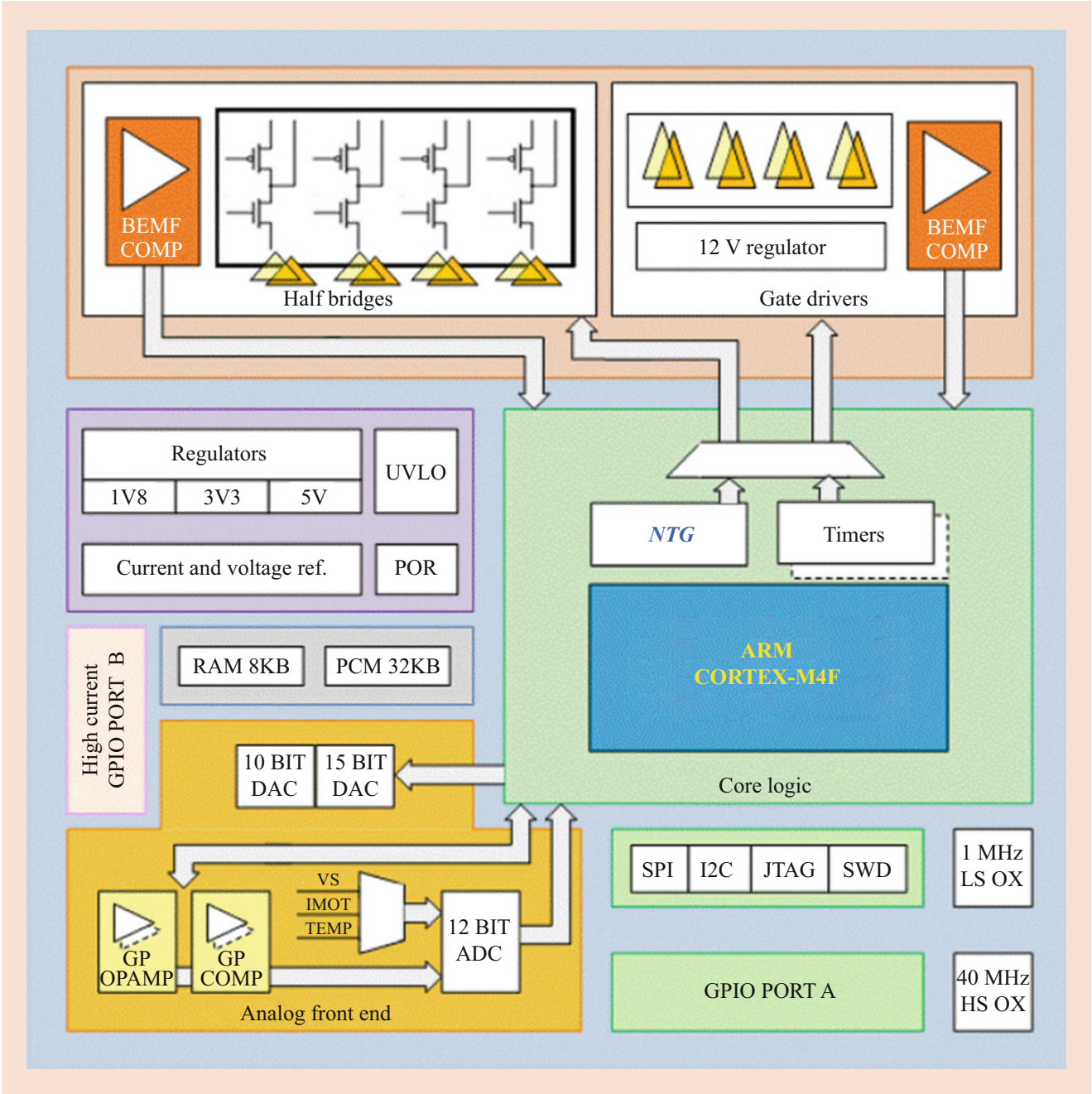

Fig. 3.30 Integrated complete motor control system block diagram

resistive path realized with N+ buried layer and N sinker was present to collect the current at the chip surface: this extra path was increasing the overall specific on resistance.

Lateral DMOS structures have become the standard architecture for power realization since the mid-1990s overcoming the limitation described above. In Fig. 3.33, a schematic cross section of a lateral N-type high voltage DMOS device is shown.

In this structure the current is flowing laterally between drain and source terminals.

Drain region is realized with a lightly doped N-type layer: doping level, drain extension length, and depth are tailored according to voltage capability. Higher doping and reduced length are securing a lower electrical resistance together with a reduced blocking voltage due to higher electric field.

Body region doping profile is another key element for the device realization. An optimum has to be fixed to meet threshold voltage and channel length requirements (the smaller, the better) avoiding the onset of source to drain anticipated breakdown coming from short channel

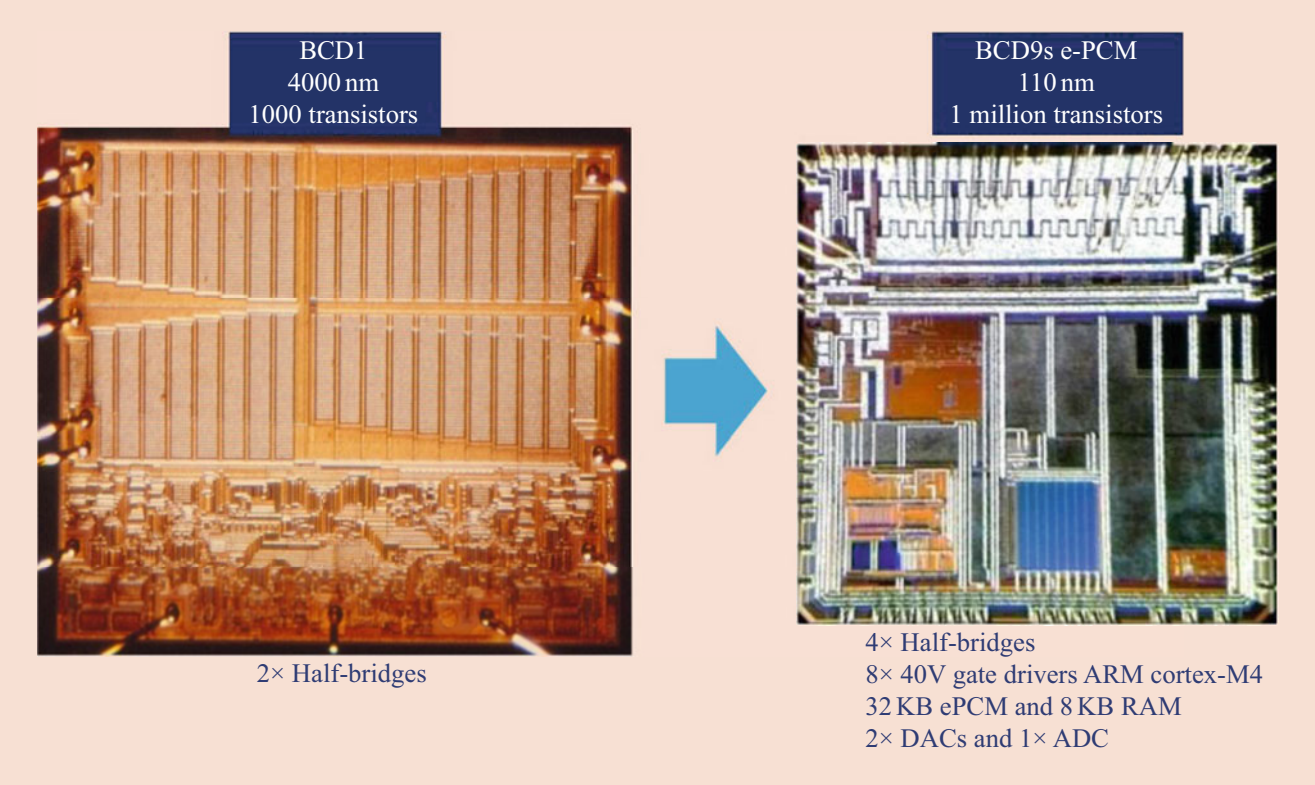

Fig. 3.31 Motor control evolution: from the simplest architecture (one full bridge in BCD1) to the full system integration (two full bridges, six external power drivers, ARM CortexM4 with 32 kBytes NVM based on PCM) in a smaller silicon area

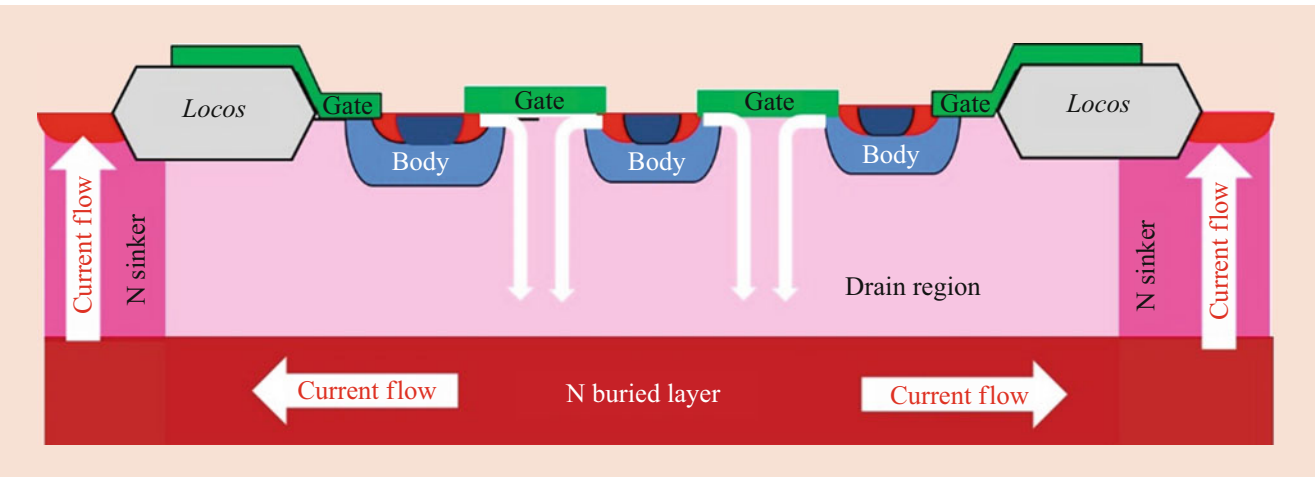

Fig. 3.32 Vertical DMOS schematic cross section

effect (punch-through). Specific care must be taken to avoid intrinsic parasitic NPN (source/body/drain – Fig. 3.19) turn-on triggered by multiplication current during device high voltage operations. For this reason, specific implant may be added to minimize the bipolar intrinsic base resistance.

In this architecture adopted for a very wide range of rating voltages, gate and drain terminals are isolated from each other by a thin oxide region usually realized with the gate oxide and by a thick oxide layer normally using the CMOS isolation module or a specific customized one as it will be detailed in the coming paragraph.

Overlapping polysilicon gate acts as a field plate to reduce the electric field at the body/drain junction. For higher voltage device, metal layers can be used to realize multi-planar field plate securing the high blocking voltage.

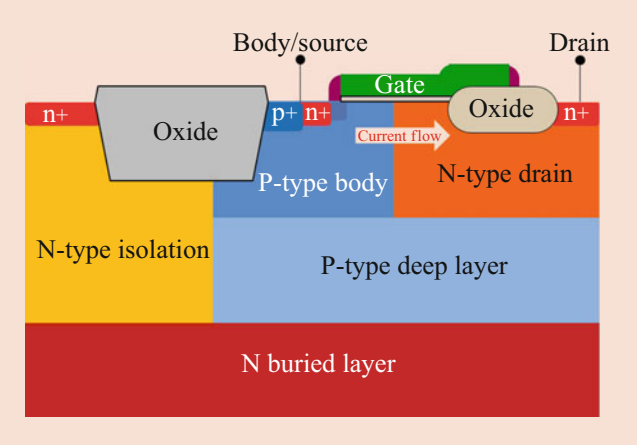

Fig. 3.33 Lateral N-type high voltage DMOS schematic cross section

N-type buried layer is present to provide a vertical isolation between the body and the P-type substrate. A deep P-layer underneath the drain can be present (as in Fig. 3.33) to isolate the drain terminal from the substrate allowing negative voltage operations.

CMOS N+ and P+ layers are used to realize drain, source, and body connection: body and source terminals are locally shorted to minimize the intrinsic NPN parasitic resistance.

Key electrical parameters for power switch devices are the voltage capability usually identified with the off-state drain to source breakdown voltage (BV_{dss}) and the specific on-state resistance ($R_{on} \times A$) that provide a direct measurement of the voltage drop and of the amount of power dissipated by the device when it is delivering the current to the load.

A trade-off between BV_{dss} and $R_{on} \times A$ has to be found with a proper architecture design solution since larger doping level required to minimize on-state resistance leads to a reduced blocking voltage.

Several models have been derived during the years describing the relationship between $R_{on} \times A$ and BV_{dss} for an ideal power device with different assumptions on the electrical profile in the drain extension region [34].

Basically a power law relationship is described:

$$R_{on} \times A = a \times BV_{dss}^{n} \quad (1)$$

This equation is related to the drift region layer, neglecting the channel and contact regions contribution to the area of the devices. This assumption is quite correct for higher voltage rating devices, while it can lead to a meaningful deviation for the lower voltage devices (60 V and below).

On standard CMOS technology at least down to 32/45 nm technology node, device scaling leading to continuous performance improvement has been achieved together with a supply voltage reduction securing same electric field across the elementary device [35].

On power device, supply voltage is strictly coming from the application requirements, and it has not changed during the years.

Automotive battery voltage is fixed since a long time (12 V), and the application-specific requirement (load dump) has been secured by a 40 V rated power since the very early stages.

Power stages requirement for laptop and data centers hard disk drivers is 20 V being limited by the supply line (12 V). All mobile applications are normally powered by battery systems: 5 V max supply has to be secured but larger current management is normally causing severe voltage spike bringing the power device requirement up to 8–12 V.

For audio applications, the voltage specification is driven by the loudspeaker power requirement: 20–60 V rated devices are needed.

In Fig. 3.34, the evolution of $R_{on} \times A$ for a 40 V rated power N-channel device is reported. Almost a factor 7 in reduction has been achieved keeping same voltage capability in the last 20 years corresponding to an average performance improvement close to 25% per each generation. For this specific voltage rating, the size reduction benefit from the new lithography generation capability is limited to the device contact regions; therefore, the performance improvement secured by the geometry scaling is really limited. Several architectural changes to the key device bricks have been adopted to sustain this continuous improvement in the new generations.

Body Region

The channel region contribution has been originally reduced thanks to the lower gate oxide thickness (i.e., larger inversion charge at fixed V_{gs}) and reducing continuously the channel length. Self-aligned large angle tilt body implant (Fig. 3.35, [36]) after gate polysilicon edge definition has been introduced in the late 1990s to tailor the body doping profile securing the amount of charge to prevent premature drain to source punch-through onset with a reduced channel length. At the same time, the lack of a dedicated high temperature step, originally used to diffuse the boron implant under the polysilicon gate, has assured the compatibility with advanced CMOS enabling the realization of power stages with thinner gate oxide.

In more advanced technology generations, thanks to the availability of new lithography tools with more accurate overlay control, body region can be realized adopting specific doping implant before polysilicon gate definition in a not self-aligned approach. Existing CMOS body wells can be used to save masking and implant steps paying specific care to the sub-surface doping vertical profile (body resistance pinched by source layer).

In a power device, the body region is the base terminal of an intrinsic NPN bipolar device that can be triggered by the

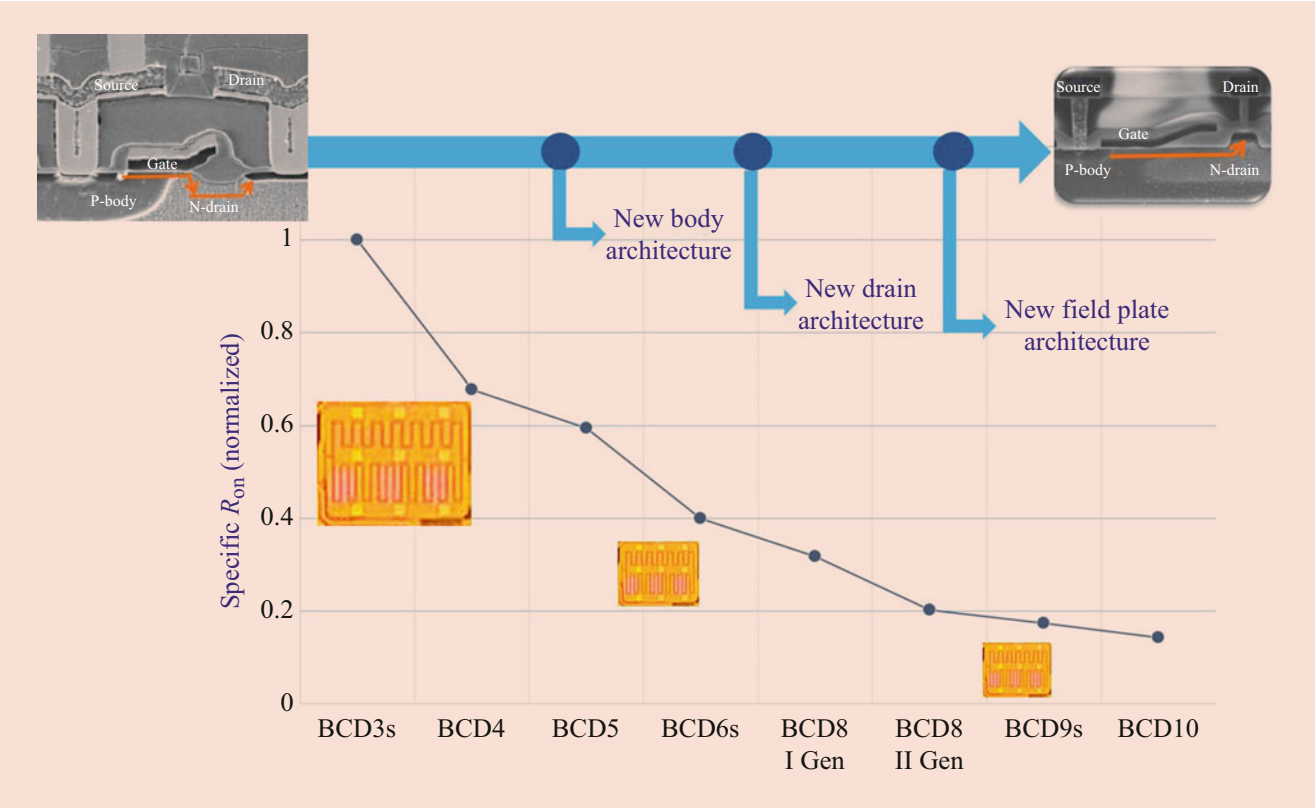

Fig. 3.34 ST BCD technology 40 V N-channel device specific R_{on} improvement in the latest generations. Value normalized to BCD3s (1 μm) technology

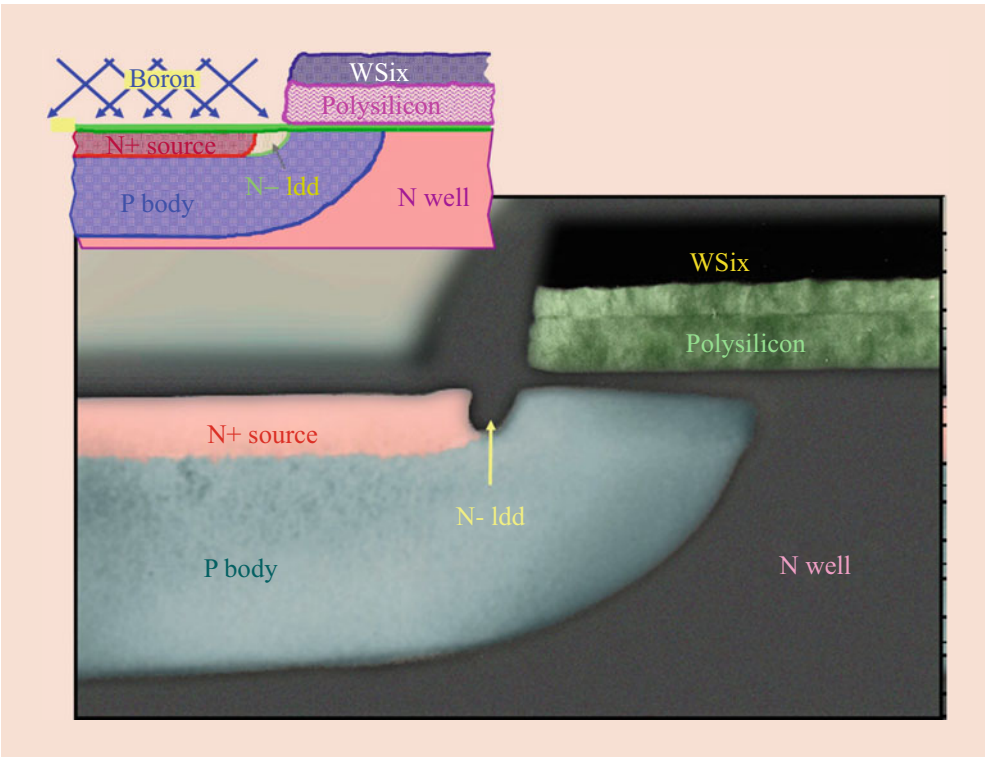

Fig. 3.35 Large tilt body implant realization in BCD5 ST technology. TEM detail of the body/source region

multiplication current present in the device when high drain to source voltage is applied in on-state operations ($V_{gs} > V_{th}$). The trigger of this bipolar transistor leads to device fail, and it limits the safe operating area (SOA). Body and drain regions must therefore be engineered to secure a wide SOA compliant with the required voltage capability: dedicated body profile has been proposed [37] to reduce the bipolar intrinsic base resistance.

When CMOS wells are used for the body realization, specific tailoring to the surface (IMP1 in Fig. 3.36) and subsurface implant (IMP2 in Fig. 3.36) can be carried out to increase the high voltage device SOA.

In the latest generations, the availability of LV CMOS devices using large tilt HALO/pocket implant at LDD (lightly doped drain) level has offered the possibility to further modify and improve the body profile increasing the NPN trigger current and minimizing the short channel effects with a self-aligned approach. In Fig. 3.37 a schematic cross section of the high voltage device source/body region is reported: the boron-doped pocket layer (HALO) is increasing the doping level under the body leading to a larger threshold voltage down to very short channel length.

Different strategies have been adopted for the realization of the body to source contact region to optimize the trade-off between two requirements:

- The electrical connection between the body and the source must secure minimum electrical contact resistance to avoid SOA penalization minimizing the NPN intrinsic bipolar base resistance.
- Body region size reduction to maximize channel density (i.e., effective width integrated in the unit area).

Self-aligned silicide (*SALICIDE*) introduction starting from 350 nm technology has enabled the possibility to improve the resistance minimizing the size needed for the connection (see Fig. 3.38): P+ contact region is placed in the middle of the body opening region and is shorted with the source layer thanks to the silicide layer.

The scaling of the body opening dimension is limited by the requirement of low resistance value associated to this region. Therefore new lithography generation would bring negligible gain, and different body region solutions have been proposed to overcome this limitation.

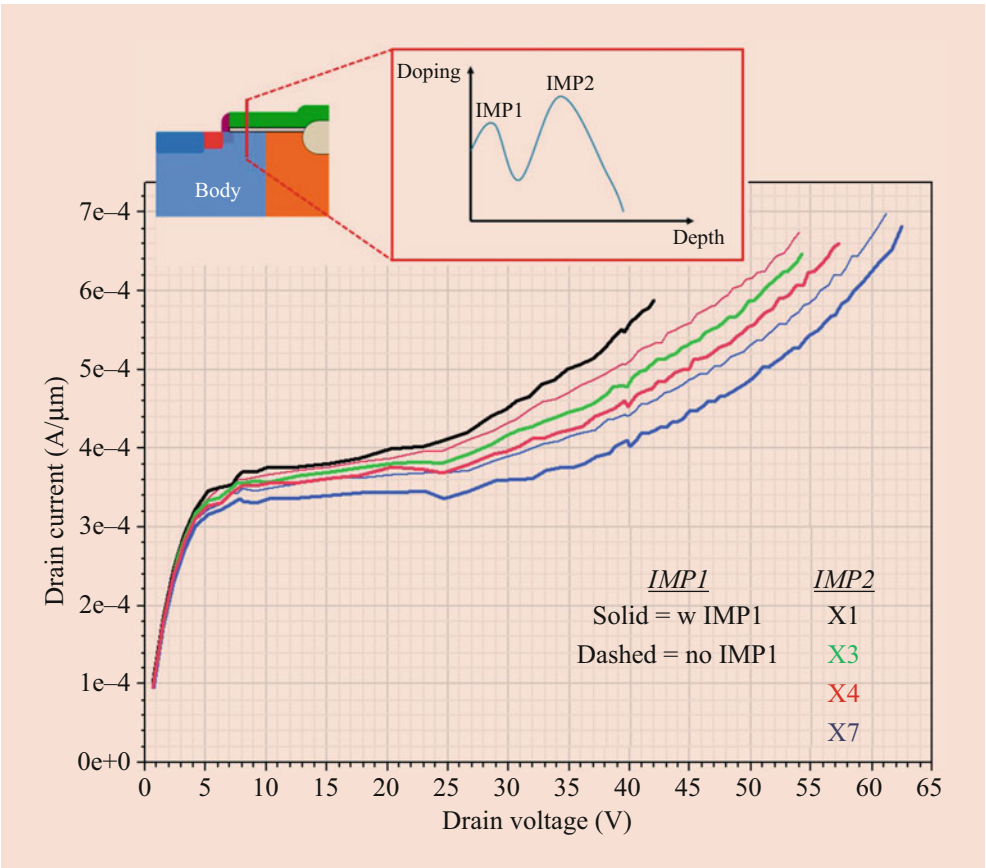

Fig. 3.36 High voltage device output characteristic. Impact of different body implant profile on safe operating area

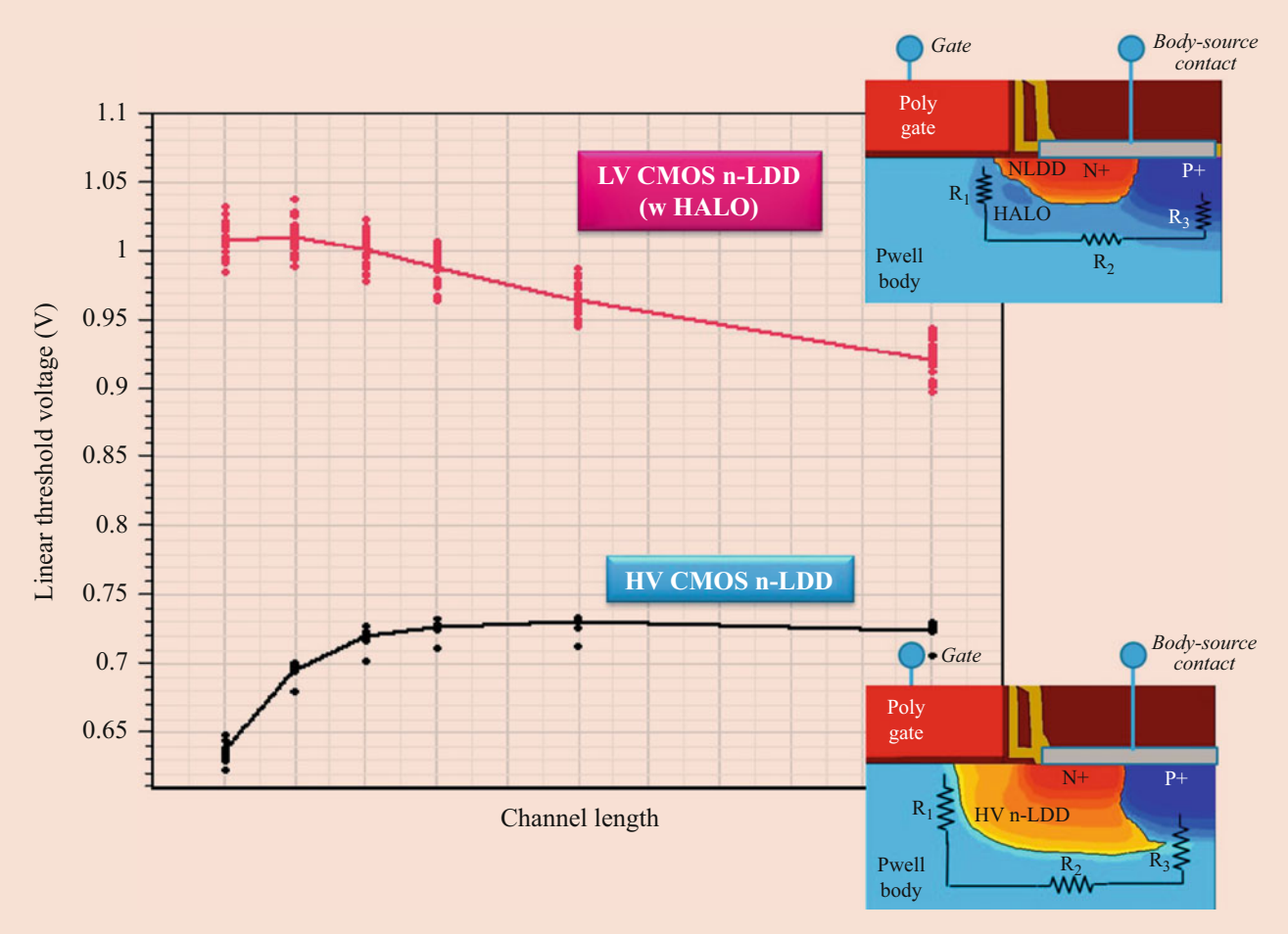

Fig. 3.37 (**a**) High voltage N-channel source/body junction profile under the poly edge: HV CMOS LDD (**b**) and LV CMOS LDD w HALO implant (**c**) and (**d**) Device threshold voltage as a function of channel length for the two different bodies

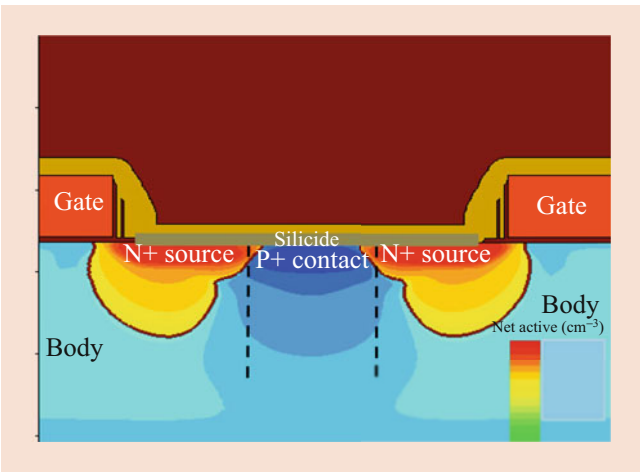

Fig. 3.38 Body to source contact region detail. A silicide layer is formed during the process securing a good conductive local connection between source and body contact areas

Alternating P+ and N+ strip across channel width (Fig. 3.39) reduces the device pitch: specific care must be taken in defining the minimum P+ area needed to avoid SOA penalization since this area is reducing the effective source width integrated penalizing device specific R_{on}.

Local connection through micro trench realization is today widely used in discrete power devices and may offer an interesting opportunity for reducing the device pitch, but dedicated process steps are needed for the realization leading to increased cost and complexity (Fig. 3.40).

Drain Region

The drain extension region plays a key role in the device realization: doping profile and geometrical dimensions are the parameters tuned during the development to optimize the performance according to the trade-off between voltage capability (BV_{dss}) and conduction losses ($R_{on} \times A$).

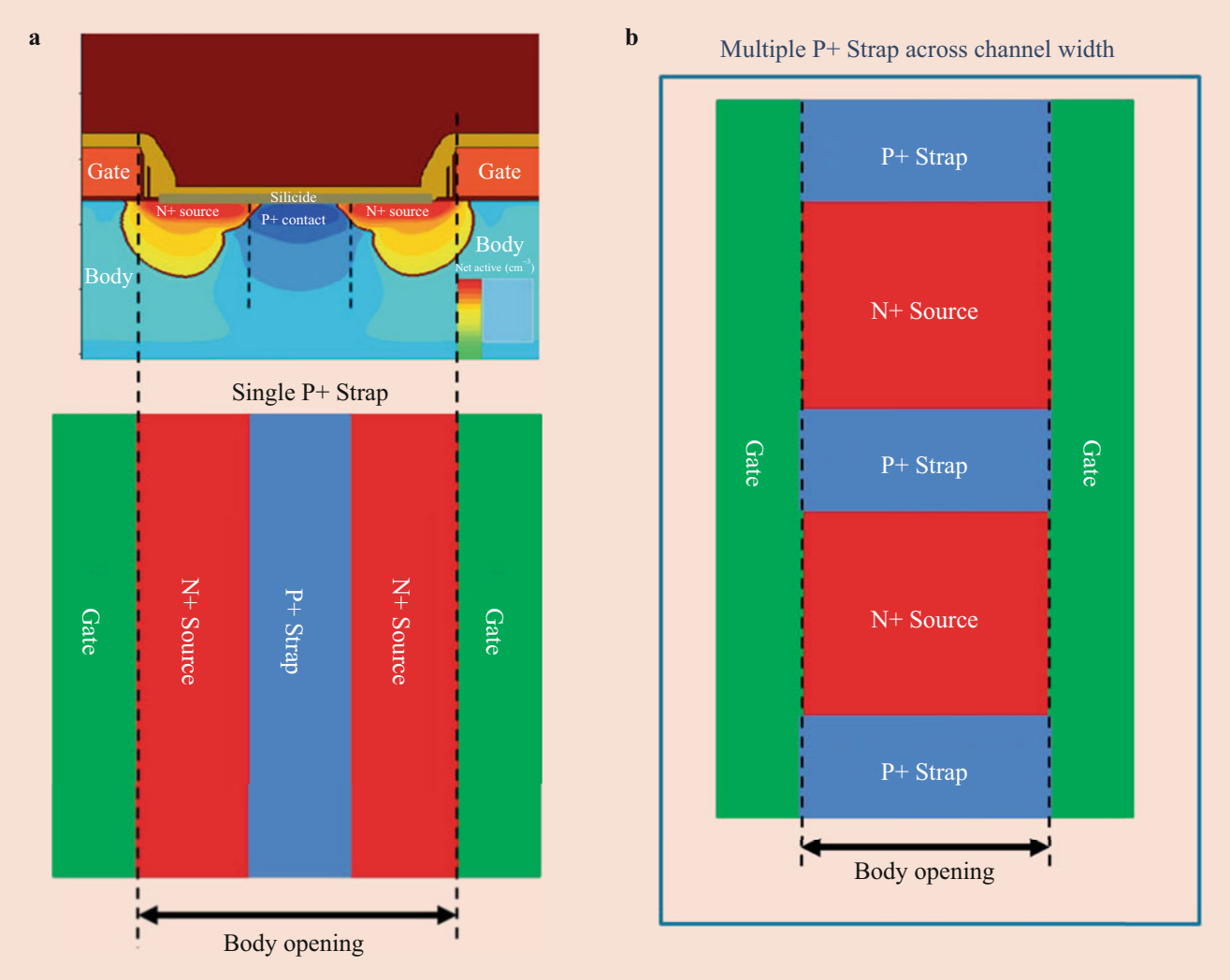

Fig. 3.39 Body to source contact region layout. (**a**) Single P+ strap. (**b**) Multiple P+ straps along channel width alternated with N+ source

RESURF technique is widely adopted to increase the drain doping level while keeping the same off-state breakdown thanks to the introduction of a vertical diode that enhances the depletion of the drain layer modifying the electric field profile [6]. In Fig. 3.41, a qualitative description of the P-layer impact is reported: thanks to the vertical P-layer drain diode effect a bell-shaped curve is obtained in the BV_{dss} vs drain dose plot.

Lower drain dose values are leading to lower off-state capability due to an electric field peak located at the drain region (red star) caused by the potential lines crowding in the higher doped drain terminal.

Increasing the drain dose, the electric field peak location is moving to the conventional surface region close to the oxide transition region (orange star): an optimum (i.e., maximum BV_{dss}) is reached when a perfect balance between the electric fields in the two regions is reached.

Increasing the P-layer dose the optimum point, i.e., the drain dose leading to the maximum off-state voltage, is moving to larger drain dose level leading to a device with same BV_{dss} but reduced $R_{on} \times A$ thanks to the increased doping level.

The limitation to the P-layer dose is given by the onset of other hot spots in the structure such as the vertical P-layer to N-type buried layer diode (Fig. 3.42). The multiple RESURF solution has been proposed during the years [34] with the purpose to maximize the depletion effects leading to an ideal electric field distribution with the maximum drain doping level.

Drain extension engineering is completed by the definition of the key geometrical parameters (see Fig. 3.43). Three main parameters play a role in the optimum device realization:

- Drain extension under thick isolation oxide (S in Fig. 3.43). Longer $R_{on} \times A$ gives benefit in terms of off-state voltage capability (larger BV_{dss}) independently of the region where the electric field peak is positioned.

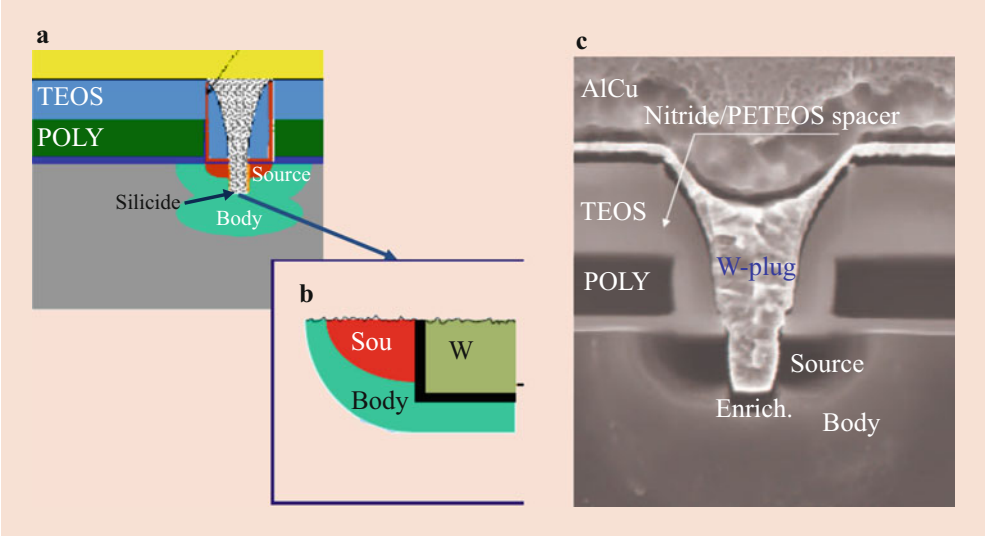

Fig. 3.40 (**a**) Schematic section of the Body to Source contact region in a Power Discrete device. (**b**) Zoomed view of the source and body diffusions with the contact region. (**c**) TEM cross section: local silicon micro trench is realized to secure the connection between the body and source terminals

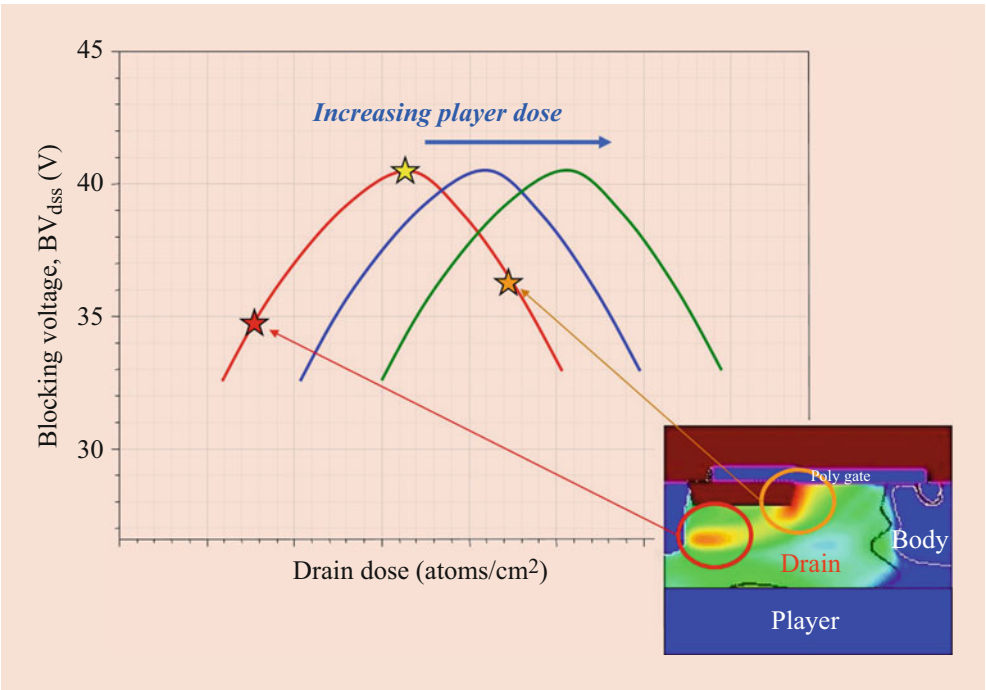

Fig. 3.41 TCAD simulation for off-state voltage (BV_{dss}) as a function of drain doping (dose) for a high voltage device with different buried P-layer dose for a fixed device geometry. In the inset, impact ionization distribution in the structure is reported

Clearly on-state resistance is penalized and the device is optimized by minimizing this value to secure the required voltage capability.

- Polysilicon gate overlap on thick isolation oxide (O in Fig. 3.43). Larger O reduces the electric field in the oxide transition region increasing BV_{dss} when the maximum avalanche generation is localized in this region. At the same time larger extension on the oxide may lead to a reduction of on-state resistance thanks to the accumulation of the drain region below. Too large extension increases the electric field on the drain side, therefore limiting the voltage capability due to the avalanche onset on the drain side. At the same time, the gate to drain capacitance is increased with an impact on the switching loss occurring during high-frequency operations. Optimum designs are generally looking to maximize this parameter since it plays a beneficial effect to mitigate some potential instability phenomena as it secures a "controlled" coverage of

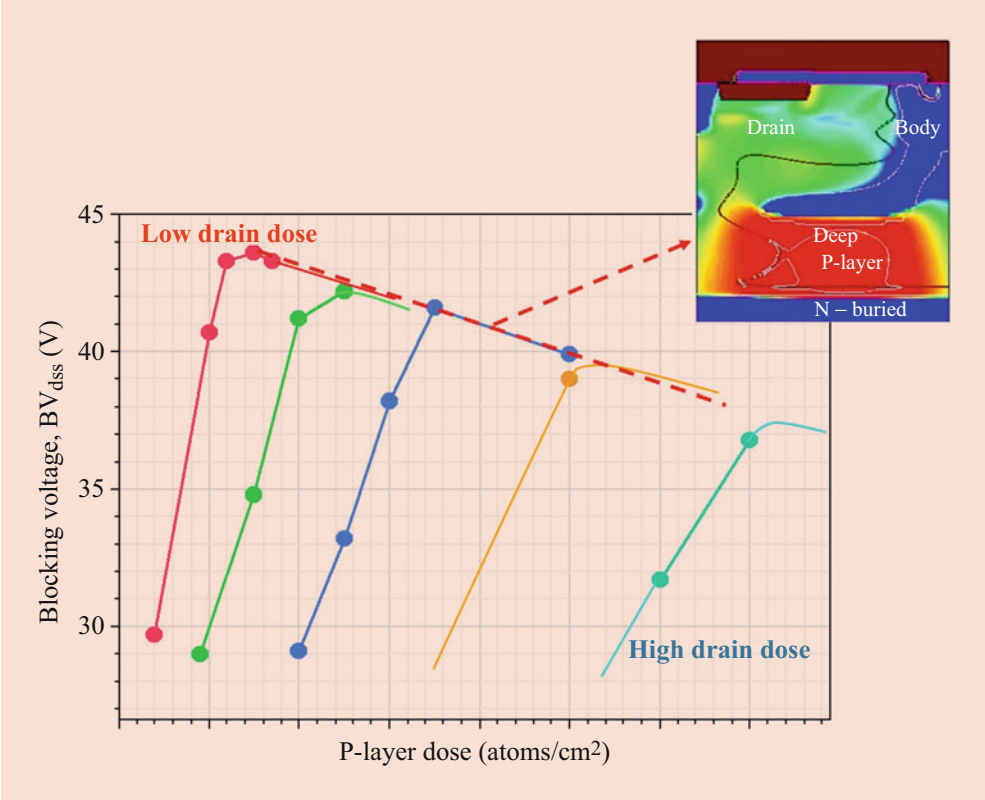

Fig. 3.42 TCAD simulation for off-state voltage as a function of P-layer dose for different drain doping for a fixed device geometry

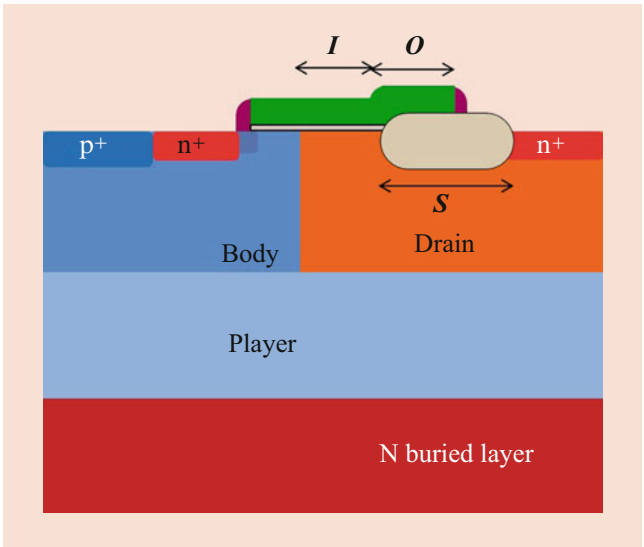

Fig. 3.43 High voltage lateral N-channel schematic cross section: key geometrical parameters highlighted

the drain extension region. This is particularly true for higher voltage rated device.

- Polysilicon gate overlap on drain in thin gate oxide region (*I* in Fig. 3.43). The reduced *I* value alleviates the electrical field in the transition oxide region thanks to increased drain depletion coming from the body/drain surface diode: BV_{dss} increase is therefore expected when the device is limited by this region hot spot (orange star in Fig. 3.41). At the same time, device switching loss benefits from the reduced gate to drain capacitance. *I* reduction is limited by the on-state resistance increase associated with the contribution related to the vertical current path. Indeed even in lateral device, a vertical current path is forced by the presence of the thick isolation oxide. Current flow section reduction is causing a sudden on-state resistance worsening when *I* is reduced (Fig. 3.44): the on-state resistance increase vs *I* is anticipated moving to lower drain doping level. Reduced *I* value is generally required for an optimum power switch but the scaling is limited by the on-state resistance increase. Both of these effects are strongly depending on the thick oxide region realization.

The availability of a deep P-type layer below the drain region enables the possibility to physically isolate it from the heavy doped buried layer (Fig. 3.45) thanks to a proper device edge construction. This configuration allows the usage of this device in all the power stages with limited negative supply rating: in fact the drain terminal can be negatively biased vs the grounded substrate provided that a proper (positive) bias

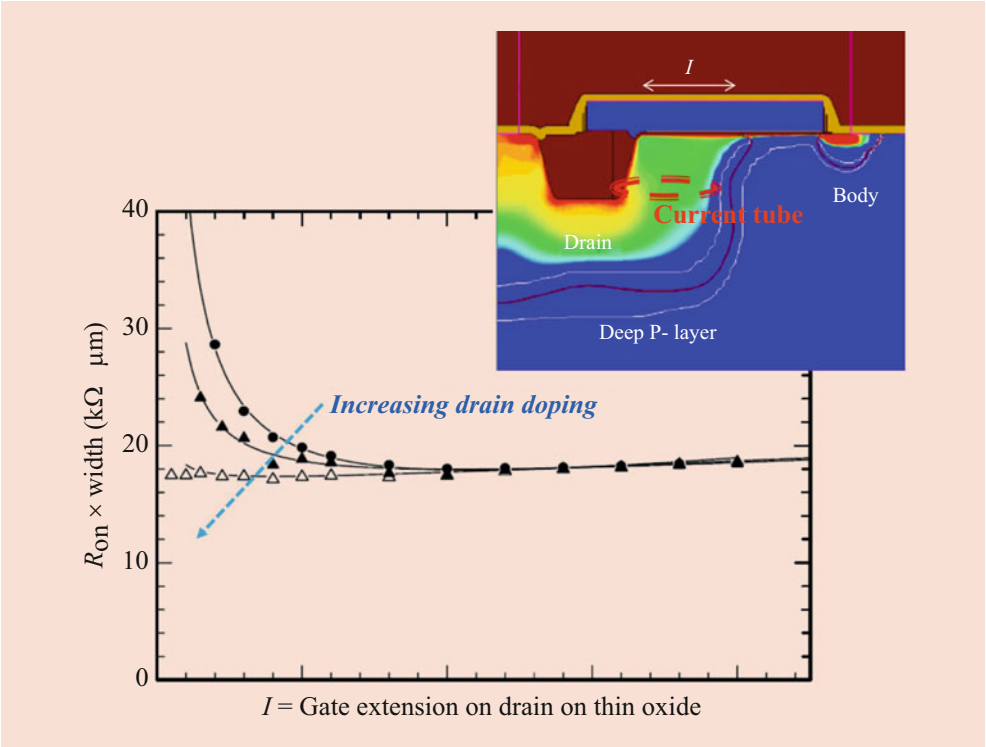

Fig. 3.44 Specific R_{on} as a function of I parameter for a 40 V rated lateral N-channel. Three different curves refer to different drain doping levels. In the inset current flow, color contour is reported when the device is biased in linear region

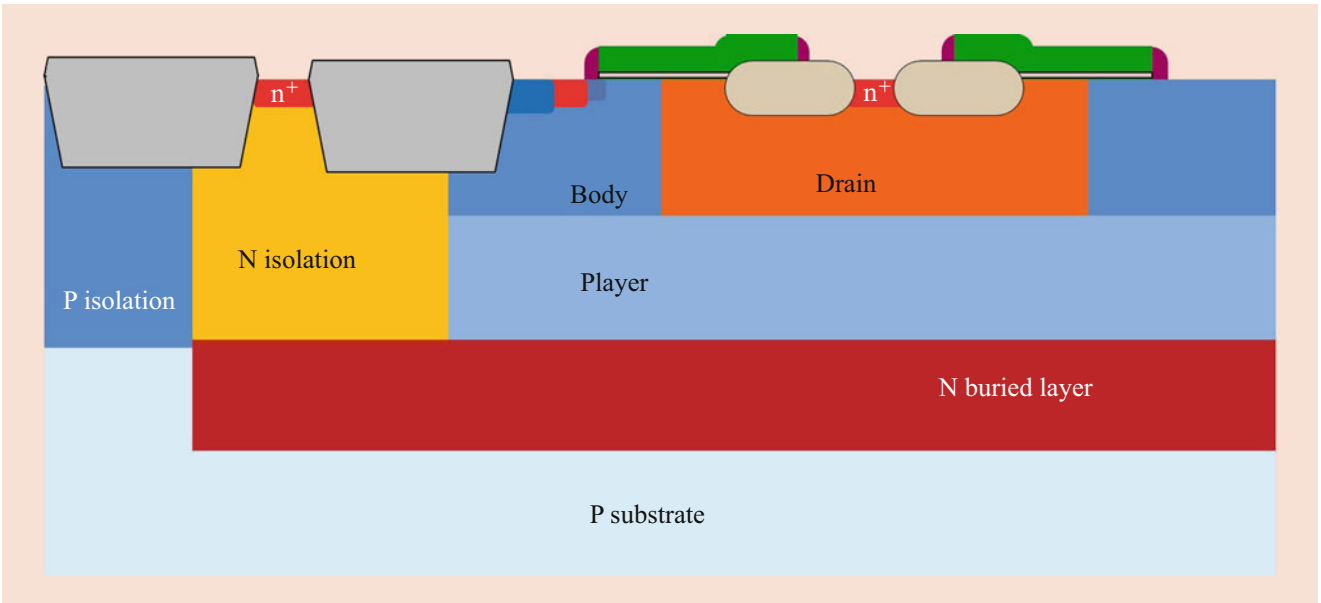

Fig. 3.45 High voltage N-channel isolated drain architecture. N-type drain regions are isolated by the N buried layer vertically by the deep implanted P-layer and laterally by a proper termination design

is supplied to the N-type isolation ring. The availability of an independent N-type isolation region offers the possibility to enhance the isolation capability during circuit operations.

More specifically in Fig. 3.46, some parasitic bipolar devices turned on during some transient period are highlighted in the inset. The availability of the isolation ring terminal can offer different possibilities in the power device stage design:

- N-isolation shorted to drain (blue line in Fig. 3.46). This is a standard situation for non-isolated device. In this

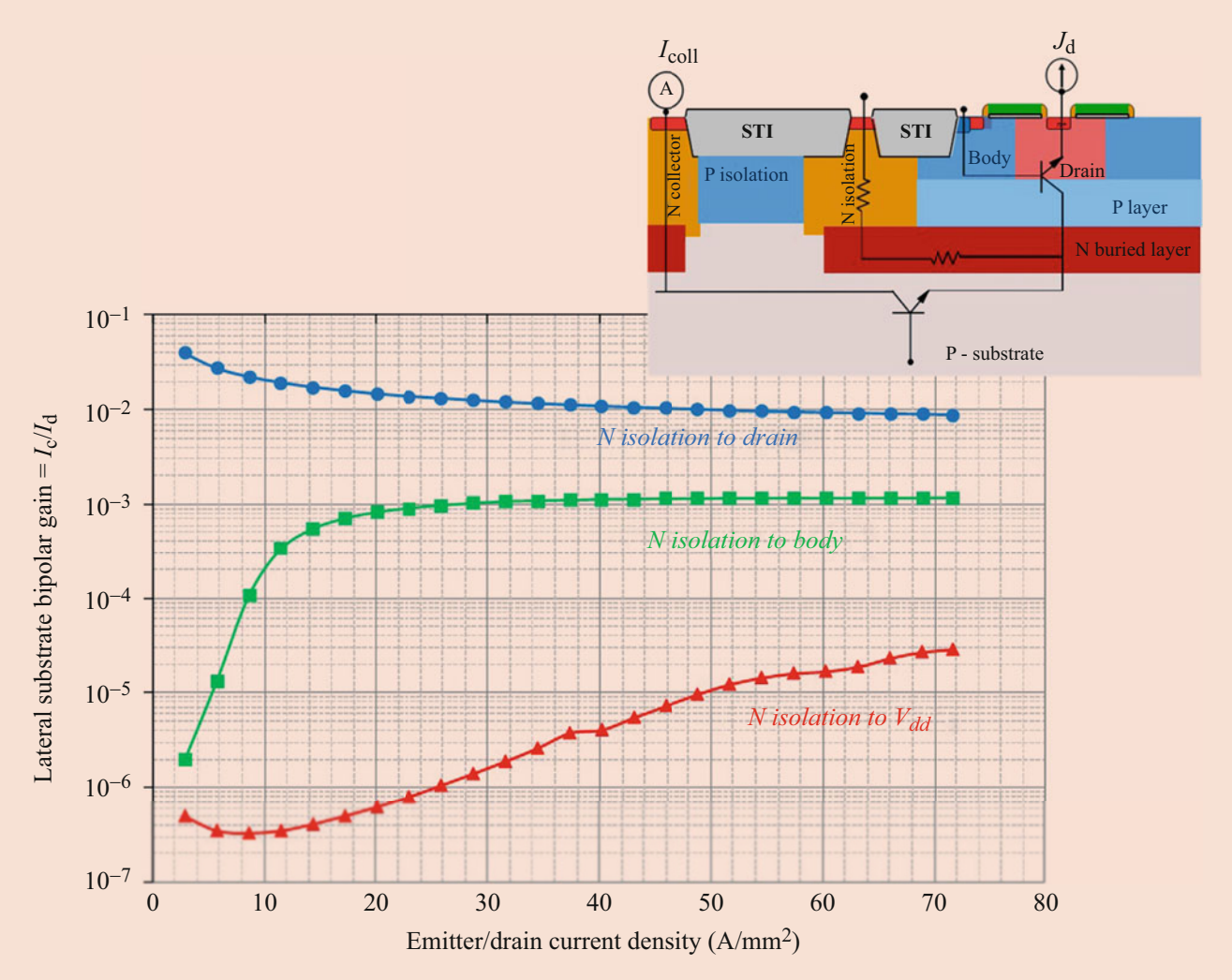

Fig. 3.46 High voltage N-channel isolated drain architecture: evaluation of external parasitic bipolar for different Isolation ring bias. Figure: collected current on an external pocket as a function of drain injected current density. Inset: architecture cross section with parasitic bipolar devices. (Reference: ST proprietary BCD technology)

configuration when drain terminal is biased negatively (vs source and substrate), a quite meaningful amount of current is collected by a neighbor device. The decay length is strongly dependent on the isolation architecture as shown in Fig. 3.11. This is clearly the most unfavorable connection strategy, but this solution may become mandatory when N-buried layer bias is fixed by overall device RESURF condition [38].

- N-isolation tied to high voltage supply (red line in Fig. 3.46). This is the most effective solution to protect the device closer to the power stage. In this configuration when the drain terminal is biased negatively, the internal NPN is turned on and the isolation region is acting as a collector. All the injected current is therefore locally collected with negligible impact on the region close to the power. To make this solution viable, the internal bipolar NPN safe operating area has to be carefully designed to secure no catastrophic event occurs during this period of large current/large voltage applied. The major drawback of this solution is the increased power dissipation when bipolar is turned on.
- N-isolation tied to body/source terminal (green line in Fig. 3.46). In the low current regime, this solution is equivalent to the previous one. However due to the internal collector electrical resistance (N buried layer and N isolation plug), the local N buried layer potential is dropping below ground turning on the lateral bipolar NPN and increasing the current collected by the external silicon region. Proper power device layout guidelines can increase the current level needed for turning on the external bipolar device: specific rules for sizing and placement of the N isolation plug are normally delivered for the optimum design depending on the application requirements. However this solution enables an increased level of protection without

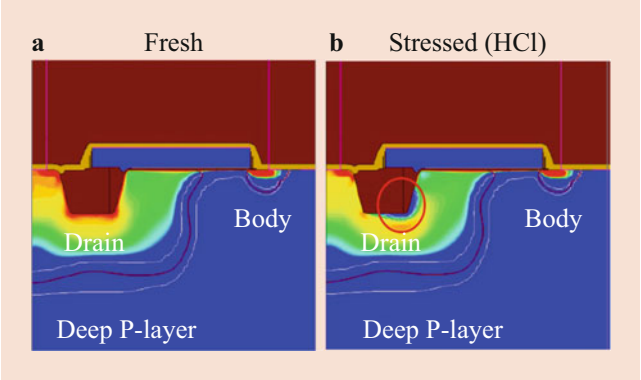

Fig. 3.47 STI terminated high voltage device linear current density plot. (**a**) Fresh device; (**b**) device after operation at high V_{ds} and intermediate V_{gs}. Red circle highlights the STI region where negative charge is trapped causing on-state resistance increase

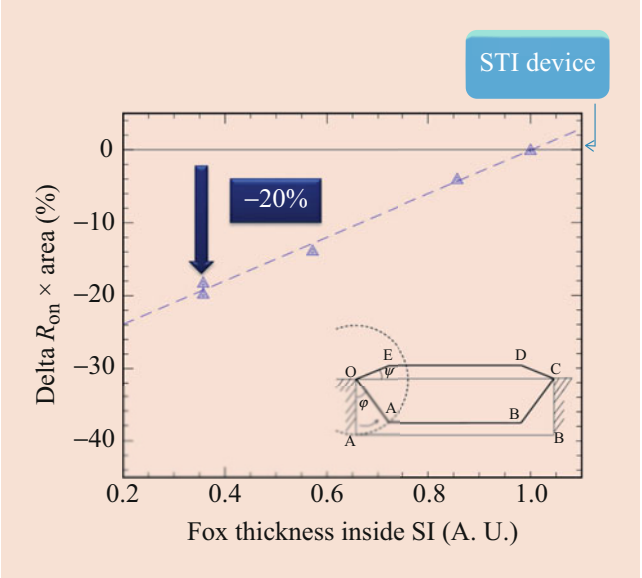

Fig. 3.48 Specific R_{on} reduction as a function of thick oxide penetration in silicon. Oxide thickness is kept fixed while moving the oxide out from the silicon starting from a vertical solution (STI like)

any power dissipation penalization and providing a faster diode recovery time.

Oxide Isolation Region

Thick isolation oxide layer is normally realized using the CMOS isolation module. The introduction of STI has given some benefits in the reduction of the drain extension length thanks to the vertical profile, but it has put a major reliability challenge for the realization of the high voltage devices [39].

During on-state device operations, when biased at high V_{ds} and V_{gs} above threshold, hot carriers are generated in the structure, and they may be injected in the gate oxide and/or generate interface states by de-passivating Si-H bonds [40, 41]. The resulting charge, associated with trapped carriers and charged interface states, modulates the drain extension width leading to an increase of the overall on-state resistance (Fig. 3.47). This phenomenon is adding a new constraint on the possible reduction of the accumulation region (*I* in Fig. 3.43) and further challenges for the device performance improvement.

To overcome this challenge, improved architecture has been presented in the latest year. Recessed gate structure has been recently reported as a viable solution to mitigate electric field at the STI bottom edge [42].

Dedicated customized thick oxide are widely adopted in many advanced BCD platforms. STI replacement with a dedicated oxide layer in power devices is mitigating the hot carrier-induced instability phenomena and is improving the device performance reducing the amount of oxide in the silicon leading to a reduced (vertical) current path. In Fig. 3.48 a theoretical analysis for a 40 V rated device is reported, keeping fixed oxide thickness: R_{on} reduction is reported as a function of the depth oxide into silicon.

While the benefits on devices' performance are evident, this solution has a few integration challenges.

Extra process steps are needed, and at the same time the compatibility with advanced CMOS process flow has to be carefully managed: in Fig. 3.49 an example of integration is presented in a 160 nm technology platform by STM [43].

A dedicated LOCOS module is realized just after STI realization: a dedicated nitride layer is patterned to protect the STI defined regions enabling the realization of the thick oxide layer in the power device. Thanks to the different profile, during high voltage operation, the electrical current flows "far" from the surface mitigating the hot carrier-induced instability (Fig. 3.50, [44]). This solution has enabled the realization of high-performance power device securing a meaningful scaling vs the previous generations.

Given the limitation coming from the latest CMOS isolation module (STI), the power device architecture has been therefore revisited with the final aim to continuously improve the performance while securing the long-term reliability and a wide safe operating area (SOA).

The gate to drain isolation region module has been re-engineered moving to a planar fully emerged power device architecture to further boost power performance scaling providing a straight current path between drain to source minimizing $R_{on} \times A$.

Within this framework, alternative device structures originally exploited for different voltage rating and usage have been re-engineered looking for an improved trade-off between integration cost and performance.

1. Planar dual oxide architecture with a tailored drain extension region (Fig. 3.51) covered by poly gate has been introduced since many years as the optimum solution for

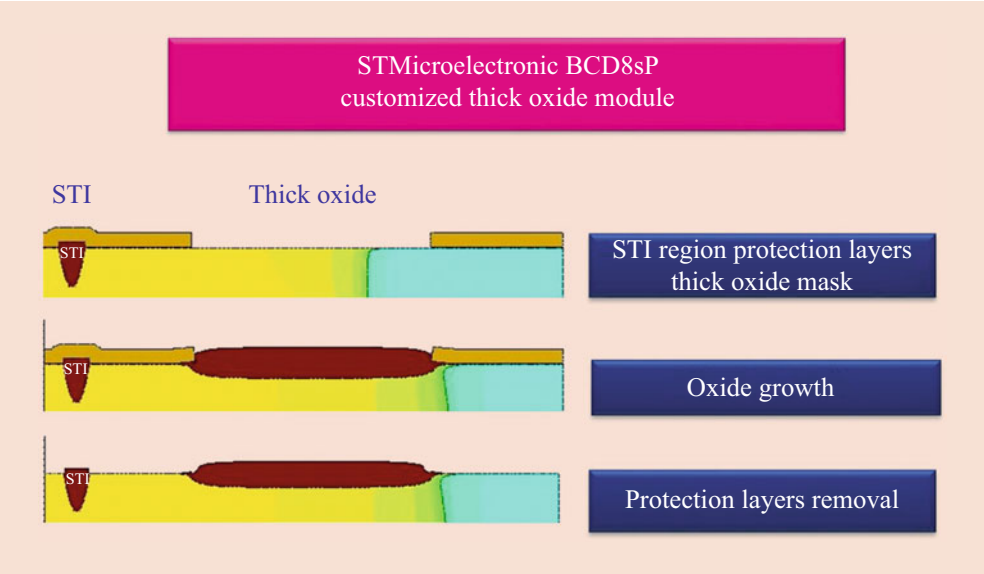

Fig. 3.49 Customized thick oxide integration in advanced BCD technology (BCD8sP, 160 nm)

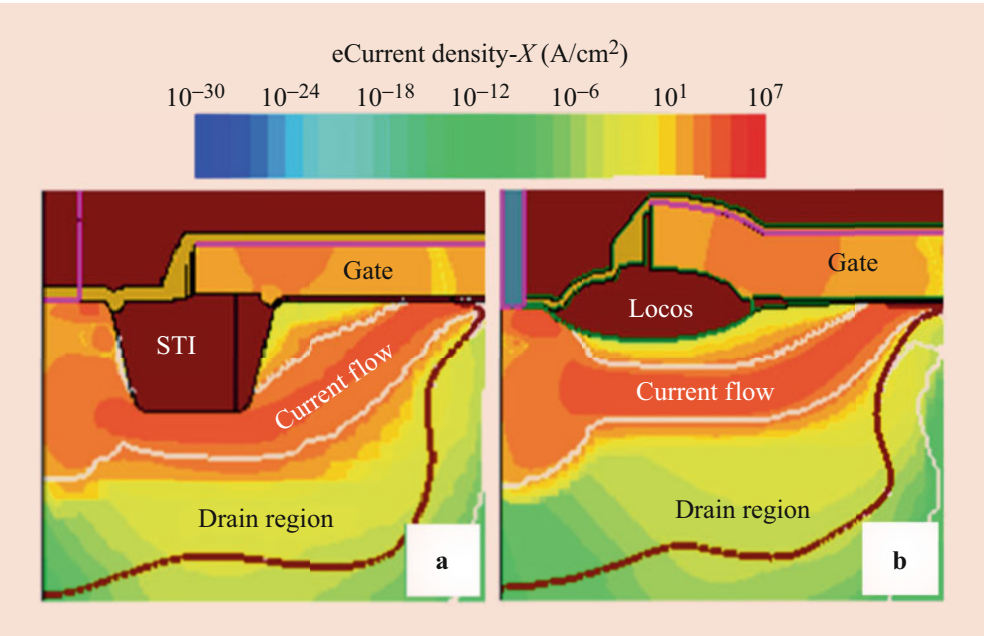

Fig. 3.50 Electron current density flow for (**a**) STI terminated high voltage device and (**b**) LOCOS terminated one. Device biasing conditions: $V_{ds} = 18$ V, $V_{gs} - V_{th} = 1$ V

minimizing gate to drain overlap capacitance in RF power LDMOS [45, 46]. This solution is currently adopted in many advanced BCD platform thanks to the improved process control leading to a better definition of the thin/thick gate oxide transition regions. Isolation oxide thickness is fixed by device voltage rating: higher voltage capability requires thicker layer to minimize the drain extension resistance. However, integration constraints (lithography depth of focus coming from non-planar surface, reduced pre-metal dielectric thickness) limit the maximum allowed value and therefore the maximum voltage capability. To overcome some of these integration challenges, a novel structure realized on the bottom of the CMOS shallow trench has been conceived and proven on silicon (Fig. 3.52).

2. Single oxide architecture (Fig. 3.38) with no specific thick oxide region is introduced minimizing the integration cost. Trade-off between gate oxide thickness and drain extension doping/length (*O* and *S* in Fig. 3.53) is key to achieve good performance up to 20 V. Recently

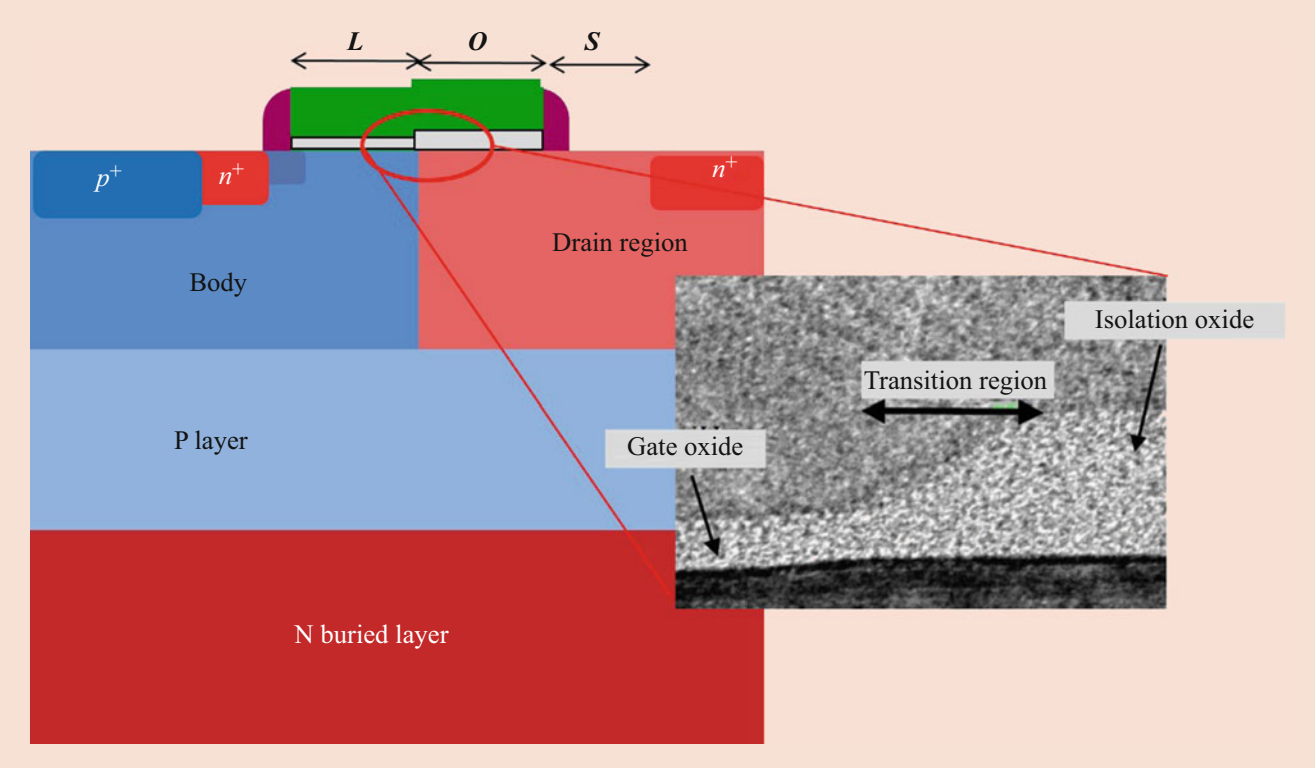

Fig. 3.51 Dual oxide architecture. Detail: TEM section highlighting the transition region between thin (gate) oxide and thick (isolation) oxide layers

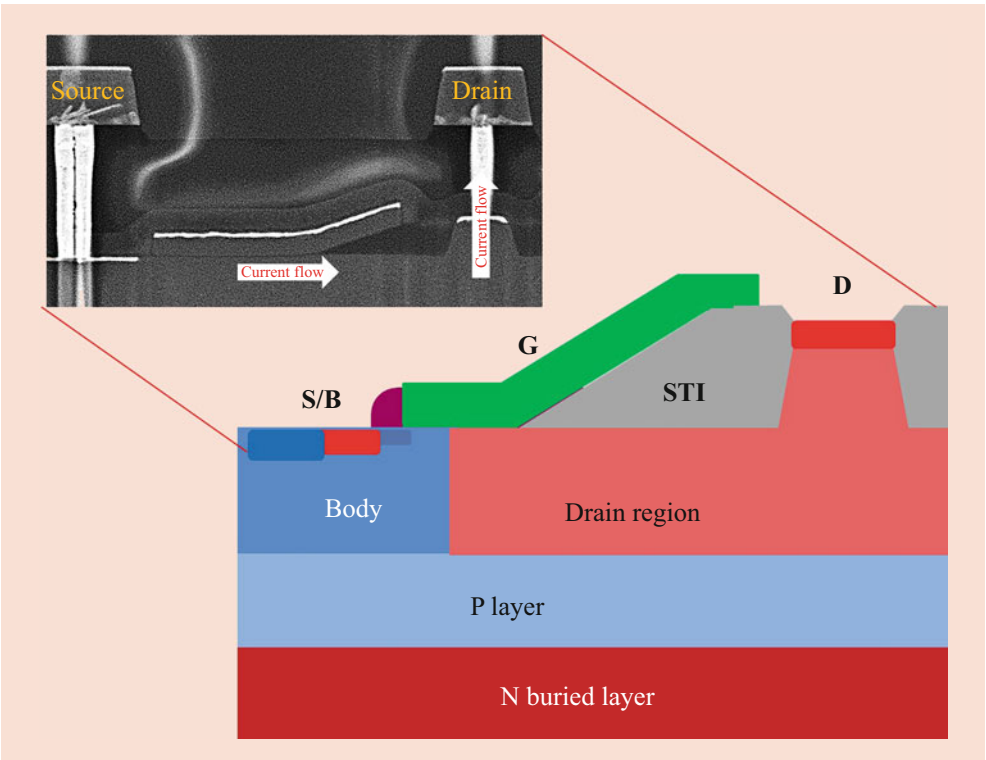

Fig. 3.52 Dual oxide architecture: novel solution to integrate thick isolation layer. Part of the device is realized on the bottom of the shallow trench region

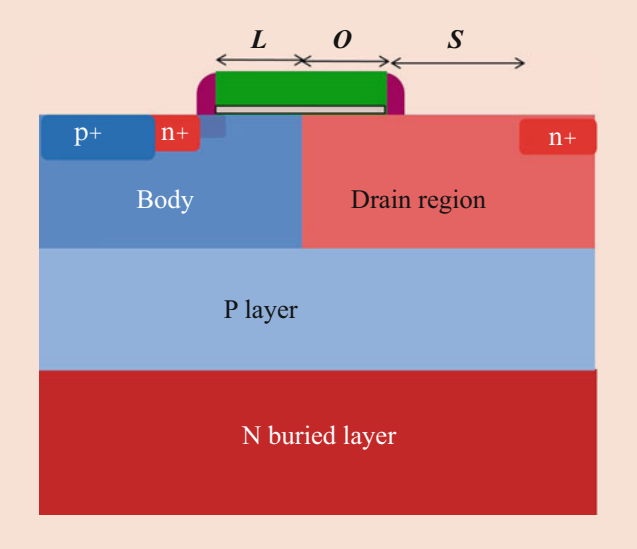

Fig. 3.53 Single active area architecture

contact layer is used as field plate on the uncovered drain extension zone to further improve performance and reliability [47].

High Voltage Power Devices

The evolution of power devices in the last 30 years has been driven by a continuous improvement in the elementary devices' architecture for classical voltage rating typical of a wide variety of applications in consumer, industrial, and automotive markets. In these segments, the main driver has been the continuous improvement of power device performances keeping the same voltage rating between 5 and 100 V.

There are many high power applications requiring larger voltage capability (Fig. 3.54). Home electronic systems connected to the AC power mains are requiring as first step an AC/DC conversion circuit to generate a stable DC voltage to supply the required current to the loads: this market is growing fuelled by the adoption of LED lighting and smart systems driven by energy-saving requirements. At the same time, high power delivery generated by high voltage battery systems is needed by car electrification and by industrial segment.

High voltage (600 V and above) system-on-chip integration is not today a viable solution. Power discrete devices are the preferred choice since monolithically integrated vertical solution for such rating voltage would require very thick epitaxial layer with high associated cost and poor performance given by the collecting path contribution. Thanks to RESURF, a lateral architecture would be the natural choice for power integration but the figures of merit ($R_{on} \times A$) of this architecture is relatively poor compared to discrete vertical power MOSFET.

In Fig. 3.55, a typical block of a high voltage system is reported: monolithic IC is realized to drive large size external power devices (IGBT or MOSFET). Together with power gate drivers, some functions are integrated in the same chip mainly for system diagnosis and control. High voltage (>600 V) platform availability enables the integration of high side gate driver and bootstrap diodes.

The management of such voltage is putting new challenges in the platform architecture conception. Very low doped substrates are required leading to an increase in the noise injected during the circuit operations. For this reason deep trench solutions can be introduced in the flow both to minimize the lateral isolation dimension and to decrease the ground collecting resistance reducing the cross talk between the different blocks [48, 49].

The high voltage device lateral architecture is very similar to the one presented above (Fig. 3.43): very light doped layers on a long drain extension (60–100 μm) are needed to satisfy the large off-state voltage requirement (BV_{dss} > 800 V). The low doping concentration makes this device very sensitive to the electrical charge distribution on the layers present above. For this reason, specific field plates are conceived to mitigate the sensitivity of the key electrical parameters (such as BV_{dss} and R_{on}) to the charge distribution (see Fig. 3.56). These specific field plate architectures play a critical role in securing the long-term stability of the device during operations [50].

In the latest years, new emerging applications are requiring larger rating voltage moving to 1200 V and even above. Recently 2000 V BCD platform has been reported using very thick SOI (12 μm oxide) for electric vehicle systems [51].

At the same time, the availability of depreciated manufacturing assets makes economically feasible the integration of advanced (180–350 nm) CMOS platform with high voltage capability [52]. Therefore more complex system can be realized integrating more functions and increasing the driving capability to manage larger power discrete devices (Fig. 3.57).

3.4.3 High Current and Energy Capability

State-of-the-art smart power technologies, thanks to the progresses in terms of microlithography and power devices improved architectures, are able to provide lower and lower $R_{on} \times A$ figure of merits in terms of power integration capability.

Even if a limit can be put as far as maximum current capability for an integrated power device in the range of 10–15 A (for higher currents, power discrete or VIPower technologies are more suitable [53]), the power density to be managed is continuously increasing.

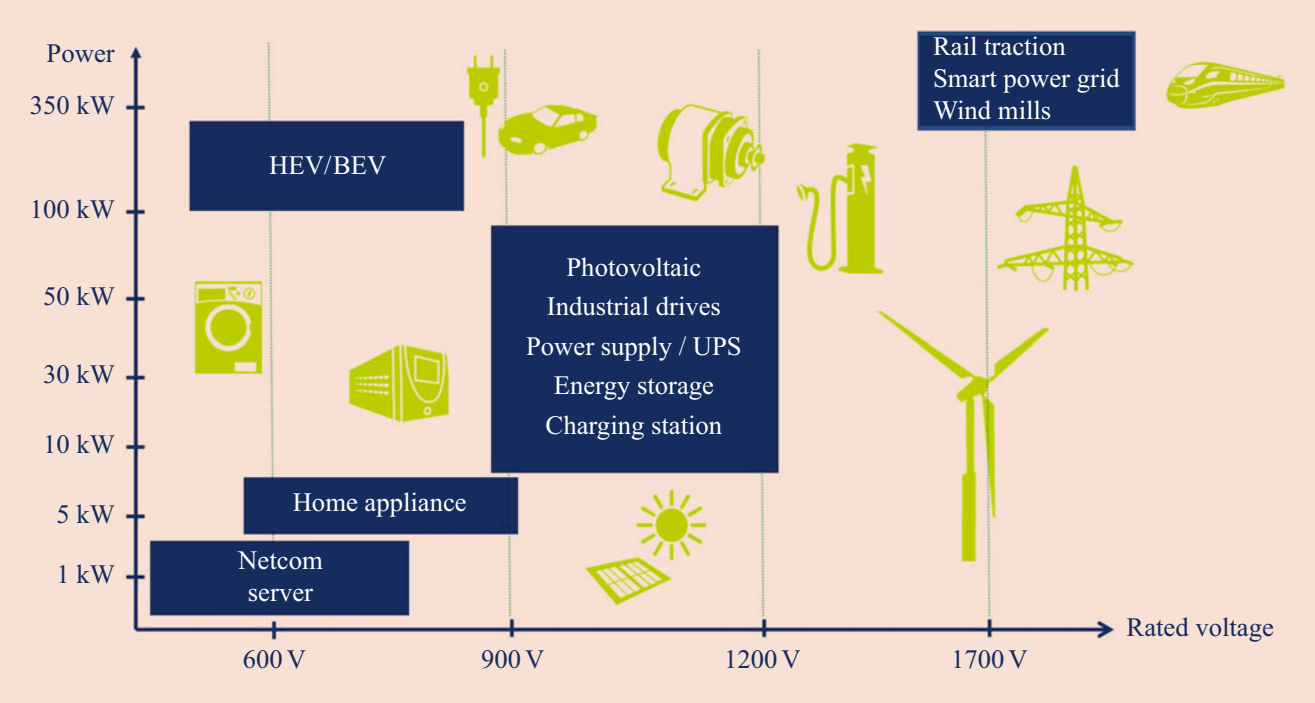

Fig. 3.54 High voltage/large power application map

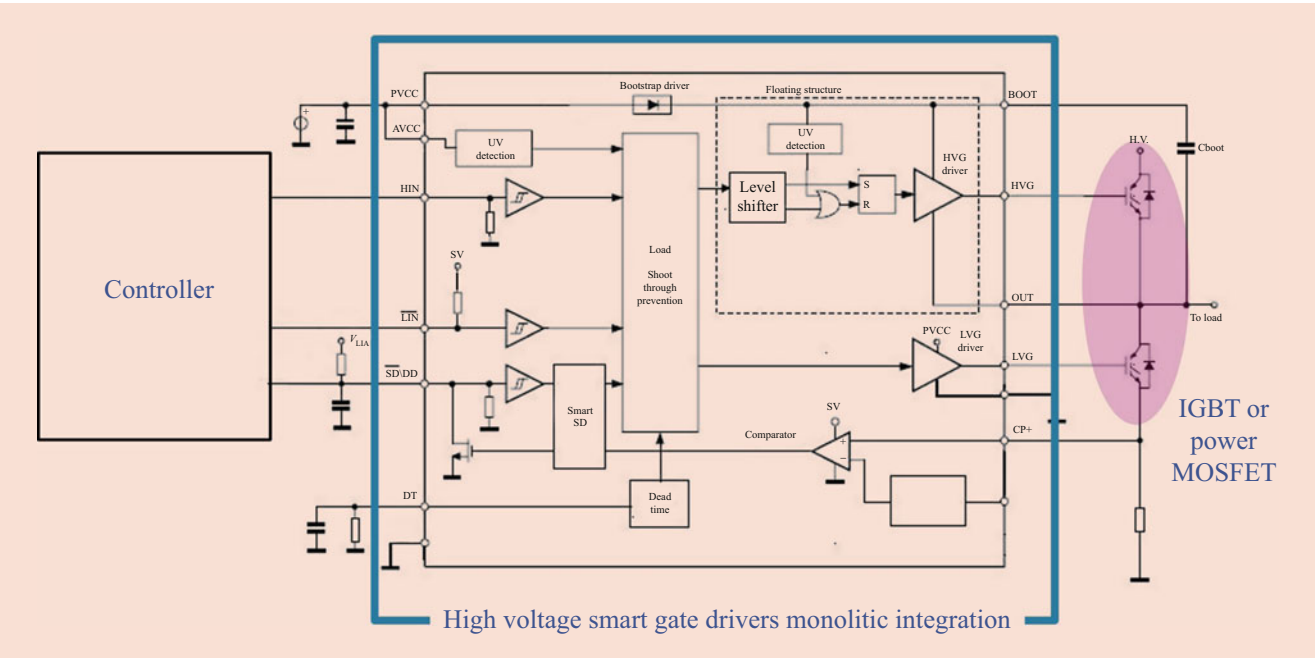

Fig. 3.55 High voltage system block diagram

These limits, together with the tough requirements of 15 years lifetime, 12,000 hours in power on and, moreover, power pulse cycling that are causing severe thermomechanical stress on inter-dielectric layers [54], are just a few examples of the main challenges to be addressed when designing smart power technologies and products.

Automotive products such as anti-lock braking system (ABS) and injector drivers are subjected to high energy pulses induced by re-circulation current of inductive loads. The pulse duration is typically in the range of 0.1–1 ms for the above applications. The energy pulses generate high temperature gradients inside the power components: due to

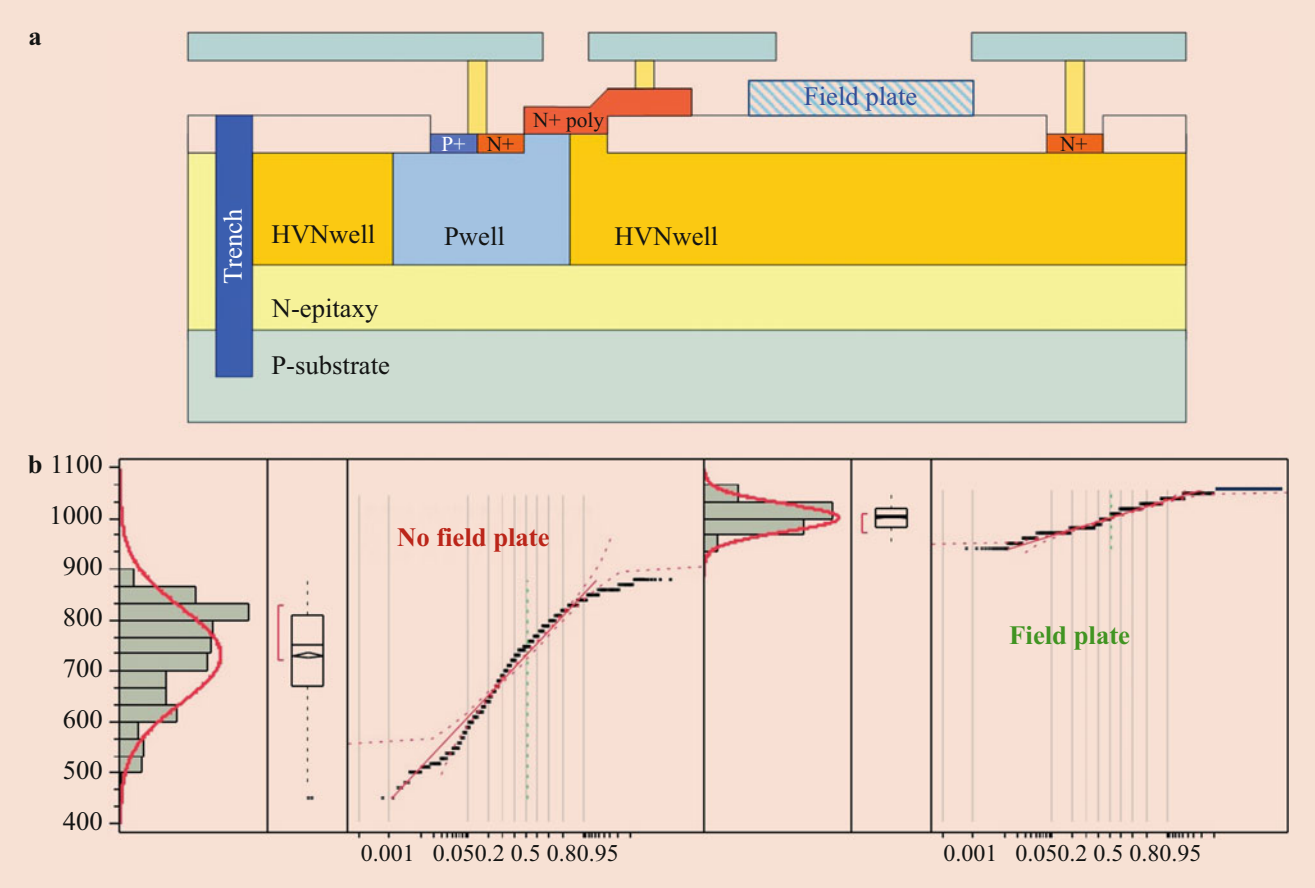

Fig. 3.56 (**a**) High voltage N-channel device in 800 V 350 nm BCD technology. (**b**) BV_{dss} distribution of two different structures with and without specific field plate on drain extension region

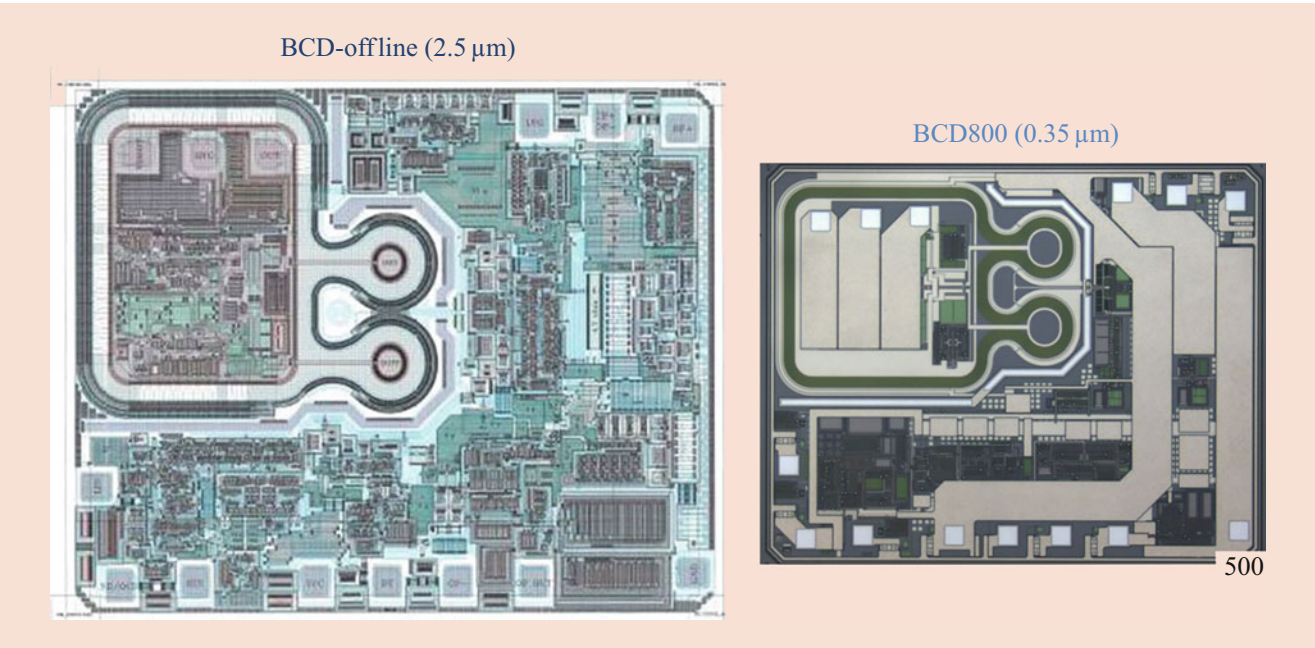

Fig. 3.57 High voltage gate driver monolithic IC evolution: from 2.5 to 0.35 µm technology platform. More integrated functions with increased gate driver capability in a reduced die size

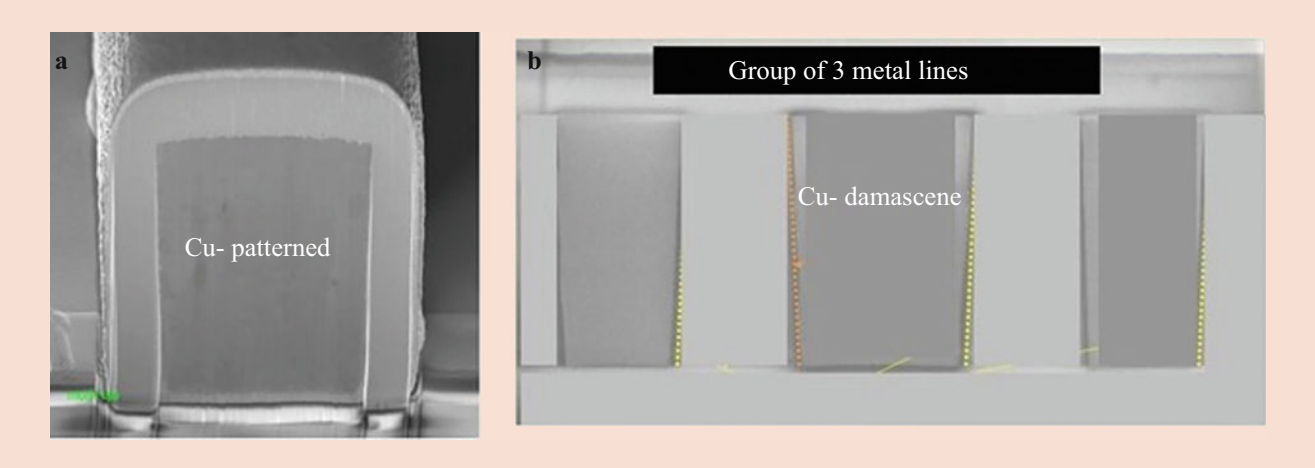

Fig. 3.58 Thick copper obtained by (**a**) patterned or (**b**) damascene electroplating

the device shrinkage, the peak temperature may be above 300 °C. Many phenomena that lead to the final device failure can be identified [55, 56], namely:

- Fatigue crack initiation within the oxide layers (high cyclic fatigue failure).
- Low cyclic fatigue failure due to alternating stress beyond the yield limit in the metal layers and ratcheting effects.
- Creep of the metal layers.

Thermomechanical stresses are induced by mismatch in coefficient of thermal expansion (CTE) in the materials coupled to a cyclic change in temperature owed to the heating power input into the system. Both material properties and geometrical parameters of the device packaging system strongly affect the thermomechanical stress state.

In general the understanding of the physics behind this failure mechanism is of utmost importance. Automotive field applications require strict mission profiles (in terms of number of pulses), and proper design guidelines are needed not to be "energy limited" in power devices sizing.

To overcome these failure mechanisms, new metallization solutions have been proposed and multilayer metallization [57, 58] and/or thick copper metal layers have been used [59]. Figure 3.58 shows two different solutions for thick copper metallization on smart power technologies: patterned and damascene.

The thick copper patterned electroplating technology allows higher thickness and is used for power metal and power bus routing. This patterned copper plating approach permits to achieve high thicknesses ($\geq$ 10 μm) for the thick copper top metal, which acts therefore more effectively as a heat sink, keeping the transistor colder at the same injected energy.

Furthermore, the low resistivity of this thick copper allows reduction of the contribution of the metallization connection to the overall on-resistance of the power device and minimizes any possible de-biasing effect on the gate-source applied voltage, especially when the power element size is so huge that the metal resistance becomes a meaningful parameter.

Table 3.2 Comparison between aluminum and copper material properties

Property	Aluminum	Copper
Electrical resistivity (μΩ × cm)	2.70	1.70
Resistance to electromigration	Low	High
Hardness (Mpa)	140–160	340–490
Young modulus (GPa)	50–70	110–130
Shear modulus (GPa)	25	46

Sources: www.matweb.com, www.memsnet.org

The thick Cu damascene technology is more VLSI oriented; it allows lower thickness but thanks to finer pitch can also be used for signal routing.

Advances in BCD technology to finer lithography (110 nm and below) brought thin Cu metallization from CMOS technology for signal routing. This thin Cu introduction demonstrated to be advantageous in further improving the energy capability of power devices, in addition to the well-known benefits associated to Cu metal lines, i.e., lower resistivity and higher electromigration robustness compared to aluminum.

The key material properties which make copper preferable for advanced BCD technologies are shown in Table 3.2 in comparison to aluminum.

The gain given by full Cu BEOL in the robustness of power devices against high and repetitive energy pulses is due to the lower plastic strain of Cu vs aluminum when submitted to thermomechanical stress, as demonstrated by the case study summarized here below [60].

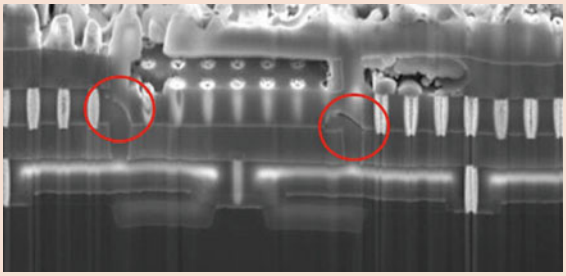

Fig. 3.59 Short between metal due to metal extrusion inside oxide crack. AlCu thin metal lines

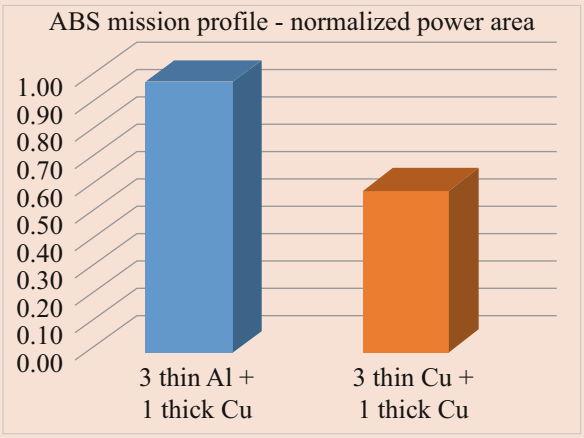

Fig. 3.60 Improvements in silicon area for energy pulsing capabilities (automotive ABS mission profile)

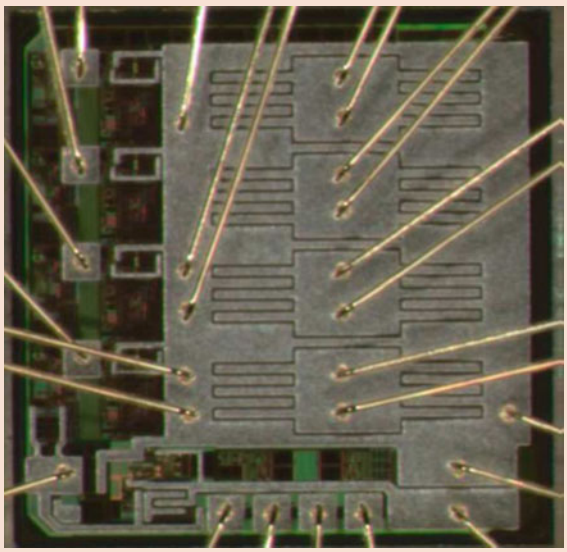

Fig. 3.61 Example of wire bonding connections on power devices active area

Repetitive power pulsing test results are reported for a power N-channel laterally diffused MOS (LDMOS) with active clamp and two differing BEOL metal configurations: (1) mixed Al thin signal metals and thick top copper power metal and (2) full copper. A 60 V power N-channel LDMOS on 160 nm BCD technology platform with active clamp has been submitted to repetitive power pulsing tests simulating the recirculation of an inductive load.

The power N-channel LDMOS has been designed with three thin metal levels plus a 4-μm-thick copper layer as top metal level. The first three thin metal layers are 0.3–0.5 μm thick for both BEOL configurations with full copper being latest BEOL scheme for 110 nm BCD technologies.

Repetitive power pulsing test is carried out until the occurrence of an electrical short: 1 ms pulses with 20% duty cycle were applied to power devices at 200 °C above the junction temperature reproducing aggressive automotive mission profiles.

As a result, the lifetime of the full Cu BEOL is improved by a factor ~10 to 100 with respect to the mixed Al and Cu BEOL.

Failure occurs because of inter-metal oxide cracking, due to metal plastic deformation, leading to metal short when the metal extrudes inside the crack (see Fig. 3.59 for Al thin metal).

The failure analysis carried out on several devices did not highlight any thin metal deformation in case of full Cu BEOL.

The effect of a full copper BEOL on the size of power components in case of an energy limited automotive application, the anti-lock braking system (ABS), is shown in Fig. 3.60: a 40% shrinkage of the power section, rated at 40 V, can be obtained.

Another limiting factor for the shrinkage of the IC size enabled by the BCD technology lithography reduction is given by the size needed for the pad structures which allow to interconnect the die to the external world. This limitation derives also from the higher pin count of advanced smart power products, which can integrate an increasing number of functions thanks to the higher digital and analog density of latest BCD technologies. Also the shrinkage of the IC area occupied by the power devices would be limited if the large bonding pads, needed for thick wires to handle the current, cannot be placed over the power transistors (Fig. 3.61).

Hence the need to move pads from passive die area to regions of the die where active components, including power transistors, are present, maintaining robustness and system reliability [61].

The use of thick copper in combination with over pad metallization (OPM) (Figs. 3.24 and 3.25) provides excellent reliability of the solder joint in high temperature applications with extended lifetime requirements and is capable to resist to the mechanical pressure coming from thick and stiff wires, reducing the stress propagation in the BEOL system and down to the active components [14, 62].

3.4.4 Passive Technology Modules for High Precision, Analog, and High Voltage Applications

The features and advances of specific applications in terms of performances (accuracy, noise), voltage domain, and safety require the introduction within BCD technology platforms of customized technology modules.

Analog accuracy demands for the availability of passive components as resistors and capacitors with excellent matching and stability capability. The basic passive elements available within the mainstream BCD flow suffer of significant parasitic contributions due to the implementation in the FEOL of the process and require also dedicated die area.

Solutions able to avoid these basic constraints can be obtained implementing such passive components inside the BEOL of the technology.

Resistors

The simplest and typical solutions can be realized with implanted layers requiring isolation versus substrate and therefore contributing significantly to the die size and with limited voltage capability and linearity due to the depletion of the doping layers.

Other resistors commonly used are made of polysilicon to be placed above the field oxide. Such kinds of resistors exhibit resistance variations upon applied voltage, high parasitic capacitance versus the silicon substrate and poor matching characteristics, which are not compatible with the specifications of the addressed functions.

Both diffused and polysilicon resistors are affected by the resistance variation as a function of temperature, usually taken into account through the temperature coefficient of resistance (TCR), defined as $(1/R)(\mathrm{d}R/\mathrm{d}T)$.

Thin film resistors integrated in the BEOL system overcome the described limitations, offering new solution for die size reduction on standard BCD technology [63].

In comparison to polysilicon or diffused resistors, they offer higher resistance values and precision tolerance, as well as lower TCR (<100 ppm/K) in the typical operation temperature range (–40 °C to 175 °C). Various materials are currently used as thin film resistors in IC applications, such as SiCr, NiCr alloys, and TaN [64–68], depending on the required resistance and TCR values (Fig. 3.62).

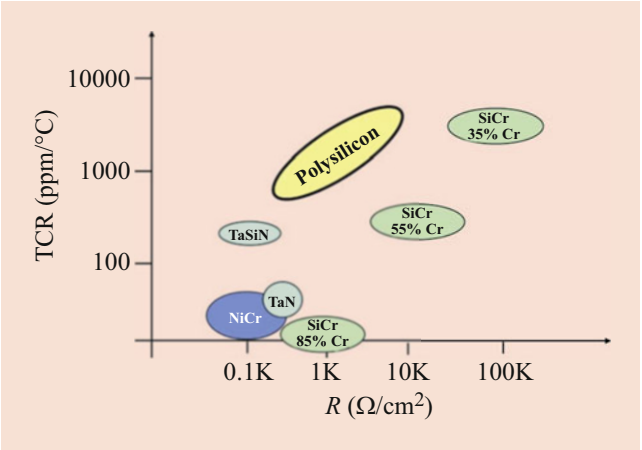

Fig. 3.62 Available thin film resistor mapping

The most interesting solution that provides very low TCR and high resistivity is the SiCr alloy, whose electrical properties can be modulated depending on the Cr content.

For SiCr resistors with 85% Cr content, 10 nm thickness and 600 Ohm/square sheet resistance, TCR in the range of 15 ppm/°C and matching accuracy within 0.5% are achieved.

Capacitors

In analog functions like decoupling, filtering, A-to-D converters, the main requirements on capacitors are the voltage linearity, the matching accuracy, and the precision control of the capacitor value.

Integration of such components demands other figures of merit to be met, namely, a small parasitic capacitance and access resistance, together with the need of a maximized capacitance density.

All of the above requirements can be fulfilled realizing metal-insulator-metal (*MIM*) capacitor structures within the BEOL scheme of the BCD technology.

Other types of capacitors commonly used, like poly-oxide-poly, poly-oxide-doped wells, or metal-oxide-metal (MOM) structures, can be implemented without adding extra process steps but are limited in terms of analog performances and of capacitance density.

MIM capacitors are realized dedicating one or two metal levels for the electrodes and thin high-K dielectric to maximize the capacitance density. To minimize the parasitic capacitance to the substrate, the MIM capacitor is preferably implemented between the upper metal levels of the technology BEOL.

Another advantage of this realization is the possibility to stack the MIM capacitor above active components, reducing the die size compared to other solutions.

Different kinds of high-K dielectric material have been presented for MIM application ranging from silicon nitride

to Al_2O_3, Ta_2O_5, ZrO_2, HfO_2, and $AlHfO_2$ with capacitance density spanning from 1 to 10 nF/mm^2 [69–71].

The MIM integration in BCD technology poses further challenges related to higher operating temperature conditions (150 °C) with reduced leakage constraints up to 5 V use. These requirements are in conflict with the increasing leakage behavior of HK insulators and therefore a trade-off must be identified.

Galvanic Isolation

Circuit isolation, usually named galvanic isolation, is a requirement in all electronic systems, where it is needed to inhibit the passage of unwanted current between two parts of the system under anomalous working conditions (voltage surges, spikes, transients) to protect equipment and users from hazardous situations.

At the same time, it is needed to transfer signal and power [72, 73].

Especially in the industrial domain, the isolation is becoming more and more needed in order to protect factory equipment which are highly interconnected with each other in the most automated factories. Automotive and medical are other application areas where high voltage isolation is required for a safe operation.

In the typical application, the low voltage signal driving the high voltage power components (IGBTs or SiC transistors) is passed through the inductive or capacitive coupling that provides also the galvanic isolation to the system.

Opto-couplers have been historically the most widely used solution for isolation purpose, but recent IC technology evolution introduced more compact, reliable, and cost-effective solutions.

The integration approach enables the isolation through a thick oxide using the dielectric layers of the BCD technology BEOL system and/or depositing additional layers on purpose. The oxide is therefore the insulating layer, with excellent dielectric and reliability features, placed between two metal layers to realize capacitive or inductive on-chip isolators.

The advantages compared to opto-couplers, which use molding compound based insulator layers, are the higher quality of the oxides deposited in IC front end manufacturing and the consequent absence of voids or large defects, which can give issues in the tests addressing the integrity of the insulating material (*partial discharge tests*).

Also in comparison to solutions using thick polyimide layer to provide the insulation function, the thick oxide approach can be considered superior due to its higher dielectric strength (2×–4×) and to the lower sensitivity to moisture absorption, which can degrade the lifetime performance of the insulator.

The system partitioning of an inductive insulator solution is shown in Fig. 3.63 and its on-chip implementation is presented in Fig. 3.64.

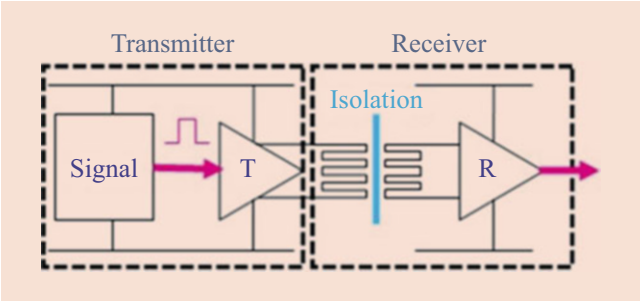

Fig. 3.63 Galvanic isolation system partitioning (inductive)

Hall Magnetic Sensor

Magnetic sensors are widely used in the industry for magnetic field sensing in very different technical domains.

Current sensing in industrial and automotive applications is an important segment where the substitution of sense resistor with magnetic sensors provides many benefits including avoidance of power losses.

Hall cells [74] in ICs are usually implemented by resistors, whose value is modulated by the presence of the magnetic field component normal to silicon surface.

Figure 3.65 shows the schematic realization of a Hall cell in a CMOS IC.

A resistive n-well layer, isolated into a p-well layer in a square shape, is realizing the Hall sensor cell.

When the n-well layer is biased between V_{dd} and ground, on the diagonal path of the resistive square, a flow of electrons is moving from the GND terminal to the Vdd terminal.

In presence of a magnetic field perpendicular to the plan, the Lorentz force applied to the electrons generates a movement of the electrons in the upward-right direction, causing the formation of positive charge in the bottom left area of the n-well layer; hence a voltage is generated between the OUT1 and OUT2 electrodes that is proportional to the magnetic field to be measured.

The addition of a magnetic concentrator [75] improves the sensitivity and allows sensing magnetic field components parallel to the silicon surface.

Figures 3.66 and 3.67 [75] show the implementation of magnetic concentrator in BCD IC.

3.5 Next BCD Development Challenges

BCD technology platform evolution has been historically driven by some main application segments:

- Hard disk drivers for computing.
- Motion control for industrial.
- Engine management, braking systems, and safety functions for automotive.

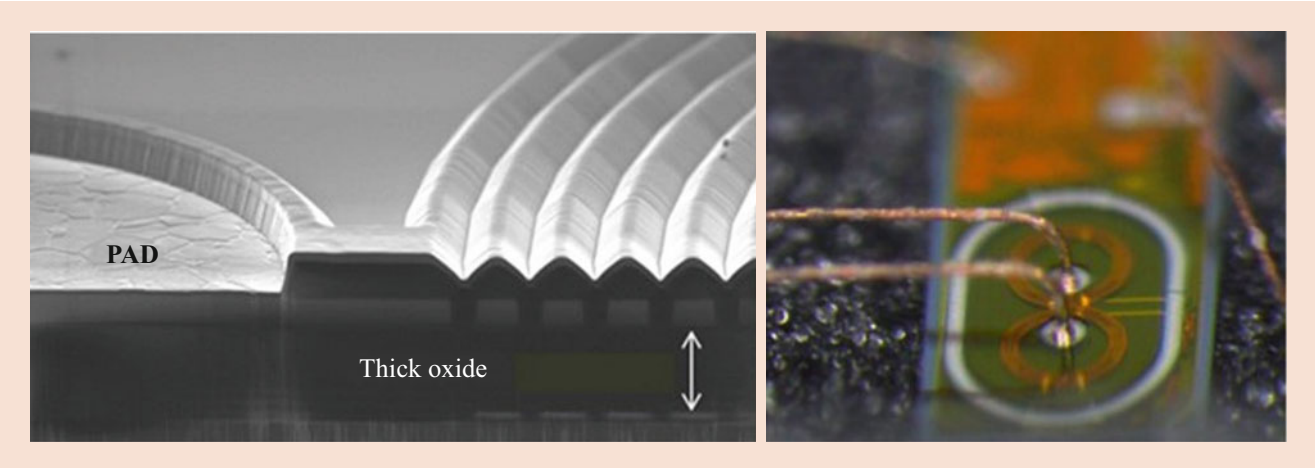

Fig. 3.64 Cross section and top view of an inductive galvanic isolation implementation

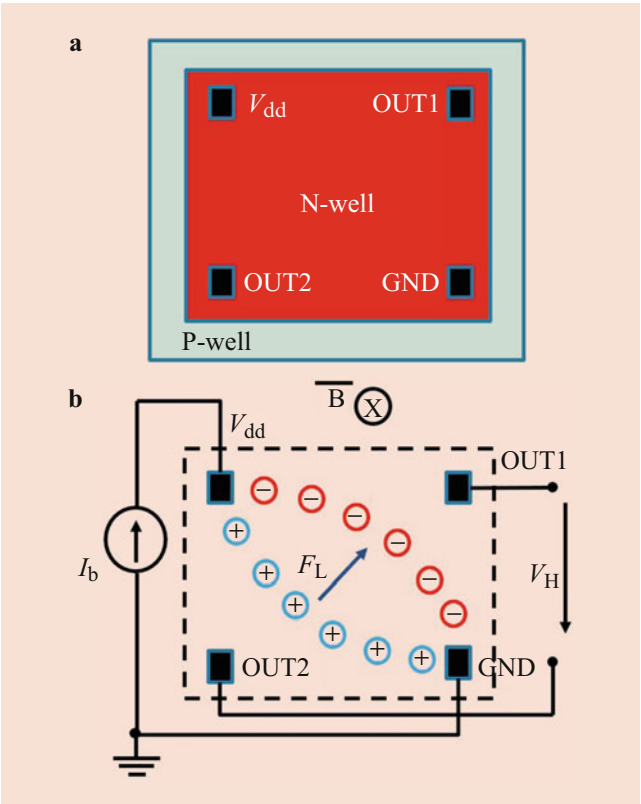

Fig. 3.65 (**a**) Top view of Hall cell in CMOS implementation and (**b**) scheme showing the Hall effect and the connections of the Hall sensor with surround circuit

- Audio systems for consumer and automotive.
- Power conversion for mobile and home appliances.

Some of these applications have reached a mature phase not requiring fast replacement of existing products with new features or functions: manufacturing efficiency is the driving force for the technology evolution to cope with the natural system cost reduction.

At the same time, new emerging applications with specific requirements are fostering the BCD technology evolution toward further lithography scaling.

The trend of increased data processing demands at very high MIPS rate for main application processor in high end mobile systems is raising the demand of high efficiency and sophisticated multiphase DC/DC power converters. These converters have consequently to integrate digital control loop with modular approach working at very high switching frequency (tens to hundreds of MHz) while delivering the large power required (tens of W).

Following the above trend, BCD technology found new applications at low voltage (5 V and below) requiring much finer lithography to meet digital complexity and speed requirement with the capability to deliver large current minimizing power losses.

Audio mobile signal processing is showing a similar trend.

Today BCD technology is offered at lithography node down to 55/40 nm taking benefit from the manufacturing perspective of depreciated plants and equipment.

Many technical challenges have to be managed to extend the possibility to use such technology platform to a wider power IC application spectrum:

- Integration of high-performance power devices targeting larger voltage capability (20 V and above).

  Due to reduced gate oxide thicknesses, larger gate to drain capacitance value and reduced drain doping layers are leading to a deterioration of the Key Performance Indicators: $R_{on} \times A$, $R_{on} \times Q_g$.
- Integration of high precision analog stages.

  The challenge is to cope with elementary devices analog performance deterioration due to ultrathin gate oxide

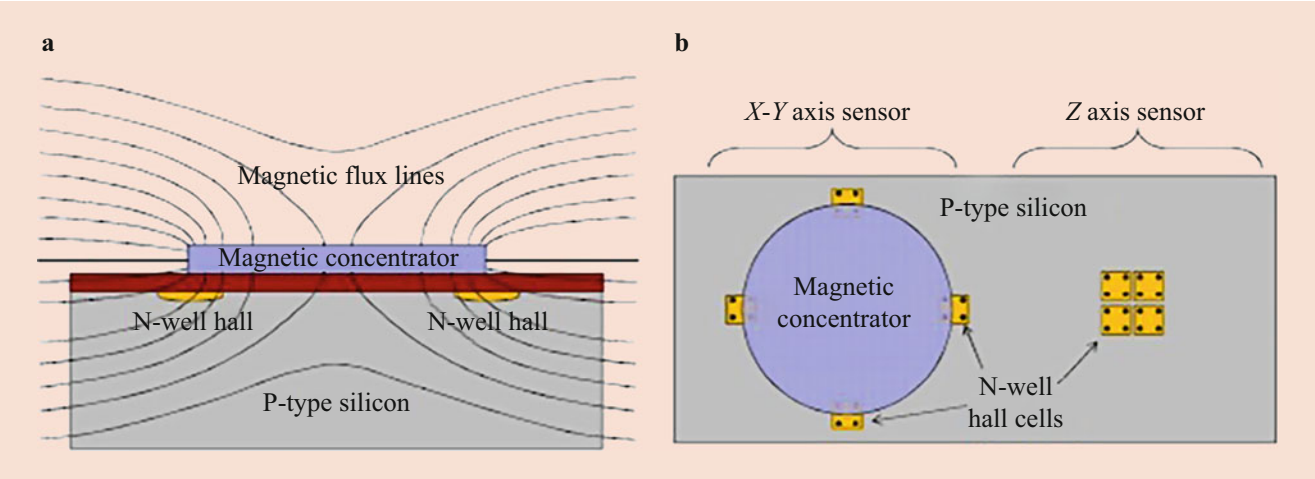

Fig. 3.66 (**a**) Cross section of an *X-Y* axis Hall sensor. (**b**) Top view of a *XYZ* axis integrated Hall sensor realized with a *XY* axis sensor and *Z* axis sensor, the last one with centroid symmetric multi-cell layout to reduce offset and noise

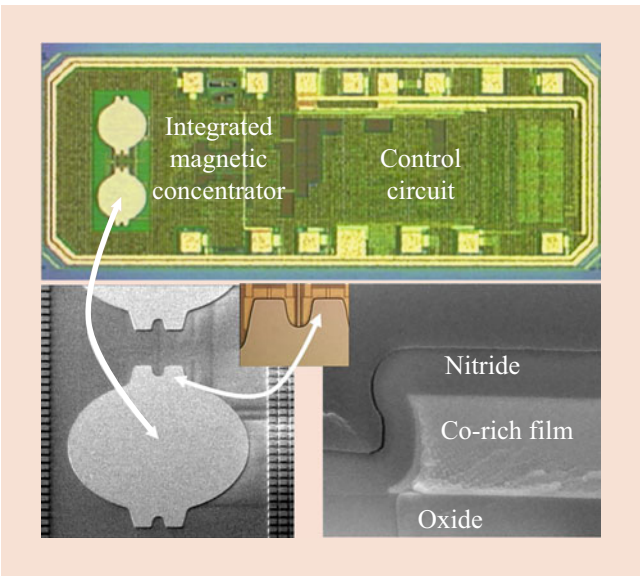

Fig. 3.67 Hall-based current sensor IC realized in advanced STM BCD technology integrating magnetic concentrator

with very cold processes leading to incomplete interface stabilization.

At the same time, the stringent layout constraints imposed by dense CMOS design rule requirements bring limitation in symmetric layout configurations (dummies placement, local density constraints, and mandatory parallel component orientation).

- High voltage signal management.

Severe limitations come from reduced isolation layer thickness and new dielectric materials with reduced permittivity and rigidity. In Fig. 3.68, the evolution of the minimum thickness between two metal lines is reported. A continuous scaling is driven by the minimum feature reduction together with the introduction of new materials with reduced permittivity. Given the fixed voltage requirement, an increase of the electric field is associated with this trend up to values that can cause detrimental effect on long-term reliability.

On the other hand, power device performance improvement is engaging significant efforts to identify novel architecture beyond the pure lithography scaling.

Since the further lateral shrinkage of the device critical dimensions (Fig. 3.43) is limited by the increase of the electric field, some very promising development lines are looking for an increase of doping levels, channel density, and carrier mobility.

Doping level increase at same voltage rating can be achieved through an optimization of the drain extension extending the usage of "Resurf" along all the dimension with the adoption of lateral super-junction solutions [76].

Super-junction architecture was first conceived on vertical power MOS to decrease on-state resistance at a given breakdown voltage originally for discrete devices with voltage rating in the range of 400–600 V.

A similar approach has been explored for the realization of integrated lateral devices (Fig. 3.69).

In this structure, the N-drain drift region is completely surrounded by P-type stripes providing a very effective depletion effect when biased in off state. A very uniform electric field is therefore obtained provided that an almost perfect compensation between the total dose present in the N and P doped regions is achieved by an optimum design of the structure (i.e., size of the regions and implanted doping dose). Exploiting this architecture, it is possible to increase the doping level of the N-drain extension region over compensating the loss of silicon area occupied by P-column and securing very low on-resistance performances close to silicon limit [77].

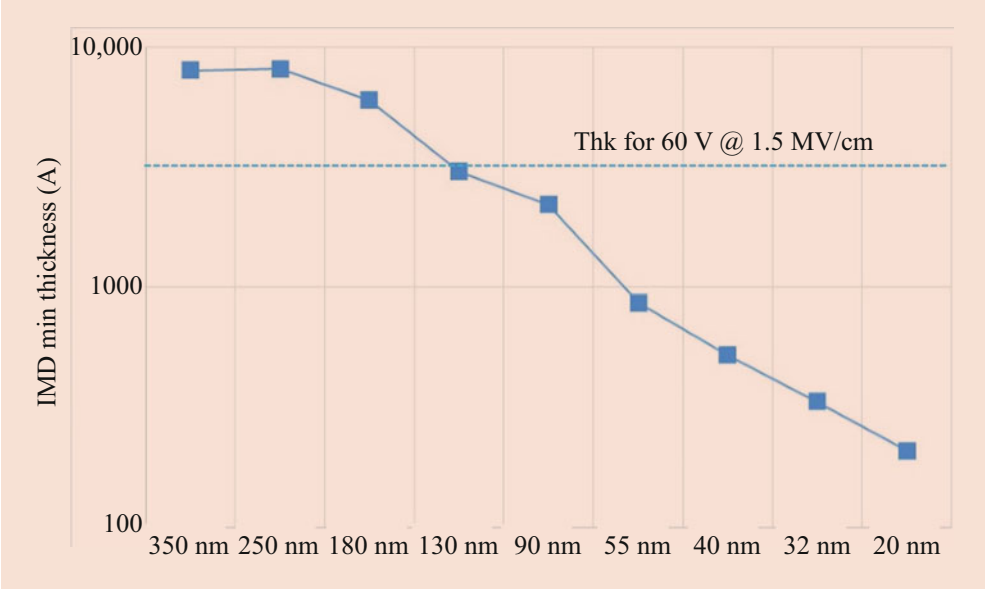

Fig. 3.68 Inter-metal dielectric (IMD) thickness evolution in different CMOS nodes. Line: minimum thickness required to secure 60 V between two subsequent metal lines with a fixed electric field

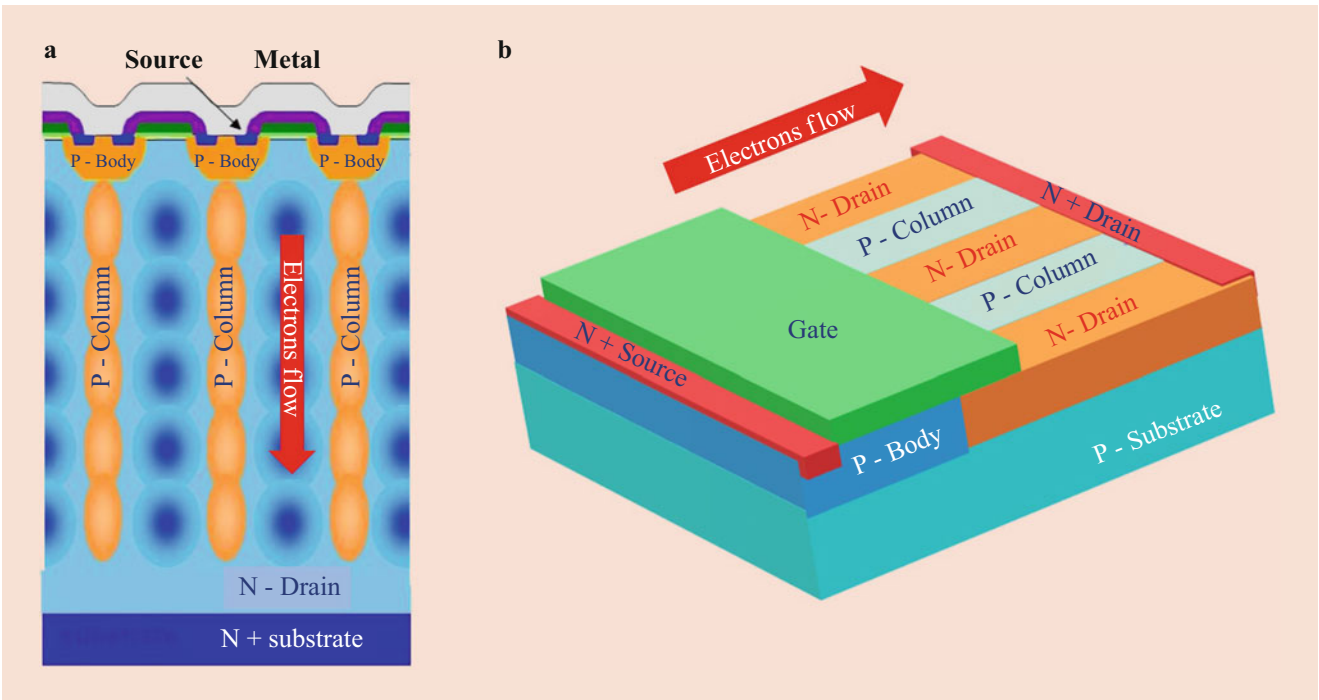

Fig. 3.69 Super-junction structure: solution for a vertical power discrete device (**a**) and extension to lateral integrated architecture (**b**)

Despite these solutions are expected to give major advantages for the higher voltage rating devices (>100 V) where the on-state resistance is dominated by the drain extension contribution, some research activities have been carried out to exploit the solution competitiveness for lower voltage integrated device [78].

Channel density (i.e., effective width integrated in the unit area) increase can be achieved exploiting the vertical dimension. Folded architectures have been presented for low voltage device [79] realization (Fig. 3.70): silicon etch is performed to realize a corrugated silicon surface covered by the gate oxide and polysilicon. From pure geometrical

considerations, density improvement is fixed by the vertical etch and the folding pitch: values between 30% and 50% seem achievable. Integration complexity and mobility control on the silicon sidewall are the limiting factors for the wide adoption of this solution.

Integrated trench FET architecture have been studied for boosting power performances in the 50–100 V rating voltage range [80]. This solution enables a drastic surface pitch reduction (Fig. 3.71) exploiting the vertical dimension for the realization of a trench-based MOS and drain extension region. This architecture is today the standard for low voltage (<100 V) rated power discrete device. The limitation for a wide usage of such architecture in an integrated BCD scheme derives mainly from the need of high conductive sinker regions and buried layers to minimize the collecting path resistance (Fig. 3.72). Integration complexity and the difficulty to scale the device for different voltage options narrows the usage of such architectures despite the meaningful performance improvement reported: factor 2–2.5 $R_{on} \times A$ reduction for a 60–70 V rated device.

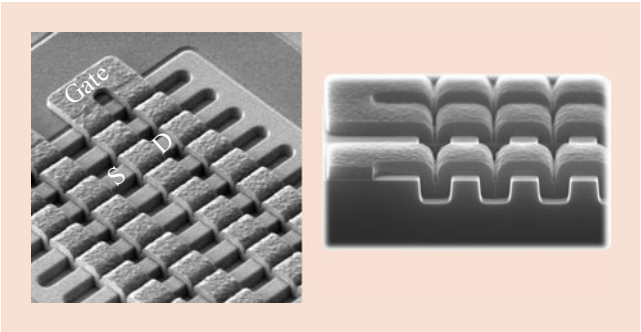

Fig. 3.70 Single active area folded architecture: planar SEM vision and section of silicon corrugation with poly gate

Carrier mobility enhancement thanks to silicon strain has been the dominant enabler to improve performance in CMOS technology evolution. The main obstacle to exploit the solutions implemented is coming from the very different lateral dimensions of the silicon areas to be strained. For this reason, few works have been so far published [81].

Wide bandgap materials advent in the power semiconductor sector is offering the opportunity for novel system architectures and performance. Silicon carbide (SiC) and gallium nitride (GaN) are compound semiconductors with some key basic material properties that make them a very competitive alternative to silicon for the realization of high-performance power devices.

Thanks to the larger energy bandgap (GaN: 3.4 eV, SiC: 3.3 eV, Silicon: 1.1 eV) the critical electric field for the avalanche breakdown on set is larger offering the possibility to realize high power devices with improved performance (better $R_{on} \times$ Area @ same breakdown voltage).

Silicon carbide-based power devices (diodes and power MOSFET) are realized on specific SiC starting material: substrate manufacturing process is quite complex and expensive and today 150 mm wafers are available on the market for devices realization. Process flow is requiring specific very high temperature process steps for the device real-

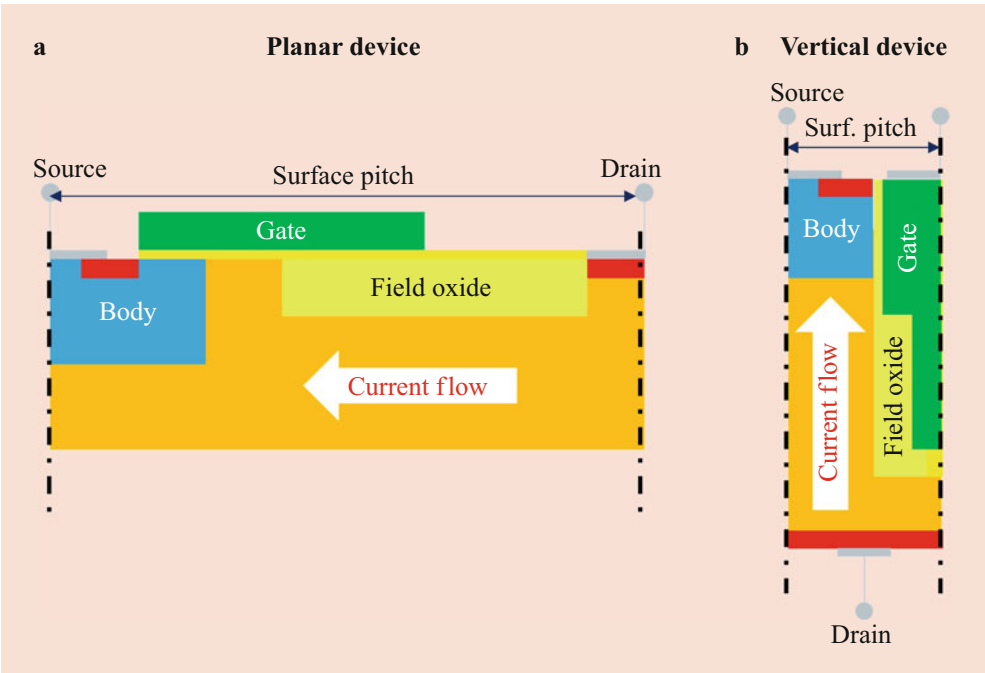

Fig. 3.71 Schematic cross section of a Vertical Trench based Device (**b**) derived from a Lateral solution (**a**). Surface Pitch scaling is obtained thanks to the vertical integration

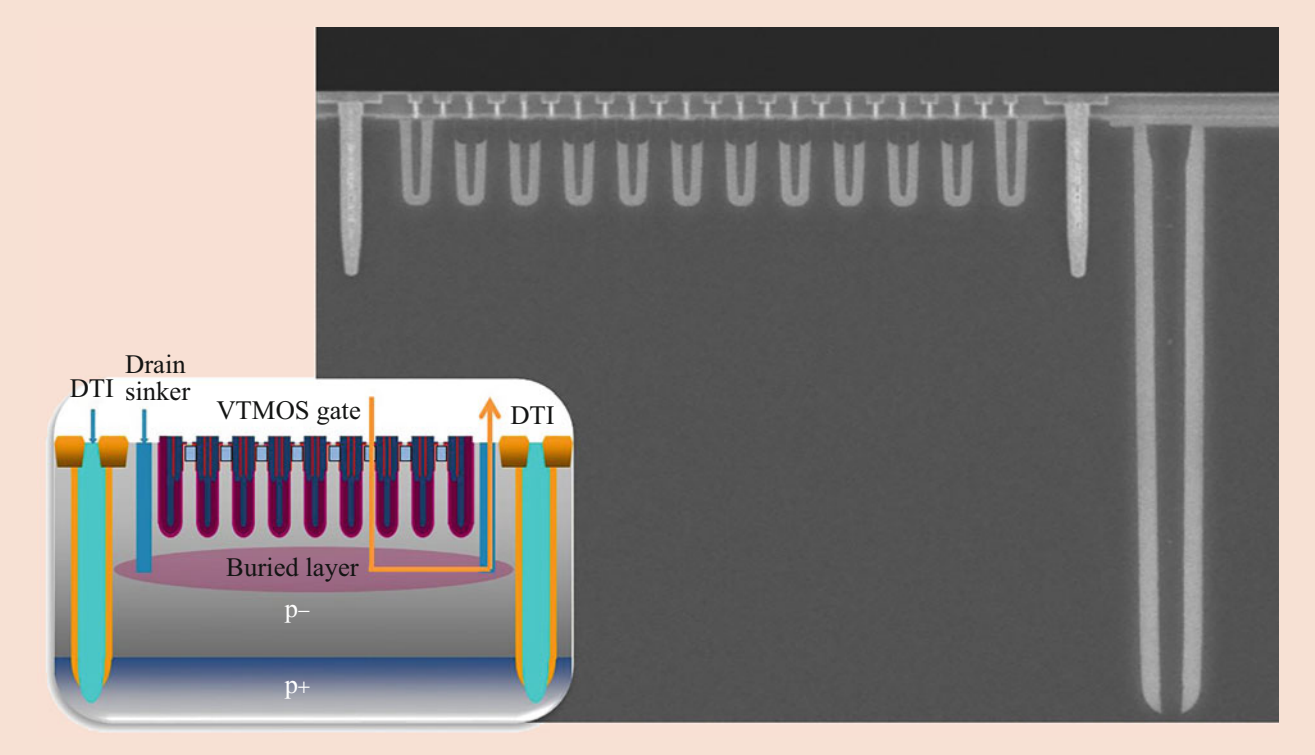

Fig. 3.72 Vertical trench power device integrated in an advanced BCD platform. High conductive sinker trench and deep trench isolation module are shown in the SEM section

ization. This is making this solution very competitive for very high power discrete application (600–1800 V rated, or even above) in some emerging markets (electric vehicle, power grid, industrial) where thanks to the meaningful performance improvement vs existing silicon devices (mainly IGBT) it enables an overall cheaper system cost solution.

Power high electron mobility transistors (HEMT) are realized using gallium nitride layers built on silicon substrate. Thanks to the possibility of realizing a good quality gallium nitride layer on a cheaper silicon starting material and thanks to the possible use of existing silicon manufacturing infrastructure, GaN-based power devices are today starting to get traction in many applications requiring large power (<600 V rated) or wherever the possibility of larger switching frequency operations is leading to a competitive market solution (passive miniaturization, LiDAR application in automotive, etc.).

Thanks to the compatibility of GaN-based power device with silicon manufacturing fabs, it is possible to imagine in the future a meaningful cost reduction together with the possibility of increasing the level of integrated functions.

First products with monolithic integration of GaN power device and gate drivers have been recently announced by different companies [82, 83] 0. The level of integration today reported is very limited due to the technology maturity and some specific limitation (lack of complementary MOS).

Optimized solutions to manage high power and energy dissipation need to take into account package technology.

Silicon and package technology must be developed in a concurrent way to get the best benefits at application level.

New packages with high pin count, high power dissipation capability, small outline, and low cost need to be conceived and developed; front end silicon and back end package technology compatibility is a major challenge that will become more and more important in the future.

3.6 Conclusions

The chapter described the evolution of BCD process technologies, today widely utilized in the industry to implement smart power IC's applications in automotive, industrial, consumer, and personal electronics field.

Introduced in the industry in the mid-1980s, BCD technologies followed three different development paths according to specific application fields, moving along three main axes: high voltage, high power, and high density.

Since its conception, based on the coexistences on the same chip of two main technology bricks (polysilicon gate CMOS and DMOS power architecture) and on the compatibility with bipolar components, it allowed the realization of SOCs, able to provide digital and analog control together

with efficient power sections, and put the basis for a sustainable innovation roadmap.

The evolution was driven by the continuous logic density increase, including the introduction of nonvolatile memories in different solutions, enabled by the lithographic shrinkage typical of CMOS roadmap, and to more and more efficient high voltage and high power integration thanks to innovation in power devices architecture.

Such trend was further supported by the introduction of new materials, such as the usage of thick copper metallization to improve current and energy capability, and new technology modules for the component isolation (Junction Isolation, DTI, SOI).

BCD technology roadmap was furthermore driven by differentiation with the introduction of technology options that allowed the integration of new functions like Hall sensing, galvanic isolation, and thin film resistors for accuracy.

As of today, BCD technologies are available with voltage rating spanning from 5 to 1200 V, with specific applications like galvanic isolation up to 6KV, and lithography features in mass production down to 90/55 nm.

New emerging applications with specific requirements are fostering the BCD technology evolution toward further lithography scaling down to 40 nm.

Future evolutions are foreseen to exploit heterogeneous integration for improved power devices integration, like GaN and silicon on the same chip.

On top of the classical BCD silicon roadmap, following the more than Moore approach, it is important to consider a complementary parallel path alternative to the monolithic integration, that is, system in advanced package solutions, like embedded die, where different silicon technologies including passive components can provide the best trade-off between performances and cost in a single package.

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Measuring Techniques for the Semiconductor's Parameters

4

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Contents

4.1 Transmission Electron Microscopy . . . 118
4.1.1 Conventional Transmission Electron Microscopy . . . 118
4.1.2 Scanning Transmission Electron Microscopy . . . 120

4.2 X-Ray Analytical Techniques . . . 128
4.2.1 X-Ray Characteristics and Common Experimental Apparatus . . . 129
4.2.2 Thin Film Analysis . . . 131
4.2.3 Case Studies . . . 133

4.3 Raman Spectroscopy . . . 137
4.3.1 General Aspects . . . 137
4.3.2 Experimental Setup . . . 137
4.3.3 Structure Analysis . . . 138
4.3.4 Carrier Concentration and Mobility Measurements . . . 139

4.4 Electrical Parameter Measurements . . . 142
4.4.1 Four-Point Probe . . . 142
4.4.2 Transmission Line Model . . . 145
4.4.3 Carrier Concentration Profile . . . 149
4.4.4 Mobility . . . 151
4.4.5 Carrier Lifetime . . . 151

4.5 One-Dimensional and Two-Dimensional Electrically Active Dopant Profiling . . . 152
4.5.1 Experimental Methods . . . 152
4.5.2 Applications of the Methods and Examples . . . 155

4.6 Optical Characterization of Semiconductors . . . 157
4.6.1 Basic Concepts . . . 157
4.6.2 Determination of the Optical Gap . . . 159
4.6.3 Dispersion Relations . . . 160
4.6.4 Impurities and Defects Absorption . . . 161

References . . . 163

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Abstract

A multiplicity of chemical (structure, composition, point and extended defects, impurities, etc.) and physical (carrier concentration, mobility, lifetime, band gap, core level energies, etc.) parameters characterize the behavior of semiconductors; some of them are more relevant than others according to the considered semiconductor and its use. The experimental technique suitable to measure a given physical or chemical parameter depends primarily on the chosen semiconductor, on its use as a device, and on the size and application of the device itself. For example, advanced silicon CMOS and SiC power devices require different measuring techniques. As it would be impossible to cover in a single chapter even the most important adopted techniques, we present just the basics of the following techniques: transmission electron microscopy (TEM), X-ray analysis, Raman spectrometry, scanning probe and atomic force microscopy, and basic electrical and optical parameter measurement techniques. Selected examples, taken from recent research activities, illustrate the capabilities and the potentialities of each technique. Most of the reported data refer to SiC, GaN, phase change materials, and Si nanostructures. For other subjects, a vast body of literature is available on the wide range of existing techniques for the characterization of basic semiconductor

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parameters. Some relevant references on more specific arguments are suggested in the chapter.

Keywords

Transmission electron microscopy · X-Ray analytical techniques · Raman spectroscopy · Electrical parameter measurements · Scanning capacitance microscopy · Optical characterization

4.1 Transmission Electron Microscopy

The fabrication of semiconductor devices requires the well-defined characterization of the adopted materials and processes. Transmission electron microscopy (TEM) is a direct technique for investigating a sample even at the nanoscale, providing morphological, structural, and chemical information. This section starts with a description of conventional TEM (CTEM) and of its use to investigate defects. The remaining part of the section deals with scanning transmission electron microscopy (STEM). The technique takes advantage of the narrow size of the electron beam, a fraction of angstrom and of the interaction with target atoms. Characteristic X-rays are emitted and adopted for elemental identification. The intensity of the scattered electrons at high angles gives information on the atomic number of the scattering centers (Z contrast) of relevance for the analysis of compound semiconductors. The determination of the atomic structure of misfit dislocations at the Si/Ge interface, of antiphase boundary in a 3C-SiC layer, and of different crystalline structures (rock salt and trigonal) in a phase-change alloy illustrates the technique. The simultaneous acquisition of different signals, characteristic of the probed element (EDX, energy-dispersive X-ray; EELS, electron energy loss spectroscopy), at the atomic scale has been used to determine the composition of AlGaAs multishell nanowire and the chemical bond of graphene layer on top of SiC as examples.

4.1.1 Conventional Transmission Electron Microscopy

The main relevant semiconductor parameters rely on crystalline and chemical properties, and TEM can straightforwardly give insights into the material properties [1–3].

From the structural point of view, extended defects as dislocations and stacking faults (SFs) play a crucial role in determining the mechanical properties of materials. Moreover, as for precipitates, grain boundaries, and point defects, they affect the electronic properties, because they act as scattering centers for charge carriers as traps or as radiative or nonradiative recombination centers. As far as extended defects are concerned, TEM analysis provides detailed information on dislocations, e.g., the type, the density, and their distribution. The main reason for using an electron microscope instead of an optical one resides in the resolution. As electrons are usually accelerated in an energy range between 60 and 300 keV, their corresponding wavelength is of the order of several picometers, well below that of visible light (400–700 nm). However, aberrations affect the focusing system of TEM, reducing the actual resolution to $\approx 50 \div 300$ pm.

In TEM, the source (gun) emits electrons by thermionic or field effect. Typical electron currents measured at the first focusing point in the microscope (the crossover) amount to several microamperes. These electrons are accelerated to a desired energy and managed by a system of electromagnetic lenses and dipoles for focusing and deflecting the beam respectively. As electromagnetic lenses are affected by aberrations, the TEM is also equipped with a set of multipole coils that correct part of the aberrations. By arranging the lenses in a proper way, the electron beam can be manipulated to illuminate the sample with a parallel beam or with a convergent beam.

In Fig. 4.1a, a very schematic sketch of TEM working in parallel mode is shown; in a real TEM instrument, tens of lenses and dipoles are present. All of them should be routinely tuned to work properly.

Electrons interact strongly with the atoms and then the specimen must be thinned to a few tens of nanometers before TEM analysis in order to have electron transparency and transmitted electrons. There are several methods to thin the sample: mechanical polishing, ion milling, wet etching, focused ion beam (FIB),, and microtome preparation. On the other hand, the strong electron interaction with the target atoms produces multiple secondary signals, such as characteristic X-rays. Their analysis gives information on the elemental composition of the sample. The most important effect, however, is regarding electron scattering and the phase shift of the incident electron wave.

In a crystalline sample, the transmitted electrons are deflected in well-defined directions, according to the Bragg diffraction criterion. For each direction, electrons are then focused on a different point of the back focal plane of the objective lens, to form the diffraction pattern (DP). Post-specimen lenses (not shown in Fig. 4.1a) can be tuned in order to show the DP or to magnify the image of the sample up to several millions of times.

The electrons emerging on the bottom of the crossed sample, if focused by the objective lens, form an image of the sample in the image plane. Although, naively, this recombined image resembles a 2D projection of the sample, the details of the micrograph contrast depend in a complex manner on the undulatory description of the interaction between the incident and the diffracted beam, and on the presence of inelastic scattered electrons. A detailed interpretation often requires simulations and/or considerations of sample

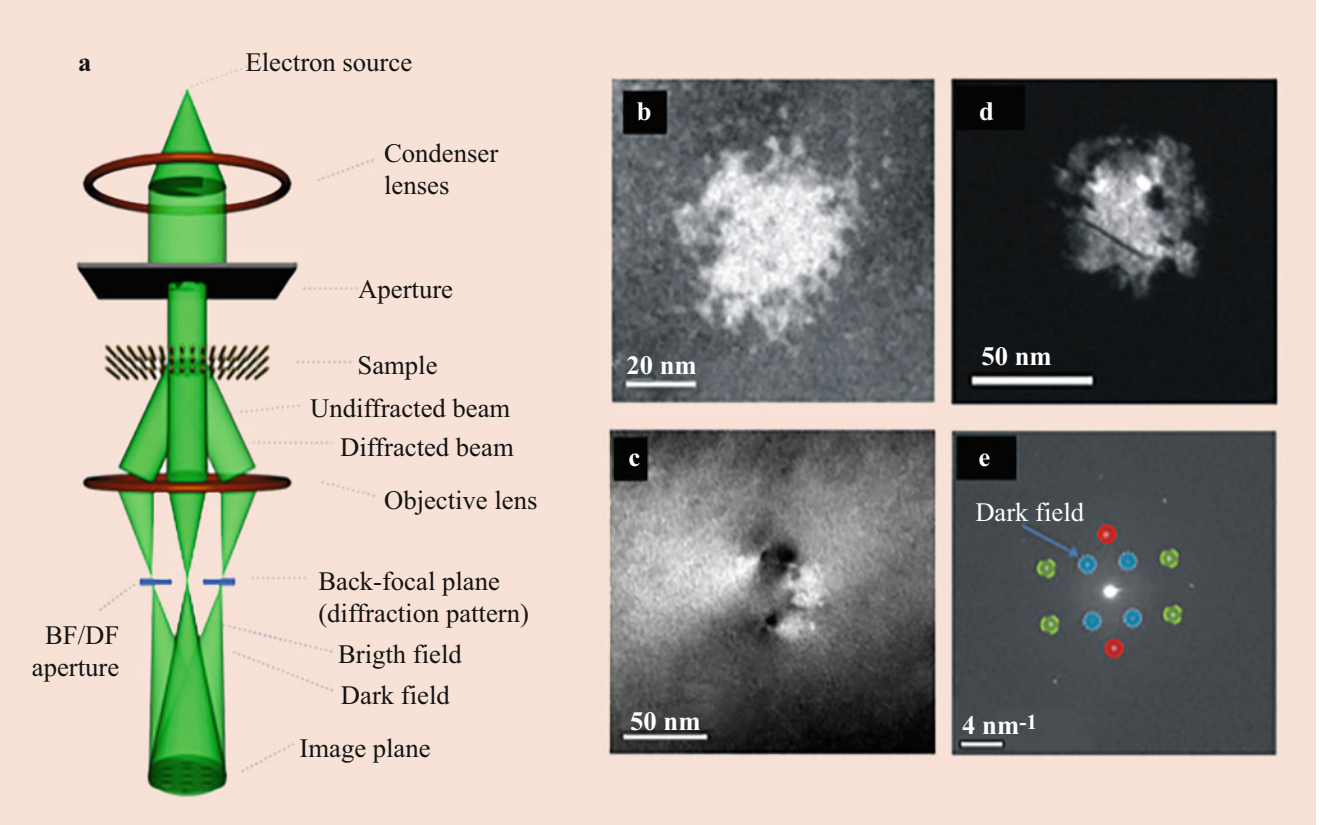


Fig. 4.1 (**a**) Sketch of TEM working in parallel mode; after crossing the sample, the diffracted and undiffracted beams are focused according to their direction by the objective lens in the back focal plane to form the diffraction pattern and then they reassemble to form the image in the image plane. A set of intermediate lenses (not shown) below the image plane can magnify either the diffraction pattern or the image. (**b**) Bright field micrograph of an amorphous area in silicon obtained by ion irradiation. (**c**) Cluster of point defects after rapid thermal annealing of (**b**). (**d**) Dark field of a twin defect in silicon obtained selecting the diffracted beam indicated in blue in the diffraction pattern (**e**). ((**b**–**e**) Reprinted from Mio et al. [4], with the permission of AIP Publishing)

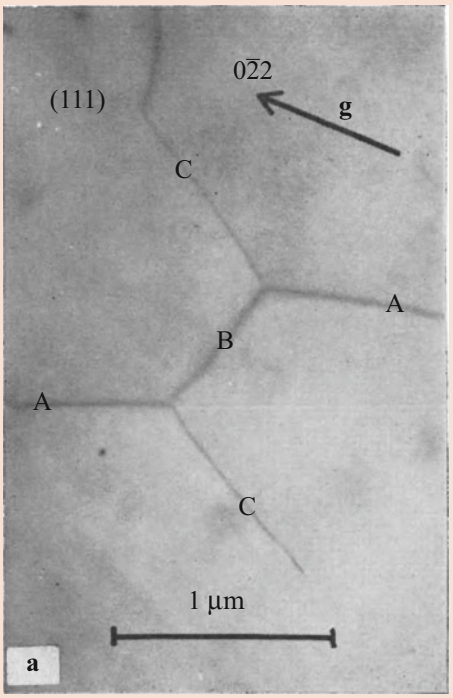
thickness, elements involved, crystalline phases, defects, etc. Indeed, until now we have presented a very simplified description. The system is actually very complex in terms of both data analysis and hardware. Specific textbooks are available for further insights [1, 2, 5, 6].

After interaction with the sample, the transmitted electrons can be exploited in several ways. For instance, by the use of particular lenses, the TEM user can obtain a magnified image of the sample from the undiffracted beam (bright field), Fig. 4.1b, c, or a diffraction pattern from a certain sample region (selected area electron diffraction pattern) or an image in which only electrons scattered/diffracted at a specific angle give a contribution (dark field) (Fig. 4.1d).

Conventional TEM is commonly used for extended defect characterization in the semiconductor. Main defects are dislocations and SFs. Dislocations are classified as pure edges, pure screws, or mixed, depending on the relative direction between the dislocation line and the Burgers vector, $\boldsymbol{b}$. CTEM allows the direction of $\mathbf{b}$ to be determined, through the $\boldsymbol{g}\cdot\boldsymbol{b} = n$ criterion [1, 2], where $\boldsymbol{g}$ is a vector of the reciprocal lattice and n is an integer.

This method is associated with the possibility of orienting the TEM sample, through a double-tilt TEM holder, in order to have only one diffracting beam $\mathbf{g}$, the so-called two-beam condition, in which the other beam is the undiffracted zero-order beam. If a dislocation fulfills the $\mathbf{g_1}\cdot\mathbf{b} = 0$ condition, i.e., $\mathbf{b}$ is perpendicular to $\mathbf{g_1}$, it disappears on both bright field and dark field micrographs [1, 2]. With a second $\mathbf{g_2}$ diffracting beam for which the dislocation disappears, $\mathbf{g_2}\cdot\mathbf{b} = 0$, the Burgers vector can be straightforwardly determined as $\mathbf{b} = \mathrm{k}\ \mathbf{g_1} \times \mathbf{g_2}$, where k is a real constant. An example of dislocation characterization is given in Fig. 4.2, where a dislocation completely disappears when a dark field is acquired selecting the -311 diffraction spot. However, several issues can affect CTEM contrast interpretation, even in this simple case. If $n > 0$, dislocation is characterized by double-line contrast [1, 7]. Excitation error from the diffraction condition, TEM lamella thickness, crystal anisotropy, dislocation type, and dislocation depth may also alter the contrast, making it difficult to exploit the $\boldsymbol{g}\cdot\boldsymbol{b} = n$ criterion [1, 8].

The CTEM contrast also permits the analysis of SFs with their typical fringe contrast. Figure 4.3 is obtained taking a



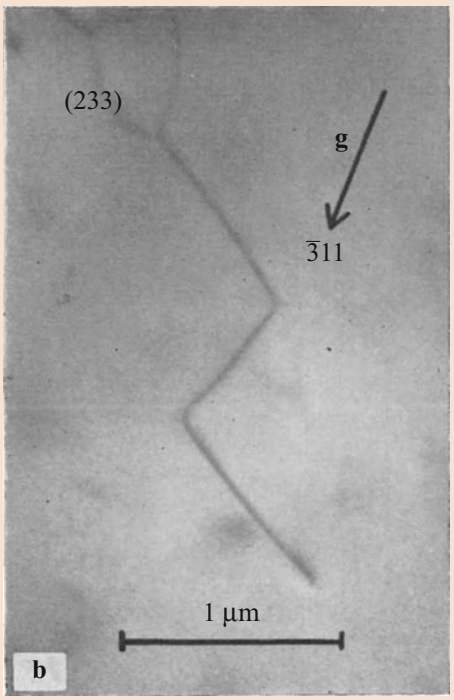


Fig. 4.2 Network of dislocations in Si with a nearly pure screw character. Dislocation lines are marked with A, B, and C. In (**a**) a dark field taken in 0–22 is shown. Under this condition the three dislocations are visible. On (**b**) the dark field is taken on the −311 and the A dislocation vanishes. This is consistent with a screw dislocation with Burgers vector ½[0–11]. (Republished with permission of the Royal Society of Chemistry, from Booker [9]; permission conveyed through Copyright Clearance Center, Inc)

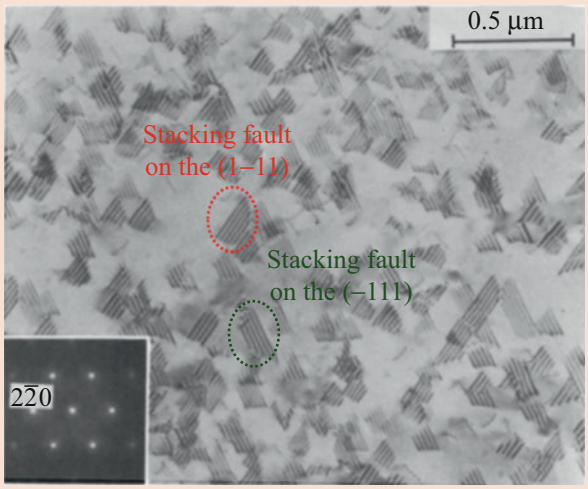


Fig. 4.3 Dark field taken in 2–20 of (111) Si sample amorphized by ion irradiation (10^{16} Si^+/cm^2 at 200 keV performed at 77 K) and then recrystallized by laser annealing (2.5 J/cm^2 of a Q-switched Ruby laser, 50 ns single pulse). Fringes indicate buried stacking faults. (Adapted by permission from Springer Nature Customer Service Centre GmbH: Springer Nature, *Applied Physics* [10], Copyright 1978)

dark field on the spot 2–20 along the [1–11] zone axis. Under this condition, buried SFs on the plane (1–11) and (−111) are visible. Their projection is emphasized by a contrast modulation, whereas SFs on the (11–1) are hidden.

Transmission electron microscopy is also a valid aid for investigating the dynamics of material processes at the nanoscale. With an in situ holder, it is possible to explore the behavior of the specimen under externally induced stimuli (thermal heating, electrical/optical pulses, mechanical stress, etc.).

Figure 4.4a shows a plain-view TEM micrograph (bright field) of $Ge_2Sb_2Te_5$ 100-nm amorphous regions surrounded by crystalline $Ge_2Sb_2Te_5$ in the trigonal phase. The amorphous regions were obtained by ion irradiation using an electron beam lithography mask to produce selective damaging. The sample is then annealed in situ at 90° C and imaged several times (Fig. 4.4b–d). It is therefore feasible to follow the kinetics of the recrystallization, inferring the absence of nucleation and measuring the regrowth velocity. As this geometry (nano-amorphous regions embedded in a crystalline matrix) is typical of $Ge_xSb_yTe_z$ (GST)-based nonvolatile memories (CDs, DVDs, Blu-ray, PC RAM), this result is quite critical to understanding the data retention limit of such devices.

4.1.2 Scanning Transmission Electron Microscopy

Although CTEM is a powerful tool for observing and characterizing extended defects, the technique exhibits several

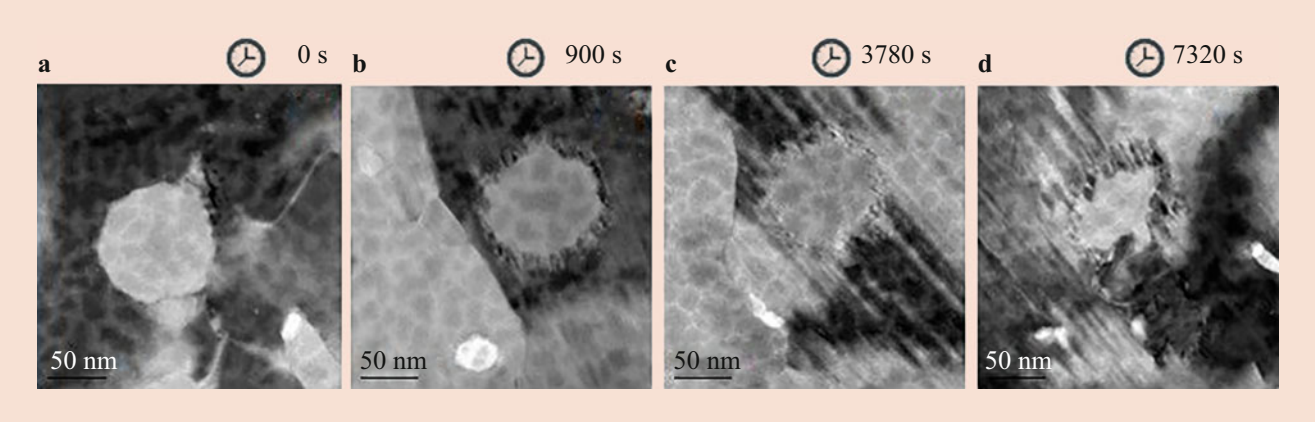


Fig. 4.4 Plain-view TEM micrographs (bright field) of 100-nm wide regions of amorphous $Ge_2Sb_2Te_5$ surrounded by crystalline $Ge_2Sb_2Te_5$ in the trigonal phase during in situ isothermal annealing at 90 °C. Crystalline regrowth proceeds from the a–c interface at the expense of the amorphous phase. (Republished with permission of IOP Publishing, Ltd., from Mio et al. [11], Copyright 2012; permission conveyed through Copyright Clearance Center, Inc.)

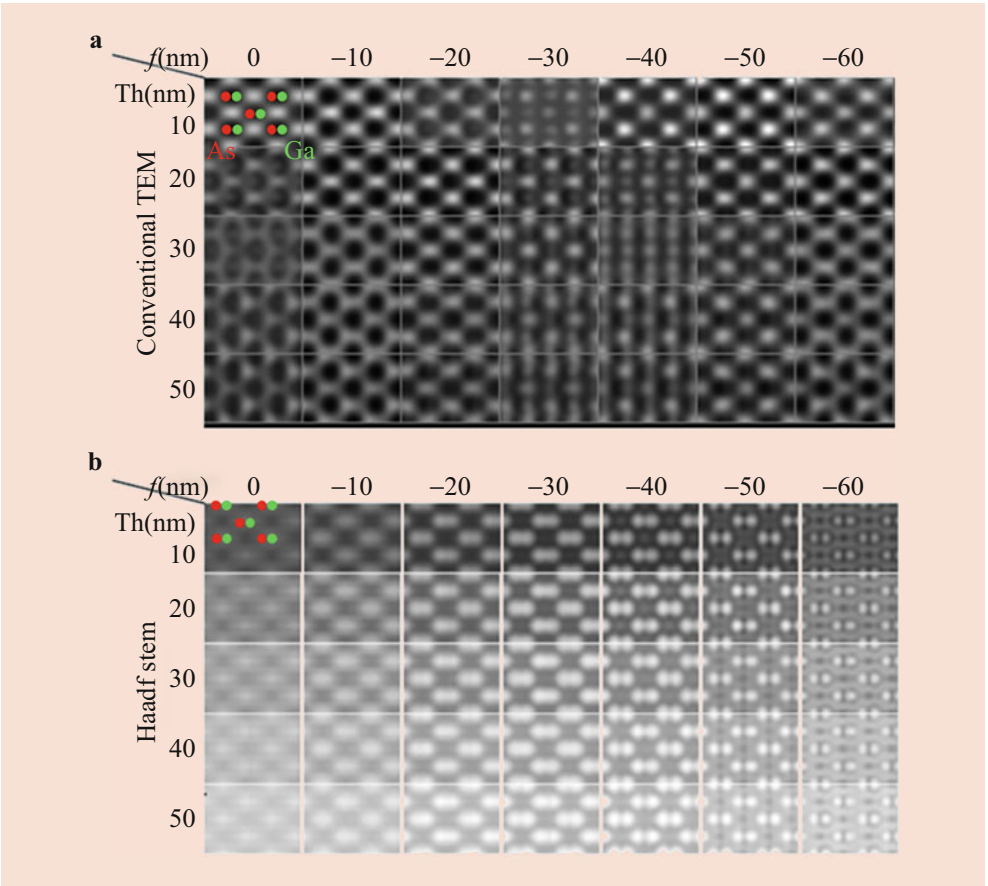


Fig. 4.5 (**a**) Conventional transmission electron microscopy simulation of GaAs bright field along the [110] zone axis (ZA). The micrograph contrast strictly depends on focus and sample thickness, resulting in a very hard comparison with the theoretical predictions. (**b**) High angle annular dark field scanning transmission electron microscopy simulation of GaAs bright field along the [110] ZA. The atomic positions As and Ga are indicated with red and green circles respectively. (Reprinted from Lamberti and Agostini [6], with permission from Elsevier)

limitations when the investigation is interested in a very local area, namely, below the nanoscale, toward the atomic scale. As the resolution of CTEM microscopes is usually 2–3 Å, the atomic structure cannot be resolved. Micrographs

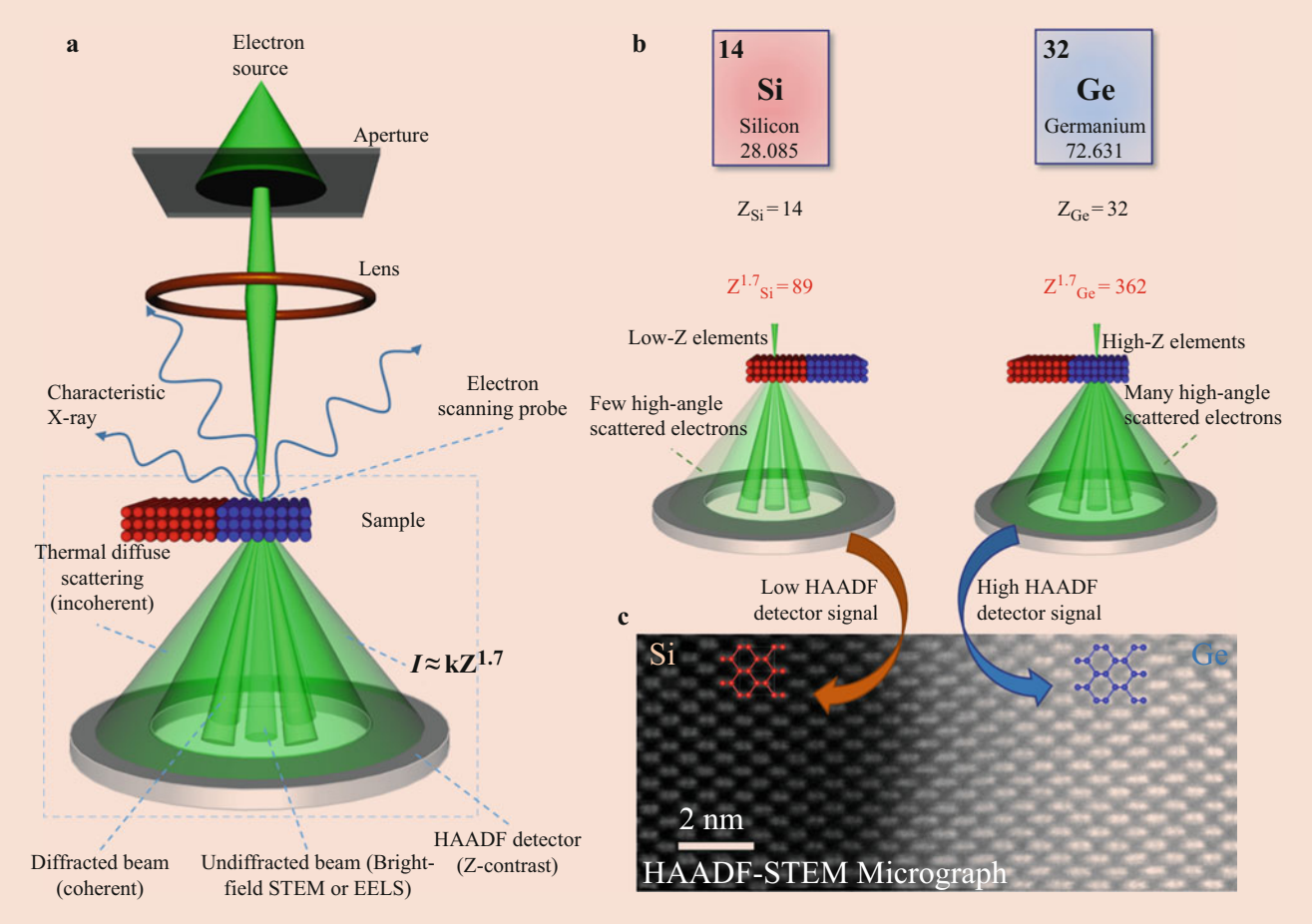


Fig. 4.6 (**a**) Schematic of scanning transmission electron microscopy (STEM): imaging and nano analysis. (**b**) High angle annular dark field STEM of the Si/Ge interface. Z-contrast permits Si and Ge to be distinguished and their atomic arrangement to be visualized. (**c**) A direct comparison with the theoretical atomic structure and the experimental raw data is shown. Si and Ge are represented with red and blue spheres respectively

are influenced by electron wave phase contrast. The strong electron beam–specimen interaction prevents a direct correlation of the intensity acquired on the phosphor screen or on the charge-coupled device with the specimen's atomic potential. In fact, the mapped intensity depends noticeably on the adopted focus and on the sample thickness as shown in Fig. 4.5a. The sample thickness should be less than 20 nm, to guarantee electron transparency, reduce inelastic scattering, and achieve better image quality. These conditions can drastically reduce the probability of selecting a particular localized defect during sample preparation.

The reduction of the effects of aberrations requires quite small objective apertures, which further influence the contrast modulation. As the intensity of the final image depends on the electron wave functions interference and on their heterogeneous dephasing, due to aberrations, or wave front cutting, due to apertures, direct micrograph interpretation is quite hard. Indeed, even changing two simple parameters, such as focus (i.e., the simplest aberration) and thickness, complete contrast inversion can occur [6, 12], as shown in the simulation reported in Fig. 4.5a. In fact, it is quite difficult in the case of interfaces to clearly define atomic positions below 3 Å. The periodicity of the crystalline lattice is preserved in the image, whereas the atomic position is generally shifted from the exact one.

In addition, with a parallel beam, it is quite difficult to perform chemical analyses, in particular in the case of high-Z elements for which energy-filtered transmission electron microscopy maps contain very weak signals.

In the last decade, STEM has been held up as a valid alternative to CTEM, as it is able to overcome the aforementioned limits. Although the first STEM was developed at about the same time as the first TEM, starting from the 1930s, for historical and technical reasons, its potential was only shown in 1970, when Albert Crewe used it to show single heavy atoms resting on a thin carbon substrate [13].

The working principle of STEM is very similar to that of scanning electron microscopy (SEM). A very narrow

electron probe is scanned over the sample (Fig. 4.6). From the electron–specimen interaction, characteristic X-rays are also produced and used for EDX mapping. The EELS of the transmitted beam also provides further information on the elemental composition at the nanoscale.

Bright-field STEM micrographs are acquired mapping point-by-point the signal (number of electrons) obtained from the direct transmitted beam. A dark-field image is obtained in a similar way collecting the electrons scattered at different angles. Typically, low-angle annular dark field detects electrons scattered from about 30 mrad, whereas those scattered at more than 50 mrad impinge on the so-called high-angle annular dark field (HAADF) [2].

One of the key advantages of STEM is the so-called Z-contrast, peculiar to the HAADF mode. In this setup the number of electrons impinging on the annular detector is roughly proportional to $Z^{1.7}$ [14]. The presence of an advanced spherical aberration corrector, available on the market since the 2000s in the last generation of microscopes, focus the electron probe well below 1 Å. This permits a direct image of an atomic structure and a direct comparison of the unprocessed micrograph with the theoretical atomic model. Quite interestingly, on the contrary with respect to the CTEM behavior, the contrast of an atomic HAADF micrograph does not strictly depend on the defocus and on sample thickness, as shown in the simulation reported in Fig. 4.5b.

Figure 4.6c shows a ball-and-stick representation of an interface between Si (Z = 14) and Ge (Z = 32), seen along the [110] ZA overlapped with a corresponding HAADF-STEM micrograph (raw data). The contrast difference between the two elements is straightforward, as well as the direct comparison with the atomistic model.

Also, for conventional semiconductor HAADF-STEM, direct imaging provides useful information on the structure of defects. Figure 4.7 shows, for comparison, a HAADF-STEM and a CTEM of 60°–60° dislocations in Ge near to an interface with Si. HAADF-STEM identifies the dislocations and their atomic position. Moreover, HAADF-STEM Z-contrast clearly distinguishes Si atoms (Z = 14) from Ge atoms (Z = 32).

In the case of SFs, HAADF-STEM permits the direct observation of their formation/annihilation mechanism, also giving insight into the local atomic rearrangement, especially near the region where different defects interact with each other. Figure 4.8a shows a series of SFs annihilated through the intersection of two {111} SFs. Figure 4.8b shows an antiphase boundary. The details of this defect are quite difficult to observe in CTEM, because the Bravais lattice remains unchanged. In the polytype 3C-SiC, the repetitive unit is a Si-C couple. When an antiphase boundary occurs, there is a flip between the Si and the C lattice site, but each unit position remains the same. As the Z-value difference between the two elements, HAADF-STEM clearly emphasizes this kind of change.

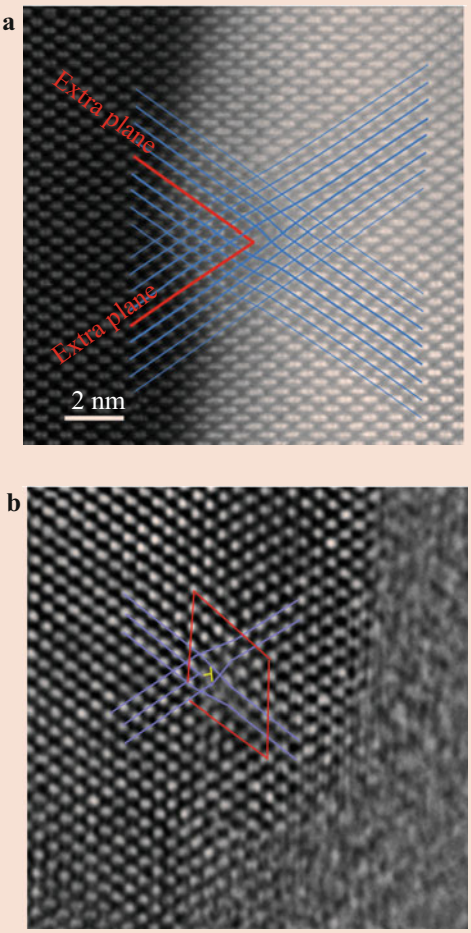


Fig. 4.7 (**a**) High-angle annular dark field scanning transmission electron microscopy micrograph, of a Si/Ge interface. Through Z-contrast, two misfit dislocations are clearly visible. (**b**) Conventional high-resolution TEM analysis. A pair of dislocations is also visible, but the atomic details are lost and the imaged bright spots are generally shifted with respect to the exact atomic position

A complex case of Z-contrast detection along the [110] ZA of $Ge_2Sb_2Te_5$, in the metastable rock-salt phase, is shown in Fig. 4.9a. In this ZA, the material stack follows an anion-cation-anion-cation layer pattern. The anion columns are composed only of Te atoms ($Z_{Te} = 52$), whereas the cation atoms are formed by randomly mixed Ge and Sb atoms and ≈20% of vacancies. Owing to the difference in atomic number between the two elements ($Z_{Sb} = 51$, $Z_{Ge} = 32$), the cations column will be brighter if the amount of Sb exceeds that of Ge. The measured spacing between two Te planes, with an intermediate plane of Ge/Sb, amounts to about 3.5 Å.

The vacancies in the cation sub-lattice play a relevant role in the electrical conductivity [16], being responsible for an unexpected metal-insulator transition (MIT) upon their ordering. This ordering happens when the GST system goes toward its stable trigonal phase, even if it is not necessary to fully reach this final state to have the MIT

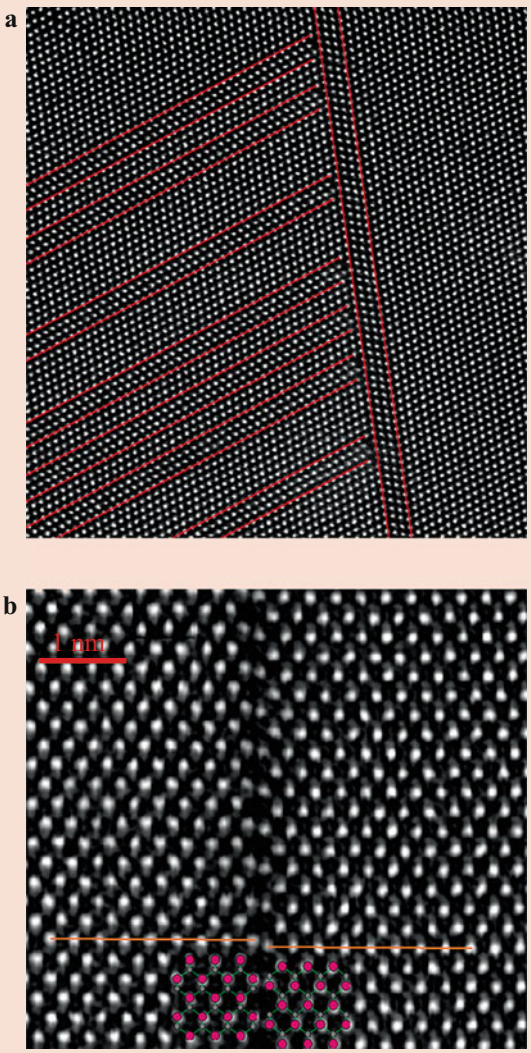


Fig. 4.8 3C-SiC High-angle annular dark field scanning transmission electron microscopy micrographs in [110] zone axis. (**a**) The annihilation of stacking faults (SFs) through the intersection of two {111} SFs (red lines) and (**b**) an antiphase boundary. Orange lines indicate the misalignment of Si atoms. A ball-and-stick sketch is shown to emphasize the Si(magenta)-C(gray) inversion

transition [17]. This property offers the opportunity to fabricate multi-level memories, encoding several resistance levels as well as different thermal resistance coefficients, maintaining lower power consumption. The same mechanism has been recently exploited to fabricate neuro-inspired prototype devices. By increasing the annealing temperature or changing the deposition parameters, the vacancies embedded in the rock-salt structure move away from the cationic sublattice and order in planes [18]. This process supports the crystal–crystal phase transition, from the metastable rock-salt phase to the stable final trigonal structure, characterized by vacancy-rich layers, the so-called van der Waals (vdW) gaps.

Cross-view HAADF-STEM micrographs of a sample prepared in the trigonal phase by epitaxial growth is shown in Fig. 4.9b. The image clearly shows dark layers that correspond to vdW gaps between two Te planes [19], as evidenced by the orange dashed lines. In the same micrograph, a twin defect is well recognizable. The image also provides compositional information. VdW gaps separate the alloy into blocks of different sizes, 9 and 11 layers respectively (see Fig. 4.9b), and each size corresponds to a different GST local stoichiometry. Blocks of 11 layers correspond to $Ge_3Sb_2Te_6$, blocks of 9 layers to $Ge_2Sb_2Te_5$. HAADF-STEM is therefore a very precise technique for detecting local variation in the stoichiometry.

STEM Nanoanalysis

Scanning transmission electron microscopy also offers significant microanalysis capabilities, as it is possible, at the same time, to acquire the aforementioned EDX and EELS signals [20] at the nanometer or even at the atomic scale using thin samples. As a rule of thumb, EDX is very effective at detecting high-Z elements, whereas EELS is better for low-Z atoms. Nowadays, however, new EELS detectors have an improved detection limit and sensitivity at higher energy loss, thus allowing the chemical characterization of heavy atoms with high core ionization energy.

An example of the simultaneous use of these different techniques is the analysis by HAADF-STEM and mapping by EDX of an AlGaAs multishell nanowire reported in Fig. 4.10. Al-rich areas are darker as Al is lighter ($Z = 13$) than both Ga and As ($Z_{Ga} = 31$, $Z_{As} = 33$). For the same reason, pure GaAs regions are brighter. EDX is a fundamental aid for locating elements at the atomic positions. Indeed, this should not be possible using only Z-contrast as the atomic numbers of Ga and As are too close.

The simultaneous EDS and STEM nanoanalysis in chalcogenides has recently permitted the correlation of structural defects with atomic stoichiometry heterogeneities. As already pointed out, different composition blocks, corresponding to the following local GST stoichiometries Sb_2Te_3 with five layers, $GeSb_2Te_4$ with seven layers, $Ge_2Sb_2Te_5$ with nine layers, $Ge_3Sb_2Te_6$ with 11 layers, etc., are present in a chalcogenide layer. These different blocks are connected via a particular kind of defect, called a bi-layer defect [21] (Fig. 4.11a, white box), which is very common in chalcogenides. They probably play a crucial role in layered GST used for interfacial phase change memory (iPCM) devices [22, 23], possibly enabling the swapping of two (or more) memory bits [21]. Indeed, these devices are supposed to switch between two resistance levels thanks to a crystal-to-crystal transition that could be promoted, changing for instance the block size through a bi-layer defect.

One key point is to understand how cations and anions are distributed along these defects. Although Ge and Te can be

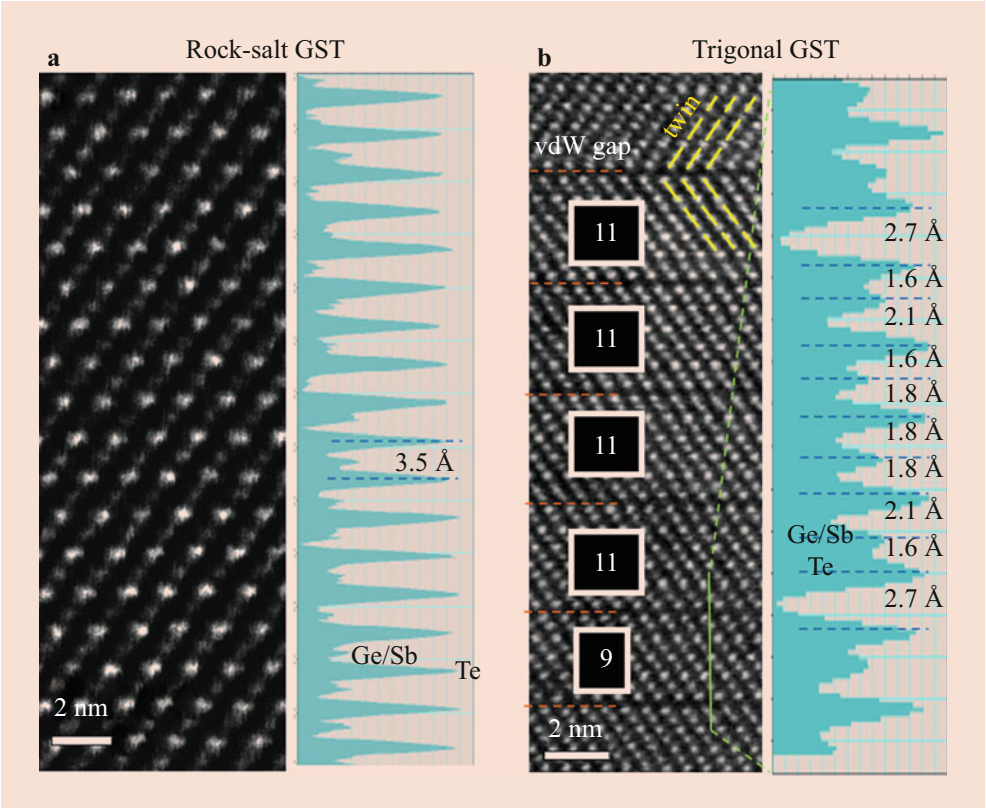


Fig. 4.9 High-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) micrograph of (**a**) rock-salt $Ge_xSb_yTe_z$ (GST) in the [110] zone axis (ZA). A line profile along the whole micrograph is also shown. (**b**) HAADF-STEM micrograph of epitaxial trigonal GST in the [11–20] ZA. Van der Waals gaps are clearly visible and highlighted by the orange dashed lines. Blocks of 9 and 11 planes are indicated, as well as a twin defect. (From Mio et al. [15], © IOP Publishing. Reproduced with permission. All rights reserved)

easily distinguished by Z-contrast, Sb and Te are too close in atomic number to be separated; therefore, another nanoanalysis technique is required. Very recently [21], thanks to the simultaneous detection of HAADF and EDX, these defects have also been chemically characterized. Figure 4.11 reports this mapping for $GeSb_2Te_4$. In particular, EDX mapping shows an intermixing of Sb and Te in the bi-layers.

As mentioned above, another technique often employed in STEM nanoanalysis is EELS. Compared with EDX, EELS has in general better detection for light elements and an energy resolution within the range of some tens of milli electron volts (the EDX resolution is ≈150 eV). The low energy loss sensitivity is thus relevant for plasmon detection and energy gap measurements. Moreover, EELS permits not only elements to be distinguished but also their chemical bonding. This technique is called energy loss near edge structure (ELNES) and is an excellent alternative to the X-ray approach of synchrotron light, as it has higher spatial resolution.

Figure 4.12 shows a series of EELS spectra at angstrom-scale resolution and the corresponding STEM image of C layers formed by graphitization at a high annealing temperature of SiC [24]. The electronic properties of each layer are studied by analyzing the intensity of the K-edge (Fig. 4.12a), and the shape of the ELNES. Two peaks compose the K edge of graphitic carbon (or graphene): the first, at 285 eV, corresponds to the 1s to π* electronic transition, associated with the sp^2 hybridization; the second at ∼295 eV indicates the presence of sp^3 hybridization (1s to σ*). σ* feature is sharp in crystalline graphitic C, whereas it is round and broader in amorphous or not pure C. The spectra show the formation of pure graphene on the surface of SiC (see the green, blue, and orange spectra respectively). In the first layer over the (0001) surface side (red spectrum) the π* intensity drops, owing to the sp^3 hybridization, typical of a buffer C layer with a strong bonding with the outermost Si atoms of the underlying SiC [25]. The absence of this bonding upon the $\left(11\bar{2}n\right)$ facets revealed a delamination of the buffer layer entailing the formation of pure graphene. This result helped to theoretically argue that the formation and stability of a buffer layer on top of the $\left(11\bar{2}n\right)$ steps of an off-axis SiC substrate correlates inherently with the angle between the (0001) and $\left(11\bar{2}n\right)$ planes [24].

While rastering the electron beam across a bi-dimensional area of the sample with the STEM probe, EELS spectra have been first collected pixel by pixel, of angstrom size,

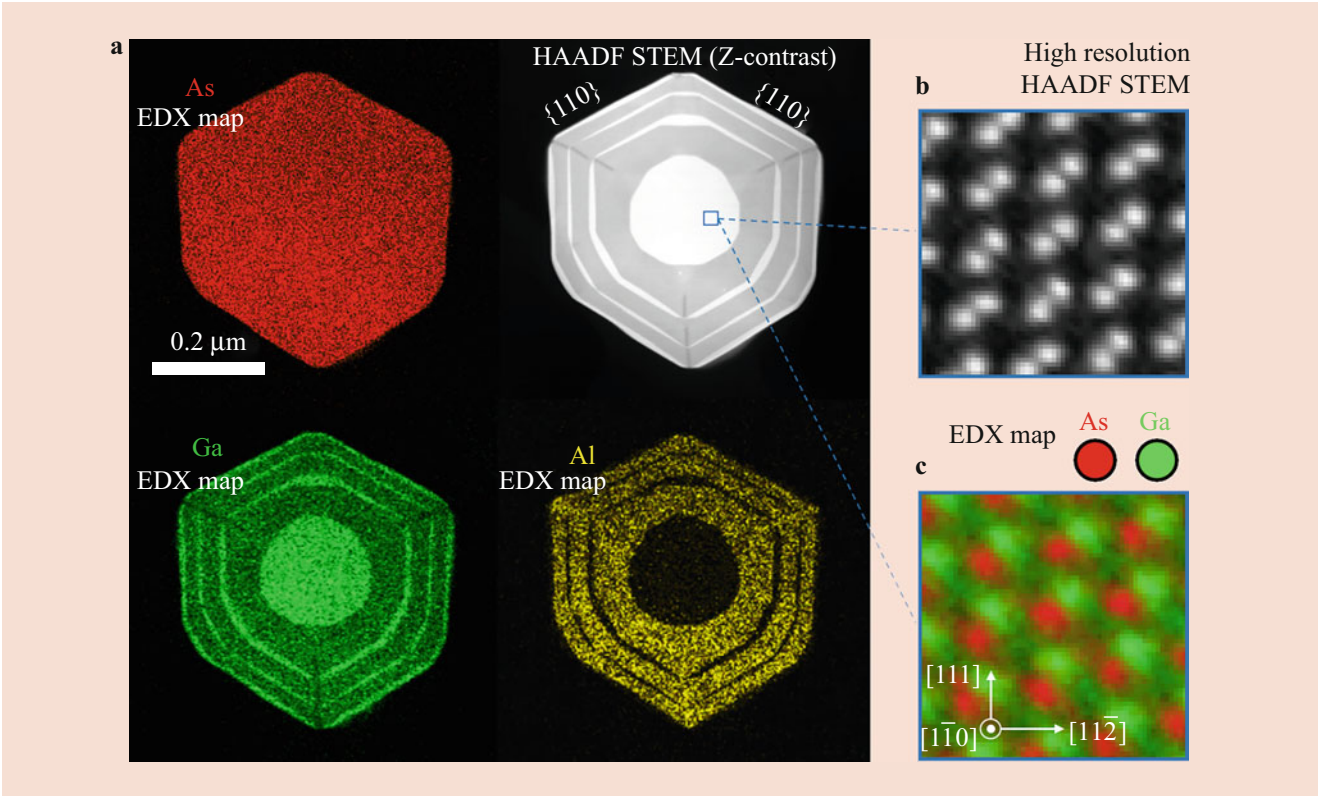


Fig. 4.10 (**a**) High-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) micrograph of an AlGaAs multishell nanowire (cross-view) and the corresponding energy-dispersive X-ray (EDX) maps. In HAADF-STEM, the dark gray areas are associated with the Al-rich regions, i.e., the lighter element in the system. (**b**) High-resolution HAADF-STEM of a pure GaAs region. As the two elements have very close atomic numbers ($Z_{Ga} = 31$ and $Z_{As} = 33$), they are indistinguishable by Z-contrast. Their identification can be performed through simultaneous EDX mapping nanoanalysis, as shown in (**c**). (Courtesy of Mario Scuderi)

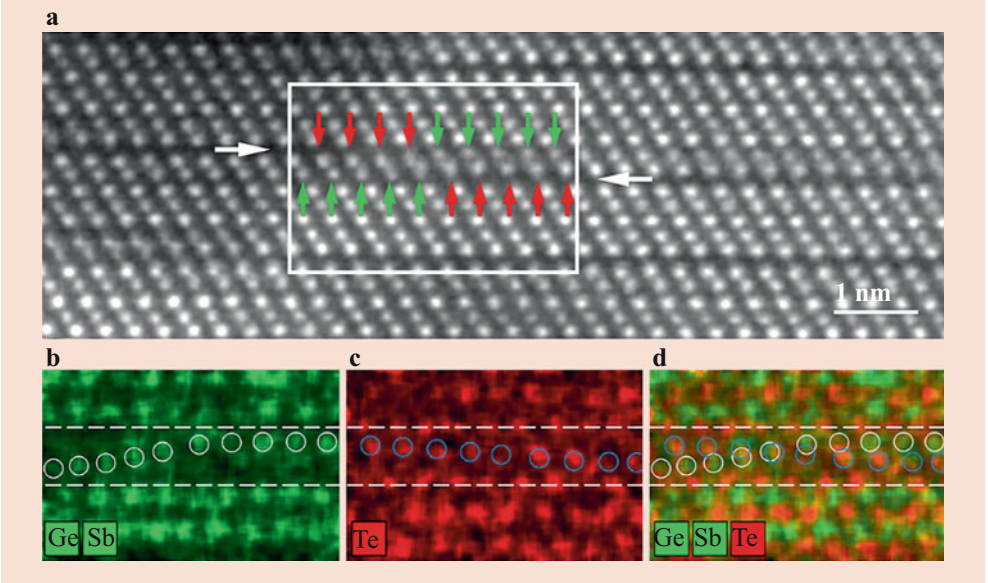


Fig. 4.11 The high-angle annular dark field (HAADF) image and the corresponding energy-dispersive X-ray (EDX) mapping of a bi-layer defect in a GST film. (**a**) HAADF image of bi-layer defect. Green and red arrows mark the Sb-rich and Te-rich layer respectively. (**b**–**d**) The corresponding EDX mappings of the area inside the white box marked in (**a**). The centers of each Ge/Sb and Te atomic column are marked with white and blue circles respectively. A smooth and continuous crossing of the Sb-rich and Te-rich layer is observed. The overlaid EDX mapping in (**d**) also indicates some intermixing of Sb and Te in the bi-layers. (Adapted with permission from Wang et al. [21], Copyright 2018 American Chemical Society)

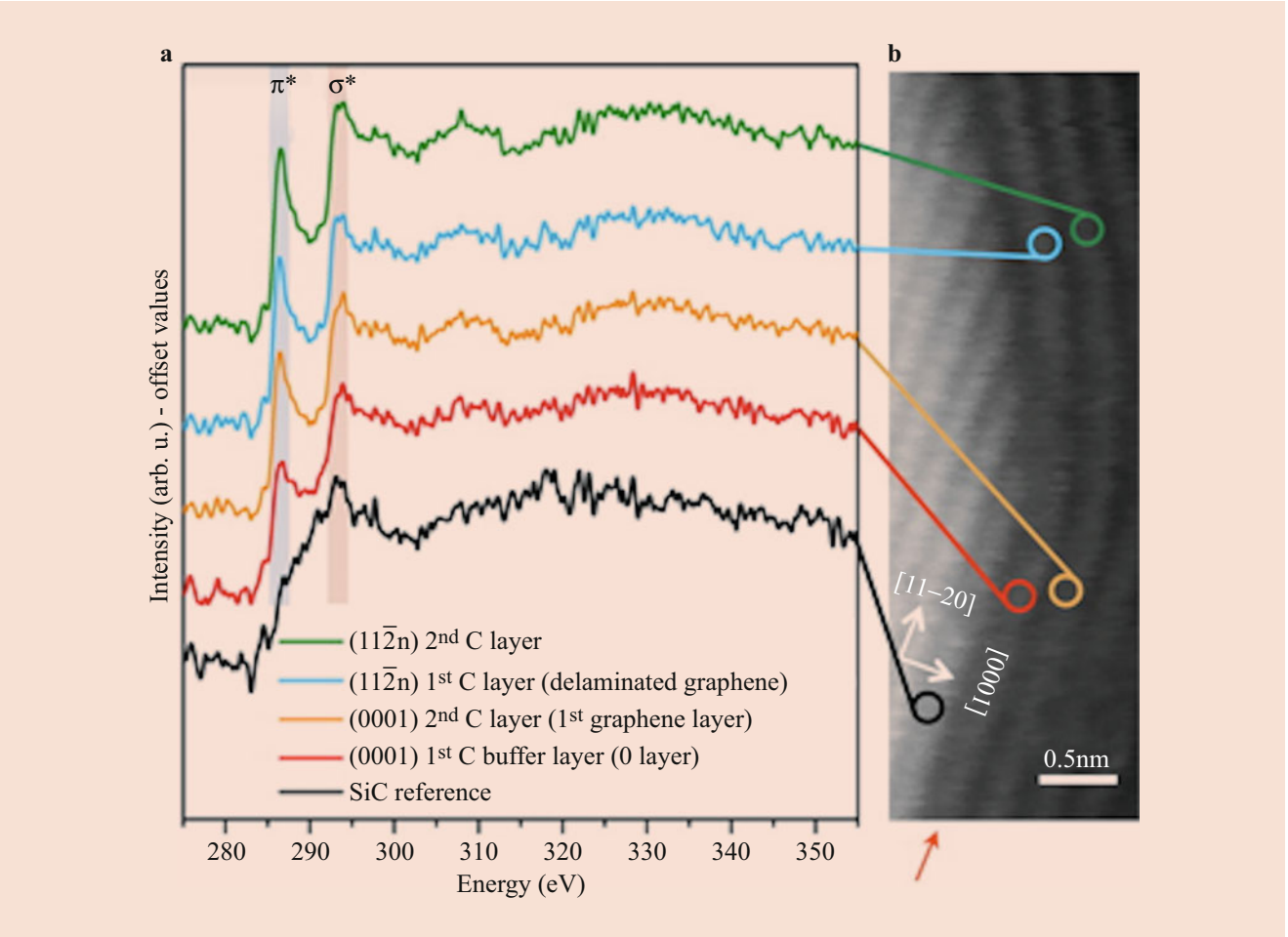


Fig. 4.12 (**a**) Spatially resolved electron energy loss spectroscopy in the K-edge of C, acquired in correspondence of different graphene layers, and (**b**) the related high-angle annular dark field scanning transmission electron microscopy micrograph. (Adapted with permission from Nicotra et al. [24], Copyright 2013 American Chemical Society)

together with the corresponding HAADF signal (Fig. 4.12b). The spatial and energy data form a three-dimensional array called a data cube. Figure 4.13 shows a schematic of this procedure, taking the name STEM spectrum imaging (SI). Once the data cube has been filled up and stored, information can be extracted and the pixels binned along a segment or a bi-dimensional region in order to average and to increase the signal-to-noise ratio (SNR). Moreover, it is possible to extract compositional information from the elemental characteristic core-loss spectrum, considering the integrated signal produced in this spectral region and reassembling this signal value in a spatial bi-dimensional chemical map. Point-by-point, the signal intensity of each pixel is proportional to the chemical concentration of the observed element.

Depending on the microscope configuration, other techniques can be combined simultaneously such as EDX, cathode luminescence (CL), nano-diffraction (ND), and electron-beam-induced current (EBIC). The set of collected data is stored in a multidimensional matrix called a dataset instead of a data cube, where the matrix Δx by Δy maps the spatial STEM signal, usually the HAADF, and the Δz_n dimensions (where n is an integer correlated with the maximum number of associated techniques) encode the information acquired by the other techniques, including energy histograms for EELS or EDX, current values for EBIC, etc. A key advantage of STEM SI is therefore the possibility of processing a whole range of data *a posteriori*.

The study of the ELNES at the interface level gives direct information on the presence of dopants, defects, as well as of details on the bonds at the atomic scale. As an example Fig. 4.14 reports the analysis of HAADF-STEM and EELS SI techniques to localize stoichiometric defects at the 4H-SiC/SiO_2 interface. These defects are responsible for near-interface oxide traps [26]. The investigation of the semiconductor/dielectric interface is crucial to improve the performances of metal-oxide-semiconductor field effect tran-

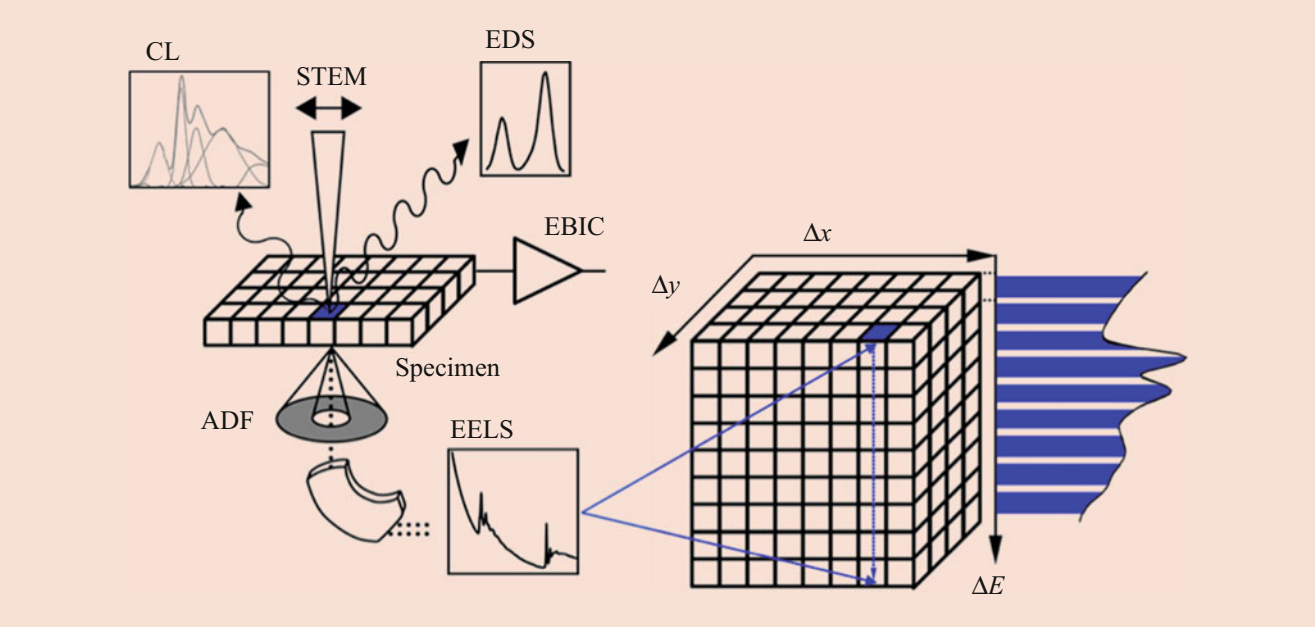


Fig. 4.13 Scanning transmission electron microscopy (STEM) spectrum imaging setup. A multidimensional array, the dataset is acquired pixel by pixel by scanning the STEM probe over a chosen bi-dimensional area. The STEM detector signal is stored in the Δx by Δy matrix. Data from a number of complementary techniques, such as electron energy loss spectroscopy, energy-dispersive X-ray, cathode luminescence, and electron-beam-induced current, are stored in the z_n dimensions

sistor (MOSFETs). Through EELS SI, spectra are acquired and collected in a data cube. Binning of the pixels is applied over rectangular regions (see inset in Fig. 4.14d) whose size is small enough to preserve the required spatial resolution but still sufficient for a good SNR. Figure 4.14d shows EELS spectra extracted from the SI dataset and integrated within the above rectangular regions located over three regions: the SiC bulk (blue), the interface between SiC and SiO_2 (red), and the SiO_2 (green). The energy of acquisition for all the EELS spectra ranged between 95 eV and 560 eV, wide enough to include all the chemical species of interest, i.e., Si, C, N, and O. The presence of a weak nitrogen K-edge peak, produced by post-oxidation annealing in NO, is revealed by an accurate background subtraction followed by multiple linear least squares fitting of the spectra.

From the software post-processing of the acquired SI dataset, the signals due to the chemical species (core-loss) are extracted and plotted in the two-dimensional chemical map, as reported in Fig. 4.14b. N accumulates at the transition layer between SiC and SiO_2. In order to localize the exact position of the N layer, the line intensity scan of each chemical signal is plotted and compared with that obtained from the Z-contrast HAADF-STEM image, which shows the exact position of the interface. All the line intensity profiles are reported in Fig. 4.14c. The analysis of the different signals indicates that nitrogen is trapped just below the last SiC atomic layer of the bulk crystal.

The smooth behavior of the other elements distribution along the interface is then confirmed by the chemical EELS analysis, indicating that SiC gradually gives way to nonstoichiometric SiC, in which C atoms are substituted with N and then with O. This is supported by the EELS chemical bond analysis for the C, K-edge (Fig. 4.14e). With respect to the SiC bulk, in the transition region the σ^* signal of carbon decreases and, at the same time, a non-negligible amount of π^* is present. This supports a mixed sp^2/sp^3 hybridization coordinating C with silicon, oxygen, and nitrogen atoms. The mixture is maintained for more than 1 nm from the nominal interface, before having a fully stoichiometric SiO_2.

4.2 X-Ray Analytical Techniques

X-ray-based techniques exploit the capability of the electromagnetic waves to deeply penetrate and interact with matter, thus providing structural information in their outgoing path. In this section, the main characteristics of the technique are illustrated, including a description of common apparatus. New frontiers of X-ray diagnostics extend the investigation to nanostructured materials taking benefit from the use of monochromatic and high-brilliance sources, and likewise from the development of modern analytical methodologies. As examples of thin film systems, the crystallization of a GeSbTe thin layer from the amorphous to rock salt and finally

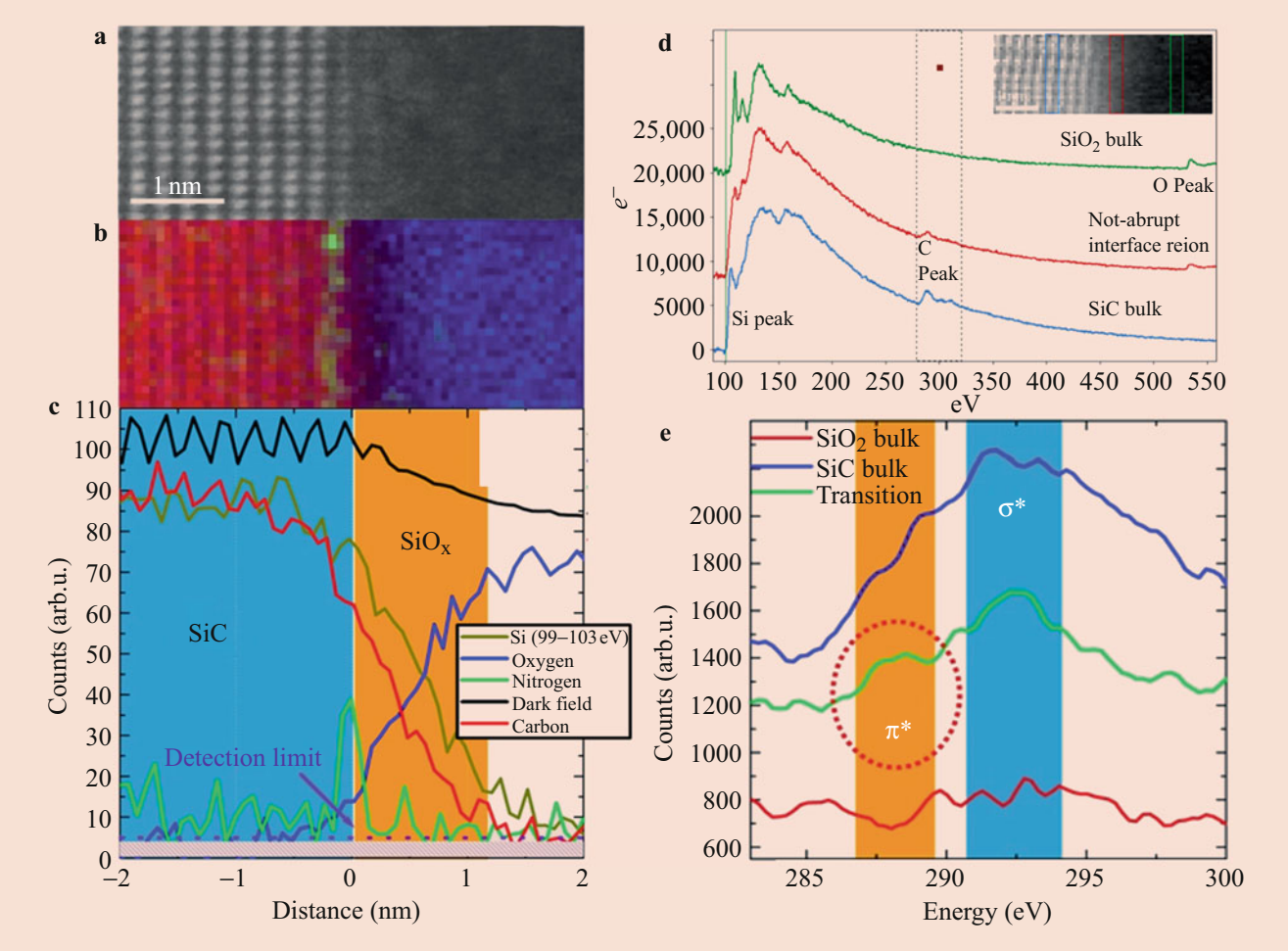


Fig. 4.14 (**a**) High-resolution dark-field cross-section scanning transmission electron microscopy (STEM) image across the SiO_2/4H-SiC interface. (**b**) Carbon, oxygen, and nitrogen superimposed electron energy loss spectroscopy (EELS) maps. (**c**) Dark-field signal, silicon, carbon, oxygen, and nitrogen EELS spectra averaged on all the scanned lines; bulk SiC is highlighted in light blue and the not-abrupt interface region in orange. In (**d**) raw EELS spectra are shown, in a wide energy range comprising silicon, carbon, and oxygen edge. The signal intensity is related to the element composition. In (**e**) EELS spectra of the carbon K-edge are shown, after background subtraction. The detail of the edge gives information on the contribution of the σ* and π* chemical bounds. (From Fiorenza et al. [26] © IOP Publishing. Reproduced with permission. All rights reserved)

to trigonal structure is tracked by the position/shape analysis of the diffracted peaks, the heteroepitaxial coupling of thin polycrystalline layers of silicides on (001) bulk silicon is investigated by polar figure analyses. In particular, the X-ray diffraction details the NiSi complex structure. Other reported studies are concerned with the shape-related analysis of silicon nanoparticles under high-resolution conditions; the stress field due to residual defects in ion implanted and annealed germanium wafer; and the formation and evolution of defects during the growth of thick monocrystalline layers (e.g., 3C-SiC, GaN). Nowadays, controlled growth of high-quality bulk and epitaxial semiconductors (SiC, GaAs, GaN, AlGaAs, etc.) represents a challenge for further advances in device architecture and performance following the previous narrative with silicon.

4.2.1 X-Ray Characteristics and Common Experimental Apparatus

The mainstay of X-rays resides in their associated wavelength being comparable with the atomic size and distances in the matter, which allows the wave front to be sensitive to the overall atomic arrangement. The outcoming beam indeed holds key information related to the lattice architecture and associated phases (interplane distances, lattice parameters, bond distances), to defects and accumulated strain, to the grain or nanoparticle size, mosaicity and texturing, to the electronic density, to the layer thickness and roughness, and to the material porosity. Depending on the method of decryption of the information, X-ray diffraction (XRD), reflectivity (XRR), scattering (WAXS and SAXS: wide-Angle and small

X-ray scattering), absorption (XAS: X-ray absorption spectroscopy), or fluorescence (XRF) techniques are dealt with. Although a degree of lattice order is required for diffraction, other X-ray techniques can even be applied to amorphous materials.

All mentioned methods can currently take advantage of exploiting high-brilliance sources at synchrotron radiation facilities. In conjunction with the more consolidated approaches, tomographic quantitative analyses by synchrotron radiation with progressively increasing resolution provides a representative case of current advances in the application of X-rays for materials at scaled dimensionality. Along the same track, laboratory equipment nowadays benefits from new-generation X-ray sources more frequently than in the past. The brilliance of a X-ray source, defined as the number of photons/second · mrad^2 · mm^2 · 0.1% BW (0.1% BW stands for the photons falling within a band-width of 0.1% with respect to the central wavelength) is $\sim 10^8$ in laboratory equipment, to increase to $\sim 10^{22}$ in synchrotron beam lines, as illustrated in Fig. 4.15a. In the same figure, a schematic of a laboratory *Kα*-Cu source with a wavelength of 1.5407 Å (Fig. 4.15b) and the penetration depth of this kind of beam into different materials (Fig. 4.15c) are also reported.

X-ray diffraction is a phenomenon based on the cooperative response of the matter under the external solicitation of an electromagnetic field with a wavelength within the angstrom range, in which each atom of the lattice behaves as a source of secondary spherical wave. If a medium- or long-range order is established, constructive interference among the outcoming waves is feasible at specific exit angles. Those angles are finally related to the interplanar lattice distances through the well-known Bragg's law (Fig. 4.16a). Diffraction intensities, linewidth, line-shape, and mutual peak positions provide detailed insights into the lattice properties of the probed matter.

High-resolution diffraction (HR-XRD) analyses of bulk materials and epitaxial layers require highly monochromatic beams. In laboratory Cu sources, the beam is accordingly wiped from its kα_2 components by the use of multiple-bounce germanium monochromators with improvement of the temporal coherence of the radiation. Point focus sources, high speed detectors, and the several rotational degrees of freedom of the setup are other key configurational parameters for spatially resolved HR-XRD (Fig. 4.16b). Multiple-axis X-ray diffractometers currently allow almost free movement through the reciprocal space for out-of-plane and in-plane

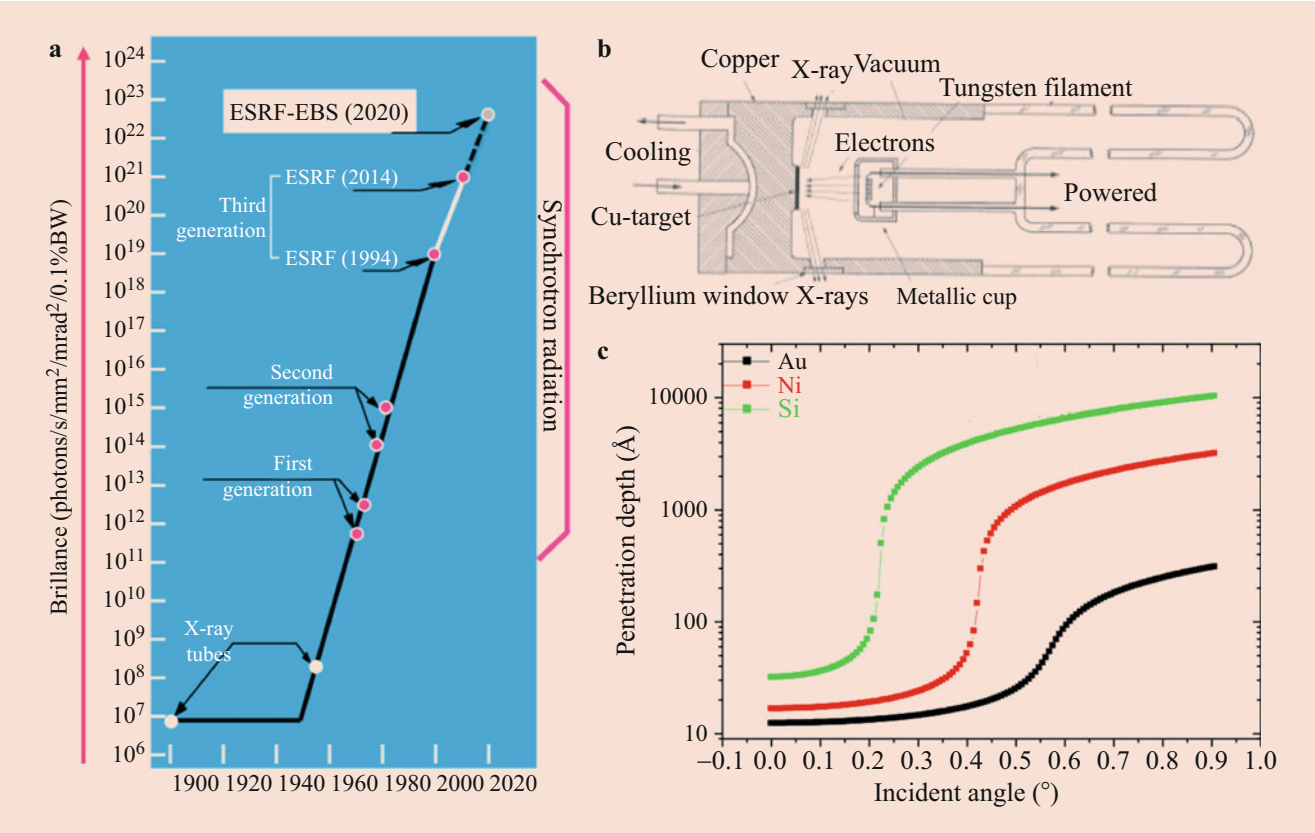


Fig. 4.15 (**a**) Brilliance of X-ray sources as reported in https://978-3-030-79827-7/www.esrf.eu/about/synchrotron-science/synchrotron-light. (**b**) Schematic of a laboratory Cu-based X-ray source (*Kα*-Cu wavelength = 1.5407 angstrom). (**c**) Penetration depth of a *Kα*-Cu beam into different materials as a function of the incident angle

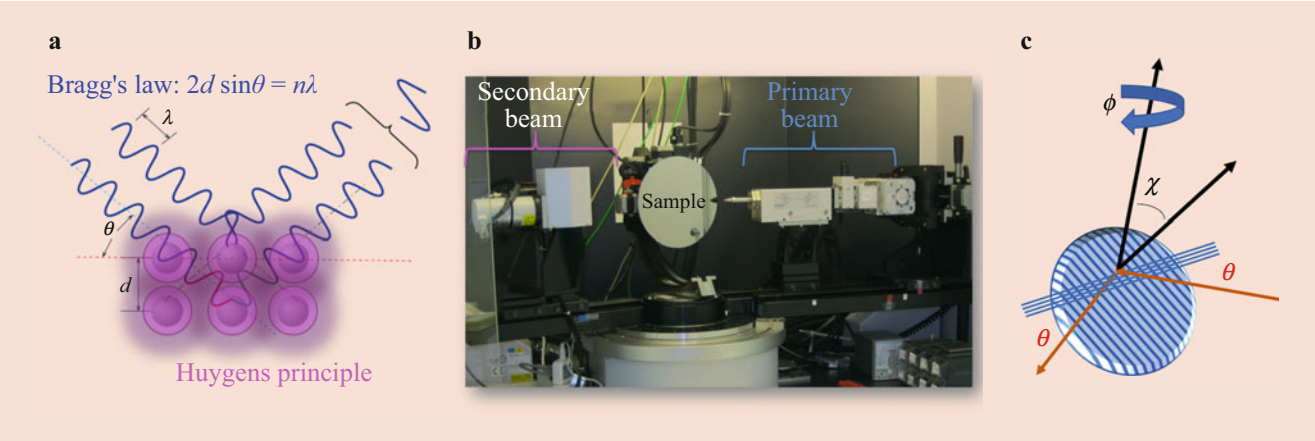


Fig. 4.16 (**a**) Schematic of the basic principle for X-ray diffraction (XRD) analyses. (**b**) Typical diffractometer setup (Bruker AXS) for high-resolution XRD. (**c**) Schematic of the typical degrees of freedom available in a diffraction setup

diffraction on the same probed area. The schematic of a typical multi-axis setup is shown in Fig. 4.16c. Shape and position analyses in the reciprocal space hand back information on internal stress, strain relaxation, displacement field around defects, compositional gradients, and mosaicity.

For polycrystalline thin films, a common analysis method is based on symmetrical $\omega - 2\theta$ scans, where the incoming primary beam and the outcoming secondary beam mirror with respect to the sample surface (ω is an angular parameter related to θ). With this geometry, the lattice planes stacked in the out-of-plane direction are detected. In order to instead access the in-plane components, φ and χ rotations are exploited, or, alternatively, an off-axis $\omega - 2\theta$ scan can be applied. Grazing incidence is tailored for thin-film analyses to partially confine the incoming beam into the probed layer. Figure 4.15c shows the penetration depth of a Cu-kα beam as a function of the incident angle in different materials. Rocking curves are ω-scans that complement the analyses on thin layers with information on the eventual preferential orientation (texturing) of the grains. In this case, polar figure analyses are carried out to provide key insights into the statistical distribution of diagnostic planes and on their eventual coupling with underlayers or bulk substrates. They are especially used for the heteroepitaxial structural coupling of materials.

4.2.2 Thin Film Analysis

GeSbTe Alloys

As a simple example of the X-ray potentialities, we report the analysis of the amorphous-crystal transition of the phase change alloy $Ge_2Sb_2Te_5$ viewed by out-of-plane diffraction [27] This transition is the basis of the working principle of optical or electronic nonvolatile memory. The amorphous phase is characterized by low reflectivity and high electrical resistivity, the opposite occurs for the crystalline phase. The high-low values correspond to 0 or 1 as binary code.

The crystallization of 50 nm-thick amorphous films deposited on a Si substrate is shown in Fig. 4.17a as a function of thermal annealing at 122 °C for different times. The analyses are carried out at a grazing angle <1° to account for the low-layer thickness. The pattern of the as deposited film shows a broad bump centered at 30° typical of the amorphous phase. The partially crystallized samples are instead identified by the (200) and (220) diffracted peaks of the metastable rock-salt (face-centered cubic, FCC) phase. Their intensity increases with the crystalline fraction. The full width at half maximum (FWHM) of the peaks is taken as a parameter to calculate the average grain diameter through the relation $d = \lambda/\text{FWHM}\bullet\cos(\theta)$, where λ is the X-ray wavelength and θ the incidence angle. In this case, the average final grain size amounts to 40 nm. Besides the metastable rock-salt phase that is observed at low annealing temperatures, a stable trigonal phase is formed after high annealing, as shown in Fig. 4.17b. The patterns relate to GST thin films after annealing at 150 °C and 400 °C with the corresponding phases labeled with different symbols.

Silicides

Silicides are widely used as conductive compounds in the semiconductor industry to mitigate contact and sheet resistance in devices. Although the long-lasting experience of the reaction and properties gained on silicon has been technologically transferred to SiC, specific critical issues have been raised and nowadays deserve a focused effort.

In the story of silicides, nickel-silicon compounds represent the latest choice that was basically motivated by their low

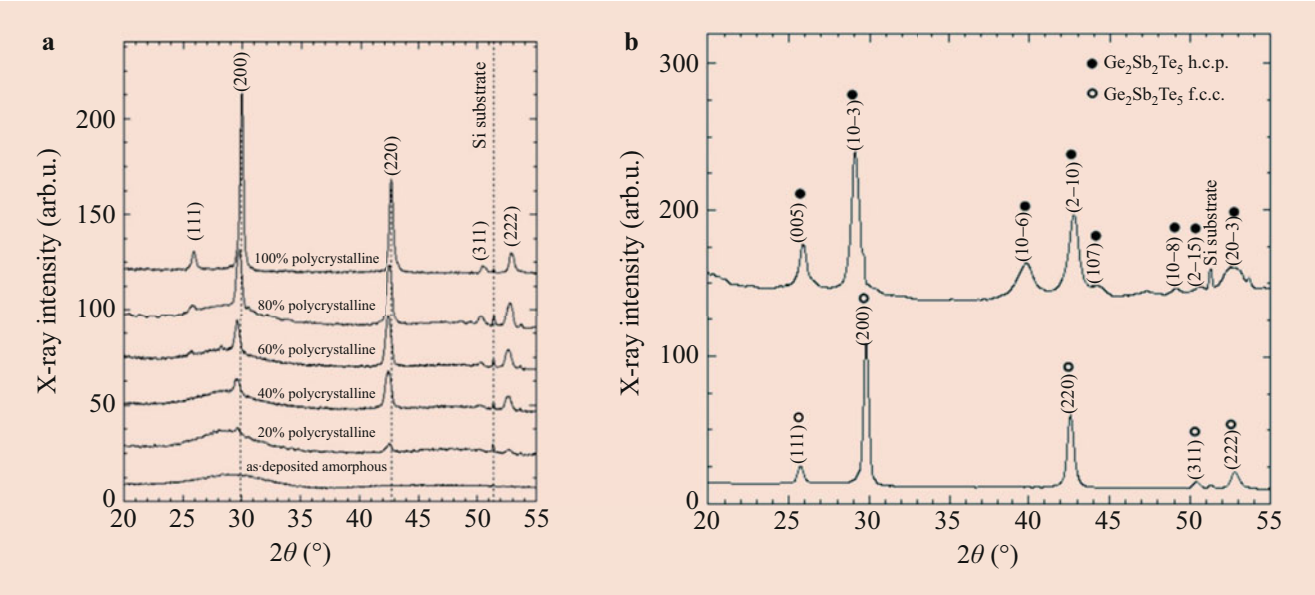


Fig. 4.17 (**a**) X-ray diffraction (XRD) of as-deposited amorphous $Ge_2Sb_2Te_5$ films at different crystalline fractions. The peak positions related to the diffraction of (200) and (220) planes are marked with dashed vertical lines along with the contribution of the Si substrate. (Reprinted from Rimini et al. [27], with the permission of AIP Publishing). (**b**) XRD pattern of $Ge_2Sb_2Te_5$ films on SiO_2/Si substrate after annealing at 150 or 400 °C for 10 min; the diffraction peaks indicate the presence of the rock-salt (open circles) and trigonal (full circles) phase. (Reprinted from De Bastiani et al. [28], with the permission of AIP Publishing)

formation temperature and excellent scalability. In addition, it has been demonstrated that a heteroepitaxial coupling of orthorhombic nickel silicides with cubic silicon is feasible by promoting the growth of transrotational structures [29]. Despite their formation demanding special care in the interfacial cleanness and deposition conditions (low deposition rate and deposition temperature ~70 °C), the advantages of exploiting the structural interfacial coupling with silicon are numerous, such as the down-scalability of the thickness that preserves flatness and thermal stability (~10 nm), the low formation temperature (≥220 °C), and the low contact resistance [30].

Figure 4.18a, b disclose the structural difference between a standard NiSi layer and a transrotational silicide of the same stoichiometry and thickness grown on [001] bulk silicon. Noticeable differences reside in the lack of grain boundaries and in the ordered electron diffraction pattern of the trans-NiSi layer [31]. In addition, trans-domains are easily traceable by the peculiar branched shape of the diffraction contours, which are called bending contours. Figure 4.18c shows the cross-section of the core of a trans-domain in which an atomic coupling is established between the metallic layer and the Si substrate. This coupling extends through the rest of the interface, moving from the core region, and involves the entire domain volume with progressive bending of the silicide lattice. This overall bending is a way for the thin metallic layer to account for the strain due to the mismatch and different lattice structure with silicon, thus representing the mainstay of a transrotational silicide architecture [29]. The kind of peculiar atomic matching established at the shared interface guarantees low barrier height for high-performance ohmic contacts, as shown in Alberti and Giannazzo [30]. The lattice configuration of thin trans-silicides can be unveiled by X-ray polar figure analysis, as shown in Fig. 4.18d. It produces specific features that account for the continuous bending of the crystallographic planes along the layer, in full agreement with the structural simulations represented by colored dots in Fig. 4.18d. Their relationship with the underlying silicon, whose contributions are marked by black squares in the same figure, is also specifically diagnostic of this kind of growth. In a complementary way, in-plane diffraction applies to further explore the trans-rotational coupling, as can be found in Alberti and La Magna [29], and likewise any kind of thin-film epitaxy.

The formation of trans-silicides on SiCs for backside metallization in currently produced power devices for microelectronics is a challenge. On the other hand, a standard silicide reaction on SiC has a bottleneck in the thermal budget to be applied for silicidation. It represents one of the last processing steps, which is further complicated by the extremely scaled wafer thickness. To overcome all those issues, laser annealing represents a reliable. Silicide reaction by laser annealing is currently in the spotlight owing to some challenges, mainly related to the carbon clustering after silicon release for silicidation and to the control of the overall composition and uniformity of the metallic contact [32].

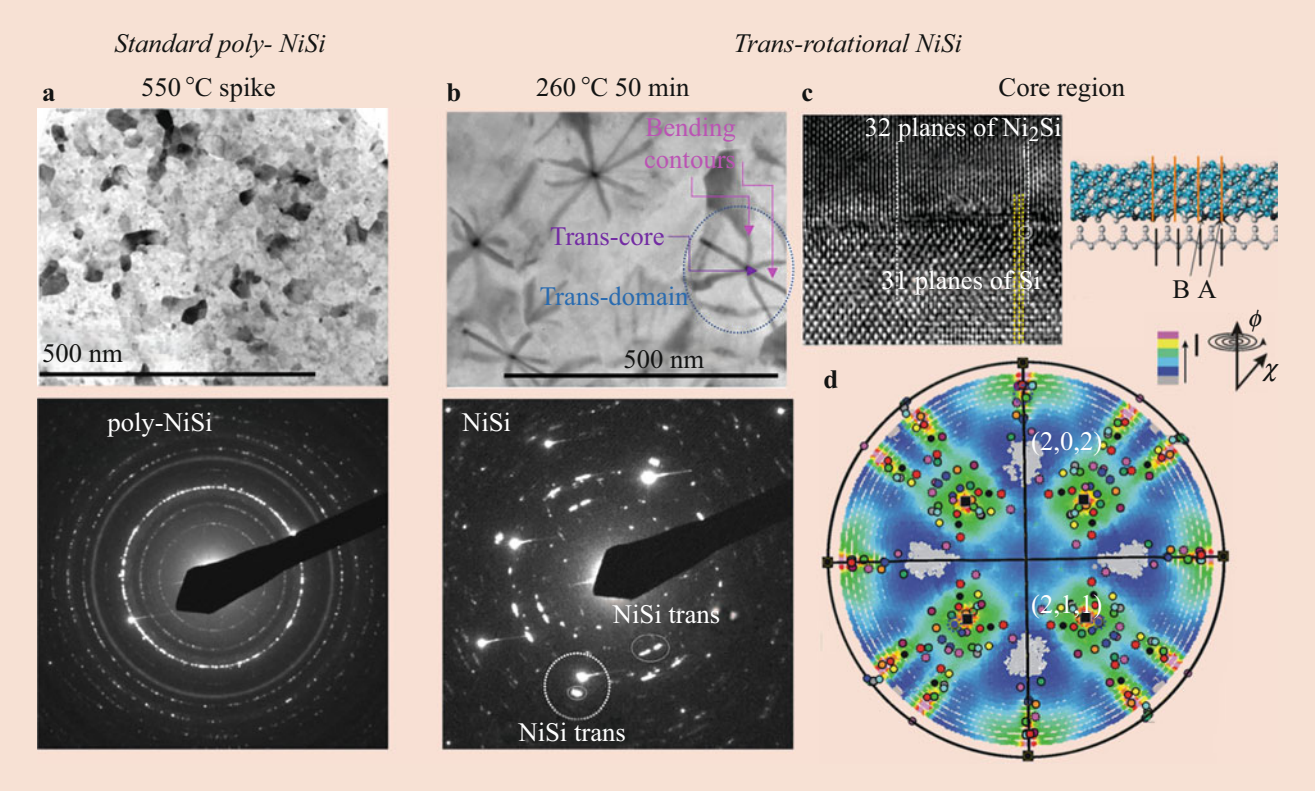


Fig. 4.18 (**a**) Polycrystalline NiSi layer. (**b**) Transrotational NiSi layer featured by crossing bending contours. (**c**) Lattice match at the core region through the silicide/silicon interface as viewed by high-resolution transmission electron microscopy imaging and atomic simulation. (**d**) (202)/(211) polar figure analysis by X-ray synchrotron radiation (European Synchrotron Radiation Facilities Grenoble) on a trans-NiSi layer with the dots representing the simulated silicide lattice. Silicon contributions are labeled by black squares. (Adapted with permission from Alberti and La Magna [29], Copyright American Institute of Physics 2012)

4.2.3 Case Studies

Shape-Related Structure of Silicon Nanoparticles

Silicon nanoparticles can be applied in light emitting diodes, flash memories, and flat screen, with their synthesis usually carried out using chemical methods. Size control and shape analyses are often performed using X-ray diffraction [33]. In this specific case, nanoparticles are isolated octahedrons with a narrow distribution in size that allow very efficient scattering and trapping of incoming radiation. They are generated into an inductively coupled plasma-chemical vapor deposition (ICP-CVD) chamber and, immediately after, land on a flat substrate under high vacuum conditions.

The octahedron facets are framed by (111), (220), (311), and (100) silicon planes as expected for the minimization of the surface energy. Figure 4.19a shows a polar figure collected using a Cu-$K\alpha$ beam to probe the spatial configuration of the (111)-Si planes over half of the solid angle on a set of as-deposited octahedrons. In the figure, the distribution of the q-vector associated with (111)-Si planes is stereographically projected onto a two-dimensional image. The resulting figure shows an intense signal at $\chi = 0$ and a ring at $\chi = 70.5°$. Their combination and the related parameters are symptomatic of the shape and geometrical configuration (landing condition) of the nanoparticles, whereas the occurrence of a ring at $\chi = 70.5°$ flows from the rotational degree of freedom around the [111] landing axis (see Fig. 4.19c). A frame of the tomographic view of an isolated octahedron, taken by TEM, and its configurational schematic are shown in Fig. 4.19b, c respectively. This information is complemented by position and shape analyses of the X-ray diffraction peaks that disclose the octahedrons being defect-free, unstrained single crystals even at a low substrate temperature (50 °C). A feasible integration of the deposition process at any production step and the use of low-cost substrates are indeed guaranteed.

The assembly of silicon nanoparticles (NPs) allows growing layers with controllable porosity and surface-to-volume ratio. Those strategic properties are suitably explored by 3D-coherent X-ray diffraction imaging (3D-CXDI), a recently developed methodology that exploits synchrotron radiation beam lines. The method allows tomographic reconstruction and quantitative analyses through mapping of the electronic density into the probed volume as well as discriminating functional materials eventually hosted inside the porous scaffold. An example of two different assemblies of silicon nanoparticles is shown in Fig. 4.19d–g [34]. Lateral pore size

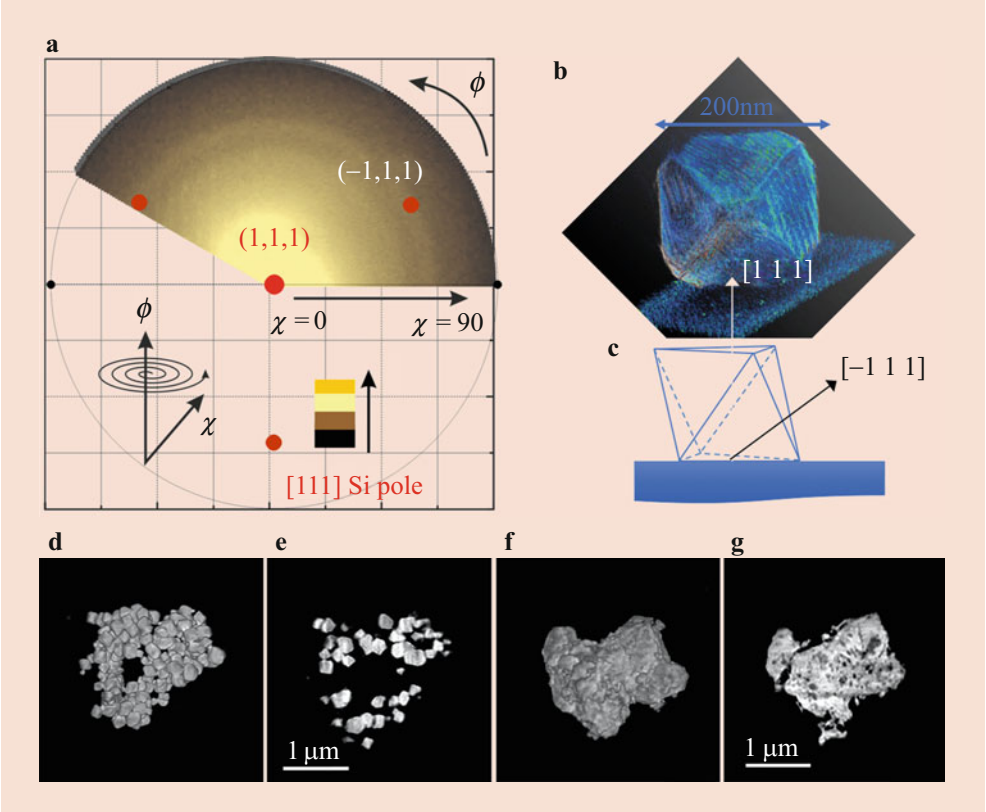


Fig. 4.19 (**a**) Stereographic projection of a polar figure mapping the (111) silicon planes over a system of octahedrons landed on a substrate after their generation into an inductively coupled plasma-chemical vapor deposition chamber. (**b**) Transmission electron microscopy tomographic view of a single silicon octahedron. (**c**) Schematic of an octahedron deposited on a flat substrate. (**d**, **f**) 3D-coherent X-ray diffraction imaging of differently assembled regular and irregular Si-NPs (respectively), performed at the beamline ID10 of the European Synchrotron Radiation Facilities [36, 37]. (**e**, **g**) Central slices (sections) of the tomographic images in (**d**) and (**f**) respectively. (Adapted from Mannino et al. and de Jong et al. [33, 34], under the terms of the Creative Commons CC BY license, Springer Nature 2015 and 2016)

and correlation distance in a porous matrix are additional parameters accessible by using synchrotron lights and applying grazing incidence small-angle X-ray scattering [35].

Residual Defects in Ion-Implanted Ge

A second example of X-ray analysis applied to single-crystal semiconductors refers to germanium. As occurs in silicon-based technologies, dopant implantation and subsequent thermal treatments, used to form ultra-shallow junctions, leave interstitial-type end-of-range (EOR) defects that are difficult to investigate and detrimental to the carrier transport in devices. X-ray analysis can be applied in this field [38].

With respect to the local analyses that can be done by TEM, XRD provides complementary average information over square-millimeter areas. The analysis consists of collecting $\omega - 2\theta$ patterns under HR-XRD conditions around the (004) planes of the germanium lattice in the reciprocal space along the direction of the q_z vector and around the $|q_{z004}|$ value. Figure 4.20 reports the data item in a sample implanted with fluence 2×10^{14} Ge/cm^2 at 100 keV after annealing at 340 °C, compared with a reference diffraction pattern. The analysis highlights that, after annealing, the disorder of the lattice due to the ionic implantation is almost completely recovered, except for a shoulder at positive q_z. It is a marker of a displacement field around the defects that is due to interstitial atoms [39]. This extra-contribution to the diffuse scattering with respect to the reference signal, called I_{excess}, is shown in a double logarithmic plot as a function of $|\Delta q_z|$ in Fig. 4.20b. It is produced by the presence of interstitial clusters into the recovered Ge matrix as disclosed by its peculiar decay vs $|\Delta q_z|$. In particular, the log-log plot in Fig. 4.20b has a double slope with exponent $-2(\Delta q^{-2})$ owing to the Huang scattering from the lattice atoms near the defects and with exponent $-4(\Delta q^{-4})$ at high values owing to the Stokes–Wilson scattering.

End-of-range defects and strain induced by ion implantation, which represent critical issues for any semiconductor technology, are investigated in detail in Capello et al. [40] on implanted bulk silicon and studied using coupling synchrotron radiation X-ray scattering to XRD.

Extended Defects in SiC and GaN Epilayers

Epitaxial layers and bulk SiCs are in the spotlight for the new frontiers of microelectronics, especially for power devices.

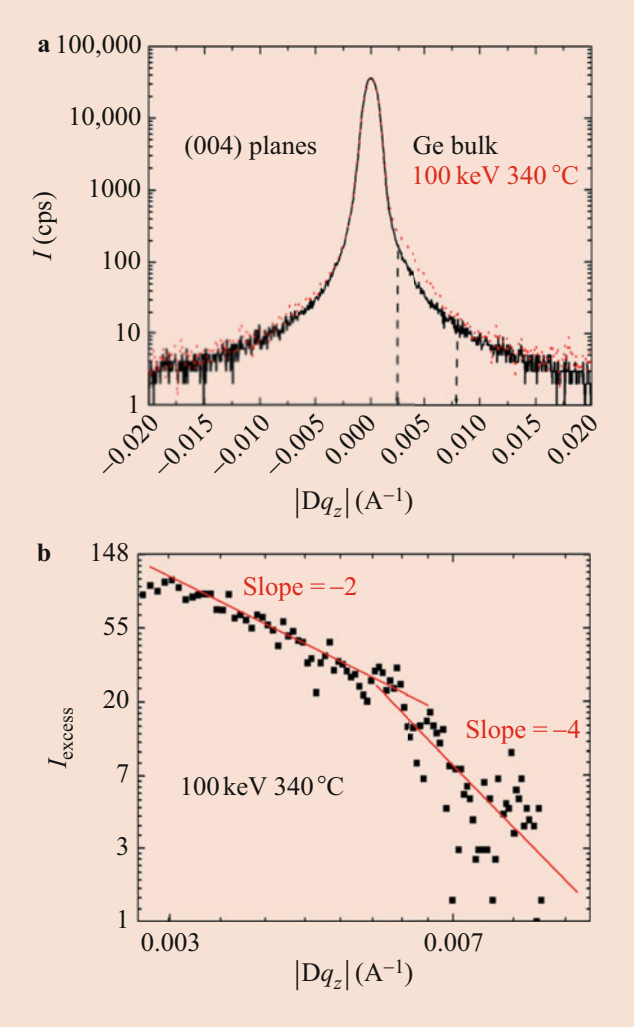


Fig. 4.20 (**a**) High-resolution X-ray diffraction pattern of a Ge sample implanted with a fluence of 2×10^{14} Ge/cm^2 at 100 keV after annealing at 340 °C, compared with the reference case. It has a shoulder at an angle above the Bragg angle owing to diffuse scattering from interstitial-type defects. (**b**) Log-log plot of the excessive intensity, in the region among dashed lines in (**a**), as a function of $|\Delta q_z|$. (Adapted with permission from Boninelli et al. [38], Copyright American Institute of Physics 2012)

Their structure, strain, defects, and coupling with other materials in the device architecture raise concerns to be addressed by newly conceived growth and deposition methodologies. Nonetheless, they remain critical owing to the high temperature of the processing steps, to the different stability window of the available polymorphisms (e.g., 3C, 4H) and to the difficulties of doping. In all those respects, XRD provides crucial insight to afford incremental improvement of the processes involved in device manufacturing.

Extended defect (e.g., SFs and dislocations) formation is especially crucial while growing 3C-SiC layers. Their qualitative evaluation is commonly addressed by measuring the FWHM of the rocking curves (Rc_s) collected at strategic peaks. As a major feature, the decrease in the FWHM of the Rc collected at the (002) 3C-SiC planes [41] is symptomatic of an overall improvement of the quality of the material. The FWHM is primarily linked by the layer mosaicity and to the presence of extended defects into the layer. Indeed, this parameter provides feedback for tuning the growth conditions. High defect density is not only detrimental to carrier mobility but even induces an internal stress field that bends the wafer, with a consequent increase in its brittleness [42]. Defect mitigation action starts from controlling the early stage of growth of epitaxial layers. The electronic density of the growing front is often measured by XRR and used as a diagnostic parameter for the compositional changes occurring during the process [42]. XRR is easily implementable in a laboratory diffraction setup.

A powerful tool for evaluating the quality of the as-grown layer is through a mapping of the q-vector associated with specific planes in the reciprocal space. An example of reciprocal space mapping (RSM) is shown in Fig. 4.21. As reported in Boulle et al. [43], the (002) 3C-SiC Bragg peak is sensitive to the density of SFs in the probed layer. They, in fact, produce streaks along the [111] directions that cross the main diffracted feature. The analysis procedure consists of extracting and simulating [43, 44] the intensity line profile along this streak as represented in Fig. 4.21. A density of defects (D) within the range of 400–450 SFs/cm, close to the value measured by potassium hydroxide etching and imaging is measured.

Gallium nitride is used for high-power and high-frequency devices with high-energy efficiency, having a large band gap (3.4 eV), a high critical field (>3 MV/cm), and high electron mobility in heterostructures (>1000 cm^2 V^{-1} s^{-1}). GaN technology, competing with its Si and SiC counterparts, has current open issues in epitaxial layer growth and device optimization that can indeed benefit from the use of X-ray diagnostics.

The nature and density of the defects in GaN epilayers can be faced by HR-XRD focusing on the growing planes. A case study is shown in Fig. 4.22: the sample is a 3-μm-thick n-type GaN epitaxial layer, with a nominal donor concentration $N_D \sim 1 \times 10^{16}$ cm^{-3}, grown onto a heavily doped (~1–5 $\times 10^{18}$ cm^{-3}) freestanding GaN substrate [45]. A family of (000 l) growing planes is investigated on purpose through $\omega - 2\theta$ scans and Rc_s by spanning over l = 2,4,6. In a non-ideal lattice with periodicity perturbed by defects, the FWHM of the Rc_s is related to the tilt angle and to the correlation length between domains [46]. The applied fitting procedure provides an average value for the screw dislocation density, 4.7×10^7 cm^{-2}. A corresponding density of edge dislocations can be inferred by exploiting the semi-empirical curve reported by Heinke et al. [47].

X-ray analytical facilities and methods have indeed been making huge progress since Max von Laue posed

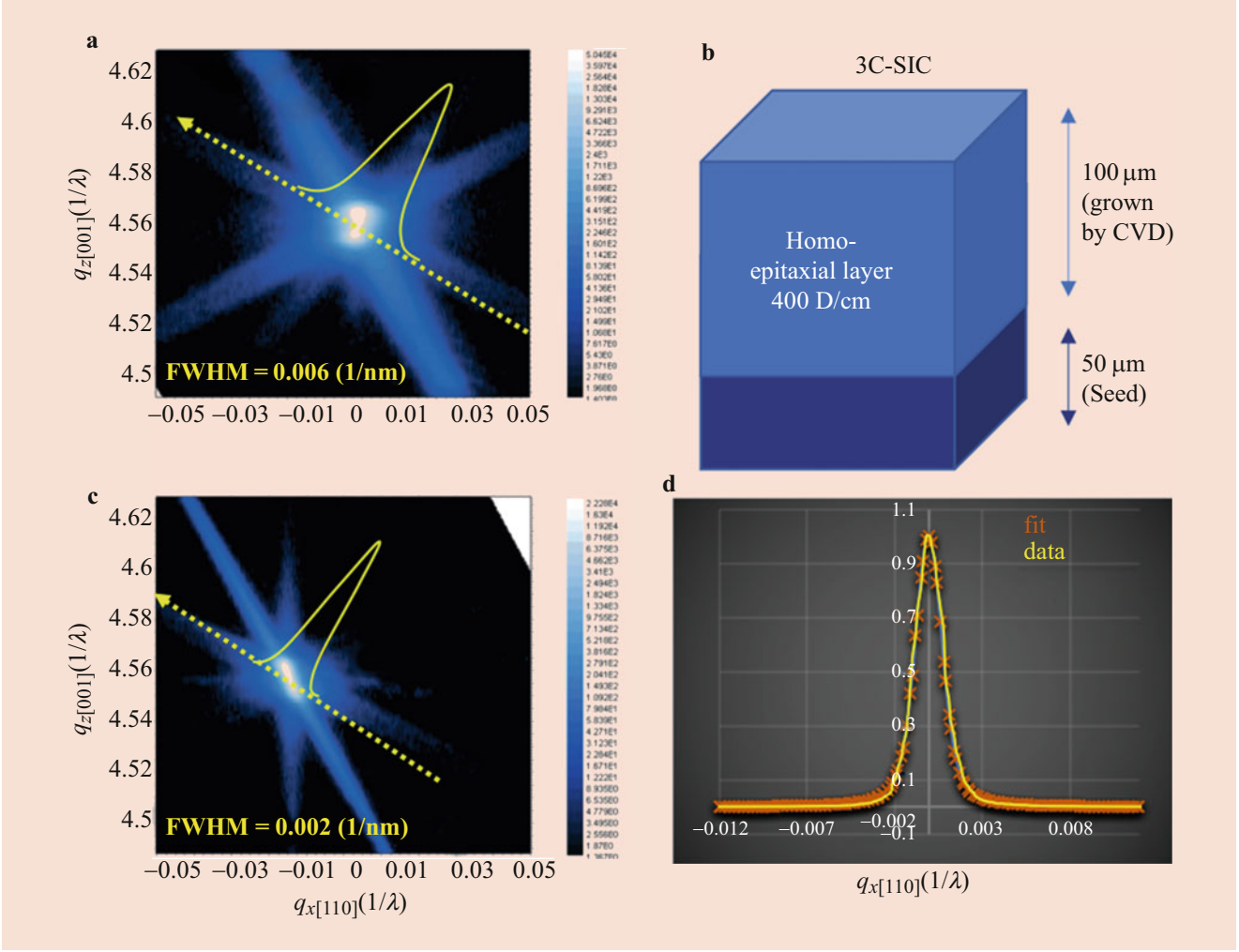


Fig. 4.21 One hundred-micrometer 3C-SiC layer grown on a 50-µm homo-seed layer. (**a**) Reciprocal space mapping (RSM) of the seed (3C-SiC). (**b**) Schematic of the sample after homoepitaxy. (**c**) RSM of the final sample. (**d**) Simulation and data of the line profile along the streak (along the yellow arrow)

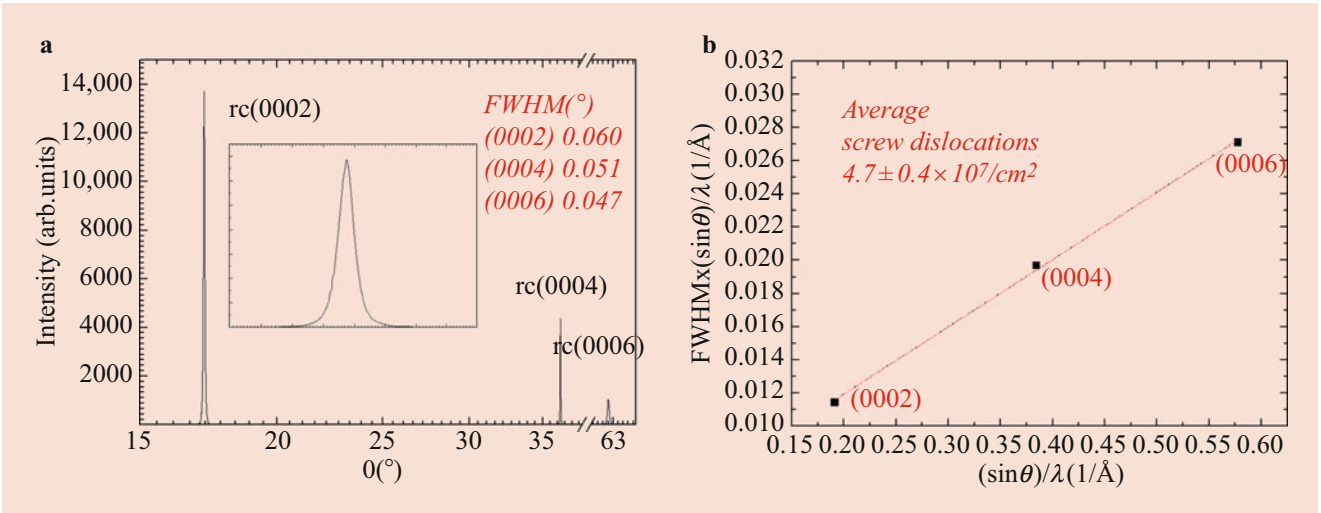


Fig. 4.22 (**a**) Rocking curves along (000l) planes and (**b**) data fitting (investigated area 2 mm in diameter) to extract the screw dislocation density in the GaN epitaxial layer. (Adapted with permission from Roccaforte et al. [45], Copyright Elsevier 2019)

the question: "What would happen if you assumed very much shorter waves to travel in the crystal?" We can partially answer that material science with its new frontiers is undoubtedly benefitting from the power of X-ray to interact deeply with matter.

4.3 Raman Spectroscopy

This section describes the working principle of Raman spectrometry, the experimental apparatus commonly adopted, and some applications. Identification of structure, either amorphous or crystalline phase and of disorder are the main characteristics of this technique. As an example, the structure of amorphous and crystalline Si and of chalcogenide alloys as analyzed by Raman spectroscopy are presented and discussed. Raman spectrometry is also a powerful contactless technique for studying the local transport properties in polar semiconductors. The method is based on the measurement of the frequency shift caused by the coupling of longitudinal optical (LO) phonon with plasmons (LOPC). The shift depends on the free carrier concentration and on the carrier mobility; these parameters can then be measured. The method is illustrated by measurements performed on SiC and GaAs heteroepitaxial layers.

4.3.1 General Aspects

Raman spectroscopy [48] is a technique adopted to determine the phases of several semiconductors and metals used in microelectronics. It is based on the interaction of light with molecules in some medium or atoms in a crystal. The Raman scattering is an inelastic process, i.e., a scattering process in which energy is transferred between an incident photon with energy $h\nu_I$ and the sample, resulting in a scattered photon with a different energy $h\nu_s$. The amount of transferred energy corresponds to the energy $h\nu_k$ of an elementary excitation in the sample, e.g., a phonon, a polariton, or a plasmon. The energy conservation law gives the correlation between incident and scattered frequencies of radiation:

$$h\nu_s = h\nu_i \pm h\nu_k. \tag{4.1}$$

The processes in which an elementary excitation is generated ($\nu_s < \nu_i$) are called Stokes processes, whereas those that imply the annihilation of an elementary excitation ($\nu_s > \nu_i$) are referred to as anti-Stokes processes. As the density of phonons for a mode κ is given by the Bose–Einstein distribution, anti-Stokes Raman scattering is a factor of $\exp(-h\nu_k/kT)$ less than Stokes Raman scattering [49].

Figure 4.23 shows the Raman spectrum of silicon, with Stokes and anti-Stokes bands.

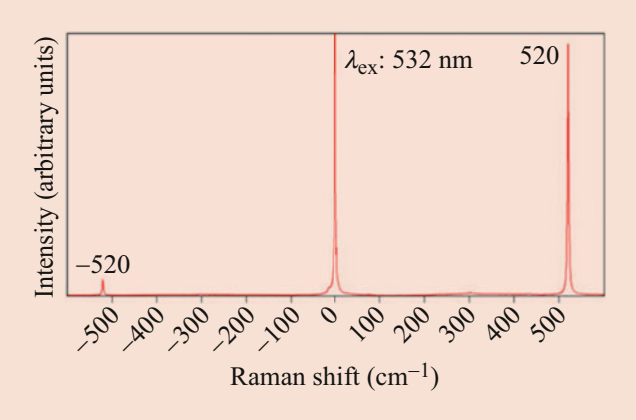


Fig. 4.23 Raman spectrum of silicon

In analogy to energy conservation, the quasi-momentum conservation law yields the correlation between the wave vector k_i of the incident light, k_s of the scattered light, and the excitation wave vector q_j:

$$k_s = k_i \pm q_j. \tag{4.2}$$

Raman spectroscopy employs a laser in the visible region with a wavelength that exceeds the lattice constant by a factor of more than 100. Therefore, the involved excitation wave vectors are within a few percent of the center of the Brillouin zone. In this region, the dispersion of optical phonons is negligible, and therefore the energy transfer $h\nu_\kappa$ is independent of the incident frequency. Actually, the conservation of momentum represents an idealized picture, which may be limited in real experiments because of the light absorption in the sample. Indeed, the attenuation of penetrating light is equivalent to a spectrum of different momentum values, thus leading to a spectral band of solid-state excitations fulfilling the momentum conservation rule. Moreover, in real crystals impurities and dislocations are responsible for momentum nonconservation, which causes a corresponding broadening of the spectral lines observed. Therefore, the line shape of phonon peaks observed in Raman spectra characterizes the degree of disorder into a solid.

As the vibrational modes of the material determines the energy shift, Raman spectroscopy distinguishes between phases with the same composition, because they are characterized by phonons with different energies.

4.3.2 Experimental Setup

In Raman experiments the energy spectrum of scattered light is very close to the energy of the incident light but usually many orders of magnitude smaller in intensity. Therefore, very good suppression of the elastically or quasi-elastically

scattered light is required. The essential parts of a Raman setup are thus a laser, which is a stable monochromatic source with considerably high intensity, a double or triple monochromator, a spectrometer, and a very sensitive photon detector. In spite of the monochromatic character of the laser light, a spectral filter into the laser beam path eliminates nonlasing emission lines. The scattered light is collected through a lens system and focused onto the entrance slit of a spectrometer.

As the intensity of the Rayleigh scattering is high enough to completely hide the Raman signal, the scattered radiation must be filtered before reaching the spectrometer. This, traditionally done by means of a double or triple monochromator, can also be obtained by a holographic notch filter. This works as a beam splitter, reflecting almost 100% at the wavelength of the laser beam and transmitting up to 80% at the other wavelengths.

The wavenumber of transmitted Raman light is tuned by tilting an interference filter. The Raman scattered light is then dispersed using a diffraction grating, which reflects a particular wavelength range to the detector. The detector is a photomultiplier, or a multichannel detector system with a very high efficiency.

A computer, usually outputting a graph of intensity versus wavelength, then processes the information. The wavelength is commonly given in relative wavenumbers (cm^{-1}) to the laser wavelength. The value is calculated by taking the inverse of the laser wavelength (in centimeters) minus the inverse of the Stokes Raman shifted wavelength (in centimeters). The relative wavenumber shift for a particular molecule or crystal is a constant no matter what laser wavelength is used as source. Raman spectroscopy thus takes advantage of this wavelength shift and allows for identification of different molecules or crystalline structures, which all have different shifts and intensities relating to the particular bond.

A large improvement in spatial resolution can be achieved using a light microscope as optics for both focusing the incident beam onto the sample and collecting the scattered light (micro Raman). For this purpose, the microscope contains a beam splitter, inserted between the objective and the ocular lens system. With this setup, the lateral resolution is limited by the light diffraction. The lateral resolution is of great importance to distinguish two different crystalline structures, both present in the sample, or for characterizing patterned samples. In comparison with standard optics with lenses of long focal lengths in the centimeter regime, the microscope setup collects a much larger solid angle of scattered light. This results in much greater collection efficiency, thus enhancing the sensitivity, though decreasing the definition of the propagation direction of the scattered wave.

The spatial resolution is improved by using confocal optics, which measure at one time the intensity of the light reflected or transmitted by a very small area of the sample. A pinhole aperture, placed in the microscope objective image-plane, selects only the scattered light coming from the area of the sample illuminated by the laser spot, whereas the out-of-focus contributions do not propagate through the confocal hole. The vertical spatial resolution depends on the optical properties of the sample. For transmitting materials, it is better than 2 μm; in absorbing samples, it is determined by the light penetration depth.

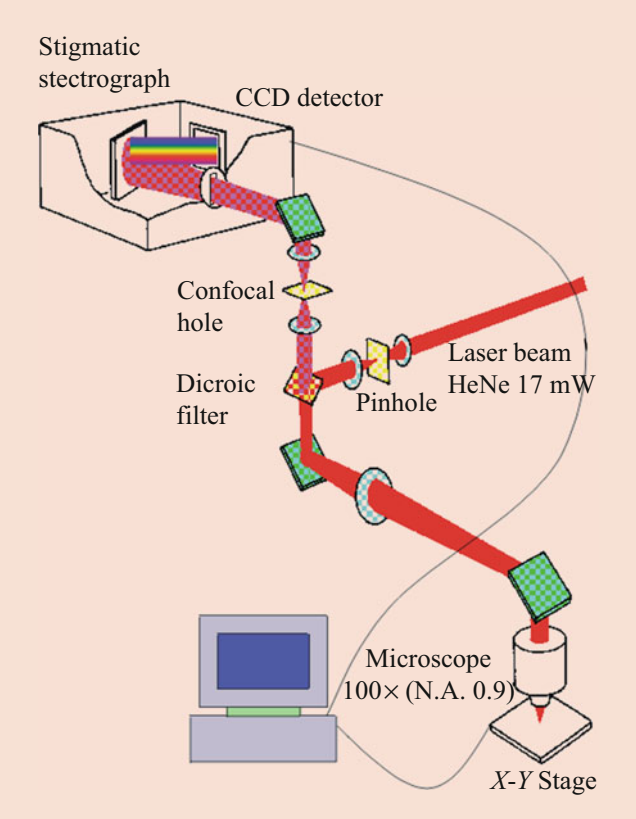


Fig. 4.24 Schematic of an experimental apparatus for micro-Raman spectroscopy and mapping

To perform spatial images of the distribution of different phases, samples are mounted on a computer controlled xy stage, which enables the sample position in steps typically less than 1 μm to be automatically changed.

Complete commercial Raman setups are available. Figure 4.24 shows a schematic of a typical setup.

4.3.3 Structure Analysis

Structurally, crystals differ from amorphous solids and glasses in that the former possess long-range translational symmetry whereas the latter lack any spatial order. Therefore, the Raman spectra of the materials in the crystalline or amorphous phase are usually different. Figure 4.25 shows Raman spectra of single-crystal and ion-implanted Si. Ion

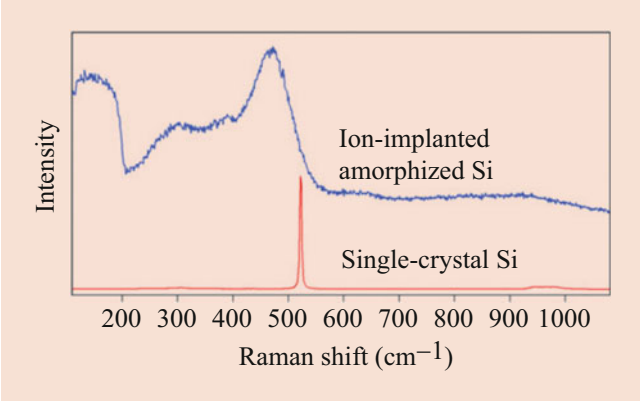


Fig. 4.25 Raman spectrum of ion-implanted amorphized silicon, and of single-crystal silicon

implantation is a commonly adopted technique for silicon doping. Implantation at a high dose of heavier elements than silicon, such as As, produces severe damage and amorphization. The Raman spectrum of single-crystal Si consists of one triply degenerate optical phonon at 520 cm^{-1} along with much weaker second-order transverse acoustic and optical modes that appear at approximately 305 cm^{-1} and 975 cm^{-1} respectively. The selection rules for first-order Raman scattering from crystalline solids dictate that only those optical phonons at the Brillouin zone center are Raman active. Consequently, the first-order Raman band at 520 cm^{-1} is very narrow, with a full width at a half maximum of only 4 cm^{-1}. The Raman spectrum of the As-implanted Si consists of very broad bands below 550 cm^{-1}. The reason for the detection of Raman scattering over this broad region is that the Raman selection rule for crystals restricting Raman scattering to phonons at the Brillouin zone center no longer holds in amorphous Si and all of the phonons from the Brillouin zone center to the edge are now sampled. The Raman spectrum of amorphous Si looks very much like the calculated populations of phonon energy states within the first Brillouin zone of crystalline Si [50].

A peculiar case is represented by phase change materials, such as GeSbTe alloys, recently employed for the manufacturing of phase change memories. As shown in Fig. 4.26 [51], the crystalline phase with rock-salt (FCC) structure, formed upon annealing within the range 125–175 °C, exhibits Raman peaks wider than in the amorphous phase, in contrast to what is usually observed in other materials (see Fig. 4.23 for Si). This is due to the high degree of disorder that characterizes the crystalline structure, in which a Ge, Sb, or a vacancy, randomly occupies the cationic lattice.

Raman with a focused micrometer beam spot can be employed to obtain a spatial image of the distribution of different phases. Figure 4.27a shows an optical image of a resistor of $Ge_2Sb_2Te_5$ with different phases. The Raman spectra taken in

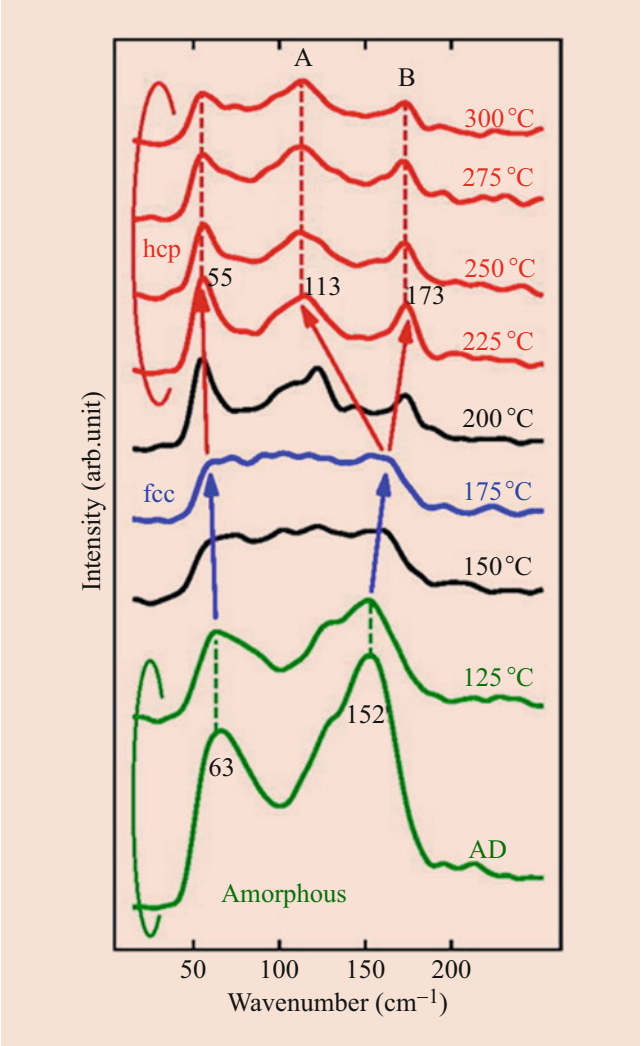


Fig. 4.26 Raman spectra of $Ge_2Sb_2Te_5$ as a function of the annealing temperature, from the amorphous phase to the crystalline structures (face-centered cubic at 175 °C and hexagonal close packing at 250 °C). (Reprinted Guo et al. [51], with the permission of AIP Publishing)

different regions, shown in Fig. 4.27b, indicate the presence of the trigonal stable phase and the amorphous phase. Figure 4.27c, d show the intensity of the integrated Raman shift in the region 100–120 cm^{-1}, corresponding to the trigonal phase, and in the region 140–160 cm^{-1}, characteristic of the amorphous phase respectively. The 2D Raman imaging clear indicates that the amorphous phase is located at the center of the resistor.

4.3.4 Carrier Concentration and Mobility Measurements

Usually, electrical characterization is performed by the Hall effect and resistivity measurements. These procedures need

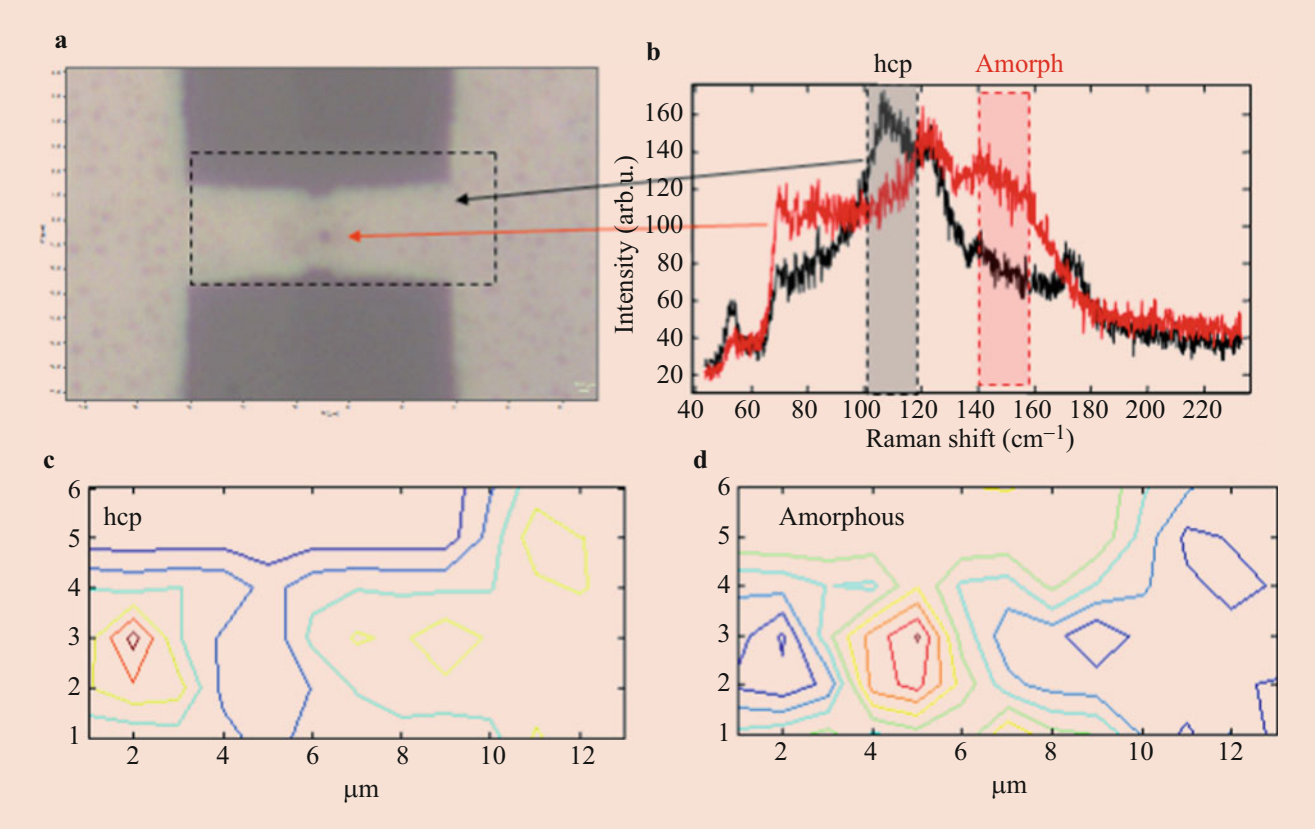


Fig. 4.27 (**a**) Optical image of a resistor with the composition $Ge_2Sb_2Te_5$. (**b**) Raman spectra taken in different regions of the resistor in (**a**), as indicated by the arrows. (**c**) and (**d**) Integral of the Raman signal corresponding to the trigonal phase or to the amorphous phase respectively. (© 2014 IEEE. Reprinted, with permission, from Privitera et al. [52])

electrical contacts and give information on the transport properties averaged over relatively large sample volumes. Local non-invasive probes are of high interest, particularly those that do not need destructive sample preparation, substantially reduce the measurement time, and provide information on very small volumes. Raman spectroscopy is a powerful technique for studying the local transport properties in polar semiconductors such as SiC and GaN [53–55].

A great deal of attention has been devoted to the analysis of LOPC modes in SiC. The Raman frequency of the LOPC mode was used to determine the free electron concentration and its measurement was used as a fast method to study the distribution of the net donor concentration ($N_D - N_A$) over the surface of a wafer [56].

More recent Raman studies, on graded doping 4H-SiC crystals, have shown a linear relationship between the peak frequency of the LOPC mode, ω_{LOPC}, and the free carrier concentration n in the range between 2×10^{17} and 3×10^{18} cm^{-3} [54, 57]. As for 4H-SiC the LOPC band shifts only by 0.8 cm^{-1} for a carrier concentration change of 1×10^{17} cm^{-3} [57] a more careful Raman measurement is needed to precisely determine the carrier density in the range below 10^{17} cm^{-3}.

The relationship between $\Delta\omega$ and n is given by a simple equation in the case of 4H-SiC [57]:

$$N = 1.25 \times 10^{17} \times \Delta\omega. \tag{4.3}$$

The plasmon-damping constant, γ_p, is expressed as a function of the carrier mobility, μ, by the following equation:

$$\gamma_p = e/m^*\mu, \tag{4.4}$$

where m^* is the electron effective mass. Equations (4.3) and (4.4) show that both free carrier concentration, N, and mobility, μ, can be calculated from the ω_p and γ_p data obtained from the fit of the LO peak [58] by taking ω_p and γ_p as the adjustable parameters.

The local information of doping and mobility is extremely interesting in several cases. For example, by analyzing the LOPC modes the electron bulk mobility (μ) of 3C–SiC layers grown on (111) and (100) Si substrates ranges between 10 and 510 cm^2 V^{-1} s^{-1}, whereas the electron carrier concentration (n) varies from 1.6×10^{16} to 5.4×10^{18} cm^{-3} [59]. These measurements indicate that the samples grown on Si (111) have a lower average mobility on a large area with respect to

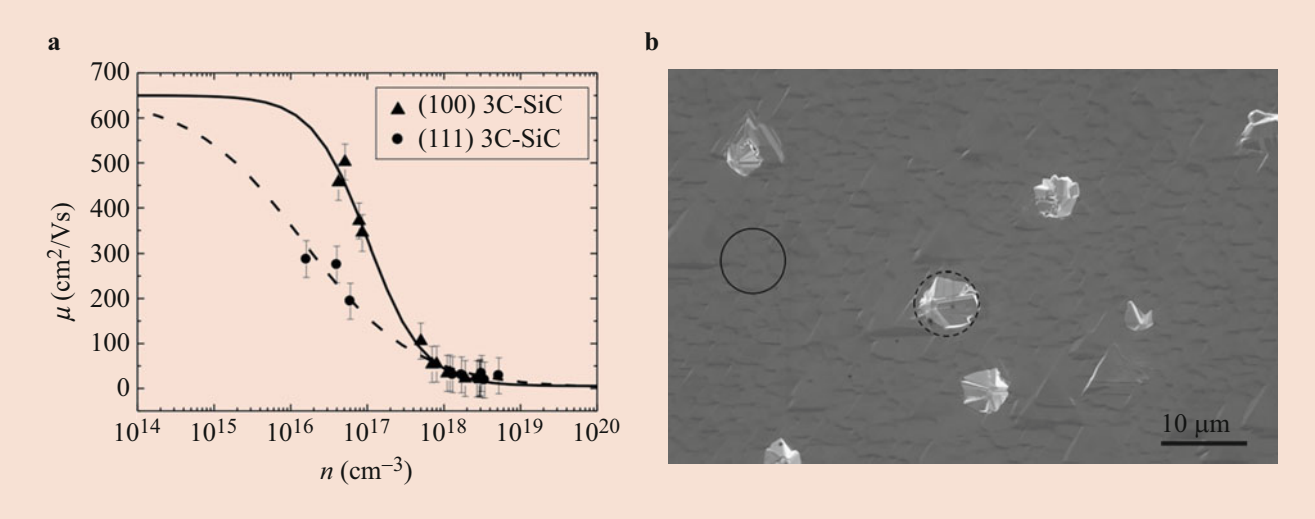


Fig. 4.28 (**a**) Electron mobility as a function of doping concentration in 3C–SiC. Solid triangles and circles represent the mobility values of samples grown on (100) and (111) Si respectively. A dashed line for (111) and a solid line for (100) are curves obtained by fitting the data. (**b**) Scanning electron microscopy image of 3C–SiC film grown on off-axis (111) Si substrate; the hexagonal defects lower the average mobility. (Reproduced from Piluso et al. [59], with the permission of AIP Publishing)

those grown on Si (100), as reported in Fig. 4.28a. The local measurements show clearly that the lower mobility of the (111) 3C-SiC layers is due to the presence of the hexagonal defects (see Fig. 4.28b). Instead, the mobility measured in free defects regions of 3C-SiC (111) is equal to that of the 3C-SiC (100) layers.

As reported in the literature [60], at high optical excitation dense electron-hole plasma forms in many semiconductors (e.g., GaAs and GaP). Under these conditions, the LOPC mode has been detected and measured in undoped GaP crystal [61]. In this context, the excess carriers, induced by laser pumping, are characterized by a carrier lifetime and electrical mobility, which can easily be measured by Raman tools. Crystallographic defects alter these properties so that a systematic study of the local (induced) carrier density variation can be used to detect crystallographic defects [62].

Based on these considerations, a new Raman methodology analysis, called induced-LOPC (i-LOPC), was designed [63]. A laser with a wavelength lower than the material band edge, at different power densities, was used to study the effect of a crystallographic defect, such as SF or point defects, on the carrier density. In the case of SFs in 4H-SiC (laser HeCd at 325 nm, 4H-SiC band-gap at 388 nm), LO Raman mode did not change on or out of the SF when the laser power was 1 mW, a value that is too low to increase the carrier density. Conversely, when the laser power increased to 10 mW, the spectrum on the SF showed a consistent reduction of the Raman shift, suggesting the trapping of free carriers. Such an effect detects the presence of defects through Raman inspection.

Figure 4.29 shows the detection of an SF in a 4H-SiC by using photoluminescence (PL) and i-LOPC techniques. The spatial morphology and the PL spectrum determine the crystal structure of the defect. In particular, the triangular shape together with a PL signal centered at 2.7 eV are related to 4SSF, which is associated with a (4,4) stacking sequence in Zhdanov's notation [64, 65]. The width of the defect along the 11–20 direction indicates that it was formed close to the epilayer–substrate interface (see Fig. 4.29a). The map in Fig. 4.29b was obtained from analysis of the LO Raman mode shift performed across the same region analyzed using the PL method. An evident modulation of the LO Raman shift is observed with the expected triangular shape. An additional LO Raman shift was observed around 4SSF. Such a variation was related to another SF with different energy characteristics (PL peak) and thus not clearly seen using the PL technique (they are seen in Fig. 4.29a merely as darker areas).

Point defects such as interstitial and vacancies act as scattering or recombination centers, reducing the average mobility or lifetime of the carriers in the epitaxial layer [59]. The Raman technique detects with good accuracy these changes of lifetime [63].

In general, the effective electron-hole pair density (n) is controlled by the equilibrium conditions between carrier generation (G) and recombination processes (U); this steady state is expressed by the following expression:

$$U = G = (n - n_0)/\tau, \tag{4.5}$$

where n is the steady-state concentration, n_0 is the initial carrier concentration, τ is the minority carrier lifetime, and G is the carrier generation rate due to the laser exposure

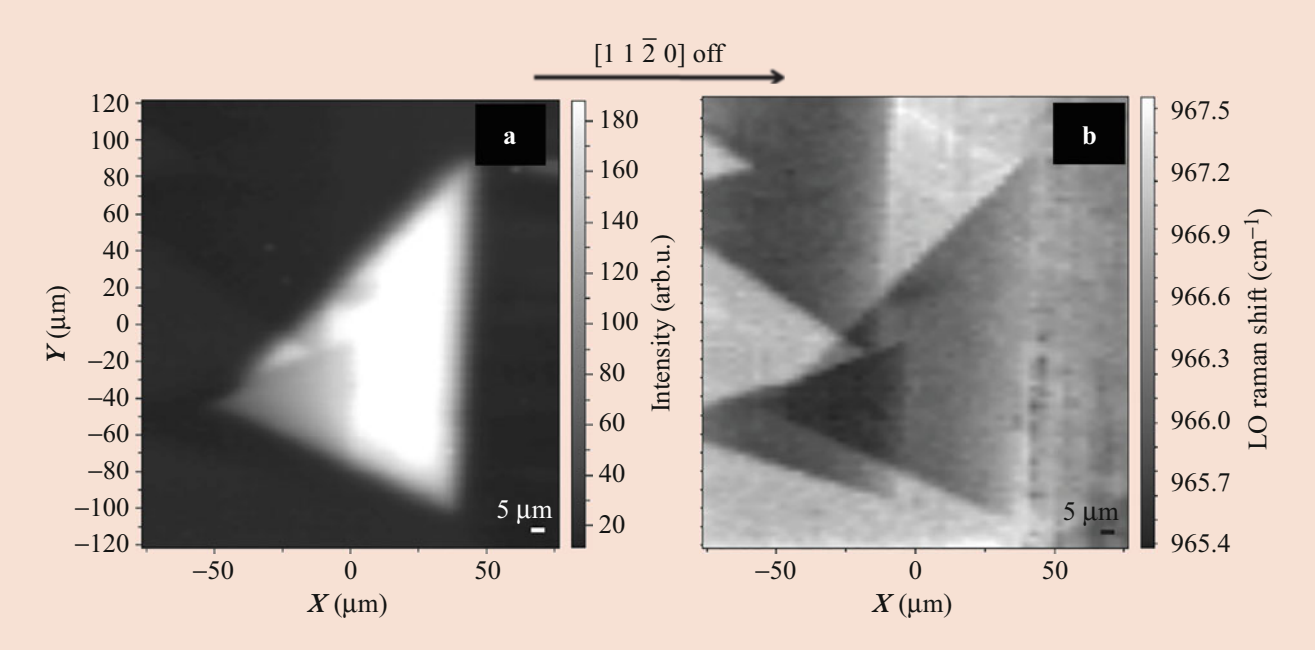


Fig. 4.29 (**a**) Stacking fault (4SSF) observed at 2.7 eV using photoluminescence. (**b**) 4SSF observed at 965 cm^{-1} using the Raman technique. Other defects are also detected. (Reproduced from Piluso et al. [63], with the permission of AIP Publishing)

$$G(x) = \Phi\alpha e^{-\alpha x}, \tag{4.6}$$

where Φ is the laser flux, α the absorption coefficient, and x is the distance within the epitaxial layer at which the carriers are generated. In the case of a highly doped epitaxial layer, low laser densities or low carrier lifetimes, $G\tau \ll n_0$, so that $n - n_0 \sim 0$, and no carrier generation is revealed. Under these conditions, the standard Raman LOPC determines the film doping (n_0). On the other hand, in the case of layers with low doping ($n_0 < 10^{15}$ cm^{-3}) and for high carrier injections ($U > 10^{17}$ cm^{-3} s^{-1}) substantial carrier generation is observed and from Eqs. (4.5) and (4.6) the carrier lifetime can be extracted.

The highest value of the LO Raman shift was observed in the oxidized sample, which has a larger carrier lifetime. An evident conclusion is that decreasing the point defect density increases the electronic free path, determining a longer carrier lifetime than the "as-grown" sample. As an example the data of Fig. 4.30 clearly demonstrate the strong reliability of the Raman method.

In conclusion, these results suggest that micro-Raman spectroscopy, through the i-LOPC method, provides carrier concentration, lifetime, doping, and mobility of 4H-SiC epitaxial films.

4.4 Electrical Parameter Measurements

Resistivity is one of the most important electrical parameters of semiconductors. This section starts with the basic physical relations concerning bulk resistivity. The main electrical measurement techniques are then described: the four-point-probe technique and the van der Pauw technique, together with the main assumptions on which they are based. Special attention is given to the transmission line model (TLM) technique that, besides its typical application to determine the specific contact resistance, can also be used to extract semiconductor resistivity. This technique is widely used on wide band gap (WBG) semiconductors, such as SiC and GaN, where temperature-dependent TLM measurements also enable insight into the ionization energies of the dopant species to be obtained. Detailed examples are reported to illustrate the potentialities of the technique. The remaining part of the section briefly describes the methods of measuring the carrier concentration profile, the mobility, and the carrier lifetime by capacitance-voltage and Hall effect measurements [66].

4.4.1 Four-Point Probe

The DC *electrical resistivity* ρ, expressed in units of [Ω cm], is one of the main parameters of the charge transport in a semiconductor, which is given by the following expression [67]:

$$\rho = \frac{1}{q\left(n\mu_n + p\mu_p\right)}, \tag{4.7}$$

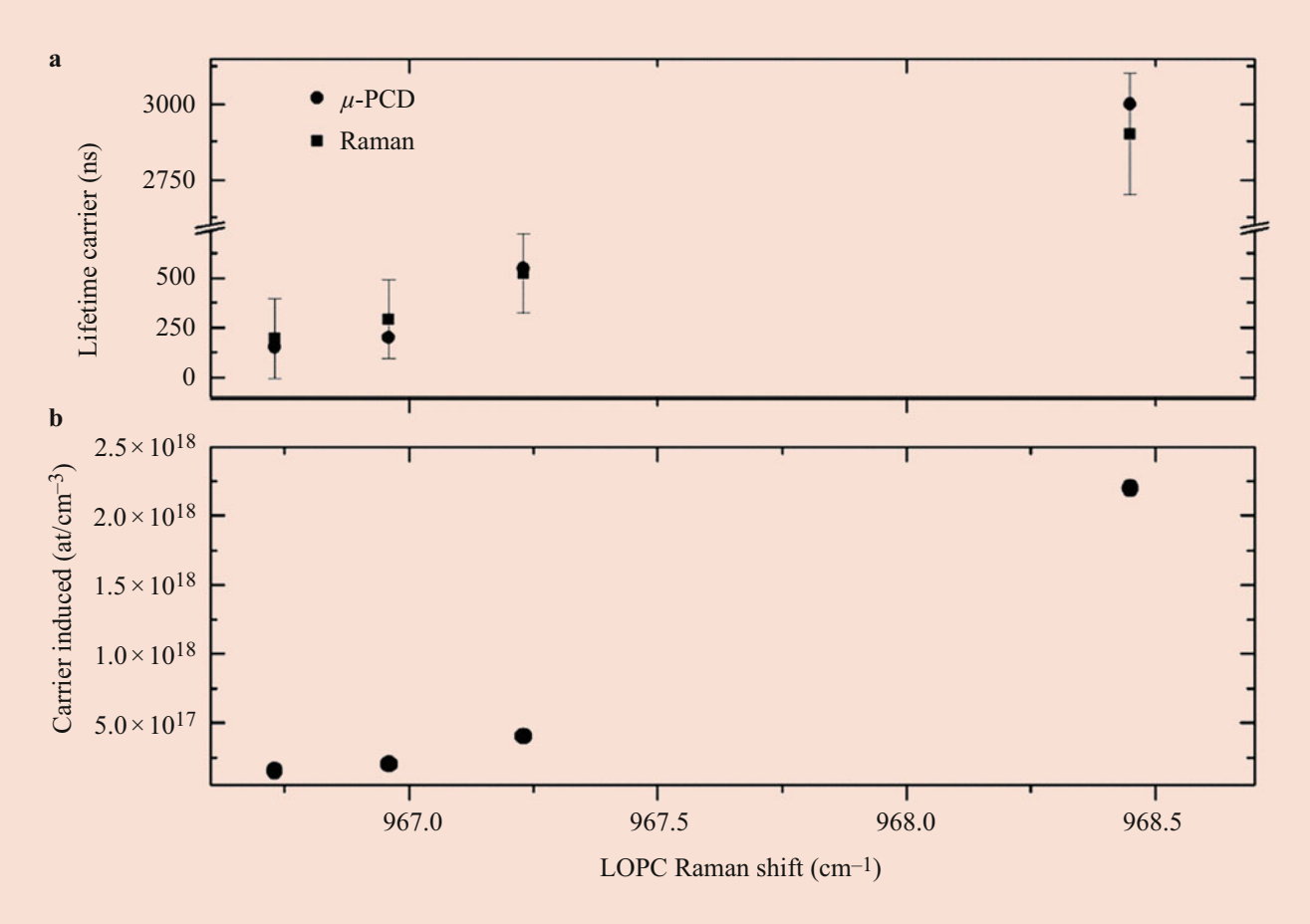


Fig. 4.30 (**a**) Comparison between the evaluation of carrier lifetime (τ) values obtained by μ-PCD and i-LOPC techniques respectively. (**b**) Evaluation of the carrier density (n) induced by laser pumping. (Reproduced from Piluso et al. [63], with the permission of AIP Publishing)

where q is the elementary charge, and n, μ_n, p, and μ_p are, respectively, the electron and hole concentrations and mobilities. It is a relevant parameter for devices and affects many electrical parameters (e.g., barrier height, specific contact resistance, and threshold voltage). The resistivity of a semiconductor can be tailored by the introduction of dopant impurities (e.g., donors or acceptors), either during the crystal growth or in selective regions of the device by ion implantation followed by a thermal treatment. Although in Si the resistivity is usually modified by ion implantation of the dopants, a different situation occurs in other materials, such as in WBG semiconductors. As an example, in SiC, owing to the extremely low diffusion coefficient of the dopants, ion implantation followed by high-temperature annealing (>1600 °C) is the unique method of achieving selective doping of the layer. In gallium nitride (GaN), ion implantation is not well consolidated, owing to the difficulty in avoiding material decomposition at the typical temperatures required for electrical activation (>1000 °C). In this case, selective epitaxial regrowth is preferred.

In a semiconductor in which the majority carrier density is much higher than the minority carrier density, the resistivity is expressed as:

$$\rho = \frac{1}{qn\mu_n} \tag{4.8}$$

for a n-type semiconductor ($n \gg p$) and as

$$\rho = \frac{1}{qp\mu_p} \tag{4.9}$$

for a p-type semiconductor ($p \gg n$).

From the above relationships, the carrier density and mobility must be known to determine the semiconductor resistivity. Otherwise, direct measurement techniques must be adopted, often requiring the fabrication of appropriate test patterns. Usually, the measurements are performed by forcing a known electrical current and by measuring the resulting voltage drop. One major issue for such measurement is to render negligible the contact resistance. This is achieved

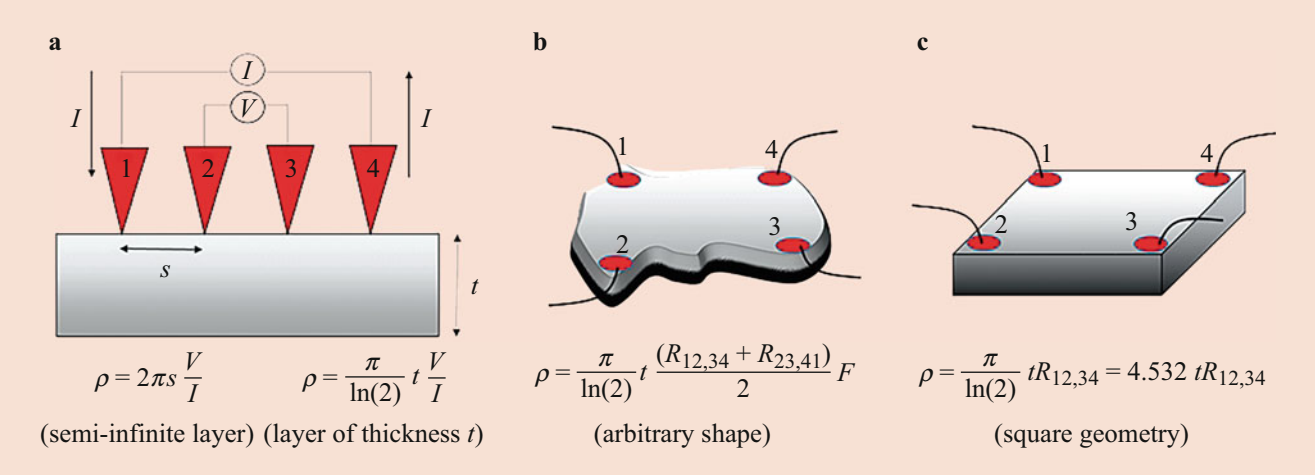


Fig. 4.31 Schematic of (**a**) the collinear four-point probe measurement to determine the semiconductor resistivity, (**b**) an arbitrary shaped sample, and (**c**) a typical square geometry used for Van der Pauw measurements

by using the Kelvin configuration with four contacts, with two separate contacts to force the current I and the other two to sense the voltage drop V. Moreover, for the voltage drop measurement it is necessary to use electrometers with a high input impedance much larger than the sample resistance. Various configurations can be used, among which the most common is the *collinear four-point probe configuration* [68], with all tips placed in line at a distance s, as illustrated in Fig. 4.31a. The two external tips force the current I, whereas the two internal tips sense the voltage drop V. The sample has to be planar and schematized either with infinite or infinitesimal thickness, t, depending on whether $s \gg t$ or vice versa $s \ll t$. For the two cases, the resistivity ρ results are as follows:

$$\rho = 2\pi s \frac{V}{I} \tag{4.10}$$

or

$$\rho = \frac{\pi}{\ln(2)} t \frac{V}{I} \tag{4.11}$$

respectively.

Thin semiconductor layers are often described by the so-called *sheet resistance* R_{SH}, expressed in units of [Ω/sq], which for uniformly doped semiconductors is defined as:

$$R_{SH} = \frac{\rho}{t} = \frac{\pi}{\ln(2)} \frac{V}{I} = 4.532 \frac{V}{I}. \tag{4.12}$$

This important parameter is a measure of the resistivity ρ averaged over the sample thickness t. In specific cases, R_{SH} is more representative than the resistivity. As an example, in AlGaN/GaN heterostructures, the presence of a two-dimensional electron gas (2DEG) [69] at the interface practically limits the current conduction in a sheet of material. In this case, the value of R_{SH} is a measure of the quality of the 2DEG.

If the sample to be characterized consists of a semiconducting layer on a semiconductor substrate (as in the case of epitaxial layers used for device fabrication), the uppermost layer to be measured must be electrically isolated from the substrate. This condition is satisfied when the layers have opposite conductivity (i.e., an n-type layer onto a p-type substrate or vice-versa), and the space charge region formed at the electrical junction guarantees the confinement of the current in the layer under investigation.

Such geometry requires the overall sample size to be infinite, that is, much larger than s, and the tips far from the sample edges. If this is not the case, numerical corrections to take into account the finite sample size are applied [68].

The collinear four-point probe method, however, is not always applicable. *Van der Pauw* developed the theoretical formulation for resistivity measurements on arbitrarily shaped samples [70]. The following assumptions were considered: (i) the contacts are very small with respect to the sample size; (ii) the contacts are located at the periphery of the sample; (iii) the thickness of the semiconductor layer is uniform; (iv) the surface is singly connected with respect to the current flows, i.e., it does not contain holes.

In this case, considering a semiconductor sample of an arbitrary shape, with contacts (1,2,3,4) located along the periphery (Fig. 4.31b), the resistances can be measured using current voltage measurements between different probes (e.g., $R_{12,34} = V_{34}/I_{12}$ or $R_{23,41} = V_{41}/I_{23}$). The resistivity ρ is given by:

$$\rho = \frac{\pi}{\ln(2)} t \frac{(R_{12,34} + R_{23,41})}{2} F, \tag{4.13}$$

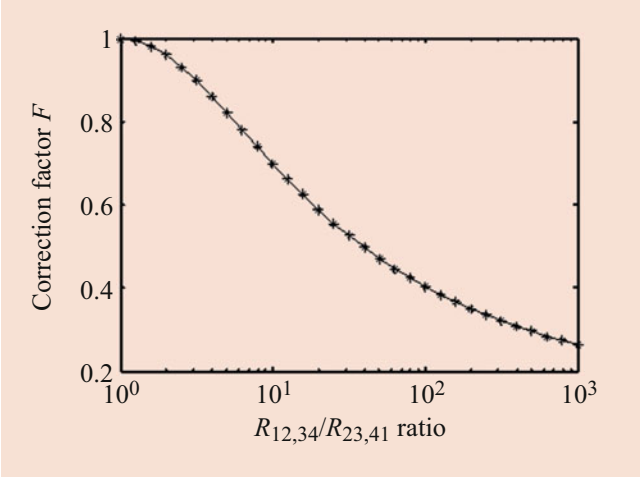


Fig. 4.32 Van der Pauw correction factor F as a function of R_r

where F is a function of the ratio $R_r = R_{12,34}/R_{23,41}$ implicitly given in Eq. 4.14 and plotted in Fig. 4.32:

$$\frac{R_r - 1}{R_r + 1} = \frac{F}{\ln(2)} \operatorname{arcosh}\left(\frac{\exp\left[\ln(2)/F\right]}{2}\right). \tag{4.14}$$

In general, for the characterization of semiconductor layers, symmetrical shape samples are used, e.g., with a regular square geometry such as that illustrated in Fig. 4.31c. As can be seen in Fig. 4.32, for this symmetric geometry $R_r = 1$ and $F = 1$ (more details can be found in Schroder [68]). Then, the expression of the resistivity ρ and of the sheet resistance R_{SH} becomes simpler and formally similar to the four-point probe method, i.e.:

$$\rho = \frac{\pi}{\ln(2)} t R_{12,34} = 4.532\, t R_{12,34}, \tag{4.15}$$

$$R_{SH} = \frac{\pi}{\ln(2)} R_{12.34} = 4.532\, R_{12,34}. \tag{4.16}$$

Other geometries used for determining the semiconductor sheet resistance by Van der Paw measurements are circular, Greek cross, cross bridge structures, etc. [68].

In performing resistivity measurements, a number of precautions have to be taken, the most common of which are the following: (i) the sample is placed on an insulating substrate, which does not contribute significantly to the charge conduction; (ii) the sample temperature is fixed and constant, thus requiring good thermal contact with a substrate of large thermal capacitance; (iii) the current source has to provide low power to the sample, in order to reduce sample heating; (iv) the current level has to be low in order to avoid high injection effects, i.e., injection of carrier densities from the forcing contacts in excess of the specimen carrier concentration.

Alternative approaches to resistivity measurement are contactless, generally applied to semiconductor wafers. The concept is to stimulate eddy currents in the sample under test and to measure the quality factor loss of the LC cavity through an inductively coupled secondary circuit. Such measurements require the additional evaluation of the wafer thickness, which can be done either by ultrasound-based techniques or by capacitive techniques. Contactless eddy current measurements are commonly used to determine the sheet resistance in AlGaN/GaN heterostructures grown onto insulating substrates and to obtain a wafer mapping of the homogeneity of the two-dimensional electron gas.

Although in Si the collinear four-point probe method is a suitable technique for determining the resistivity, in other materials such as SiC and GaN this technique cannot be used. In fact, owing to their wide band gap, it is not easy to make a good ohmic contact between the tip and the semiconductor [71, 72]. Hence, lithographically defined alloyed ohmic contacts must be formed at the sample periphery in Van der Paw structures in SiC and GaN.

4.4.2 Transmission Line Model

Alternative routes to the Van Paw method are adopted for these wide band gap semiconductors. The *transmission line model* (TLM) [73–75] is the method of choice for the determination of the specific contact resistance ρ_c (expressed in units of Ωcm^2) of ohmic contacts. Indeed, all the textbooks focus on the determination of ρ_c by the TLM method. However, in addition to the measurement of the specific contact resistance, the TLM structures enable the semiconductor sheet resistance to be extracted. Therefore, the method is particularly useful in WBG semiconductors, where the collinear four-point probe method cannot be easily applied.

The test structures for the TLM measurements consist of an array of identical metallic pads of length L and width W, at different distances d on a semiconductor surface, as schematically illustrated in Fig. 4.33a. The semiconductor is typically laterally isolated by a mesa etch, forming a resistor of width $W + 2\delta$.

When a current I is injected between two adjacent pads, the potential distribution under a contact in a certain position x will depend on the specific contact resistance ρ_c and on the semiconductor sheet resistance R_{SH}:

$$V(x) = \frac{I\sqrt{R_{SH}\rho_c}}{W} \frac{\cosh\left[(L - x)/L_T\right]}{\sinh\left(L/L_T\right)}, \tag{4.17}$$

where L_T is the so-called *transfer length*, defined as the distance at which the voltage drops to $1/e$ of its maximum value:

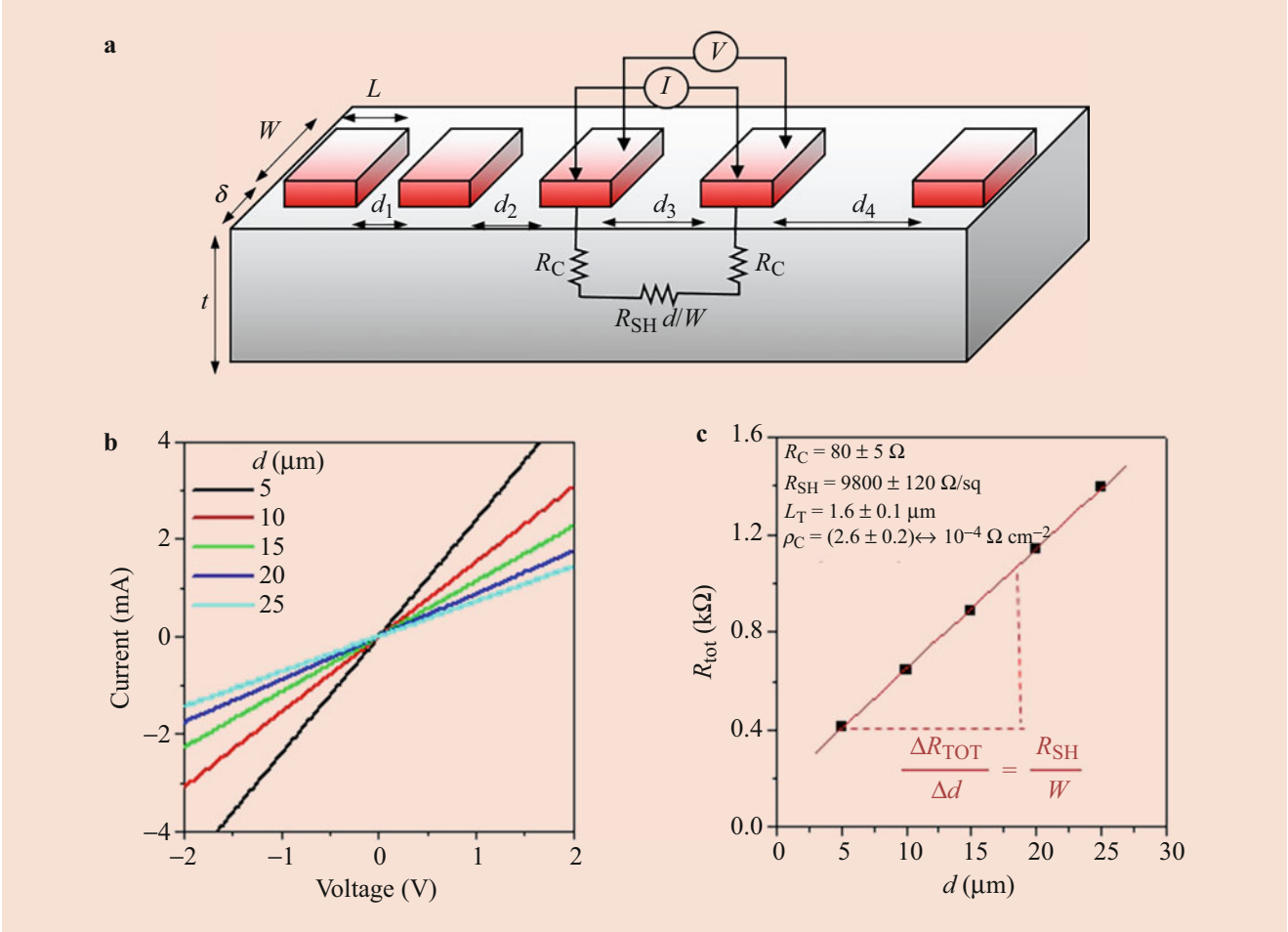


Fig. 4.33 (**a**) Schematic of a transmission line model (TLM) structure to illustrate the operation principle of the technique. (**b**) Example of I-V measurements acquired on adjacent TLM pads placed at different distances *d*. (**c**) Linear plot of the total resistance R_{TOT} as a function of the contacts distance *d*. The experimental data refer to TLM structures fabricated on a p-type implanted 4H-SiC layer (of thickness $t = 300$ nm), using Ti/Al/Ni thin film as ohmic contacts

$$L_T = \sqrt{\rho_c / R_{SH}}. \tag{4.18}$$

Assuming that $\delta \ll W$, the total resistance R_{TOT} between two adjacent pads at a distance *d* depends on both the contact resistance R_C and on the semiconductor sheet resistance R_{SH}:

$$R_{TOT} = 2R_C + \left(\frac{R_{SH}}{W}\right) d. \tag{4.19}$$

By performing current-voltage (I-V) measurements between adjacent pads, the total resistance R_{TOT} can be determined at various pad distances *d*. Then, from a linear fit of R_{TOT} values as a function of *d*, the intercepts with the *y*-axis ($2R_c$) and with the *x*-axis ($2L_T$) can be determined. Figures 4.33a, b show an example of I-V measurements and R_{TOT} vs *d* plot, carried out on TLM structures fabricated on p-type implanted 4H-SiC. From the slope of the linear plot R_{TOT} vs *d* plot in Fig. 4.33c a sheet resistance of 9800 Ω/sq is obtained. The resistivity of the 4H-SiC layer is given by $\rho = R_{SH}\, t = 0.29$ Ωcm [76].

For alloyed contacts, the *semiconductor sheet resistance under the contact* (R_{SK}) can be different from its bulk value R_{SH} measured outside the contacts (see Fig. 4.34a). Hence, the correct value of the transfer length L_T cannot be simply extracted by the *x*-axis intercept of the R_{TOT} vs *d* plot; it must be obtained by an additional measurement of *end-contact resistance* [74, 75]. The end contact resistance R_E can be seen as the resistance due to the voltage drop at the end of the contact length. The standard procedure to determine this parameter is to force a constant current (*I*) between two adjacent TLM pads and to measure the potential (*V*) between one of these pads and an opposite outside TLM pad (Fig. 4.34b) [75]. Contact resistance R_C and end contact resistance R_E are related by:

$$\frac{R_C}{R_E} = \cosh\left(\frac{L}{L_{TK}}\right) \tag{4.20}$$

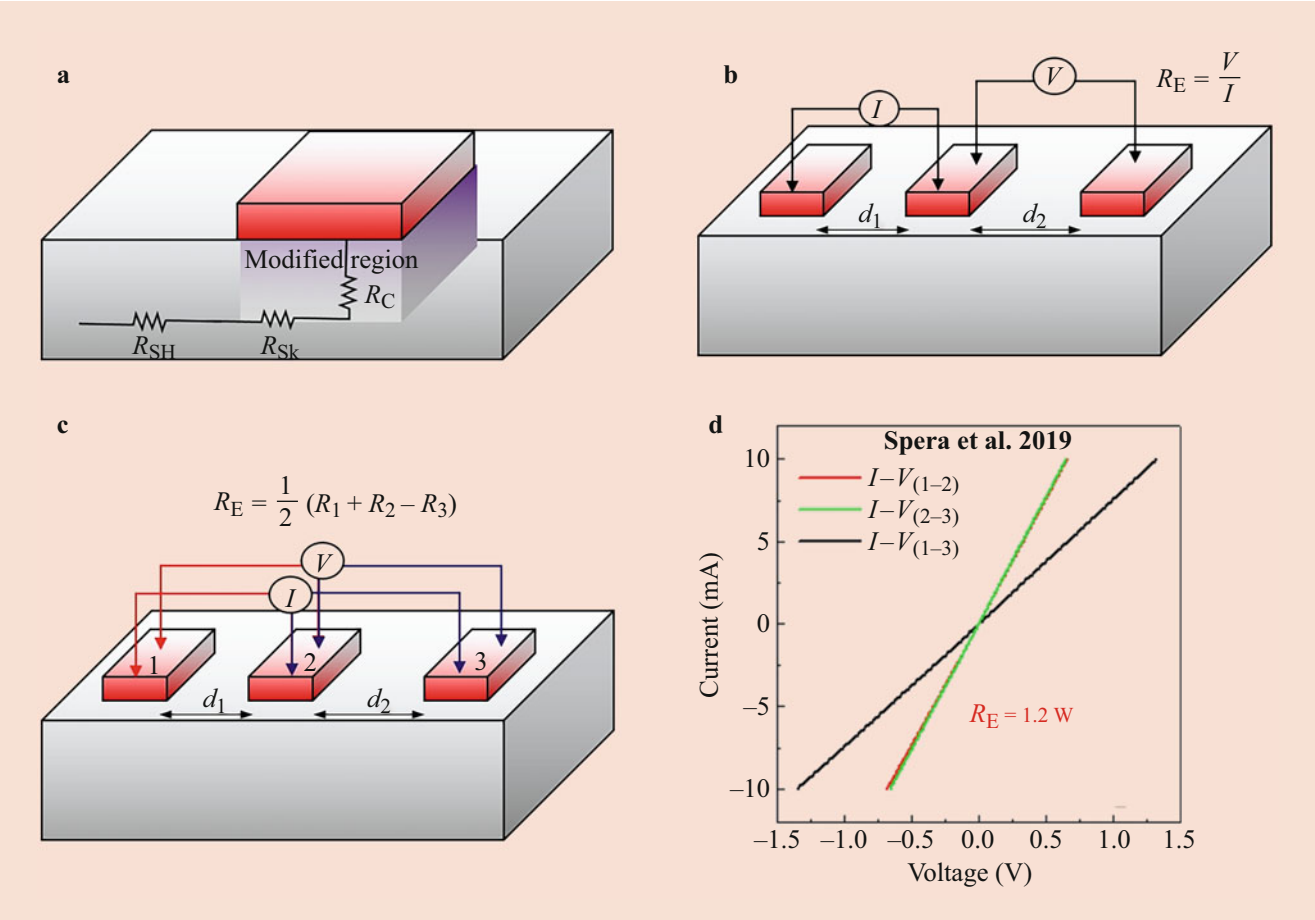


Fig. 4.34 (**a**) Schematic representation of the modification of the sheet resistance of a semiconductor material under the contact. (**b**) Conventional method of determining the end contact resistance. (**c**) Alternative three terminals procedure proposed in Reeves and Harrison [75]. (**d**) Application of the three terminals method for the determination of R_E in alloyed Ti/Al/Ni/Au ohmic contacts to AlGaN/GaN heterostructures. (Figure (**d**) is adapted with permission from Spera et al. [77], Copyright © 2017, Elsevier Ltd)

Hence, from a measurement of the R_E it is possible to extract the corrected transfer length L_{TK}, i.e., the transfer length in the case that $R_{SH} \neq R_{SK}$. Finally, the sheet resistance under the contact R_{SK} becomes:

$$R_{SK} = \frac{R_{SH} L_T}{L_K}. \tag{4.21}$$

However, measuring the end contact resistance from the voltage drop at the end of the contact is extremely difficult, owing to the very low values of the voltage drop. An equivalent procedure [75] to determine R_E from I-V measurements on a "three terminals test-pattern", is schematically shown in Fig. 4.34c. The measured resistances between the adjacent contacts 1–2 and 2–3 (R_1 and R_2) placed at a distance d, and between the two external ones 1–3 (R_3), give R_E by the relation:

$$R_E = \frac{1}{2}(R_1 + R_2 - R_3). \tag{4.22}$$

As an example, Fig. 4.34d shows the I-V characteristics acquired in the three terminals test-pattern to determine the end contact resistance R_E on alloyed Ti/Al/Ni/Au ohmic contacts to AlGaN/GaN heterostructures [77].

In most of the cases, the metal stacks for the ohmic contacts are subjected to thermal annealing, which can lead to reactions with the substrate and formation of new phases. Under these conditions, the sheet resistance of the semiconductor under the contact R_{SK} is modified with respect to its value outside the contact pad. Its knowledge is a useful input parameter for device technology computer-aided design (TCAD) simulation and a valuable insight into the physical effect of the alloying/sintering process of ohmic contacts. However, these kinds of measurements are not widely discussed in the literature.

Table 4.1 reports a survey of literature data extracted by TLM measurements on different semiconductor materials. As can be seen, a reduction of the sheet resistance under alloyed contacts is typically revealed by the end contact resistance measurements on TLM structures.

Table 4.1 Survey of literature data of sheet resistance R_{SH} and sheet resistance under the contact R_{SK} obtained by transmission line model measurements on different n-type semiconductors. The annealing temperatures and the adopted processes for ohmic contact formation are also reported

Semiconductor	Contact process	R_{SH} (Ω/sq)	R_{SK} (Ω/sq)	Reference
Si	Al; sintered	2100	430	[75]
GaAs	Ni/Ge/Au; alloyed	430	22	[75]
GaAs	AuGe/Ni/Au; $T_{ann} = 400$ °C	276	49	[78]
InP	Ni/Ge/Au; $T_{ann} = 750$ °C	200	20	[79]
6H-SiC	Ni; $T_{ann} = 900$ °C	1652	92	[80]
GaN	Ti/Al/Ni/Au; $T_{ann} = 850$ °C	40	3	Present work
AlGaN/GaN	Ti/Al; $T_{ann} = 900$ °C	505	236	[81]
AlGaN/GaN	Ti/Al/Ni/Au; $T_{ann} = 800$ °C	535	26	[77]
AlGaN/GaN	Ti/Al/Ti; $T_{ann} = 500$ °C	565	114	Present work

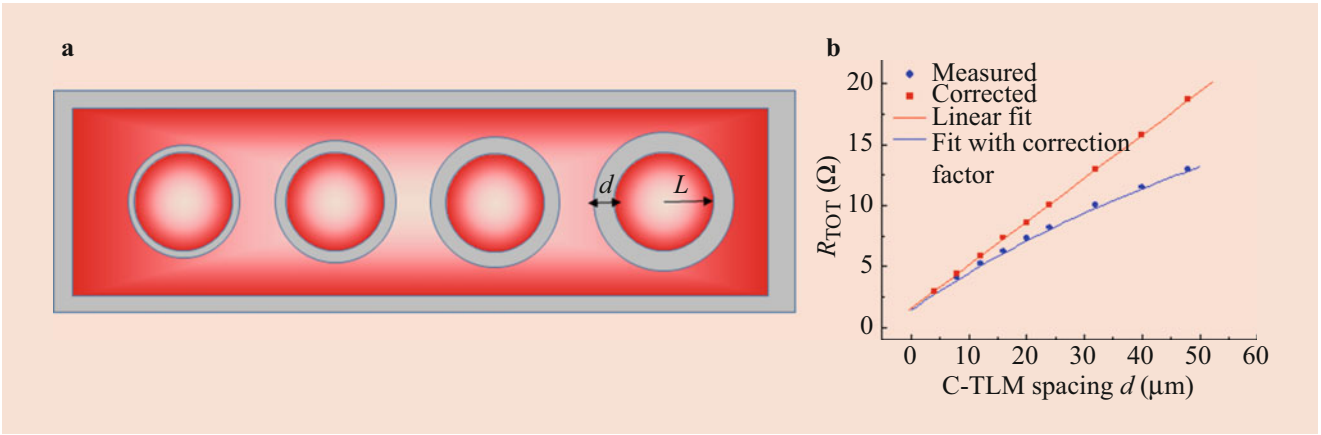


Fig. 4.35 (**a**) Schematic of a circular transmission line model (C-TLM) structure. (**b**) Example of total resistance R_{TOT} versus pad spacing d plot in C-TLM before and after the application of the correction factor

The TLM method is based on the assumption of identical contact pad and diffusion layer widths. However, in real cases the contact width W is smaller than the TLM resistor, thus causing lateral current crowding effects that reduce the accuracy of the analysis. In fact, lateral current crowding decreases the measured value of the total resistance R_{TOT}, owing to the presence of outer conductive paths, acting as a parallel conductance. Hence, the simple one-dimensional TLM analysis leads to a lower slope (i.e., a lower extracted R_{SH}) in the plot of Fig. 4.34c. To take into account these parasitic effects, correction factors are introduced or evaluated by complex two-dimensional models [82–84]. Practically, lateral current crowding effects can be avoided using the *circular transmission line model* (C-TLM) [68, 85, 86]. The C-TLM pattern is a sequence of symmetrical structures consisting of circles of radius L and annuli of varying width d, as schematically shown in Fig. 4.35a. By applying a bias between the external and the internal contact, the current will flow in the radial direction.

The analytical description of the C-TLM is rather complex. However, for large structures, $L \gg d$, the total resistance R_{TOT} measured between two adjacent contacts simplifies to [68, 86, 87]:

$$R_{TOT} = \frac{R_{SH}}{2\pi L}(2L_T + Cd) \tag{4.23}$$

where $C = \frac{L}{d}\ln\left(1 + \frac{d}{L}\right)$ is a correction factor.

Then, for $d/L \ll 1$, R_{TOT} assumes the following linear expression with the pad spacing d:

$$R_{TOT} = L_T\frac{R_{SH}}{\pi L} + \frac{R_{SH}}{2\pi L}d \tag{4.24}$$

Also in this case, from a linear fit of the R_{TOT} vs d plot, it is possible to extract the semiconductor sheet resistance R_{SH} and, hence, its resistivity $\rho = R_{SH}\, t$. An example of C-TLM measurement before and after the application of the correction factor is reported in Fig. 4.35b.

The fabrication of C-TLM test structures is easier than the linear TLM structure. In fact, in the C-TLM structures only one lithography mask level is required and no dry etching processes are needed to define the diffusion layer, contrary to the linear TLM patterns [71]. However, in the C-TLM extremely low metal sheet resistance is required to obtain measurement with good accuracy [87].

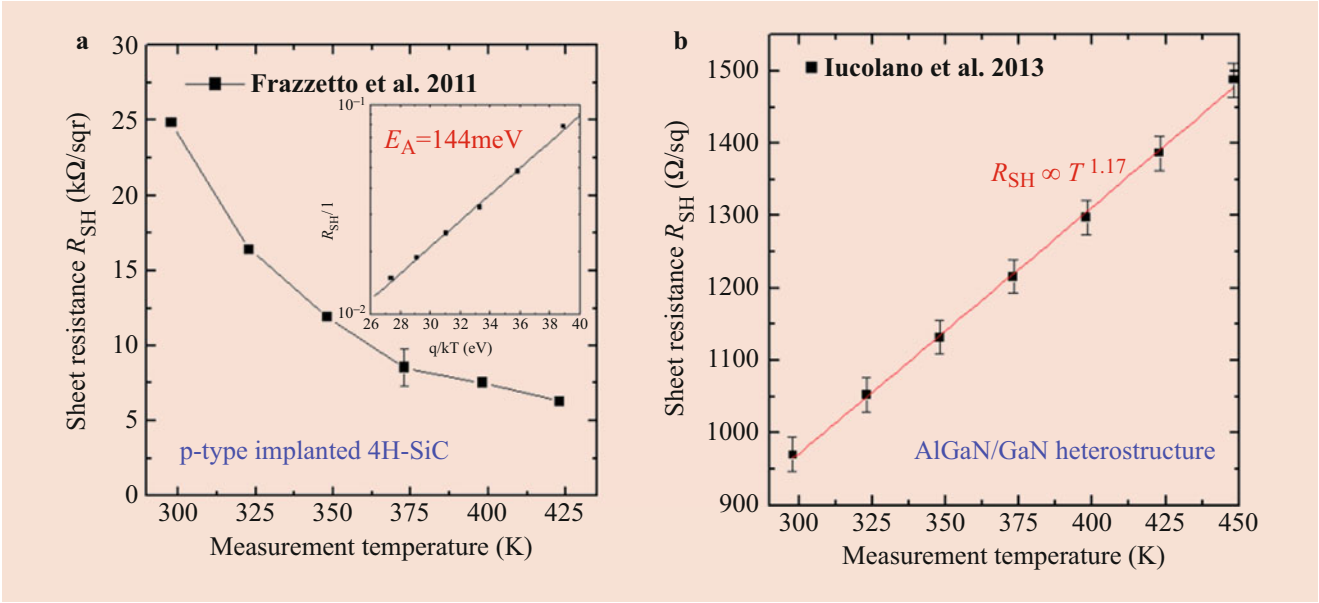


Fig. 4.36 Example of temperature dependence of the semiconductor sheet resistance measured using TLM structure for (**a**) a p-type doped 4H-SiC layer (reproduced with permission from Frazzetto et al. [88] Copyright © 2011, IOP Publishing) and (**b**) an AlGaN/GaN heterostructure. (Reproduced with permission from Iucolano et al. [90], copyright © 2013, AIP Publishing)

Temperature-dependent measurements on TLM structures provide additional insights into important parameters, such as the ionization energy of the dopant species and physical mechanism in semiconductors. The decrease in the semiconductor resistivity with increasing temperature is related to the increase in the ionized dopant concentration. This aspect is particularly important in SiC, where the wide band gap and the high ionization energy of the dopant (especially in p-type doped material) implies that only a small fraction of the donors or acceptors might be ionized at room temperature. In this case, the temperature dependence of the sheet resistance is mainly ruled by the exponential dependence of the active dopant concentration on the ionization energy E_A, i.e., $R_{SH} \propto \frac{1}{\exp(-E_A/kT)}$ [67, 68].

Figure 4.36a reports as an example the temperature dependence of the sheet resistance R_{SH} of a p-type implanted 4H-SiC layer [88]. An Arrhenius plot of the sheet resistance (see inset) gives the value of the ionization energy of the acceptors (aluminum): $E_A = 144$ meV. Recently, this method has been successfully applied to p-type implanted 4H-SiC layers subjected to different post-implantation conditions, demonstrating the dependence of the ionization energy on the acceptor concentration [76, 89].

In other systems, such as AlGaN/GaN heterostructures, the presence of a 2DEG induces "metal-like behavior" of the resistivity. In this case, as shown in Fig. 4.36b, the sheet resistance R_{SH} measured on TLM structures increases with increasing temperature, following a power law $T + \beta$ (with $\beta = 1.17$) [90].

4.4.3 Carrier Concentration Profile

The determination of the electrically active dopant distribution within semiconductor materials is a key requirement for the fabrication of electronic devices.

Secondary ions mass spectrometry (SIMS) is the most commonly employed technique for 1D dopant concentration profiling in semiconductors, owing to its excellent sensitivity, good quantification properties, high depth resolution, and ease of application [91–93]. For routine applications, SIMS measurements are carried out on blanket samples on a rather large analysis area (from ~20 × 20 to 200 × 200 μm^2), in order to collect a large number of secondary ions (10^8–10^9 for an average profile) with excellent signal/noise ratio and statistical relevance. This method has been widely employed to study dopant incorporation and diffusion in silicon technology, as well as in compound semiconductors.

On the other hand, the depth distribution of the electrically active dopants can be determined by several electrical profiling methods, including capacitance-voltage (C-V) measurements, differential Hall effect (DHE) measurements [94], and the spreading resistance probe (SRP) [95].

The C-V profiling method relies on a Schottky or metal-semiconductor junction, and information on the depth distribution of the majority carrier concentration, i.e., the active dopants ($N_D - N_A$) in the semiconductor is achieved by progressively increasing the junction reverse bias, i.e., the width of the depletion region. In fact, if $W(V)$ is the depletion

layer thickness of the junction under a reverse bias V and Q_s is the semiconductor charge, then

$$Q_s = qA \int_0^W N \mathrm{d}x \tag{4.25}$$

where N is the net doping density, in equilibrium equal to the net carrier density, and A the junction area. The differential capacitance C is given by:

$$C = -\mathrm{d}Q_s/\mathrm{d}V \tag{4.26}$$

and

$$C = k\varepsilon_0 A/W, \tag{4.27}$$

where ε_0 is the vacuum dielectric constant and k the low frequency relative dielectric constant. It follows that:

$$N = -\frac{C^3}{qk\varepsilon_0 A^2 \mathrm{d}C/\mathrm{dV}}. \tag{4.28}$$

The $N(W)$ function is obtained by using Eqs. (4.27) and (4.28) and the C-V curve data in reverse bias. Note that Eq. (4.28) has a strong dependence on the area, so A has to be known with good accuracy for an accurate N profiling. The metal-semiconductor C-V technique for carrier profiling can be performed by depositing a metal structure on the planar semiconductor or by using an Hg probe. The latter in principle does not require sample preparation for the metal–semiconductor junction geometry formation, but in any case, much care has to be taken in order to verify that the contact to the semiconductor is ohmic or of a very large area, in order to provide a negligible contribution to the measured capacitance. Clearly, because of this working principle, this approach can work only for relatively low-doping concentrations ($N_D - N_A$ up to 10^{17}–10^{18} cm^{-3}).

A very similar approach can be used in metal–oxide–semiconductor (MOS) junction structures, although in such cases Eq. (4.27) should be modified to take into account the oxide capacitance in series with the semiconductor capacitance C, still given by Eq. (4.27). Moreover, the MOS junction should be driven into deep depletion, the reverse bias ramp has to be quickly compared with the time required for the MOS inversion layer build-up. This time T is given by:

$$T = 10\, N/n_i \tau_g, \tag{4.29}$$

where n_i is the intrinsic carrier concentration and τ_g the generation lifetime. Note that T is much larger than the carrier lifetime, depending on the ratio of the active doping concentration and the intrinsic carrier concentration. The MOS C-V technique for carrier profiling can be also extended to the case of an air gap rather than a complete MOS junction. Such an approach is therefore a contactless carrier profiling technique, and it only requires special probes to realize a metal–air–semiconductor junction and proper semiconductor surface preparation.

Another technique for the carrier concentration measurement is the Hall effect technique. The Hall coefficient is experimentally determined by the ratio

$$R_H = \frac{tV_H}{BI}, \tag{4.30}$$

where t is the sample thickness, V_H the Hall transverse voltage, B the magnetic field, and I the forced current. In Hall geometry, for hole conduction, the magnetic field, the current density, and the Hall field are oriented according to the right-hand rule. For electron conduction, the Hall coefficient has the opposite direction. Therefore, the Hall effect allows a distinction to be made between hole or electron conduction in a semiconductor or a metal. In general, it can be demonstrated that the Hall coefficient, in the approximation of an energy-independent scattering time, is given by:

$$R_H = \frac{\left(p - b^2 n\right) + \left(\mu_n B\right)^2 (p - n)}{q\left[\left(p - b^2 n\right)^2 + (\mu_n B)^2 (p - n)^2\right]}, \tag{4.31}$$

where b is the ratio μ_n/μ_p. The low field limit is when $B \ll 1/\mu_n$ for an p-type material, or when $B \ll 1/\mu_p$ for an n-type material. This means $B \ll 10T$ for a mobility of 1000 cm^2/Vs and $B \ll 0.1T$ for a high mobility material with μ of 1×10^5 cm^2/Vs. Generally, for semiconductors such as Si with $b < 10$ and μ_n 1000 cm^2/Vs or less, and with B of $1T$ or less, the Hall coefficient simplifies into $R_H = 1/q(p - n)$. In fact, by taking into account an energy-dependent scattering time, one finds that for an n-type material:

$$R_H = -r/qn \tag{4.32}$$

and for a p-type:

$$R_H = +r/qp, \tag{4.33}$$

where $r = <\tau^2>/<\tau>^2$ is the scattering factor. r depends on the scattering mechanism: $r = 1.18$ for phonon scattering; $r = 1.93$ for charged impurity scattering; $r = 1$ for neutral impurity scattering. In general, $r \to 1$ for $B \to \infty$. r can then be directly measured as the ratio $R_H(B)/R_H(\infty)$. In other semiconductor materials, the lack of experimental data and models often leads to the assumption that the Hall scattering factor is equal to one. However, this can lead to an overestimation of the carrier density. In the case of p-type 4H-SiC, the Hall scattering factor has been determined by correcting

the experimental carrier density determined by Hall measurements, with the doping and compensation levels extracted by independent *C-V* and SIMS measurements [96, 97].

The Hall effect, thanks to its experimental simplicity, is heavily used in semiconductor characterization for carrier density measurements, especially for the measurement of the carrier concentration as a function of temperature. This is particularly useful for identifying the temperatures of the intrinsic regime at a high temperature and for the carrier freeze-out regime at a low temperature. The DHE profiling relies on the combination of conventional Hall effect measurements with iterative chemical etching of the semiconductor surface, with the depth resolution defined by the etch rate. Both the *C-V* and DHE approaches have the advantage of being absolute methods, as they do not require calibration samples.

Finally, the SRP approach is based on resistance measurements carried out by two aligned probes moved on the beveled surface of the semiconductor sample, thus allowing depth resolved information. The SRP has been employed as a 1D carrier profiling method in silicon technology, owing to its wide dynamic range (from 10^{15} to 10^{20} cm^{-3} both for n- and for p-type doping). The quantification of the carrier concentration from the measured resistance profiles requires the minimization of the tip contact resistance contribution (achieved by applying a high pressure with the metal (tungsten) tips to Si) and the knowledge of the mobility dependence on the doping. Furthermore, an optimized preparation protocol of the beveled surface is required to minimize the effects of surface damage. In practice, quantitative carrier profiling by SRP relies on the use of proper n- and p-type calibration samples, consisting of CVD-grown multilayers with different independently measured doping concentrations.

The above-discussed electrical profiling techniques were developed and widely employed in silicon technology. On the other hand, extending their application to other semiconductors required proper optimization or the adoption of specific calibration samples, and, in some cases, it proved unsuccessful. As an example, SRP profiling in the case of SiC is prevented by the high contact resistance of the probes on this wide-band-gap semiconductor, as well as by SiC hardness, causing rapid degradation of the probes.

4.4.4 Mobility

From the measurement of the resistivity and the Hall coefficient in a material, given the relationship between ρ, μ, and R_H (see Eqs. (4.7), (4.31), and (4.32) or (4.33), one can deduce the carrier mobility. The Hall mobility is defined as the ratio:

$$\mu_H = R_H/\rho. \tag{4.34}$$

Therefore, μ_n (or μ_p) can be determined as the ratio μ_H/r.

Various sample geometries can be used, and one of the most frequently adopted is the Van der Pauw geometry, shown in Fig. 4.31b, with the magnetic field oriented orthogonal to the figure plane. It can be shown that μ_H is given by

$$\mu_H = \frac{t\Delta R_{24,13}}{B\rho}, \tag{4.35}$$

where $\Delta R_{24,13}$ is the difference of the resistance $R_{24,13}$ measured with and without the application of the magnetic field B. The carrier mobility can be measured by many other techniques, but these generally require transistor device structures such as MOSFETs, junction-gate field-effect transistors, metal–semiconductor field-effect transistors, high-electron-mobility transistor, etc. In this case, the effective mobility or the field effect mobility is determined from the device conductance or transconductance [68]. The extraction of these parameters is treated in other chapters of this book.

4.4.5 Carrier Lifetime

Carrier lifetimes in a semiconductor are related to the carrier generation and recombination processes. When these are bulk processes, the lifetimes are represented by characteristic recombination and generation lifetimes, τ_r and τ_g respectively. When such processes take place at surfaces or at interfaces, then the characteristic figures are surface recombination and generation velocities, s_r and s_g, which have the dimension of a velocity. Three processes rule the recombination: Auger (τ_{Aug}), Shockley–Read–Hall (SRH, τ_{SRH}), and radiative (τ_{rad}), and the overall τ_r is given by:

$$1/\tau_r = 1/\tau_{Aug} + 1/\tau_{SRH} + 1/\tau_{rad}. \tag{4.36}$$

An analogous relationship is valid for $1/\tau_g$, where instead of $1/\tau_{Aug}$, one has to consider the effect specular to the Auger, that is, the impact ionization, whereas for $1/\tau_{SRH}$ one has to consider the SRH generation processes. For the τ_r measurement, a number of techniques are available. Two techniques of great interest and of common use are transient photoconductance decay (PCD) and the quasi steady-state photoconductance (QSSPC) method. Both techniques are based on the measurement of the transient of the photoconductance during or after the application of an illumination stimulus. In general, in a p-type semiconductor the excess minority carrier Δn under uniform illumination is ruled by the continuity equation:

$$\frac{\partial \Delta n}{\partial t} = G - R = G - \frac{\Delta n(t)}{\tau_{eff}}. \tag{4.37}$$

In transient photoconductance decay, a light pulse with a sharp decay is applied. After the pulse $G \ll \mathrm{d}\Delta n/\mathrm{d}t$, and therefore

$$\tau_{\mathrm{eff}}(\Delta n) = -\frac{\Delta n(t)}{\mathrm{d}\Delta n(t)/\mathrm{d}t}. \tag{4.38}$$

In the quasi steady-state photoconductance method, on the contrary, a slowly varying light stimulus is applied. Then, $G \gg \mathrm{d}\Delta n/\mathrm{d}t$, and therefore:

$$\tau_{\mathrm{eff}}(\Delta n) = \frac{\Delta n(t)}{G}. \tag{4.39}$$

τ_{eff} is not directly the bulk lifetime τ_{r}, but rather a combination of τ_r and s_{r}, also dependent on the minority carrier diffusivity D and the sample thickness (see Schroder [68] for details). PCD can be affected by a contactless time-resolved measurement of the photoconductance, from which Δn is evaluated. This is done through an RF bridge or a microwave reflectivity measurement. For the QSSPC one needs to measure Δn, evaluated from the photoconductance, and G, evaluated from a calibrated photodiode.

A widely employed technique to determine the nature and concentration of defects responsible for SRH generation in semiconductors is deep-level transient spectroscopy (DLTS). The most typical DLTS technique measures capacitance transients in metal–semiconductor junctions. The concept is the following: a voltage pulse first forward biases the junction. During this phase, the defects in the semiconductor quasi-neutral region are filled with majority carriers. Then a sudden reverse bias step pulse at a constant voltage V is applied. Under such a condition, the junction is in depletion and the junction capacitance C is:

$$C = A\sqrt{\frac{qk\varepsilon_0 N}{2\,(V_{\mathrm{bi}} - V)}}, \tag{4.40}$$

where V_{bi} is the junction built-in voltage and N is the total net density of charged impurities. N is the net doping density plus the charged defect density in the depletion layer. During the period in which the junction is reverse biased N changes because the defects filled during the previous forward bias pulse can emit electrons to the conduction band or holes to the valence band, depending on the nature of the defect. Such emission changes N, and therefore C, and one therefore observes a capacitance transient. The sign of the transient, i.e., whether N increases or decreases with time, provides the nature of the emission process, i.e., whether one observes electron or hole emission. The capacitance transients are systematically analyzed as a function of the junction temperature, and from such study the defect ionization energy and carrier capture cross-section are measured.

DLTS measurements can be performed by monitoring capacitance, current or charge transients. DLTS [68, 98]. It is a very powerful technique, which allows the identification of numerous types of defects in various types of semiconductors, with excellent sensitivity. There are numerous other τ_{r} and τ_{g} measurement techniques, mostly based on semiconductor device structures, that are described in other sections of this book. More detailed descriptions of such methods are reported in Schroder [68].

4.5 One-Dimensional and Two-Dimensional Electrically Active Dopant Profiling

In the previous section, we discussed the basic relations between the relevant electrical parameters and presented simple experimental techniques. In the present section, a brief presentation of other methods adopted for the measurement of carrier profile in compound semiconductors is provided. The main part of the section deals with, in great detail, the electrical atomic force microscopy (AFM) techniques for the characterization of nanosized regions. Carrier concentration profiles and mobility can be determined by these methods at the nanoscale size, not only in silicon-based devices but also in compound devices, with some limitation, for example, the necessity of calibration curves. As examples, the analysis of 4H-SiC MOSFET, of AlGaN/GaN heterostructure, and of a planar MOSFET structure illustrates the possibilities of the technique.

4.5.1 Experimental Methods

The application of traditional carrier profiling techniques to other semiconductors beyond silicon on one hand and the extreme miniaturization of the state-of-the-art silicon devices on the other present several challenges. In the first case (compound semiconductors), two-dimensional (2D) or even three-dimensional (3D) characterization methods are required [99], which are able to furnish the 2D carrier and dopant distribution inside the semiconductor with high sensitivity (10^{14}–10^{21} cm^{-3}) and high spatial resolution (<1 nm). In this context, a 2D version of secondary ions mass spectrometry (2D-SIMS) and the atom probe tomography techniques have been developed for 2D/3D chemical mapping of dopants [99]. However, these techniques are difficult and extremely expensive to implement.

On the other hand, relevant efforts have been dedicated in the last 20 years to developing electrical characterization techniques based on AFM, in order to meet the requirements scheduled in the International Technology Roadmap for Semiconductors [100] for spatial resolution, concentra-

tion, and concentration gradient sensitivity in 2D carrier profiling.

Among the large number of electrical AFM techniques, *scanning capacitance microscopy* (SCM), *conductive atomic force microscopy* (CAFM), and *scanning spreading resistance microscopy* (SSRM) are the most promising ones for 2D carrier profiling, owing to their ability to carry out capacitance and current measurements with nanometer resolution [101–103]. Although these measuring techniques are currently implemented in commercial AFM microscopes, in most of the cases they are employed only for qualitative imaging of carrier profiles. On the other hand, only a few specialized laboratories worldwide developed dedicated sample preparation protocols and quantification algorithms for the conversion of the measured 2D maps in carrier concentration maps.

In the following, we limit the discussion to SCM and SSRM techniques, presenting the working principles; the application of these techniques to relevant case studies in silicon technology, as well as to other semiconductors, will be provided.

In SCM measurements, a conductive AFM tip is scanned, in contact mode, on the surface of a semiconductor coated with an ultrathin (few nanometers) insulating film (usually SiO_2, but also high-k dielectrics), thus forming a nanometric metal–insulator–semiconductor (nanoMIS) device, as schematically depicted in Fig. 4.37a. The tip is connected to a high-sensitivity capacitance sensor, which records the capacitance variations due to changes of the semiconductor depletion volume underneath the tip in response to the AC modulating bias. Owing to its nanoscale dimensions, the capacitance of the nanoMIS structure is to the order of 10^{-18} F. This is illustrated in Fig. 4.37b, showing the calculated C–V curves for an AFM probe (with a typical curvature radius of 20 nm) on p- and n-type Si (10^{15} and 10^{17} cm^{-3} respectively) coated with a 2-nm-thick SiO_2 layer. A SCM map is formed of a 2D array of values proportional to the derivative dC/dV at the fixed DC bias applied to the sample. The DC bias is usually fixed on the peak of the dC/dV curve, corresponding to the flat-band voltage condition. Obviously, the sign of dC/dV is negative for p-type doped semiconductors and is positive for n-type doped semiconductors (as illustrated in Fig. 4.37c), thus distinguishing between different types of doped areas. Moreover, the absolute value of the dC/dV curve decreases monotonically with increasing carrier concentration.

Two typical calibration curves [104], correlating the SCM signal (proportional to $|dC/dV|$ through the capacitance sensor gain) with the carrier concentration for p-type and n-type Si are reported in Fig. 4.37d, e respectively. The experimental points are measured on dedicated calibration samples, whereas the lines are calculated with a 3D model of the nanoMIS capacitor [104]. These curves show a sensitivity with a wide concentration range ($\sim 10^{15}$ to $\sim 10^{20}$ cm^{-3}), which is limited at the highest concentrations ($>10^{20}$ cm^{-3}) by the very small capacitance variations (i.e., no depletion of the semiconductor), and at the lowest concentrations ($<10^{15}$ cm^{-3}) by the oxide–semiconductor interface states [105].

The SCM lateral resolution is concentration dependent too, as the probed semiconductor volume underneath the tip is ultimately related to the maximum depletion extension W. As an example, for a tip curvature radius of ~20 nm and for carrier concentrations $>10^{18}$ cm^{-3}, the lateral resolution on a uniformly doped Si sample is set by the tip dimension itself, whereas for carrier concentrations $<10^{18}$ cm^{-3}, the lateral resolution is set by the depleted semiconductor volume underneath the tip. An improved depth resolution is achieved by the geometrical magnification of the sample region under investigation by angle beveling [106]. Quantitative carrier profiles with nanometric resolution (along the bevel direction) have been obtained using this method on unipolar-doped semiconductors [107]. However, some caution must be taken in the interpretation of SCM measurements on beveled bipolar devices, owing to the occurrence of the carrier spilling effect [108], determining a shift of the electrical junction position toward the surface.

The SSRM technique [109] is a variant of CAFM. In SSRM, a hard conductive tip (typically, a Si tip coated with a doped diamond film or a full diamond tip [110]) is scanned in contact mode applying a high force on the cross-sectioned sample's surface, whereas a DC bias is applied between the tip and an ohmic contact on the backside (see schematic in Fig. 4.38a). The resulting current is measured using a logarithmic current amplifier (with a typical dynamic range from 1 pA to 0.1 mA) connected to the tip. As illustrated in Fig. 4.38b, the total measured resistance R is the sum of the following contributions:

$$R = R_{tip} + R_c + R_{spr} + R_B + R_{bc}, \tag{4.41}$$

where R_{tip} is the resistance of the conductive probe, R_c is the tip–semiconductor contact resistance, R_{spr} is the spreading resistance encountered by the current to spread in the nanometric semiconductor volume underneath the tip, R_B is the resistance of the bulk semiconductor, and R_{bc} is the back-contact resistance. Among these contributions, only R_c and R_{spr} are related to the local electrical properties of the semiconductor and, under typical conditions, are much larger than the other terms, owing to the nanoscale size of the tip–semiconductor contact. In particular, R_{spr} is proportional to the local semiconductor resistivity ρ as $R_{spr} = \rho/4a$, where a is the effective contact radius. Hence, by minimizing the contact resistance R_c under proper experimental conditions, the resistance maps collected by SSRM provide information on the 2D resistivity distribution in the semiconductor.

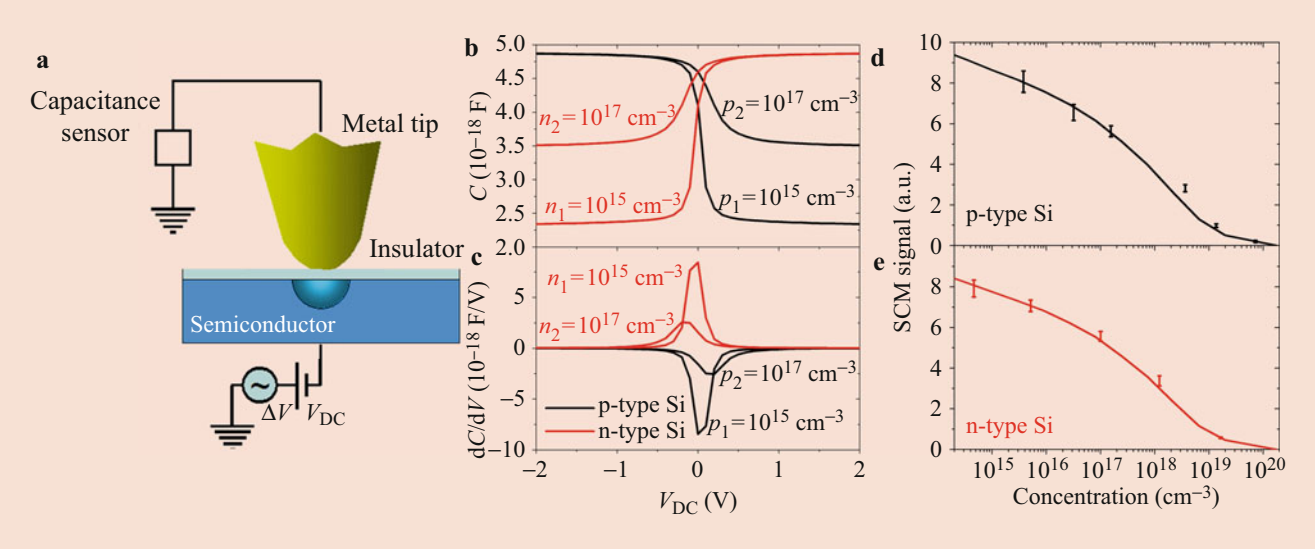


Fig. 4.37 (**a**) Schematic illustration of the scanning capacitance microscopy (SCM) setup.(**b**) Calculated capacitance and (**c**) derivative d*C*/d*V* versus tip bias curves for p-type and n-type silicon. Panels (**d**) and (**e**), show the SCM signal versus carrier concentration calibration curves for p-type (**d**) and n-type (**e**) silicon. (Adapted with permission from Giannazzo et al. [104], Copyright American Vacuum Society 2004)

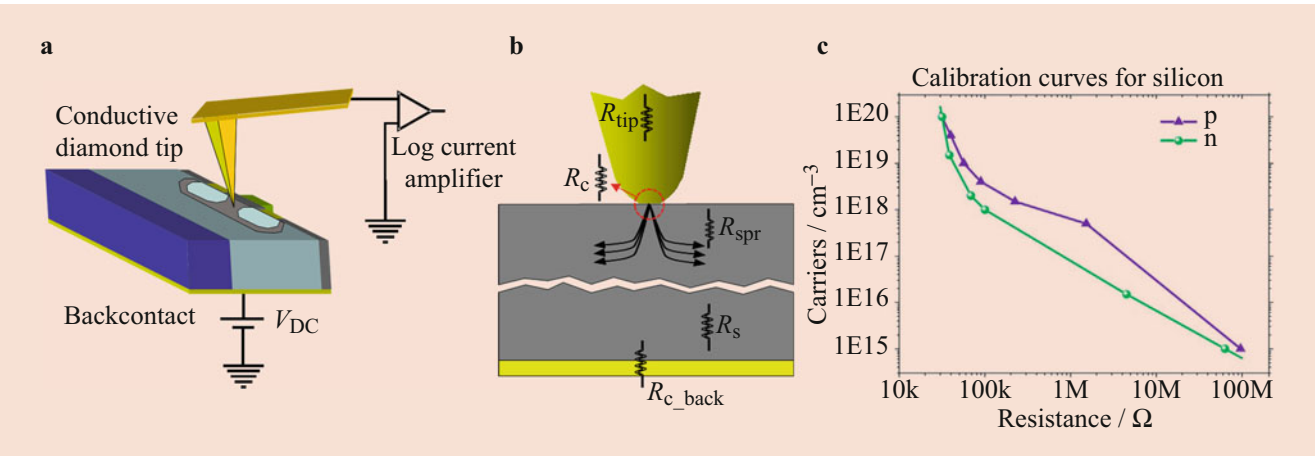


Fig. 4.38 Schematic illustrations of the scanning spreading resistance microscopy experimental setup (**a**) and of the resistance contributions to the measured resistance (**b**). (**c**) Typical calibration curves relating to carrier concentration and measured resistance for p- and n-type doped silicon. (Reproduced with permission from Vandervorst et al. [99], Copyright Elsevier 2017)

In the case of silicon, the R_c contribution is found to be strongly reduced by applying a high force (in the order of μN, corresponding to a GPa pressure) with the conductive AFM tip, as a result of a local temporary phase transformation of the silicon material from the diamond cubic structure to the β-tin metallic phase [111]. The dimension of this locally modified conductive region underneath the tip corresponds to the effective contact radius a, typically in the order of nanometers, thus resulting in a very high lateral resolution of the SSRM technique [99]. As the SSRM raw data are related to the local resistivity ρ, the quantification of the carrier distribution in the semiconductor requires the knowledge of the mobility dependence on the doping concentration.

This issue is typically addressed by using proper calibration samples, consisting of a set of epitaxial layers with known resistivity and doping concentration both for n- and p-type doped semiconductors [113]. Figure 4.38c shows two representative calibration curves, correlating the carrier concentration with measured resistance for p- and n-type doped Si, which evidences the wide sensitivity range (from $\sim 10^{15}$ to $\sim 10^{20}$ cm^{-3}) of the SSRM technique.

4.5.2 Applications of the Methods and Examples

The SCM technique has been widely used for 2D mapping of carrier distribution in silicon devices [112], in order to evaluate critical dimensions, such as the effective channel length of MOSFETs [106] or the effective base thickness in bipolar transistors [113]. Furthermore, it is extremely useful for investigating physical phenomena related to electrical activation and 2D diffusion of dopant species, such as boron, implanted in silicon at ultralow energy and in laterally confined windows [114, 115]. Besides silicon, SCM has been applied to other semiconductor materials, including Si_xGe_{1-x} quantum wells [116], and wide-band-gap semiconductors, such as SiC [117, 118], GaN [119], and AlGaN/GaN heterostructures [120].

As an example, Fig. 4.39 shows a schematic cross-section of a 4H-SiC power MOSFET (a) and the SCM map of the device active area (b). This image provides information on critical device parameters, such as the 2D carrier distribution of the p-doped body and n^+-doped source (obtained by Al and P ion implantation respectively) and the effective channel length. Such results are important, both as a feedback on the process conditions and input for TCAD simulations of the electrical characteristics of the device.

Scanning capacitance microscopy has also been employed on GaN to obtain nanoscale resolved information on the electrical behavior of typical defects (threading dislocations) of epitaxial GaN and their impact on Schottky diodes fabricated from this material [121].

Figure 4.40 shows an example of application to an AlGaN/GaN heterostructure, subjected to a selective area oxidation process at a temperature of 900 °C, which was demonstrated to result in a local suppression of the two dimensional electron gas (2DEG) at the AlGaN/GaN interface [120]. Figure 4.40a schematically illustrates the heterostructures with a partially oxidized and non-oxidized near surface region, whereas Fig. 4.40b reports a cross-sectional TEM analysis showing the thickness of the surface oxide. Finally, Fig. 4.40c, d show a cross-sectional SCM analysis comprising the non-oxidized and oxidized regions and two representative line-scans of the dC/dV signal in the two areas respectively.

As can be seen, in the non-oxidized region, the insulating GaN substrate, the n^+-GaN, the AlGaN barrier layer, and the 2DEG at the AlGaN/GaN heterointerface can be clearly identified. On the other hand, in the oxidized region, no difference exists between the insulating GaN substrate and the entire thickness of the heterostructure. This latter indicates that not only was the 2DEG suppressed but the GaN and AlGaN regions, including the highly doped n^+-GaN layer were also depleted. The high-temperature annealing of the uncapped surface during oxidation led to local compositional changes in the underlying layers, plausibly related to the Al and Ga losses associated with the formation of the oxide. Furthermore, owing to the high thermal budget, a relaxation of the AlGaN/GaN heterostructure can also occur, thus leading to the degradation or to the local suppression of the 2DEG.

Thanks to its high spatial resolution and wide dynamic range, SSRM has been used extensively to study doping technologies and active dopant distributions in planar transistor structures. A representative 2D resistance map obtained on a planar p-MOSFET structure is shown in Fig. 4.41, where the various regions (source/drain, extension regions, halo implants), as well as the gate electrode, are clearly visible [122].

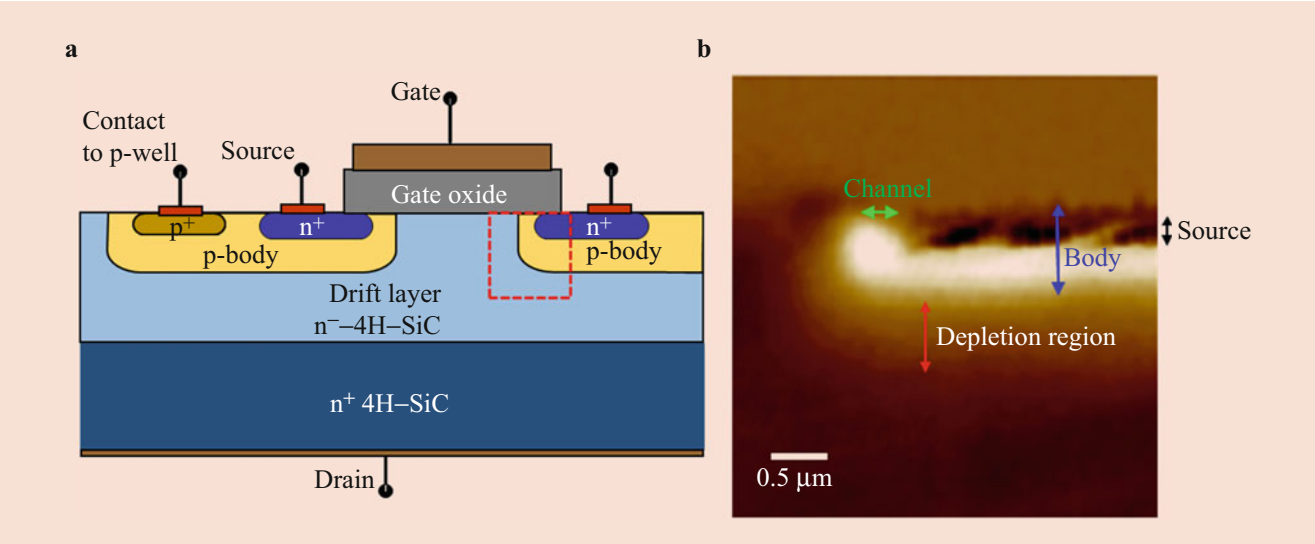


Fig. 4.39 (**a**) Schematic cross-section of a 4H-SiC power metal–oxide–semiconductor field-effect transistor and (**b**) scanning capacitance microscopy map of the channel region

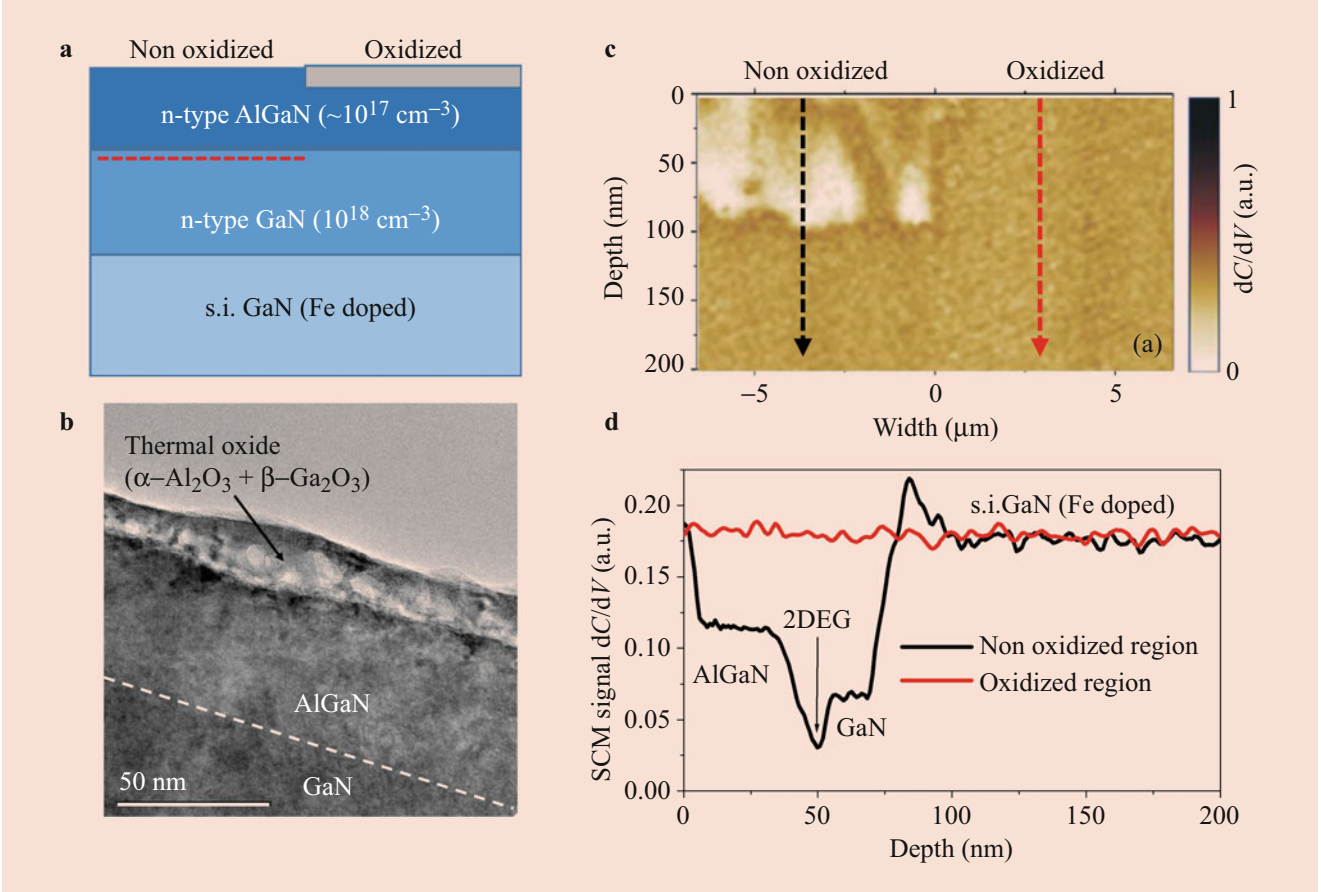


Fig. 4.40 (**a**) Schematic illustration of an AlGaN/GaN heterostructure subjected to selective area thermal oxidation at a temperature of 900 °C. (**b**) Cross-sectional transmission electron microscopy analyses of the heterostructure, showing the thin oxidized region (consisting of a mixed α-Al_2O_3/β-Ga_2O_3 phase) at the AlGaN surface. (**c**) Cross-sectional scanning capacitance microscopy analysis and (**d**) representative line profiles in the non-oxidized and selectively oxidized regions. (Figures adapted with permission from Roccaforte et al. [120], Copyright American Institute of Physics 2009)

Starting from its first demonstration in 1994 [123], SSRM has been continuously refined for applications in the measurement of ultra-scaled silicon devices [99]. Currently, one of the major limitations of conventional SSRM when applied to modern ultrascaled devices is its loss of sensitivity, especially at high carrier concentrations. This is because in 3D device architectures or in nanowire based devices, the nonlocal series resistance contributions of R_B and R_{bc} in Eq. (4.41) are not negligible with respect to the local R_{spr} contribution. To overcome such a limitation, a novel variant of SSRM, namely, fast Fourier transform-SSRM (FFT-SSSRM) has been recently introduced [124]. FFT-SSRM is capable of isolating the actual R_{spr} from all the nonlocal resistance components by modulating the load-force on the tip at a given frequency (thus effectively increasing and decreasing the radius of the tip/semiconductor nano-contact) and measuring the current at that frequency with a lock-in technique.

In order to reconstruct the 3D carrier distribution in complex device structures (such as FinFETs), a new approach with SSRM has been demonstrated, named scalpel-SSRM. This is a 3D tomographic technique based on a slice-and-view approach whereby the conductive diamond tip is used to perform subsequent SSRM maps and to remove Si material in a controlled way after each scan [125].

The SSRM technique has been initially developed and thoroughly assessed on silicon. However, it extends its application to other semiconductors, including Ge [126], III–V semiconductors (InP, GaAs) [127], ZnO [128], and SiC [129, 130]. In the case of Ge, the properties of the tip/semiconductor nano-contact have been modeled, and, similar to the case of Si, the formation of a β-tin metallic phase under high pressure has been identified. On the other hand, no detailed investigation on the nature of the nano-contact is available in the case of compound semiconductors, and the applicability of SSRM to these material systems mostly relies on empirical calibration curves determined on calibration samples.

Owing to their different physical working principles, the SCM and SSRM techniques provide information on the active dopant concentration and on the resistivity profiles

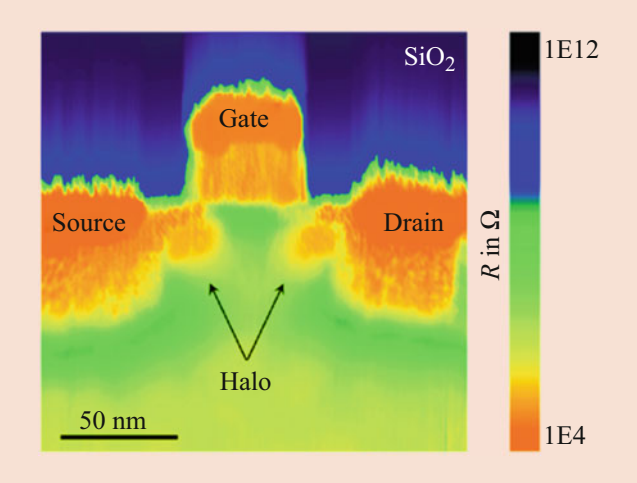


Fig. 4.41 Two-dimensional spreading resistance map obtained on a planar MOSFET structure. The differently doped regions (S/D, extension regions, halo implants) as well as the gate electrode are clearly visible. (Image reprinted with permission from Schulze et al. [122], Copyright Springer Nature AG 2019)

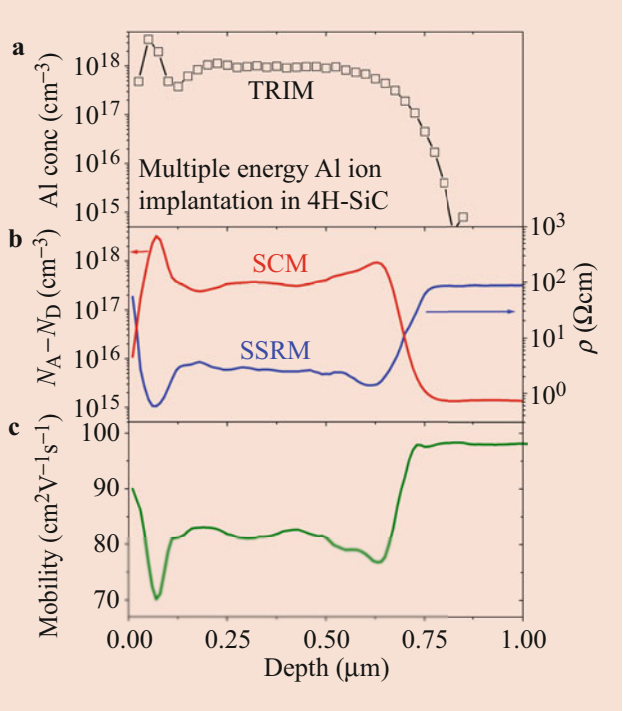


Fig. 4.42 (**a**) Simulated Al concentration profile in 4H-SiC implanted with multiple energy (40–550 keV) Al^+ ions at a dose of 1×10^{13} cm^{-2}. (**b**) Net doping concentration profile ($N_A - N_D$) from the SCM data (left scale) and resistivity profile ρ from the scanning spreading resistance microscopy data (right scale) acquired on the sample annealed at 1650 °C for 30 min. (**c**) Mobility profiles evaluated from the combination of the net doping concentration and resistivity profiles. (Figures adapted with permission from Giannazzo et al. [130], Copyright American Institute of Physics 2007)

respectively. Hence, the combined application of the two methods allows, in principle, the carrier mobility to be locally evaluated in semiconductors with inhomogeneous doping or defects concentration. This approach was employed in the case of silicon carbide (4H-SiC) implanted with multiple energy Al ions and subjected to annealing at 1650 °C [130]. Figure 4.42a shows the Al concentration depth profile, calculated by Monte Carlo simulations with the TRIM (transport of ions in matter) code. Figure 4.42b, left axis, reports the net active dopant concentration $N_A - N_D$ (with N_A the acceptors concentration and N_D the donor compensation, owing to electrically active defects) obtained by calibrated SCM analyses, whereas the resistivity (ρ) profile extracted by SSRM data is shown in Fig. 4.42b, right axis. Finally, Fig. 4.42c shows the depth resolved mobility, evaluated by a combination of the two experimental profiles in Fig. 4.42b, using the neutrality equation correlating $N_A - N_D$ with the hole concentration p and the well-known relation $\mu = 1/(qp\rho)$ between mobility, resistivity, and carrier concentration.

So far, applications of scanning probe microscopies to 2D electrical profiling in bulk semiconductors have been discussed. Obviously, thanks to their high spatial resolution and genuine surface sensitivity, these techniques are the methods of choice in low-dimensional materials, including quantum dots (0D), nanowires and nanotubes (1D), and 2D materials. In particular, SCM and CAFM have been extensively applied in recent years to explore carrier transport phenomena in graphene, semiconducting transition metal dichalcogenides, insulating hexagonal boron nitride, as well as their heterostructures [131, 132].

4.6 Optical Characterization of Semiconductors

The use of light is a powerful tool for material characterization because of its simplicity and because it needs no sample preparation. Of the techniques available, even the simplest one, i.e., the measurement of light intensity reflected and/or transmitted by a sample, provides essential information both for materials characterization and for process control. In what follows, we will provide the basics of the technique and a few illustrative examples concerning the determination of the band gap, and of the energy levels of defects, impurities, and dopant atoms.

4.6.1 Basic Concepts

The interaction of a plane wave with a sharp and flat boundary between two media with a different refractive index n_0 and n_1 can be understood by solving the Maxwell equations with the boundary conditions of continuity of the field at

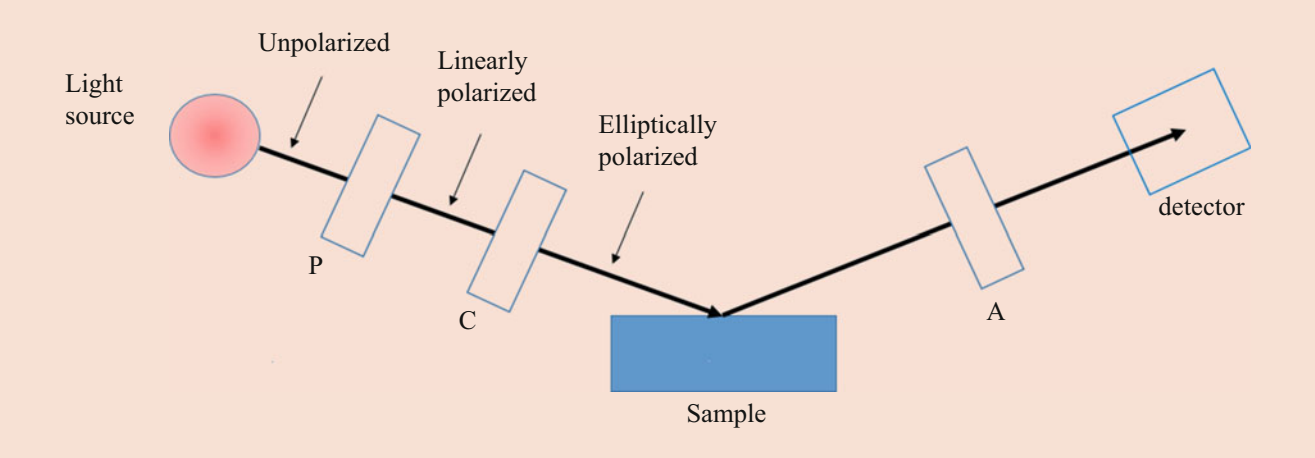


Fig. 4.43 Schematic arrangement of an ellipsometer apparatus

the interface [133]. This procedure gives the ratio of the amplitudes of the reflected and transmitted electric fields for the two components of the polarization vector, the so-called Fresnel coefficients. Keeping in mind that in general the refractive index is a complex quantity, the intensities will be given by the squared modulus of the respective coefficients.

In real life the second medium is not semi-infinite and the presence of (at least) a second interface gives rise to multiple reflections inside the sample. At a normal angle of incidence the Fresnel coefficients for the two polarizations are equal and if the coherence length of the light source is smaller than the sample thickness, interference effects are averaged out and the reflectance and transmittance can be approximated by

$$R = \frac{(n_0 - n_1)^2 + k_1^2}{(n_0 + n_1)^2 + k_1^2}; \qquad T = \frac{(1-R)^2 \mathrm{e}^{-\alpha d}}{1 - R^2 \mathrm{e}^{-2\alpha d}}, \tag{4.42}$$

where $\alpha = 4\pi k/\lambda$ is the absorption coefficient and k is the imaginary part of the complex index of refraction $\tilde{n} = n - ik$. It is also assumed that the measurements are taken in a transparent medium ($k_0 = 0$), as is usually the case. For thin films, interference effects give rise to characteristic oscillatory behavior that must be taken into account [134].

In principle, the simple R and T measurements allow the determination of the refraction index, which is in turn related to the material properties. This is true only when the substrate is transparent and hence the measurement of T is possible. For absorbing substrates, it is possible to use the Kramers–Kronig relations [133], but suitable extrapolations outside the measured wavelength range are required.

The Fresnel coefficients, either of a single surface or of a layered structure, are in general complex numbers. As a consequence, there will be a phase shift between the two polarization directions and then a change in the polarization state of the reflected light. This is the field of ellipsometry.

To work with polarization, it is important to control both the incident and the reflected state of polarization. In a typical setup, the light source is unpolarized and is followed by a polarizer and a compensator to control the polarization before the probed sample. After reflection, there is another polarizer that works as an analyzer of the state of polarization and then a detector. A schematic drawing is shown in Fig. 4.43. The incident and the reflected beam define the incidence plane.

In ellipsometry, it is customary to express the complex ratio of r_p and r_s as:

$$\rho = \frac{r_\mathrm{p}}{r_\mathrm{s}} = \tan \Psi \mathrm{e}^{i\Delta}, \tag{4.43}$$

where r_p and r_s are the Fresnel coefficients for p and s polarizations respectively (light that is polarized parallel to the incidence plane is named p-polarized, whereas light polarized in the perpendicular direction is called s-polarized) [133], and Ψ and Δ are called ellipsometric angles.

In modern instruments the optical elements, P or C or A, can be rotated continuously, and then the modulated signal is analyzed. For example, it is possible to show [135] that in the case of a rotating analyzer the light intensity at the detector is given by:

$$\frac{I}{I_0} = 1 + a \cdot \cos\left[2A(t)\right] + b \cdot \sin\left[2A(t)\right], \tag{4.44}$$

where $A(t)$ is the time-dependent angle of the analyzer and α and β are coefficients related to Ψ and Δ. It is then clear that a simple Fourier analysis of the detector signal will immediately give the ellipsometric angles.

Ellipsometry is a powerful and very sensitive technique and allows the accurate determination of very thin layers at the nanometer scale. As an example, Fig. 4.44 shows the

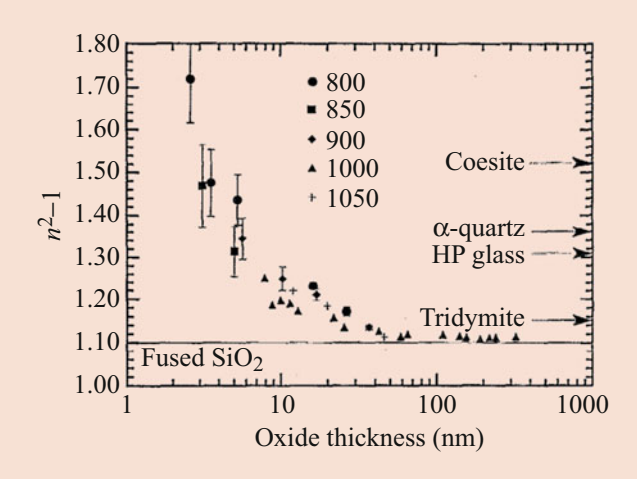


Fig. 4.44 Long wavelength limit of n^2–1 as a function of SiO_2 film thickness on silicon. (Reprinted from Jellison [136], with the permission of AIP Publishing)

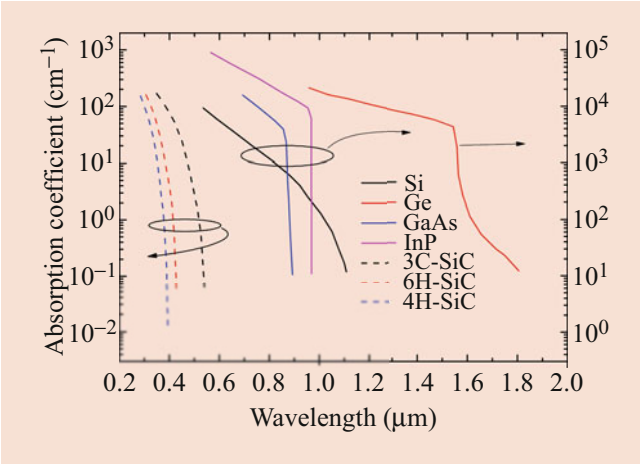


Fig. 4.45 Absorption coefficient of several semiconductors as a function of wavelength

dependence of the long wavelength limit of the quantity, n^2–1, of SiO_2 films on silicon as a function of layer thickness down to 2 nm [136].

4.6.2 Determination of the Optical Gap

Although the theoretical definition of the optical gap is clear, its accurate experimental determination is not straightforward. Indeed, even in an ideally defect- and impurity-free semiconductor, several factors influence the absorption coefficient α near the absorption edge, thus making it difficult to determine where α would go to zero. Just to name the two most important effects, near the absorption edge there are excitonic influences [137] and the presence of an exponential decay called the Urbach tail [138]. In practice, then, one has to model the response within a limited range of energy above the absorption edge and extrapolate it to $\alpha = 0$ [139].

It can be shown [137] that for a direct transition (same crystalline momentum value for the initial and final states in the valence and conduction bands respectively) in crystals α^2 is linear with energy, i.e., $\alpha^2 \propto (E - E_g)$, where E_g is the energy gap. Similarly, for indirect transitions (different crystalline momentum between the initial and the final state), the relation between α and E is $\alpha^{1/2} \propto (E - E_g)$. Extrapolation of these linear relations directly gives E_g. Figure 4.45 shows the absorption coefficient of several direct and indirect gap semiconductors to highlight the different energy dependence. For SiC, three different polytypes are considered.

This method is widely used and accurate enough to determine, for example, the narrowing of the band gap due to doping [140] or dependence on composition [141] or on external parameters [142].

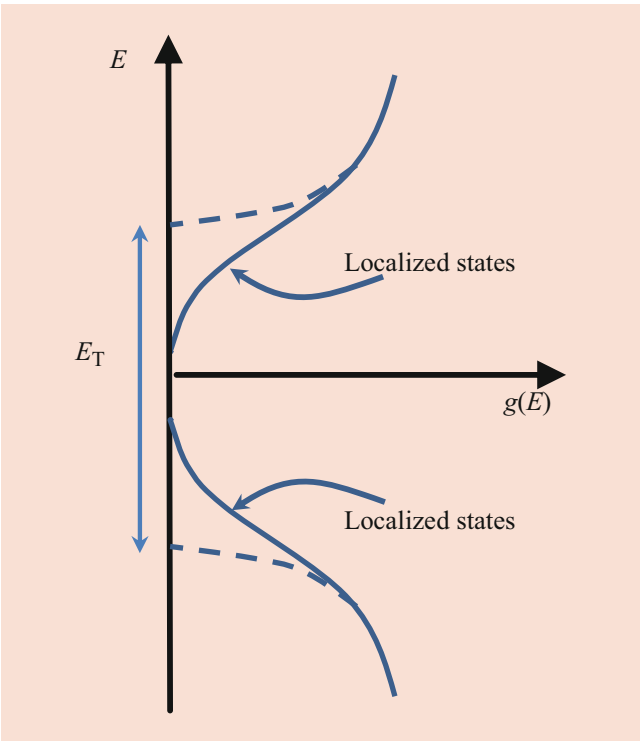


Fig. 4.46 Density of states in amorphous solids

The situations are different for amorphous semiconductors and glasses. It has been long recognized that structural disorder leads to the presence of long tails of localized electronic states, both below the conduction band and above the valence band [143]. The density of states can then be described as being composed of a parabolic part of an extended state followed by an exponential tail of localized states, as schematically represented in Fig. 4.46.

The presence of these tail states makes it impossible to have a univocal definition of the band gap. Following the

initial suggestion of Tauc et al. [144], it is customary to quote the so-called Tauc gap E_T as the energy difference between the extrapolation to zero density of states of the parabolic part of the conduction and valence band. As these states are extended [144], the absorption coefficient depends on energy as:

$$\sqrt{\alpha E} \propto (E - E_T)\,. \tag{4.45}$$

At energies below the gap, though, there is still significant absorption corresponding to optical transitions between localized states in one band and extended states in the other. These transitions give rise to an exponential tail in the absorption coefficient called the Urbach tail [138]. The origin of this tail has been much debated in the literature. As the tail is also present in crystals, it has been identified as being due to thermal disorder in a way similar to the Debye–Waller factor. In amorphous structures, topological disorder adds to the thermal effect and is treated similarly [145]. The width E_u of the exponential tail is then expressed as the sum of two terms in the average square displacement U, one due to temperature T and the other due to disorder X:

$$E_u\,(T, X) = K\left[\langle U^2\rangle_T + \langle U^2\rangle_X\right]. \tag{4.46}$$

Using the simple Einstein oscillator model for the temperature-dependent term, the above expression can be written as [146]:

$$E_u\,(T, X) = \frac{K\Theta}{\sigma_o}\cdot\left[\frac{1+X}{2} + \frac{N}{\exp\left(\Theta/T\right) - 1}\right], \tag{4.47}$$

where $\Theta = 3/4\ \Theta_D$ with Θ_D Debye temperature, σ an Urbach edge parameter, X a parameter related to $\langle U^2\rangle_T$, and N a parameter related to a possibly partial phonon occupancy. It is worth noticing that both the energy gap E_T and the Urbach width E_u share a dependence on temperature and disorder [145] and then are both useful for the characterization of amorphous semiconductors and oxides [147].

4.6.3 Dispersion Relations

The availability of spectroscopic instruments is of great help for optical characterization. Indeed, if suitable dispersion relations are available, the entire wavelength range dependence can be fitted with a few parameters. This procedure has proven successful and is now widely used.

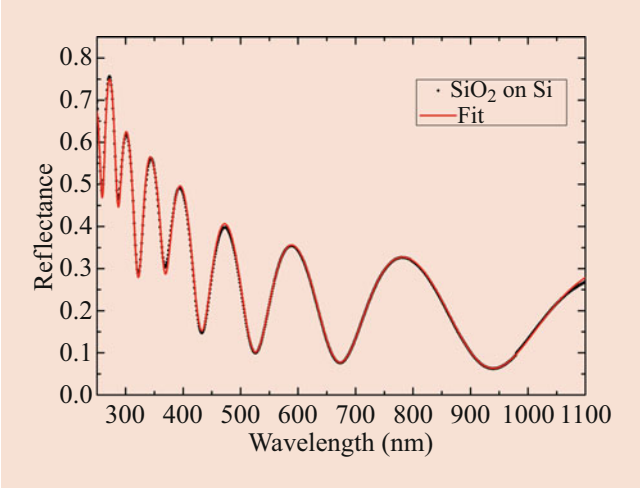


Fig. 4.47 Reflectance of an 800-nm-thick SiO_2 film on Si versus wavelength

For transparent layers grown on a known substrate, several dispersion relations have been proposed, the most widely used being the Cauchy [148] and the Sellmeier [149] relations. These empirical dispersion relations proved to be relatively accurate in describing the behavior of the index of refraction as a function of wavelength and then useful for the straightforward measurements of both the refractive index and the thickness of thin films. As an example, Fig. 4.47 reports the reflectance of a nominally 800-nm SiO_2 layer on silicon and the resulting fit using the Cauchy relation.

Based on more solid physical ground is the well-known Lorentz model that includes the so-called anomalous dispersion region and absorption. It can be derived from the classical response of a bound charge that behaves as a damped harmonic oscillator to the incoming electromagnetic wave [150]; the quantum-mechanical treatment gives basically the same result. In this model, the expression for the dielectric function is:

$$\epsilon = \epsilon_\infty + \frac{4\pi N q^2/m}{\left(\omega_o^2 - \omega^2\right) - i\Gamma\omega}, \tag{4.48}$$

where N is the number of oscillators, q the charge, m the mass, ω_o the resonance frequency, and Γ the damping constant of the oscillator. It is worth noticing that the Drude model for metals can be derived directly from the Lorenz model by putting $\omega_o = 0$, i.e., no restoring force. As the dielectric function is a linear response function, contributions from other oscillators simply add up.

This model can be applied to lattice vibrations in polar semiconductors [150]. Reflectivity measurements within the infrared range show the presence of the so-called Rest-

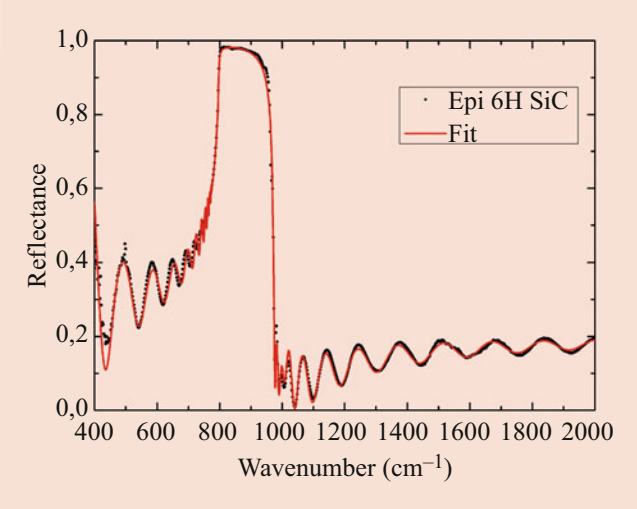


Fig. 4.48 Reflectance of a 10-μm intrinsic homoepitaxial 6H-SiC grown on a heavily doped substrate versus wavelength

strahlen band [151], a band of high reflectivity between the transverse (TO) and longitudinal (LO) optical phonon frequencies near the center of the Brillouin zone. The shape of the curve depends on Γ, which in turn depends on crystal quality. For example, it has been successfully applied to monitor ion implantation damage and recovery in 4H-SiC [152].

If the semiconductor is doped, a Drude-like term is added to the dielectric constant to account for the contribution of free electrons. The change in ε, due to doping, allows the measurement of the thickness of a low doped epitaxial layer on a highly doped ($N \sim 10^{19}$ cm^{-3}) substrate, as shown in Fig. 4.48 for a 10-μm low doped ($N < 10^{14}$ cm^{-3}) 6H-SiC epitaxial layer.

The absence of a charge in nonpolar semiconductors makes them unresponsive within the infrared range and only multiphonons [153] or impurity-related [154] processes are detected. Still, whatever the semiconductor type, in the presence of doping, the response of free electrons is clearly measurable [151, 155]. It is worth noticing that the parameter Γ, the inverse of a characteristic electron scattering time, is dependent on dopant concentration [155].

The simple harmonic oscillator model can also be used as a simplified model for interband absorption. The imaginary part of the dielectric function is related to the sum of all possible transitions from the valence to the conduction band separated by energy E_{CV}. This factor is called the joint density of states, which is given by [137].

$$D\left(E_{CV}\right) = \frac{1}{4\pi^3} \int \frac{\mathrm{d}S_k}{\left|\nabla_k \left(E_{CV}\right)\right|}, \tag{4.49}$$

where S_k is a constant energy surface. Singularities, called Van Hove singularities, are present at energies where $|\nabla_k(E_{CV})|$ is zero. Calculating the dielectric function in this formally correct way is somewhat cumbersome. In any case, absorption above the band gap is dominated by these transitions and then it should be possible to express the dielectric function as a sum of contributions from the known critical points. This has proven to be a useful approximation, even though it is not possible to assign each oscillator derived from the fits to a specific critical point [156, 157].

Whichever the adopted model, absorption at the critical points is sensitive to both doping and defects. It has been shown that in doped germanium absorption at the critical points depends both on doping level and dopant species [158]. Also, the residual damage after ion implantation can be followed through the continuous change in the dielectric function [159].

The Lorentz model works reasonably well at energy well above the band gap, but it cannot reproduce the behavior near it. Indeed, the absorption coefficient goes to zero aymptotically at low energies and not at the energy of the gap as expected, thus precluding its direct determination from the model.

4.6.4 Impurities and Defects Absorption

Imperfections in crystals due to the presence of impurities and/or crystallographic defects typically give rise to electronic states inside the energy gap and possibly to local vibrational modes (LVM). Both can be detected by optical absorption. The energy of the former depends on the characteristic of the defect and on the gap and may be within the visible or the infrared range; the latter, instead, always fall within the infrared range. In any case, always being at energies lower than the energy gap, they fall within the region of transparency of the semiconductor and are then accessible to transmission measurement. Being a vast topic, in what follows we will give just a few examples to highlight the capabilities of the technique, more details can be found in specialized books (see, for example, Pajot and Clerjaud [160]).

Carbon and oxygen are the two most abundant unintentional impurities in silicon single crystals. Carbon atoms are present both in interstitial Ci and in substitutional position Cs. Although Cs can be detected by infrared absorption owing to an infrared active local vibrational mode (LVM) at a frequency of 1107 cm^{-1} [161], no bands related to Ci have been univocally identified. On the contrary, oxygen atoms give rise to absorption bands both in substitutional Os and interstitial Oi positions around 510 cm^{-1} and 1100 cm^{-1} respectively.

These two impurities can be present in Czochralski-grown silicon at relatively high concentrations of the order of 10^{17} cm^{-3} for carbon and 10^{18} cm^{-3} for oxygen. After irradiation, they form CiOi complexes with several characteristic absorption bands between 529 cm^{-1} and 1116 cm^{-1} [162]. The CiOi complex has been found to efficiently trap self-interstitial silicon, which has its own LVMs at 936 cm^{-1} to 1020 cm^{-1} at room temperature [163].

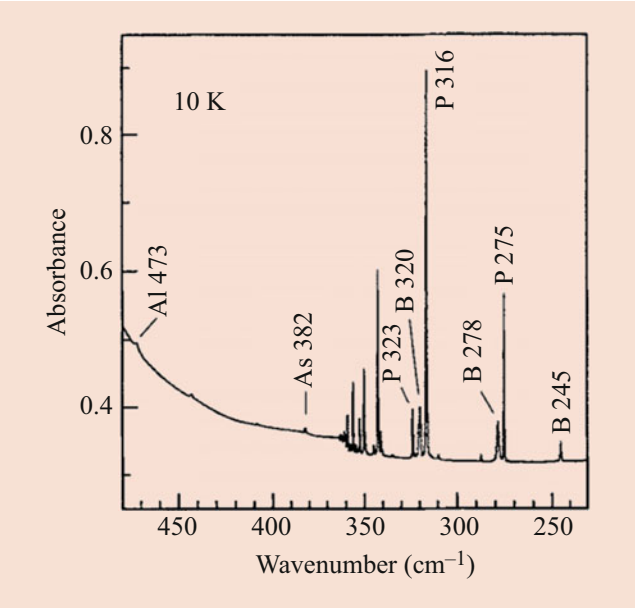


Fig. 4.49 Absorbance of As, P, and B impurities in silicon. (Reprinted from Alt et al. [162], with the permission of AIP Publishing)

Electron or hole transitions from a defect or dopant energy level to the nearest band can also be detected by optical absorption. The corresponding electronic structure can then be assessed and the concentration determined upon calibration from the integrated absorption of a band. If the level is relatively near the band, low temperature measurements may be required to increase the occupancy factor. In Fig. 4.49 we show an absorption spectrum in a single crystal of silicon containing B, As, and P impurities [162].

The integrated absorption of a specific band is linked to the number of oscillators by a well-known sum rule [151], and it is possible to calculate the latter from the former. In practice, though, the oscillator strength is typically poorly known and one has to resort to a calibration procedure. In this way, it has been possible to accurately measure the concentration of several shallow dopants in silicon down to 10^{10} cm^{-3} [162], as shown in Fig. 4.50 for boron and phosphorous.

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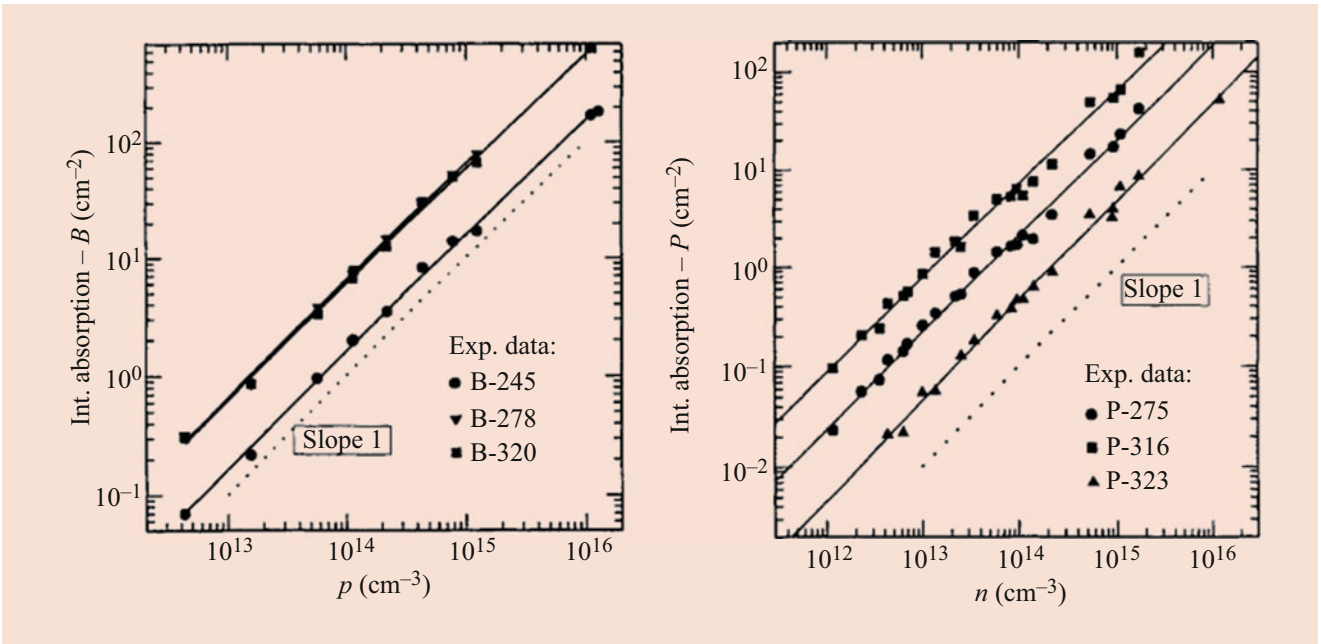

Fig. 4.50 Integrated absorption of impurity bands in silicon versus dopant concentration. (Reprinted from Alt et al. [162], with the permission of AIP Publishing)

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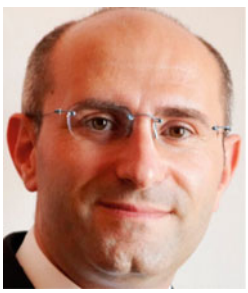

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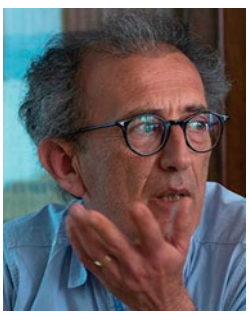

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Interconnect Processing: Integration, Dielectrics, Metals

5

Shyng-Tsong Chen, Nicholas A. Lanzillo, Son Van Nguyen, Takeshi Nogami, and Andrew H. Simon

Contents

5.1 BEOL Integration and Performance . . . 170
5.1.1 Copper Interconnect Single Damascene Scheme . . . 170
5.1.2 Additional Material Films Used in the Damascene Process Flow . . . 172
5.1.3 Via-First Dual Damascene Integration Scheme . . . 173
5.1.4 Trench-First Dual Damascene Integration Process Flow . . . 173
5.1.5 Single Patterning Versus Double Patterning . . . 173
5.1.6 Trench-First Pitch-Split Double Line Patterning with Self-Aligned Via Integration Scheme . . . 174
5.1.7 Self-Aligned Double Patterning (SADP) . . . 175
5.1.8 2D Versus 1D Self-Aligned Double Patterning (SADP) . . . 177
5.1.9 Future Outlook: EUV Single and Double Patterning . . . 179
5.1.10 BEOL Performance . . . 180

5.2 BEOL Dielectric Films . . . 180
5.2.1 Fabrication of BEOL Low-*k* Dielectric Films . . . 182
5.2.2 Low-*k* and Ultralow-*k* Porous pSiCOH ILD Dielectrics . . . 182
5.2.3 Advanced Dielectrics and Processes for Metal Interconnect . . . 187
5.2.4 Summary . . . 191

5.3 BEOL Thin-Film Metals . . . 192
5.3.1 Requirements for Barrier, Liner, and Seed Layers . . . 192
5.3.2 Sputter Deposition Tooling for Barrier, Liner, and Seed Layers . . . 193
5.3.3 Barrier/Liner/Seed Process Sequences and Enhancements . . . 197

5.4 Dielectric Cap Deposition and Interconnect Capacitance . . . 204
5.4.1 SiN and SiCNH Caps . . . 205
5.4.2 Advanced Caps with Reduced *k* and/or Reduced Thickness . . . 206
5.4.3 Integration of Advanced Selective Cobalt/Dielectric Cap . . . 211

5.5 Summary . . . 211

References . . . 211

Abstract

This chapter covers integration, performance, and three main process sectors concerning back-end-of-line (BEOL) wiring ("interconnect") process technology: intralevel dielectrics (ILDs), thin-film metals used in thin-film processing, and dielectric capping layers. The integration section contains an overview of patterning schemes used in damascene wiring fabrication and covers developments up to current leading-edge schemes which use extreme ultraviolet (EUV) lithography. Performance considerations are also discussed in Sect. 5.1, with a focus on BEOL metrics such as resistance and capacitance. The dielectric section reviews the history of materials used as BEOL damascene dielectrics and covers the history of low-dielectric constant ("low-*k*") materials as well as recent trends concerning air gap and porous dielectrics. The thin-film metals cover developments in physical vapor deposition (PVD) tooling and processes as well as chemical vapor deposition (CVD) wetting and cap layers. In the final section, modern trends in dielectric and selective metal caps are covered.

Keywords

Interconnects · Wiring · Back-end-of-line (BEOL) · Dielectrics · Metals · Damascene · Copper · Electromigration · Time-dependent dielectric breakdown (TDDB) · Low-*k*

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5.1 BEOL Integration and Performance

Back-end-of-line (BEOL) integration is a building process to wire the active transistor devices on the wafer to form functional electronic circuits. Figure 5.1a, b show 3D cross-sectional views of a complete BEOL build. Shown in the picture are multiple levels of copper line wiring with top aluminum level for terminal connections. "1× Cu" symbols marked in the image are the bottom Cu wires with minimum pitch built right on top of the FEOL devices. "2× Cu" symbols mark 2× pitch fat wires. Top level Cu wiring levels also called FBEOL (Far-BEOL) levels can have up to 25× or even 40× pitch wires depending on the complexity of the chip design. The total number of wiring levels also depends on the nature of the chip design. A CPU chip often has more levels than a chip only for a specific task. It is also possible to have memory devices as well as other types of devices integrated into BEOL levels, which will have separate process flows in addition to the wiring process flow. The standard wiring process flow may need to be modified to accommodate the embedded memory process. This chapter will only cover the basic wiring part without other embedded devices.

Figure 5.1b shows the multilevel copper wires in the build as well as the tungsten wire (gray color) underneath with dielectric material removed.

The process flow for building this structure is called "damascene" which is an ancient Jewelry-making process for fabricating an embedded pattern inside a host material.

BEOL damascene process was developed in the 1990s and is used when there is a need to planarize the wafer surface for finer pitch patterning. The CMP (Chemical-Mechanical Polishing) process for damascene integration scheme was invented first for the chip with aluminum wires and tungsten stud (via). Single damascene scheme was used at via levels with metal etch to pattern the aluminum line levels.

To reduce the metal line resistance, copper fabrication processes were developed to replace aluminum wire with copper wire. The dual damascene process to pattern the line and via together, using copper as the conductor, was also developed at the same time and soon became the industry standard. These methods for fabricating the wire and via together are also referred to as "dual inlaid" by some authors.

The following sections describe the basics of copper damascene processes used in microelectronic industry for BEOL interconnection integration. The detailed material stack and process flow used in actual chip manufacture may be somewhat different, depending on the chip manufacturing company, but the general principles are the same.

5.1.1 Copper Interconnect Single Damascene Scheme

A simplified schematic diagram (shown below) is used to show the general concept with the basic steps of a copper single damascene integration scheme:

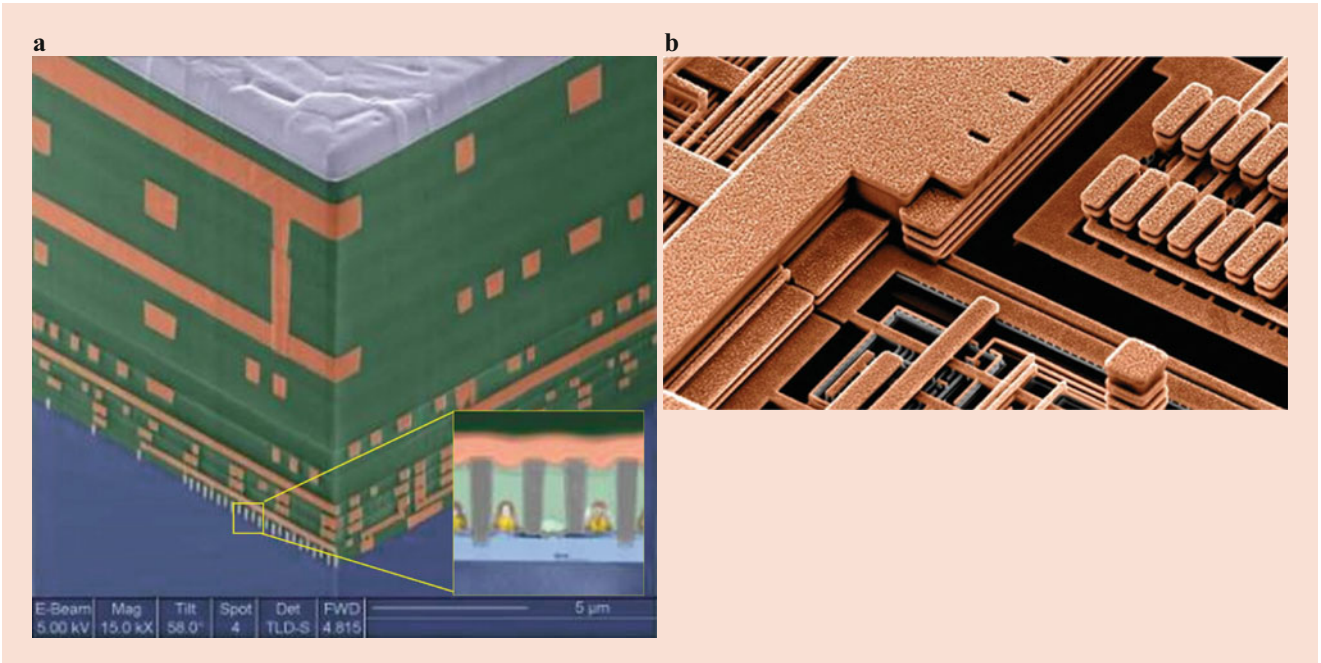

Fig. 5.1 (**a**) Focused ion beam (FIB) section of 90 nm logic chip illustrating multiple levels of Cu interconnects at multiple ground rules. The transistor structure is shown in the inset. (**b**) Dual damascene metal interconnects revealed by etching of the intralevel dielectric material. (Ref. [1], courtesy of Daniel C. Edelstein)

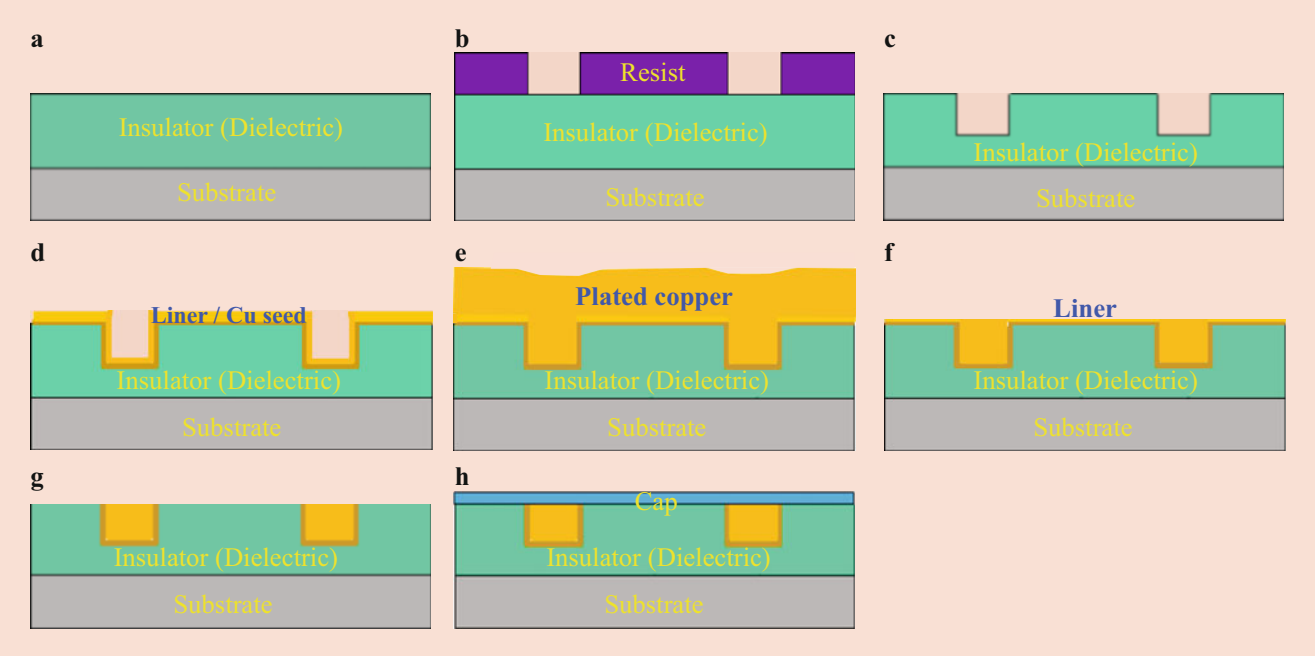

Fig. 5.2 (**a**–**h**) Schematic process sequence for single-damascene copper interconnects (see text)

Figure 5.2a depicts the dielectric stack deposition with thickness measurement. Additional etch hardmask material deposition may be needed on top of the dielectric stack; this will be addressed in later sections.

Figure 5.2b depicts the lithographic ("litho") process to print the pattern on the wafer. Additional material such as OPL (organic planarization layer) between the dielectric stack and resist may be needed to increase the etch budget as the resist thickness may not be enough to survive the targeted dielectric etch depth (see next section). Post-litho CD (critical dimension) measurement is needed for process control. This measurement usually shrinks the resist material, and re-measuring at the same spot will not provide the correct result. Typically, a specific CD measurement target is designed for CD control and usually placed across the chip to monitor CD uniformity.

Figure 5.2c illustrates the etch process used to create a recessed pattern in the dielectric, followed by a wet process to clean up the residues from the etch process. The post-etch wet clean process also removes the etch-damaged dielectric material. This will remove some sidewall material in the trench. The etch-damaged dielectric material usually has a higher dielectric constant compared with the pristine material. The effective dielectric constant of the dielectric material in the chip will be higher than the pristine material if the damaged dielectric material is not removed. As the result, the capacitance in the circuit will be higher, which will have a negative impact on the chip performance. However, the industry usually chooses not to remove most of the etch-damaged layer, as this may create a large undercut if there is a hardmask layer on top of the dielectric material for patterning purpose. The large undercut will make the metal filling into the trench more challenging. A post-etch pattern CD (critical dimension) measurement is needed, but it must always use a measurement location different from the litho CD measurement spot.

Figure 5.2d shows the deposition of the liner material. The liner material usually has two layers and acts as an adhesion layer and oxygen barrier layer. Typical materials used are Ta/TaN as the Ta/Cu interface provides a good adhesion while Ta does not mix with copper when the chip is operated at an elevated temperature, and the line resistance will not increase over the chip's lifespan. A thin copper seed layer on the liner material is needed for copper plating process. There is a requirement for minimum copper seed layer thickness as some copper may be dissolved in the copper plating bath during the initial phase of the copper plating process.

Figure 5.2e shows the fill of the damascene structures with electroplated copper. The plated copper thickness is typically much larger than the line trench depth to provide enough process window for the CMP process. A furnace anneal is used after plating to increase the copper grain size. This will reduce the line resistance and also improve the reliability.

Figure 5.2f illustrates the use of copper CMP to remove excessive copper and planarize the wafer surface. This part of the CMP process is usually designed to stop the polish on the liner layer with some overpolish, to make sure that no copper is left on the liner surface.

In Fig. 5.2g, liner CMP is used to remove liner and some dielectric material from the dielectric surface. Due to pattern-density variation across the chip, enough liner overpolish into dielectric material is needed to prevent the metal lines

from becoming electrically leaky or shorted. This step also removes etch-damaged dielectric top surface, if not protected by hardmask during the etch.

Following liner CMP, a defect inspection is performed (not illustrated). This process can be done post CMP or post cap (next step) when necessary. This is usually done after the cap layer deposition process if there is a queue time requirement which limits the time delay between the CMP and capping processes. Post CMP top of CD measurement can be done before capping.

Figure 5.2h shows the capping of the metal pattern. The cap serves as a copper and oxygen barrier. Typically, cap is a single dielectric layer with good barrier properties. SiN was used in early technologies and later changed to SiCN to reduce the interlevel capacitance. When the layer thickness scaled from generation to generation, it is often required to scale the cap thickness as well. When the traditional SiCN hits the thickness limitation as an effective barrier film, multiple layers of new materials may be used with thinner total thickness, still providing an effective barrier film. For very fine metal line patterning, a selective metal cap, such as Co (cobalt), may be deposited on the metal line top surface to improve the electromigration lifetime. This is common for 1× level, copper wiring post-14 nm technology. There is usually a queue time control to minimize the waiting time between CMP and cap process steps, especially for very fine Cu line fabrication in a porous low-*k* dielectric material. The queue time control is to prevent oxidation of the copper surface as well as moisture or other ambient contamination of the dielectric. The copper oxidation could also happen if the cap deposition chamber is not completely free of oxygen.

5.1.2 Additional Material Films Used in the Damascene Process Flow

As the technology evolves, it is usually necessary to add additional materials for the damascene integration scheme. Additional materials serve different purposes which will be explained in the following sections. This section will cover the most common additions.

Figure 5.3a shows the post-litho film stack. It is common to have a hardmask layer on top of the main dielectric layer, which will remain as an ILD (interlevel dielectric) after the build is done. It is common to use a metal hardmask ("MHM") on ILD, which is often needed for a trench-first integration scheme (see later sections). A typical metal hardmask material is TiN for good etch selectivity; it usually remains on the wafer after etch. It is also common to have additional thin dielectric hardmasks above and below the metal hardmask. The dielectric hardmask below the metal hardmask is often used to protect ILD material from processing damage during the metal hardmask deposition or during the etch process. The dielectric hardmask above the mask is usually used in the double patterning scheme (see later sections). As mentioned above, an additional OPL layer is used here to improve the etch budget, as resist alone may not survive the etch process to reach the targeted depth of the trench.

Figure 5.3b shows the post-RIE (etch) film stack. Typically, there will be some hardmask material left on the ILD material after etching. If the hardmask material is an insulator, it will be polished away during the CMP process. For the TiN metal hardmask, there is an option to remove it after etch using a wet clean process. For TiN hardmasks with better etch selectivity, the film mechanical stress is usually higher. This high stress could cause pattern deformation during the metal liner deposition process if the underlying dielectric material has low mechanical modulus; this has been observed with some ultralow-*k* materials. Also, there may be an ILD undercut below the metal hardmask when the etch-damaged ILD is removed by post-RIE, wet clean process. This can cause metal fill problems as it will be more difficult for the metal liner to cover the undercut area. In general, removing the metal hardmask before metallization can fix this metal fill problem.

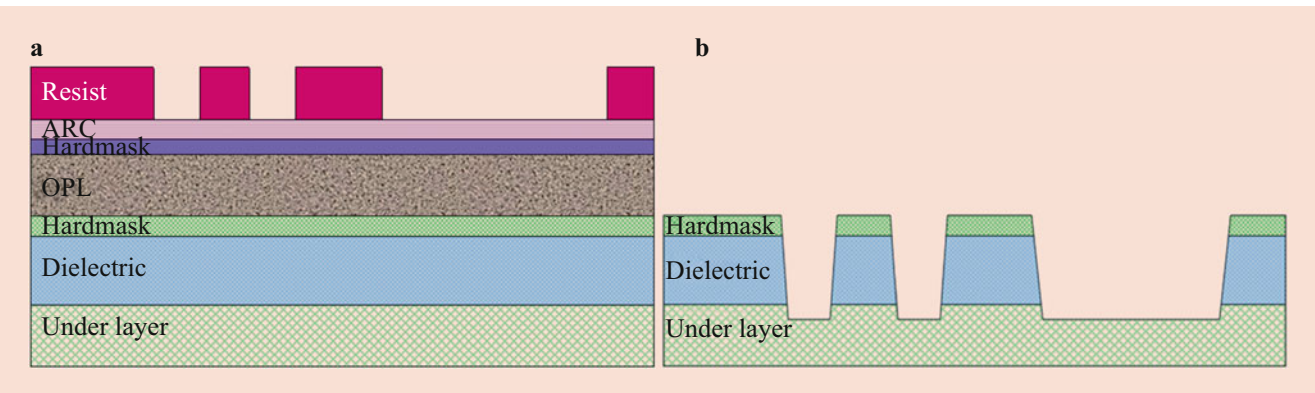

Fig. 5.3 (**a**, **b**) Damascene process sequence for metal hardmask (MHM) layer (see text)

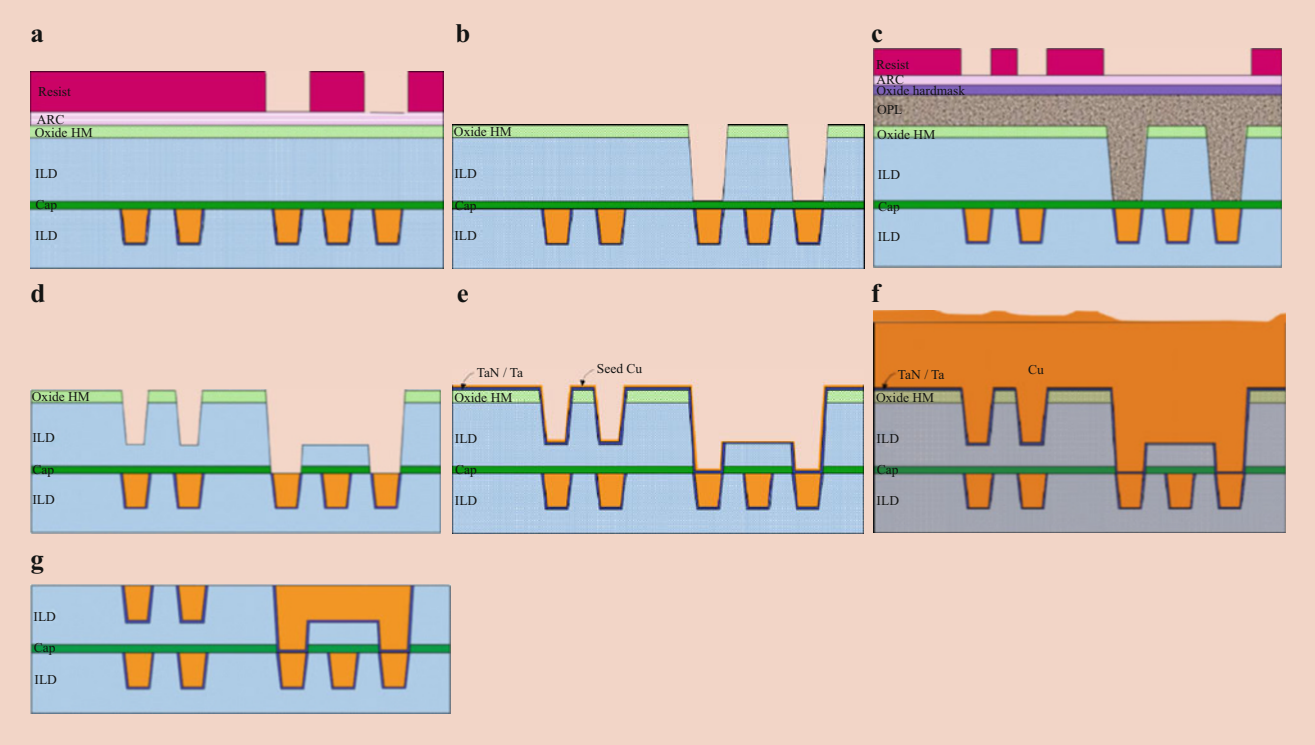

Fig. 5.4 (**a**–**g**) Process sequence for via-first dual damascene integration scheme (see text)

5.1.3 Via-First Dual Damascene Integration Scheme

The via-first scheme is the first dual damascene scheme developed. It was commonly used in earlier technologies. As technology evolved, it is still used in upper levels of the BEOL build in recent technologies as upper levels with larger feature sizes were qualified in previous generation technologies. Most fine pitch levels in late technologies are using the trench-first integration scheme described in the next section. For current technology, a complete BEOL build will have both via-first and trench-first dual damascene scheme in the process flow [1].

Below is a typical via-first dual damascene integration process flow:

Figure 5.4a depicts the start of the integration scheme with a via litho pattern on top of a full via/line ILD stack. Oxide hardmask on ILD is typical for this scheme.

Figure 5.4b shows the via etch stopped on the cap of underlying metal level.

In Fig. 5.4c, the via holes are filled with a spin on OPL material followed by trench litho.

Figure 5.4d depicts the structures after post-trench etch, strip OPL, and wet clean.

Figure 5.4e depicts the fabricated structures after metal barrier and Cu seed deposition.

Figure 5.4f shows the feature fill and overburden with electroplated copper.

Figure 5.4g shows the completed dual damascene level after copper and liner CMP.

5.1.4 Trench-First Dual Damascene Integration Process Flow

Figure 5.5a shows the post-trench litho. An OPL film may be added to improve etch process window.

Figure 5.5b shows the trench etch process to open the hardmask to form the line level pattern.

In Fig. 5.5c, the trench pattern is filled with OPL/HM followed by via litho.

Figure 5.5d shows the via etch followed by trench ILD etch. Metal hardmask wet removal is optional.

Figure 5.5e shows the completed wiring level, post metallization, and CMP.

5.1.5 Single Patterning Versus Double Patterning

Metal lines with pitch size smaller than 80 nm are required for BEOL interconnection beyond 22 nm device technology generation. Conventional 193 nm immersion lithography has

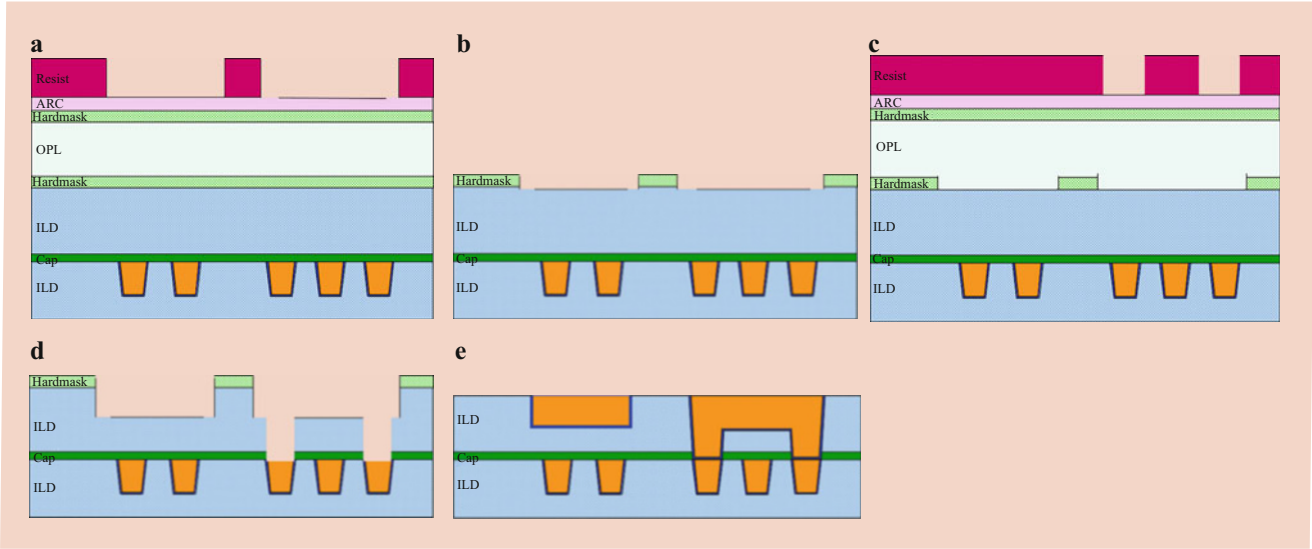

Fig. 5.5 (**a**–**e**) Process sequence for trench-first dual damascene integration scheme (see text)

difficulty resolving trenches below 80 nm pitch with single litho exposure. It is possible to continue the single litho patterning scheme using extreme ultraviolet lithography (abbreviated as "EUVL," or simply "EUV"). Figure 5.6 shows the post-CMP pattern of 36/48/64/72 nm pitch using EUV single exposure in the integration process flow. It covers the BEOL patterning need for 14 nm, 10 nm, and 7 nm generation technologies. However, high EUV litho manufacturing cost and delayed tool availability prevented the semiconductor industry from using it when the product was needed for the market. The double patterning techniques using the conventional 193 nm litho process were developed to meet manufacturing needs; they are described in the following sections [2].

5.1.6 Trench-First Pitch-Split Double Line Patterning with Self-Aligned Via Integration Scheme

Metal lines with pitch size smaller than 80 nm are required for BEOL interconnects beyond the 22 nm device technology generation. The conventional 193 nm immersion lithography has difficulty resolving trenches below 80 nm pitch with a single litho exposure. A patterning method with multiple litho/etch passes per level is needed to build desired BEOL structures, and several possible patterning methods have been proposed [3–6]. The example below demonstrates a patterning method that uses a pitch-split, double-exposure litho process to define the line patterns. Electric yield and reliability concerns associated with this particular patterning method are mainly the line-to-line and line-to-via spacing variation related to the litho double-exposure overlay errors. A self-aligned via (SAV) integration scheme usually is used to (a) minimize the via size variations, (b) minimize the via-to-line alignment errors, and (c) maximize the via-to-line spacing. The details of the SAV process will be described in the next section.

A. Trench pitch-split double patterning

Figure 5.7a shows the first line litho-printed 2× pitch line pattern.

In Fig. 5.7b, the first 2× pitch pattern is etched through hardmask 2.

In Fig. 5.7c, the second 2× pitch line pattern is printed.

Figure 5.7d shows the etching of the second 2× pitch pattern through hardmask 2 and then the etching of both 2× pitch patterns into hardmask 1 to form a 1× pitch pattern. To prevent ILD damage during the second hardmask open etch process, an additional hardmask layer could be added underneath hardmask 1.

Figure 5.7e below shows an example of the top-down SEM image of a post-hardmask, open RIE line pattern. Two 128 nm pitch line patterns (L1 and L2) were printed in sequence to form a 64 nm pitch line pattern. The image on the right shows the post full-dielectric etch trench pattern.

Figure 5.8 shows the post-CMP 64 nm pitch line patterns [2]. It demonstrates that 193 DUV (deep ultraviolet) litho double patterning is feasible.

B. Trench pitch-split double patterning with self-aligned vias (SAV).

Figure 5.9 shows the SAV process flow [7]:

Use pitch-split double patterning scheme to create line patterns in the hardmask.

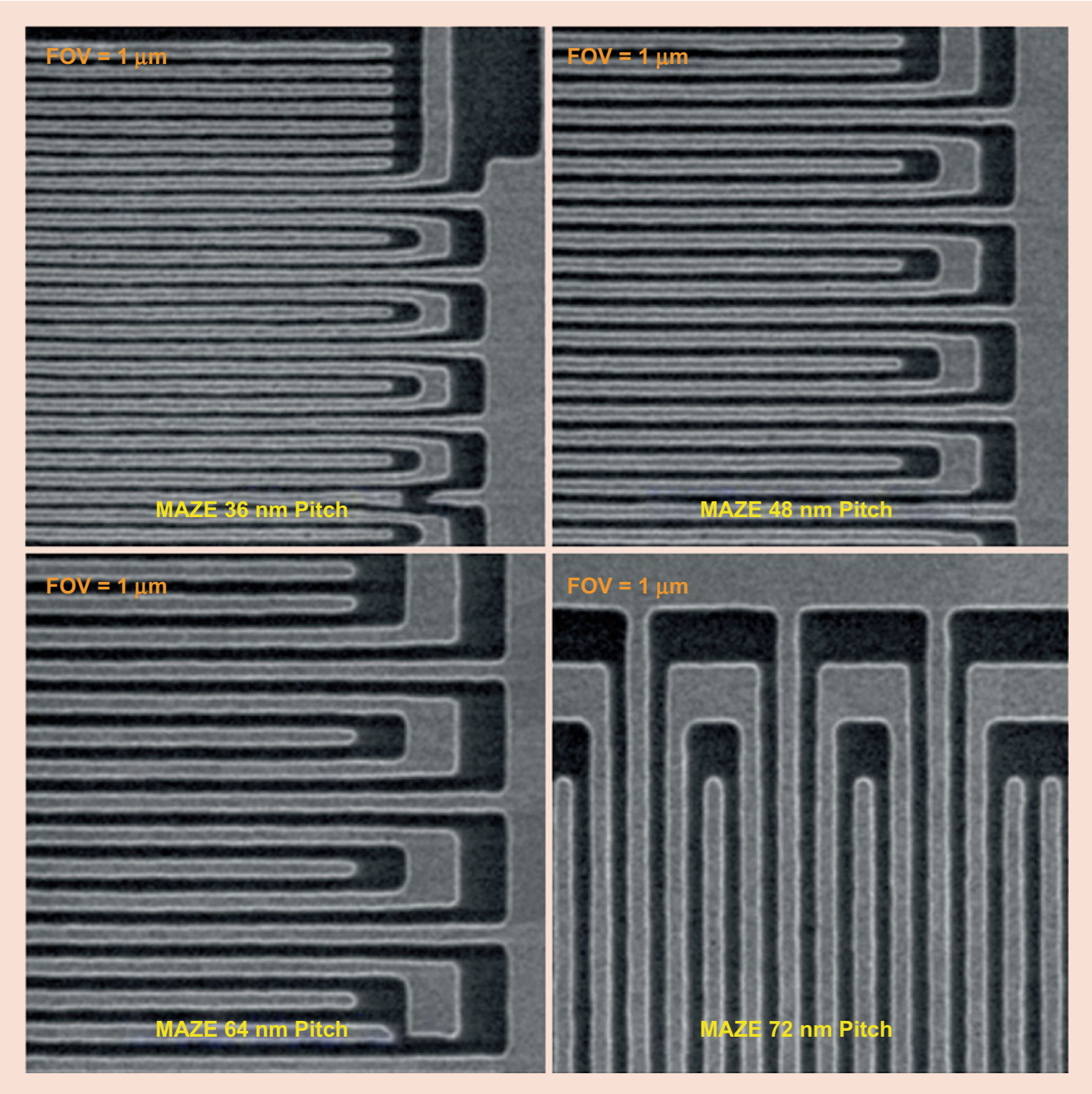

Fig. 5.6 Post-CMP SEM images of 36 nm, 48 nm, 64 nm, and 72 nm pitch wiring structures using a single EUV expose process flow

Planarize the surface with spin on OPL followed by via litho process. Vias are elongated across the line edge defined by the hardmask, i.e., the via litho CD is larger than the line CD.

Etch vias through the dielectric film stack, stop on the cap below. Metal hardmask also served as an etch mask to confine vias inside the line trench pattern.

Complete the line ILD etch and via bottom cap open etch.

Post full-etch SEM top-down image shows vias confined inside line trench patterns.

5.1.7 Self-Aligned Double Patterning (SADP)

As 193 nm DUV lithography is not capable of printing fine pitch patterns needed for 14 nm, 10 nm, and 7 nm node technology generations, double patterning techniques such as litho-etch-litho-etch (LELE) [1], litho-litho-etch (LLE) [2–6], and self-aligned double patterning (SADP) [4, 7] – also known as sidewall image transfer (SIT) – have been used to enable the fine pitch patterning. This section explores the nature of SADP technique. A

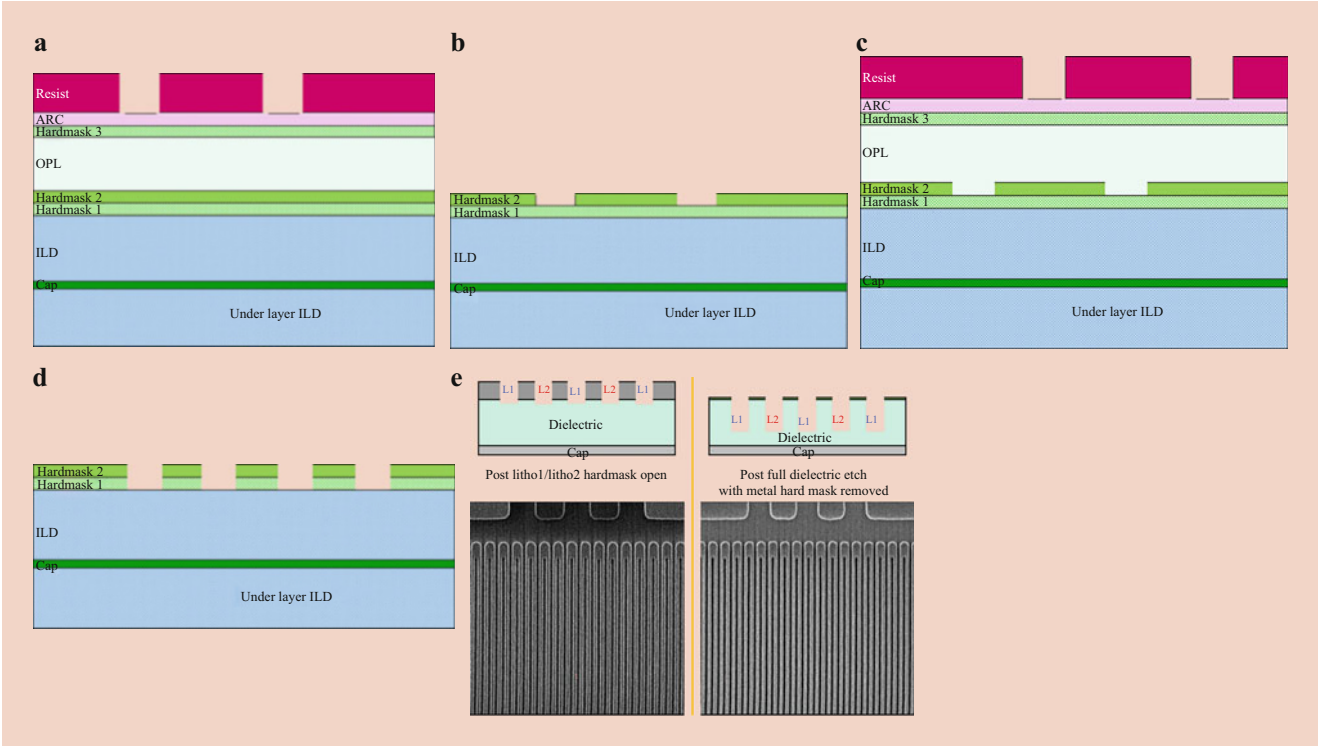

Fig. 5.7 (**a**–**d**) Process flow diagram for a trench-first pitch split patterning scheme. (**e**) SEM images of two 128 nm pitch line patterns (L1 and L2) forming a 64 nm pitch pattern (see text)

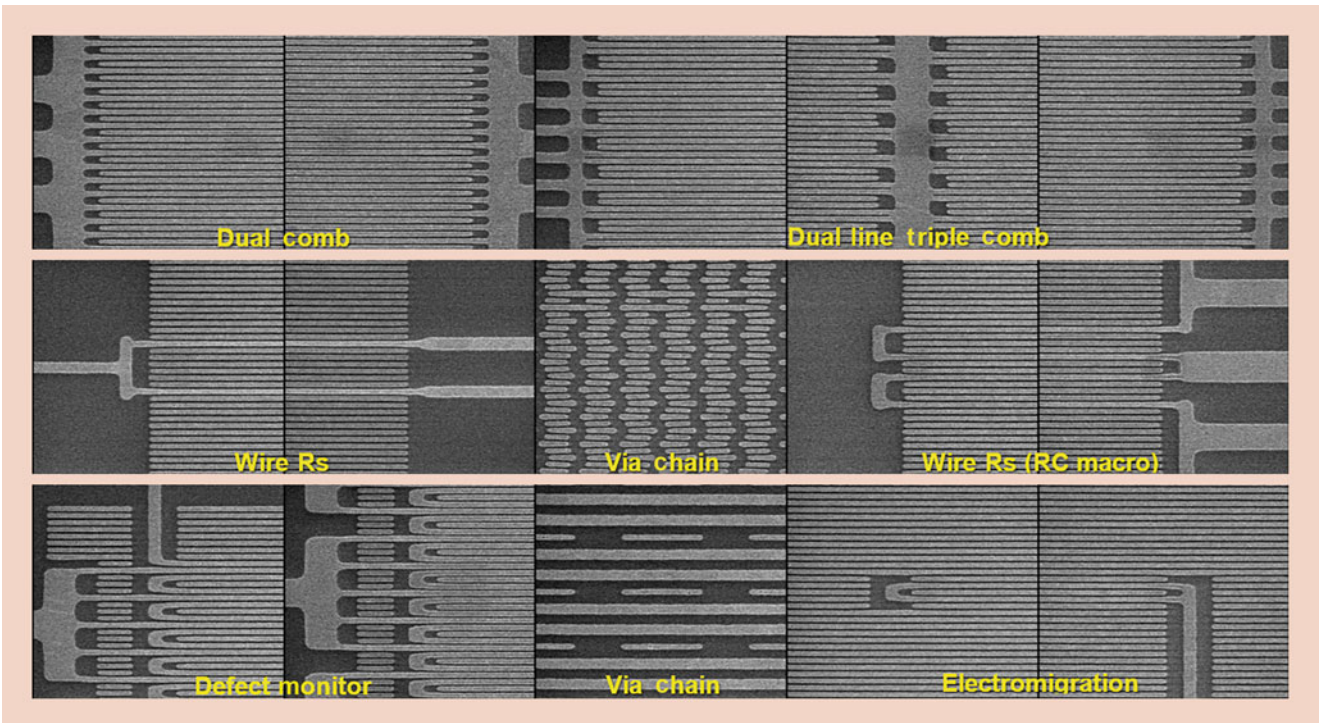

Fig. 5.8 Wiring structures at 64 nm pitch fabricated using a 193 DUV litho double patterning process flow. (Ref. [7], reprinted with permission)

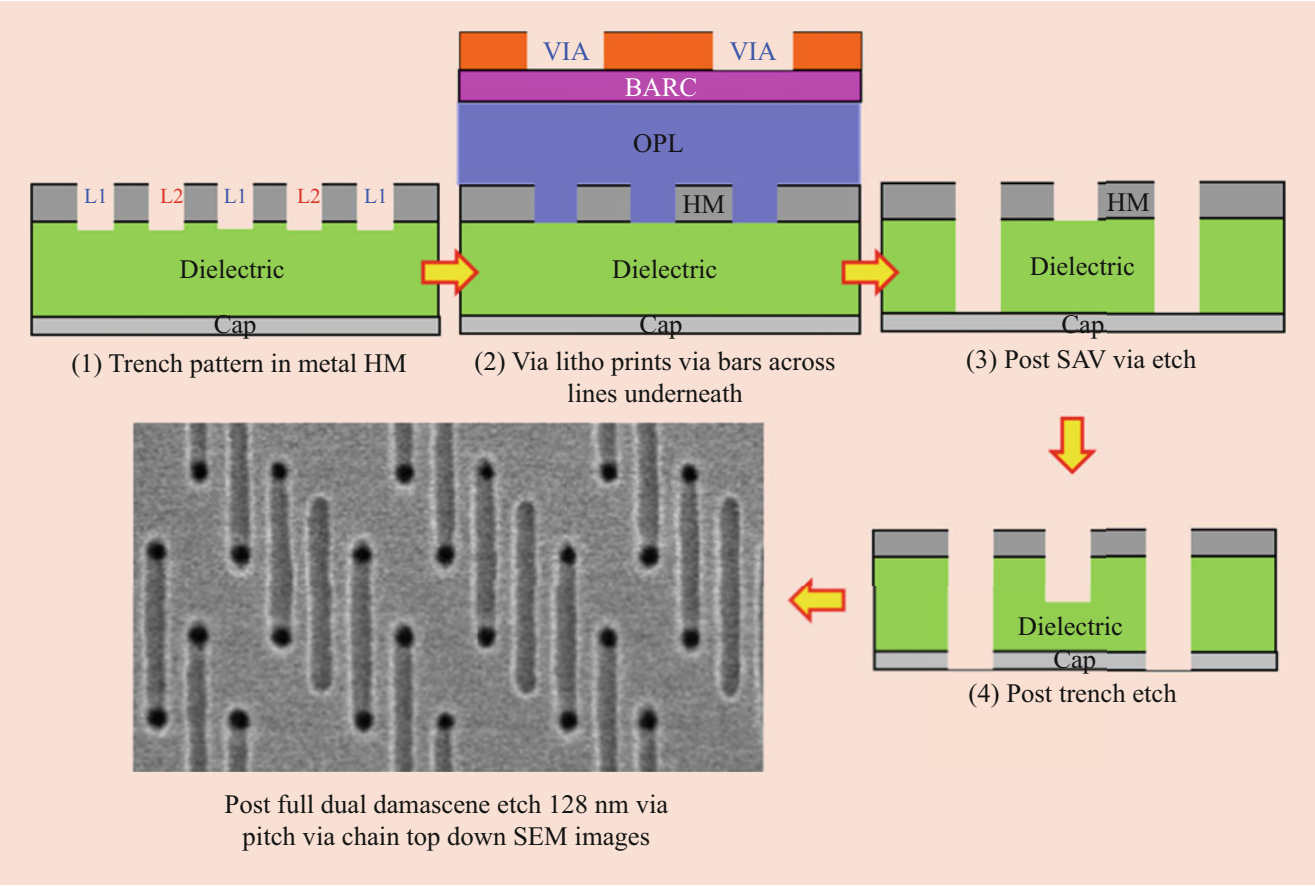

Fig. 5.9 Diagram of a self-aligned via process flow using a pitch-split double patterning scheme, with SEM image of the resulting structures. (Ref. [7], reprinted with permission)

48 nm line pitch SADP build was used as an example here [8].

Process flow of SADP integration scheme is shown below with corresponding top-down SEM image placed below each schematic step.

1. Figure 5.10a shows post-mandrel pattern litho
2. Etch follows to form the 2× pitch mandrel pattern in mandrel dielectrics.
3. A conformal spacer dielectric is deposited over the mandrel pattern.
4. Figure 5.10b: After spacer etch back and mandrel dielectric material etch. The 1× pitch pattern is formed on the wafer.
5. BLOCK TRIM lithography patterning follows.
6. BLOCK TRIM litho/etch are used to block areas that do not need final trench pattern formed.
7. Figure 5.10c: For single damascene build, a final etch is used to form final trench pattern. For dual damascene integration, additional via patterning steps are implemented before the final trench etch step.
8. Metallization.
9. Cu CMP.

5.1.8 2D Versus 1D Self-Aligned Double Patterning (SADP)

The SADP process flow demonstrated in the last section is for 2D patterning. Because of the nature of the process flow, spacing between lines are fixed and determined by the spacer thickness. This means that even large size metal features will only have small spacing same as the minimum size features. This scheme often causes defect issues. Also, fine line features with tight turn around or cross shapes often have defects associated with these types of patterns.

As the result, it is common for chip industry to limit the pattern using SADP process to 1D only. This means that only straight-line patterns are allowed in one preferred orientation (horizontal or vertical). The level above or below will be the same with alternating horizontal and vertical wiring orientations. This simplifies the process but will require interlevel vias for signal transmission and electrical testing.

In general, a SADP, double patterning process flow is more complex than the pitch-split double patterning, but it may be able to provide a smaller final pitch pattern. It is also possible to combine both schemes to further reduce the

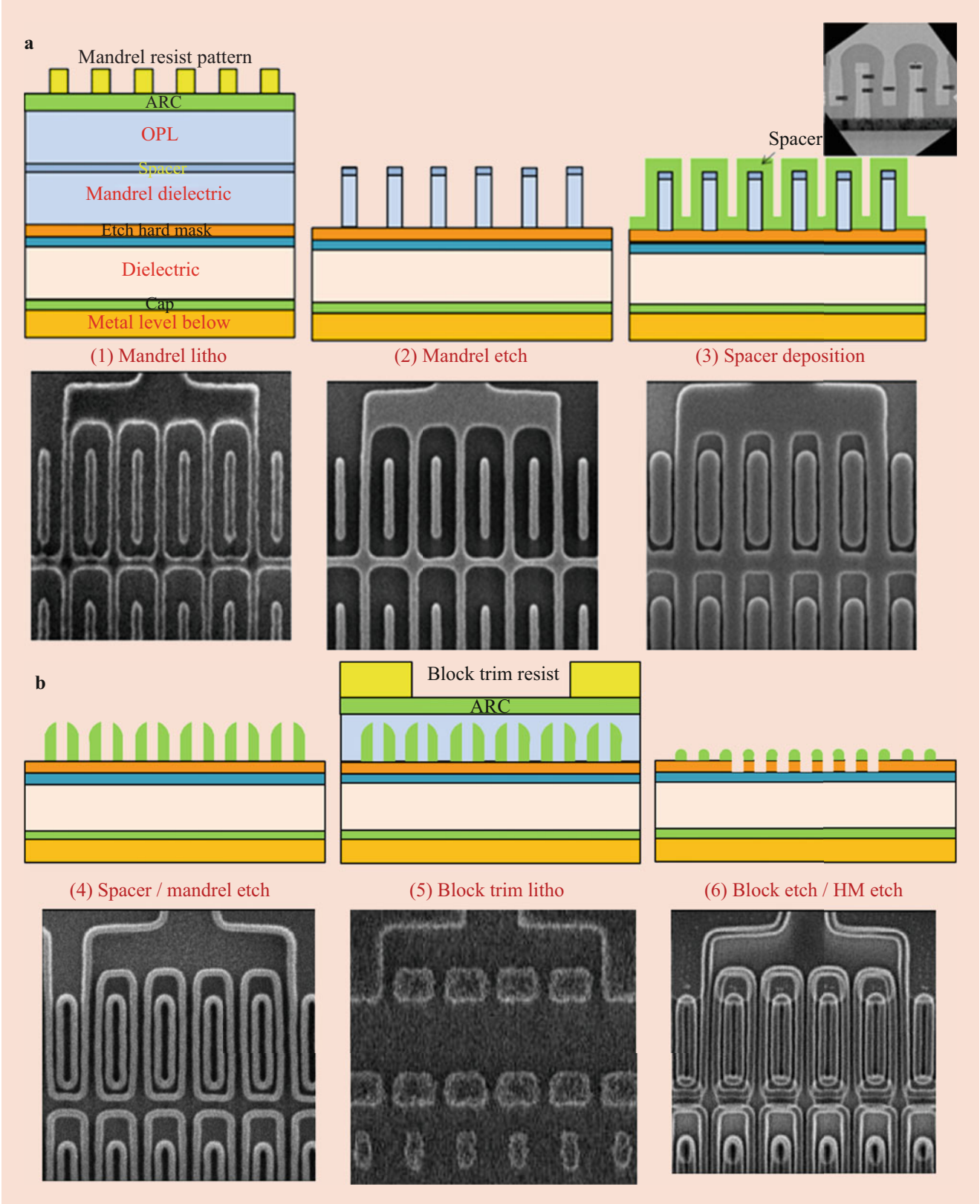

Fig. 5.10 (continued)

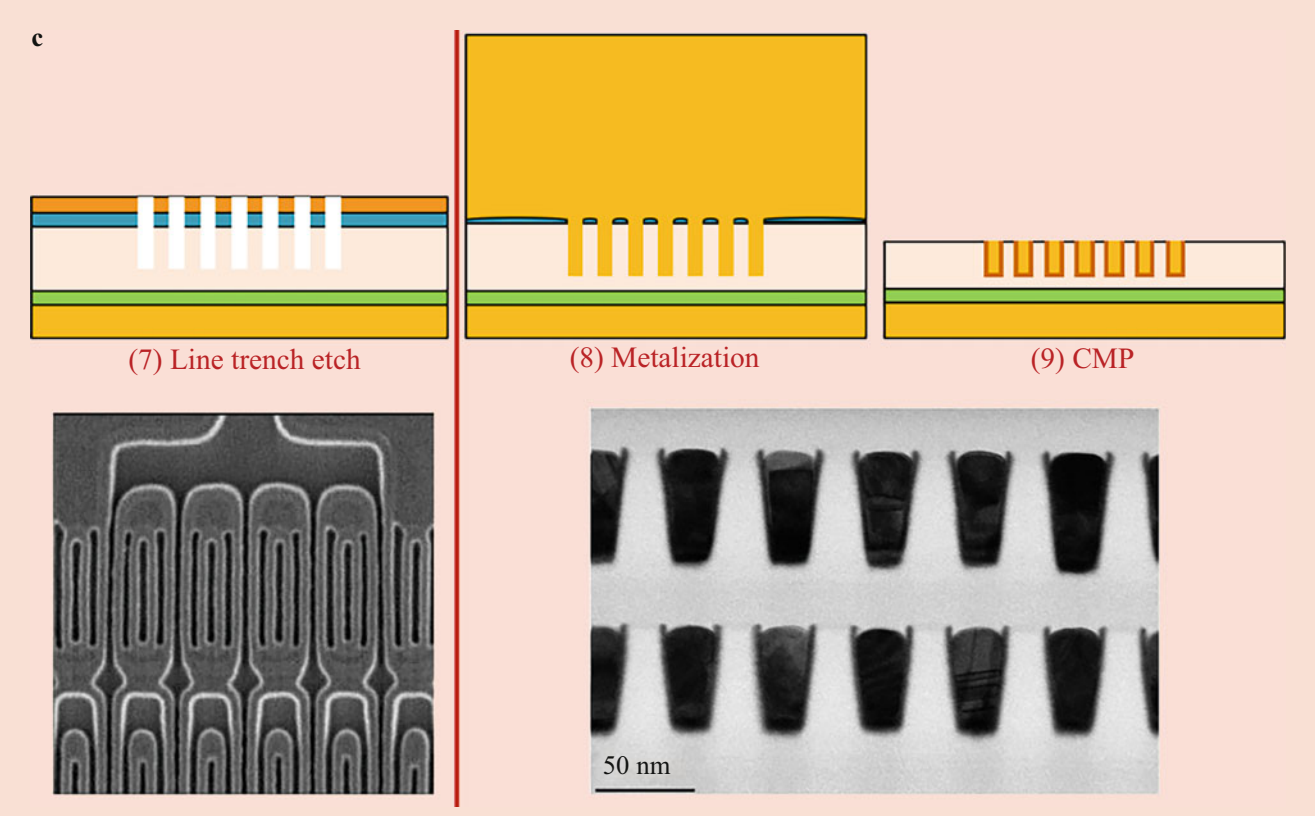

Fig. 5.10 Diagram of a self-aligned double patterning process flow with representative SEM images from each stage of the process (see text). (Ref. [8], reprinted with permission)

minimum pitch size. For example, one may use pitch split to create mandrel pattern for the SAHD process flow.

5.1.9 Future Outlook: EUV Single and Double Patterning

Future logic development at technology nodes of 5 nm and below will depend heavily on further development of EUV patterning schemes. With that in mind, several issues related to integration of EUV into BEOL will figure prominently.

EUV single patterning innovation will be critical. The EUV litho tool has evolved to print smaller and smaller feature size pattern with single exposure. With high NA (numerical aperture), it may be possible to print 20 nm pitch line patterns on the wafer. In this case, the pattern size on the mask would be 80 nm pitch, as traditionally the print reduction from mask to wafer is 4–1. This 80 nm pitch size may already hit the mask patterning limitation. To print details smaller than a 20 nm pitch on the wafer may require increasing this reduction ratio to over 4. For example, if the reduction ratio is 5 with new optics in the litho tool, it may be possible to print 16 nm pitch pattern on the wafer assuming that the photo resist is available for this feature size. EUV double patterning will also present opportunities. Just like 193 nm DUV litho double patterning, it is also possible to use EUV double patterning for integration. It would be much easier to print 2× pitch pattern using EUV litho tool.

Integration of advanced BEOL nodes at smaller ground rules will also open up other issues in integrating advanced lithography. Defect characterization and minimization will evolve. As pattern feature size becomes very small, it is more challenging to characterize the defects in the pattern and eliminate them. For very fine lines, copper may not be the best conductor material for the metal line. The traditional damascene scheme using a liner and copper fill metal may result in the higher resistance liner layers simply filling up the trench space, leaving minimal volume for the copper conductor to fill. Also, at small line widths, copper line resistance may not be smaller than other candidate materials, such as cobalt, ruthenium, etc. If choosing another conducting material to replace copper, the integration scheme may need to be re-engineered to adapt the new material. Some of these topics will be covered further in the metallization section later in this chapter. In summary, very fine pitch line patterning remains as a very challenging task, and it will require a significant amount of effort and resources to accomplish the mission.

5.1.10 BEOL Performance

Back-end-of-line (BEOL) interconnect resistance has a major influence on overall device performance in advanced CMOS technology nodes. As critical dimensions continue to shrink, interconnect line resistance increases due to reduced cross-sectional area available for conduction as well as because of the well-known resistivity size effect [9–12]. Tight process control is critical to minimize structural variations, which in turn impact line resistance and overall performance. Even relatively minor variations in interconnect geometry arising from line edge roughness, RIE lag, and CMP can have nontrivial impacts on overall performance [13].

Gauging the impact of minimum pitch interconnect line resistance on overall performance depends on several factors, including design architecture. For example, an inverter can have a variable fanout (FO) depending on how many inverters are being driven by the output of the first. In Fig. 5.11, we show schematic circuit diagrams for simple inverters with FO of 1, 2, and 3. It has also been reported that the impact of BEOL resistance modulation depends on the relative FEOL resistance, determined by the device architecture and driver size [14]. Device architectures with larger inverter drive strength have larger contacts and lower resistance, which increases the sensitivity to BEOL resistance.

In advanced technology nodes beyond the 7-nanometer node, BEOL loading represents an increasing percentage of the overall delay. In Fig. 5.12a, we show the frequency as a function of power for a four-fingered inverter with a three-way fanout. The loaded case assumes 30 nm pitch interconnects with line resistance estimated based on temperature coefficient of resistivity (TCR) measurements as reported in the literature [15, 16]. The unloaded case assumes zero BEOL resistance. The difference between the loaded and unloaded cases is quite large, indicating that interconnect delay is a major bottleneck in achieving favorable overall performance.

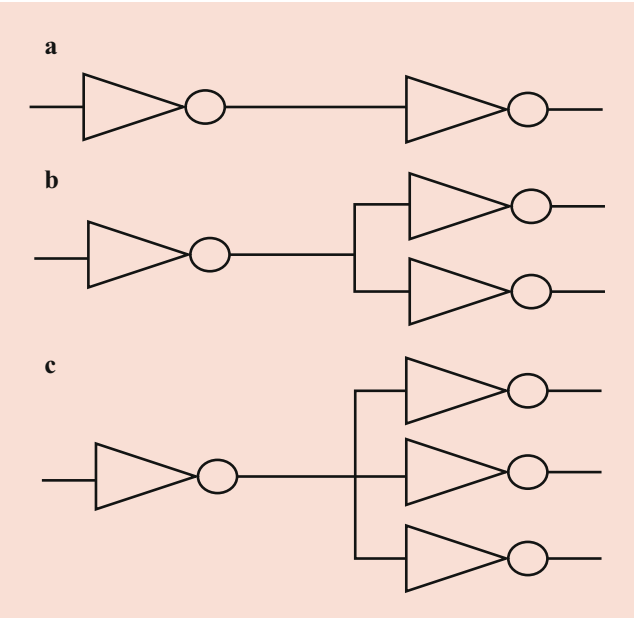

Fig. 5.11 Circuit diagrams for inverters with fan-out of (**a**) 1, (**b**) 2, and (**c**) 3 used for performance benchmarking

In Fig. 5.12b, we show the impact of line resistance reduction for a four-fingered inverter with variable fanout. We see enhanced sensitivity to line resistance modulation as the fanout increases from 1 to 3, since the BEOL load is being spread over more and more transistors. The performance uplift arising from a 50% reduction in line resistance at 30 nm pitch is between 10% and 15% depending on the circuit topology.

As technology nodes continue to shrink, the importance of BEOL parasitic resistance will grow ever larger. Significant innovation in metallization and the development of tight process control are paramount to enabling the successful scaling of future technologies.

5.2 BEOL Dielectric Films

In 1965, the first semiconductor device was fabricated at Bell Laboratories [17] to initiate a semiconductor industry that integrates various electronic components onto the same Si chip creating the integrated circuits (IC) and using the same materials in its structures. Today, the industry is integrating also various materials in the same chip, after extensive and prolonged development efforts to accomplish successful integration of the required new materials. Among these new materials are the dielectric insulators of the interconnects of VLSI chips.

For the last 50 years, the performance of the VLSI integrated circuits was progressing following Moore's law [17], by shrinking the dimensions of the individual devices and packing more devices in the same area. The decreasing dimensions of the devices made them faster with each new technology generation. Tremendous progress in the manufacturing of integrated circuits over the past 50 years has reduced the device feature size, which has gone from 10 μm down to 5 nm and beyond. The per transistor cost has decreased by eight orders of magnitude, and the maximum number of transistors per chip has increased by billions of times.

Figure 5.13 shows a diagram of a typical cross section of an advanced IBM 14 nm devices circuit and an illustrated graphic of an integrated memory/logic circuit that will be implemented for advance AI structure in the Cu low-*k* interconnect. Most of the device cross section's real estate is occupied by the interconnect back end of line (BEOL). These wirings are to connect between individual active devices,

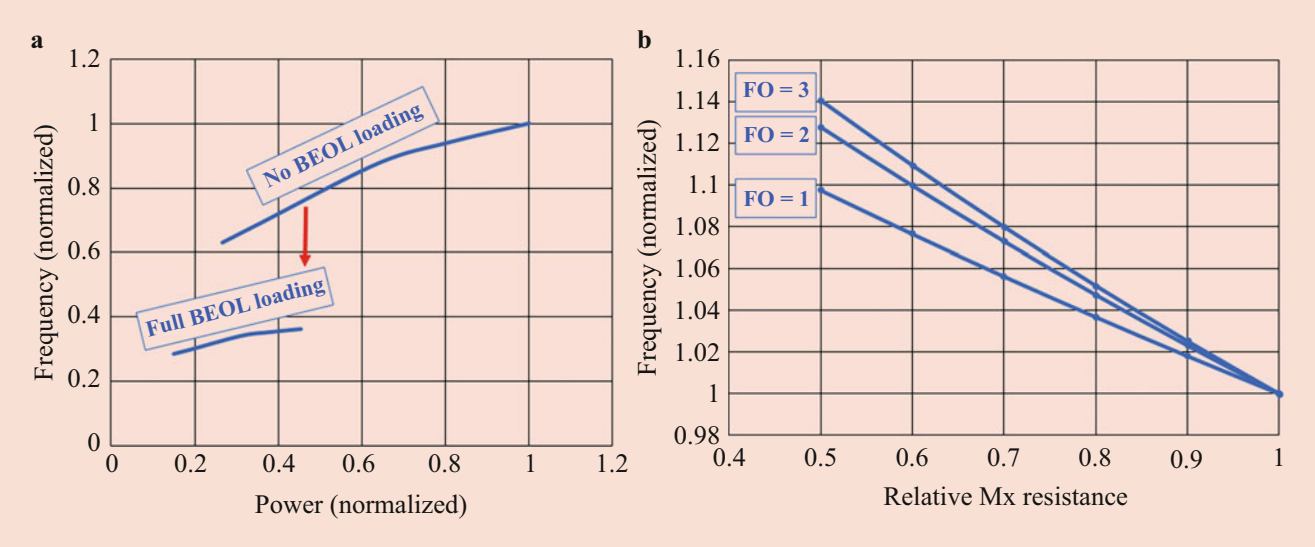

Fig. 5.12 (**a**) Overall device performance for a circuit with and without BEOL loading. (**b**) Performance impact of line resistance reduction for variable inverter fan out

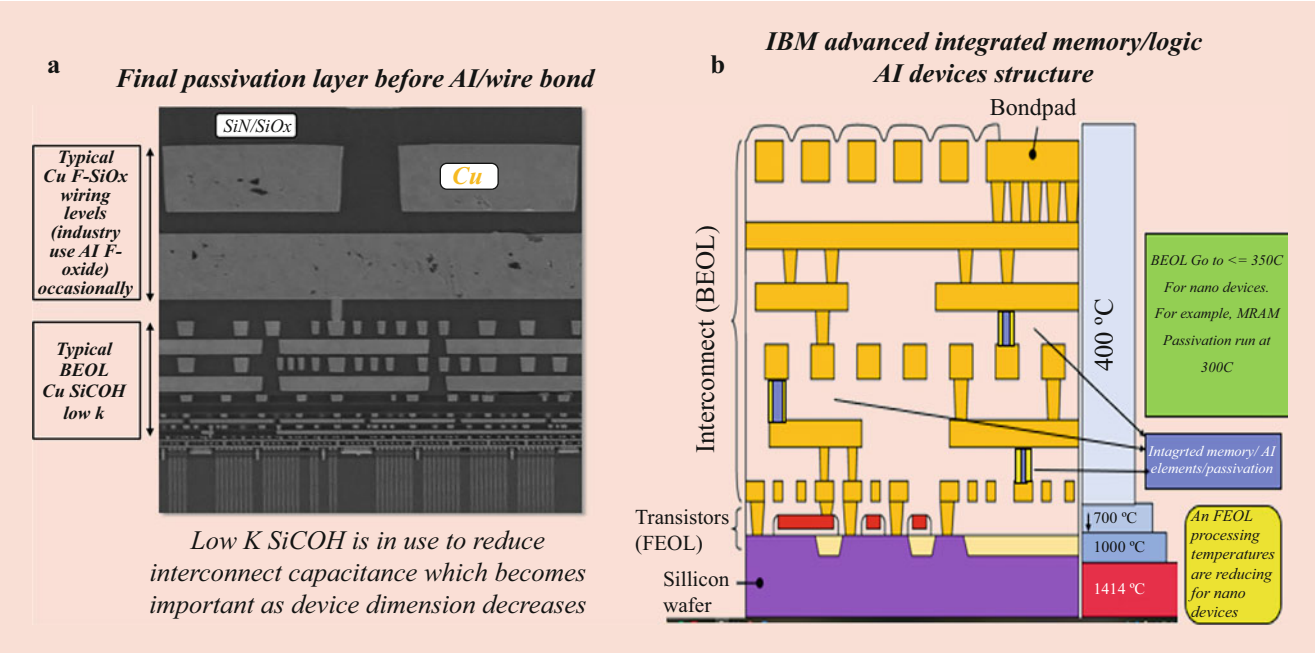

Fig. 5.13 (**a**) Scanning Transmission Electron Microscopy (STEM) picture of an Advanced IBM 14 nm chip. (**b**) Diagram of a cross section of an advanced integrated circuit, integrating both memory and logic using nano-dimension circuit with Cu/low-*k* interconnect

transferring signal between the logic/memory devices and eventually the outside of the chip as electrical current signal. For nano-dimension circuits, the signal delay between the active devices, the integrated memory and logic, and the cross talk between devices and the outside world strongly depend on the *RC* (R = resistance; C = capacitance) of the BEOL. Resistance R is directly related to the metal wiring (Al, Cu, Co, etc.) and capacitance C is directly related to the dielectric material used in the BEOL fabrication. Until the 0.25 μm generation, the interconnect was composed mostly of the elements Si, O, N, and F for dielectric and aluminum and polysilicon for wiring. At this technology node, the *RC* of the BEOL became a bottleneck to the improvement of the performance of the VLSI devices. The *RC* of a metallization level in the interconnect can be defined by [18].

$$\mathrm{RC} = 2\rho k\left(4L^2/P^2 + L^2/T^2\right)$$

where L = line length, P = metal pitch, T = thickness of metal line, ρ = metal resistivity, and k = dielectric constant.

The reduced dimensions of the devices resulted in the increase of both R and C to the extent that, while the active devices became faster, the interconnects did not. Since the original SiOx dielectric, the next material to be successfully integrated in a microprocessor was fluorinated silicon glass (FSG or SiOF), introduced in 2000 as the intra- and interlevel (ILD) dielectric at the 0.18 μm technology node [19, 20]. The fluorination of the silicon dioxide reduced its dielectric constant from 4.1 to 3.6, thereby reducing the capacitance of the interconnect and reducing the overall RC.

5.2.1 Fabrication of BEOL Low-*k* Dielectric Films

The promotion of a chemical reaction by an electrical discharge through gasses has been known for over a century. The first work specifically aimed at plasma deposition for microelectronic uses appeared in 1963 but 10 more years passed before commercial batch processing equipment was introduced [42]. Plasma-assisted deposition of thin films is widely used in microelectronic circuit manufacturing since the 1980s [43], and a comprehensive review of the previous generation of dielectric materials such as SiOx, SiNx, and F-SiOx before SiCOH generation, including high-density plasma processing, are included in these two reviews [43, 44]. In the early 1980s, IBM evaluated low-k SiCOH as plasma-deposited organosilicon polymer using various organosilicon polymers for lithographic measurement [45]. Early metal-insulator-semiconductor (MIS) electrical measurement showed that SiCOH organosilicon film with dielectric constant (k) value around 3.4 may be obtained for this SiCOH. Since the late 1990s, plasma-deposited processing has also been used to deposit SiCOH film with $k \sim$ 3–3.2 for advanced Cu/SiCOH microelectronic fabrication for 90 nm device node [25–28].

The first successful non-SiOx low-dielectric constant material in IBM was the organosilicate glass, SiCOH, deposited by plasma-enhanced chemical vapor deposition (PECVD) [21] with a dielectric constant k = 3.0. SiCOH 3.0 was successfully integrated in some 130 nm and 90 nm products starting in 2001 [22–24] and then in almost all the 90 nm node industry products since 2004 [25–27]. Figure 5.13 shows a typical advanced IBM 14 nm node chip and representative diagram of various layer and potential integrated memory element that can be implemented in advanced integrated memory-logic device structure. There are many polymers and dielectric materials that have been explored as low-k dielectrics over the years [28–30], but the most successful ones are plasma-deposited SiCOH and porous SiCOH that have been implemented widely in Cu/low-k interconnect BEOL by the semiconductor industry in the last 20 years. In this section, we will focus mostly to the plasma-deposited SiCOH and other potential plasma low-k dielectrics.

For plasma-deposited SiCOH dielectric materials, there are two main approaches that have been implemented to reduce the k value in the film: (1) insertion of carbon into the well-known SiO_2 bonding network for SiCOH film and increase of the low-polarity bonding and materials (increase C-C, Si-CH_3, Si-C-Si low polar bonding) in the SiCOH film to reduce the polarizability. (2) Creation/insertion of porosity into the SiCOH film by changing deposition process parameters and/or subsequent post-deposition film's treatment by low-temperature UV/E-beam or thermal processing.

The "carbon-doped" oxide (a-SiOC:H) material has a reduced dielectric constant value k in the 3.0–3.2 range, and the porous low-k SiCOH film has a dielectric constant value in the 1.8–2.8 range with 7–50% porosity. The slow progress in implementing highly porous, ultralow-k SiCOH ($k < 2.7$) into production has been mostly related to the weak mechanical properties of the low-k film. The difficulties in integrating these new materials into current metallization and patterning are well documented [31–41].

5.2.2 Low-*k* and Ultralow-*k* Porous pSiCOH ILD Dielectrics

Dense SiCOH and Porous pSiCOH ILDs

Plasma deposition of SiCOH interlevel dielectrics is normally achieved in a parallel plate reactor with a skeleton organosilicon precursor mixed with a porogen precursor in liquid (with carrier gas) and reactive gasses in the reactor during the deposition. Tetramethylcyclotetrasiloxane (TMCTS), octamethylcyclotetrasiloxane (OMCTS), and Tetramethyl Silane, Diethoxymethylsilane (DEMS) decamethylcyclopentasiloxane, or linear or branched compounds such as methyltriethoxysilane, methyltriethoxysilane, or vinyl variations of above are the widely used skeleton precursors (see Fig. 5.14) [46–48]. For porogen, unsaturated cyclic hydrocarbons like terpinenes or norbornenes as listed in Table 5.1 are widely used. These skeleton organosilicon precursors, especially the one with stable ring structure precursor as OMCTS and TMCTS, have a common stable structural property with a sufficiently low dissociation level under RF power. The stable structure retention with increased cross-linking bonding will increase overall SiCOH film's bonding density and subsequently enables the increased film's modulus and hardness for the produced low-k dielectric material. The porogen precursor is an organic molecule with enough volatility. Other precursors like linear alkenes, or molecules with strained rings like cycloalkene oxides or butadiene monoxide, have been explored but with limited use [40, 49]. The as-deposited SiCOH-CxHy organosilicon-hydrocarbon matrix films are normally deposited by plasma CVD process in temperature range below 300 °C. After the deposition, the film must be

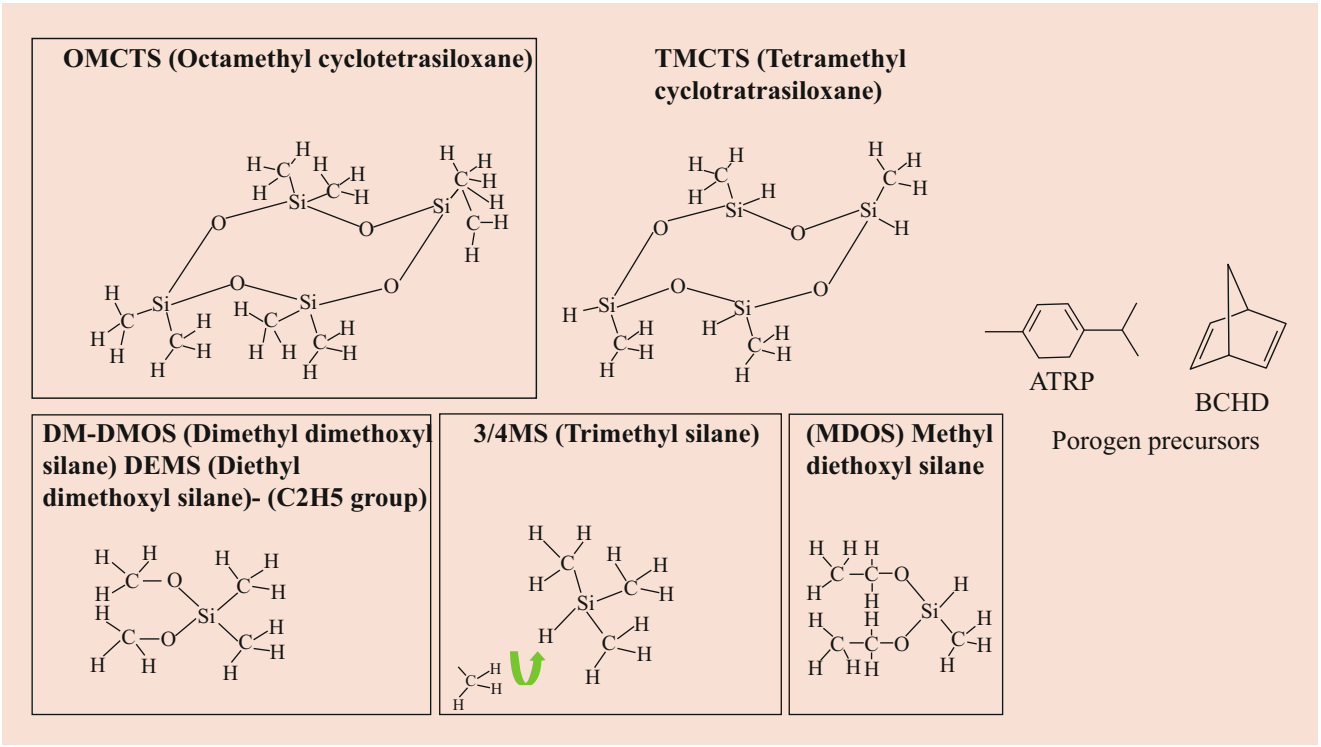

Fig. 5.14 Typical organosilicon precursors and two basic commonly used hydrocarbon porogens for low-*k* SiCOH dielectric and SiCN, SiC caps. The plasma CVD processes also uses various oxygen (O_2, N_2O, CO_2) and nitrogen (N_2, NH_3)-based gases

cured to remove the labile organic porogen fraction CxHy and form a porous film. The curing can be done thermally [50] or using electron beam or ultraviolet (UV) irradiation [51]. For Cu interconnect, the thermal cure is not in favor since it requires several hours curing at 400 °C and generally produces films of low mechanical strength. E-beam curing has been explored and generally found to cause some device damage. The semiconductor tooling industry has adopted instead broadband UV curing for the fabrication of pSiCOH dielectrics. The UV curing with 210–400 nm wavelength is normally done in a few minutes with limited device's thermal and radiation exposure of under layers and has become the choice process for the industry. For porous SiCOH film's formation, the UV curing process removes some weakly bounded porogen volatiles, breaks a fraction of mainly the Si-CH_3 (Si-Me) bonds, and rearranges and enhances the cross-linking of the skeleton. Better removal efficiency of volatiles can be done by UV-assisted curing. However, the temperature of the curing must be limited at ≤400 °C. The mechanical strength (elastic modulus and hardness) of the porous low-*k* SiCOH dielectric material is improved by UV-assisted curing due to the rearranging and enhancing of the cross-linking of the skeleton of the low-*k* SiCOH. Long UV cure may increase the modulus by increasing cross-linking bonding for even extreme porous low-*k* materials. However, long overcure can cause loss of too many Si-Me bonds and pore collapse, resulting in films of higher-*k* values [40].

For dense SiCOH ($k \sim 3.0$) and lightly porous SiCOH ($k \sim 2.7$–2.8), the film is normally deposited at the 350–400 °C temperature range [52, 53] with an adhesion layer of SiOx film to increase the adhesion strength between the SiCOH and the deposited under layer, e.g., the SiN or SiCN cap [54]. The reduced *k* SiCOH films with $k \sim 2.7$–2.8 is also deposited in a production-300 mm PECVD system using a commercially available, simple ring structure organosiloxane OMCTS precursor, and oxygen at 350 °C under the dual RF frequencies. Low-*k* SiCOH of 3.0 and lightly porous $k \sim 2.7$–2.8 film deposition using basically the same precursors and process equipment are utilized. The plasma deposition process parameters such RF power frequencies and densities, pressure, temperature, electrode spacing, and precursor ratio can be changed to deposit higher or lower-*k* values by changing the SiCOH film's porosity from none (dense SiCOH film, $k \sim 3.0$) to lightly porous SiCOH (7–8% porosity, $k \sim 2.7$–2.8). SiCOH films are characterized by using various electrical measurement and analysis techniques including nanoindentation for modulus (E) and hardness (H), four-point bending method for adhesion, Fourier transform infrared (FTIR) and nuclear magnetic resonance (NMR) for bonding structure, and X-ray reflection (XRR) for film density. The crack velocity and cohesive strength is also measured at this stage. The film structure analysis shows that the optimized films have 7–8% porosity and contain a high level of cross-linked Si-O and Si-CH2-Si bonding, which

Table 5.1 Comprehensive physical, electrical, and bonding structure properties and performance of dense SiCOH 3.0 and lightly porous SiCOH 2.7–2.8, low-*k* dielectrics

Film properties	SiCOH 3.0	SiCOH 2.7	Low-stress SiCOH 2.7	SiCOH 2.8
K 23C (MIS AI dots) at 150 °C	3.05	2.63	2.67	2.76
		2.56	2.62	2.70
Vbd 23C 150 °C	9.0 MV/cm	8.5 MV/cm	9 MV/cm	9 MV/cm
	9.5 MV/cm	9 MV/cm	>9 MV/cm	>9 MV/cm
I–V @ 2MV 23C 150 °C	1E−10	1E−10	1E−10 (small water peak)	8E−9 (water peak)
	5E−9	5E−9	5E−9	1E−B
Stress (MPa)	30	42.9	49.1	66
Modulus (GPa)	15.8	7.1	7	9
Adhesion (J/m^2)	4.8∼5.1	3.79	4.07	4.08
Density (XRR)	1.45	1.31	1.42	1.41
Cohesive strength (J/m^2)	6.0	4.6	5.3	∼4.8
Hardness (GPa)	2.20	0 75	1.08	1.04
G (energy release rate J/m^2)	59	380	326	397

Table 5.2 Comprehensive physical, electrical, and bonding structure properties and performance of dense SiCOH 3.0 and lightly porous SiCOH 2.7–2.8, low-*k* dielectrics

Film properties	SiCOH 3.0	SiCOH 2.7	Low-stress SiCOH 2.7	SiCOH 2.8
Film/process transparency compare to dense SiCOH 3.0	NA	2X RIE lag:0.826 μm	2X RIE lag:.876 um	2X RIE lag:.875 μm
		RGA: low H2O, m > 58	RGA: higher H2O, higher m > 58	
Thermal conductivity (as a reference data)	0.31	0.22	0.21	0.21
CTE [ppm/C]	11.6	11.6 (est)	11.6 (est.)	11.6 (old data)
Composition (RBS/HFS) = Si: C: O: H	0.22: 0.11: 0.35: 0.32	0.18:0.12: 0.27:0.43	0.19:0.12 0:29:0.4	0.20:0.13: 0.31:0.36
NMR (=M: D: T: Q)	0.06: 0.25: 0.51: 0.18	0.07:0.27 0.46:0.14	0.034:0.216 0.527:0.178	0.027:0.156 0.550:0.267
Thermal desorption analysis	61	n/a	∼80	80
Cracking thickness threshold	10–15 μm	>2.8 μm	4.0 μm	3.0
Porosity [%] (EP)	<1.0	7.0	7.0	8%

is attributed to its overall lower-*k* and improved mechanical strength. The improved low-stress mechanical properties make SiCOH 2.7 implementation possible in various interlevel dielectrics of 65/45/32 nm Cu/low-*k* BEOL. Tables 5.1 and 5.2 show a list of film's properties of plasma-deposited dense SiCOH with $k \sim 3.0$ and lightly porous SiCOH with $k = 2.7$–2.8 range.

The fabrication of low- and ultralow-*k* SiCOH dielectrics in the BEOL interconnect structures of ULSI chips involves may complex stacks with multiple interfaces as shown in Fig. 5.13. Complex and reliable chips require strong adhesion between the different layers of the stacks. A critical interface in the dielectric stack is the interface between the standard diffusion cap (SiCN or AlOx/SiCO) and the SiCOH inter- and intralevel dielectric materials. In standard deposition of SiCOH process, the interface layer is weakened both by a low adhesion strength between SiCNH and SiCOH and by the formation of an initial layer of SiCOH with reduced cohesive strength. By modifying and engineering the gas and RF power during initial deposition process, the interface composition can be modified to obtain interfacial strengths close to the cohesive strengths of the bulk ILD [53]. The film integration into 65/45/32 nm ground rule structures is achieved by direct CMP and results in high-yield, low RC Cu low-*k* interconnect as representatively shown in 65 nm node, 10 levels BEOL Cu/low-*k* structures fabricated with F-SiO*x* ($K \sim 3.6$), dense SiCOH ($k \sim 3.0$), and lightly porous SiCOH ($K \sim 2.75$), Fig. 5.15. Capacitance reduction by various low-*k* dielectrics can be demonstrated by measuring the RC reduction in a single layer of 4× fat wire of 45 nm BEOL, as shown in Fig. 5.16.

Development of Advanced pSiCOH with Improved Properties

Further reduction of the dielectric constant of the above SiCOH 2.7 films requires further introduction of porosity higher than 10% in the low-*k* SiCOH dielectrics. Porous pSiCOH films can be fabricated by the *subtractive* methods [39] to achieve highly porous SiCOH film with $k \leq 2.55$ [39–41]. As mentioned above, the porous SiCOH films are

deposited as a dual-phase material, SiCOH-CHx with the UV cure, to obtain porous low-*k* film with improved mechanical strength (higher elastic modulus and hardness). The value of the modulus increases with longer UV cure; however, over-cure can cause loss of too many Si-methyl bonds and pore collapse, resulting in films of higher-*k* values. Mechanical robustness of low-*k* porous SiCOH can also be improved by controlling porogen decomposition prior to UV curing, to achieve significant reduction in the dielectric constant from 2.3 to 1.8 with Young's modulus in the range 4.6–5.2 GPa even at very high porosity levels, e.g., from 32% to 46% open porosity [55]. The increase in Young's modulus is attributed to an enhanced molecular bridging mechanism when the film is hardened without porogen. UV cure wavelength also has significant impact on pSiCOH film performance such as plasma processing-induced damage (PID) [57]. The choice of the UV curing light source ($\lambda = 172$ nm vs $\lambda > 200$ nm) has significant impact on the chemical composition of the low-*k* material and modifies the porogen removal efficiency and, subsequently, the material porosity [20]. However, the high and open porosity will cause a significantly high moisture absorption and diffusion, making the material too fragile for high-yield reliable nano integrated circuit fabrication.

Furthermore, high porosity in SiCOH film will have strong effect on the p-SiCOH electrical leakage and breakdown [57]. Under specific UV processing, the leakage current is found to be insensitive to porosity, suggesting a bulk conduction mechanism. However, the increasing porosity results in lower breakdown fields which indicate that porosity can degrade the electrical reliability performance of the dielectric materials. The impact of porosity into the electrical properties of SiCOH has been attributed to the complex change in the film's bonding structure with film's deposition process and UV cure conditions [57].

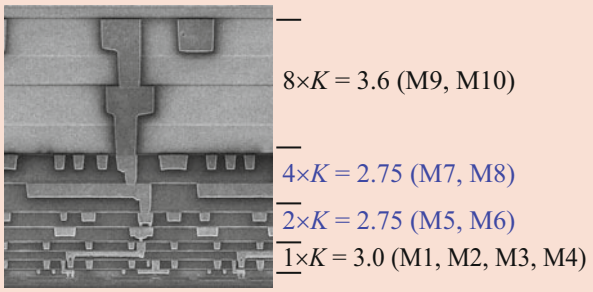

Fig. 5.15 Typical 65-nm node, 10 levels BEOL Cu/low-*k* structures fabricated with F-SiO*x* ($K \sim 3.6$), dense SiCOH ($k \sim 3.0$), and lightly porous SiCOH ($K \sim 2.75$)

BEOL Integration Challenges for Low-*k* and ULK SiCOH

For a successful SiCOH dielectric integration into nano ULSI electronic devices, the dielectric needs to meet many critical material and subsequent process integration steps to meet device performance, yield, reliability, and packaging requirements. Some of the main SiCOH dielectric material requirements are:

1. High interfacial strength (adhesion) to dielectric caps such as SiN, SiCN, and composited AlO*x*/SiCO cap. Strong adhesions between various dielectric cap layers are required during and after device fabrication steps, to maintain the integrity of the devices and the reliability of the ULSI chip in packaging [53].
2. Sufficiently high mechanical properties, i.e., a high elastic modulus, especially for chip packaging (or chip-package

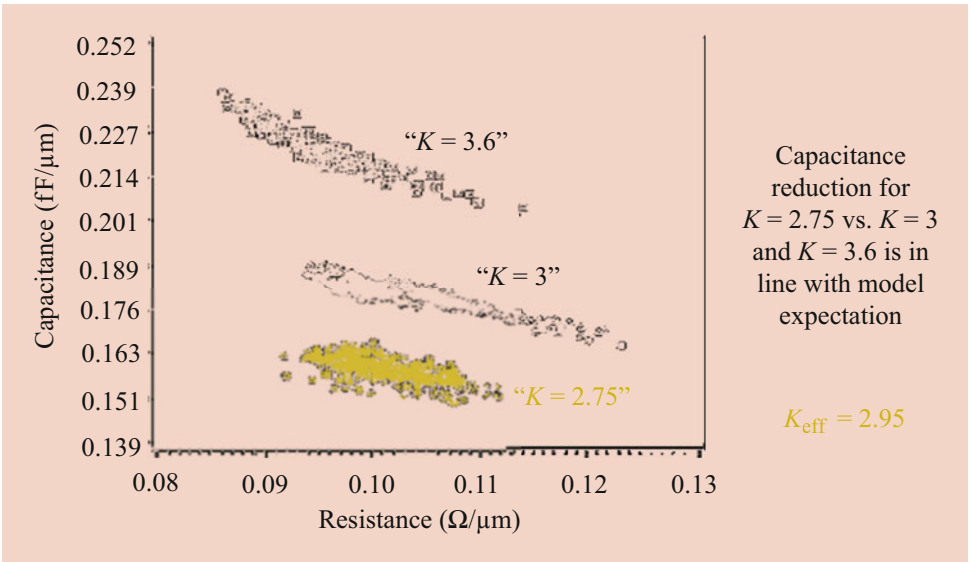

Fig. 5.16 Typical capacitance reduction in a 4× fat wire level of 45-nm BEOL using various low-*k* values for comparison

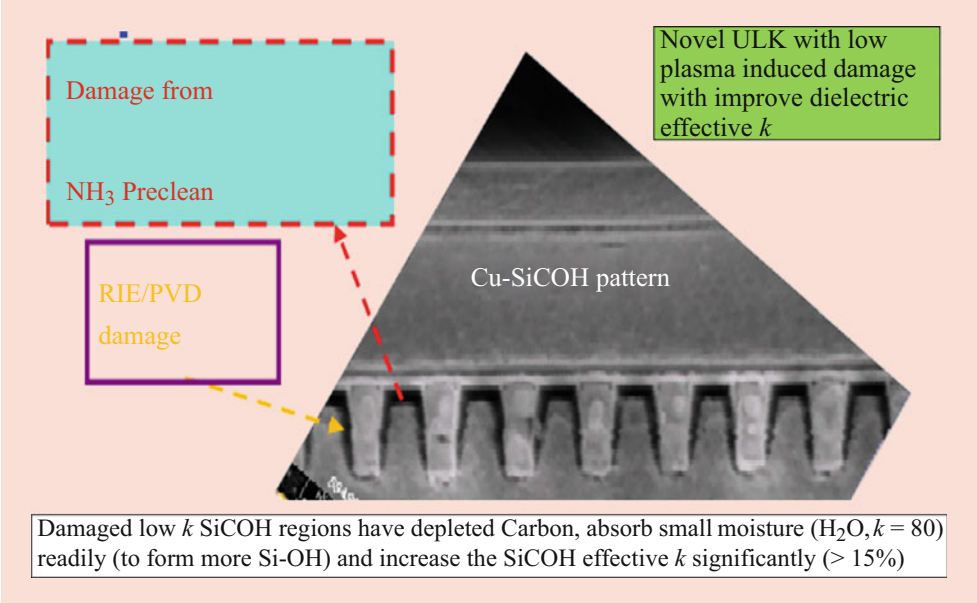

Fig. 5.17 Scanning Transmission Electron Microscopy (STEM) of a Cu/SiCOH nano-size structure showing plasma-induced damage to SiCOH by physical vapor deposition (PVD), reactive ion etching (RIE), and plasma surface treatments such as H_2/O_2 and NH_3 plasma

interaction, CPI), and high hardness for CMP. Low-*k* porous SiCOH films worsen the mechanical properties of SiCOH, due to the decrease in strong Si-O bonding by porosity and/or the reduction of the coordination number due to the replacement of some O with C in case of porous C-Rich SiCOH [41].

3. High resistance to process-induced damage (PID) during fabrication [58]. Other process-induced damages include damage to the ULK caused by CMP, PVD metal deposition, and especially during dielectric etching and photoresist removal by ashing. Figure 5.17 shows the scanning transmission electron micrograph of a sub-40 nm patterned Cu/SiCOH structures that have been highlighted with diluted buffered HF acid wet etching to reveal a typical SiCOH damage. Water moisture in air ambient (H2O, $k \sim 80$) can be absorbed readily into damaged SiCOH region and produces a significant overall increase of *k* (to more than 15%). If the damaged layer is removed by wet etching, then the CD control will be an issue for nano-size metal lines. A good ULK dielectric with good resistance to PID is required in order to enable control of critical dimensions (CD) and to preserve the initial *k* value.
4. Ultralow-*k* porous SiCOH with small pore size (<1.4 nm diameter, <28% porosity) and with minimal interconnectivity is needed to prevent penetration of liners and humidity into the dielectrics and maintain the low-*k* values and device's reliability.
5. Hydrophobicity is necessary to maintain *k* values. Penetration of humidity into the dielectric will increase the dielectric constant. C-rich SiCOH films normally have lower-*k* and higher hydrophobicity [41].

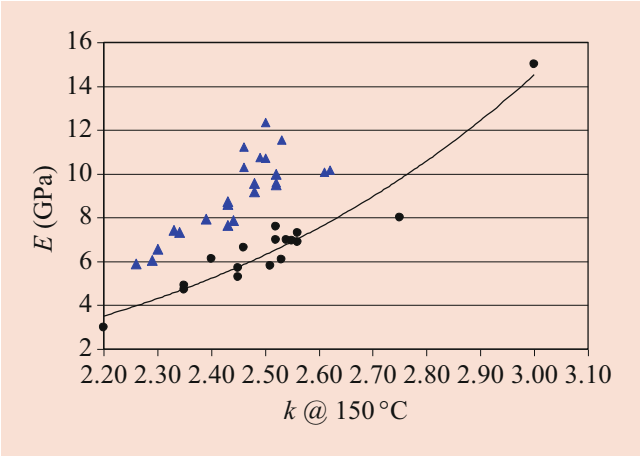

Fig. 5.18 Typical plots of the modulus versus *k* value for various dense SiCOH ($k \sim 3.0$) and porous SiCOH ($k \sim 2.2$–2.8) films, deposited by plasma CVD processing with and without UV. (Ref. [39], reprinted with permission)

All these requirements are quite difficult to achieve at the same time for specific ULK porous SiCOH dielectrics, as in the last decade the dielectric film's thickness reduced, with reducing device size, below 20 nm. For several years, most device manufacturer were stuck with SiCOH with *k* value around 2.5–2.7 range in device manufacturing, even if the lower-*k* pSiCOH can be deposited readily by PECVD process [40, 55–57].

For device integration, it has been very difficult to integrate porous SiCOH film with dielectric constant below 2.4 and porosity above 30%, due to the poorer electrical and weak mechanical and chemical properties of the lower-*k*, high-porosity pSiCOH film. For SiCOH film with dielectric

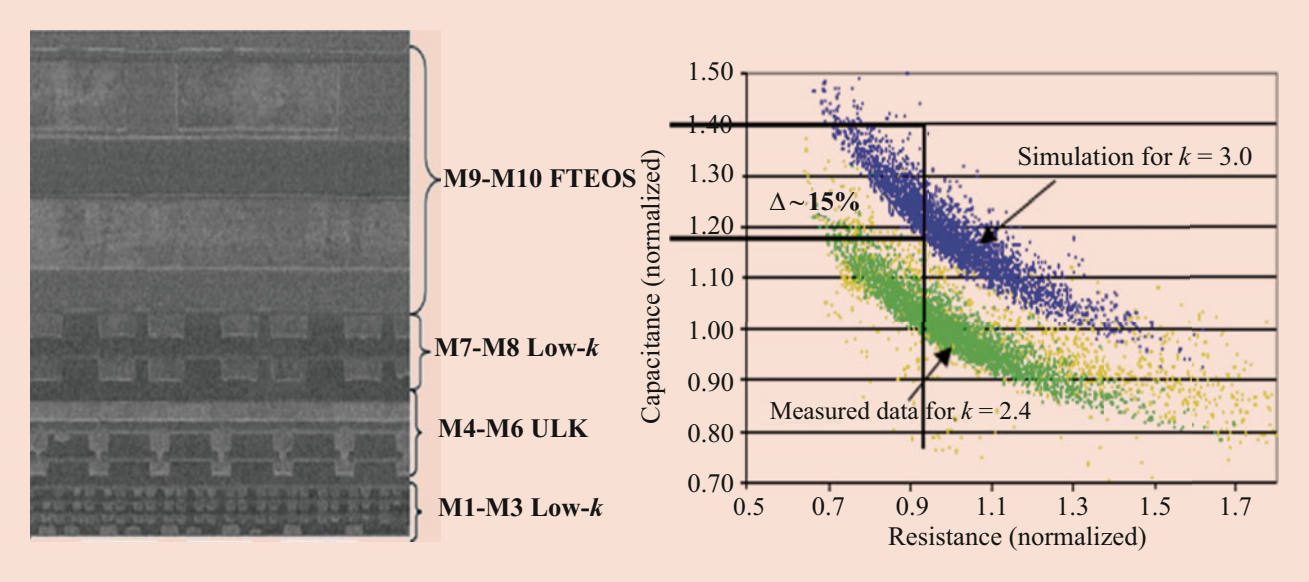

Fig. 5.19 Significant capacitance reduction (~15%) in 45-nm BEOL structures when metal M4-M6 levels change from low-*k* SiCOH ($k \sim 3.0$) to ultra-low-*k* porous SiCOH ($k = 2.4$)

constant in the range of 2.4–2.45, the typical dependence of SiCOH film's modulus vs dielectric constant value is shown in Fig. 5.18. For high-reliability and high-yield semiconductor device manufacturing packaging, high modulus (≥7 GPa) SiCOH dielectrics are preferable. Currently, SiCOH and pSiCOH dielectrics implemented in advanced BEOL semiconductors have been limited to *k* value above 2.5 with modulus higher than 7 Gpa. Our IBM process has used pSiCOH with $k = 2.4$ in device fabrication of 45 nm node BEOL for advanced high-performance power chip [36], to achieve significant capacitance reduction as shown in Fig. 5.19. Plasma CVD C-rich pSiCOH named as OEx SiCOH, deposited with single OMCTS precursor and UV curing, has also been used to deposit lower porosity, high hydrophobicity, and low PID pSiCOH with good device reliability for Cu/low-*k* interconnect [41]. The film has no porogen as a part of the initial deposition at low temperature and RF power to retain the original stable OMCTS precursor backbone bonding. There are no residue porogens to remain in the film after UV cure, and all carbon atoms in this C-rich SiCOH film are bonded in a stable Si-C and Si-CH2-Si bonding structure of the precursor, thus improving the pSiCOH film's stability and PID. Table 5.3 compares the relative PID, carbon, porosity, and other properties of the OEx pSiCOH 2.4 with other pSiCOH film. The overall dielectric reliability and performance are clearly superior to other pSiCOH dielectric with similar *k* value. The new OEx *k* 2.4 film shows comparable or better film properties than the reference $k = 2.55$ and other 2.4 films. The increased carbon content improves the resistance to process-induced damage, this resulting in better TDDB

Table 5.3 Blanket film properties of ultralow-*k* materials

Properties	Film			
	ULK 2.7	ULK 2.55	ULK A (*k* 2.4)	OEx
Dielectric constant	2.7	2.55	2.4	2.4
Porosity (%)	7	14	19.7	20
Pore diameter (nm)	1.1	1.2	1.3	1.3
%C	21.6	23.2	17.2	30
Modulus (GPa)	3	6.64	7.34	7
PID Ratio	0.33	0.57	0.65	0.35

performance over multiple semiconductor nodes. Higher carbon content, mostly incorporated and retained in the bridging bond (Si-CH2-Si), improves the modulus of the film. Apart from reliability benefit, the film retains the capacitance benefit by demonstrating an overall lower integrated *k* value as compared to the SiCOH *k* 2.55 dielectric. Figure 5.20 shows a STEM cross-sectional structure of 7 nm BEOL devices with three thin wires: dual damascene Cu in $k = 2.45$ porous SiCOH, 36 nm pitch with significant capacitance reduction. It is shown that excellent reliability results can be obtained for Cu interconnects with this OMCTS-based pSiCOH 2.45 at these small dimensions [59].

5.2.3 Advanced Dielectrics and Processes for Metal Interconnect

Flowable Gap Fill SiCOH

For low-*k* SiCOH film with good gap fill, flowable gap fill CVD of Lightly porous pSiCOH with $k \sim 2.75$ with

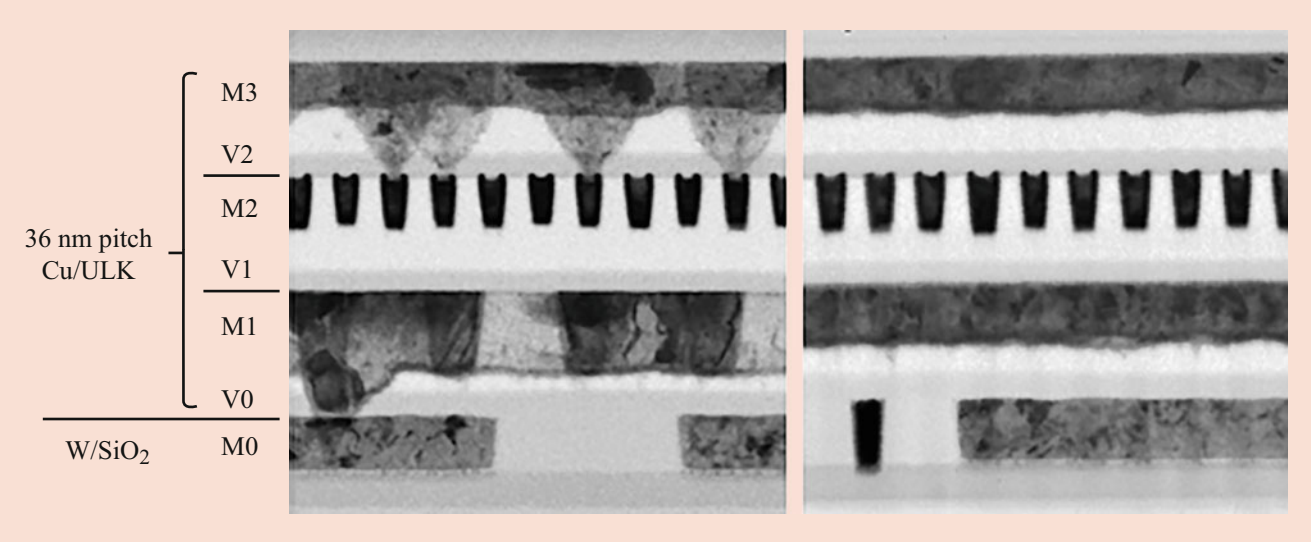

Fig. 5.20 Cross section of a 7-nm BEOL structure with 3 thin wires: dual damascene Cu in ILD $k = 2.45$ porous SiCOH, 36 nm pitch with significant capacitance reduction

excellent gap fill capability was developed for fully aligned via (FAV) structure application 5 nm BEOL and beyond [60]. Figure 5.21 shows typical good fill behavior of FCVD SiCOH 2.75 over high aspect ratio. The film was deposited using cyclic organosilicon precursor like OMCTS and linear precursor tetramethoxyl silane (TMOS) deposited at <100 °C to fill high aspect ratio gap and then UV cured at 400 °C to densify and to enhance cross-linking Si-CH2-Si and Si-O bonding in the structure to improve film's modulus. The UV cure also creates porosity in the film to reduce *k*. Post UV cure flowable low-*k* SiCOH 2.7 dielectrics has higher porosity and higher PID than standard plasma-deposited SiCOH 2.7. Table 5.4 shows the relative comparison between industry plasma CVD SiCOH 2.7 and 2.55 vs FCVD SiCOH 2.78. As deposited, the FCVD SiCOH film has relatively lower carbon concentration, higher porosity, and higher relative PID compared to plasma-deposited film than the sample *k* value. Furthermore, the as-deposited FCVD SiCOH 2.75 film is also inferior to plasma CVD SiCOH 2.7 in terms of dielectric reliability performance. However, the FCVD SiCOH film improves significantly with subsequent processing ion implant and laser annealing [61].

A recent study [61] showed that a UV cure-based silylation process can be implemented at post-etch/strip step to repair the processing damage of Cu/ULK (ultralow-*k* SiCOH ~2.6–2.7) interconnect. This will reduce post processing capacitance by 3.0% and 4.0% at 32 nm and 24 nm line widths, respectively. Also, TDDB lifetime improves by 5 orders of magnitude. The simple UV-based recovery process using in situ plasma preclean of Cu will restore some of the pristine ULK IMD properties and reduce the capacitance in pattern structures. The UV cure-based silylation process can also remove some volatile weakly bonded ULK impurities, smoothening the film's surface roughness, and enhance sur-

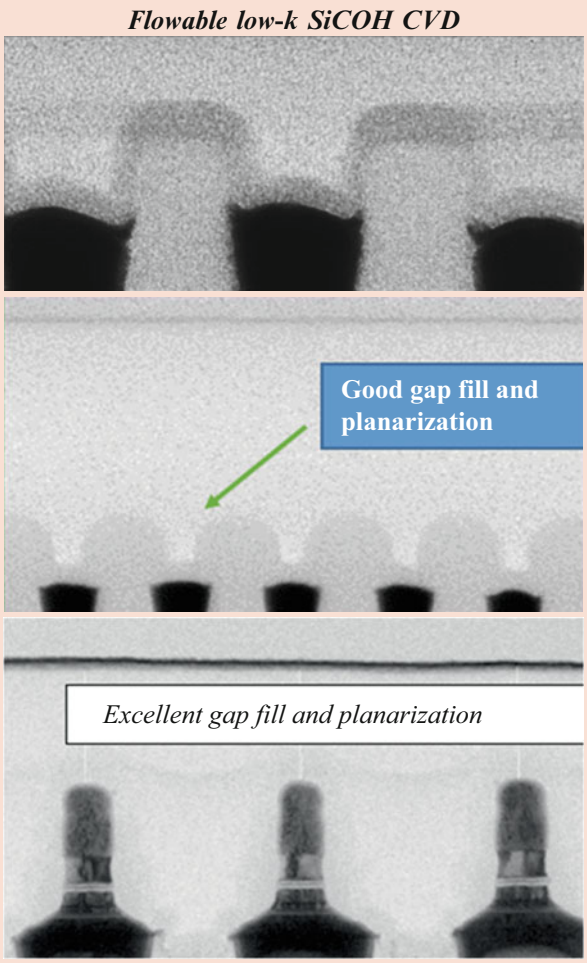

Fig. 5.21 Flowable CVD SiCOH deposited on high aspect ratio structures. All three structures show good gap fill and planarization with FCVD SiCOH 2.75

Table 5.4 Relative dielectric value of laser toughened FCVD SiCOH versus typical industry plasma CVD SiCOH 2.7 and 2.55

Blanket property measured	SiCOH 2.7 (Industry standard)	p-SiCOH 2.55 w/UV	Laser toughened SiCOH 2.6–2.7	
			Laser first	Laser last
k @ 150 °C bulk	2.77–2.85	2.55–2.6	2.6	2.7
Porosity by EP (%)	6.5	18	>10	7
Pore size (nm)	0.7	0.6	0.6	0.6
Relative PID (wet etch resistance of plasma damaged ILD)	*0.13*	*0.17*	*0.13*	*0.165*
Relative atomic % C	32	28	27	27

The PID measurement normalized to relative value. Relative % C does not include hydrogen

face hydrophobicity. This subsequently results in a strong improvement of TDDB and EM in the Cu/low-*k* interconnect structure. This UV-based low-*k* silylation recovery process can be implemented as an RC performance and reliability booster to the conventional damascene Cu/low-*k* integration scheme.

Pinch-Off Deposition Air Gap

Further capacitance reduction is therefore vitally important for BEOL device performance. To further reduce capacitance below SiCOH 2.4, other innovations in device structure and process integration such as air gap are surely needed [63–68]. For BEOL, air gap is one promising approach to reduce capacitance that has widely been published by IBM [63, 64] since early 2007. More significantly, this air gap technology may be the only road map ensuring that effective dielectric constants ≤ 2.0–2.2 can be achieved [69]. Examples of alternate schemes with better capacitance reductions by simpler processing steps have been reported [68]. Air gap technology has also reached manufacturing in the Intel 14 nm technology node [67]. Our recent work [70] presents an overview of material and process technology requirements for FEOL air spacer and BEOL air gap formation using a pinch-off deposition approach. These approaches utilize established dielectric materials and processes such as plasma CVD of SiN, SiCN, SiCOH, and pSiCOH in the formation of the air spacer/air gap. The selection of these dielectric materials and processes has a large impact in the void (gap) dimension and volume. The void dimension and volume in air gap/air spacer structures can be controlled with various dielectric deposition processes and materials to facilitate subsequent process fabrication steps and ultimately to build a robust device with substantial capacitance reduction. Figure 5.22 shows typical pinch-off plasma CVD

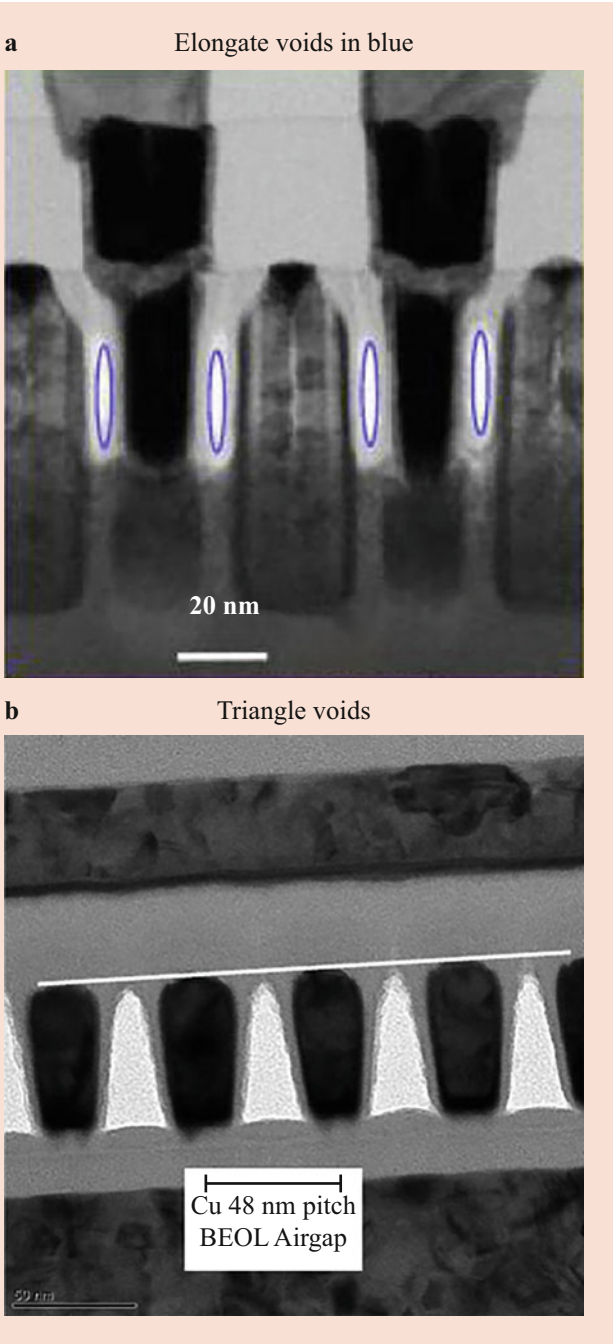

Fig. 5.22 (**a**) Typical pinch-off plasma CVD processes for elongated voids in FEOL gate region of devices and (**b**) triangle voids in BEOL Cu-low-*k* interconnect

processes for elongated voids in FEOL gate region devices (Fig. 5.22a) and triangle voids (Fig. 5.22b) in BEOL Cu low-*k* interconnect. The void's shape, volume, and dielectric material selections have significant impacts in the total effective capacitance of the devices. We successfully implemented a pinch-off deposition process with suitable device integration to produce significant capacitance reduction in both 10 nm FEOL FinFET air spacer and 48 nm pitch Cu-ULK BEOL structures. The capacitance reduction was obtained with improved device performance and without degradation

in reliability. Typical capacitance reductions can be tuned to 15–25%, depending on the air gap depth. For BEOL Cu low-*k* interconnect, a capacitance reduction of ~20% is achieved with no line resistance increase relative to the baseline ungapped process. Additionally, both TDDB and EM reliability are equivalent to those of ungapped controls.

Novel Low-*k* C-Rich SiCN Dielectrics

With device scaling reaching below sub-7 nm and beyond, Cu interconnect extendibility is reaching a limit [69, 70]. Reducing barrier-liner thickness to increase Cu volume for lower R degrades EM performance and dielectric TDDB. Similarly, using a lower dielectric constant *k* (lower capacitance) of pSiCOH below 2.4 material impacts TDDB performance [39–41]. Furthermore, mechanical considerations, plasma-induced damage (PID) integration challenges, pattern collapse, and reliability requirements of pSiCOH materials for future nano fabrication have been a great concern [71–74]. In a recent paper [75], we reported a new class of the plasma CVD of mechanically robust, low-*k* C-rich SiCN, and pSiCN dielectrics with excellent built-in Cu oxidation and diffusion barrier properties that have been developed and evaluated as potential alternative to low-*k* interlevel dielectrics for Cu interconnects [62]. The novel low-*k* dense C-rich SiCN ($k = 3.3$) and lightly porous C-rich SiCN ($k = 2.8$) films have high modulus (E ~> 15–30 GPa) and significantly lower plasma-induced damage (PID) as compared to our current advanced pSiCOH (k ~ 2.4–2.7) dielectrics as shown in Tables 5.5 and 5.6. The excellent Cu diffusion barrier properties of these SiCN dielectrics enable the use of thinner metallic Cu barriers resulting in larger Cu line's volume, reduced Cu metal resistance up to 30%, and overall RC in the sub-50 nm pitch interconnects without TDDB reliability penalty. The high modulus dielectrics also enable high aspect ratio sub-40 nm patterning without pattern collapse. Figure 5.23a–c show the typical dual damascene M2 level Cu-SiCN ($k = 3.3$) dielectric stacks and analysis; specifically (a) STEM of fabricated structure of "5 nm" BEOL metal 2 low-*k* C-rich SiCN-CuMn (0.5% Mn) interconnect with no metal liner. (b) SIMS analysis showing no Cu diffusion (no Cu detected) into C-rich SiCN and the formation of $MnSiO_x$ at interfaces. (c) EDX analysis confirms no Cu diffusion and no significant plasma damage to the dielectric. No copper is detected in the voltage sweep run, SIMS, and EDX analyses performed at

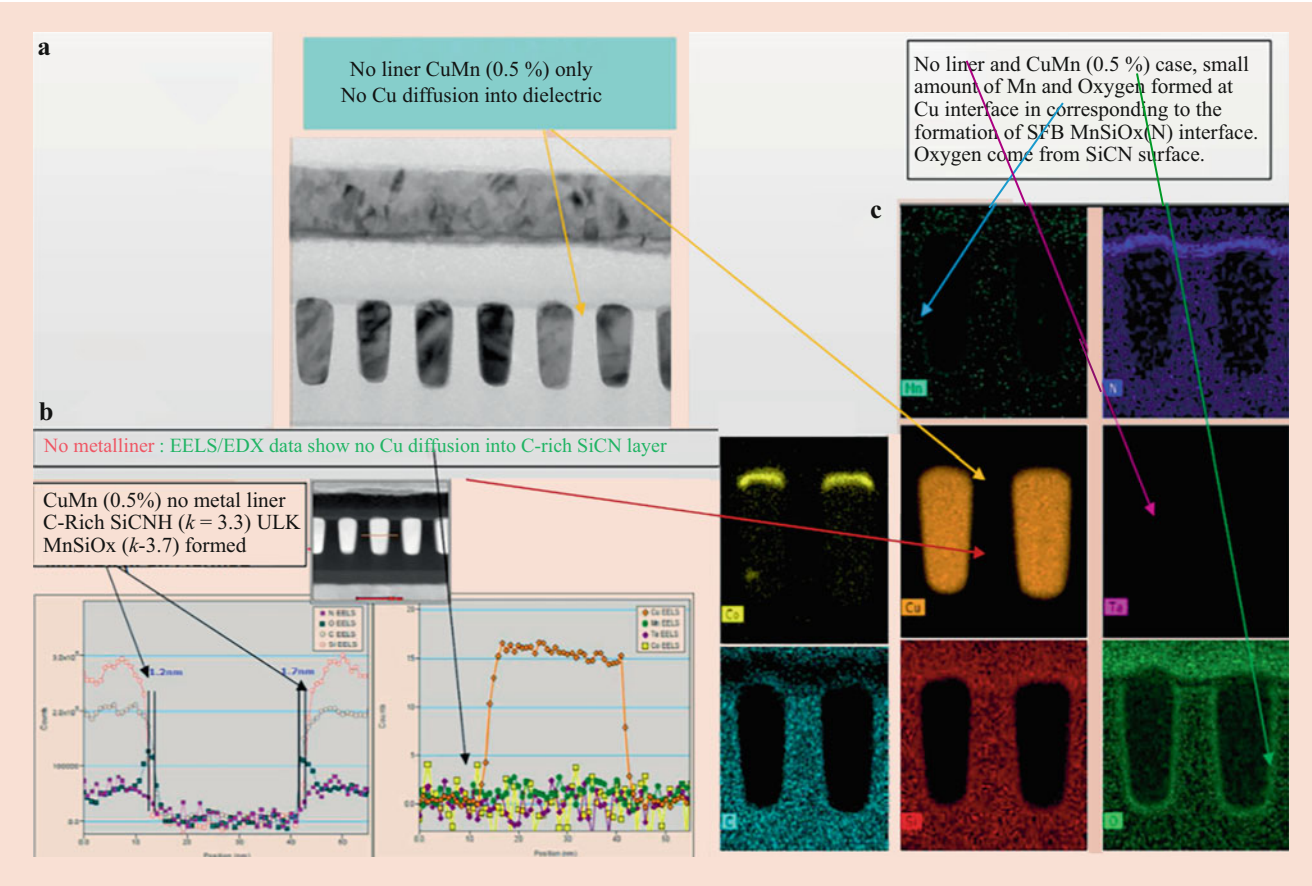

Fig. 5.23 (**a**) STEM of BEOL M2 low-*k*, C-Rich SiCN-CuMn interconnect with no metal liner. (**b**) SIMS analysis showing no Cu diffusion (no Cu detect) into C-Rich SiCN and MnSiOx at interfaces. (**c**) EDX analysis of X-section confirming no Cu diffusion or plasma damage even without metal liner

multiple sites on a wafer fabricated at 36 nm pitch BEOL. Figure 5.24 shows the 48 nm pitch Cu_SiCN3.3 TDDB (5 MV/cm, 125 °C) test result of the M2 structure, indicating robust TDDB breakdown performance even without metallic liner and with substantially thinner liners with thicknesses in the range of 2 and 6 nm. The TDDB data for pSiCOH $k = 2.55$ and $k = 2.45$ were also measured and used as references. No TDDB degradation (leakage performance or yield) as compared to standard pSiCOH dielectric is observed for SiCN with 10% smaller dielectrics spacing. For Cu and low-k dielectric extendibility to sub-5 nm dimension, these robust low-k SiCN dielectrics with ultrathin ≤2 nm metallic liner show promising potential as future dielectric materials for Cu and other metal interconnect.

5.2.4 Summary

We summarize various types of low-k interlevel dielectric materials development k implemented in various technology nodes at IBM development/manufacturing facilities over last 25 years in Table 5.5. This provides a simplified overview. Similar types of low-k interlevel dielectrics have also been used in semiconductor device fabrication over the years.

The search for extremely low-k dielectrics with robust performance properties for nano-device metal interconnects continues as devices reach the sub-5 nm dimension [68]. In a recent publication [76], it was reported that 3 nm thick boron nitride (BN) films deposited by inductive plasma CVD processing have ultralow κ values of 1.78 and 1.16 (close to that of air, $\kappa = 1$), at operation frequencies of 100 kHz and 1 MHz, respectively. The films are mechanically and electrically robust, with a breakdown strength of 7.3 megavolts per centimeter with good cobalt diffusion barrier properties. The measured extreme low-k value of ultrathin films generated some excitement in the low-k dielectric and nano-device community, but the low-k value needs to be confirmed by other measurement. Plasma CVD BN deposited on top of n-type silicon substrates is known to form p-n junctions and produce erroneous k measurements [77]. Our work in the 1990s showed that thick plasma-deposited boron nitride and silicon-boron nitride films are somewhat unsuitable for interlevel dielectric and are unlikely to be suitable for low-k interlevel dielectric for metal interconnect [77–79] due

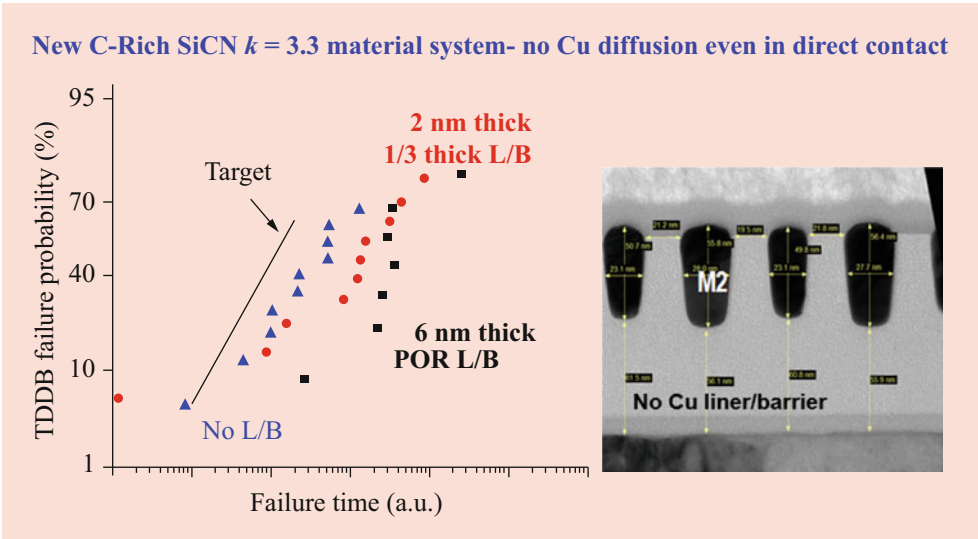

Fig. 5.24 Robust improvement in the Cu diffusion and oxidation barrier properties of the SiCN novel dielectric are demonstrated at sub-50 nm pitch TDDB of Cu (Mn)-SiCN interconnects. The TDDB performance exceeds the desired target over a substantially expanded range (2–6 nm) of metal liner/barrier (L/B) thicknesses

Table 5.5 Physical properties and comparison of novel low-k C-rich SiCN versus advanced p-SiCOH

	Advanced p-SiCOH	Novel low-k C-rich SiCN	
	p-SiCOH	C-rich SiCN	pSiCN
Precursor	OMCTS+UVcure	TMS+NH3+C2H4	DMSCP+NH3+UV
k (@150 for bulk	2.45	3.3	2.8
E (GPa)	8	34	~15–17
%C (by XPS)	28	~50 (without H)	~46 (without H)
Porosity (%)	18	0	~12–13
Blanket PID	0.31–0.35	0.125	0.189
Adhesion to Cu (J/m^2)	4–4.13	>4	>4
Graded layer for adhesion	~5–6 nm	0 (not needed)	0 (not needed)
Cu oxidation	Poor	Good	Moderate

Table 5.6 Summary table for advanced low-*k* dielectric material development since 130 nm technology node [52]

Technology	Lowest *K* BEOL ILD material	Dielectric constant (*k*)	Modulus/hardness (GPa)	Film stress (MPa)	CTE (ppm/C)
130 nm	FTEOS	3.6	60/∼7–9	175	∼0.5 (lit. SIO2)
90 nm	SiCOH 3.0	3.1	15/2.2	35	10.7–11.6
65 nm	Lightly porous SiCOH 2.7 (Air Gap demo)	2.7	8/1.0	47	20
45/32/22/14/10/7 nm	P-SiCOH 2.4 ULK and lightly porous SiCOH 2.7 (Air Gap R&D)	2.4	6–8/∼0.7	∼48–50	14 ± 2
5 nm and beyond (on going R&D)	1. FCVD SiCOH (Gap Fill High AR)	2.75	8/∼0.6	<45	∼14 ± 2 (Est.)
	2. C-rich SiCN/pSiCN (Airgap R&D)	3.3	33/3.0	∼55–65	NA
		2.8	16/1.8	55–65	

to higher-*k* value and moisture absorption during device fabrication. More research and development work are likely to continue for a robust low-*k* dielectric suitable for sub-3 nm device nano-electronic fabrication.

5.3 BEOL Thin-Film Metals

The initial development and continued scaling of copper damascene interconnects have been enabled by the concomitant development of suitable barrier, liner, and seed layers which enable the integration of copper wires into damascene features [80, 81]. When combined, these layers must satisfy multiple requirements: (1) They must provide sufficient adhesion of the copper wiring features to the dielectric, both under reliability and temperature stresses, as well as under the strong mechanical shear stresses which are experienced during chemical-mechanical polishing (CMP). (2) They must serve as diffusion barriers between the copper metal and the dielectric. This capability serves two functions: it prevents copper from diffusing into the dielectric, which would lead to dielectric breakdown or current leakage. It also prevents oxidizing species in the dielectric from migrating into copper, which would compromise conductivity and reliability. (3) They must serve as robust initiation (seed) layers for the electroplating processes which have been traditionally used to fill the wiring features in damascene interconnects. Wherever possible, the demands of scaling and process simplification make it preferable to select materials that can satisfy multiple demands at the same time. We shall review prior developments in this area, including more recent developments that have been driven by the demands of interconnect scaling.

5.3.1 Requirements for Barrier, Liner, and Seed Layers

Prior to the introduction of copper interconnects in the late 1990s, the commonly used metals for back-end-of-line (BEOL) conductors were aluminum for intralevel wires and tungsten for some interlevel via plug applications [82–85]. The development of dual damascene aluminum interconnects later obviated the need for tungsten vias. Both aluminum and tungsten typically used thin, conformal films of titanium (Ti) and/or titanium nitride (TiN) as liner layers, due to their adhesion properties and chemical compatibility with the integrated BEOL process flows.

The development of copper interconnects [86, 87] required an entirely new material set for barrier and liner layers. Titanium was fundamentally unusable as a liner due to its solubility in copper, which results in diffusion of Ti into copper wiring structures when the two metals are in contact. This leaching of Ti into the Cu conductor metal results in monotonic increases in wire resistance ("poisoning") with thermal cycling or current stress. In addition, Ti and TiN both form corrosion couples with copper with some commonly used chemical-mechanical polishing (CMP) slurries, making them unsuitable even in combination with other materials, where the Ti or TiN and Cu layers are not in direct contact.

Tantalum (Ta) and tantalum nitride (TaN) emerged as the leading candidates for use as Cu liners for multiple reasons [80, 81]. Of primary importance is that Ta is not soluble in Cu, so the resistance poisoning effect is absent. There are no corrosion reactions observed between Ta and Cu in the presence of CMP slurries or commonly used wet clean chemistries. The Cu diffusion barrier properties of Ta and TaN are well established, ensuring safe integration of Cu with dielectrics.

One salient concern in the initial development of copper interconnects was adhesion. TaN was seen to have excellent adhesion to silicon dioxide, but adhesion and wettability of Cu seed layers were relatively poor. Conversely, Cu wettability and adhesion on Ta is very good, but Ta adhesion on silicon dioxide was very poor in early studies.

An additional consideration in the selection of tantalum-based liners was the desire to replicate the current strapping redundancy seen with the combination of TiN liners and aluminum conductors that preceded copper. This capability

enables the liner to serve as a parallel conduction path in case of electromigration voiding in the conductor metal, so that the voided point exhibits increasing resistance as a warning of impending failure but does not become a catastrophic "hard" open. Such behavior can be important in signaling impending electromigration failures in applications where reliability is of paramount concern.

In cases where Ta or TaN layers are used separately, such parallel current strapping was not readily possible. Tantalum deposited in thin films deposited on silicon dioxide by magnetron sputtering typically nucleates in the metastable β-phase (tetragonal or hexagonal), with an effective resistivity typically in the range of 150–220 μΩ-cm. Tantalum nitride (TaN) as deposited by reactive magnetron sputtering normally has resistivities of 200 μΩ-cm up to 350 μΩ-cm, depending on the deposition conditions. By contrast, current redundancy for the liner layer typically requires an in-plane resistivity of <50 μΩ-cm, which is only achievable with the body-centered cubic (bcc) α-phase of Ta. This low-resistivity α-phase Ta is stable and naturally occurring but is quite difficult to form when sputtered as a thin film directly on silicon dioxide. Achieving α-Ta formation in thin films sputtered directly on silicon dioxide typically requires some combination of either high temperatures (>600 °C), incompatible with BEOL processing, or extremely low power, low-deposition rate process conditions which typically have poor throughput, uniformity, and step coverage.

One fortunate property of the TaN and Ta system during sputter deposition is that a bilayer deposition on silicon dioxide of TaN first followed by Ta on top results in the nucleation of α-Ta in the top layer under conventional magnetron conditions [80, 81]. When used as a liner for Cu interconnects, this bilayer of TaN on the bottom and Ta on the top thus places the low-resistivity (<50 μΩ-cm) α-Ta in direct interfacial contact with the Cu conductor, enabling the redundant current strapping capability for high-reliability applications. The Ta/Cu interface is also optimal for liner-conductor wettability and adhesion, while the TaN layer next to the silicon dioxide insulator is optimal for adhesion at that interface.

A further advantage of the TaN/Ta bilayer as a Cu liner is that TaN can be reactively sputtered in the same chamber as Ta, with the only difference in the process conditions being the simultaneous flowing of nitrogen and argon at the same time as sputter gasses. Once the TaN deposition is complete, the Ta can be deposited by shutting off the flow of the nitrogen and continuing the sputter process with argon only. In production magnetrons, the sputter yields and binding energies of TaN vs Ta are similar enough that the transition between TaN and Ta happens without hysteresis, i.e., the same target voltage is achieved regardless of whether the nitrogen flow is increasing or decreasing. This lack of hysteresis in the reactively sputtered TaN/Ta system means that the bilayer structure can be deposited in the same chamber repeatedly under production conditions, unlike other reactively sputtered liner metals, such as Ti and TiN. The α-Ta layer has been observed to be formed with only ~20 Å of TaN underneath. Moreover, very high step coverage can be obtained with TaN/Ta layers, owing to the low sticking coefficient and multiple-bounce kinematics inherent in the sputtered TaN and Ta depositions. Following its initial adoption into production use for copper interconnects, multiple generations of directional, ionized sputter sources for the TaN/Ta system have been developed by the semiconductor tooling industry. A summary of the advantages of the TaN/Ta liner system over other candidate materials is shown in Table 5.7 [80, 81].

The standard method of filling BEOL interconnect structures with copper has been electrolytic plating using copper sulfate chemistries with proprietary additives. The initiation of electrolytic copper plating requires a copper seed layer [86, 87]. High-quality, void-free filling of wiring structures requires the copper seed layer to be continuous over the field area (top surface of the wafer) and all along the sidewalls and bottoms of trench (horizontal, in-plane) and via (vertical level-to-level) structures. For dual damascene structures, the maximum aspect ratio (height/width) of the completed, planarized wiring structures is typically on the order of 2:1–4:1 and can be roughly twice has high for unplanarized structures during the barrier/seed layer deposition and plating steps. Directional sputtering of copper is needed to achieve sufficient seed layer coverage over all surfaces of unfilled structures. As a result, process and equipment development for copper sputtering has been a major focus in the semiconductor tooling and manufacturing industries since the inception of copper interconnects. At advanced ground rules, barrier and seed layer processes and the associated electroplating chemistries and waveforms often require co-optimization in order to achieve reliable, high-yielding copper interconnects. In the next section, we will discuss tooling and typical process flows for traditional copper barrier and seed layer deposition.

5.3.2 Sputter Deposition Tooling for Barrier, Liner, and Seed Layers

Sputter processing is one of the most widely used processes in thin-film fabrication. Sputter deposition is a method of depositing thin films onto a substrate by accelerating ionized gas atoms into a target made of source material for the film. The sputter gas is usually argon for its relatively high mass, low cost, and chemical inertness, but other noble gasses or reactive gasses such as nitrogen and oxygen are also used for specific applications. If the sputter gas ions have kinetic

Table 5.7 Selection criteria for barrier/liner layers used in the introduction of Cu interconnects [80, 81]

Attribute ↓	Cr	TiN	TiN/Ti	Ti/TiN	TiN/Ta	TaN	Ta (β-Ta)	TaN/Ta	TaSiN	WNx
Cu barrier	✗	✓	✓	✓	✓	✓	✓	✓	✓	✓
Adhesion to ILD	✓	✓	✓	✓	✓	✓	✗	✓	✓	✓
Cu on liner adhesion	✓	✗	✓	✗	✓	✗	✓	✓	✗	?/✗
Liner on Cu adhesion	✓	?	?	✓	?	✓	✓	✓	✓	?
Low-in-plane resistivity	✓	✗	✓	✓	?	✗	✗	✓	✗	✗
Solubility in Cu	✓	✓	✗	✓	✓	✓	✓	✓	?	✓
CMP, Cu corrosion	?	✗	✗	✗	✗	✓	✓	✓	✓	?
Single-chamber	✓	✓	✗	✗	✗	✓	✓	✓	✓	✓
Via res. (thru-resistivity)	✓	✓	✗	?	✓	✓	✓	✓	✓	?
Cu interfacial res.	✓	✓	✓	✓	✓	✓	✓	✓	✓	?
Thermal stability	?	✓	✗	✗	✓	✓	✓	✓	?	✓
Stress/cracking	✗	✓	✓	✓	✓	✓	✓	✓	✓	✓
Step coverage	?	✓□♦	✓♦★	✓♦★	✓♦★	✓□♦	✓♦	✓♦★	✓	✓□
Final selection	✗	✗	✗	✗	✗	✗	✗	✓	✗	✗

✓ Satisfactory, ✗ Unsatisfactory, ? No data/not investigated
□ CVD or ALD available, ♦ ionized PVD available, ★ ionized PVD available for nitride & pure metal; CVD/ALD for nitride only

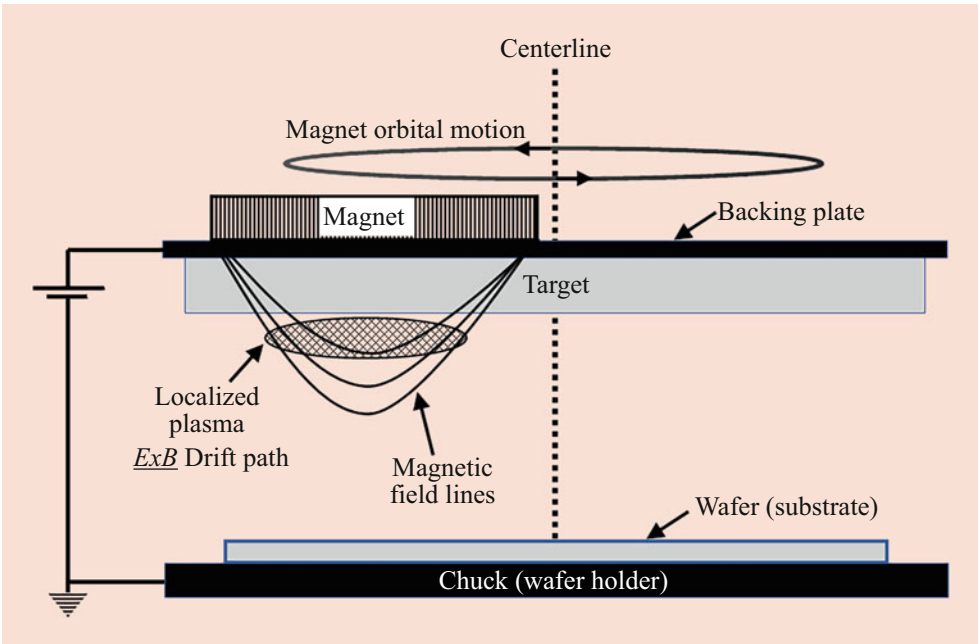

Fig. 5.25 Cross-sectional schematic of a planar magnetron. The magnet moves across the back of the target in an orbital motion so that the plasma is localized near the target surface (see text)

energies in the correct range, atoms of the source material will be ejected from the target. The substrate is positioned so that the ejected target atoms are collected on it and then nucleate and coalesce into a thin-film layer of the target material. The same mechanism can be done in reverse, with ionized gas items being accelerated toward the substrate, resulting in ejected atoms from the substrate depositing onto the chamber shielding. This type of process is called sputter etching, and it can be used for surface cleaning and material removal. An in-depth discussion of the fundamentals of sputter processing is beyond the scope of this chapter, but the interested reader is referred to references [88–94] for a more thorough treatment of the subject matter. Sputter processing falls under the broader category of deposition methods known as physical vapor deposition ("PVD"), which can also encompass evaporation. In modern semiconductor fabrication, sputter processing is the only PVD method used in mass production, so the terms PVD and *sputtering* are effectively interchangeable in this context.

For deposition of metallic liner and seed layers for copper interconnects, modern semiconductor manufacturing relies on DC magnetron sputter chambers which process one wafer at a time. A simplified schematic is shown in Fig. 5.25 for illustration. The magnetron is a rotating mechanism which sweeps a powerful permanent magnet in regular orbits across the backside of the sputter target. Magnetrons are designed so that the magnetic field from the permanent magnet keeps the free electrons liberated during argon ionization confined

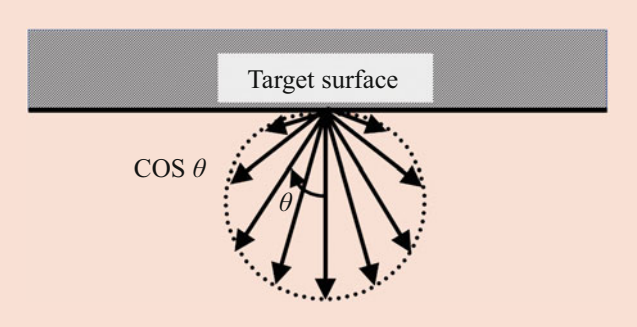

Fig. 5.26 Illustration of the cos θ emission distribution from the target surface. When sputter gas ions impact the target, atoms are ejected from the target in a spatially broad distribution of velocities, with the velocity being proportional to cos θ

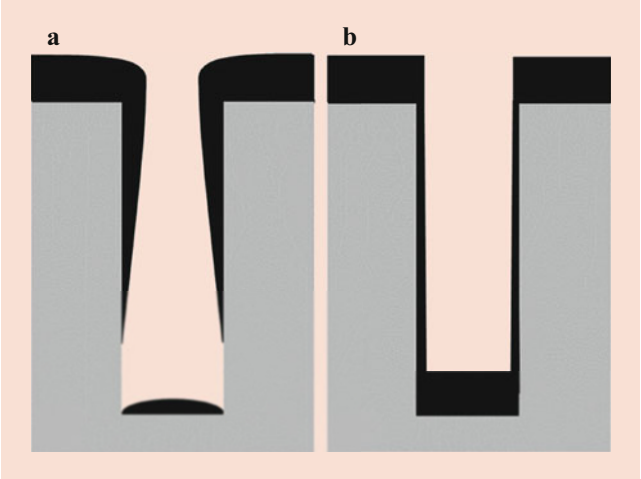

Fig. 5.27 Schematic illustration of sputter deposition coverage on a high aspect ratio feature (**a**) with an uncollimated flux (**b**) with collimation

near the target surface. With the magnetic field lines running parallel to the target surface, free electrons travel in cycloidal orbits along the field lines, due to the $E \times B$ drift force, and can ionize multiple sputter gas atoms by collisional ionization. This magnetic confinement enables the free electrons to make multiple orbits of the magnetron and thereby maintain a high plasma density and rapid sputter deposition rate.

When the sputter gas atoms are ionized, they are accelerated into the target by the naturally occurring plasma potential near the target surface (cathode fall), causing target atoms to be ejected. The atoms are ejected from the target in a spatially broad distribution of velocities, with the magnitude of the velocity being approximately proportional to cos θ, where θ is the angle of the atom's velocity relative to the normal from the target surface (see Fig. 5.26). The actual velocity distribution my deviate somewhat from a pure cos θ distribution, depending on the sputter gas energy and target material, but the overall result nevertheless is that sputter deposition usually results in a broadly distributed flux of metal atoms with weak directionality.

For applications where there is little or no topography on the substrate, a nondirectional flux of sputtered atoms is often perfectly acceptable and might even be desirable for depositing thicker layers at a rapid rate. However, barrier/liner/seed applications for copper interconnects typically require a very high degree of conformality on all the surfaces of damascene features, which will often have aspect ratios >4:1 during the metallization process steps. Minimum thickness requirements of ~15–20 Å are typical to ensure sufficient barrier coverage for films like TaN, Ta, and Cu seed. Given these demanding constraints, sputter deposition of barrier/liner/seed layers like TaN, Ta, and Cu typically requires a very high degree of directionality in order to guarantee conformal coverage of the layers.

The need for directional sputter deposition in barrier/liner/seed applications is illustrated schematically in Fig. 5.27a, b. As shown in Fig. 5.27a, for high aspect ratio damascene features with vertical sidewalls, the off-normal flux of sputtered atoms from uncollimated deposition results in significant buildup of sputtered material on the top corners of damascene features. The overhang from this thick accumulation of deposition at the corners ("bread loafing") results in shadowing of the bottom sidewalls of the features and minimal coverage on the bottom corners. This bread loafing phenomenon is more pronounced in sputtered materials with a high sticking coefficient, such as Cu, and is less pronounced in materials with a low sticking coefficient, such as Ta and TaN, which can undergo multiple bounces that result in more uniform coverage. In contrast, Fig. 5.27b illustrates the advantages of collimated sputter deposition for high aspect ratio features. The reduction of off-normal sputtered atom flux results in less overhang and shadowing of the sidewalls, enabling better coverage of the bottom surface, sidewalls, and corners.

Several methods have been developed and refined by the semiconductor tooling industry to enhance the directionality of sputter deposition for damascene liner applications. Figure 5.28 shows a generic magnetron diagram with uncollimated flux from the target. The simplest means of increasing the directionality of the sputtered atom flux is to increase the target-to-substrate spacing, a configuration sometimes referred to as "long throw" PVD. By moving the target and substrate further apart, the substrate subtends less solid angle relative to the target, which has the effect of filtering out off-axis sputtered atom flux. The remaining flux is therefore more directional than with a smaller target-substrate spacing. The use of "long throw" PVD has several limitations that limit its extendibility. As the target-substrate distance increases, the center-edge uniformity of the sputter deposition will be adversely affected, owing to the size limitations of

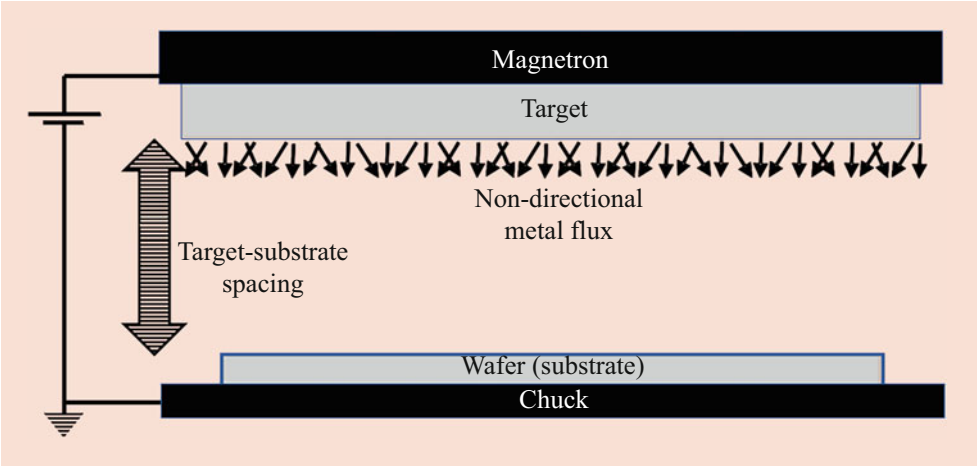

Fig. 5.28 Cross-sectional illustration of a sputter source illustrating the adjustment of target-substrate spacing to increase directionality through directional selection. At longer spacings, the wafer subtends a smaller solid angle of the target flux, resulting in a more directional deposition onto the wafer

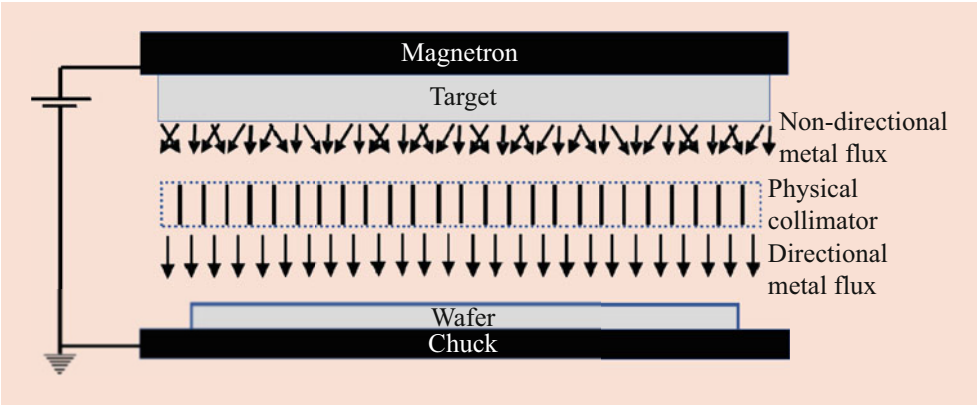

Fig. 5.29 Schematic illustration of a directional sputter deposition source using collimation. The collimator is positioned in between the target and the substrate and is typically a metal honeycomb structure fabricated from sheet aluminum or stainless steel

the target. Even if the target could be enlarged indefinitely, the normal operating pressure of modern PVD discharges is at minimum ~0.1 mTorr or higher. At these pressures, the mean free path for gas atom collisions is ~10–20 cm, so that scattering of the directional flux off the ambient sputter gas negates the collimation effect of the long throw geometry [91–93, 95, 96].

One method of filtering out off-normal sputtered atom flux that avoids the pitfalls of long throw PVD is to use a physical collimator in between the target and substrate [95–97]. A schematic diagram is shown in Fig. 5.29. A physical collimator is just a continuous sheet of tubes that span the sputter chamber below the target and physically filter out off-axis sputtered atoms while maintaining a close target-substrate spacing. In practice, the "tubes" are just an array of honeycomb-shaped structures fabricated from a sheet metal like stainless steel or aluminum. The collimation effect can be increased or decreased by adjusting the aspect ratio (height/diameter) of the collimator cells. Typical collimator heights might be on the order of 1–2 cm, with a lateral cell dimension of ~1 cm, resulting in an aspect ratio of 2:1. The effect of collimator aspect ratio of the angular filtering of sputtered flux is discussed in more detail in [90]. One disadvantage of physical collimators is that the off-axis flux deposits on the top and sidewalls of the collimator, creating a buildup of material over time that obstructs deposition and can also increase the effective aspect ratio of the collimator. This phenomenon results in a steady decline in deposition rate over time, which means that the deposition time must be continually adjusted upward so as to keep a constant deposition thickness on the substrate. Sputter tool vendors will typically have software applications to do the deposition time adjustment automatically once the deposition rate decline is calibrated. It is not unusual for collimators to be replaced as a preventive maintenance measure in the middle of the target and shielding life, while the rest of the shielding and the target continue to end-of-life after the collimator replacement. Collimators can also be subject to significant heating in high deposition rate applications, which can be mitigated by water cooling of the collimator holder.

While collimators are still used in some advanced PVD applications, the technique that offers the most control over liner and seed layer coverage on damascene features is ionized PVD [98–101]. A commonly used ionized PVD configuration in BEOL liner and seed layer deposition is shown schematically in Fig. 5.30. In this configuration, metal atoms are ejected from the target using a magnetron in the normal manner. Argon sputter gas flows are typically set to achieve

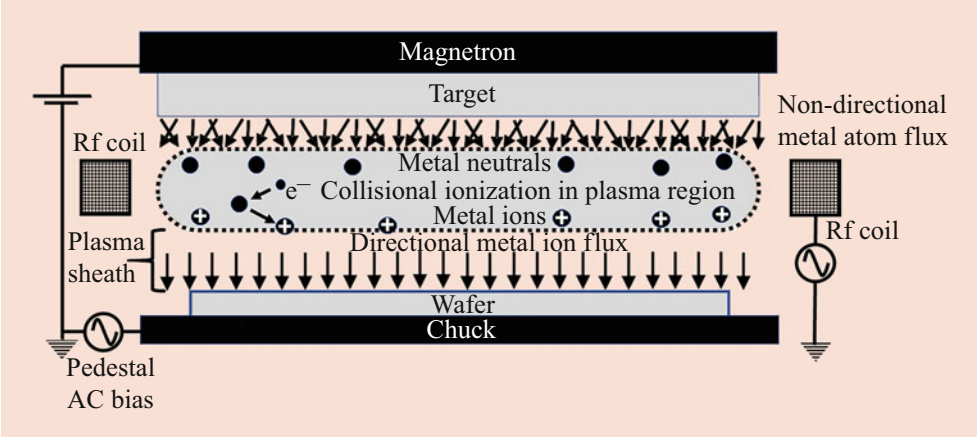

Fig. 5.30 Schematic illustration of a typical sputter source for ionized sputter deposition. The RF coil encircles the source and is used to create an inductively coupled plasma between the target and the substrate (wafer)

pressures in the range of ~1–10 mTorr. A secondary argon-ion plasma is ignited in the space between the target and the substrate, using radiofrequency coils driven at 13.56 MHz, to create an inductively coupled plasma with densities typically greater than 10^{11} cm^{-3} As the sputtered metal atoms traverse the secondary plasma region, they are thermalized by collisions with the argon sputter gas and ionized by collisions with free electrons in the plasma. The collisional ionization efficiency can be quite high, owing to the relatively low ionization energies of typical sputtered metals (<8 eV) relative to the ionization energy of the argon sputter gas (15.8 eV). Once the ionized metal atoms traverse the plasma region, their positive charge causes them to be accelerated toward the substrate. The acceleration of the ionized metal species in the plasma potential provides a strong collimation effect, which is usually augmented by an externally applied AC wafer bias to the substrate. This ionized collimation effect can be achieved with close target-substrate spacing and without interposing a physical collimator, enabling more control over uniformity and stability in deposition rate. Further enhancements to the ionized metal flux density and uniformity can be achieved with magnetic fields generated using electromagnets mounted external to the chamber.

It should be noted that commercially available PVD systems for liner and seed layer depositions will sometimes combine more than one of the collimation techniques discussed here. Additionally, other configurations for ionized PVD have been used commercially, though they are less common. Optimization of ionized PVD for advanced technology nodes is an area of continuous research and development for semiconductor tooling vendors.

5.3.3 Barrier/Liner/Seed Process Sequences and Enhancements

Now that we have reviewed standard techniques for directional deposition of BEOL copper barrier seed layers, we shall review how these techniques are typically used in deposition sequences for high-volume manufacturing. Figure 5.31a is a schematic illustration of a damascene interconnect structure which is incoming to barrier/liner/seed layer deposition. The trench structure is used for intralevel (within-level) signal and power transmission. The via performs the same functions for interlevel (between-level) signals and power transmission, as indicated by the exposed contact to the prior level metal.

In modern semiconductor manufacturing, the deposition of damascene barrier, liner, and seed layers for copper interconnects occurs in single-wafer process chambers which are clustered together on the same ultrahigh vacuum mainframe [92, 93]. Inside the tooling mainframe, wafers are moved from one single-wafer process chamber to another robotically, without breaking vacuum. After the wafer is introduced into the vacuum tool, the unfilled damascene structure (Fig. 5.31a) is subjected to a "degas" step for desorption of water and other oxidizing species which might have been absorbed into or on to the surfaces of the dielectric. Subsequently, the wafer will typically be moved to a preclean chamber for a reactive clean using a hydrogen plasma to reduce copper oxides on the exposed metal contact from the layer below. Historically, physical sputter etching using argon-ion plasmas has also been used for surface cleaning, but sputter etching is typically too damaging to low-*k* dielectrics to be used in technology nodes smaller than 45 nm.

Once the degas and surface cleaning steps are complete, the wafer is moved to the PVD TaN/Ta deposition chamber. Ionized PVD deposition, using a source like that depicted in Fig. 5.6, has been used for TaN and Ta barrier layers going back many technology nodes. The TaN layer is deposited first, as indicated in Fig. 5.31b, since it has the higher adhesion to the dielectric, has better barrier properties than Ta, and promotes nucleation of the low-resistivity alpha-phase Ta on top. The TaN layer is deposited reactively by flowing both argon and nitrogen gasses during the deposition. Once the TaN deposition is complete, the Ta deposition takes place by switching off the nitrogen flow so that a pure Ta layer is

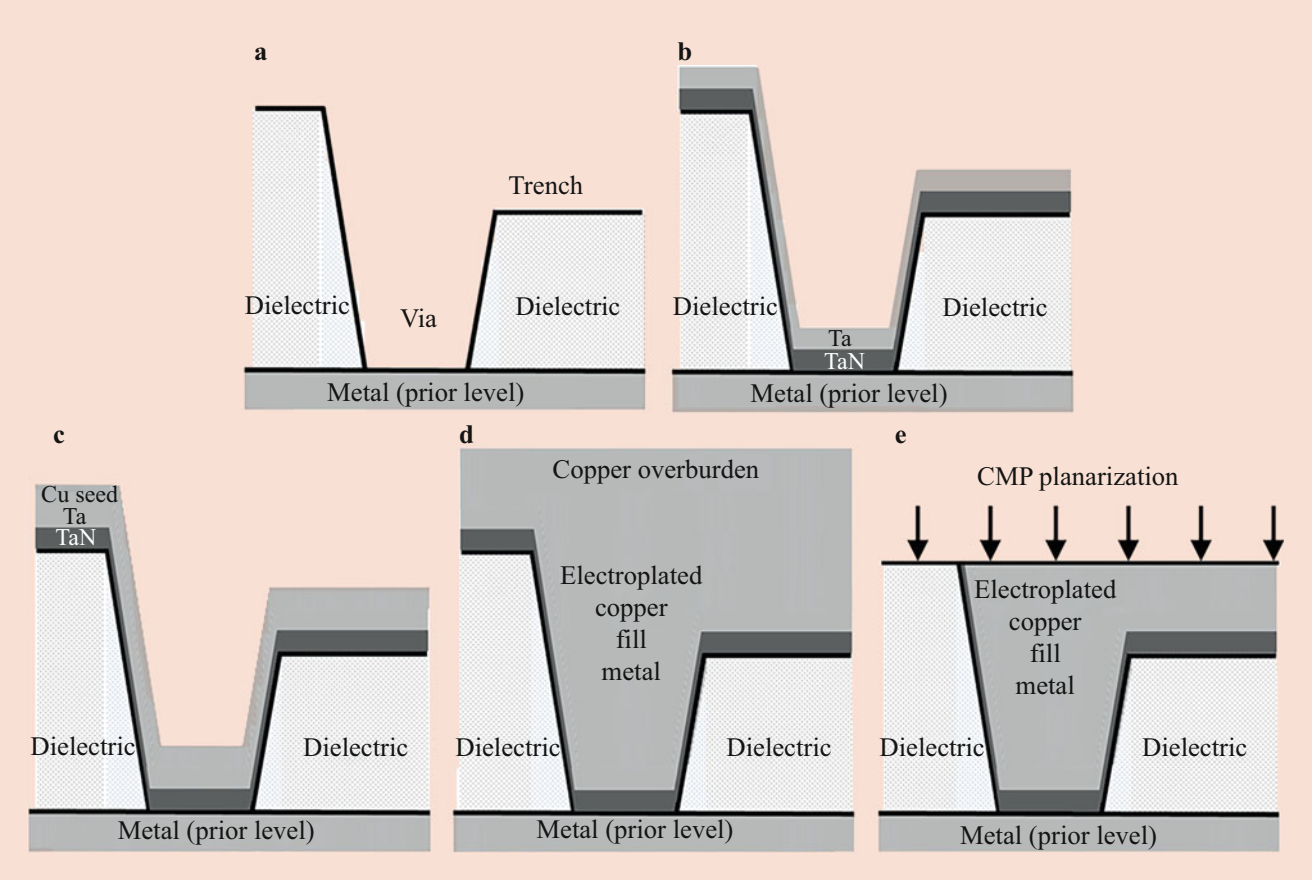

Fig. 5.31 (**a**–**e**) Typical deposition sequence for barrier/liner/seed process sequence used in copper damascene metallization, with subsequent plating (**d**) and CMP (**e**) steps added (see text)

deposited, using only argon as the sputter gas. The result is that the Ta liner layer is deposited conformally on top of the TaN barrier layer, as shown in Fig. 5.31c [80, 81, 102–108].

The final deposition process in this clustered sequence is the deposition of the copper seed layer, which is also done by ionized sputtering. The copper seed layer has critical requirements: it must be sufficiently thick so that even the thinnest areas of coverage (~20–30 Å inside small features) carry adequate plating current inside the feature and serve as a nucleation layer for electroplated fill. In the field area (top surface), it must be thick enough to distribute plating current evenly over the full surface area of the wafer from the wafer edges, where the plating current contact is made. Due to the higher sticking coefficient of copper, it is more prone to the "bread loafing" effect described earlier. Copper, like a handful of other metals such as silver and gold, is capable of sustaining a self-sputtering plasma without using argon as a sputter gas once the plasma has been ignited. This "self-ionized" sputtering has been used for copper seed layer deposition for several technology nodes [109–113]. In self-ionized sputtering, the plasma is typically ignited at low power with argon flowing, but the argon is shutoff once ignition is achieved. Copper atoms, which have an ionization potential (7.7 eV) roughly half that of argon (15.8 eV), have sufficiently high sputter yield (>2.0) that a self-ionized plasma of copper atoms can be sustained in the absence of argon sputter gas. In practice, a negligible argon flow will be present between the cooled wafer chuck to the wafer backside for temperature control. With self-ionized sputtering, the bias power applied to the wafer can be used to adjust the directionality and resputter properties of the copper atom flux at very low process pressures of <1 mTorr. Low bias powers will result in a less directional copper deposition which gives poor coverage in high aspect ratio features but a higher deposition rate on the top surface, similar to Fig. 5.27a. High bias powers will result in very directional deposition with high bottom surface coverage inside high aspect features, similar to Fig. 5.27b. Due to the high sputter yield of copper, the high bias powers come with the trade-off that high copper-ion energies can result in a net etching of copper on the top surface due to copper-on-copper collisions, which will resputter copper from the top surface onto the shielding. In

practice, self-ionized copper seed depositions typically use some combination of a low-bias initial step combined with a high-bias second step to achieve sufficient coverage both in the field area and inside high aspect ratio features.

The schematic illustration in Fig. 5.31c shows the result of the completed deposition sequence, with the TaN, Ta liners, and Cu seed layer coating the damascene feature without vacuum break. Once the wafer is vented to atmosphere, it will move to the electroplating sector to fill the structure with copper, with the PVD Cu seed layer deposited here serving as the plating initiation layer. Following Cu plating fill and overburden deposition (Fig. 5.31d) and CMP planarization (Fig. 5.31e), the finished damascene level is typically deposited with a CVD $SiC_xH_yN_z$ dielectric cap layer for hermeticity and is moved on for the next-level build.

Copper-Alloy Seed Layers

The process technologies described above have been scaled successfully from the introduction of copper interconnects at the 220 nm node down to nodes in the 45–28 nm range. At line widths in the range of 100 nm and smaller, a significant limitation on electromigration performance arises due to the need to suppress Cu atom diffusion along the top-surface interface between the copper and the CVD $SiC_xH_yN_z$ dielectric capping layer.

One advance that has been particularly successful in enabling scaling of Cu interconnects below the ~100 nm dimension is the introduction of Cu-alloy seed layers. With Cu-alloy seed layers, the conventional ultrapure Cu target (typically 99.99% pure or higher) is replaced with an alloy target containing a minority-alloy component, typically Mn or Al in a concentration range of <1%, with the remainder ultrapure Cu [114–122]. The minority alloy is selected for several key properties: it must have an energetically favorable reaction with oxygen so that its oxide forms more readily than does SiO_2. It must be soluble in copper, and it must diffuse readily through copper during standard BEOL process heating cycles. In addition, there must not be any traces of oxygen within the copper interconnects, such as those found with CVD or ALD films deposited using organometallic precursors. When these conditions are satisfied, the minority-alloy component will exhibit a "self-capping" behavior, in which the minority-alloy atoms diffuse through the copper and form a chemical bond with the cap during the cap deposition. This top-surface interfacial layer promotes adhesion between the dielectric cap and the top surface of the copper conductor and has been proven to boost electromigration performance by impeding copper diffusion along the copper-capping layer interface. A schematic illustration of the alloy seed self-capping process is shown in Fig. 5.32a–d. Images from TEM/EELS/EDX analysis which illustrate the self-capping phenomenon are shown in Fig. 5.33.

Wetting Layers for Copper Liner Applications

When first introduced into the semiconductor industry, copper interconnects relied on the PVD TaN and Ta barrier/liner layers described above. With the progression of copper interconnect scaling to feature dimensions smaller than 40 nm, the need for an enhanced liner that would enable copper gap fill at smaller dimensions has become critically important.

The most critical area for improvement for copper liners is the wettability of the copper seed on top of the liner layer. Wettability is the property of the liner surface that enables a copper seed layer to coalesce into a continuous film when deposited on top of the liner. A liner with improved wettability will enable the copper seed layer to coalesce into a continuous layer at a thinner copper thickness than would be the case with a liner with poorer wettability. Improved wettability liners will thus enable thinner copper seed layers to be deposited on small-dimensioned features, with concomitant reduction in seed layer overhang ("bread loafing") and improved feature fill with copper plating. Many everyday phenomena exhibit analogous behaviors, such as the dewetting of water on a hydrophobic surface (poor wettability). A common example is the "beading up" of water on a freshly waxed automobile finish. In contrast, good wettability is illustrated by the phenomenon of water flowing off a hydrophilic surface in continuous sheets, as in the case of an unwaxed automobile finish.

Research on BEOL liners with improved wettability relative to Ta dates back to the early 2000s. Fundamental studies of alternative candidates for copper liner applications have been conducted by Shimogaki et al. [123–125]. In these experiments, the surface wettability and adhesion strength of different copper/liner interfaces were measured by depositing thin copper layers on top of different liner films and assessing the agglomeration and dewetting behavior of the copper following thermal cycling. The wetting angles of the copper films on the different liner candidates were then measured using electron microscopy. The wetting angle data was used to extract the adhesion strength of the copper liner interface using the Young-Dupré equation. These studies found the adhesion strength of the Cu/Ru and Cu/Co interfaces to be in the range of 2.8–2.9 J/m^2, a significant improvement over the Cu/Ta interface adhesion strength of 2.0 J/m^2 [124]. Some correlation can be seen between higher Cu/liner adhesion and smaller lattice mismatch between the liner material and crystalline copper [123].

Cobalt and ruthenium have the additional advantages that they both are insoluble in copper and can be deposited using commercially available CVD (chemical vapor deposition) chemicals and tooling. The CVD deposition method is more conformal than the directional PVD deposition methods used to deposit TaN and Ta. They also have resistivities similar to alpha-Ta, although their poor barrier properties and adhesion

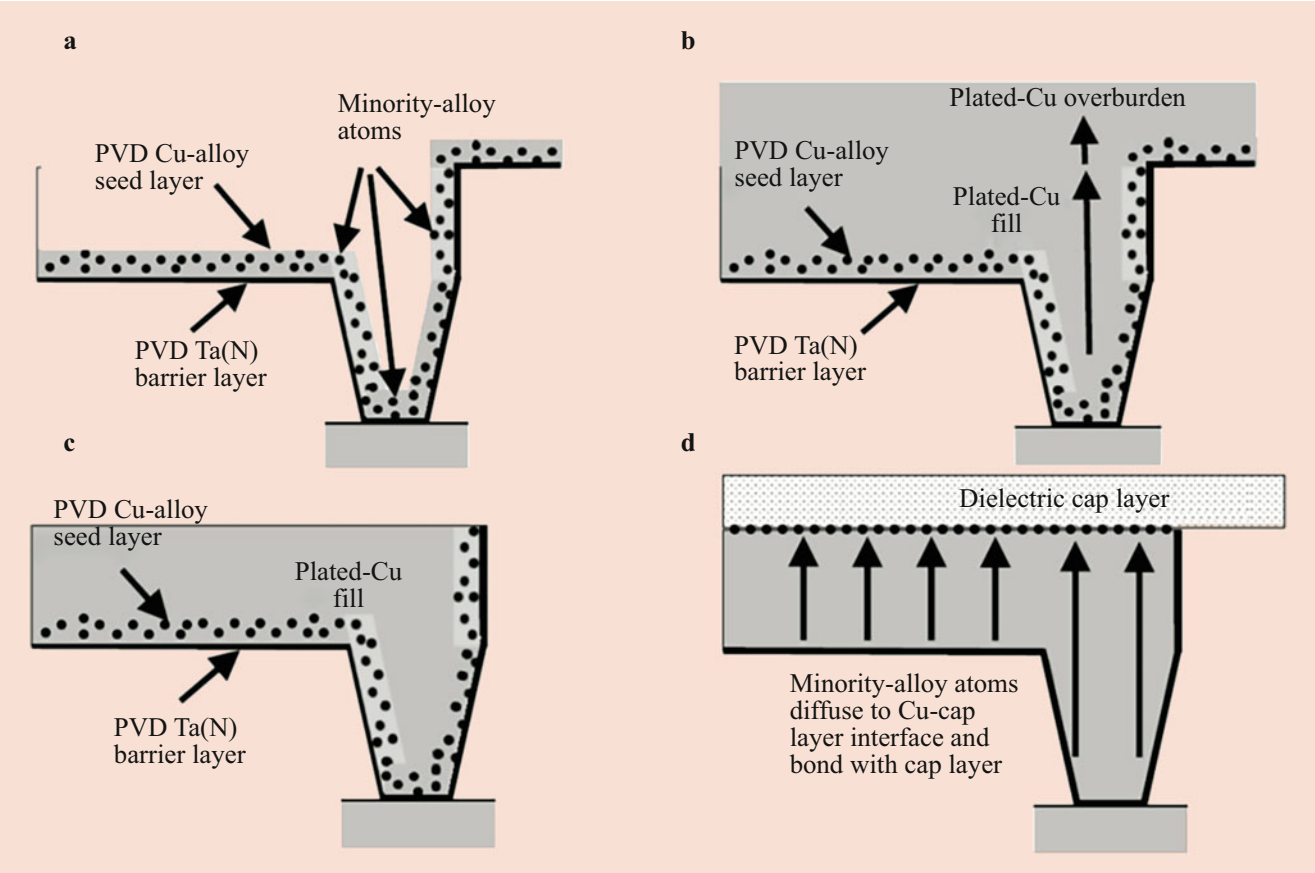

Fig. 5.32 (**a**–**d**) Schematic illustration of the self-capping effect used with alloy seed layers. The barrier/liner layers are not shown. Atoms from the minority alloy component (typically Al or Mn) are represented by the black dots (see text)

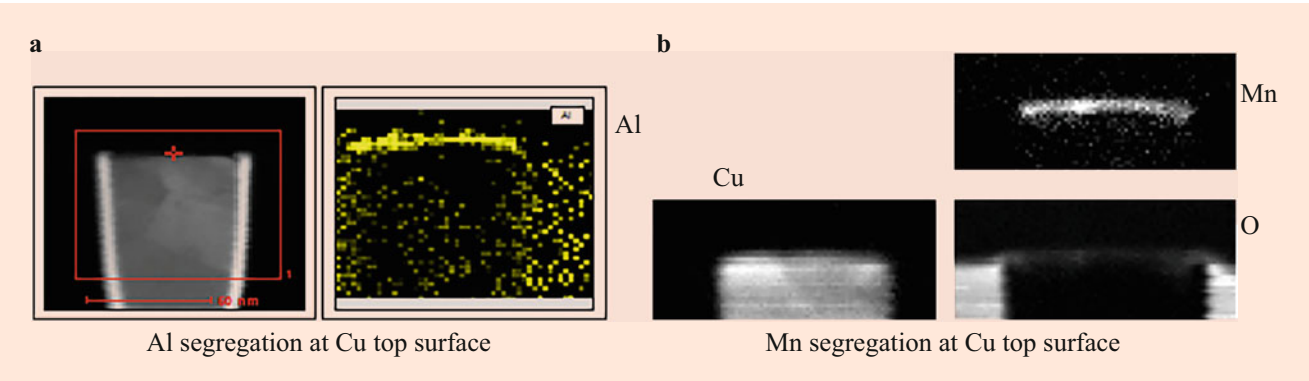

Fig. 5.33 TEM/EDX images of copper interconnect structures built using PVD CuAl (**a**) and PVD CuMn (**b**) alloy seed layers. The self-capping behavior of the alloy components is illustrated by the Al and Mn elemental maps. (Ref. [120], reprinted with permission)

to dielectrics generally make them inadequate as stand-alone barriers. Thus, a PVD and/or ALD TaN adhesion and barrier layer is needed between the liner and the dielectric, similar to the TaN/Ta bilayer discussed previously. Single-wafer chambers for CVD Co or Ru can be integrated onto the same vacuum cluster tooling as PVD Ta(N), PVD Cu, degas, and preclean chambers, so that integrated process flows which deposit a CVD Co or Ru liner in between a PVD TaN barrier and Cu seed layer can be run without breaking vacuum.

Development of integrated process flows using copper wetting layers has proceeded in parallel with the fundamental studies. Numerous studies of ruthenium liners have demonstrated improved copper feature fill, yield, and reliability at ground rules down to the 7 nm technology node and

below [126–138]. Initial studies of process flows using CVD Co liner layers began somewhat later [138–143] and have demonstrated similar yield and reliability improvements at advanced ground rules.

In terms of industry adoption in high-volume manufacturing, CVD Co wetting layers have had far more success than CVD Ru, for a combination of reasons. The Ru liner material, which is a "noble metal" in the platinum group, is difficult to polish in damascene process flows due to its chemical inertness. Cobalt liners can be polished quite easily with standard CMP slurries and are thus easier to integrate into existing copper process flows. While CVD Ru liners gained considerable initial attention due to the high Cu wettability and feature fill they displayed, the higher Cu surface mobility they show relative to Co liners results in generally poorer electromigration results when the two materials are compared directly. Some work on "Co-doped" Ru liners has attempted to address this discrepancy [144–146]. Finally, at advanced 7 nm ground rules, Cu interconnects using Co liners have been observed to have resistances ~10–15% lower than Cu interconnects using Ru liners. The resistance difference is attributed to differences in sidewall scattering behavior as well as different grain size distributions [147].

Due to the presence of oxygen compounds in the precursors for CVD Co and Ru liners, the use of Cu-alloy seed layers for self-capping and electromigration enhancement, as described previously, is ineffective [142, 143]. The residual oxygen in the CVD wetting layers neutralizes the self-capping effect of the minority-alloy components. As a result, one related advance that has been critical to the adoption of CVD Co liner wetting layers into high-volume manufacturing is the development of precursors for selective CVD Co deposition on copper surfaces. These precursors, which are different from those used for the (nonselective) CVD Co wetting layers discussed above, enable thin Co capping layers to be selectively deposited only on the exposed top surfaces of damascene Cu wires without any deposition on the surrounding dielectric. A schematic picture is shown in Fig. 5.34. In comparison to Fig. 5.31a–d, the PVD Ta liner is replaced with a nonselective CVD Co liner which serves as the wetting layer. Since the CVD Co's adhesion and barrier properties are not sufficient when the layer is used alone, the PVD TaN barrier layer is kept as the first layer next to the dielectric. In parallel to the PVD-only TaN/Ta/Cu sequence described previously, deposition of the CVD Co wetting layer and PVD Cu seed layer follows after the TaN barrier deposition in a clustered vacuum system. Electroplating is used to fill the feature with copper, and CMP is used to planarize the structure to the requisite trench height. Following planarization, the polished damascene layer is then placed in another clustered vacuum deposition system, where a reactive preclean is done to remove native copper oxide from the exposed metal, and the selective CVD Co cap

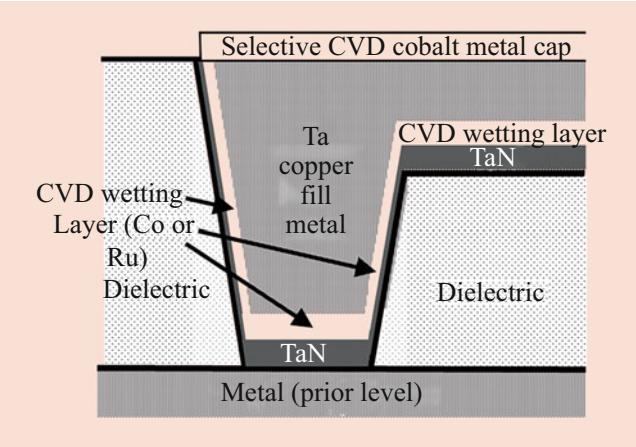

Fig. 5.34 Schematic illustration of an interconnect structure with a CVD wetting layer (Ru or Co) replacing the PVD Ta liner. The CVD wetting layer requires the deposition of a selective CVD Co metal cap in order meet electromigration requirements

layer, typically ~20–30 Å, is deposited on top of the exposed Cu wire in the same vacuum cluster tool. The result of this type of process flow is that the copper wiring structures are surrounded on all four sides by cobalt layers, either from the nonselective liner/wetting layer on the bottom and sidewalls or from the selective capping layer on top, as shown schematically in Fig. 5.34. This metallization scheme has shown 10–100× improvement in electromigration performance and up to 70% improvement in electromigration activation energy [142]. The cobalt liner/selective capping scheme has been widely adopted in the semiconductor industry wiring dimensions of 32 nm and below. The selective CVD Co cap layer integration will be discussed in more detail in section "Selective Cobalt/Dielectric Cap", in conjunction with advanced capping schemes.

Copper Reflow for Damascene Feature Fill

Further scaling of semiconductor interconnects has made electroplated fill more difficult for structures smaller than ~10–15 nm in size. This trend has driven the development of alternative feature fill methods using PVD Cu combined with reflow at elevated temperature.

A fundamental physical consideration with small damascene features is the minimum thickness of the barrier and liner layers relative to the feature dimensions. For TaN layers used as copper barriers, the minimum thickness necessary for the layer to serve as a barrier is typically of order 1.5–2.0 nm. Even for the most advanced ionized PVD deposition, the minimum thickness is typically achieved on the middle sidewalls: thicker nominal deposition on the field area (top surface) will be required to meet the minimum sidewall coverage. Wetting layers such as Ru or Co are normally deposited using CVD and have conformality approaching 100%. Nevertheless, they have similar minimum

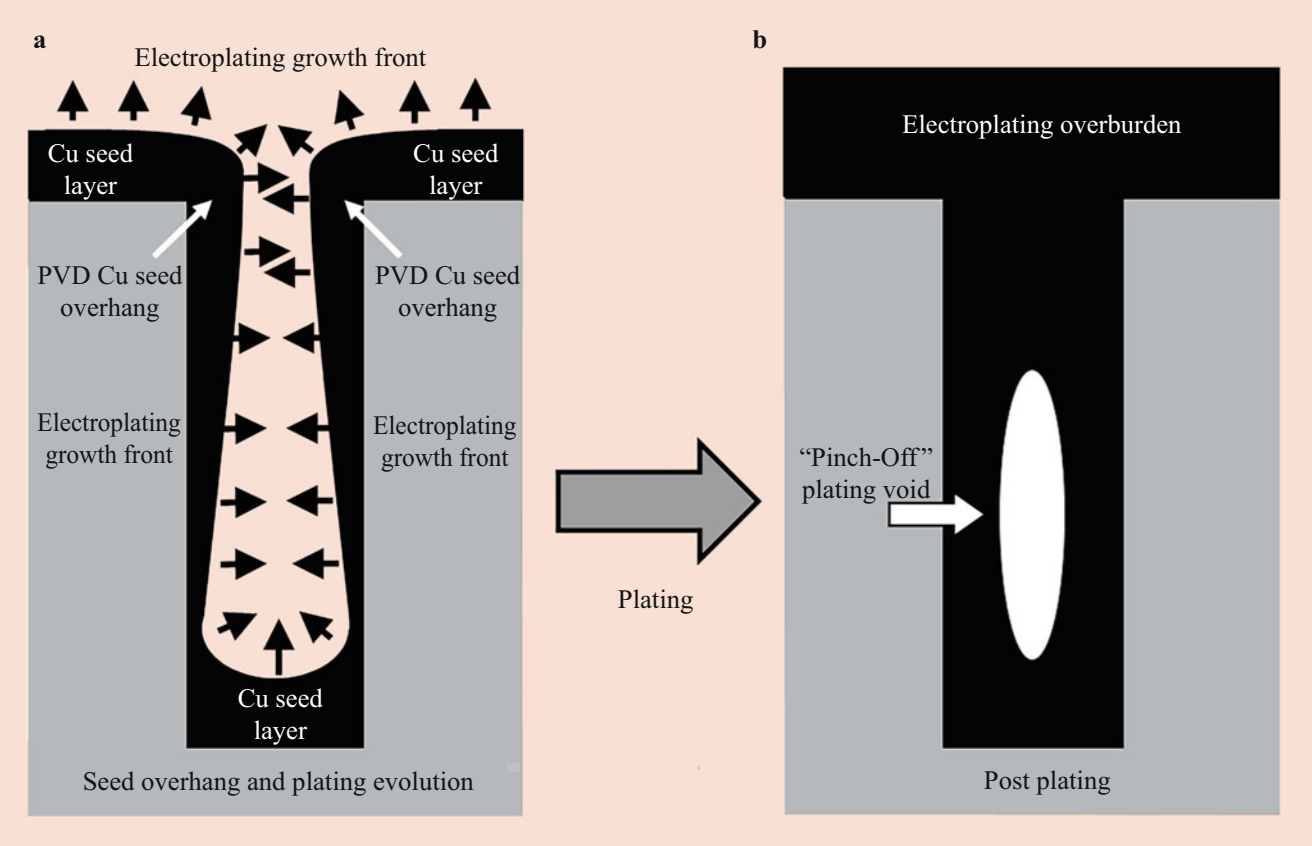

Fig. 5.35 Schematic illustration of Cu fill issues seen with features <20 nm in size. The barrier and liner layers are omitted for clarity. The encroachment of the PVD Cu seed layer makes electroplated feature fill unfeasible, due to the large overhang inherent in the deposition (**a**). Electroplated fill results in trapped voids inside the feature (**b**)

thickness requirements of approximately 2.0 nm. Sputter-deposited copper seed layers will typically require slightly higher minimum thicknesses of 2.0–3.0 nm, which is also typically achieved on the sidewalls. The resulting aggregate thickness of the combined barrier, liner/wetting layer, and seed layer will therefore be at least 5 nm at the very minimum point on the sidewalls and likely thicker. The problem this presents for trench or via features with minimum dimensions of <15 nm is readily apparent: with barrier, liner, and seed layer encroaching from opposite sides of the feature by at least 5 nm, the remaining space for mass transport of Cu into the feature through electroplating becomes vanishingly small at <5 nm. In addition, the effective aspect ratio of the feature will be increased dramatically by ~2× or more, due to the higher proportion of lateral encroachment from the sides relative to the bottom.

The previous example is idealized in that it does not consider the lack of conformality of the PVD TaN and PVD Cu layers. In particular, even the most advanced ionized PVD Cu seed layers are highly non-conformal, owing to the high sticking coefficient of Cu during sputter deposition. The resulting overhang ("bread loafing") effect discussed previously puts even more prohibitive constraints on the feature fill capabilities of PVD Cu seed and electroplating, as is illustrated schematically in Fig. 5.35a. The overhang of the Cu seed layer seen at the top of the feature accumulates heavily at the upper corners due to the high sticking coefficient during PVD Cu deposition, which results in a pronounced narrowing at the top of the feature opening. Once the electroplating process is initiated, this narrow top-corner opening becomes closed ("pinch-off"), since the copper plating growth from the feature bottom cannot advance quickly enough to fill the feature before the opposite sides at the top merge together. Furthermore, overhang at the top corners will result in shadowing of the bottom sidewalls during directional sputter deposition, making coverage in the bottom corners very thin. The thin coverage at the bottom sidewalls makes the seed layer vulnerable to etching or complete dissolution by standard sulfuric acid-based electroplating baths. As illustrated in Fig. 5.35b, the result is the formation of "pinch-off" voids deep inside the feature, which make it impossible to meet basic yield, performance, and reliability metrics.

An alternative means of filling damascene features smaller than ~20 nm with copper combines many of the methods

described previously, such as TaN barriers, CVD wetting layers, and self-ionized PVD copper, with the new technique of reflowing the PVD copper at elevated temperature. Reflow of PVD conductor metal was previously developed to fill damascene aluminum interconnects in the 1990s at feature sizes in the range of ~250 nm [83–85]. The introduction of copper interconnects in the late 1990s made electroplating the preferred feature fill method for many technology generations [85, 86]. With the introduction of reflow for copper interconnects, metal deposition schemes have come full circle.

The reflow of the PVD copper inside features <20 nm in size is accomplished either by adding radiant lamp heating capability to ionized PVD copper deposition chambers or by the use of a heated chuck, either in the PVD Cu deposition chamber or a separate high-temperature chamber [148–152]. A schematic illustration of a process sequence using ionized PVD and radiant lamp heating is shown in Fig. 5.36. Following deposition of TaN barrier and CVD wetting layers (not shown), a high aspect ratio feature is deposited with a layer of self-ionized PVD Cu. Subsequently, the wafer is heated using radiant lamps so that Cu atom surface mobility is increased, enabling diffusion of the copper surface layer atoms from the top and sidewalls of the feature down into the bottom. In the smallest features, the interfacial attraction between the wetting layer and the copper enhances feature fill from the bottom upward as a result of capillary action. By exploiting this capillary effect, PVD copper reflow is complementary to electroplating due to its superior capability to fill features that are too small to be filled by acid plating solutions. This sequence can be repeated in whole or in part, in order to enhance small-feature fill or to deposit a "touch-up" seed layer on the top surface. Wider features in the same patterning level, which are too large for the capillary action to be effective, can subsequently be filled using electroplating after the smallest features have been filled by PVD Cu reflow. Electroplating can also be used to give a thicker overburden for planarization by CMP. Similar process flows are possible using heated deposition chucks or separate anneal chambers instead of radiant lamps.

The requirements for successful PVD Cu reflow fill are generally more stringent than for copper seed and

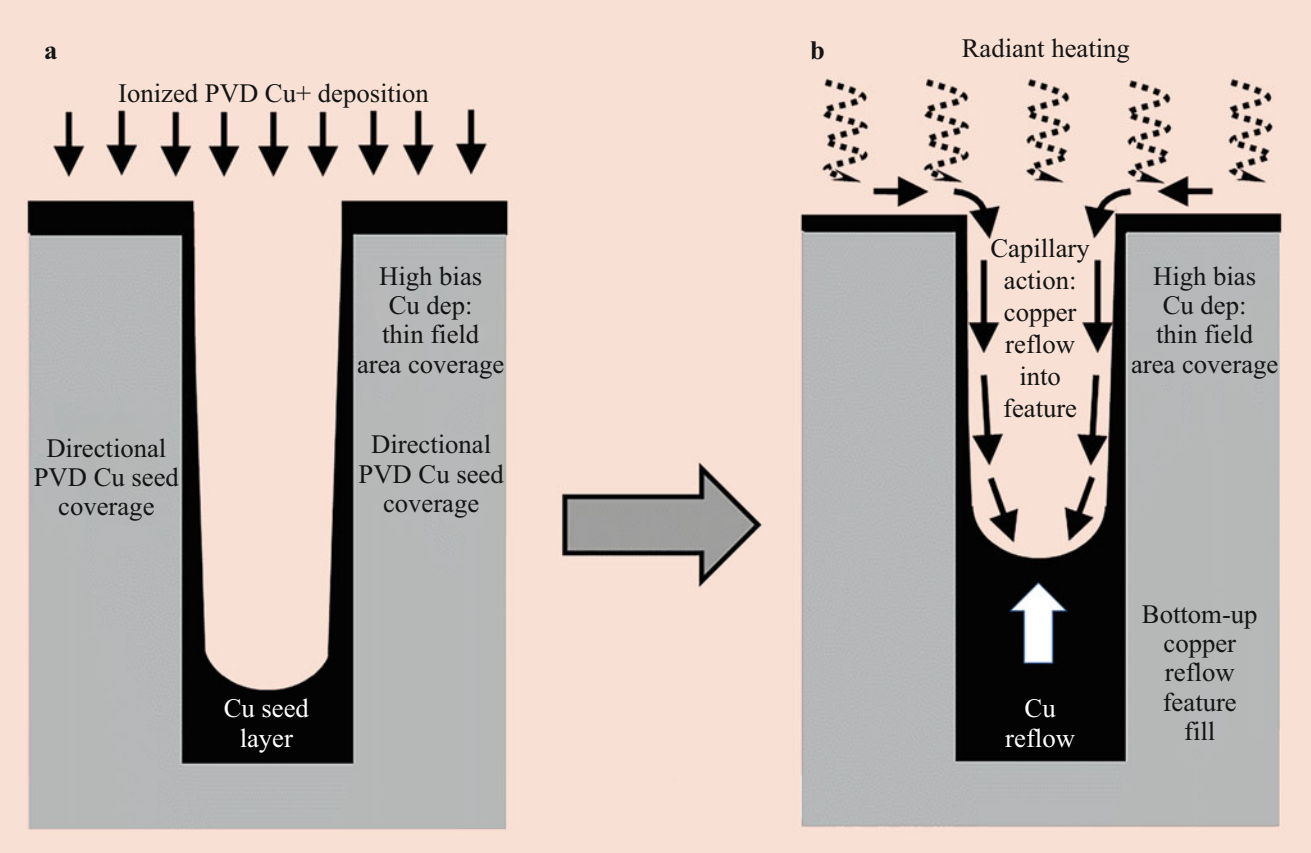

Fig. 5.36 Illustration of PVD Cu reflow fill of features <20 nm in size. The barrier and liner layers are omitted for clarity. By tuning the feature profile, top-surface coverage, and bottom coverage, a continuous film of Cu can be deposited with a larger volume of Cu inside the feature (**a**). Following radiant heating, capillary action and surface tension in the PVD Cu cause it to flow down into the feature, providing void-free fill that cannot be achieved with electroplating (**b**)

electroplating at larger dimensions. The process parameters for the PVD Cu deposition must be carefully tuned and optimized so that multiple conditions are satisfied: the thickness and volume of the top surface Cu must not be so thick as to cause Cu diffusion upward out of the feature and onto the top surface during the heating cycle, which would lead to Cu dewetting on the sidewalls and voiding. Alternatively, if self-ionized PVD Cu deposition is deposited at a bias power that is too high, the top surface layer can be partially sputtered away by Cu-Cu self-sputtering, which leads to mixing between the wetting layer and the Cu and to increased Cu resistance [150]. The proper balance between feature bottom coverage and top-surface coverage can typically be adjusted using the bias power on the self-ionized PVD Cu deposition. The reflow time and temperature cycle, which is typically at ~200–350 °C, must be optimized so that there is surface diffusion of the Cu down the sidewalls into the feature but must not be so extreme as to cause the Cu to dewet and agglomerate where coverage is thin. Similar precautions must be taken with trench and via profiles, to ensure continuous Cu sidewall coverage without dewetting or producing a discontinuity which would break the Cu surface tension and diffusion path down into the feature. Incoming feature profiles and sidewall angles must be engineered so that there are no undercuts or excessively steep sidewalls that would cause discontinuities in the PVD Cu coverage, which is generally line-of-sight.

Evaluations of copper fill using reflow have been published using 14 nm [129, 132, 133], 10 nm [135], and 7 nm technology ground rules [145, 146, 148–152], corresponding to nominal feature dimensions ranging from 32 nm down to 18 nm. These studies show improved fill capability, yield, and reliability reflow copper at these ground rules. Initial studies at 32 nm feature dimensions demonstrated the elimination of sidewall voids, tighter resistance distributions, and improved via-chain yields with reflow copper when compared against PVD seed/plating fill [150, 151]. One advantage of the reflow-type process is that the elevated temperature of the fill results in better annealing and larger grain sizes of the copper which lower the interconnect resistance and enhance electromigration performance. Studies at 7 nm used Kikuchi backscattering to demonstrate an overall upward shift in the grain size distribution of approximately 2× when compared with traditional seed layer-electroplating process flows. This grain size enhancement was also confirmed by electromigration studies which showed >10× longer fail times for the earliest fails and >2× longer fail times for the median points when reflow copper was benchmarked against seed layer-plating fill schemes [145, 146]. Reflow copper thus has potential to extend copper damascene technology beyond the limitations imposed by acid electroplating processing at feature sizes smaller than ~20–30 nm.

5.4 Dielectric Cap Deposition and Interconnect Capacitance

Figure 5.37 shows the results of modeling of the total capacitance vs cap dielectric constant and thickness for 14 nm node BEOL M2 interlevel metal structures with a fixed interlevel dielectric pSiCOH ($k \sim 2.55$) and constant Cu line dimensions. The modeling shows that both the dielectric constant (k) of the cap film and its thickness determine the capacitance increase of the interconnect.

At a fixed cap thickness of 20 nm, a ~20% decrease in total capacitance can be obtained when the k of the dielectric cap is lowered from 7 to 3. The decrease in capacitance with the reduction of cap thickness is much more significant for higher-k caps (e.g., $k = 5$ or 7) as compared to lower-k caps (e.g., $k = 3$ or 3.5). The modeling shows that the difference in capacitance is significant for thicker cap films (~3% @ 20 nm) even for small differences in dielectric constant (e.g., $k = 3$ and $k = 3.5$ curve). Figure 5.37 thus shows that thinner caps with lower dielectric constant are required to reduce the total capacitance of the device. However, a robust dielectric barrier film is required for fabrication of reliable device structures, and, as we will see later, thinning of the cap is limited by the requirements that it must satisfy. Therefore, the first approach used by industry to address the contribution of the cap to the RC delay of the BEOL was the reduction of the dielectric constant, k, of the cap.

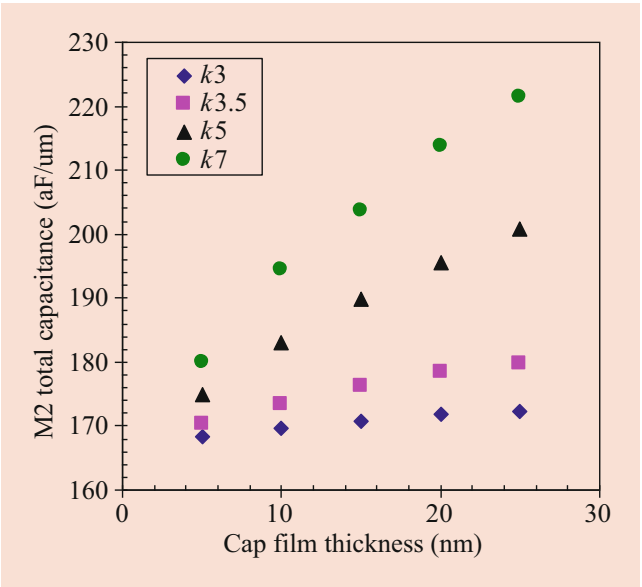

Fig. 5.37 Total capacitance as a function of the thickness of the dielectric cap and its dielectric constant. The modeling shows reduction in capacitance with thinner, lower k dielectric caps. (Ref. [54], reprinted with permission)

Table 5.8 Selected properties of dielectric caps – most caps have compressive stress, and some turn to tensile after post-UV, ultralow-*k* SiCOH cure

Cap	Description	Minimum thickness (nm)	*k*	Breakdown voltage (MV/cm)	Modulus (GPa)	Stress after UV (350C cure in Ar) (Mpa)
SiCNH	SiCNH	20	5.3	5	100	Tensile
Bilayer low-*k*	SiCNxH/C-rich SiCNyH	25–30	3.8	4.2	104	Low tensile
Bilayer nitride	SiNx/SiNy	10	6.8	7.5	150	Compressive
Trilayer	SiNx/SiNy/SiCNH	25–30	4.2	5	150	Compressive
Cyclic SiN	Multilayer SiN	12–20	6.1	8	160	Compressive
Cyclic SiCN	Multilayer SiCN	4	5.8	5	120	Compressive
Co/SiN	In situ clean/s-elective CVD Co/multilayer SiN	Co (1.8–2.4)/SiN (12–20)	6.1	8	NA	Compressive
AlO*x* /oxygen-doped carbide	Conformal AlOx + oxygen-doped SiC (ODC)	2–4 nm (AlO)x/ 3–5 nm (ODC)	4.5–6	5	>50	Compressive

Tensile stress is undesirable

5.4.1 SiN and SiCNH Caps

The first generation of dielectric cap that was integrated successfully with Cu metallization was SiN ($k \sim 7$) at 0.22 and 0.18 μm technology nodes [153, 154]. Conventional SiN film was a robust Cu cap, but with a relatively high dielectric constant.

The second-generation cap with lower-*k* value was SiCNH ($k \sim 5.3$) obtained by incorporation of carbon into the SiN. SiCNH cap was initially introduced at 130 and 90 nm technology nodes and has been used since for several technology generations [155]. The significant decrease of the dielectric constant from 7 to 5.3 reduced the cap's contribution to the total capacitance of the interconnect and the RC delay. Other properties of the SiCNH cap film are shown in Table 5.8.

Key Requirements for Dielectric Caps

While it is desirable to reduce the thickness of the dielectric cap as much as possible, this reduction is limited by the key requirements that a cap must satisfy. The cap has to:

1. Be a barrier to Cu diffusion into the dielectric.
2. Protect the Cu lines from corrosion during patterning steps in the fabrication of the device.
3. Act as an etch stop layer for via build and, in some cases, as stopping layer for planarization by chemical-mechanical polishing (CMP), balancing the stress at copper low-*k* interface [155].
4. Protect Cu from oxidation. During the fabrication process, the Cu lines covered by the cap are exposed to oxidizing plasmas during the deposition of SiCOH or pSiCOH ILD, and the cap has to prevent the oxidation of Cu.
5. Provide a hermetic seal and prevent humidity ingress to the Cu in the final device.

Finally, the breakdown voltage and current leakage of the cap should be maintained above minimal values and the mechanical properties of the cap should be maintained in order to withstand subsequent processing steps [156].

The requirements described above that must be satisfied by a dielectric cap induce challenges in the thinning of existing caps or the development of new ones. This is illustrated next by the description of the oxidation barrier test.

Effects of Reduction of SiCNH Thickness of Oxidation Barrier Properties

Caps of SiCNH in the thickness range of 35–40 nm were implemented at 90–45 nm technology nodes [157]. The thickness of the SiCNH cap film needs to be scaled down further for sub-30 nm devices in order to minimize the overall device capacitance. Various barrier performance tests along with evaluation of electrical properties were performed to evaluate the lower limit of acceptable cap thickness that will satisfy the requirements described above and it was found, as illustrated next, that material modifications are required to further scale the thickness of the SiCNH cap film below 20 nm [157].

An oxidation barrier test was performed on SiCNH films, 5-nm to 35-nm thick, and the results are shown in Fig. 5.38. The figure shows optical images of as-deposited SiCNH over Cu and after exposing the Cu covered by the SiCNH to the oxidation test (at 310 °C in air-ambient exposure for 24 h [39]). The first panel in Fig. 5.38a shows an optical image of the as-deposited SiCNH cap film on top of blanket Cu, while

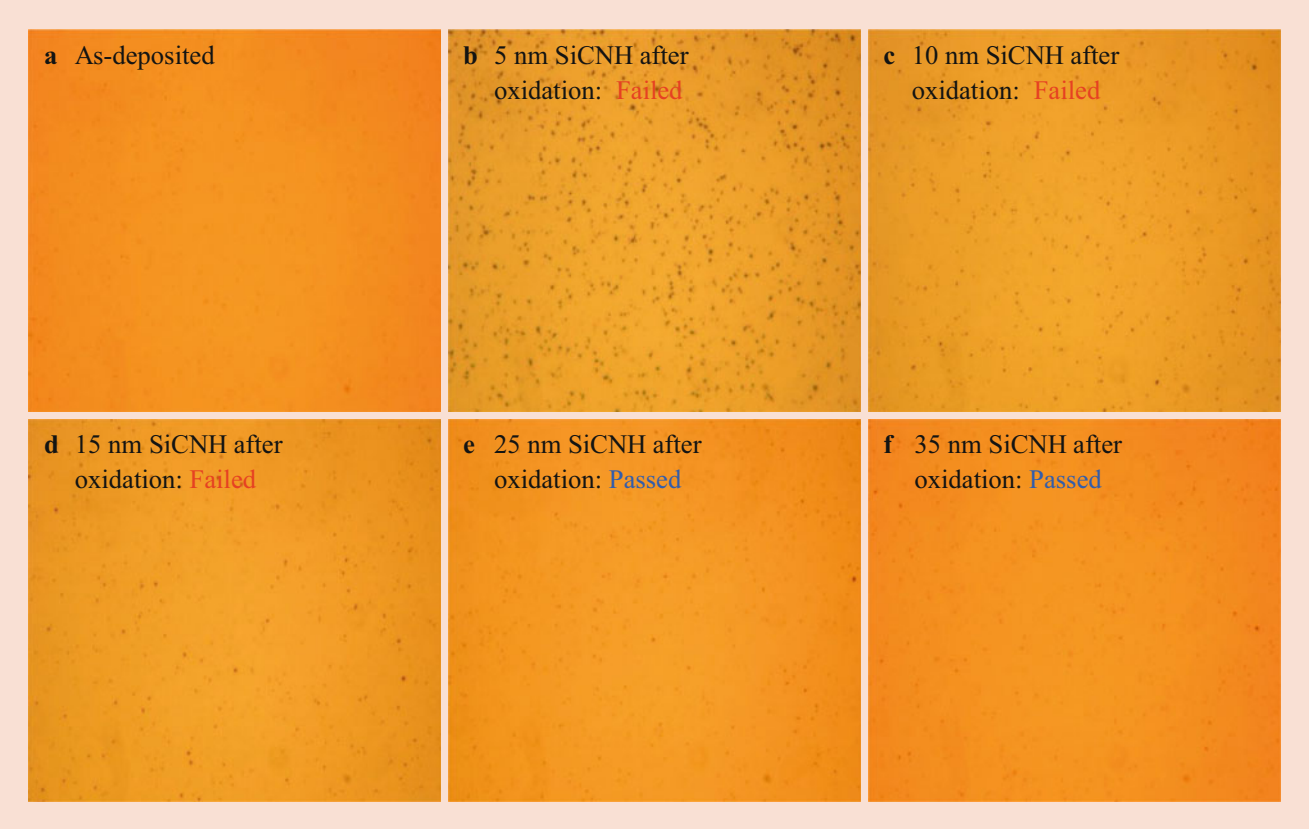

Fig. 5.38 (**a**–**f**) Top-view optical image of (**a**) as-deposited SiCNH on Cu, (**b**–**f**) 5–35 nm SiCNH on Cu post oxidation test (310 °C, 24 h, ambient air). Dark spots represent oxidized copper. (Ref. [54], republished with permission)

the other panels (Fig. 5.38b–f) show images of SiCNH cap films of different thickness on Cu after the oxidation anneal. The black dots visible in the optical images corresponding to 5, 10, and 15 nm caps indicate partially oxidized copper (CuOx) after the oxidation test. The amount of oxidized copper (density of black dots) decreases with the increase in cap thickness and for 25- and 35-nm-thick caps, no sign of copper oxidation was detected after the oxidation test. These results indicate that a thickness bigger than 15 nm is required for SiCNH to act as an oxidation barrier.

The scaling down of the cap thickness for reducing the RC delay is also limited by the cap's performance as a barrier to Cu diffusion. It was shown elsewhere [156–159] that the thickness range of SiCNH caps showing good oxidation barrier performance is also the thickness range satisfying the requirement for robust copper diffusion barrier. The Auger analysis has shown that, while the oxygen penetrates in the SiCNH cap to about 10 nm below the surface and the Cu diffuses into the cap by less than 10 nm during the oxidation test, the formation of Cu hillocks under thin caps is another factor imposing a lower limit on the thickness of a reliable SiCNH cap [157].

The breakdown and leakage of SiCNH also showed degradation with reduction of cap thickness from 35 nm to 20 nm and were further affected by exposure to UV. These observations indicate that minimum SiCNH thickness required for reliable device performance is about 20–25 nm [157]. Thinner caps are possible but require more complex advanced processing or multilayer deposition and treatment. Other properties of SiCNH caps such as modulus, breakdown voltage, and stress are summarized in Table 5.8.

5.4.2 Advanced Caps with Reduced *k* and/or Reduced Thickness

Bilayer Low-*k* Dielectric Cap (SiCNxH/SiCNyH)

The results discussed in the previous section indicate that new cap materials are required for further reduction of the BEOL capacitance. As shown in Fig. 5.37, one way to achieve the capacitance reduction is to decrease the k value of the cap. A new PECVD bilayer SiCNxH/SiCNyH dielectric cap film was developed to achieve this goal [158]. The two layers have different properties and the combined bilayer stack retains the benefits of both films. The first layer (SiCNxH) interfacing the copper has high nitrogen content and robust barrier properties, while the second layer (SiCNyH) is a film of lower nitrogen content, lower dielectric constant,

and good plasma etch selectivity. The difference in nitrogen content of the layers was obtained by changing the precursor chemistry used for depositing them. Silane + ammonia or trimethyl silane + ammonia mixtures were used to deposit the first nitrogen-rich layer. The chamber was then purged prior to introduction of a carbon-rich organosilicon precursor (dimethyl silacyclopentane) and ammonia for the deposition of the second carbon-rich layer [158].

The thickness of the two layers in the bilayer film can be adjusted to obtain robust cap performance at a low effective dielectric constant. The range of *k* values of the bilayer film obtained by varying the precursor flow rates and the thickness of the individual layers have been discussed elsewhere [156]. The two layers can be combined to obtain a reliable cap with a dielectric constant of the bilayer film of ~3.8, significantly lower than that of the SiCNH film discussed in the previous section (see bilayer low-*k* cap in Table 5.1). The barrier performance, electrical properties, and electromigration (EM) performance of this bilayer film have been found to be comparable with that of the single layer SiCNH, indicating that this capacitance reduction strategy has minimal impact on reliability [154, 158]. A scanning electron micrograph (X-STEM) of a cross section of a bilayer cap of total thickness of 26 nm is shown in the left panel in Fig. 5.39a.

With each technology node the layers of the metallization stack become thinner and the thickness of the cap needs to be reduced, especially in the thin wire levels. In this section, an alternate ultrathin bilayer cap film will be discussed. Reduction of the cap's thickness require better intrinsic cap properties compared with that of SiCNH, and this bilayer cap is therefore based on SiN.

The new bilayer cap film is deposited using silane and ammonia as precursors. The two layers in the bilayer film offer different properties and the combination of the two layers in a single stack offers additional advantages. In the SiN*x*/SiN*y* bilayer stack, the first silicon nitride, SiNx, layer is deposited at a low plasma power to minimize the damage to the pSiCOH ULK film. The second silicon nitride layer, SiNy, is a denser film deposited using same precursors but at a high RF power. This second layer is characterized by relatively high compressive stress, and hence the film stack retains compressive stress post exposure to UV cure [159].

The first layer interfacing the Cu is less dense and may not be a robust copper barrier. But this film protects the ULK surface from damage that could be created during the deposition of the dense second layer. Since the purpose of the first layer is to protect the ULK surface, an ultrathin (1–1.5 nm) first layer is enough to form a continuous film. The second layer provides the barrier properties, and a film thickness in the 7–10 nm range is required. This combined bilayer stack can provide robust barrier performance in the 8–12 nm thickness range [159]. The modulus of this bilayer SiN film (bilayer nitride cap in Table 5.8) is higher than that of the carbon containing SiCNH or the bilayer SiCNxH/SiCNyH cap films discussed in the previous section.

Trilayer Low-*k* Ultrathin Dielectric Cap (SiNx/SiNy/SiCNyH)

The bilayer SiCN*x*H/SiCN*y*H described above is a low-*k* dielectric cap showing robust barrier performance. However, upon exposure to UV used for the cure of the pSiCOH ILD, the bilayer cap film changes its stress from compressive to

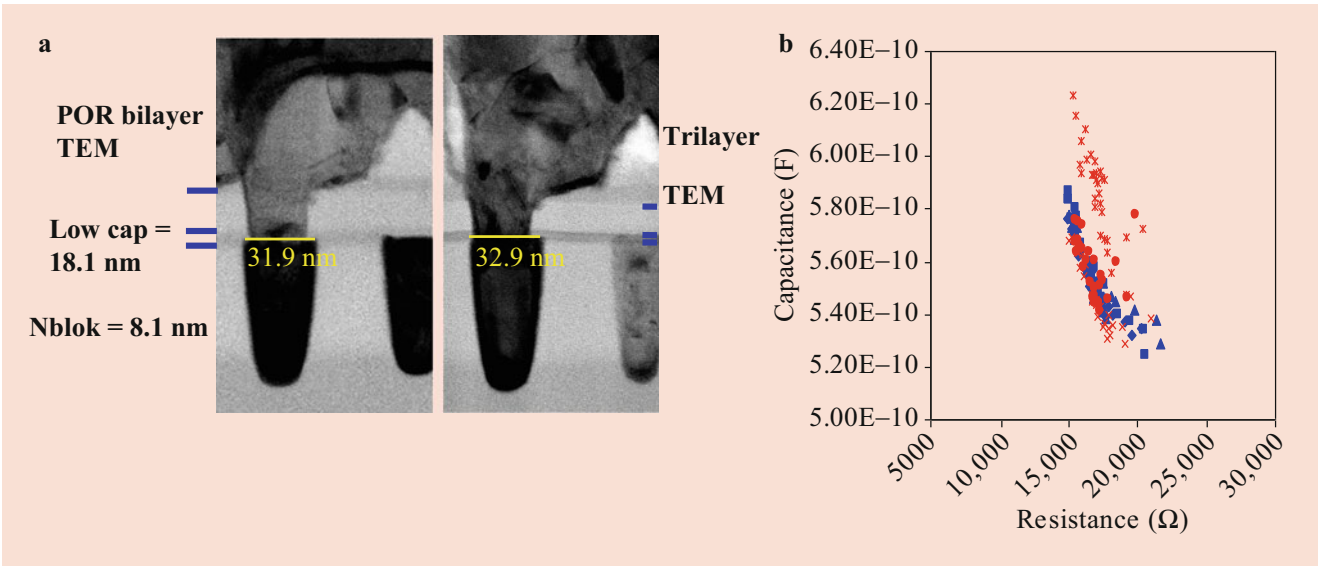

Fig. 5.39 Typical 20–26 nm thick low-*k* bilayer and trilayer caps on 32 nm Cu low-*k* interconnect structure. (**a**) Cross-sectional micrographs of bilayer (left) and trilayer (right) caps. (**b**) Capacitance versus resistance of ~20 nm trilayer cap (blue) and ~26.2 nm bilayer cap (red). A ~ 4% capacitance reduction was obtained with thinner trilayer cap as compared to the bilayer cap. (Ref. [54], republished with permission)

tensile. The stress of the as-deposited bilayer SiCNxH/SiCNyH is lower than that of the SiCNH film (Table 5.1), but both films become tensile after exposure to UV. This can lead to potential cracking in the BEOL structure, impacting the device reliability. The SiN*x*/SiN*y* bilayer film discussed above overcomes the stress change problem because it retains compressive stress post UV exposure. But this bilayer film is a silicon nitride cap; hence the dielectric constant of the cap is relatively high. In order to overcome these issues, a robust trilayer cap film, which retains compressive stress post UV cure of the pSiCOH, was developed with a dielectric constant of ∼4 (see trilayer cap in Table 5.1).

PECVD was used to deposit the three layers of the trilayer cap films in a sequential manner. Silane and ammonia were used for depositing the first two SiNx and SiNy layers of a total thickness of ∼4 nm. These layers were deposited at low and high RF plasma power to form a film with high, as-deposited, compressive stress (∼1200 MPa compressive). The third layer was deposited using trimethyl silane + ammonia as precursors. This is a carbon-rich layer with $k \sim 3.3$ and reduces the effective k value of the trilayer stack. The presence of the first two nitride layers provides high modulus to the composite cap.

The trilayer film provides excellent cracking resistance in BEOL ULK structures. The initial low power SiNx layer prevents damage to the pSiCOH surface. The right panel in Fig. 5.39a shows a cross-sectional scanning electron micrograph (X-STEM) of a typical 20 nm trilayer cap. The trilayer cap has low leakage and provides ∼4% decrease in capacitance as compared to the low-k bilayer SiCNxH/SiCNyH cap (Fig. 5.39b) [159].

Conformal Cyclic SiN

Dielectric films with high conformality are required for various applications for sub-20 nm technology nodes [160]. In the case of copper interconnects, the interface between copper and the cap plays a critical role in electromigration (EM) lifetime. Often, recesses can be seen in Cu lines near the corners after CMP, and such recesses can result in voids in the BEOL structure and affect EM lifetime. With increasing density of the interconnect structure, such recesses are expected to be more frequent. Thus, a newer conformal dielectric cap film is required to cover the copper lines without leaving any voids. In contrast to changing the deposition technique from PECVD to ALD or PEALD [160] as discussed by many in the industry, we describe a new cyclic conformal SiN cap prepared by PECVD. Such films can be deposited in existing PECVD cap tools without requiring significant investment in tool upgrades.

The new conformal SiN film is formed by using a cyclic deposition-plasma treatment process. The multilayer SiN film is formed by depositing ultrathin (∼2 nm) layers using mixtures of silane and ammonia. Each layer is deposited using a low-power RF plasma to improve the film's conformality and reduce damage to the pSiCOH ILD. After the deposition of each layer, a mild plasma nitridation is performed to densify the film. The process is repeated until the desired film thickness is achieved. The multilayer SiN is a highly conformal film that provides good step coverage with conformality of ∼70% or greater, as illustrated in Fig. 5.40.

The multilayer, cyclic SiN film has high breakdown voltage and low leakage currents, and ultrathin (10–14 nm) caps show robust copper oxidation barrier performance. The as-deposited films are compressive and remain compressive after exposure to UV irradiation. Other properties of this cap are summarized in Table 5.1. The conformal cyclic SiN shows higher modulus and breakdown in comparison to previously discussed dielectric caps and retains compressive stress post UV curing.

Selective Cobalt/Dielectric Cap

As was previously discussed in the thin-film metals Sect. 5.3.3, as the spacings between the Cu lines decrease with each technology node, there is a significant drop in EM reliability because of potential fast diffusion paths between the lines. This problem has become critical for sub-32 nm nodes. The interface between Cu and the dielectric cap plays a critical role in the EM performance. Weak adhesion between Cu and the dielectric cap makes the structure susceptible to EM induced mass flow [160, 161]. It was shown that the void growth rate under EM testing increases with decreasing interface de-bond energy between the copper and cap [161, 162]. The post-CMP recess observed in copper lines can aggravate this issue.

Metal capping layers have better adhesion to Cu wires, but any residual metal deposited on top of the ILD dielectric can cause the degradation of the time-dependent dielectric breakdown (TDDB). Furthermore, metal caps could interact with Cu and increase its resistivity, an issue that should be avoided to prevent an increase in RC. Different selective deposition methods have emerged to provide a selective metal cap solution for EM enhancement without TDDB degradation. One of the methods for selective metal capping is to use electroless deposition of Co cap [163]. The major issue with this approach is the contamination of the ILD from the plating bath, which can cause degradation in yield and potential impact on capacitance. In addition, the electroless-plating approach adds processing steps and increases wafer cost.

Alloy (doped) Cu seed layers [120, 164], using Mn or Al which is the preferred doping component, were covered previously in the metals section. The alloy self-capping technique is ineffective in the presence of CVD liner wetting layers such as Co or Ru, due to the presence of oxygen in the organometallic CVD liner precursors, which suppresses the

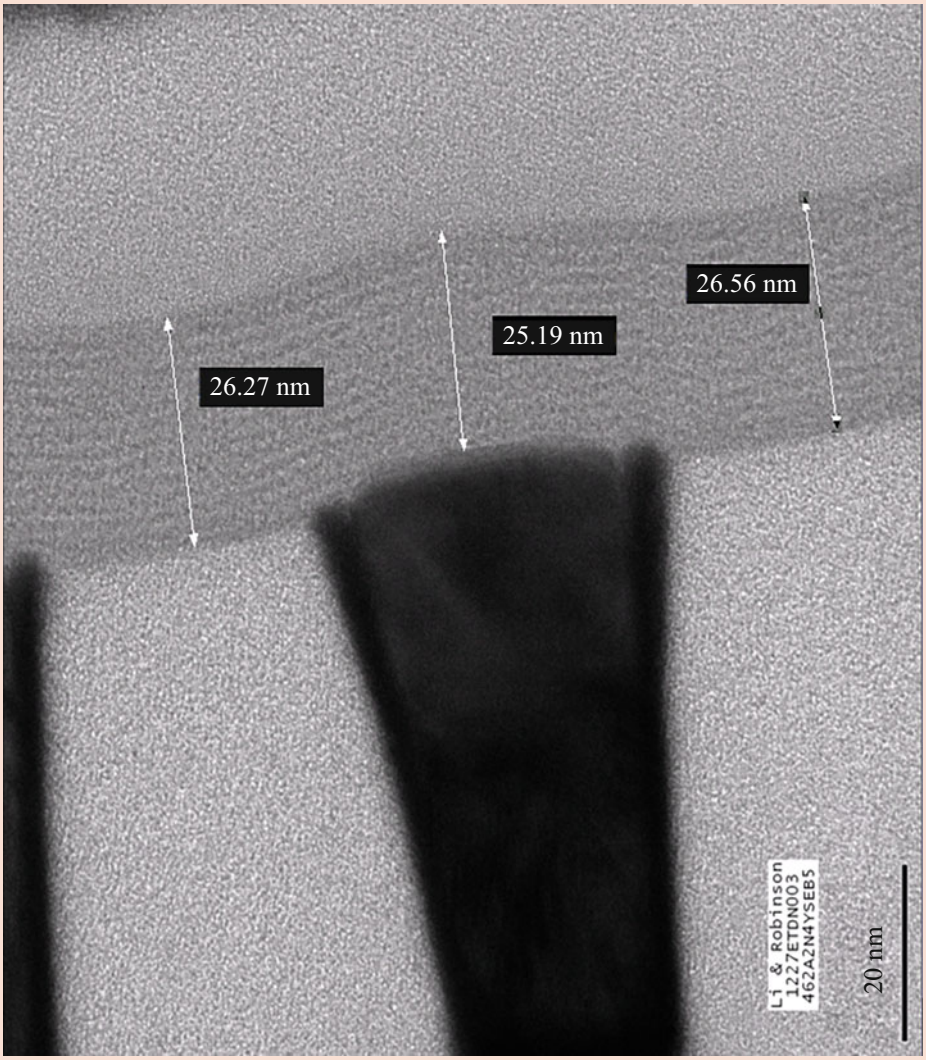

Fig. 5.40 Conformal cyclic SiN copper barrier film. The multilayer film with good conformality over copper recess. (Ref. [54], republished with permission)

cap layer bonding of the Mn or Al alloy components. They also have the drawback that un-segregated dopant (minority-alloy) atoms can stay in solution in the Cu wire and drive up resistance due to impurity scattering [120].

A more robust approach for improving EM is the use of a metal cap layer, e.g., Co, deposited on top of the metal lines using selective chemical vapor deposition (CVD). The deposition should be highly selective to enable the deposition of a sufficiently thick cap on Cu without metal deposition on the ILD dielectric. Such a process is described next.

A carbonyl-based precursor is used in the current selective CVD Co process [162, 164]. Prior to the deposition of Co, the copper surface is cleaned to remove any copper oxide and carbon residues. Co is deposited selectively only on Cu using a cyclic process where in each cycle the deposition of a thin Co layer is followed by a plasma treatment. The deposition rate drops with time in each cycle and the plasma treatment generates a fresh metal surface to restore the deposition rate. Co is not deposited on top of the oxygen rich pSiCOH. Figure 5.41 illustrates the selectivity of the Co process after the deposition of a 3 nm Co film.

Figure 5.41a–c show the EDX scans of Co liner and Co cap selectively deposited on top of Cu lines, TaN/Ta liner, and the conformal cyclic SiN cap, respectively. Co is identified only on top of the Cu but not outside it on the dielectric.

A similar, but nonselective, PECVD Co wetting layer, as described in the thin-film metals Sect. 5.3.3, was used to fabricate Co liners along the walls of the Cu lines and vias. Electromigration reliability was then evaluated for structures using an ultralow-$k \leq 2.55$ pSiCOH ILD and either dielectric caps, or selective Co plus dielectric cap, or a wrap-around Co structure where the Cu is encapsulated between Co cap and Co liner. The EM lifetime distribution for these structures is shown in Fig. 5.42. Electromigration testing was performed under a constant DC current density. In order to get any substantial fails on samples with Co cap, the testing

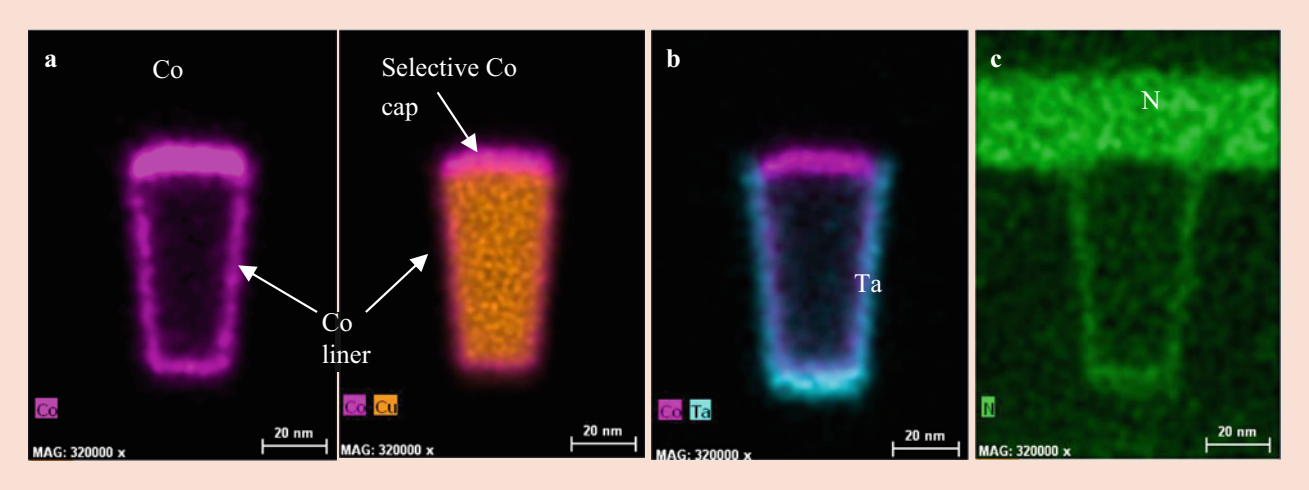

Fig. 5.41 EDX signal of (**a**) Co from selective cap and liner and Cu in the trench; (**b**) Ta from the barrier layer and Co from the selective cap; (**c**) N from dielectric cap and liner layer. Co selectively deposits on top of Cu and not on ILD or the Ta liner. A complete wrap around structure is achieved by using a Co cap and Co liner. (Ref. [54], republished with permission)

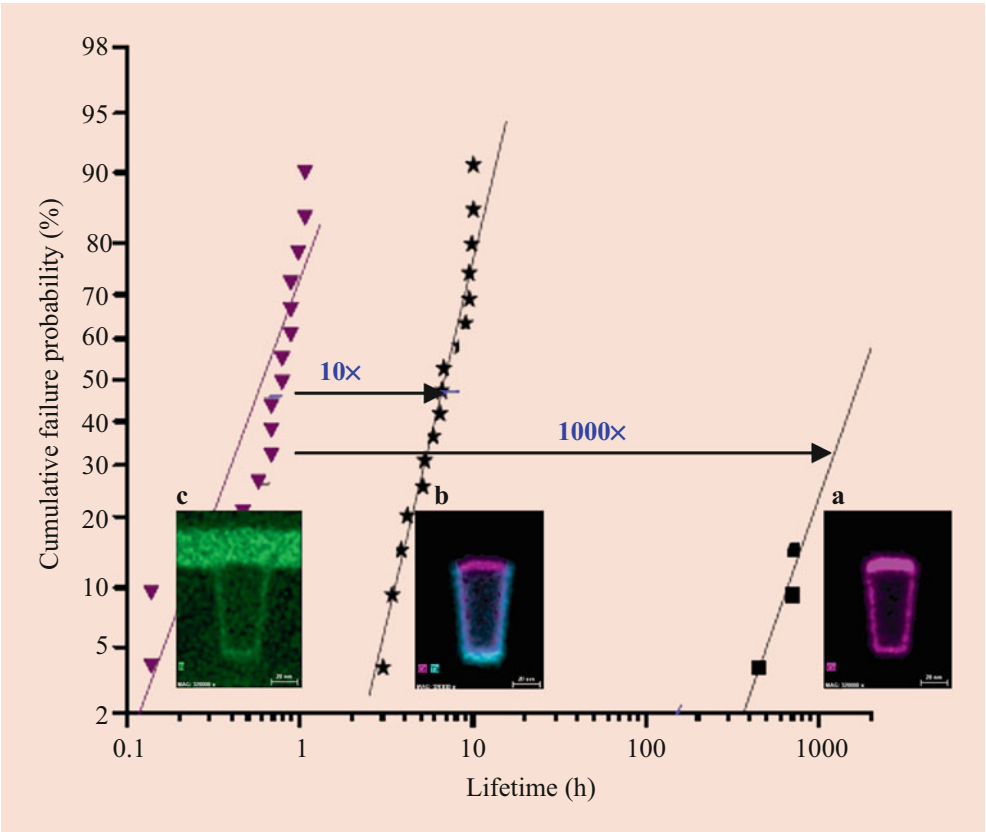

Fig. 5.42 Electromigration lifetime distribution with: (**a**) conformal cyclic SiN dielectric cap, (**b**) selective Co/conformal cyclic SiN cap, and (**c**) Co liner along with selective Co/conformal cyclic SiN cap. 10× improvement in lifetime is achieved with a metal only cap layer and ~1000× improvement is obtained with a Co cap and Co liner complete wrap-around structure as compared to dielectric only cap structure. (Ref. [54], republished with permission)

temperature was increased to 340 °C, i.e., 25–50 °C higher than the regular testing temperature. As shown in Fig. 5.42, the use of the CVD Co cap film improves the EM lifetime by ~10×, while the Co wraparound structure increases the EM lifetime by ~1000× compared to the structure with only dielectric cap.

Thin Co at the edges of Cu lines, with Cu recess at the corners is a weak point for Cu migration. As shown in Fig. 5.41b, Co cap aligns well with the Co liner but does not deposit on top of TaN/Ta liner. Thus, a preferred approach for obtaining the maximum EM benefit is to use a combination of Co liner with selective Co cap.

5.4.3 Integration of Advanced Selective Cobalt/Dielectric Cap

The results discussed above show a considerable improvement in device reliability with the selective metal cap process. It is important to understand the impact of any other parameters on device performance, especially if the selective Co cap deposition was followed with an in situ vs an ex situ dielectric capping process [165]. After the Cu lines are selectively capped with Co, there is still a need to deposit a dielectric barrier cap layer before depositing the ILD pSiCOH film. The dielectric barrier cap prevents the selective Co from oxidizing during the pSiCOH deposition. The dielectric cap can be deposited without a vacuum break after the deposition of the Co, in a chamber sharing the same platform as the CVD Co chamber (in situ), or can be deposited in a stand-alone tool, whereby the Co cap is exposed to air before the deposition of the dielectric cap (ex situ). In the ex situ process, the Co surface will be partially oxidized, and it will be difficult to reduce the Co oxide prior to dielectric cap deposition. Furthermore, a thicker Co cap film is required for an ex situ process to prevent the oxidation of Cu underlying the Co layer. In contrast, with an in situ process, the dielectric cap is deposited on Co without any intermediate oxidation of the Co or Cu. In this case, a thin continuous Co layer as low as 1.8 nm is sufficient to get the required EM benefits. A ~10× improvement in EM was observed with an in situ capping process [165] vs the ex situ process. Similar selective metal caps such as Mn [166] or Ru [167] have also been investigated. The combination of CVD Co liner and selective CVD Co cap has seen widespread adoption in advanced logic technologies at ground rules of 16 nm and below.

5.5 Summary

SiCNH and SiN*x* dielectrics have been used as cap materials for Cu/low-*k* interconnects in many device generations. The SiCNH cap has minimum thickness limit for performing as an oxidation barrier. Reduction in RC with aggressive interconnect scaling therefore required development of new, thinner, lower-*k* dielectric barrier films. This led to development of several multilayer caps with $k < 4.5$ and thinner 4–25 nm caps. Conformal dielectric cap film was developed to provide good coverage of recesses in copper lines. In addition, a selective Co cap process was developed to further improve the EM performance in recent years together with various dielectric cap listed in Table 5.8 [166–169].

There are good etch stops such as AlO*x*/oxygen-doped SiC (ODC) [168] that have also been used as excellent stops in manufacturing sub-20 nm node devices. Aluminum oxide films characterized by a dielectric constant (k) of less than 7 (such as between about 4 and 6) and having a density of at least about 2.5 g/cm^3 (such as about 3.0–3.2 g/cm^3) are deposited on partially fabricated semiconductor devices over both metal and dielectric to serve as etch stop layers. The films are deposited using a deposition method that does not lead to oxidative damage of the metal. The deposition involves reacting an aluminum-containing precursor (e.g., a trialkylaluminum or other cyclic aluminum oxide compound). A second layer of oxygen-doped silicon carbide (ODC) was deposited on top to act as a secondary oxidation barrier. This composited AlO*x*/ODC cap/etch stop has excellent etch stop properties and is currently the leading cap being used in tight metal pitch levels by leading semiconductor manufacturers, for sub-20 nm BEOL device fabrication in addition to the standard SiN, SiCN, and cyclic SiN/SiCN cap listed in Table 5.8. These are the most common dielectric caps that are being used at various levels as oxidation barriers and etch stops in semiconductor fabrication.

There are also many other promising caps and etch stops such as high-*k* dielectric HfOx, SiC, SiCNO, and others that have been described in detail with various references in recent cap review [170]. However, those caps tend to have limited use and generally tailor to specific application. In the near future, lower-*k* metal oxide etch stop such as MnOx and MnSiOx ($k \sim 3.7$) together with ODC with thickness in 1–3 nm range should be explored as alternate device-compatible etch stop/cap for sub-5 nm Cu interconnect device fabrication in air gap [170] or ultrathin cap/liner [171, 172]. When other low-diffusivity metals such as Co or Ru are used in interconnect, the need for good etch stop and oxidation barrier cap with excellent electrical and mechanical properties is still highly critical to achieve desirable performances and improve reliability in future nano-electronic devices.

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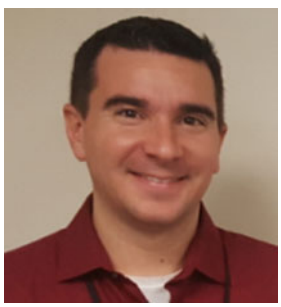

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Wet Chemical Processes for BEOL Technology

6

Cornelius Brown Peethala, James J. Kelly, Donald F. Canaperi, Mahadevaiyer Krishnan, and Takeshi Nogami

Contents

6.1 Wet Cleaning/Etching for Cu Interconnects 220
6.1.1 Wet Clean Tooling 220
6.1.2 Wet Clean or Wet Etch Applications 221

6.2 Cu Electroplating 228
6.2.1 Background 229
6.2.2 Cu Plating Chemistries 231
6.2.3 Tooling for Copper Electroplating 233
6.2.4 Copper Electroplating, BEOL Yield, and Reliability 234
6.2.5 Extendibility of Copper Electroplating: Future Perspectives 237

6.3 Chemical Mechanical Planarization 240
6.3.1 CMP Tool Description 240
6.3.2 CMP Process Description 242
6.3.3 Copper CMP 243
6.3.4 Control of CMP Defects 249
6.3.5 Copper CMP for Alternative Barrier/Seed Systems . . . 250
6.3.6 Summary 252

References 253

Abstract

This chapter covers wet processes for logic back-end-of-the-line interconnect technology – namely, wet cleans and wet etching (Sect. 6.1), electroplating (Sect. 6.2), and chemical mechanical planarization (Sect. 6.3). Each section details the introduction of the process and equipment used in 300-mm semiconductor industry from the beginning of Cu era. All the critical components of the process and equipment are described followed by the experimental results and discussion for each of the application. In wet cleans and wet etching section, applications like post-etch residue clean, backside clean, and hardmask wet etch are covered. Plating section includes copper electroplating of damascene and dual damascene structures. In chemical mechanical planarization section, metal – copper, tantalum, tantalum nitride, and cobalt – polishing and planarization, and post-cleaning applications are covered.

Keywords

Wet clean · Wet etch · Corrosion · Copper · Electroplating · Electrodeposition · Plating · BEOL · Damascene · Interconnect · Chemical mechanical planarization · Slurry · Planarization · Topography · Polish · Brush clean

6.1 Wet Cleaning/Etching for Cu Interconnects

In fabrication of Cu interconnects, wet cleans are integrated in every module to meet the defectivity requirement that is essential to wafer electrical yield and reliability. Wet cleans are primarily used in Cu interconnects for surface cleaning and etching materials. In general, "wet clean" is applied on the wafer to:

(a) Remove organic and metallic particles or contaminants [1, 2]
(b) Remove unreacted residues or particles after film deposition [3]
(c) Remove plasma reactive ion etch (PRIE) residues after plasma etching step [4]
(d) Remove organic and metallic contaminants on backside or bevel of the wafer [5–9]

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On the other hand, "wet etch" is applied to:

(a) Remove sacrificial materials – dielectrics, metals, organic layers, silicon antireflective coating, and metal nitrides [10]
(b) Partially etch or recess a material to a target thickness – dielectrics, metals, and semiconductor materials [11]

In both cases, wet chemical solution which is a mixture of chemical components is the core of this process. Both aqueous and non-aqueous solutions are used in semiconductor industry. Standard wet clean solutions used in Cu interconnects include, but not limited to, dilute hydrofluoric acid (dHF), standard clean 1 (SC1), standard clean 2 (SC2), ultra-dilute sulfuric peroxide (uDSP) mixture, and chrome phos. These solutions are applied at temperatures ranging from room temperature to 70 °C. Starting from 14 nm technology, formulated vendor cleans were introduced both for cleaning and etching materials. In this chapter, advancement of wet cleans in Cu interconnects is discussed.

6.1.1 Wet Clean Tooling

Before going into the details of wet chemistries that are used in Cu interconnects, an understanding of equipment is needed to describe how a wet clean is performed. There are two major types of equipment for wet cleans. First one is a batch tool, where a boat of wafers is immersed in the target chemistry to perform the cleaning. A 200-mm wafer wet processing was by immersion batch process which continued into early 300-mm wafer process. As technology advanced, additional defectivity reduction requirements from wet clean triggered equipment to move from batch to single wafer processing. The immediate benefit is isolating device side process fluids without exposure to entrained particles from the backside. In the interest of Cu interconnects, the below section is dedicated to single wafer wet clean equipment.

Figure 6.1 shows a scheme of a single wafer wet clean equipment. Key components in single wafer wet clean tool are shortly described in the following:

Chemical solutions are procured in bulk 55 gallon drums and are situated in sub-fab to supply to the tool level via supply pump. These chemistries are supplied at room temperature and fed either into a day tank or onboard chemical mix tank (30–50 L capacity). In some cases, 5 gallon carboy is also used as the feed.

Chemical mix tank is where all the chemical components are mixed. In an example of aqueous chemistry, targeted chemicals are mixed with deionized (DI) water in the chemical mix tank at the targeted ratios. After mixing is complete, mixture is heated to target temperature. Chemical recirculates between the chemical mix tank and chamber in a loop, chemical mix loop, with an extension at the chamber to dispense chemistry through nozzle on a scan arm, as shown in Fig. 6.1.

Scan arm consists of several channels extending to nozzles that dispense onto the wafer. Through each channel one of (a) formulated chemical mixture (b) DI water, (c) isopropanol or (d) nitrogen is dispensed onto the wafer. There can be multiple scan arms within a chamber.

Chuck pins are used to hold the wafer both in stationary position and rotating movement. They are in contact at the bevel of wafer extending up to 4 mm of the wafer edge.

In wet clean tool, *drain cup* is used to direct the post-process chemical into specific drain. Drain options include acid waste, base waste, solvent, and fluoride. Depending on the chemical compositions, these drains are selected in the recipe steps to direct each chemical for downstream treatment before disposal.

Wet clean process recipe on the tool can be broadly divided into four steps. First step involves preparation of the chemical in the chamber. In this step, the chemical is dispensed from nozzle to drain directly for few seconds to ensure that a fresh chemistry is ready to be dispensed on the wafer. During this step, scan arm is in home position, i.e., not on top of the wafer. In the second step, scan arm position comes onto the top of the wafer, and the chemical mix is dispensed onto the wafer to perform the targeted cleaning or etching. During this step, wafer is continuously rotated at rpm varying from 300 to 1500. There are substeps within second step, which involve change in rotation speed and change in scan arm position to optimize the uniformity and particle removal efficiency across the wafer. In the third step, dispense liquid is switched from chemical mixture to DI water. During this step, wafer continues to rotate, and DI water replaces the chemical mixture on the wafer and rinses off any residual chemical from the wafer. The final and fourth step is wafer drying step. In this step, wafer is dried using nitrogen flow or a combination of isopropanol and nitrogen flow. During all the four steps, wafer is continuously rotated, and at the end of fourth step, wafer rotation slows down to zero.

6.1.2 Wet Clean or Wet Etch Applications

Wet clean innovation and development for Cu interconnects have been driven by the advancements in patterning, materials, continuous scaling of the critical dimensions, and the requirement of defectivity levels to sub-100 nm size. Cu interconnect cleans are mainly divided into (a) post-film deposition clean, (b) pre-lithography backside clean, (c) patterning and hardmask open clean, (d) post-via etch clean, and (e) hardmask wet etch.

(a) Post-film Deposition Clean

Each interconnect level begins with deposition of several films including dielectric cap, interlevel dielectric (ILD),

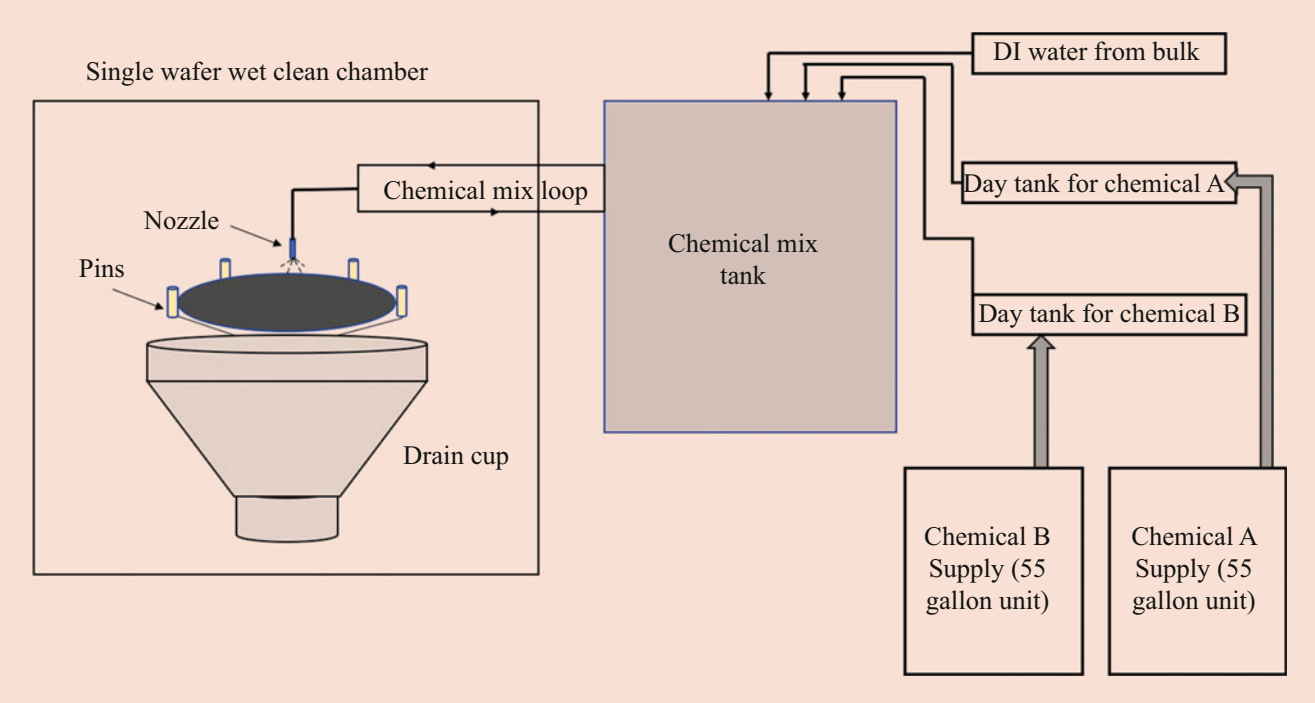


Fig. 6.1 Schematic of a single wafer wet clean tool

silicon dioxide, silicon nitride, and titanium nitride. Usually after dielectric film deposition, unreacted species remain on surface as particles. These particles appear as embedded defects in downstream processing and negatively impact patterning process. Wet cleans are applied on these films to remove these unreacted species or particles. These cleans need to be chemically mild to avoid any chemical etch or damage to the films. Known solutions include SC1, brush clean, or DI water spray.

(b) Pre-lithography Backside Clean

After coating lithography films including organic planarization layer (OPL), silicon antireflective coating, and photo resist, backside cleans are performed to remove backside particles to eliminate any hotspots during lithography exposure. The main sources of these particles are from wafer handling and chucks from the upstream tooling. Particles are mostly composed of carbon, oxygen, and silicon. Figure 6.2 shows the evaluation of backside cleans for this step. DIW brush clean is commonly used at this step and is efficient at removing particles as shown in Fig. 6.2. Brush assists in scrubbing off particles, and DIW liquid carries them away in solution. The unremoved defects are mostly chuck marks. With the advanced development of backside chambers by equipment vendors, DIW with high N_2 flow is used as an alternative to brush clean, and when this is combined with chemicals like dilute HF and SC1, it is shown to provide similar results as brush clean (Fig. 6.2). In addition, backside cleans have been implemented at other steps in the process including post-dielectric deposition, post-plasma etch, and post-metal liner deposition [9]. These cleans reduce the defectivity on backside and eliminate the possibility of particles falling onto topside of the wafer in foups.

(c) Patterning and Hardmask Open Cleans

Optical 193 nm lithography is shown to have difficulty in resolving features below 80-nm pitch structures in a single exposure. Several patterning methods such as double patterning – litho-etch litho-etch (LELE) – sidewall image transfer (SIT), self-aligned double patterning (SADP), and triple patterning, litho-etch litho-etch litho-etch (LELELE), were used to extend 193 nm lithography down to 48-nm pitch structures [12]. Wet cleans play an important role to clean the residues during these patterning steps and remove sacrificial layers. As an example, SIT patterning scheme is shown in Fig. 6.3.

In this case, OPL was used as mandrel material, silicon dioxide as spacer material, and TiN as hardmask (HM) material. Wet cleans are performed during this patterning (a) after mandrel etch and (b) after spacer etch back. Here, the wet clean is intended to clean post-etch residues around the mandrel material and spacer materials and on TiN HM. The key requirement of this wet clean is to not etch/attack any of the materials exposed. Dilute HF (dHF) wet clean works

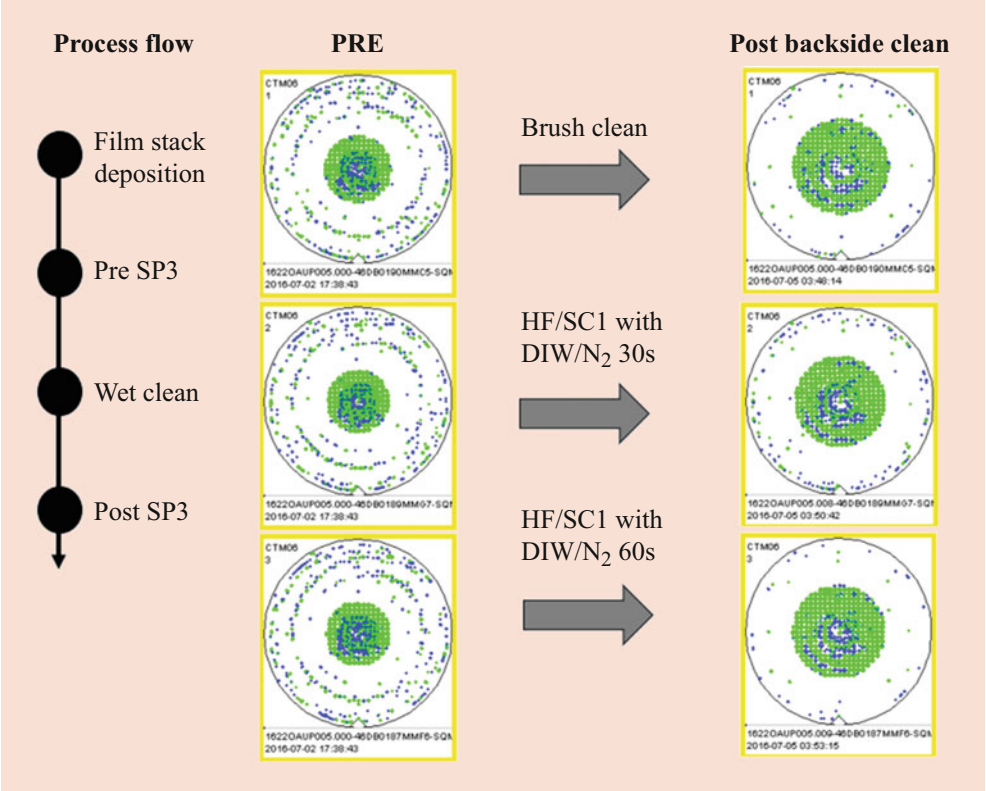


Fig. 6.2 Evaluation of backside cleans at pre-lithography step

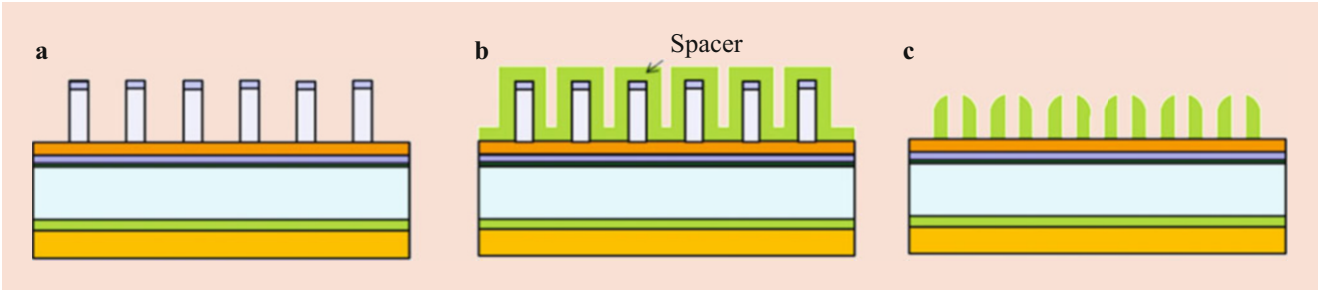


Fig. 6.3 SIT patterning module: (**a**) post-mandrel etch clean, (**b**) post-spacer deposition, and (**c**) post-spacer etch back/mandrel removal and wet clean to remove etch residues

well for both applications in removing the post-etch residues. Concentration of dHF is varied between 300:1 and 1300:1 – DIW:49% HF and temperatures between room temperature and 60 °C were evaluated for this step [14]. dHF etch rate of oxide at these concentrations is <1 Å, and that is enough to remove few monolayers of oxide/native oxide on the surface of the exposed materials. Removal of these films results in undercut and lift-off of the post-etch residues that are on the surface. One of the challenges with silicon dioxide as spacer materials is the potential undercut at the spacer and hardmask interface from dHF wet clean. This undercut at the interface results in spacer flopover. Alternatively, chemistries such as ultra-dilute sulfuric peroxide (uDSP), dilute SC1, and formulated chemistries were also proven to efficiently clean the post-etch residues. Figure 6.4 shows the impact of wet clean after spacer etch back on electrical resistance and yield. When there was "no clean" after spacer etch, very high line resistance and ISOVIA resistance were observed. This indicates shallow trench or smaller trench CD due to blockage of the trench pattern from residues after spacer etch back. In all the other cases where clean was applied, very high yields were observed with dHF split showing the best distribution.

At 7-nm technology node and 36 nm pitch, EUV lithography was introduced as a single patterning method to direct print lines [15]. The single patterning method simplifies the patterning stack in terms of wet cleans, and the first post-plasma etch clean is applied after hardmask open (HMO)

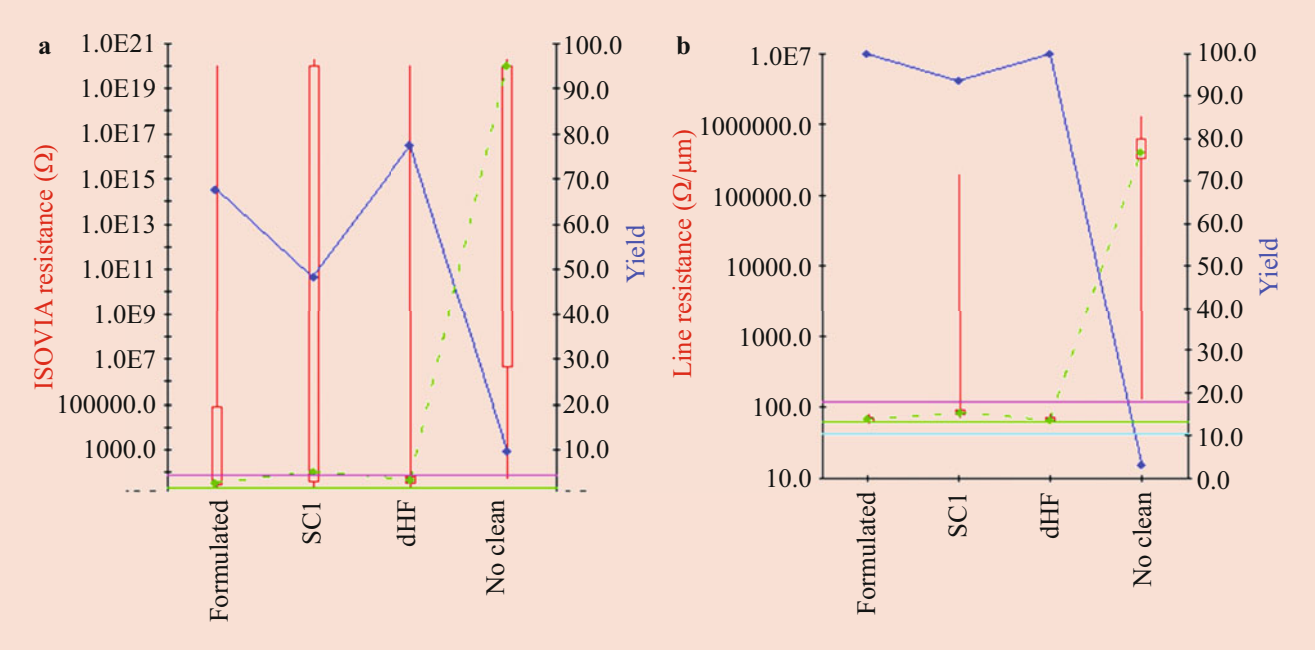


Fig. 6.4 Impact of wet clean after spacer etch back on electrical resistance and yield of (**a**) ISOVIA macro and (**b**) line macro

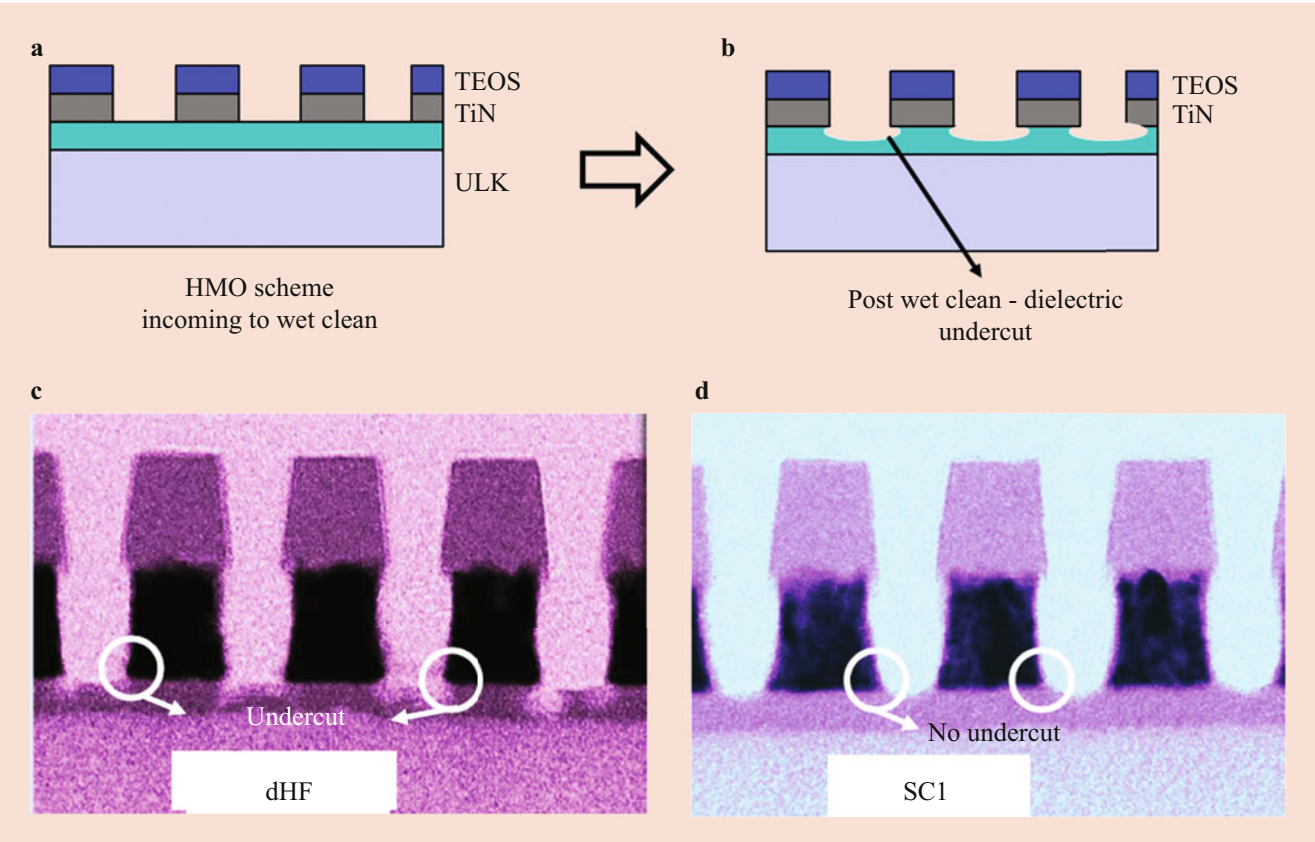


Fig. 6.5 (**a**) Pre-wet clean cartoon (**b**) post-hardmask open (HMO) wet clean for EUV 36-nm pitch single line patterning. (**c**) shows undercut with dHF wet clean and (**d**) shows no undercut with SC1 wet clean

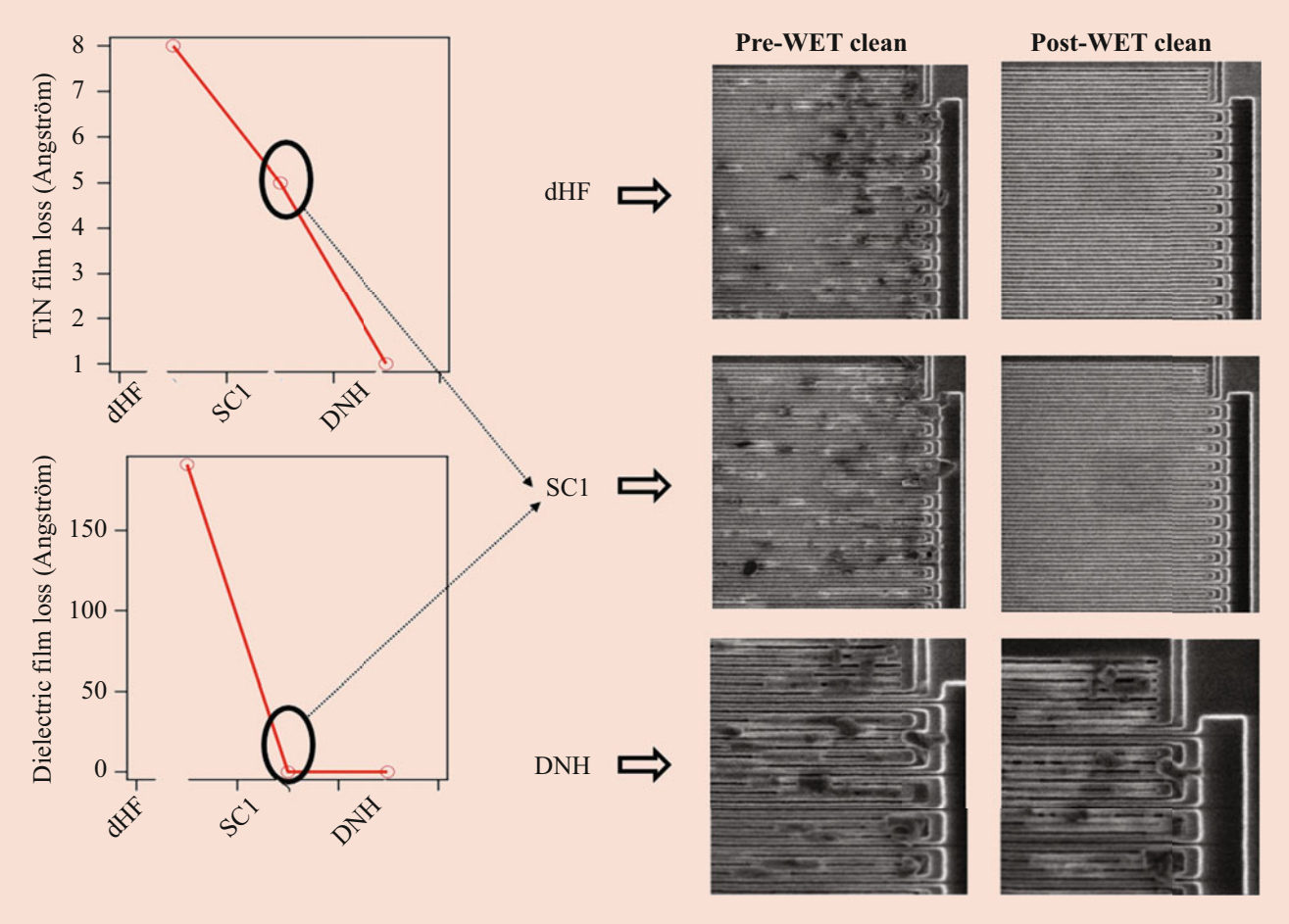


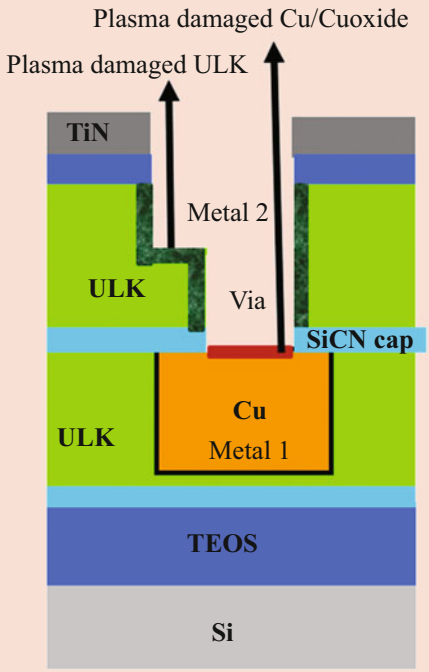
Fig. 6.6 Wet clean evaluation for EUV HMO application

step. Incomplete residue removal blocks downstream trench and via etch and results in an electrical open. On the other hand, TiN undercut can result in increased or nonuniform CD of trench, and in the worst case, it will lift off TiN resulting in an electrical short to the neighboring line. Figure 6.5 shows the pre- and post-HMO wet clean. The post-wet clean cartoon is an example of chemistry where there is active undercut into the dielectric hardmask. dHF for this application cleans residues efficiently, but as can be seen in Fig. 6.5c, there is clear undercut underneath TiN. The undercut is a result of active etching of the exposed dielectric film underneath TiN. In some cases, even though the pristine dielectric material does not etch in wet chemistry, a plasma-modified material can have active etch rat. As an alternative wet clean, SC1 chemistry for this application shows no undercut in Fig. 6.5d.

Figure 6.6 shows the TiN and dielectric wet etch rate with various wet cleans and top-down scanning electron microscope (SEM) images before and after wet clean. To test the effectiveness of wet clean in removing post-etch residuals, an aggressive polymerizing etch chemistry was applied at HMO step. As expected, a high number of post-etch residues were seen on the trench macro. In comparison to dHF, SC1 and dilute ammonia wet clean (DNH) show lower TiN removal. Mostly the removed film removal here is the titanium oxynitride (TiO_xN_y). dHF completely removes TiO_xN_y, ~8 Å, whereas SC1 removes it partially, and no etch rate was observed with DNH. For the dielectric etch rate, dHF showed the highest etch rate of >150 Å, and no etch rate was observed for both PAM and DNH. The observed high etch rate of dHF is the root cause of the undercut. In terms of post-etch polymer residual removal, both dHF and SC1 showed 100% removal as shown in Fig. 6.6 TDSEM. In contrast, DNH did not remove the residues. So, while both SC1 and DNH are attractive in having low etch rates of dielectric, only SC1 is effective in completely removing the residues. Both the ability of breaking down the residues by peroxide in SC1 and partial removal of TiO_xN_y provide optimal wet clean solution for this application.

(d) Post-via Etch Cleans

The next wet clean in BEOL module after HMO cleans is post-via etch clean. With interconnect scaling, trench (line) and via resistance increase are expected due to reduced Cu



Element	Target
Cu loss	Total Cu loss after damage removal <5 Å per cleaning cycle
Dielectric (ULK and Cap) compatibility	ULK loss including damage removal <5 Å No impact on ULK properties (n and k) Dielectric cap loss <5 Å
Cleaning of Cu residues	No Cu void at the via bottom
Critical dimension (CD)	CD growth <1 nm
Reliability	No degradation
Defectivity	Less than 50 adders at 30 nm
Pattern collapse	No collapse for aspect ratios upto 10:1

Fig. 6.7 Schematic of post-via etch structure and material removal targets for wet clean

volume. For trench there is no metal-to-metal interface at the bottom, but for via, there is additional interface resistance between via and the line below. To meet the via resistance targets, this interface must be free of metal oxides or post-plasma etch residues.

For via etch, fluorine-based reactive ion etch (RIE) gases with the combination of CO/CO_2 ash are used. After finishing the plasma etch, carbon-fluorine-hydrogen (CxFyHz)-based post-etch residues (PER) are present on the exposed structures. A wet clean is essential here to remove dry etch polymer residues, remove plasma etch damage on Cu, and retain critical dimension (CD) by not etching all exposed materials like metal nitride hardmask, sacrificial hardmask, ultralow-k (ULK) , SiCN dielectric cap, Cu, barrier/liner - TaN, Ta, Co, Ru, etc. [16–18]. Also, pattern collapse needs to be prevented on the narrow structures with aspect ratios >6:1, and particle performance needs to be <50 @ 30 nm. As shown in Fig. 6.7, there is plasma damage on the sidewall of ULK and top of exposed Cu surface. Plasma from RIE depletes carbon in the outermost layer of ULK resulting in more like a silicon oxide film. This makes the damaged ULK more susceptible for wet removal in chemistries like dHF. Plasma-damaged Cu was shown to contain oxygen, fluorine, and carbon on the top surface. Table in Fig. 6.7 summarizes the key requirements of wet clean.

In the literature, cleaning formulations were published for post-via etch clean that include dilute hydrofluoric acid solutions, semi-aqueous fluoride solutions, hydroxylamine, and solvent-based chemistries that may also contain tetramethylammonium hydroxide and ammonium fluoride [19–23]. Among these wet cleans, TMAH-based cleans are known to negatively impact CD by removing excessive dielectric [24]. While organic solvent-based chemistries were also considered for this application, they are not preferred over aqueous commodity chemicals due to cost and environment health and safety (EHS) concerns.

Dilute-HF(dHF) solutions with and without the addition of organic acids are proven effective for post-via etch clean application while meeting the critical requirements listed in Fig. 6.7 [16, 18]. These solutions are cost-effective and applied at very dilute concentrations to clean the post-etch residues. They are efficient in removing Cu oxide and have shown to have varying control of damaged low-*k* dielectric films (CDO) removal. In the following, the main challenges with dHF-based chemistries and known methods to address those are summarized.

- **Dissolved oxygen**: The dissolved oxygen in the solution enables continuous etch of Cu by the sequence of oxidizing Cu into Cu oxide and dissolving Cu oxides. This is anisotropic etch at the via bottom that leads to undesirable voids during downstream metallization and electromigration degradation. To address this concern, oxygen levels were reduced both in liquid and the environment of the chamber by purging nitrogen [25]. In dHF solution, oxygen concentration reduction from 7 ppm to <30 ppb was reported by purging N_2 in the liquid. N_2 purge solutions are referred as deoxygenated solutions. Cu etch

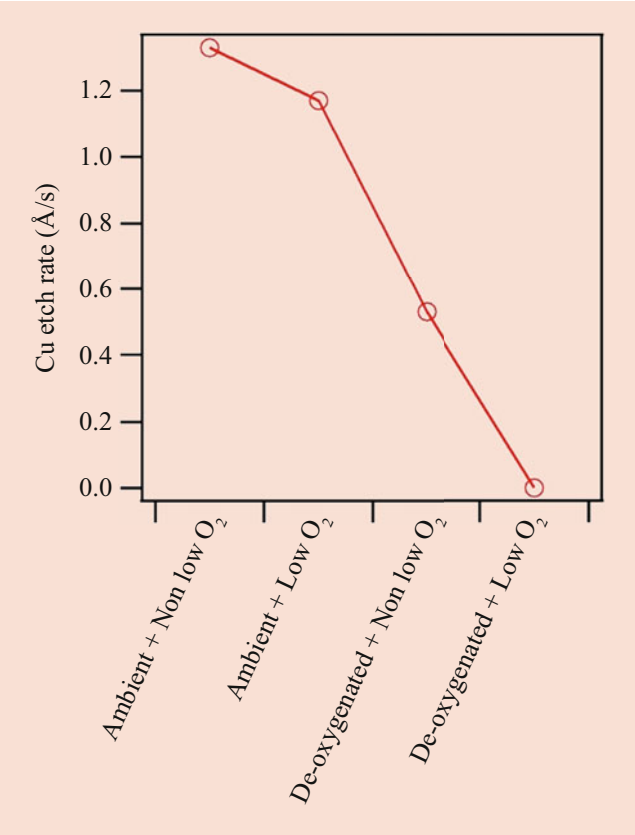


Fig. 6.8 Copper etch rate (Å/s) under varying chamber and liquid dHF conditions [25]

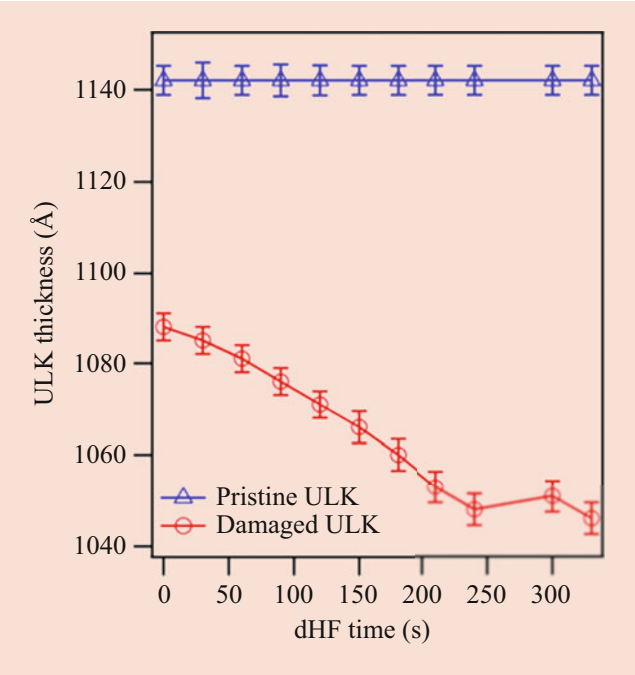


Fig. 6.9 ULK thickness loss as function of dHF time

rates under ambient and deoxygenated dHF solutions with and without low O_2 chamber conditions for as-deposited (electroplated) Cu films are shown in Fig. 6.8 [25]. The etch rates were measured using x-ray fluorescence (XRF) technique. Copper etch rate of 1.3 Å/s was measured for the non-deoxygenated solution and non-low O_2 chamber condition. Reducing the oxygen level below 30 ppb in the low O_2 chamber slightly decreased the etch rate to 1.1 Å/s. Deoxygenating the solution with N_2 purging significantly reduced the Cu etch rate ($\sim 3\times$). Deoxygenated dHF solution and low O_2 chamber condition showed the lowest Cu etch rate of ~0.1 Å/s. The importance of both deoxygenation and low O_2 chamber environment is required to control copper etch rate during the post-via etch cleaning steps, which is critical to avoid any excessive Cu etch at the via bottom.

- **Excessive ULK removal**: It is important to control the amount of damaged ULK removal to avoid increase in critical dimension (CD) and undesirable profiles for metallization. For this reason, dHF concentration must be ultra-dilute (>1000:1 H_2O:HF). Figure 6.9 shows negligible etching of non-damaged or pristine ULK film in dHF-based (0.05 wt% HF) solutions even in prolonged treatment time of up to 3 min [25]. In the case of a damaged ULK film (simulating via sidewall by exposing ULK to partial plasma etch), an etch rate of 0.1 Å/s was observed. This example shows that the amount of damaged ULK removal can be controlled both by concentration of HF and wet clean process time.

(e) Hardmask Wet Etch

In BEOL, a metallic hardmask, titanium (Ti), or titanium nitride (TiN) is commonly used as a patterning for Trench-First-Metal-Hard-Mask (TFMHM) scheme, achieving smaller dimensions and high aspect ratios during etch processes [27–29]. For BEOL pitch of ≥64 nm pitch, post-via etch clean is immediately followed by metallization of barrier/liner/Cu to fill the trenches and vias. However, void-free metallization became challenging for sub-64-nm pitch structures due to the incoming profile after post-via etch wet clean [29]. Figure 6.10a shows the TEM cross section of 48-nm pitch (23-nm metal CD) trench structures with ultralow-k (ULK), dielectric hardmask (HM), and metal HM in the stack [28]. In this example, titanium nitride (TiN) is used as metal HM. The re-entrant profile and undercut under at the interface of dielectric HM and ULK are the main reasons for the voids observed during metallization as shown in cross section, Fig. 6.10b, and top down of scanning electron microscope image, Fig. 6.10c.

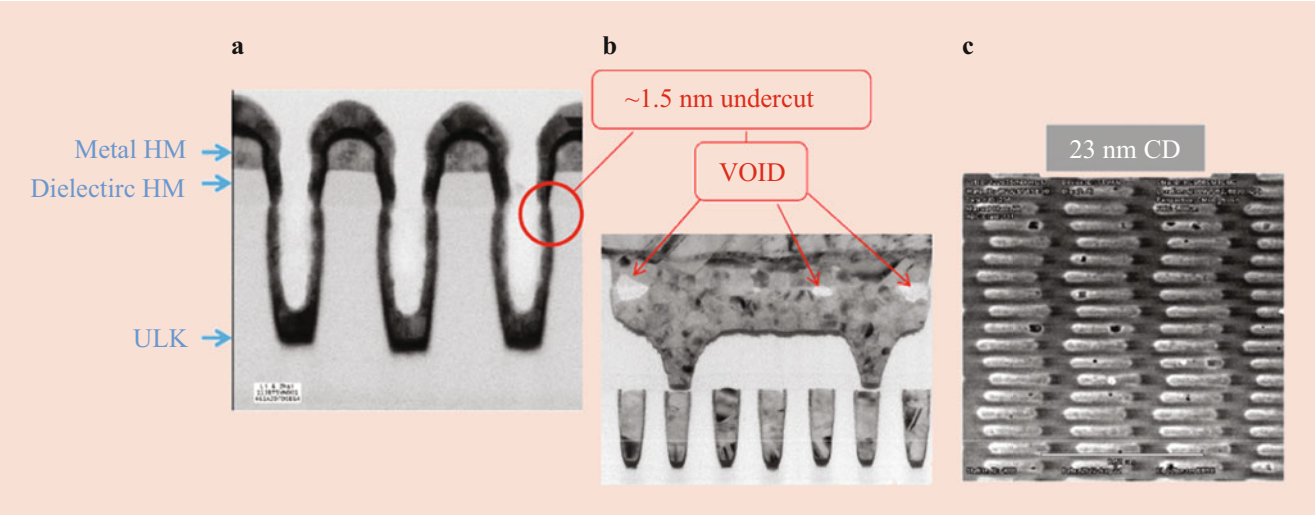


Fig. 6.10 (**a**) TEM cross section pre-metallization, (**b**) TEM cross section post-metallization, and (**c**) SEM top-down image post-CMP

To address the gap fill challenge, MHM needs to be removed before the metallization. Hence, it is essential to remove MHM selective to ILD materials, metals including Cu, Co, and TaN. To enable this, plasma dry etch or wet etch solutions were evaluated in industry [30]. Plasma dry removal of TiN was not successful due to the excessive damage of ULK that results in poor time-dependent dielectric breakdown (TDDB) in reliability test. Wet etch is very attractive for this application as ULK damage can be minimized. However, none of the commodity chemicals can be directly applied here due to low etch rate or incompatibility with the exposed materials. For example, dHF solutions do not have appreciable TiN etch rate, and concentrated or extensive exposure of dHF solutions leads to ULK damage as described in post-via etch clean section. On the other hand, chemistries like SC1 and SC2 are capable of etching TiN but are not compatible to the metals (Cu, Co) that are exposed at the bottom of the via. Due to these challenges, this application required development of a "custom chemical mixture."

At metal levels > M1, TiN HM wet etch needs to be compatible to M1-level Cu that is exposed at the bottom of the via like shown in Fig. 6.7. Several vendors developed custom chemical solutions for this application [31, 32], and in general the chemical mixture includes four key components mixed with DI water:

- Oxidizer – to oxidize TiN
- Corrosion inhibitor – to passivate metal (in some cases dielectric too)
- pH-adjusting agent – to adjust pH
- Chelating agent – to complex metal ions and form stable soluble compound

In addition to the four key components mentioned above, other chemical additives are added at very low concentration (<5%) for further stabilization and improved compatibility with exposed materials. For oxidizer, hydrogen peroxide is proven for this application with the following reaction with Ti^{3+}-forming soluble Ti^{4+} compounds in water [33]:

$$Ti^{3+} + 3/2\ H_2O_2 + 4OH^- = [TiO_2(OH)_3]^- + 2H_2O$$

For TiN wet etch, higher temperature gives faster TiN etch rate as TiN etching follows Arrhenius temperature behavior. For every 10 °C increase in temperature, the etch rate almost doubles. The pH of the mix solution is preferred to be in the range of 6–9 due to required compatibility with ULK films and better stability of H_2O_2. Corrosion inhibitor is added to passivate Cu and Co metals that are exposed at the bottom of via. Typically, in these solutions, Cu and Co etch rates are <2 Å/min compared to TiN etch rate of ~120 Å/min at 65 °C. At the same conditions, no etch rates were observed for pristine and damaged ULK. In contrast to the top-down SEM and TEM cross-sectional images shown in Figs. 6.10 and 6.11 shows void-free gap fill when TiN HM is removed with a wet etch. This was a clear technology enabler at 48 nm pitch, and a new wet step is introduced in manufacturing.

Figure 6.12 shows summary of two products evaluation for TiN HM removal. Product A clearly shows later attack of Co at the bottom of via, and product B was optimized with corrosion inhibitor for Co and shown to have good compatibility with Co. Retention of Co cap is critical for electromigration.

Finally, reliability evaluations with and without TiN wet removal were summarized in Fig. 6.13. Three times improvement was observed in upstream electromigration, and no degradation was observed in TDDB. This result indicates minimal to no damage to ULK with TiN wet removal

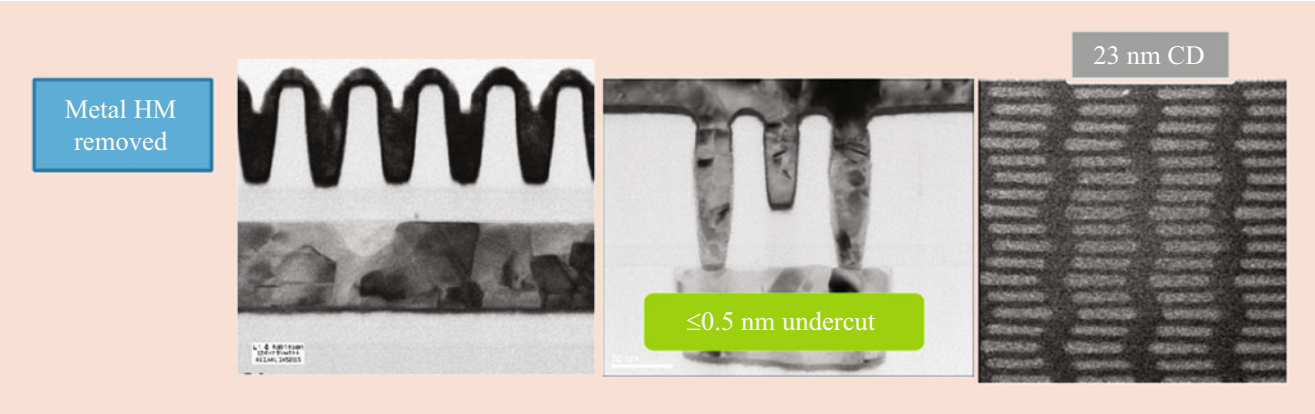


Fig. 6.11 TEM cross-sectional of (**a**) line (**b**) via and (**c**) top-down SEM images of 48-nm pitch structures with TiN HM removed prior to metallization

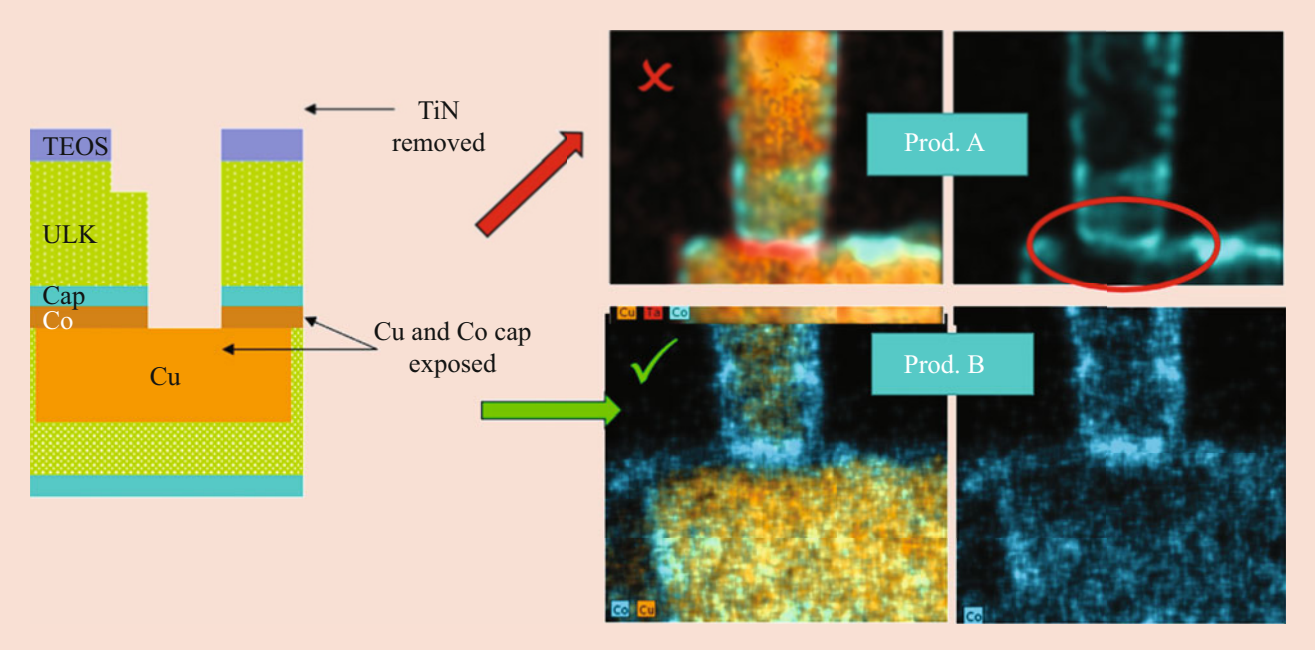


Fig. 6.12 Importance of corrosion inhibitor in TiN removal chemistry and in its role of protecting Co at via bottom. Product A is without corrosion inhibitor, and product B is with corrosion inhibitor

chemistry and gap-fill improvement due to metallization friendly profile.

In summary, wet cleans are widespread in every module of the fabrication of BEOL copper interconnects. The applications have extended from a mere particle clean with SC1/SC2/dHF to specialized custom chemical mixtures to clean and wet etch various materials. Single wafer tools made it possible to achieve defects <50 nm and excellent across wafer temperature and uniformity control. Additional chamber developments controlling oxygen concentration in chamber to sub-100 ppb levels enabled minimal metal corrosion in advanced interconnect features for post-via etch cleans. Metal hardmask wet etch opened gates for several formulated chemistries from vendors and is now implemented in manufacturing for ≤14 nm technologies. As traditional technology node scaling becomes increasingly difficult, wet clean and wet etch needs continue to increase to enable novel integration schemes.

6.2 Cu Electroplating

A brief survey of the literature shows that copper and copper electroplating have been active areas of material research for about the last 20 years, no doubt driven by the adoption of electroplating as an enabling copper interconnect process in the late 1990s. This is reflected qualitatively in the literature trends; an internet search shows that the number

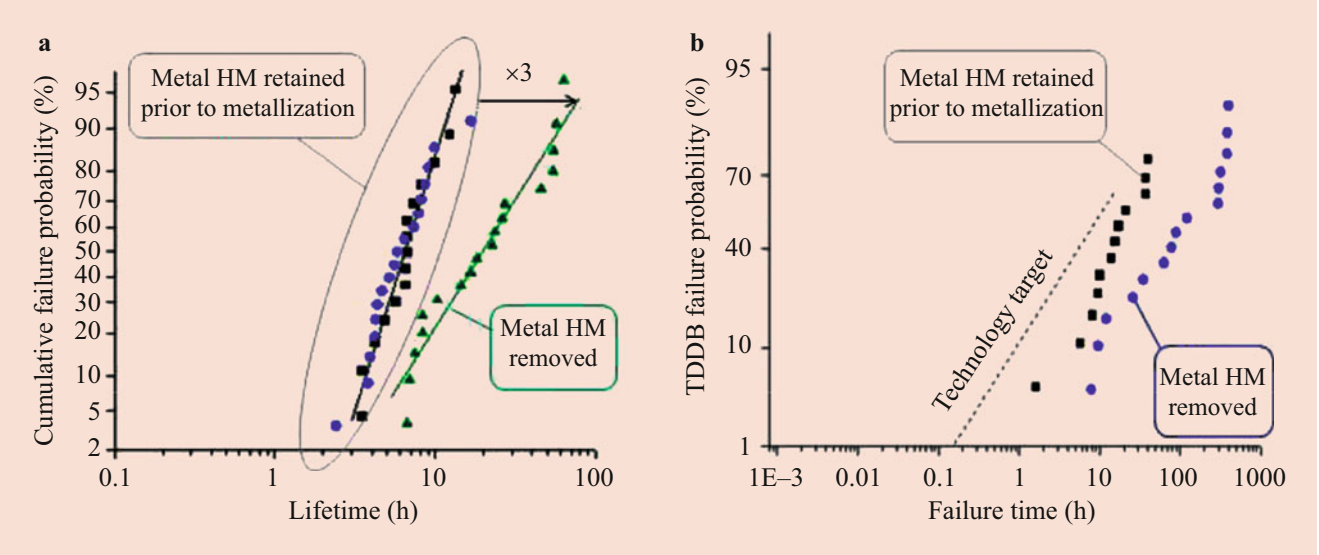


Fig. 6.13 Electromigration and TDDB summary with and without TiN HM wet removal. (**a**) 3× improvement on upstream electromigration. (**b**) No TDDB degradation

of publications with occurrences of "copper electroplating" from 2011 to 2015 was over ten times greater than that between 1991 and 1995 (just prior to the announcement of electroplated Cu interconnects). Although research interest in copper electroplating may be starting to plateau somewhat (the period between 2016 and 2020 appears on track to finish with less literature occurrences of copper electroplating than the prior 5-year period), technological challenges in the field of plating for BEOL are in contrast increasing rapidly. Small BEOL feature sizes at advanced nodes complicate extending conventional electroplated Cu interconnect approaches, with new copper fill techniques and new interconnect metals being considered as alternatives at small dimensions [34, 35]. In this chapter section, we will give some background on the initial electroplated copper interconnect work, describe the basic mechanism of how Cu is plated in interconnect features void free (and associated models), cover some of the relationships between electroplating processes and interconnect performance, and then discuss some future electroplating challenges for both copper and some new possible interconnect metals. We note that several excellent reviews on the application of copper electroplating in BEOL processing are available [36–42]. We build here upon this previous work with more recent data, attempting to emphasize the influence of electroplating process and chemistry on 300-mm wafer BEOL yield and reliability where possible, using internal results as well as some selected from the literature.

6.2.1 Background

The electrodeposition or "electroplating" of metals has found use in numerous industrially important applications to produce protective, functional, or decorative metal coatings and fully formed objects [43–46]. Among these applications are several related to microelectronics and semiconductor technology [47, 48]. Compared to other film deposition methods, key advantages of electrodeposition include the ability to produce relatively thick, sound, high-purity metal and alloy films with tailored properties in nonplanar geometries. Since many metals and alloys can be electrodeposited at or near room temperature with relatively low-cost and straightforward chemistries and equipment, these processes can be successfully scaled up and implemented in high-volume manufacturing. Examples include several decades of copper, nickel, and chromium plating in the automotive industry as a metal finishing treatment for bulk metal parts [43, 45]; multiple generations of copper, nickel, gold, and solder alloy plating for microelectronic packaging since the 1970s [49–52]; and more recently for about the past 20 years superconformal copper electroplating in semiconductor fabs worldwide for on-chip BEOL interconnects [53].

Some of the history behind how electroplating was selected as the preferred Cu interconnect fabrication process at IBM is described in references [37] and [53]. Multiple Cu deposition approaches were evaluated besides electroplating, including electroless, chemical vapor deposition (CVD), and a few different types of physical vapor deposition (PVD). Electroplating was the only deposition technique at that time that could "superfill" Damascene features with copper, i.e., fill faster at the feature bottom than at the feature top and sidewalls, enabling a void and seam-free copper interconnect. The superfilling effect is shown in Fig. 6.14, where the bottom-up copper fill of the high aspect ratio feature is evident. Without a significant local deposition rate difference

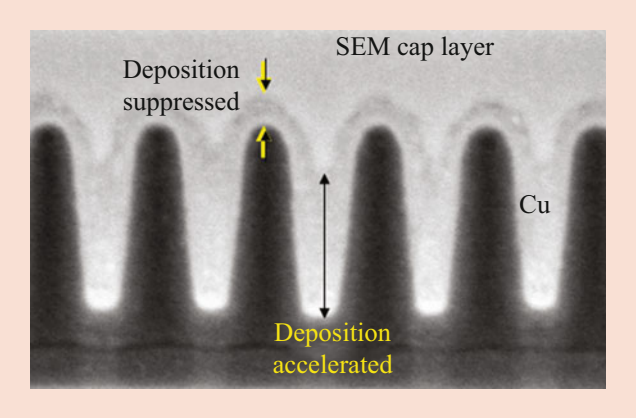


Fig. 6.14 Superfilling effect shown by scanning electron microscopy (SEM). Electroplated copper (dark gray) fills the features etched into the dielectric (black). The thickness deposited into the etched areas is higher than that outside the features, enabling void-free fill. The light gray layer at the top of the micrograph is an SEM encapsulation layer

between the feature bottom and sidewalls, a seam or void would be visible (see, e.g., Reference [39]). We distinguish true superfilling from the phenomenon of "geometric leveling"; in the latter case, certain conformal fill processes appear to be bottom-up due to the feature geometry (this typically occurs for geometries with much lower aspect ratio than conventional BEOL features; see references [54–57] for a discussion of this effect). Since these plated interconnects had the best characteristics, work continued on integrating electroplated copper in the BEOL. We should note that some of these initially unsuccessful, alternative deposition methods from copper interconnects' early days have attracted interest again as the conventional electroplated copper fill approach encounters scaling difficulties (this will be discussed later in this section).

6.2.2 Cu Plating Chemistries

Current BEOL Cu plating baths are sulfate based, with copper sulfate providing the metal species to be electrochemically reduced and sulfuric acid the electrolyte conductivity (there is also typically a small amount of chloride ions, historically added to promote copper anode corrosion, but also helping in the function of the organic additives [58–60]). These sulfate baths displaced older chemistries where a complexing agent such as cyanide or pyrophosphate was employed to promote a good copper electrodeposit morphology and to prevent poor plated adhesion from a copper "displacement" reaction on less noble substrates (such as zinc, steel, etc.). References [43] and [51] discuss the limitations of these older copper chemistries and why they fell out of favor. Good quality copper plating from the new sulfate baths (sometimes referred to as "acid copper plating") would not be possible without organic additive systems that were developed in the 1970s that enabled low resistivity, ductile copper [61–63]. Once work using these baths for copper interconnect plating started, it was discovered that these organic additives are also critical for copper superfilling.

Typically, three types of additives are used in copper baths for interconnect plating [38, 39, 41]. The first type, known as suppressors (or less commonly "carriers"), are polymers usually employed at fairly high concentrations such that they are not very sensitive to mixing or transport conditions [38, 39] and strongly inhibit copper electrodeposition when chloride ions are present. The second type, accelerators, are sulfur-containing molecules that strongly adsorb on the copper surface, displacing the suppressor and hence increasing the local Cu deposition rate relative to the fully suppressed state. Levelers, the third class of additive, are usually aromatic nitrogen-containing molecules (Janus Green B is one model leveler) employed at low concentrations and also deposition-inhibiting species. Being dilute, they are more sensitive to transport or mixing conditions and thus act to smooth or level out any protrusions in the substrate surface (see references [54–57] for a discussion of this mechanism). One should note that to achieve superfill, only the first two additive types are necessary, suggesting that the interaction between the suppressor and accelerator is the most important aspect in the superfill mechanism [38, 64, 65].

The impact of the suppressor and accelerator on copper deposition kinetics (in other words, how easily the cupric ions in solution are reduced to copper metal) is shown schematically in Fig. 6.15 for a copper substrate (leveler effects on copper kinetics won't be discussed here, but the reader is referred to references [66, 67] for a discussion of this topic; levelers will be discussed later with respect to their impact on electrodeposited copper surface topography and potential for disrupting copper superfilling). Curve A represents the cathodic current density (shown on the y-axis and proportional to the copper deposition rate through Faraday's law) as a function of the electrode potential (the x-axis) when no additives are present. The isolated electrodeposited Cu crystallites obtained in the absence of additives are shown qualitatively also [68, 69]. As stronger cathodic potentials are applied, the current density rapidly increases once the copper reduction potential is attained. After adding a suppressor to the bath, a similar cathodic potential sweep results in curve B; deposition current does not start to increase until the electrode is much more cathodically polarized, reflecting a suppression or inhibition of the copper electrodeposition reaction. The adsorption of the suppressor on active growth sites to inhibit Cu deposition is shown qualitatively as well. For both curves A and B, the observed current density is identical for both the forward and reverse potential scans, suggesting that the copper deposition kinetics are essentially reversible with and without suppressor. Finally, curve C shows the impact of the addition of an accelerator species to a

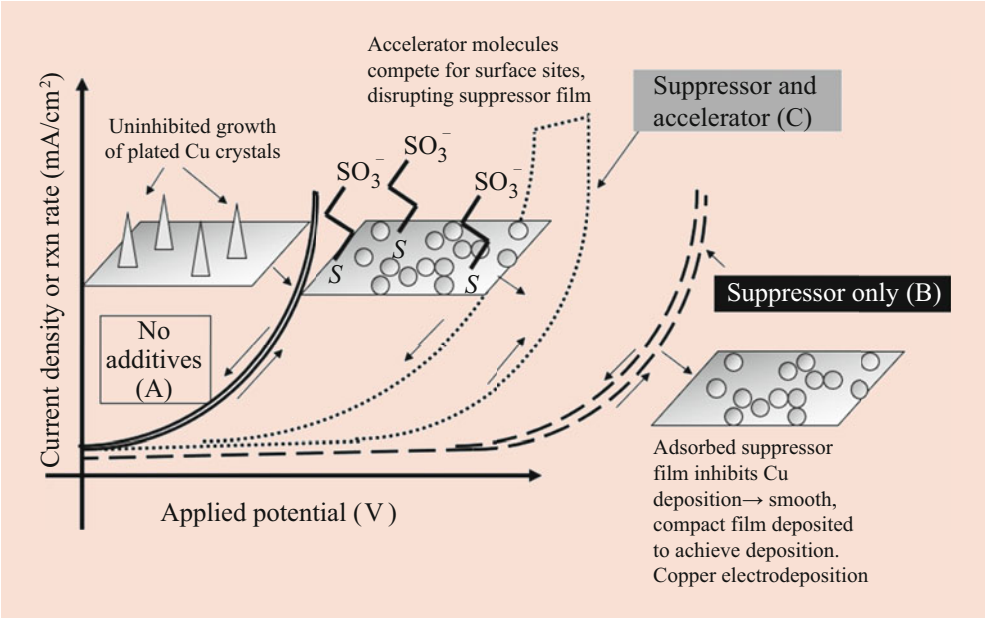


Fig. 6.15 Schematic polarization curves for an acid-sulfate copper bath, with additives as indicated. In the case of no additives (A), isolated uninhibited deposited crystals emerge. When a suppressor is added in (B), copper deposition is inhibited, requiring larger applied overpotentials to achieve deposition. Copper electrodeposit morphology is improved, with a denser film resulting. No polarization hysteresis occurs. When an accelerator and suppressor are used together (C), hysteresis for the copper deposition polarization results

bath with suppressor. As expected for the accelerator, the Cu deposition reaction is less polarized, with a given potential having a higher current density (or deposition rate) as compared to the fully suppressed condition exhibited by curve B (the displacement of the suppressor by the accelerator molecule is shown qualitatively also). Another characteristic appearing with the introduction of the accelerator to the suppressor-containing chemistry is the hysteretic nature of the polarization curve, i.e., deposition currents are higher on the return scan as compared to the forward one. This hysteresis shows that when an accelerated (or high deposition rate) state is achieved, it tends to persist with these additives. Physically, this could be understood as a tendency for the accelerator to remain adsorbed on the copper surface and allow copper deposition to freely occur once the suppressor has been displaced. Reid provides a more detailed discussion of these aspects in Reference [39]. These additive characteristics are the basis of most superfill models in that a locally high copper deposition rate at the feature bottom and/or a highly suppressed one at the feature top leads to a bottom-up Cu fill (superfilling).

Many models have been developed to explain copper superfilling; earlier models emphasized the inhibition of copper electrodeposition at the feature top [36, 70], while later ones focused on a locally higher accelerator coverage at the feature bottom to explain the bottom-up fill effect [41, 64, 65]. Since these later models were consistent with the observation of copper superfill in the absence of leveling additives (and also with the experimental observation of "bumps," or regions of locally high Cu thickness just over Damascene trench features after superfilling [64]), they have become generally accepted. Figure 6.16 shows schematically how a locally high accelerator concentration may occur at the feature bottom due to changes in the copper surface curvature as metal is deposited. Simply put, as copper deposition occurs, the two surfaces from the two trench bottom corners meet, forming a copper surface of very pronounced curvature. The additives that were initially distributed uniformly across the copper surface become packed together as the two deposition fronts from the trench bottom meet. Since the suppressor is usually present at a fairly high concentration with its inhibiting effect saturated, no additional suppression in the copper growth rate occurs with the increased copper surface curvature. But the accelerator is added in a concentration range where higher surface coverage results in an increased copper deposition rate; thus, the "crowding" of accelerator at the feature bottom leads to a faster local plating rate. Though this type of mechanism is more or less accepted, other copper superfill models emphasizing additional aspects have continued to be proposed [71–73]. While the exact mechanism of additive superfilling is still studied and debated, a number of effective additive packages for copper superfilling have been commercially available since electroplated copper interconnects became mainstream in the late 1990s [41, 74–77]; these initial additive sets have evolved over the years to maintain good copper gap fill in the face of shrinking BEOL feature dimensions and increasingly limited PVD copper seed coverage.

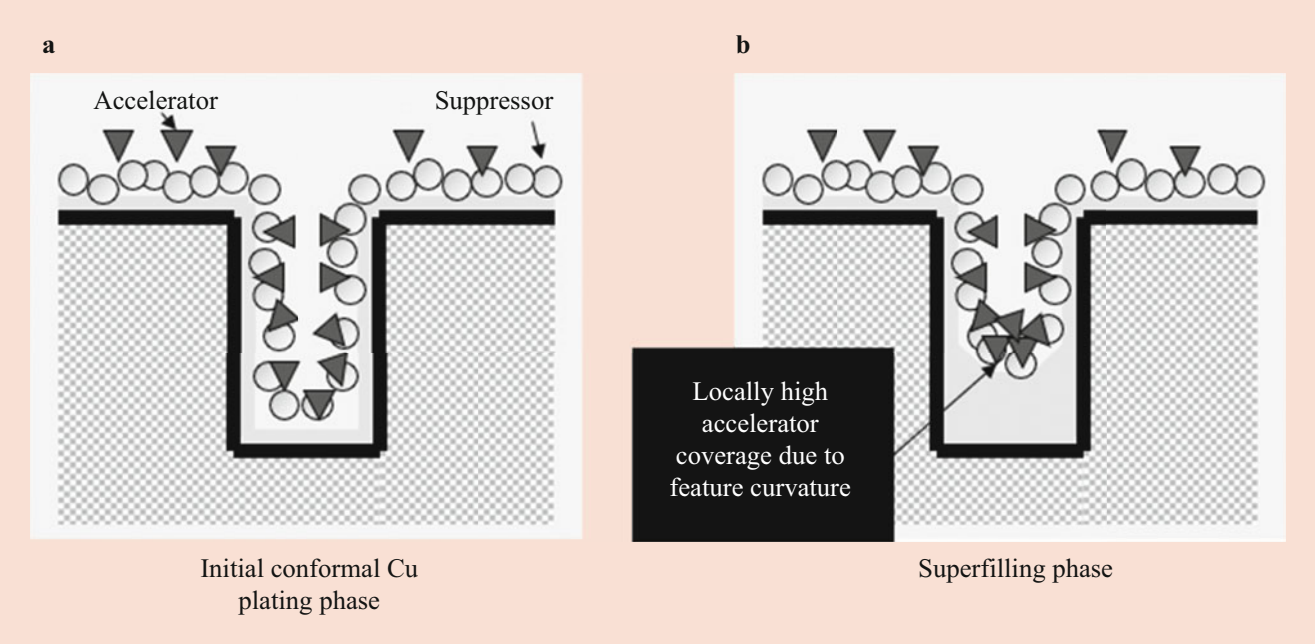


Fig. 6.16 Schematic illustration of the superfilling mechanism. Initially (**a**), additives are adsorbed uniformly across the copper surface. As filling proceeds and the copper bottom surface curvature changes (**b**), the additives become locally concentrated

It should be noted that superfilling is not unique to copper. Damascene features have been superfilled with other electrodeposited metals such as silver, gold, nickel, and cobalt [78–82]. Some of these metals could be of interest as potential replacements for copper as it becomes more difficult to scale to smaller feature sizes (this will be discussed later).

6.2.3 Tooling for Copper Electroplating

The superfilling characteristics of copper plating chemistries discussed in the preceding section could not be leveraged for BEOL interconnect fabrication without appropriate equipment for handling, immersing, electroplating, rinsing, and then drying a copper-seeded silicon wafer [38, 40, 42, 83]. Such equipment is known in the industry as a "tool." With current state of the art technology interconnect sizes approaching just 20 nm in width (and even smaller ones in development), the Damascene features are fully filled in less than a second or two of plating [42]. It is interesting to compare this to fill times for one of the early copper interconnect technologies where features were only partially filled after 20 seconds even with a current density (i.e., deposition rate) much higher than that typically used today [84]. In just under a second or so, today's copper plating tools must fully immerse a wafer in the electrolyte without entrapping any air bubbles or wetting defects, distribute the additives in the bath uniformly across the wafer surface, and allow them to adsorb, all the while carefully controlling the potential or current between the copper-seeded wafer (acting as the cathode) and the copper anode to protect the PVD copper seed from corrosion (most typically by dissolved oxygen in the bath), nucleate plated copper on the seed, and initiate copper fill. Since they have the smallest copper volume, the narrowest (and hence most challenging) Damascene features are the first to fill, usually within a second or less. This process is shown schematically in Fig. 6.17 (of course, commercially available plating equipment for the semiconductor industry is much more sophisticated than the sketch here). A description of a more advanced wafer entry waveform is in reference [85]. Another process aspect that has been engineered over the years is the wafer-scale plated copper uniformity, both in the initial stages of the fill (to have uniform plated copper nucleation and fill rate across the wafers) and the final wafer thickness distribution (to facilitate the subsequent planarization of the plated copper overburden) [42].

For high-volume production, the tool must process a considerable number of wafers each day; as a result, any aging or breakdown of the plating chemistry from this heavy use must be minimized to maintain good quality copper gap fill. A tool may have many hardware features to ensure good quality copper fill and keep defectivity low over time during production (most of these are proprietary and hence can't be discussed here), but among them perhaps the most important is an analysis and dosing system to maintain the additive chemistry within control limits. Since the additives impact the copper deposition kinetics, electrochemical methods are convenient to measure the concentrations of the various

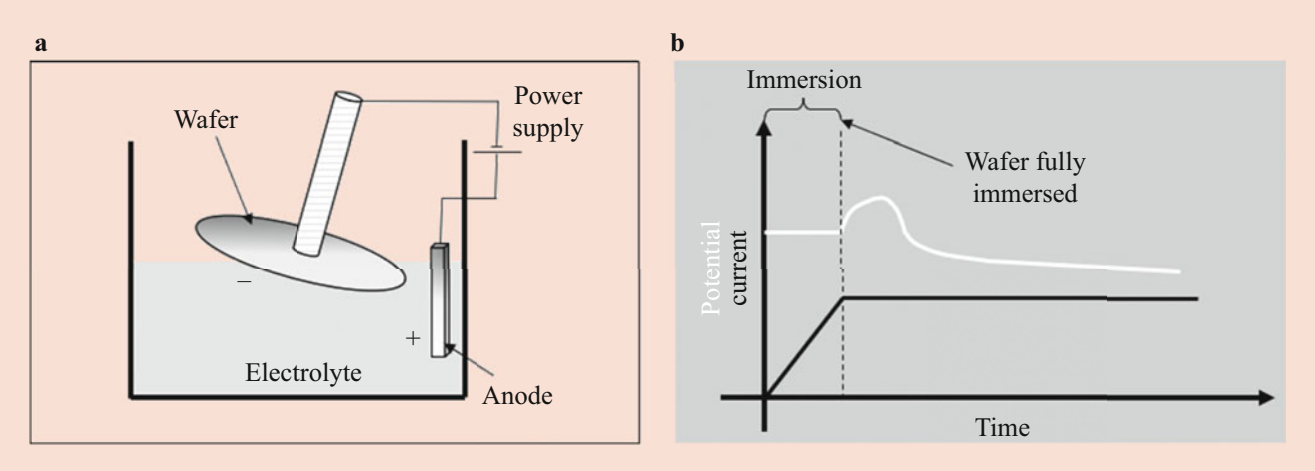


Fig. 6.17 Simplified sketch of electroplating equipment (**a**) and waveform control (**b**). A power supply controls the potential and current between the wafer (the cathode) and an anode. The waveform manipulation is synchronized with the mechanical movement and immersion of the wafer into the electrolyte so as to provide optimal filling

organic species in the bath (the inorganic species can be measured electrochemically or with other techniques) [86, 87]. Typically, the analysis method is validated by testing a known standard solution periodically.

6.2.4 Copper Electroplating, BEOL Yield, and Reliability

Since successful plated copper fill of Damascene structures relies on a continuous coating of PVD Cu seed, both copper plating and seed must be developed in tandem for a given feature geometry. If the feature geometry or seed process changes (e.g., an intentional change due to a new integration requirement or an unintentional one from a process drift), the copper plating process often must be re-optimized. The relative quality of the copper metallization is typically gauged while the wafers are still in the fab (through in-line electrical testing of test macro-yield and defectivity inspections) [88–91] as well as during post-fab characterization (usually reliability and quality assurance testing) [92]. Yield can be very sensitive to voiding originating from either the barrier/seed or plating process, while electromigration reliability tends to be more strongly influenced by interfacial adhesion quality and thus more dependent on the barrier/seed process.

An example of the interplay between seed and plating processes is shown in Fig. 6.18. The current flowing through a dual-Damascene viachain (with a metal line and via critical dimension or "CD" of about 33 nm) is shown for wafers processed with three different copper additive chemistries (all had the same inorganic makeup but with additive sets provided by different vendors); two different liner/seed processes were used for each chemistry. A viachain is a convenient macro to evaluate metallization fill quality as one defect will cause a break in the metal chain, resulting in a blockage of current flow. Metallization with more defectivity will thus have a lower viachain current. If the structures are exposed to thermal budget, smaller defects will often coalesce into larger voids and further impede the current flow, allowing enhanced sensitivity to defect characterization by this method. For the plot on the left, it is obvious that all chemistries perform well with liner/seed process 2, while for liner/seed process 1, they are all worse, with similarly low yields. By applying a long thermal budget (similar to what the structures would be exposed to by being built up and packaged), all wafers suffer some yield degradation, but chemistry B appears to be a bit better than the others for wafers with liner/seed process 2 (as expected, liner/seed process 1 shows further yield degradation with more temperature exposure). It is only possible to distinguish between chemistry performance with the more optimized liner/seed process, and only then after applying some thermal budget to induce some yield loss. These differences in chemistry could be related to differences to the additive molecules themselves or their relative concentrations (in this example, the vendor-recommended concentrations were used). Although most vendor additives are from the same general class of compounds, subtle differences may exist that can lead to large differences in Damascene fill performance; see, for example, articles by Reid and coworkers on suppressor and leveler additive effects [39, 42, 93].

Even for a single additive chemistry, the concentrations of the additives and other inorganic species can be important in achieving good parametric yield. Figure 6.19 shows viachain currents for both short and long via chains having about 28-nm metal CD processed with the same additive chemistry but with changes in concentrations for some of the constituents. All conditions perform well for the short viachain

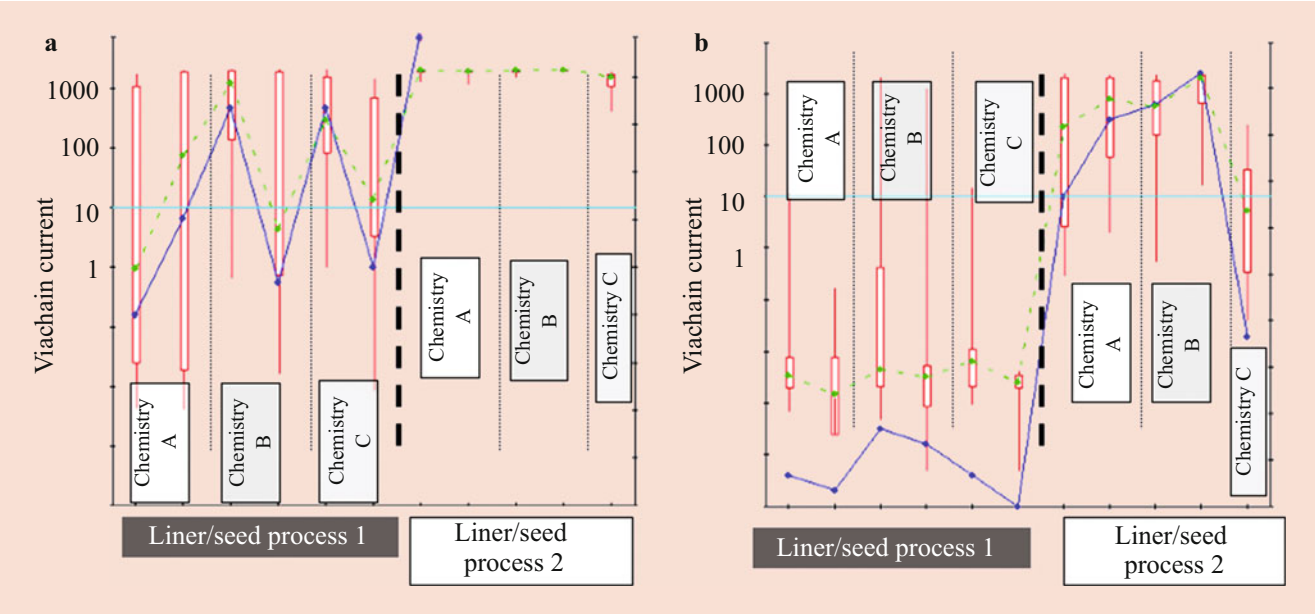


Fig. 6.18 Viachain test current for various chemistries and liner/seed processes as shown (higher currents suggest better quality fill). (**a**) at-level test. (**b**) post high temperature anneal test data. The top and bottom of the whiskers in the plot represent 5% and 95% of the data population, respectively, while the top and bottom of the box represent 25% and 75% of the data population, respectively. The point in the middle of the box is the median value. Each set of data values is taken from a number of chips on a single 300 mm wafer. Both liner/seed and plating chemistry affect copper fill quality

macro, but for the longer chain (which is more sensitive to defects), some differences are apparent. The reference split (marked "A") is a concentration set for this additive package that was widely used for some time in the industry. Split condition "B," with a significantly higher accelerator concentration than split "A," has much better yield, with about 50% and 30% of tested chips having the expected target current value for these conditions, respectively. Split "C" shows that an adjustment to the chloride ion concentration with the same accelerator content as in "B" gives a further yield improvement to about 80%. The last experimental condition in the plot is for a bath identical to that in split "A" but freshly made up (the one used for split "A" had been in use for some time in a fab). The improvement from the chloride ion level adjustment could be related to some interaction with the suppressor [58–60] resulting in faster superfill and/or better plated copper nucleation on thin PVD copper seed. The similar performance of a fresh bath and one in use (with otherwise identical chemical makeups) suggests that the lower yield for this chemistry is unrelated to any bath aging effects.

As alluded to in Fig. 6.19, in some cases, adjusting accelerator concentration can result in a copper fill improvement. Another example of this is shown in Fig. 6.20 by post-CMP top-down scanning electron microscopy (SEM) , where ~23-nm CD metal structures are processed with various accelerator concentrations (all other processing conditions were kept constant). Clearly, copper fill is significantly improved once a threshold accelerator concentration is surpassed for this chemistry and test structure. The mechanism for this improvement is not clear but, as described above for the case of improved copper fill and chloride ion concentration, could be related to a faster superfill and/or improved plated copper nucleation. Since most suppressors are present in concentrations such that their inhibiting effect is saturated, it is perhaps not too surprising that Damascene copper fill is more sensitive to accelerator concentration.

Although higher accelerator concentrations can potentially offer some copper fill improvement, some complications may occur with this approach. Figure 6.21 shows the copper mounding mentioned previously that develops in areas with high feature pattern density and how employing a leveler can lessen this effect (the beneficial impact of a leveler on CMP is discussed in references [94] and [95]). For a given accelerator concentration, a leveler can mitigate plated copper topography, but mounding can reappear as more accelerator is used. Figures 6.21 and 6.22 shows the shorts leakage for a comb-serpentine macro as the accelerator concentration is increased; shorts current gradually increases until the accelerator is ~3 times its initial concentration, when it rises significantly. Adding more leveler can suppress the increased mounding observed at higher accelerator concentrations (far right split on plot A), but as shown in part B, excessive leveler concentrations can also degrade viachain yield. These results are consistent with similar experimental work in reference [93]. The fill degradation is likely due

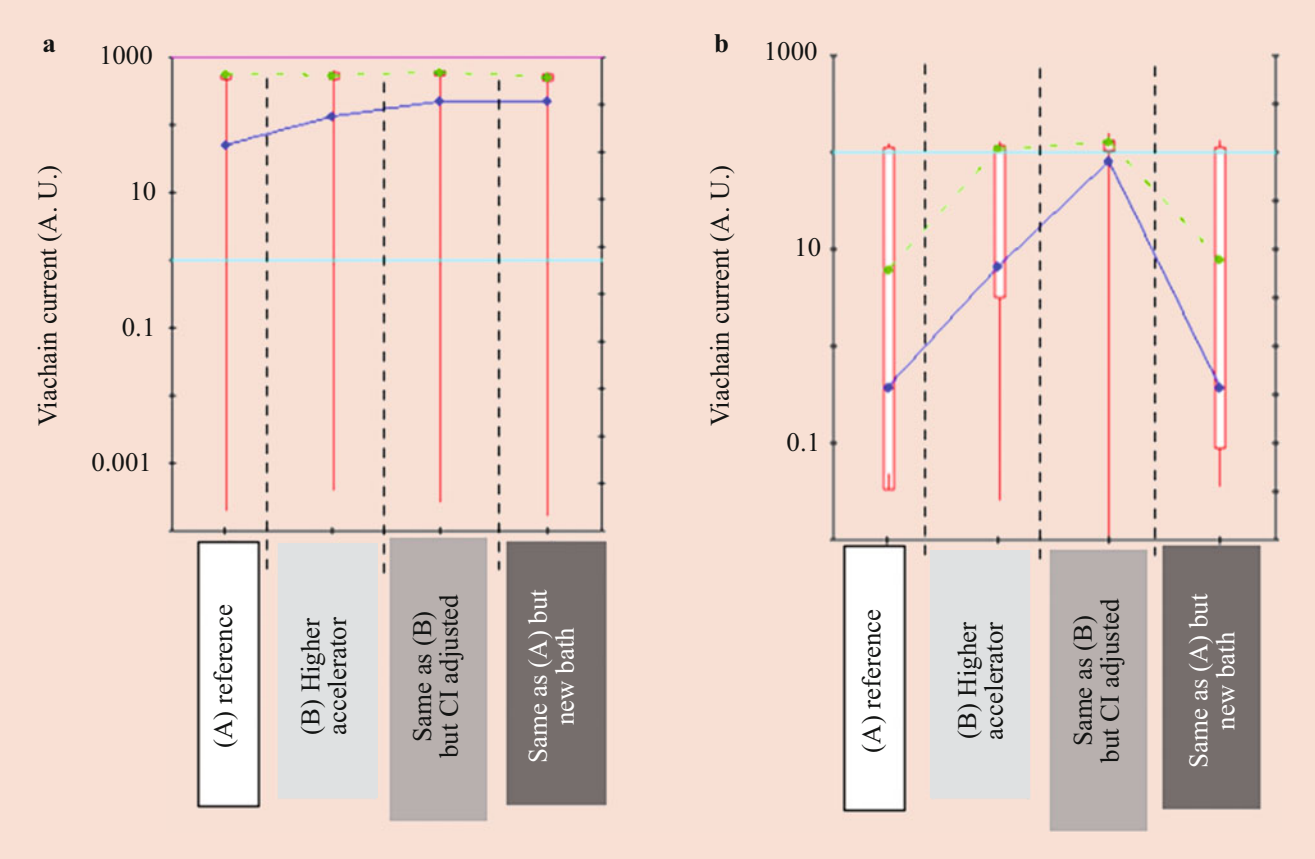


Fig. 6.19 Viachain test current for various chemistries (short viachain **a**, long viachain **b**). Chart symbols depicting the data distribution are as described in Fig. 6.18

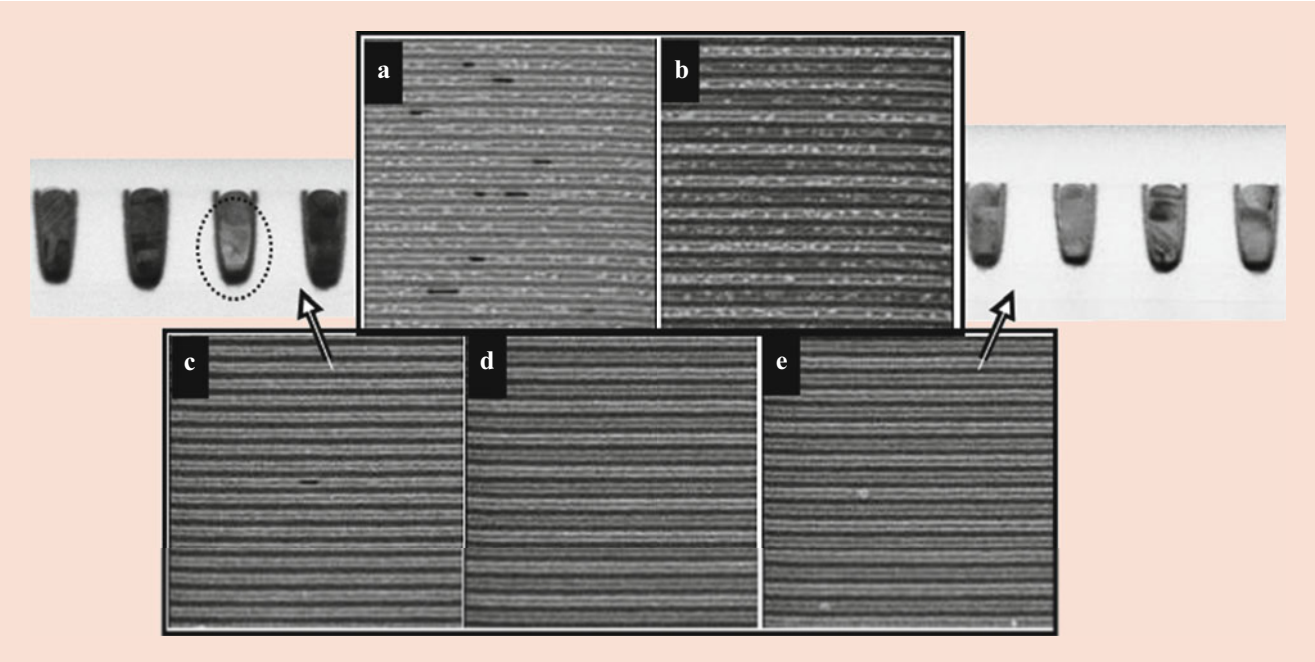


Fig. 6.20 Top-down post-CMP SEM images of metal lines filled with various accelerator concentrations. (**a**) reference accelerator concentration. (**b**) 1.6× reference concentration. (**c**) 2.3× reference concentration. (**d**) 3× reference concentration. (**e**) 3.3× reference condition. Insets show transmission electron microscopy images for conditions as shown (circle indicates likely void). Fill generally improves for these structures and liner/seed with increased accelerator

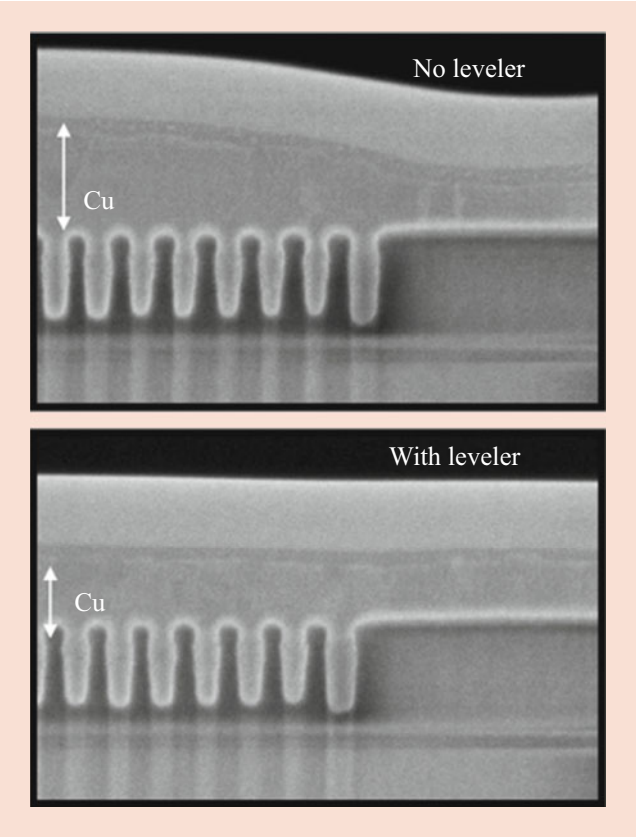


Fig. 6.21 SEM cross section post-plating with and without leveling additive. (Reproduced with permission from Kelly et al. [94]. Copyright © 2013 Elsevier Masson SAS. All rights reserved)

to an interference of the leveler molecule with the superfill mechanism (Zhou and Reid discuss leveler effects on copper Damascene fill in detail) [93].

As Damascene copper additive packages have matured over the years with improvements in fill performance from new additives becoming more modest, other avenues for engineering copper plating processes have been explored. One such approach is using a low cupric ion concentration plating chemistry. Historically, a bath with a low copper content was not often discussed as a tactic for improving plated copper fill; given their limited deposition rates, such electrolytes likely did not seem like a preferred option for the thick copper overburdens required to fully fill the Damascene features on early BEOL technologies. Zhou and Reid discuss improved fill on 48-nm CD features with low copper baths, along with likely mechanisms based on electrochemical measurements [96]. In their study, low copper baths showed enhanced deposition polarization, higher plated copper nucleation densities, and better solubility and wetting of the suppressor [96]. Another recent study shows improvement for low copper baths on 24-nm dual-Damascene features with PVD Cu seed and a CVD Co liner [97]. Figure 6.23 shows electrical data for a 15,000 link viachain, ISOVIA, and wire resistance macros for a reference chemistry with 40 g/L copper and a low copper one. Test data for these structures is shown after they received more thermal budget to simulate the build of the upper-level BEOL wiring. It is clear that the low copper bath has lower ISOVIA and wire resistances as well as a higher viachain current, suggesting better metal fill quality (the authors state the wire resistance improvement for the low copper bath could be related to line height variations due to CMP differences, but it is pointed out that the ISOVIA and viachain macros are not influenced by CMP and are likely better due to a low copper fill benefit).

Besides chemistry modifications to improve fill, modifications to waveform can be beneficial. Ahmed and coworkers employed an optimized entry waveform to repair a marginal copper seed on sub-50 nm structures, showing improved post-CMP defectivity, via opens, and electromigration (due to elimination of early fails) thanks to improved plated copper nucleation [85]. Jing and coworkers showed defectivity improvements by optimizing entry conditions and waveform for 28- and 32-nm technology node BEOL structures [98, 99]. Since plating wafer entry conditions and waveforms can be replicated by competitors without much difficulty, details on such process parameters and their favorable impacts are not widely discussed in the literature by chip manufacturers.

6.2.5 Extendibility of Copper Electroplating: Future Perspectives

The original approach of using PVD barrier and copper seed layers followed by electroplating was successfully employed with relatively minor adjustments for the first few copper BEOL technology generations. As interconnect dimensions decreased, much effort was spent in reducing the thicknesses of these barrier and seed layers (as well as improving their conformality) to provide as wide a gap opening as possible for the subsequent plated fill step. Similarly, copper electroplating chemistries and waveforms were optimized to tolerate narrow gap openings to maintain good plated fill when appreciable barrier and seed scaling were no longer feasible. It was recognized that this conventional metallization approach would eventually have difficulties extending to small feature sizes due to a couple of fundamental issues. The first limitation is a loss of copper diffusion barrier performance once the barrier layer is thinned below some threshold thickness (typically considered to be below 5 nm or so based on blanket wafer measurements [100, 101]). The second limitation is the oxidation of thin copper seed; since in some narrow features the seed can be as thin as a few nm, a significant fraction of seed can be oxidized [102], resulting in a fill void (copper oxide is not stable in the acidic plating electrolyte and readily dissolves) [103]. This challenge of achieving adequate barrier/seed coverage while maintaining

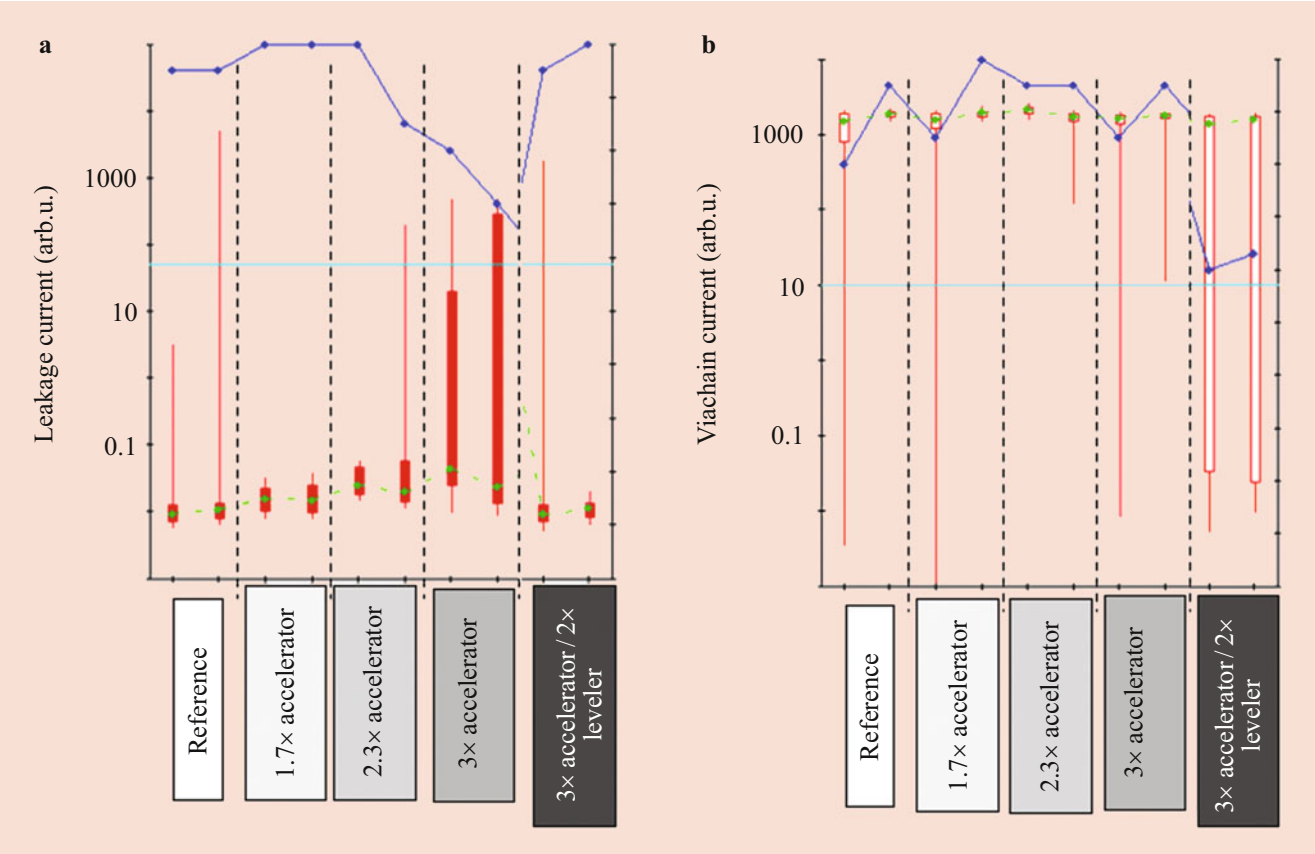


Fig. 6.22 (**a**) Shorts leakage for comb-serpentine macro with accelerator conditions as listed. As accelerator increases, shorts current rises once a threshold is passed. Adding more leveler restores shorts leakage to low levels. (**b**) Viachain currents for conditions as in (**a**). The increased leveler additive lowers viachain yield. Chart symbols depicting the data distribution are as described in Fig. 6.17. SEM cross section post-plating with and without leveling additive. (Reproduced with permission from Kelly et al. [94]. Copyright © 2013 Elsevier Masson SAS. All rights reserved)

a sufficient gap opening for plating is illustrated in Fig. 6.24. Dark-field transmission electron micrographs and associated energy dispersive x-ray (EDX) images for Co are shown for BEOL trench features just after copper plating with thick and thin PVD copper seed layers in Figs. A and B, respectively. A CVD Co liner, used in each case, can serve as an indication of the sidewall copper seed coverage quality as any exposed Co is attacked by the copper plating bath [97]. In Fig. 6.24a, a clear, uniform Co liner signal is visible with no evidence of any voiding at the sidewall interfaces, indicating good copper seed coverage. But a center void suggests that the gap opening is not large enough for defect-free copper feature fill. If the copper seed layer is thinned to enlarge the gap opening for better plated copper fill (shown in Fig. 6.24b), the center defect is eliminated, but sidewall voiding in the dark-field image and Co liner loss (note the nonuniform intensity of the Co liner signal) is evident (poor adhesion at the copper-barrier interface will significantly degrade reliability performance).

As a result of these expected difficulties in extending the Damascene copper seed and electroplating approach to future technology nodes, various BEOL metallization alternatives have been researched extensively for several years. A comprehensive review of these process alternatives is beyond the scope here, but some background will be given along with selected references for the ones that have attracted the most interest. To the authors' best knowledge, none of these approaches discussed below have been implemented in high-volume production at the time of this writing. For some of these schemes, some time has passed since any significant research activity has occurred (presumably due to the realization that some challenges inherent in a given approach were intractable), while for others some work is still ongoing.

One of the first alternative approaches considered was employing an additional copper plating step (sometimes using a copper plating bath with a neutral to alkaline pH) to "repair" any defects in the PVD copper seed before the conventional plated copper superfill step [104–106]. In some cases, fill could be improved on defective seeds with this approach. The most likely reasons this approach was not widely adopted are (1) the need for an additional copper plating step, ex-

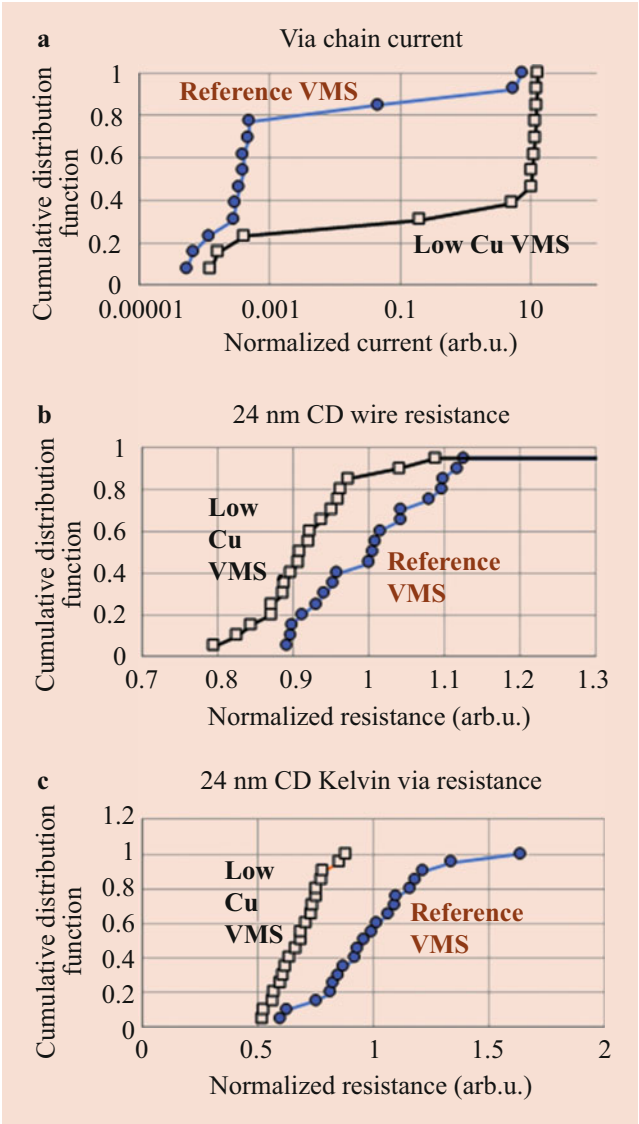


Fig. 6.23 Normalized viachain current (**a**), wire resistance (**b**), and ISOVIA resistance (**c**), expressed as a cumulative distribution plots. Low copper baths show better viachain yield and lower ISOVIA resistance. (Reproduced with permission from Reference [97])

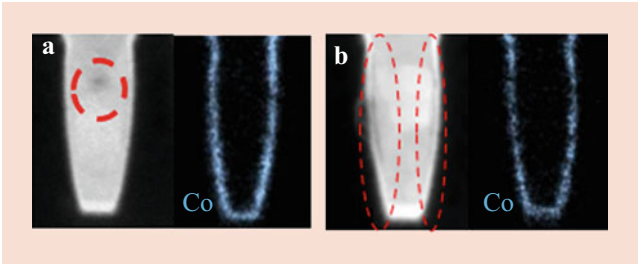


Fig. 6.24 (**a**) Dark-field scanning transmission electron microscope (DFSTEM) micrograph of trench feature with Co liner and thick Cu seed post-plating. While a center fill defect is present, no delamination is observed in the sidewall metal interfaces. The corresponding Co EDX map has a uniform intensity, suggesting that the liner is intact. (**b**) DFSTEM micrograph of trench feature with Co liner and thin Cu seed post-plating. Sidewall voids are visible, and liner discontinuities are noted in the Co EDX map. (Reproduced with permission from Reference [97])

acerbating pinch-off issues during superfill of narrow CD features, and (2) compromised reliability from a defective seed (although these baths can nucleate on thin seeds and/or exposed barrier and improve Cu fill, adhesion may still be compromised from an oxidized liner and/or barrier). Another early alternative metallization approach involved dispensing with the PVD copper seed altogether and plating directly on a CVD or ALD liner such as Ru or Co (that have higher conformality due to the CVD process), alleviating pinch-off constraints due to the PVD copper seed [107–117]. The main challenges with these "direct plating" approaches are (1) high incoming substrate resistance due to lack of PVD copper seed and (2) obtaining good adhesion at the copper/liner interface (see Reference [101] where electromigration results are given for direct plated copper on Ru). Since the liner is air-exposed, its native oxide can complicate achieving copper/liner adhesion quality sufficient to pass reliability as in the case of seed repair. For Ru substrates, there is an additional challenge of CMP with a noble metal liner [118]. Another approach that has been evaluated is via prefill, [119–122] where a metal (typically Co) is selectively deposited (usually electroless deposition, but other techniques have been demonstrated as in reference [122]) in the via only on top of the exposed underlying metal level; the subsequent line metallization level is then fabricated in the conventional way. Since the barrier metal is moved from the via bottom to the via top for this method, a via resistance benefit is expected due to the larger area of the barrier layer. Other benefits include a relaxed aspect ratio for copper plating and a less difficult geometry for liner/seed when the overlying line level is metallized. Challenges for this technique likely involve obtaining good selectivity for the metal deposition and achieving good reliability (the selectively deposited metal is not encapsulated in a diffusion barrier, so it must not move into the dielectric or contain any diffusing species). The last alternative copper interconnect approach discussed here is the "reflow" technique, where the copper electroplating step is only used to provide the bulk metal overburden as the finer features are filled with copper PVD and a subsequent anneal [35, 123–127]. Since the entire metallization process (including the copper feature fill) is carried out without breaking vacuum, the copper seed oxidation issue is overcome, and good interconnect reliability can be achieved. The main challenges with this approach are throughput (although thick PVD metal layers are not required, the subsequent annealing for the reflow can slow the process) and the filling of complex dual-Damascene geometries by reflow in high-volume production (fill is not truly bottom-up and instead relies on the movement or "wetting" of the PVD copper across the substrate with temperature).

Finally, as interconnect dimensions shrink, other metals are being considered to replace copper due to its high line resistance at small interconnect CDs [128]. For a metal to be a good narrow CD interconnect candidate, it must (1) require only a thin or no barrier layer (to minimize the cross-sectional area of the typically more resistive barrier material), (2) possess favorable electron scattering properties at small dimensions [128], and (3) be compatible with conventional BEOL integration. It was mentioned previously that superfilling has been demonstrated for other metal systems; the one metal of this group whose use as an interconnect in a high-volume silicon technology has been disclosed in the literature is electroplated cobalt [34, 129]. These publications cite a lower via resistance as well as better electromigration performance as compared to copper (line resistance was not mentioned in these references). As future BEOL technologies are developed and new challenges emerge, it is possible that other plated metal systems could be researched and implemented as interconnects.

In summary: electroplating has been an essential process step in the fabrication of BEOL copper interconnects for over 20 years. The unique superfill capability of copper plating baths is made possible by organic additives that promote enhanced local deposition rates at the feature bottom, a phenomenon whose mechanism has been studied extensively. Incremental improvements in copper electroplating chemistries and waveforms (along with the barrier, liner, and seed layer processes on which plating depends) have reliably enabled the scaling of BEOL wiring dimensions from the submicron regime all the way down to just over 20 nm in width. As traditional technology node scaling becomes increasingly difficult, more exploratory metal fill processes (including metals besides copper) are being considered to meet the new challenges presented at these advanced nodes. With the potential for manufacturable, void-free fill of high aspect ratio features for a variety of metals, plating processes will likely continue to play a significant role in future BEOL interconnect fabrication.

6.3 Chemical Mechanical Planarization

As described earlier in this chapter, semiconductor devices are layered structures created through repetition of a small number of highly evolved process steps. Before the introduction of chemical mechanical planarization (CMP), the basic steps in semiconductor fabrication comprised of (1) deposition of a material layer, (2) deposition and lithographic patterning of masking layers to protect some areas of this material layer, and (3) a subsequent etching process to remove the unprotected first material, transferring this pattern into the structure below. This process would be repeated many times to create the semiconductor device and subsequent layers for contact to the device and on-chip interconnect wiring. However, each cycle of deposition and material removal would generate nonuniform topography in the wafer surface. This approach became a limiting factor for lithography since the topography exceeded the acceptable depth of focus (DOF) [130]. In 1983, a new process was invented which can accomplish material and topography removal to achieve a planar surface [131, 132]. This process of CMP was quickly adopted and allowed separation of duties in the process flow of semiconductor fabrication: RIE material removal for creation of patterned trenches and CMP to eliminate topography and remove unwanted overburden of deposited material. Initially applied to dielectric planarization steps such as the shallow trench isolation (STI) process [133], CMP has been an enabling technology for semiconductor manufacturing and is utilized for more than 14 interconnect levels in the 7 nm product [134].

6.3.1 CMP Tool Description

CMP Tool

CMP is a geometrically selective process for material removal; the highest points of topography are removed at a faster rate as compared to the low-lying areas. This planarizing effect is achieved by the combined action of an abrasive slurry and a moving polishing pad pressed against the wafer surface [135]. The CMP tool and process are depicted schematically in Fig. 6.25. The polishing pad is mounted face up on a rotating platen, and slurry is dispensed from above onto the pad surface. The wafer is held face down in a wafer carrier. During polishing, the wafer is rotated and pressed against the polishing pad. After completion of polishing, water is dispensed onto the platen to rinse slurry from the pad and wafer. The wafer is then removed from the platen and transported to cleaning and drying processes. To maintain consistent properties of the pad surface, a pad conditioner is pressed against the moving pad. The conditioner may be a

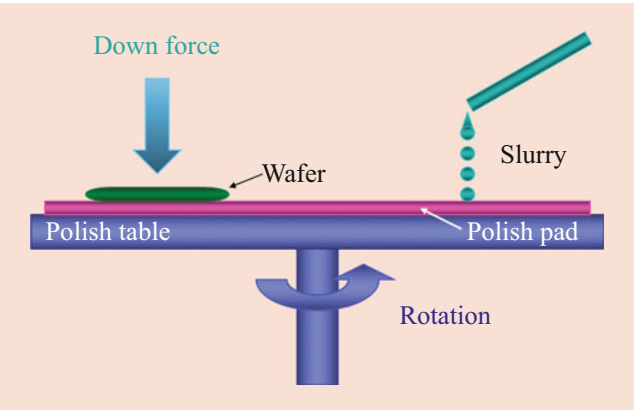


Fig. 6.25 Schematic diagram of the CMP tool and process

hard abrasive such as a diamond disc or a brush containing polymeric fibers. Conditioning may be applied during or before wafer polishing to prepare the pad surface.

CMP is fundamentally a local phenomenon; a successful CMP process requires the precise control of local chemical and mechanical conditions at the surface of the wafer. To achieve the required wafer-level uniformity, these local conditions must be reproduced across all areas of the wafer. Many mechanical approaches have been tried to achieve the required wafer-level uniformity in planarity [135]. Over time a common approach has evolved utilizing a rotating polishing platen and wafer carrier. Converging on a common approach has allowed the CMP industry to achieve a high level of tool and process optimization while reducing cost [136].

CMP Pad

The CMP pad covers the surface of the platen and is attached through an adhesive backing. The platen is typically more than twice the diameter of a wafer and has internal passages for flow of a liquid to control temperature. The pad is a consumable item; at the end of usable life, it is peeled off, and a new pad is installed. The hardness of the pad surface provides primary control of the planarizing effect of the CMP process. Pads of varying hardness or flexibility are available to suit the needs of different CMP processes. The use of a "hard" pad results in better planarity, but higher levels of defects while use of a "soft" pad result in better defectivity and higher topography. To achieve better planarity and better defectivity, a pad stack containing a softer sub-pad is often used underneath a hard pad. Modern pads with composite materials that incorporate the properties of conventional hard pads while providing better defectivity have become available in recent years.

The top portion of the pad often contains a pattern of grooves to aid in distribution of slurry as the pad passes under the wafer. The pad material is typically a urethane polymer and contains a distribution of pores. During polishing, these pores serve as local reservoirs for slurry to maintain the polish rate and uniformity of the CMP process. Key CMP parameters such as removal rates, planarity, and defectivity depend on the performance of the pads, and these parameters can vary over the lifetime of the pad. In addition, pad-to-pad (within batch) and batch-to-batch variations in pad performance have been observed in manufacturing. The pad manufacturing is a very complex process, and manufacturers have made tremendous progress in their methods for process control over the past decade. Still, pads are a major contributor of CMP process-related variabilities in semiconductor manufacturing.

(i) Pad Conditioner

A consistent pad surface must be maintained to achieve adequate and repeatable removal rate of material from the wafer [137]. An abrasive pad conditioner is used to remove spent slurry abrasives and restore the pad surface to a repeatable condition. This also removes polishing debris, exposes new pores, and creates asperities in the pad surface which are local high points [138]. The abrasive material used is typically diamond, but conditioning may be effected by using a brush for some softer pad materials. During CMP these asperities create local regions of high pressure and are necessary for maintaining adequate polish rate. Without conditioning, the CMP pad will typically "glaze over," and rate will drop significantly. As noted above, conditioning may be applied prior to polishing a wafer or in situ during polishing.

(ii) Wafer Carrier

The wafer carrier has evolved into a sophisticated component of the CMP process. In a basic sense, the carrier holds the wafer face down against the polishing pad. A retaining ring is employed around the circumference of the wafer to resist the sheer forces of the CMP process, preventing the wafer from sliding out of the carrier. The carrier also serves to provide local control of the downforce for annular regions or "pressure zones" of the wafer. The local force is typically applied through pressurized air to the backside of the wafer through an elastomeric membrane [136, 139]. The pressure can be varied for individual annular regions to control local polish rate. This downforce control is essential for achieving uniform material removal across the wafer. Modern wafer carriers currently comprise as many as eight pressure zones. Typically, the force of the retaining ring applied to the pad can also be controlled. This "active" retaining ring is useful for further control of wafer-level uniformity of removal rate, particularly near the edge of the wafer.

(iii) Wafer Cleaning

During polishing, the wafer is exposed to chemicals and abrasive particles from the CMP slurry. After polishing, the wafer must be cleaned and dried. The surface of the exposed materials on the wafer such as copper must also be protected from atmospheric corrosion or chemical attack and remain stable until the deposition of a capping layer to seal the copper surface. To accomplish this, water is typically dispensed onto the CMP pad after completion of polish to dilute and rinse away the slurry chemicals and abrasive particles. In place of water, this pad rinse may be accomplished with a solution formulated to promote cleaning and passivation of the wafer surface. The wafer is then transported through a series of one or more cleaning steps. The wafer may be immersed in a tank of cleaning solution with megasonic energy applied to facilitate removal of slurry particles from the surface. To achieve effective removal of slurry particles, it is necessary to employ a mechanical brushing action as well [140–142]. This brushing is accomplished using soft,

hydrophilic PVA (polyvinyl alcohol) brushes, usually in conjunction with a cleaning solution. The brushes are typically cylindrical in shape and pressed against the wafer surface while both brushes and wafer are rotated [143]. The wafer is processed through one or more stages of brush cleaning; each stage can be accomplished in separate modules of the CMP tool. An alternative approach for brush cleaning employs PVA material which is rotated and swept like a phonograph needle across the wafer surface in the presence of wafer or cleaning chemical.

(iv) Wafer Drying

The final step in CMP processing is drying of the wafer. Originally wafer drying was accomplished through spin drying whereby the wafer is rotated at high speed and water is flung off the surface by centrifugal force and the remaining traces are removed by evaporation. However, the defectivity requirements for modern semiconductor products cannot be met through spin drying alone. Evaporating water, even water of high purity, tends to leave "water mark" defects on the wafer surface. For this reason, wafers are now typically dried through the use of the Marangoni effect [144, 145]. In this method, the wet wafer is passed through a zone of saturated gaseous isopropyl alcohol (IPA). As the leading edge of the wafer is wetted by alcohol, a surface tension gradient is created. Through this Marangoni effect, water on the wafer surface is drawn away from the leading edge, and the remaining IPA evaporates readily, leaving a clean, dry wafer surface.

6.3.2 CMP Process Description

As the name implies, *both* mechanical and chemical forces are necessary to accomplish the CMP process. Chemicals present in the CMP slurry create a modified surface layer of the material, and the mechanical action of the CMP pad with slurry particles removes this modified layer. It is important to stress that CMP does not proceed by direct mechanical abrasion; only the material which has been chemically modified will be removed [146]. The mechanism described enables CMP to achieve a smooth, scratch-free surface. CMP processes can typically achieve surface finishes of less than 0.5-nm RMS roughness.

To understand the fundamentals of the CMP process, it is useful to begin with the Preston equation, which was developed in 1927 to describe the mechanism for lapping or polishing glass [147]:

$$r = kPv \tag{6.1}$$

where r is the material removal rate, P is the force applied normal to the surface, v is the differential speed, and k is the Preston coefficient. The differential speed pertains to the pad moving against the wafer surface. For many CMP processes, the Preston equation serves as a useful model; we find that removal rate varies linearly with the Pv term. As an example, we can consider a CMP process for removing SiO_2 whereby the slurry has a basic pH and the abrasive particles are silica (SiO_2). In this case, the SiO_2 surface of the wafer is partially hydrolyzed by hydroxyl ions in the slurry. This "softened" SiO_2 layer is then removed by action of the CMP pad and abrasive particles. This paves the way for further hydrolysis of the SiO_2 surface which is again removed by mechanical action. In practice these phenomena occur simultaneously during CMP to produce a steady state of material removal. This simple CMP model, comprising an abrasive and a chemical medium that "softens" the wafer surface, is applicable to many semiconductor applications where the goal is to reduce the thickness of a single material. Systems behaving this way will tend to reduce topography and planarize the surface of this material, since the local pressure and thus the Pv product will be larger on points of higher topography. The effectiveness of reducing topography can be expressed as planarization efficiency E_p, given by:

$$E_p = 1 - \frac{E_u}{E_d} \tag{6.2}$$

where E_d is the removal rate on a raised area of topography and E_u is the removal rate on an area of recessed topography.

Many CMP applications require the exposure of more than one material on the wafer to the CMP process. In these cases, it is necessary to control the relative removal rates of individual materials. For example, CMP is often used to remove an overburden of material which has been deposited to fill a trench formed in a layer of another material. In this case, a high removal rate is desired for the overburden material, while a low removal rate is desired for the underlying layer. This difference in removal rate is referred to as *selectivity* (S) and is given by the equation:

$$S = \frac{R_A}{R_B} \tag{6.3}$$

with R_A, R_B the removal rates for materials A and B, respectively. An example of this process is CMP for shallow trench isolation (STI) [148], where an SiO_2 overburden is removed with the goal of stopping on silicon nitride. In this type of application, the object is for the SiO_2 fill material in the trench to be coplanar with the surrounding SiN as shown in Fig. 6.26.

Polishing must proceed long enough to ensure complete removal of overburden over the entire wafer. To ensure this, all areas of the wafer will experience some "overpolish" or

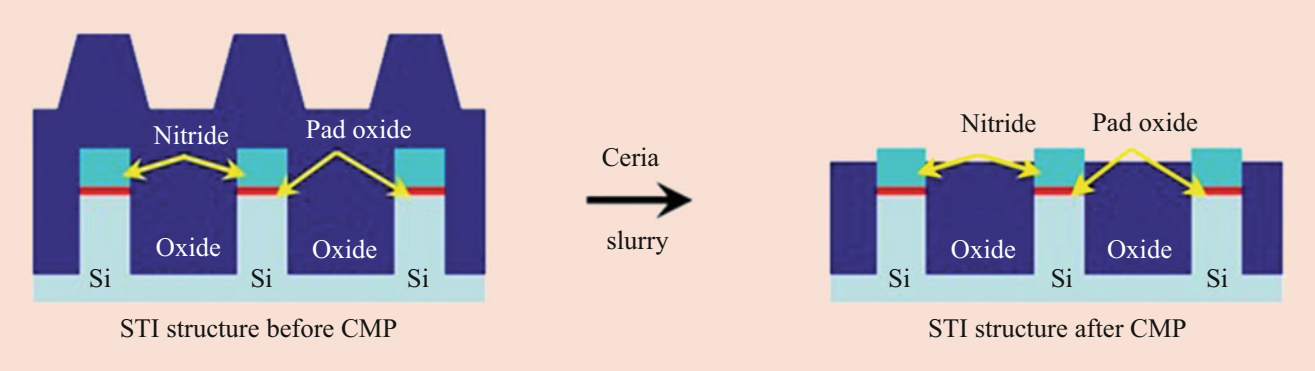


Fig. 6.26 Schematic diagram of the STI CMP process

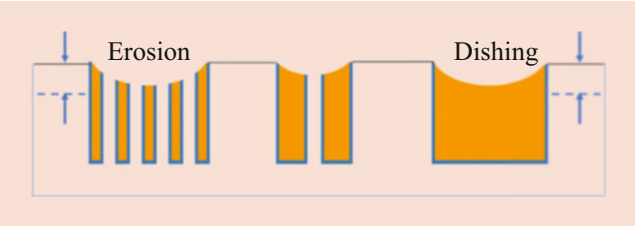


Fig. 6.27 Dishing and erosion from copper CMP

continued polishing after overburden has been removed in some areas. During overpolish, we do not want to create a recess in the filled trench structure. Here, the "Prestonian behavior" of CMP is useful for minimizing the topography of the final surface. Once a recess begins to develop in the trench region, the pad acts as a beam across this area, exerting a lower local pressure (the *Pv* product is locally reduced). If CMP continues, the recess will tend to reach a limiting value which is dependent on the stiffness of the polishing pad and the process selectivity for the materials present. The post-CMP recess in an individual trench is defined as "dishing" (Fig. 6.27). Wider trenches tend to dish more since the beam (polishing pad) will deflect more over this larger span. Planarization will also be affected by the number and placement of multiple trench features with respect to each other. If several trenches are arranged in near proximity, the relative area of low polish rate "stopping" material between the trenches is decreased. The stopping material between the trenches will experience higher mechanical Pv conditions, and local polish rate will increase. As a result, the entire region will polish faster and will become recessed. This recessing of patterned regions is referred to as erosion (Fig. 6.27).

Varied trench widths and pattern densities are necessary in circuit design but present challenges for the CMP process. To some extent, the circuit pattern can be modified to improve overall planarization. Ideally, we would maintain a uniform density of trench widths and density of pattern across all areas of the chip. In practice there are limitations to achieving this through circuit layout, so it has become common practice to further improve pattern factor by the addition of non-active "dummy" fill features [149]. For copper CMP processes for interconnects, it is typical to define an acceptable range of pattern densities and to use a dummy fill technique to achieve densities with that range. Similarly, trench features tend to dish more as width increases. If a circuit requires wide trench features, dishing can be reduced by the addition of small areas of stopping material within the trenches. As an example, large copper shapes may be necessary for electrical test probing or for lithographic alignment marks. Small dielectric "cheese" features can be added within these shapes to reduce copper dishing.

6.3.3 Copper CMP

The schematic diagram of the Cu BEOL fabrication process is shown in Fig. 6.28.

Copper interconnect "wires" are fabricated through a series of steps which are repeated to create each wiring level of a multilevel structure. In simple terms, (i) a trench pattern is formed in a stack of dielectric layers through lithography and RIE, (ii) TaN/Ta barrier, Cu seed layer, and Cu conductor metal layers are deposited over the patterned dielectric to fill these trenches, and (iii) the Cu overburden, TaN/Ta barrier, and a portion of the underlying patterned dielectric are removed through CMP. To meet the requirements of the semiconductor circuit, the resultant wires must be within a specified range of resistance per unit length. To achieve the target wire resistance, the unit processes used to form these wires must provide adequate control of the wire dimensions. Lithography and RIE are responsible for controlling the width and depth of the lines, while CMP is responsible for the height of the lines through control of material removal.

To achieve the required control of line height, copper CMP is typically accomplished in two steps: (i) a highly selective removal of copper overburden stopping on the barrier metal

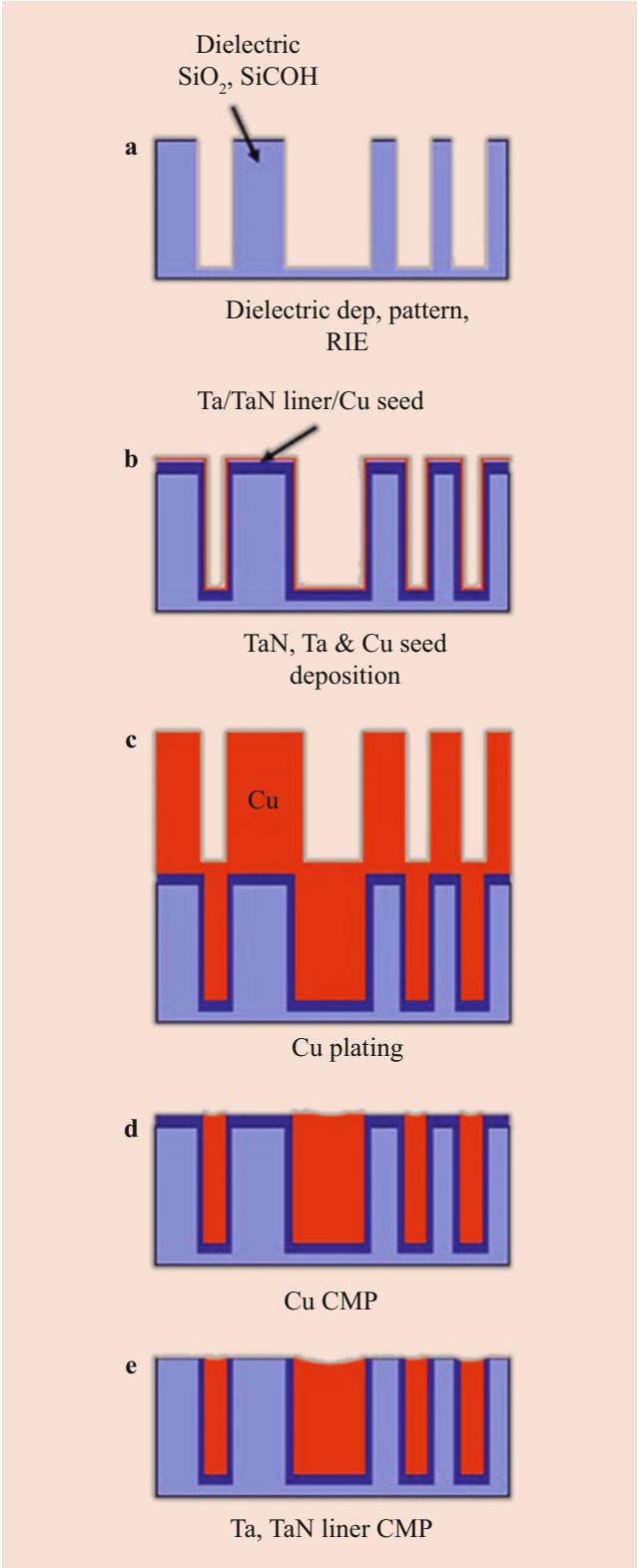


Fig. 6.28 Schematic diagram of the Cu BEOL CMP process (**a**) Dielectric deposition and patterning (**b**) Barrier and copper seed deposition (**c**) Copper plating (**d**) CMP of copper overburden (**e**) CMP of barrier metal

followed by (ii) a low selectivity removal of liner/barrier metal, dielectric, and trench copper to achieve target line height and a planar final surface.

Step 1: Copper CMP – Removal of Copper Overburden

The control of material removal rate across varying line widths and pattern densities is the primary challenge in achieving line height targets. For copper interconnect CMP, the chemical difference between the copper overburden and the underlying barrier and dielectric lends itself nicely to a two-CMP-step approach to achieving target line height. The first CMP step, bulk removal of Cu overburden, exploits this chemical difference to achieve a high selectivity to the barrier material. By stopping on barrier, the task of overburden removal is accomplished with little or no pattern-dependent erosion of the underlying structure. The resultant top surface of barrier becomes a consistent starting point for the subsequent nonselective barrier CMP step. In addition to stopping on barrier, the bulk Cu CMP process must also provide minimal or no dishing across the range of line widths present. The design of a copper slurry to meet these requirements requires understanding and control of surface chemistry during the polishing process.

The planarization mechanism for the bulk copper CMP process is depicted in the schematic diagram shown in Fig. 6.29.

The typical components of a bulk copper slurry are (i) oxidizer, (ii) inhibitor, (iii) abrasive, (iv) surfactants, and (v) polyelectrolytes and similar materials to prevent the adhesion of abrasive particles, pad debris, and other materials to the polished surface. Understanding of the role of each on the kinetics of the CMP process is critical for the development and optimization of the slurry composition.

Oxidizer The oxidizer provides chemical driving force for the dissolution of copper. The oxidizer removes electrons from copper metal forming Cu^{2+} ions which are soluble in the slurry.

$$Cu^0 \rightarrow Cu^{2+} + 2e^-$$

The oxidizer must provide the chemical potential to remove electrons from copper. In addition, it must be stable in the slurry and not react with other slurry components except as required during the CMP process. A common oxidizer for bulk copper is hydrogen peroxide.

Copper Inhibitor To achieve planarization, the reaction between Cu and oxidizer must not proceed without the action of the CMP pad and abrasive. In other words, removal of

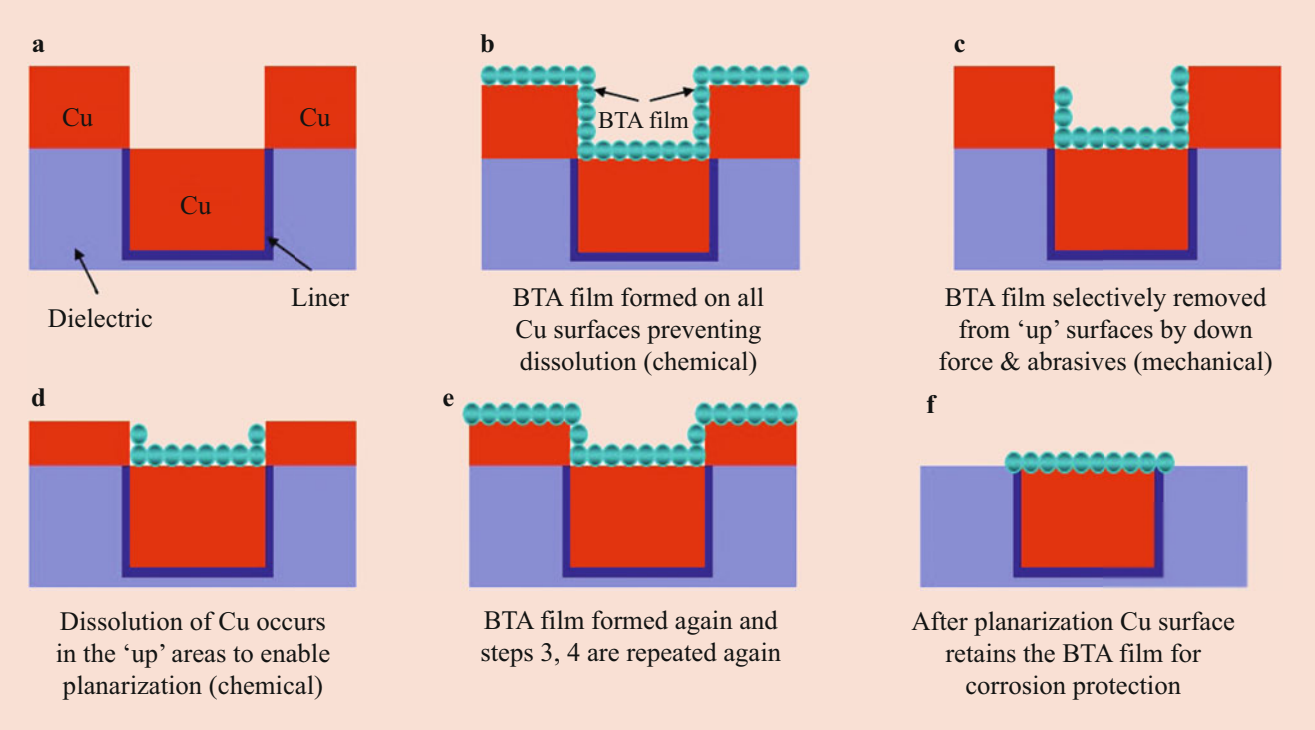


Fig. 6.29 Schematic diagram of the Cu planarization processa. (**a**) Wafer surface with plated copper overburden (**b**) Copper surface exposed to CMP slurry, with adsorbed BTA film (**c**) Copper surface with BTA film removed from "high" areas, due to mechanical action of pad and slurry (**d**) Dissolution of exposed copper in high areas (**e**) Reformation of BTA film due to exposure to slurry (**f**) Planarized structure after removal of copper overburden

copper under "static" conditions must be prevented. This is accomplished by using an inhibiting agent, a molecule which specifically adsorbs on copper to form a film which blocks the oxidizer from coming into contact and reacting with the copper surface. Multiple classes of molecules can adsorb strongly enough on copper to achieve this purpose; among these are sulfur compounds and heterocyclic compounds of nitrogen such as triazoles [150]. Benzotriazole (BTA) is a well-known copper inhibitor which has been employed effectively in copper slurries. BTA is strongly adsorbed onto the copper surface, particularly under acidic conditions [151], and readily forms a protecting film. Depending on the BTA concentration and chemical composition of the slurry, a thicker BTA film can be formed. The adsorbed BTA molecules can interact with each other to form a durable, compact film. Figure 6.30 illustrates the behavior of the BTA inhibitor in suppressing the dissolution of copper during CMP.

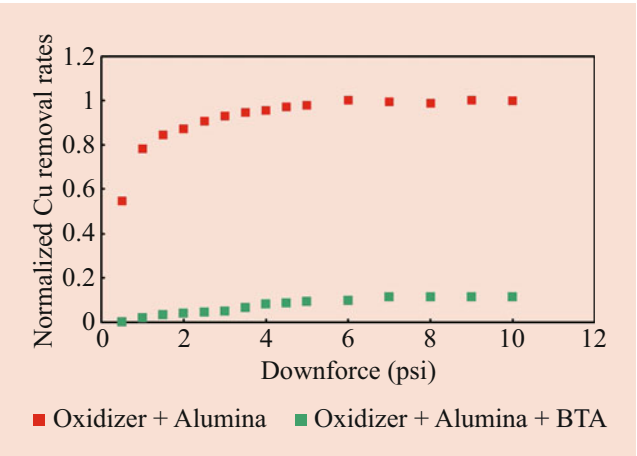


Fig. 6.30 Normalized Cu removal rates vs. applied pressure (down force) in the absence and presence of BTA

Abrasive The abrasive is comprised of highly engineered particles, typically oxides of silicon or aluminum. Particle size can be as small as 25 nm but can range up several hundred nm. Best polishing performance is achieved through well-controlled distribution of particle size and shape. The industry trend is toward solution-grown, (colloidally grown) abrasive particles for leading edge semiconductor technology nodes with stringent planarization and defect requirements.

During polish, mechanical force is transferred through the pad, and the slurry particles are pressed and moving against the wafer surface. If a particle impacts the surface with sufficient force, it can disrupt the inhibitor film and allow local dissolution of copper. After dissolution, the freshly exposed

copper surface is chemically active, and the inhibitor can readily reform the surface film. Due to the mechanical action of the pad, areas of raised topography on the wafer experience a higher local pressure and a larger number of *Pv* film-disrupting impacts as compared to areas which are not raised. These effects promote high planarization efficiency since raised areas will experience a significantly higher removal rate for copper.

Additives for inhibitor film modification Copper slurries offered by industry vendors have evolved dramatically as interconnects have scaled from 180 nm to 7 nm and beyond. This evolution has been necessary to meet increasing planarization and defectivity demands for each new node. Controlling the properties of the adsorbed inhibitor film is essential to meeting these requirements. Some of the factors which must be considered in manipulation of this film are:

- Chemical nature of inhibitor: Choice of adsorbing molecule determines strength of adsorbate to copper surface interaction.
- Concentration of inhibitor: Affects fraction of copper surface covered by inhibitor molecule.
- Manipulation of inhibitor film properties: Addition of other species which compete for adsorption onto copper surface allows tuning of chemical and mechanical properties of the film.

Surfactant molecules can compete with the BTA film and modify the overall film properties. Typical anionic surfactants such as sodium alkyl sulfates form a surface film by physical adsorption as opposed to the strongly adsorbed compact BTA film. Thus, the surfactant film can influence the Cu removal rate by competitive adsorption and BTA film modification as illustrated in Fig. 6.31. The result is an increase in removal rate for a system with surfactant as compared to a system with BTA alone.

A more detailed explanation of this behavior can be found through adsorption theory. Surfactant molecules adsorb onto the Cu surface by physical adsorption. This type of physical surface adsorption can be described by the Langmuir isotherm, as shown below:

$$\beta C = \frac{\Theta}{1-\Theta} \tag{6.4}$$

The coverage of the copper surface by surfactant can be expressed as βC, where β represents the free energy of adsorption of the molecule, C is the concentration of the surfactant, and Θ is the fraction of area covered. The Langmuir adsorption isotherm describes the physical adsorption with no mutual interactions between adsorbed molecules.

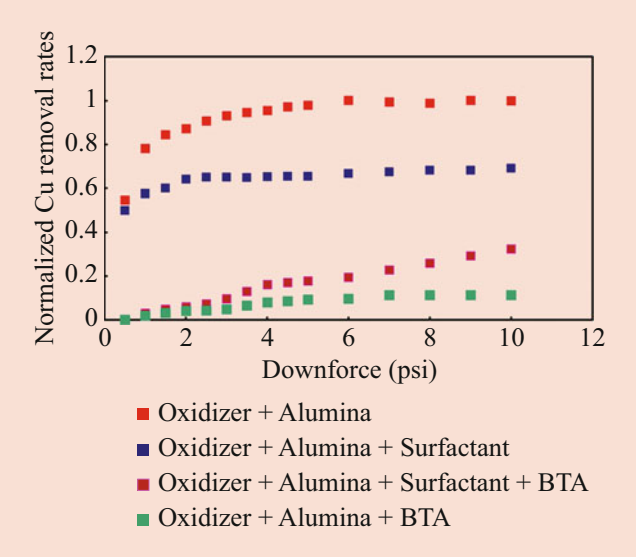


Fig. 6.31 Normalized Cu removal rates vs. applied pressure (down force) in the presence and absence of BTA and the surfactant

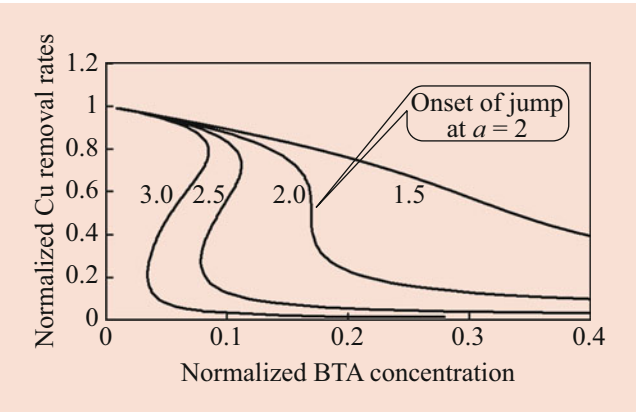


Fig. 6.32 Normalized Cu removal rates vs. normalized BTA concentrations, showing inflection at $a > 2$

The Frumkin isotherm also describes the surface coverage βC of an adsorbate, with parameter a introduced to account for adsorbate-to-adsorbate interaction as shown below:

$$\beta C = \frac{\Theta}{1-\Theta} \exp\left(-2a\Theta\right) \tag{6.5}$$

Values of a greater than 2 indicate a strong, compact surface film. BTA molecules are known to interact or bond to one another once they are adsorbed on the copper surface. Figure 6.32 describes the normalized copper removal rate predicted as a function of BTA concentration. Per the Langmuir isotherm, for values of a greater than 2, there is a discontinuity in film coverage with BTA concentration, resulting in a dramatic decrease in removal rate vs. BTA concentration.

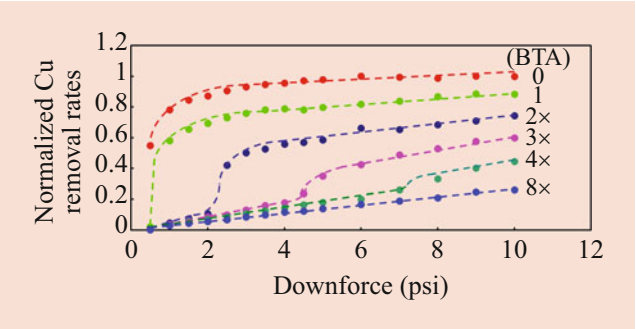


Fig. 6.33 Normalized Cu removal rates vs. applied pressure (down force) at various BTA concentrations

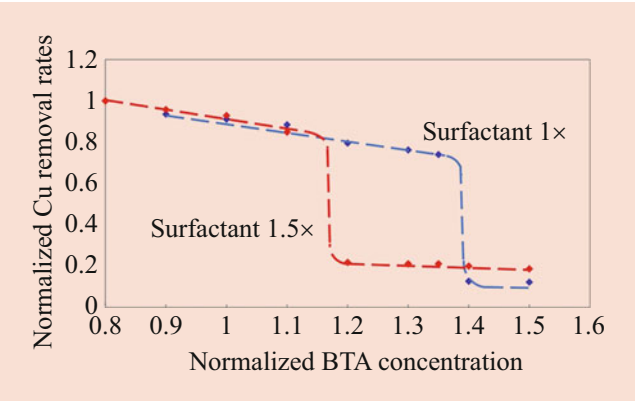


Fig. 6.34 Normalized Cu removal rates vs. normalized BTA concentrations at various surfactant concentrations

The applied downforce is also a factor in the stability of the BTA film during polishing. Consistent with this model, a jump CMP polish rate is observed as a function of downforce (Fig. 6.33). The understanding and control of these relationships are useful in optimizing slurry formulations and tuning copper CMP processes for specific applications. High and low areas experience different local downforce (Fig. 6.29). Enhanced planarization efficiency and reduced copper dishing can be achieved by establishing film conditions that magnify the removal rate differences between the high and low areas of topography.

The inhibiting film behavior and the resulting downforce transition can further be tuned through the introduction of a second adsorbing species. For an inhibiting system based on BTA, if a second species is introduced which adsorbs onto copper, it will take the place of some BTA molecules and interrupt some of the BTA-to-BTA bonding. The result is a less compact film; in this way tuning of the system can be accomplished through adjusting the concentrations of both adsorbing species (Fig. 6.34).

To meet the requirements of semiconductor fabrication, the amount of copper removed in the CMP process must be carefully controlled at all locations on the wafer. To achieve this, film thickness measurement during CMP is important. For measurement of copper, induced current sensors can be embedded in the platen under the polishing pad [156]. As a sensor passes under the wafer, a current is induced which is used to determine metal film thickness as a function of wafer radius. This thickness information can be used to control the pressure zones in the wafer carrier to maintain uniform metal removal across the wafer. This measurement can also be used for determining the approximate endpoint of the metal polishing step. The signal strength for induced current diminishes with metal thickness; therefore the exact point of metal clearing is difficult to detect. The *presence* of a metal film at various radii on the wafer can be detected by reflection of a signal from a laser embedded in the platen. While this reflectivity measurement cannot measure the thickness of metal, it can be used in conjunction with the induced current technique to more accurately detect the point of metal clearing. In the bulk copper CMP step, it is important that virtually all copper to be removed above the barrier film since the copper polish rate of the subsequent barrier CMP step is relatively low and the barrier CMP process is not tuned to remove remaining bulk copper. Using the endpointing techniques described above, it is possible to detect the point of bulk copper overburden removal. However, copper overburden does not clear simultaneously in all areas within a die; varying pattern density and the presence of topography from previously built layers will cause some local regions to clear later than others. Also, even with optimization of wafer-level removal uniformity, some regions of the wafer may clear later than other regions. For these reasons, the bulk copper CMP process is typically not stopped immediately at the detection of endpoint. A period of continued copper polish or "overpolish" is used to ensure that copper is removed from all areas of the wafer and all areas with the die. The polish conditions may be adjusted during the overpolish period. For example, downforce may be reduced to control dishing and erosion. The duration of the overpolish step can be for a few seconds or longer than 1 min, depending on the interconnect structure and level being polished. In setting up a new copper CMP process, it is useful to inspect the wafer surface after the bulk CMP process step through optical and SEM methods to determine optimum overpolish time and ensure complete removal of copper.

Step 2: Barrier CMP – Removal of Barrier and Setting Copper Line Height

To reiterate, the *overall* copper CMP process must achieve electrically separated copper conductors with a consistent line heights, independent of pattern density and with a minimum of defects. The first step, bulk copper removal, was described above and relies on high selectivity and high planarization efficiency to achieve removal of copper overbur-

den with minimal loss of barrier metal. Typically, a relatively hard pad is used to maximize planarization and to minimize removal differences due to pattern density. Some introduction of defects (from hard pad) can be tolerated at the bulk copper CMP step in the interest of planarization, since the barrier layer and some dielectric will be removed in Step 2 and minor defects may be removed.

The second step, barrier CMP, must meet numerous, interrelated, and often conflicting requirements:

1. Nonselective removal of barrier metal, remaining hardmask (if present), and a specified amount of dielectric.
2. Achievement of final CMP topography within specified limits to enable subsequent lithography and further downstream processing. This includes correction of topography generated in Step 1 due to copper dishing.
3. Setting of copper line height across all pattern densities to meet circuit design requirements.
4. Achievement of low defectivity for outgoing wafer surface including removal of defects if present from Step 1 overburden removal.

Barrier slurry formulation In concept, a slurry for barrier CMP needs to be nonselective or have equal polish rates for barrier, copper, dielectric, and hardmask if present. In practice, this is a complex challenge, since the chemical reactivity of copper (a metal) is different from the barrier (a semi-metallic material) and the dielectric (a ceramic). For copper removal, an oxidizer/inhibitor system can be employed, similar to that used for the bulk copper slurry. The oxidizer is typically hydrogen peroxide, and a film formed by a copper inhibitor provides self-limiting behavior that aids in controlling topography generated in areas where copper is removed. For dielectric removal, silica abrasive is typically used. Silica generally follows the polishing mechanism described for oxide CMP earlier in this chapter; the silica particle interacts with the partially hydrolyzed dielectric surface. This "softened" dielectric is removed in the interaction, and then further hydrolysis can occur at that site. The polish rate for a low k dielectric is typically lower than for silicon dioxide. This is thought to be due to the presence of carbon which renders the material more hydrophobic and less prone to hydrolysis.

A polishing system built solely upon these mechanisms for copper and dielectric cannot be readily optimized for the variety of pattern densities normally found in interconnect circuits. For dense regions of copper lines, the copper mechanism dominates; the small areas of dielectric between these lines receive relatively more mechanical force and polish quickly. Polishing in these regions will ultimately be controlled by the copper inhibitor film mechanism. However, for areas sparsely populated with copper lines, polishing of the dielectric will dominate, and simple "Prestonian" polish behavior is obeyed. The polish rate will vary according to the amount of dielectric area present (Fig. 6.35). The difference in these mechanisms creates differences in overall removal rate (and resulting copper line height) for different pattern densities.

To manage this, a self-balancing system is needed which can accommodate both copper-rich and dielectric-rich areas of the pattern. To achieve control of polish rate in dielectric-rich regions, an inhibitor molecule can be employed which adsorbs on dielectric. Similar to the action of BTA on copper, this inhibitor allows removal on raised areas of dielectric and decreases removal rate in recessed areas. One such group of molecules are polyelectrolytes which have been shown to enhance planarization in barrier slurries.

Tantalum nitride is the typical barrier used for most copper interconnect products. The barrier film thickness is typically less than 10% of trench width; therefore, tuning of the barrier material polish rate is not as critical as tuning of copper and dielectric polish rate. Once the horizontal barrier film is removed from the dielectric surface, planarization is domi-

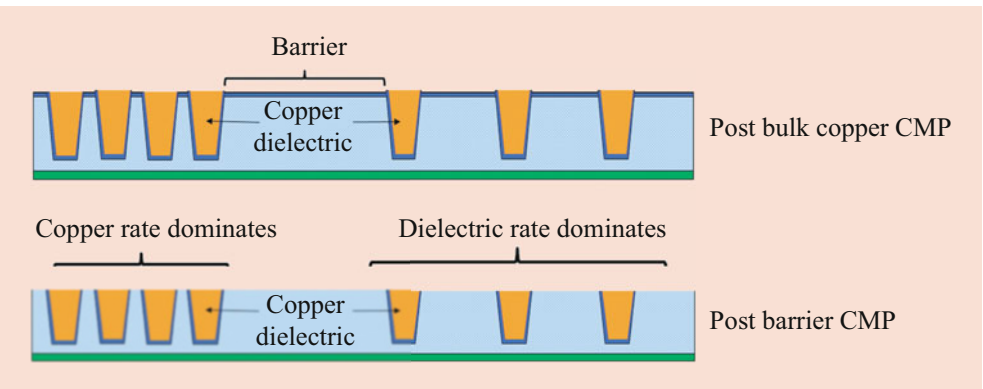


Fig. 6.35 Polish rate behavior of barrier CMP process for dense and sparse patterned areas

nated by the materials present in larger areal fractions: copper and dielectric. TaN can be polished by silica abrasive alone but will typically have a removal rate of less than one half that of dielectric. The presence of oxidizer can enhance TaN removal rate to be approximately equal to dielectric rate. The mechanism here is thought to be surface oxidation of TaN to Ta oxide. The thin surface oxide layer is then removed in a mechanism analogous to the polishing of SiO_2. In support of this mechanism, a peak in TaN removal rate is observed with increasing oxidizer. For oxidized concentrations beyond this peak, TaN becomes passivated; the growth rate of oxide exceeds the ability of the abrasive to remove it, and polish rate decreases.

Process Control for Barrier Polish

Control of the barrier CMP process is critical in meeting the copper line height specifications. These translate directly to resistance distribution for the interconnect circuits. As described above, control of topography and pattern density variations can be accomplished through a properly formulated barrier slurry. Unlike the bulk copper polish step, barrier CMP is a blind polish; there is no "stop layer" to provide a built-in means of controlling the total amount of material removed. Additionally, the induced current and laser methods used for control of bulk copper polish are not readily applied to the barrier CMP process. For these reasons, barrier CMP may be controlled by time (duration of polish). It then follows that consistency of removal rate and control of within wafer removal uniformity are critical. Wafer and platen rotation speed and wafer carrier zone pressures must be carefully optimized for within wafer uniformity. To provide better control over total material removal, optical critical dimension (OCD) measurement capability is often incorporated in the CMP tool to measure copper line height. This measurement is performed after CMP once the wafer is clean and dry but before the wafer is returned to the cassette. This capability can be used for automated process control (APC) in a production environment. The line thickness result from onboard OCD can be used to adjust the polish time for subsequent wafers. With wafers loaded throughout the tool, a few wafers may be polished before the result can be used for polish time adjustment. After that, OCD feedback from selected wafers can be used to continually adjust polish time for subsequent lots. A measurement of copper line height in situ during barrier polish would be very valuable for controlling removal uniformity through carrier zone pressures and for endpointing. CMP tool vendors are working on development of in situ measurement techniques including optical and induced current sensors for measurement of metal thickness. Further progress toward effective in situ measurement for barrier polish is expected.

6.3.4 Control of CMP Defects

The chemical and mechanical forces present in the CMP process provide the potential for generating defects in the interconnect structure. These defects can degrade chip yield, performance, and reliability. This section describes the typical defects observed from CMP and approaches to mitigate these. Figure 6.36 illustrates some examples of defects which can be caused by copper CMP.

Scratches

Scratches are created when foreign particles, other than normal slurry particles, are present between the pad and wafer surface. In general, a harder pad will generate more and deeper scratches than a softer pad. As a trade-off, a softer pad will be less efficient at planarization and will have a shorter useful life. Due to the relative softness of copper and low k dielectric materials, a very soft pad is typically used for barrier polish; pad life for these is much lower than for the harder pads used in bulk copper polish. To control scratching, it is important to maintain clean conditions at the wafer-to-pad interface and to prevent the introduction of unwanted solid material. Care must be taken when handling and installing polishing pads and whenever work is being done in or near the polishing module. Slurry blending and delivery systems must be designed to prevent agglomeration of abrasive particles. These systems should contain filters which are properly sized to catch unwanted particles and should be replaced at proper intervals. Scratches can also occur from particles or material generated within the CMP process. If delamination occurs, where pieces of solid material break loose from the wafer itself, scratches will typically result. Particular attention must be paid to the die patterns at the extreme edge of the wafer and the wafer bevel. The upstream processes which form the underlying patterned layers do not all terminate at the same location at the wafer edge. Locally, there can be missing or poorly adhered areas which can break free and cause scratches. Similarly, the unpatterned bevel area at the wafer edge can be a source of residues from previous processing that can break free and cause scratches in CMP. Typically, wafer bevel cleaning is used in a manufacturing fab to remove these residues periodically in the flow of processing.

Delamination Delamination is caused by an interface failure in the wafer structure during CMP. A portion of material can break away and, as mentioned above, will often cause scratches. While this occurs during the CMP process, the root cause of delamination is a weak interface in the underlying structure. The tensile strength of materials and interface adhesion in an interconnect structure

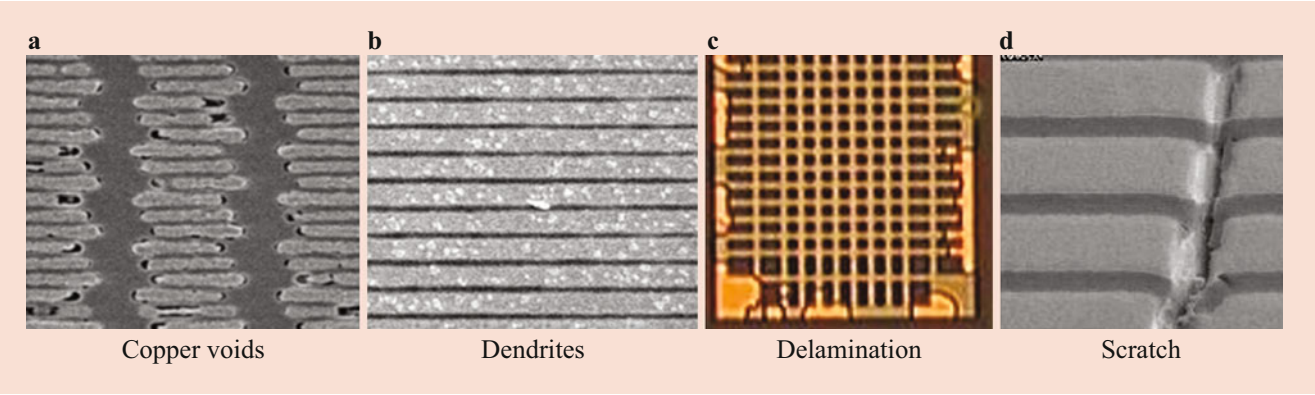


Fig. 6.36 Typical defects which can be caused by the copper CMP process. (**a**) Copper voids (**b**) Dendrites (**c**) Delamination (**e**) Scratches

should far exceed the mechanical forces generated in CMP. When delamination is observed, the integrity of underlying materials and interfaces must be improved.

Metal voids Bulk copper and barrier slurries are available from numerous commercial sources. These are highly developed to achieve copper removal and planarization without "attack" or uncontrolled local dissolution of the metal. If post-CMP metal voids are observed using a proven, qualified CMP process, the root cause may lie in the upstream metallization processes. It is essential that the post-RIE trench profile, barrier/seed deposition, and plating processes are co-optimized to provide robust, void-free metal fill with strong metal to dielectric interfaces. If metallization is marginal, voids may be observed post-CMP, even though they are not detectable post-copper plating.

Dendrites After CMP, the copper surface may react with ambient oxygen. The resulting copper oxide product can grow unevenly, taking the shape of small bumps on the copper lines or growths with various other shapes. If not suppressed, these "dendrites" can grow to bridge across one or more copper lines and cause circuit shorting [152–154]. The continued industry trend of scaling interconnects, including reduced interconnect pitch and lower k dielectrics, has exacerbated the tendency to grow dendrites. Following CMP, a dielectric capping film is deposited on the copper surface which serves as a hermetic seal to prevent further oxidation of copper. In practice, there will be some delay period between copper CMP and deposition of this cap. In a production environment, the wafers must be able to wait for a few hours before capping without significant dendrite growth. It has been shown that exclusion of moisture and oxygen by storage of wafers in dry nitrogen can significantly delay the growth of dendrites until capping is performed [153]. In addition, an important factor in dendrite suppression is passivation of the copper surface in the post-CMP cleaning process. An inhibiting film is present on the wafer surface after the barrier CMP step. This film serves to protect copper from oxidation during post-CMP rinse and wafer transport to the brush clean module. In the brush clean process, this inhibiting film is removed and replaced with a uniform passivating layer, typically copper oxide with other adsorbed inhibiting species. These commercially available brush clean chemistries are typically very alkaline; they are carefully formulated to achieve effective passivation of the copper surface. The selection of this cleaning solution and optimization of the overall brush clean process are therefore essential to achieving a usable post-CMP queue time to capping.

6.3.5 Copper CMP for Alternative Barrier/Seed Systems

Filling of trenches with copper has been a challenge with pitch scaling. To assist in copper fill, additional "seed assist" materials such as cobalt or ruthenium may be employed between the barrier and copper seed [155]. The implementation of a new material in the interconnect structure requires careful selection of barrier slurry and optimization of CMP process conditions [156]. CMP processes are dependent on the redox reactions which enable the dissolution of copper and barrier metals. The electrochemical potential driving these reactions is a function of the metals present; the introduction of an additional metal layer will shift this potential and change the behavior of the CMP process.

Ru Liner CMP

Considering the electromotive series, ruthenium is more noble than copper. During CMP the potential of copper is shifted toward the anodic direction in the presence of Ru.

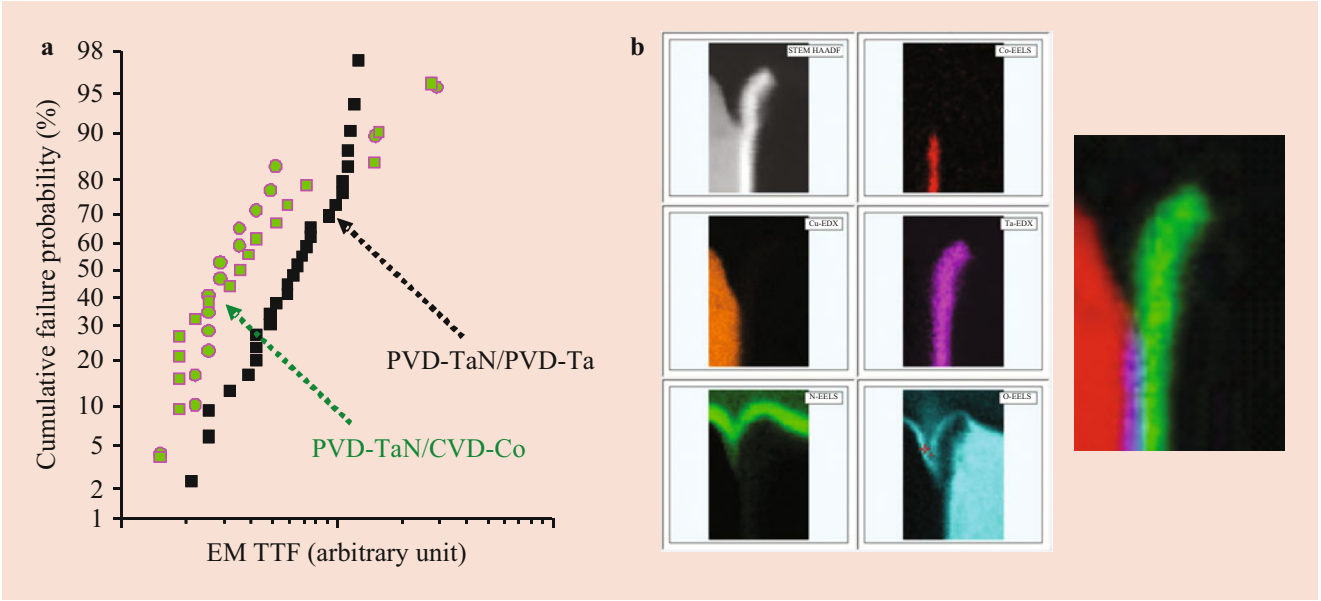


Fig. 6.37 EM lifetime degradation with TaN/Co liner (**a**) and STEM/EDX map showing Co divot defect formation (**b**)

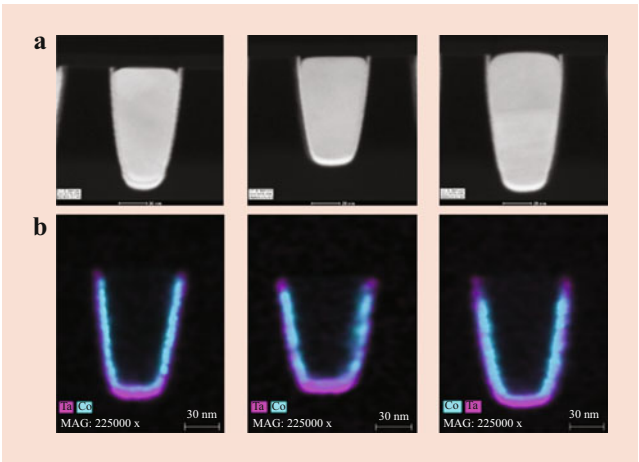


Fig. 6.38 STEM images (**a**) and EDX/EELS maps (**b**) with different wet process chemistries. No difference in imaged divot size is seen among different samples (**a**), while large differences in the depth of the Co recess (slit) are still detected by EDX/EELS mapping (**b**)

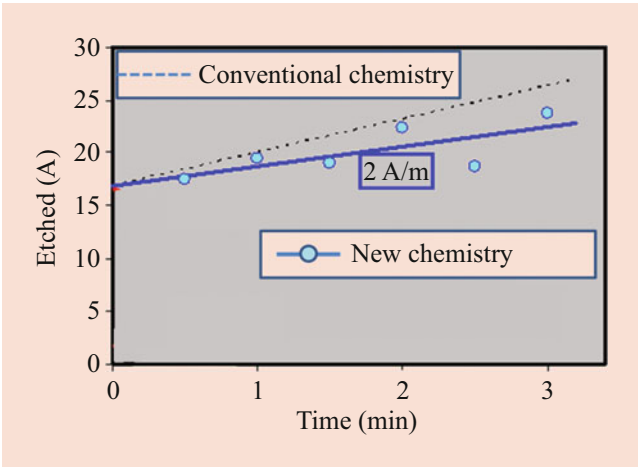


Fig. 6.39 Co etching rate reduction through modification of post-CMP clean chemistry

Using a copper CMP process designed for a conventional TaN barrier system, there is typically a higher rate of dissolution for copper when Ru is present. Subsequently, the top surface of the copper lines becomes recessed with a concave shape. This is in contrast with the flat or slightly convex copper shape usually observed for TaN liner alone. Also, polish rates for ruthenium are typically very low. This difficulty in removing the Ru film translates to a strong dependence on the fraction of Ru area present, i.e., on pattern density. The result can be a significant difference in post-CMP line height between different circuits within the same die.

Co Liner CMP

Unlike ruthenium, cobalt is *less* noble than copper. Once again, the barrier slurry and overall CMP process need to be specifically optimized for cobalt. If a TaN barrier CMP process is applied to a structure containing a cobalt wetting layer, cobalt can dissolve preferentially to copper. In this case, the top surface of copper lines may tend toward a more convex shape as the cobalt is lost at the interface to dielectric. In some cases, this cobalt loss can create deep divots or sidewall voids at the interface to dielectric [157].

Figure 6.37a shows an EM comparison between Cu lines with TaN/Ta liner vs. TaN/CVD-Co liner. For the Co liner structure, post-CMP trench top corners have divot defects, as shown in the STEM/EDX images in Fig. 6.37b [158]. Such

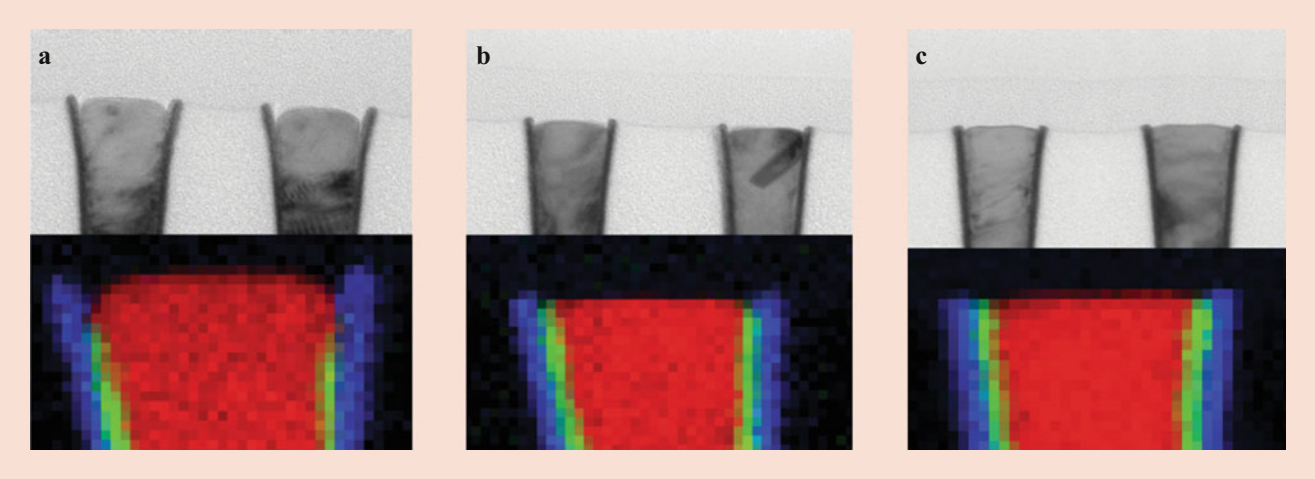


Fig. 6.40 Cross sections and EELS mapping of copper interconnects with Co seed assist layer. Red = copper signal, Blue = Ta signal, Green = cobalt signal. (**a**) Post CMP cleaning with chemistry developed for "normal" TaN/Ta barrier without Co layer. Divot is present at top corner of line due to loss of cobalt. (**b**) Same CMP process with addition of special inhibitor rinse on CMP pad after barrier CMP, divot is reduced. (**c**) Same CMP process as in a., but brush clean chemistry optimized for cobalt seed assist layer

divots can be the source of EM void nucleation sites; the recessed Cu surface where the cap dielectric cannot cover causes reduced EM lifetimes as shown in Fig. 6.37a.

Careful optimization of all CMP processing steps is necessary to effectively minimize these divot voids. Studies showed that even when no difference in imaged divot size is seen among different samples (Fig. 6.38a), large differences in the depth of the Co recess (slit) are still detected by EDX/EELS mapping (Fig. 6.38b) [158]. It was reported [159] that alkaline barrier slurries and reduced hydrogen peroxide concentration may help to suppress divot formation.

The post-CMP clean process must also be optimized to prevent unwanted dissolution of cobalt. Figure 6.39 illustrates the relative cobalt etching rates between a standard post-CMP clean chemistry and a chemistry modified with an inhibitor specifically for cobalt. This new chemistry was shown to reduce the formation of Co divots from the CMP process [158].

Figure 6.40 shows the EDX/EELS maps of the wire top corners for chips A, B, and C which are TaN/Co/Cu wires processed with different post-CMP clean chemistries. Figure 6.41 illustrates the EM performance for these structures. A clear correspondence between the EM performance and the divot suppression is evident, illustrating the need for specific optimization of post-CMP cleaning for cobalt liners.

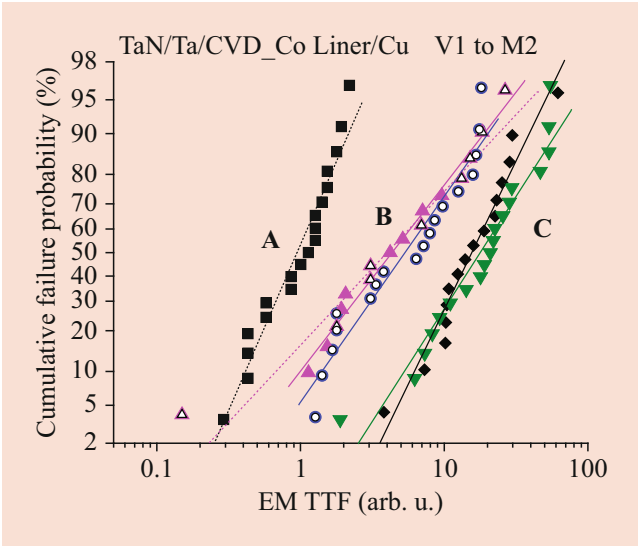


Fig. 6.41 EM lifetime dependence on divot formation. Each structure was processed with a different post-CMP clean chemistry as in Fig. 6.40

6.3.6 Summary

Since the dawn of copper interconnects, CMP has been fundamental to the fabrication process flow. Minimum conductor line widths which were initially 0.18 μm have been reduced to 18 nm and below! The CMP process will continue to be scalable through the understanding and control of the mechanical and chemical parameters described in this chapter. Slurry and post-CMP clean chemical formulations must be carefully tuned to the materials present to achieve the required control over conductor line height with low defectivity. The evolution of CMP process tools continues to improve control over mechanical parameters, while improvements in CMP endpointing techniques and automated process control will help to advance interconnect manufacturing.

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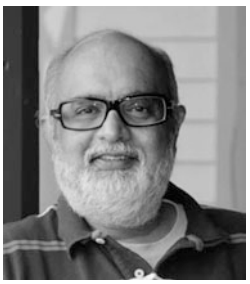

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From FinFET to Nanosheets and Beyond

7

Nadine Collaert

Contents

7.1 Introduction . . . 259
7.2 From Pure Dimensional Scaling to Design-Technology Co-optimization . . . 261
7.3 Gate-All-Around Devices: The Evolutionary Path from FinFET . . . 263
7.4 High-Mobility Materials . . . 267
7.5 Going 3D: CFET and Sequential 3D Integration . . . 271
7.5.1 Complementary FET or CFET . . . 271
7.5.2 Sequential 3D Integration . . . 272
7.6 Conclusions . . . 276
References . . . 276

Abstract

Moore's law has for more than five decades been the roadmap guiding the semiconductor industry. While originally driven by lithography advancements and material innovation, since the 22 nm/14 nm node, new device architectures like FinFET have been introduced to tackle the increasing challenges related to power efficiency, performance, area scaling, and cost. With the introduction of FinFET, design-technology co-optimization also gained a lot of importance. More than ever, the industry is looking for that magic device concept to continue CMOS scaling beyond the 3 nm technology node. Gate-all-around devices, coming in different flavors (nanowires or nanosheets), have been proposed as possible candidates for keeping leakage under control. These architectures can be seen as an evolutionary step from FinFET. More disruptive is the introduction of high-mobility channel materials like (Si)Ge. While many hurdles have been overcome, especially the lower bandgap and thus higher leakage are still a concern. Next, going 3D seems a straightforward way to continue area scaling. Based on the gate-all-around integration scheme, complementary FET (CFET) where nMOS and pMOS are stacked on top of each other shows potential for not only area scaling but also power-performance improvements, but it comes at the cost of a more complex integration scheme. Finally, as the industry will move more toward heterogeneous integration, sequential 3D, allowing for fine-grained connections between the different layers of active devices, will be key in enabling these more complex systems.

Keywords

CMOS · Scaling · FinFET · Nanosheets · CFET

7.1 Introduction

In his famous paper "Cramming more components onto integrated circuits" [1], Gordon Moore laid out the guidelines of today's nano-electronics industry. Based on only a few data points, he predicted that the number of transistors would double every year with innovations in lithography as the main driving force to enable transistor scaling. This was later adjusted to every 18 months and even 2 years. For more than five decades, the semiconductor industry has been very successful in following this Moore's law, using the scaling guidelines, set out by R. Dennard et al. in 1974 [2] as, with every new technology node, the following advantages can be expected: 50% area reduction, 30% cost reduction, 20% power reduction, and 25% performance increase (at reduced V_{DD}). This metric, known as PPAC (power-performance-area-cost), has become very important in recent years to assess the viability of new technology nodes. As Moore's law

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is a law of economics in nature, transistor scaling can only be maintained if the benefits outweigh the manufacturing efforts and costs that come along with the increased complexity of scaling.

Scaling was "business as usual" until the 90 nm technology node. Three scaling scenarios can be distinguished: constant voltage scaling, constant field scaling, and general scaling. Constant voltage scaling was done mostly in the 1980s and the early days of scaling. It was a pure geometrical process where the increasing electric field in the devices was disregarded. This resulted in excessive power dissipation and reliability issues. Constant field scaling, where all dimensions and voltages were scaled with the same factor, was rediscovered in the 1990s and used to mitigate the increasing problems with power density and hot carrier degradation. But it had some drawbacks: the performance improvement was reduced as compared to the constant voltage scaling scenario, and with scaling of the supply voltage V_{DD}, the threshold voltage V_T needed to be scaled accordingly which started to become an issue. Finally, general scaling where the dimensions of the basic building block, the MOSFET, are scaled down with a factor α ($\alpha = 1/\sqrt{2} \sim 0.7$) and the voltages with a different factor k is probably the most relevant for today's CMOS technology. Ion implantation, silicidation, chemical mechanical polishing (CMP), and the use of Cu in the back-end (BEOL) were successfully introduced along the way to improve the performance of the devices and to keep the leakage under control.

Scaling limits can basically be divided into three categories: wiring, lithography and more general patterning, and the limitations set by the device physics itself. The 90 nm technology node was a first breaking point. Boosting the device performance and keeping the unwanted short channel effects (SCE) under control was mostly done by scaling the gate oxide thickness t_{ox} of the transistor. By then, the nitrided gate oxide SiON had reached a physical thickness of only 1.2–1.3 nm. The gate leakage density, however, had increased to 100 A/cm^2 [3] as the quantum mechanical tunneling limit was reached and further scaling of the gate dielectric seemed impossible. Other ways needed to be found to improve the device performance. Strain engineering was introduced to boost the performance as t_{ox} was no longer scaled down. Channel strain engineering by either source/drain (S/D) boosters like SiGe for pMOS or strained contact etch stop layers (CESL) for nMOS were very effective in increasing the mobility and thus the on-current of the device I_{ON} [4, 5]. Figure 7.1 also shows that around the 90 nm node, scaling of the gate length started to slow down, allowing the reduction of SCE without impacting the density scaling, as for the latter, the reduction of the gate length L_G is not the key metric, but rather the scaling of the metal pitch and the contacted poly or gate pitch (CPP or CGP; this is the gate-to-gate pitch where the contact is placed in between as shown in the top-view schematic of Fig. 7.2). Scaling of both parameters by a factor 0.7 provide the required 50% area reduction with every technology node. Nowadays, gate length scaling is merely a consequence of CPP scaling as depicted in Fig. 7.3. At 90 nm, the CPP was roughly 300 nm, allowing for some room to relax the gate length from that node on since gate oxide scaling stopped.

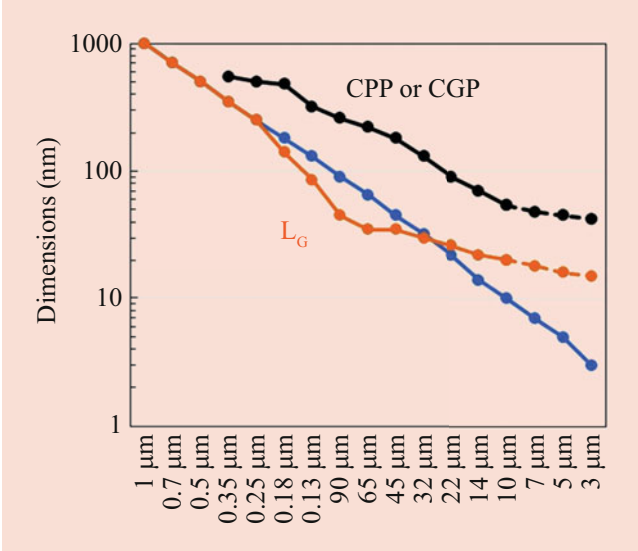

Fig. 7.1 Gate length and contacted poly pitch or gate pitch (CPP or CGP) as function of technology node; the blue line indicates the technology node while the orange line the gate length and the black line the CPP or CGP

Finally, at the 45 nm technology node, metal gate and high-k dielectrics were introduced replacing the traditional poly/SiON gate stack in MOSFETs and allowing further gate dielectric scaling. The next major innovation was introduced at 22 nm: the FinFET [6]. The advantage of this multi-gate device architecture is its better gate control and better immunity to SCE which reduces the subthreshold leakage significantly. This fully depleted device is to some extent very similar to the planar fully depleted silicon-on-insulator (FDSOI) device, where scaling of the channel thickness on the buried oxide (BOX) is used to keep the SCE under control. In FinFET, the gate is wrapped around the up-standing thin channel or fin (Fig. 7.4). The height of that fin FH is an important design parameter that, different from FDSOI, allows to increase the current drivability without having an impact on the active footprint of the device.

The use of fully depleted devices (FinFET and also FDSOI) is key to allow further scaling of the gate pitch and as such implicitly the scaling of the L_G and V_{DD}. The supply voltage V_{DD} of the transistors had been bottomed out at around 1 V at the 32 nm node, even though dissipated power density had gone up to 100 W/cm^2, basically reaching a limit where innovations in packaging and cooling would be needed to guarantee reliable operation of the integrated circuits.

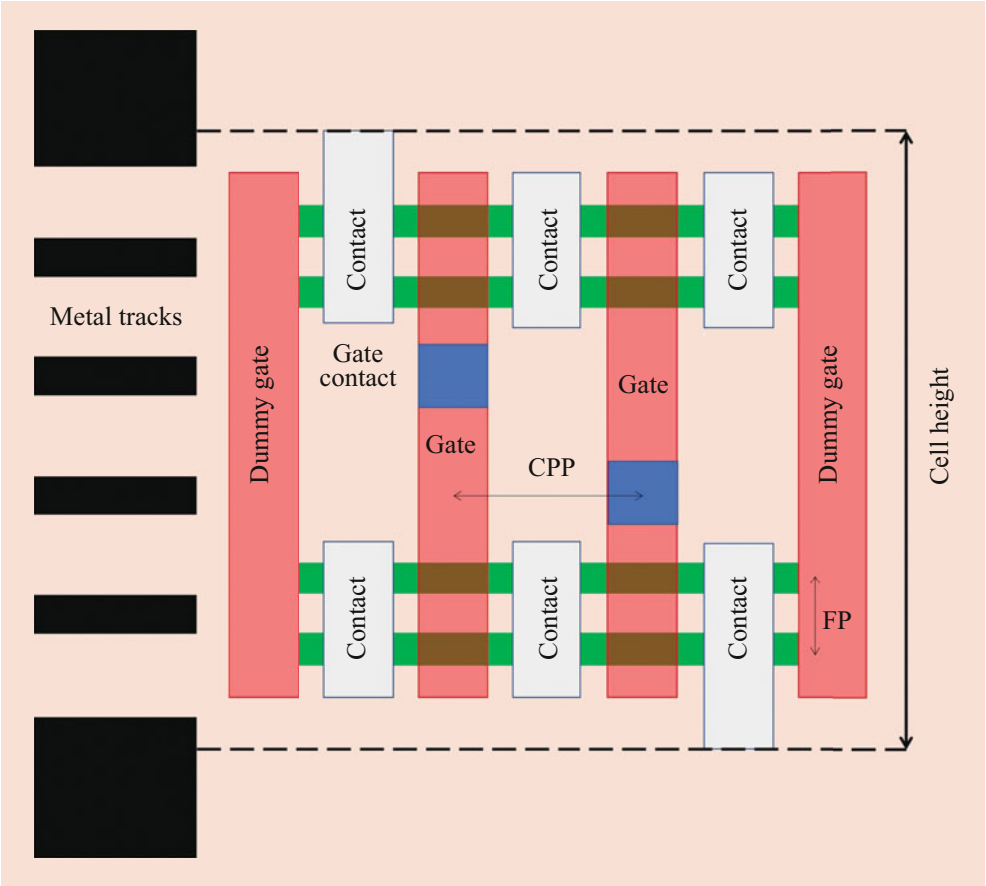

Fig. 7.2 Schematic presentation of the contacted poly pitch (CPP), fin pitch (FP), and metal track, key features enabling area scaling; in this case, the top view of a 6-track (6T) FinFET standard cell layout with four internal tracks for signal routing and the outer V_{SS}/V_{DD} power lines is shown. The device depicted in this figure has two fins per device; the dummy gates are used to ensure that the performance of all devices, center and edge, closely match

The reduced subthreshold swing and thus lower threshold voltage V_T of the FinFET allow to keep the gate overdrive constant while reducing the V_{DD} without compromising the switching speed. State-of-the-art FinFET technologies nowadays show very well-controlled subthreshold swings (~65 mV/dec) down to gate lengths of 20 nm [6].

7.2 From Pure Dimensional Scaling to Design-Technology Co-optimization

The FinFET introduced new features and degrees of freedom that allowed the designers to further reduce the area. The width of the transistor is defined as $W_{eff} = n(2FH + FW)$ where n is the number of fins, FH the fin height, and FW the fin width. While the fin width is largely defined by the gate length and the SCE control, reduction of the fin pitch FP and number of fins n allow to further reduce the active footprint of the device. However, challenges in patterning and device performance no longer allow for aggressive scaling of CPP and metal pitch (MP) (Figs. 7.3 and 7.5), putting a lot more emphasis on the area reduction at standard cell level and block level. While area scaling was before merely a matter of scaling of the basic transistor dimensions, for technology nodes 14 nm and beyond, it has become a matter of standard cell scaling (SDC), entering the area of design-technology co-optimization (DTCO) [7]. Increase of the density is achieved by CPP and cell height reduction which is expressed in the number of metal tracks that are needed to access the standard cell. In the example depicted in Fig. 7.2, the track height is 6 (6T). Reduction of the cell height is achieved by reduction of the number of fins (fin depopulation) and reduction of the number metal tracks by innovations like buried power rail where the power lines (V_{SS} and V_{DD}) are embedded or buried in the isolation and as such partly taken out of the footprint (Fig. 7.6). Buried rail is one of the scaling boosters, special process, and/or layout constructs to facilitate area scaling.

In Fig. 7.7, it is shown that while the CPP and FP are no longer scaling with $\sqrt{2}$, the cell height is. One of the concerns in this scenario is the increasing complexity that the scaling

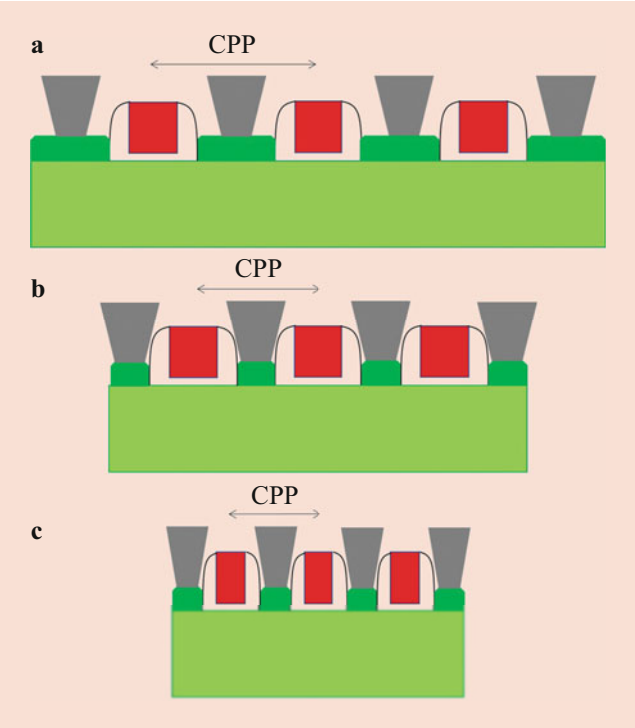

Fig. 7.3 Scaling of the CPP and its impact on gate length, contact area, and spacer scaling; in the case of (**a**) and (**b**), CPP can be scaled down without affecting L_G, spacer, and contact; case (**c**) requires the scaling of gate length, spacer, and contact to allow for further reduction of CPP

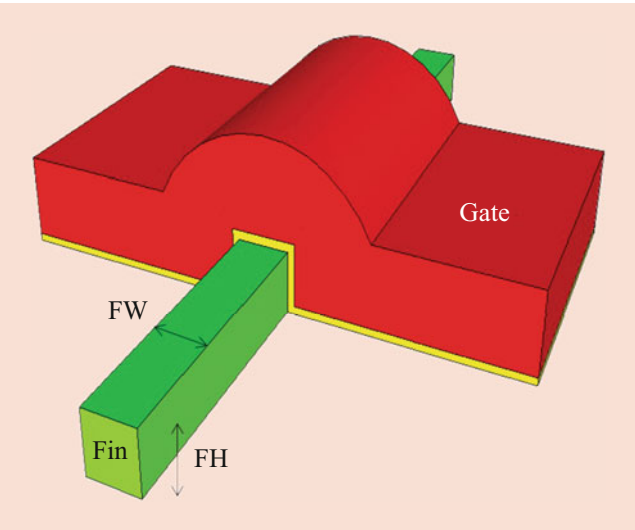

Fig. 7.4 Schematic presentation of a FinFET device indicating the most relevant features FH = fin height and FW = fin width; the current flows in both the sidewalls of the fin and the top of the fin

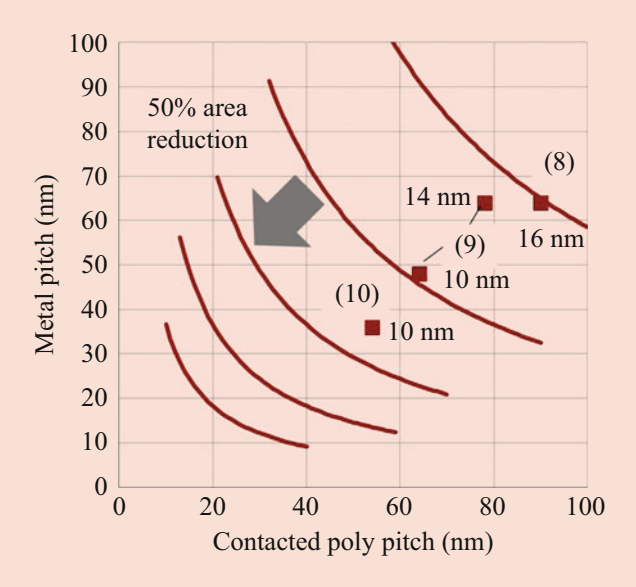

Fig. 7.5 CMOS scaling by contacted poly pitch CPP and metal pitch MP [8, 9]; lines are isolines of constant area; data points of published commercial technologies have been added

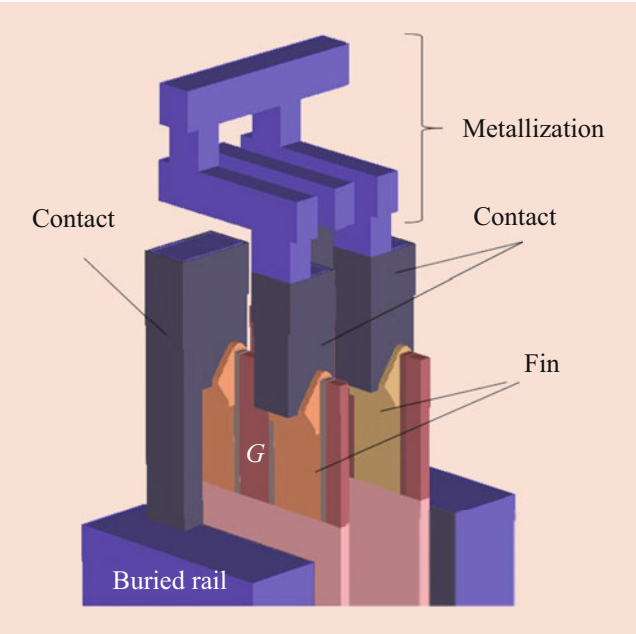

Fig. 7.6 Schematic presentation of the buried power rail [7]

boosters bring and with the trend toward fin depopulation the increase in variability. Moreover, to compensate for the loss in drive current, the fin height needs to increase leading to increased parasitics and challenges to process and integrate these high aspect ratio fins. Fin width control and fin collapse are only a few of the problems that one needs to deal with in this case. Figure 7.7 clearly shows a slow-down in CPP scaling, and this is related to the patterning challenges but more so the device performance. L_G, spacer, and contact are all competing for the limited available area. Reduction of L_G gives room to increase the spacer and contact area but leads to problems in short channel control and thus leakage. Gate-all-around or nanosheet devices are considered here as a possible solution, and this will be discussed in the next section. Reduction of the spacer leads to increase

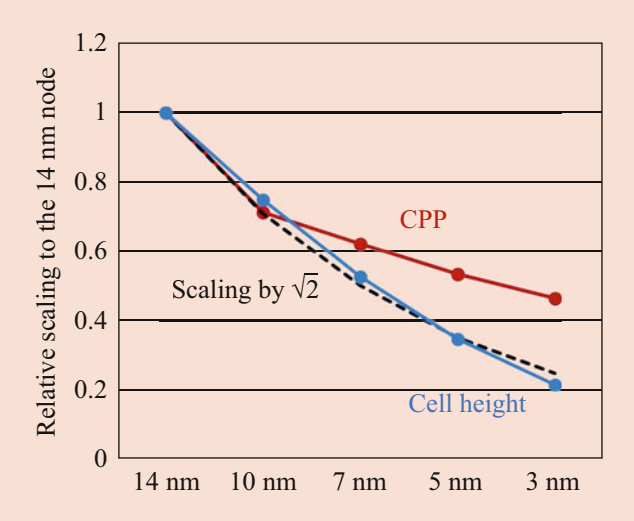

Fig. 7.7 Scaling trends for the contacted poly pitch (CPP) and cell height as referenced to the 14 nm technology node

of the parasitic overlap capacitances. This can be improved by changing the spacer material from nitride ($k \sim 7.2$) to low-k materials like silicon oxycarbide (SiCO) and airgap or partial airgap spacers ($k < 4$). This is again not without challenges both in integration (material conformality, etch selectivity, robustness to cleans, etc.) and at reliability level. Significant reduction of the contact area has led to contact resistance requirements well below 1×10^{-9} Ωcm^2 [11]. This can be achieved by increasing the active doping level in the semiconductor on the one hand (in situ P-doped Si for nMOS and B- and/or Ga-doped SiGe for pMOS) and, on the other hand, choosing the proper contact material. For the latter, direct contacting using Ti is used. While typically no silicidation anneal is performed at contact level, a TiSi alloy is by definition formed at the interface during subsequent processing.

It was reported that in the case of highly n-type doped Si, the contact resistivity tends to saturate at ~2e–10 Ωcm^2 [12], and the electron injection becomes independent of the barrier height between the semiconductor and metal. It is primarily limited by the intrinsic transmission probability of electrons being injected from the metal into the semiconductor, which depends on the Fermi level of the metal and the effective masses of both the semiconductor and the metal, favoring metals with a high effective mass.

Figure 7.8 shows the performance improvement over several technology nodes. While clear performance improvement of more than 20% at constant power could be achieved down to the 5 nm node, the performance increase at the 3 nm node hardly reaches 5–10%. In the best case, a 2-fin transistor was assumed with 30 nm fin height, which offers this power-performance improvement at the cost of larger area (5.5T cell height vs. 4.5T cell height in the case of a 1-fin scenario). The other option with a 1-fin transistor with 50 nm fin height allows for further area scaling but at the expense of lower drive current. At the 3 nm technology node, it is not straightforward anymore to achieve both area scaling and power-performance improvement with the FinFET device architecture. Therefore, there is a lot of interest to look at gate-all-around devices to improve these trade-offs.

7.3 Gate-All-Around Devices: The Evolutionary Path from FinFET

While industry will continue to scale the FinFET architecture further, with a clear trend toward higher aspect ratio for the fin and overall standard cell scaling by reducing the cell track height, likely new device architectures will be needed to keep the subthreshold swing and thus leakage under control for the 3 nm technology node and beyond. In that respect, lateral nanowires (in general called gate-all-around (GAA) devices) have emerged as possible successors of the FinFET device architecture, offering improvement in both power consumption and performance over FinFET at extremely scaled dimensions. Figure 7.9 shows a simulation study comparing the subthreshold swing SS_{SAT} in saturation ($V_{DD} = 0.7$ V) for FinFET devices with different fin widths. As the gate length for the 3 nm technology node will need to be scaled down to 14–15 nm, control of the subthreshold swing ($SS_{SAT} < 75$ mV/dec) becomes challenging, driving the required fin width down to 5 nm. Moving to nanowire devices at 14 nm L_G, however, allows to reduce the SS_{SAT} further and to use more relaxed dimensions as compared to the FinFET case. This is interesting as degraded mobility has been reported for ultra-scaled device dimensions [13]. Next to that, vertical stacking of several nanowires is considered as a way to increase drivability without impacting the active footprint.

These devices can be seen as an evolutionary step from FinFET, having many modules and the overall integration scheme in common as shown in Fig. 7.10. The main differences are related to the starting channel stack, consisting of a multi-stack of thin Si/SiGe layers and the selective removal of either SiGe or Si at the replacement metal gate (RMG) module to form Si or SiGe wires [15, 16]. Process innovations like reduction of the shallow trench isolation (STI) thermal budget and introduction of a SiN liner in the STI module are key to improve the shape controllability and the electrical performance of the devices.

Recent publications have also shown that possible variations of the GAA architecture like nanosheets where elongated thin film slabs (Fig. 7.11) are stacked on top of each other can be very interesting options to keep both electrostatics under control and increase current drivability [17]. Nanosheet devices offer higher W_{eff} per

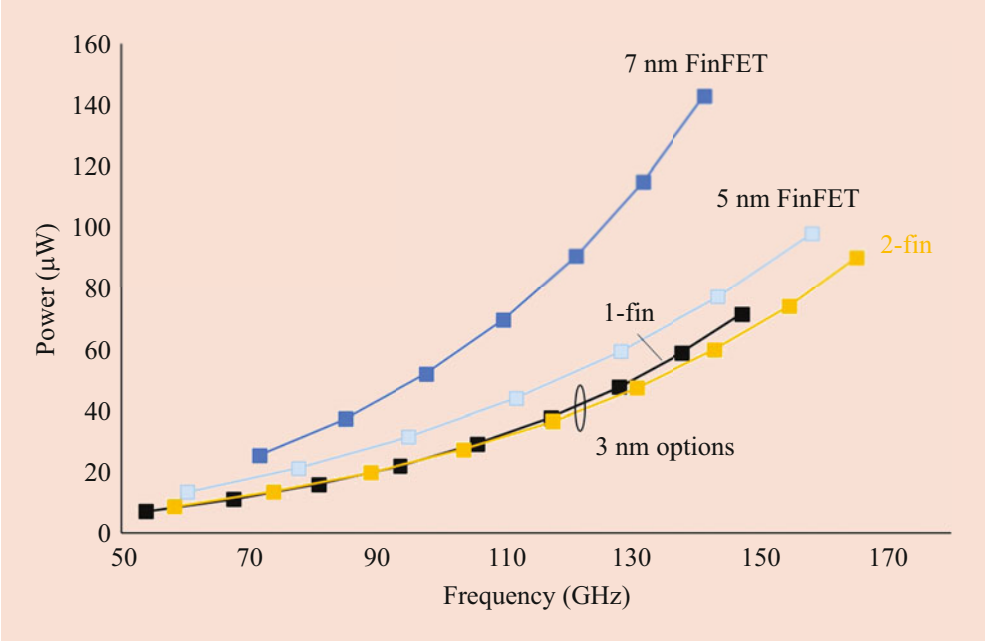

Fig. 7.8 Power versus performance comparing different FinFET technology nodes; the different points represent sweeps at different V_{DD} conditions (starting from $V_{DD} = 0.5$ V, in steps of 50 mV); the 7 nm and 5 nm FinFET devices have two fins

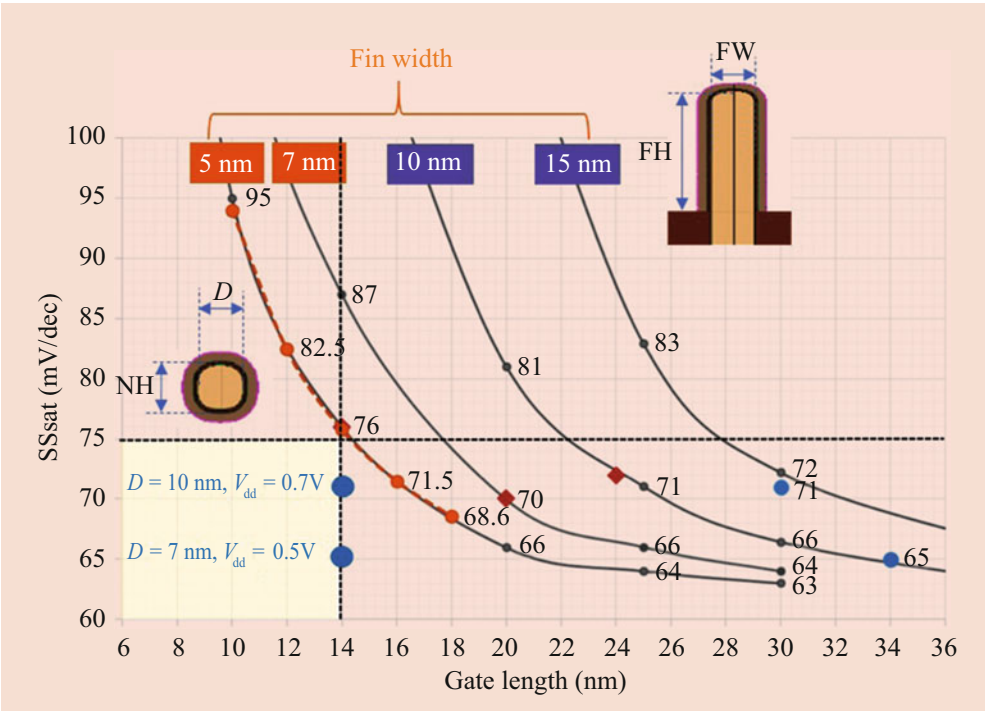

Fig. 7.9 SS at $V_{DD} = 0.7$ V as function of gate length comparing FinFET and GAA or nanowire (NW) devices; especially at shorter gate lengths, the GAA structure outperforms FinFET enabling reduced subthreshold swings; FH fin height, NH nanowire height, D diameter. (©2017 IEEE, reprinted with permission from Ref. [14])

given footprint with a less complex patterning strategy as compared to FinFET where double and quadruple patterning are required to achieve the fin width (~5 nm) and fin pitch FP requirements (~21 nm) for a 3 nm technology. One of the concerns with nanosheets is the possible degradation in electrostatics, but in [17], good short channel control was shown down to $L_G = 12$ nm at a CPP of 44/48 nm. Next to that, higher W_{eff} implies a higher parasitic capacitance, and impact on the dynamic power needs to be considered.

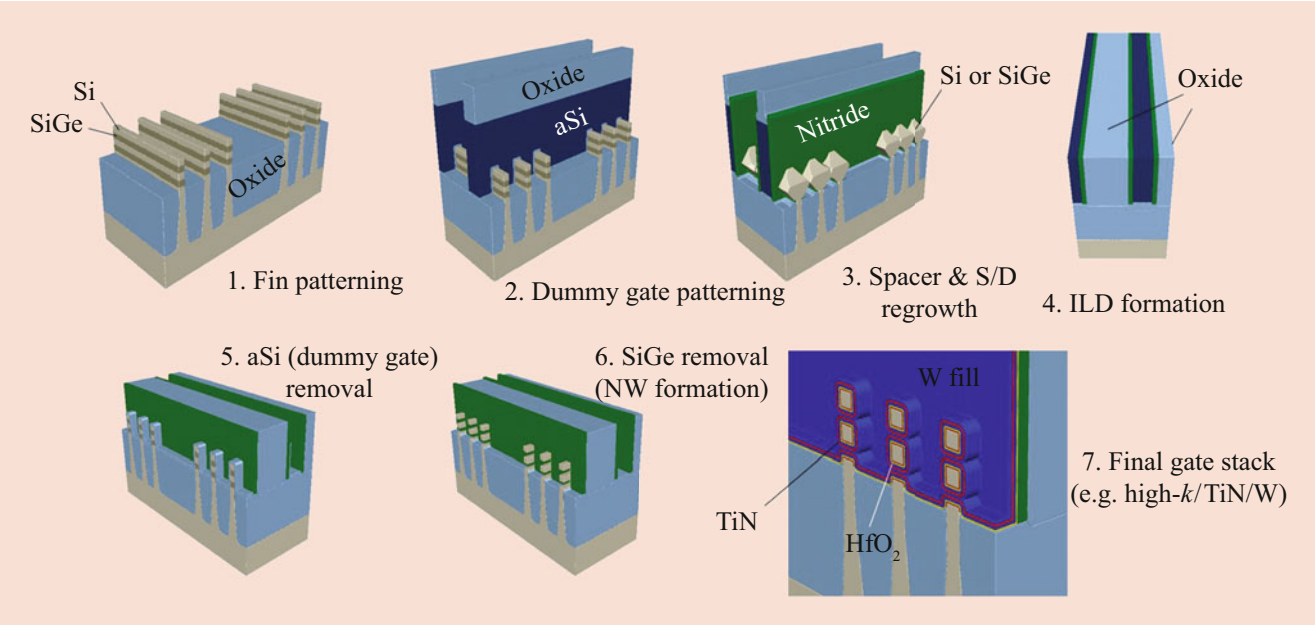

Fig. 7.10 Schematic presentation of the gate-all-around flow, which is based on a typical replacement metal gate (RMG) FinFET flow; the flow is shown up to RMG; starting with fin patterning, dummy gate patterning, spacer formation and S/D regrowth, interlayer dielectric (ILD) deposition and CMP, dummy gate removal, SiGe removal, and final gate stack formation. (©2017 IEEE, reprinted with permission from Ref. [14])

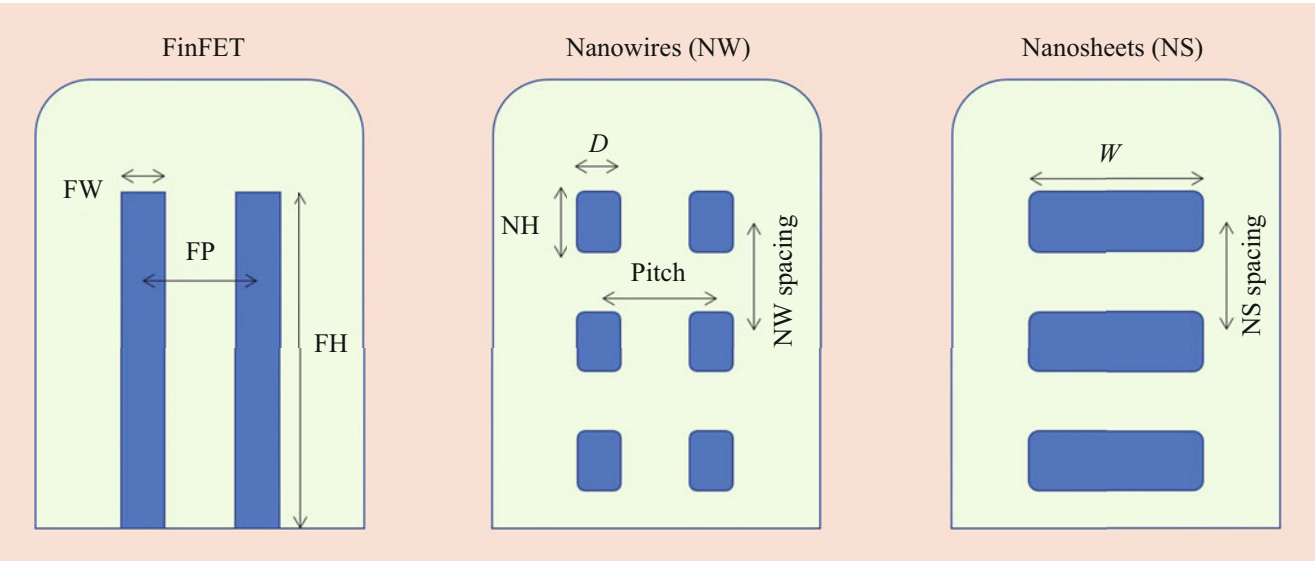

Fig. 7.11 Schematic presentation of FinFET device, a nanowire, and nanosheet device, indicating the most relevant geometrical parameters

In [18], a study is presented looking at the feasibility of 4.5T standard cells using nanosheet devices. The cell layout and parasitics set quite stringent requirements on the nanosheet geometry limiting the design space. Best performance and trade-off were achieved with three sheets with a 21 nm width and tight vertical pitch between the sheets (<14 nm). In that case, the nanosheet 4.5T cell outperforms the 5.5T (2-fin) and 4.5T (1-fin) FinFET cells but needs careful optimization of the intra-cell and inter-cell connections. The devices are most efficient with low fan-out and reduced wire length.

Further improvements come again from device scaling boosters like contact resistivity reduction down to 0.5e–9 Ωcm^2, the use of low-k spacers, and strain engineering (e.g., use of strain relaxed buffers (SRB) and SiGe channel for pMOS). Different from FinFET, the additional complexity

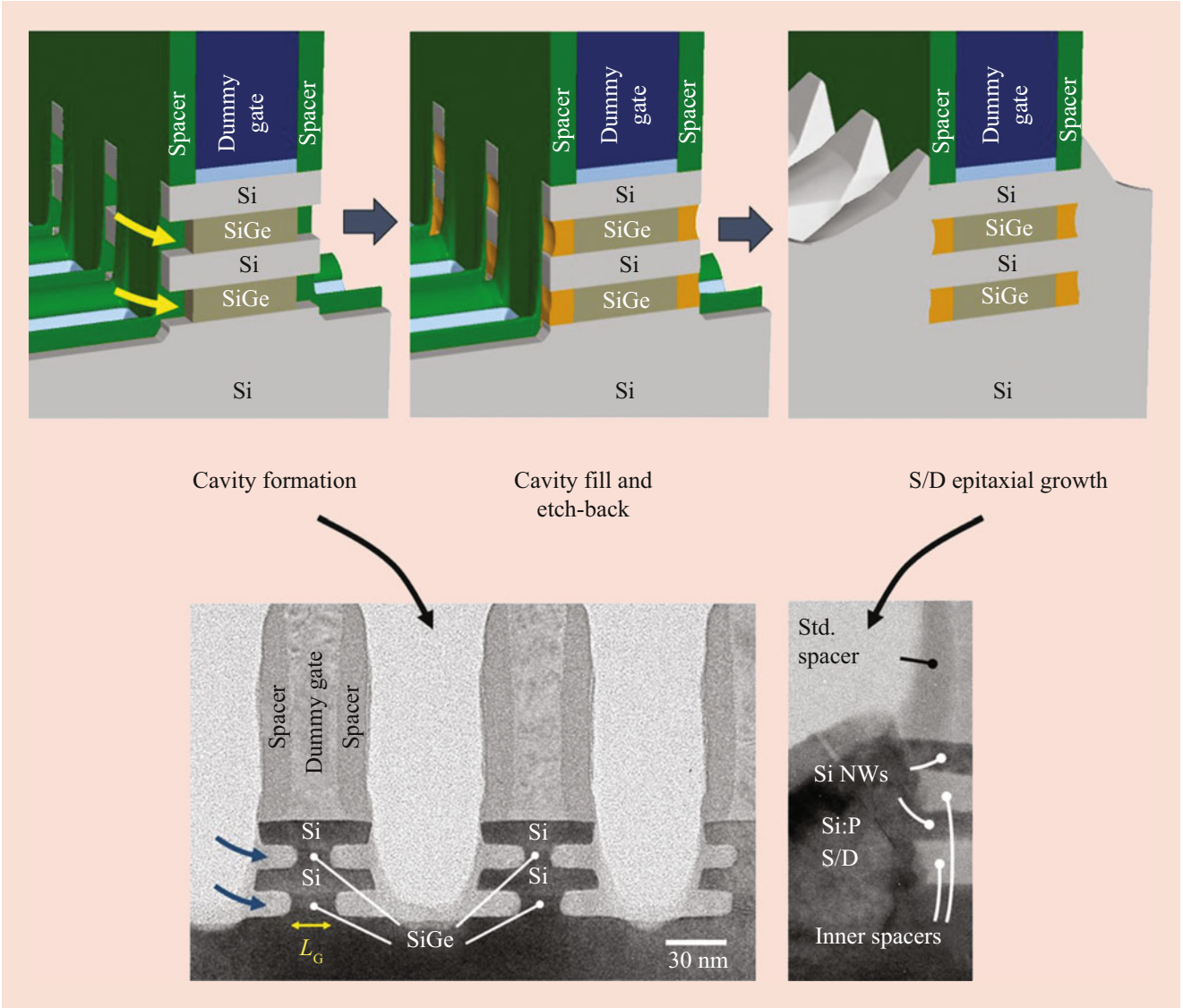

Fig. 7.12 Schematic presentation of the internal spacer formation (in orange) and transmission electron microscopy (TEM) pictures after cavity formation and S/D regrowth. (©2017 IEEE, reprinted with permission from Ref. [20])

for GAA devices in general lies in the use of internal spacers [19, 20] to reduce the parasitic capacitance and improve the ring-oscillator performance. There are several ways of introducing this internal spacer. The most attractive process scheme introduces, after source/drain (S/D) etch-back, a cavity by selectively etching the SiGe dummy layers, still present at that point in the flow, then filling the cavity with the spacer material and etching it back, and finally growing the source and drain areas (P-doped Si in the case of nMOS; B-doped SiGe in the case of pMOS) (Fig. 7.12).

In [19], it is also shown that the use of S/D stressors like SiGe for pMOS can still introduce a significant amount of strain in the nanowire channels. This has also been confirmed in [21] for Ge nanowire devices fabricated on a 70% SiGe SRB. While the Ge wire is relaxed after S/D etch-back, the Ge S/D regrowth on the SRB recovers the strain, and it has also been confirmed that the strain is maintained after wire release and gate stack formation.

Figure 7.13 shows the power-performance trade-off for the different FinFET technology nodes again. In this case, the 3 nm option with nanosheet devices ($W = 21$ nm, 4.5T) has been added. The latter option delivers the best power-performance at reduced area, meeting the requirements for the 3 nm technology node. While on paper this seems the most feasible route to continue scaling, it will require the introduction of all possible device boosters like low-k spacers (incl. internal spacers), contact resistivity below 1×10^{-9} Ωcm^2, S/D strain engineering, and innovations in local interconnects like the introduction of Co or Ru replacing the typical tungsten-based interconnects [10],

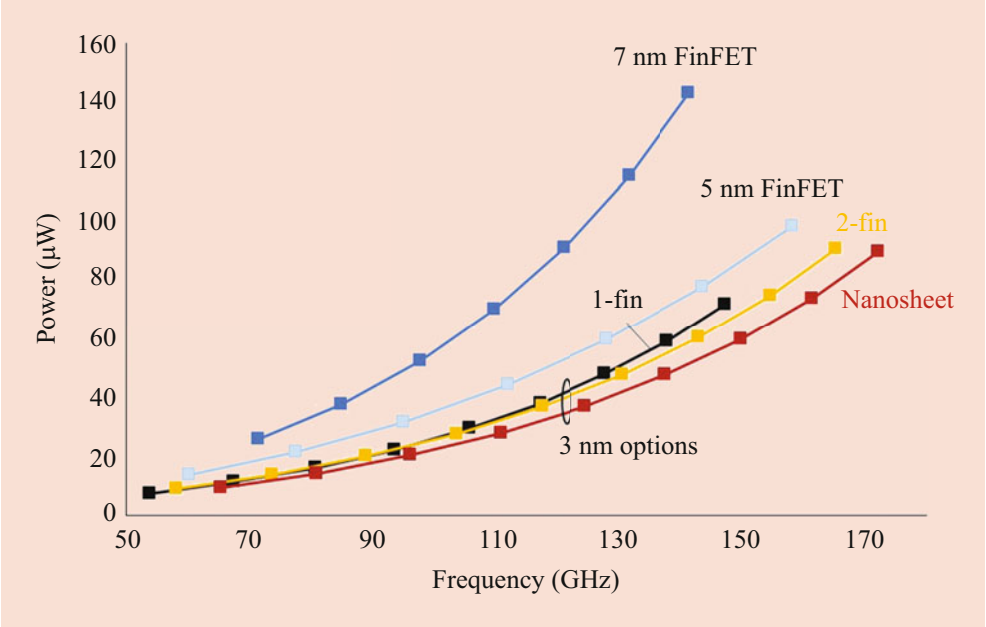

Fig. 7.13 Power versus performance comparing the different FinFET technology nodes and a nanosheet case (4.5T) for the 3 nm technology node; the different points represent sweeps at different V_{DD} conditions (starting from $V_{DD} = 0.5$ V, in steps of 50 mV); the 7 nm and 5 nm FinFET devices have two fins

going hand-in-hand with cell scaling boosters like buried rail and gate over active contact. Next to that, optimizations at the process module level are needed to further improve the shape controllability by modification of the STI, patterning of the multi-stack (Si/SiGe and increased aspect ratio), and improved etch selectivity at the wire release. Furthermore, conformal gate stack solutions that address the tight vertical pitch between the sheets for V_T setting and tuning will be needed. Reducing the vertical pitch means that less area is available to put the high-k dielectrics and the work-function metal layers, and this issue is even more problematic for vertically stacked GAA devices as compared to FinFET [16].

Alternatively, vertical devices are being considered. Vertical transistors (VFET) allow to form GAA structures and truly make use of the third dimension. They have been already successfully introduced for memory applications cfr. 3D NAND. What is quite interesting is that for these devices, the gate length can be decoupled from the CPP and, in principle, this allows further increase of the density. However, challenges in connectivity show that mostly regular designs like SRAM [22] could benefit from the vertical architecture, especially when several layers of VFET devices can be stacked (Fig. 7.14). Overall challenges for VFET are related to the disruptive integration, connectivity, and reduced current drivability due to problems related to the alignment of the gate to the source and drain areas [23] and also contacting of the source and drain, which make them in effect asymmetric devices. So far this architecture is not considered as a possible option to continue CMOS scaling, but needs to be seen rather in the context of heterogeneous integration where one could consider a VFET SRAM co-integrated with FinFET or GAA devices for the enablement of the standard cells (random logic). This can be done using 3D stacking or even co-integrated in the same plane/substrate.

7.4 High-Mobility Materials

New materials in which carriers can travel at much higher velocity than silicon can be solutions to the power density and switching speed dilemma. They allow to reduce the power supply voltage without impacting the device performance and as such would lead to a better power-performance trade-off. However, to be economically viable, these new materials should be introduced on a Si platform, and more specifically, they will need to be compatible with a FinFET or GAA-based technology. Figure 7.15 shows the bulk hole and electron mobility of different semiconductor materials as function of the material bandgap.

III–V materials like InSb, InAs, InP, and GaAs typically have high bulk electron mobilities, while the highest hole mobility can be achieved in Ge. Therefore, research during the last decade was focused on the use of InGaAs materials for nMOS and Ge for pMOS. Ge can also be considered for nMOS, thereby allowing a full Ge CMOS solution [24]. However, gate stack [25] and junction/contact engineering [26] have been identified as the major roadblocks for Ge nMOS, and overall literature shows that Ge n-FinFET is a

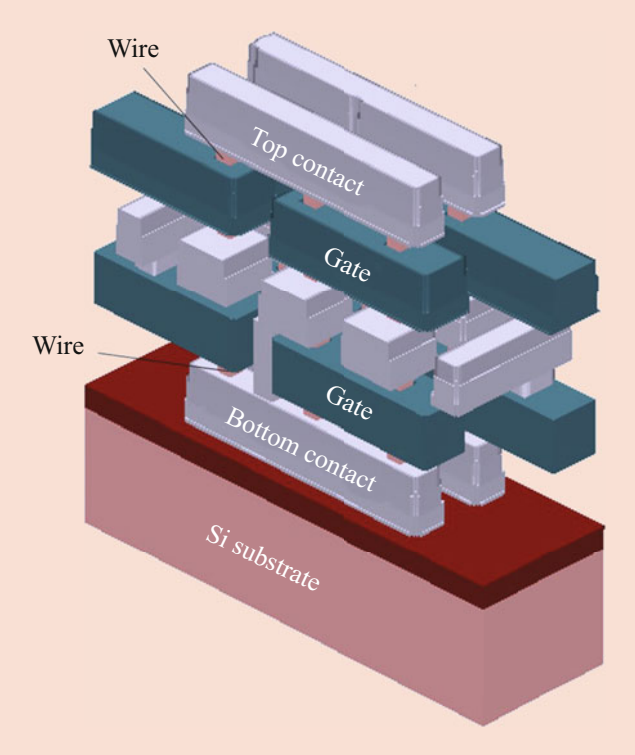

Fig. 7.14 Schematic view of an SRAM using two layers of stacked vertical devices

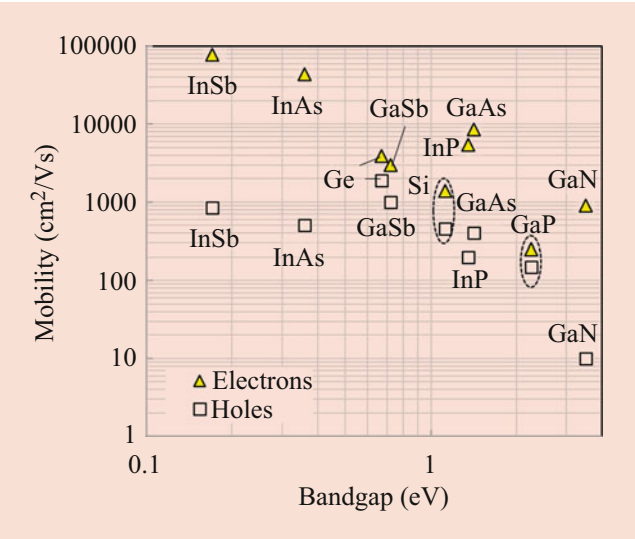

Fig. 7.15 Electron and hole mobility as function of bandgap for different semiconductor materials

rather weak device [27], for now unable to compete with strained Si. Next to the higher mobility and injection velocity, these materials, especially the III–V compound semiconductors, are interesting for the design of heterostructures. These heterostructures allow to fabricate quantum well (QW) devices with increased electrostatic control and more complex architectures like tunnel FET (TFETs) [28].

While high mobility is basically an indicator of high on-state current, the material bandgap shows how far the supply voltage can be scaled down. High bandgap materials typically need a high gate voltage (and thus V_T) to switch the transistor on, and as such, this does not allow reducing the supply voltage V_{DD}. On the other hand, low bandgap materials suffer from high off-state leakage currents as both band-to-band tunneling (BTBT) currents and thermionic emission currents are increased [29]. As such, trade-offs will be needed, and different technology flavors will require different channel materials. High-mobility channels are usually considered for high-performance (HP) applications, while Si devices will be required for low power, thereby highlighting the need for integration on a Si-based platform.

The major challenge related to the integration of these high-mobility materials is the large lattice mismatch (4% for Ge, 8% in the case of $In_{0.53}Ga_{0.47}As$), which introduces a large number of defects in the semiconductor layers. Typically wafer-scale hetero-epitaxy relies on the growth of thick metamorphic buffer layers [30] to achieve lowly defective channel layers, which is expensive and often complicates the integration of different materials on the same wafer. Patterned selective area growth (SAG) is a more appealing route to provide a direct and potentially more flexible means to integrate disparate materials. One such technique is the well-known aspect ratio trapping (ART) method [31], which relies on trapping of defects at the bottom of a high aspect ratio trench. However, reduction of defects along the trench still requires careful optimization of the epitaxial process, e.g., it was found (Fig. 7.16) that the starting Si interface in the trench (e.g., (111) V-groove) and the shape/roughness of the trench profile play an important role in achieving very low defective SAG [32], which was demonstrated for both III–V and Ge. Further reduction of the defectivity has been shown by combining defect trapping and epitaxial lateral overgrowth. In [33], the use of the latter approach, called nano-ridges, has also been successfully demonstrated for the integration of III–V lasers for photonics applications (Fig. 7.17).

Finally, III–V GAA [34] and Ge GAA [21, 35] devices have been demonstrated using either the buffer or the SAG approach (Fig. 7.18). The formation of high-mobility GAA devices, just like in the case of Si GAA devices, relies on the epitaxial growth of a multi-stack of a sacrificial layer and the final channel material. In the case of InGaAs, the sacrificial material is InP that can be selectively removed to InGaAs at the RMG level by HCl. For Ge GAA, SiGe (Ge concentration >50%) is used, but different from Si, the challenge lies in finding a chemistry that can remove the SiGe layer selective to Ge. In [35], a clear improvement in electrostatics for the Ge GAA devices has been shown over Ge FinFET. In the case of III–V, GAA structures allow to leave the channel n-type, thereby forming a junction-less device where the leakage

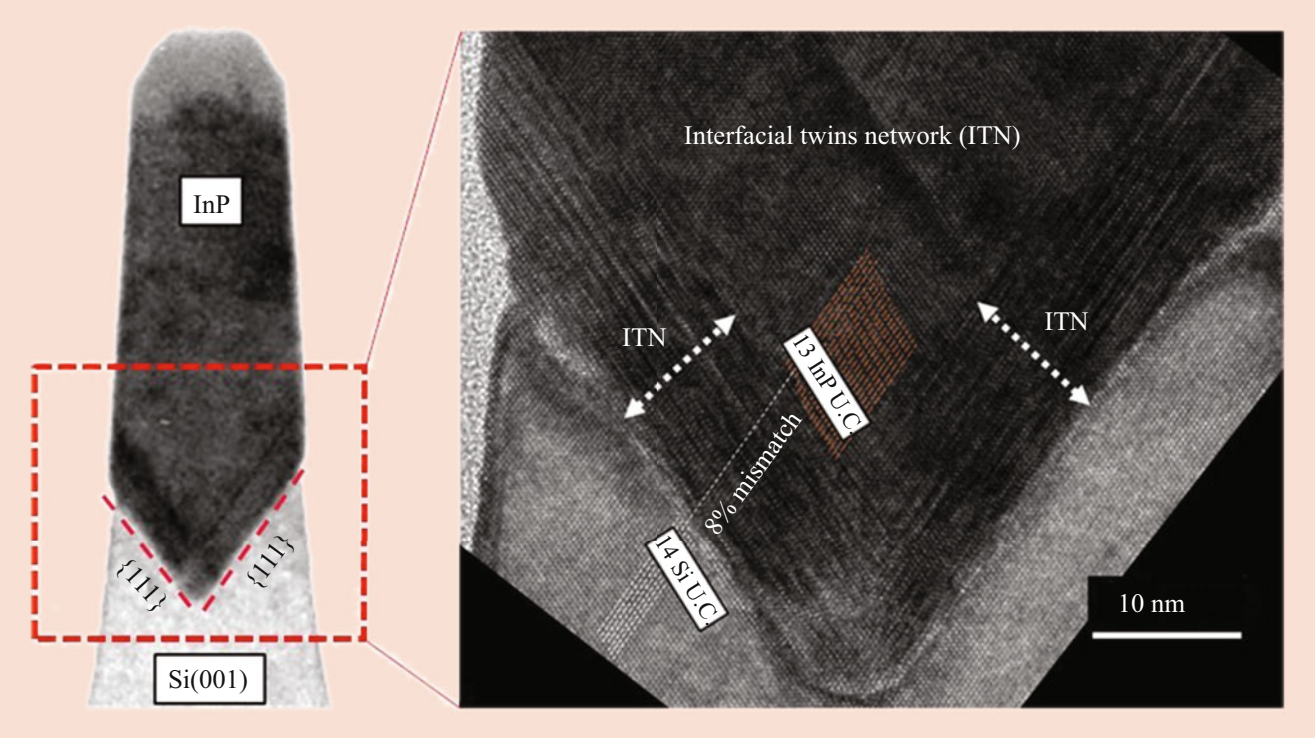

Fig. 7.16 TEM picture of the InP/Si interface where the InP has been selectively grown in the trench; a 10 nm interfacial twin network (ITN) is visible at the interface with the Si accounting for the 8% mismatch between the two materials [32]

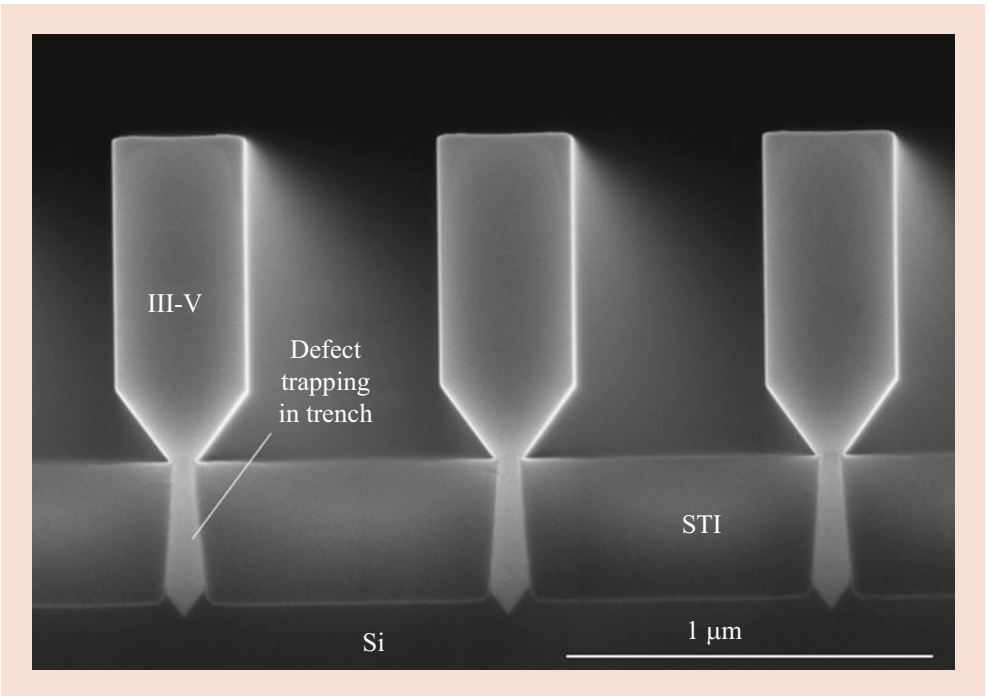

Fig. 7.17 SEM picture of the III–V nano-ridges grown on a 300 mm Si substrate; for this technology, the optimization of the growth conditions and the exploitation of the difference in growth rate on the different facets play an important role

can be suppressed. This cannot be achieved in a FinFET, even in an InGaAs/InP quantum well structure where the conduction band offset ΔE_c between the different materials allows to confine the carriers in the channel. Simulations have

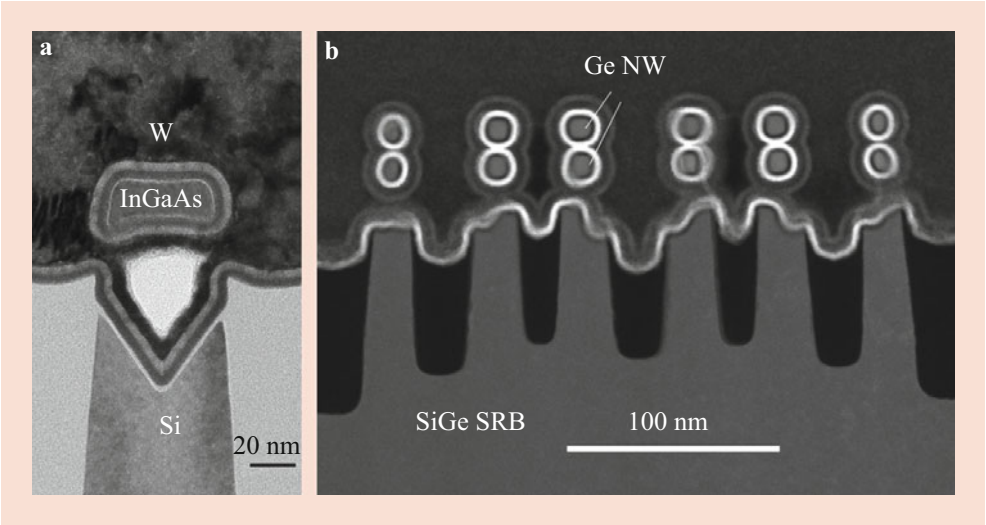

Fig. 7.18 TEM picture of III–V nanosheet devices (**a**) [34] and high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) of a vertically stacked Ge GAA device (**b**) [21]

shown that the 260 meV conduction band offset is not enough to fully suppress the leakage path, especially when the InP cannot be highly p-type doped, and that a combination of InGaAs with InAlAs is more beneficial ($\Delta E_c \sim 460$ meV). The latter material, however, poses many challenges in epitaxial growth, related to both the quality of the material and selectivity.

The difficulty in InGaAs is achieving a p-type doping in the channel to fabricate an nMOS device. Dopants like Zn and Be either are not compatible with front-end-of-line (FEOL) processing or are toxic, while Mg is a good candidate but requires a high number of dopants to be incorporated which deteriorates the quality of the material and the mobility of the devices [36].

Just as the case for Si devices, device scaling boosters like low-k spacers and contact resistivity reduction will need to be introduced to achieve the targets for the 3 nm technology node and beyond. For Ge pMOS, Ga-doped source/drain are quite interesting as about one order of magnitude higher dopant activation can be achieved over B-doped Ge. Even more interesting is that this can be achieved at low temperatures (~400 °C), thereby limiting the diffusion and being fully compatible with the low-T processing required for Ge [37]. Lowering the contact resistivity in InGaAs is more complicated. Only few data points show resistivity values below 1×10^{-8} Ω.cm^2 [38, 39] using InAs as contact material rather than InGaAs because of the Fermi level position in the conduction band. Most metal organic chemical vapor deposition (MOCVD)-grown InGaAs materials suffer from low dopant activation levels ($\sim 5 \times 10^{19}$ cm^{-3}), thereby limiting the contact resistivity levels to $\sim 5 \times 10^{-8}$ Ω.cm^2.

Another challenge related to high-mobility materials is the passivation of the Ge or III–V/high-κ interface which is much more challenging than for Si. Interface engineering and reduction of trapping in the gate dielectric are key to realize a reliable and scaled gate stack. In the case of Ge, the use of Si cap passivation has been very successful in improving the bias temperature instability (BTI) performance [40]. This can be attributed to the fact that only a part or small amount of the oxide traps in the high-κ layer is accessible by the carriers in the channel in the case of relaxed and strained Ge channels as compared to Si. For InGaAs, a large defect peak is observed close to the valence band edge, and a smaller peak exists at mid gap [41]. This can lead to degradation of the subthreshold swing and higher off-state leakage, while Fermi-level pinning in the conduction band severely degrades the on-state performance of the devices. Moreover, the interaction of the carriers with fast border traps or near interface traps can lead to frequency dispersion in both the CV and the MOSFET transconductance curves, leading to significant hysteresis. Recently [42], much progress has been made to find a scalable and reliable gate stack on InGaAs. The solution lies in finding a suitable (low defective) interfacial layer (IL) which reduces the interface traps (D_{IT}) and thus improves mobility, and dipole engineering, by, e.g., using $LaSiO_x$, which allows to decouple the channel carriers from the defects in the HfO_2 layer, thereby significantly improving the BTI behavior.

While much progress has been made in integrating III–V materials on Si in the last decade, there is more and more a consensus that these materials are more suited for particular applications like RF and photonics rather than replacing the channel material in ultra-scaled CMOS technologies. A DTCO assessment shows that while these devices are able to outperform strained Si at relaxed dimensions and reduced V_{DD}, when aggressively scaled down, the advantage becomes

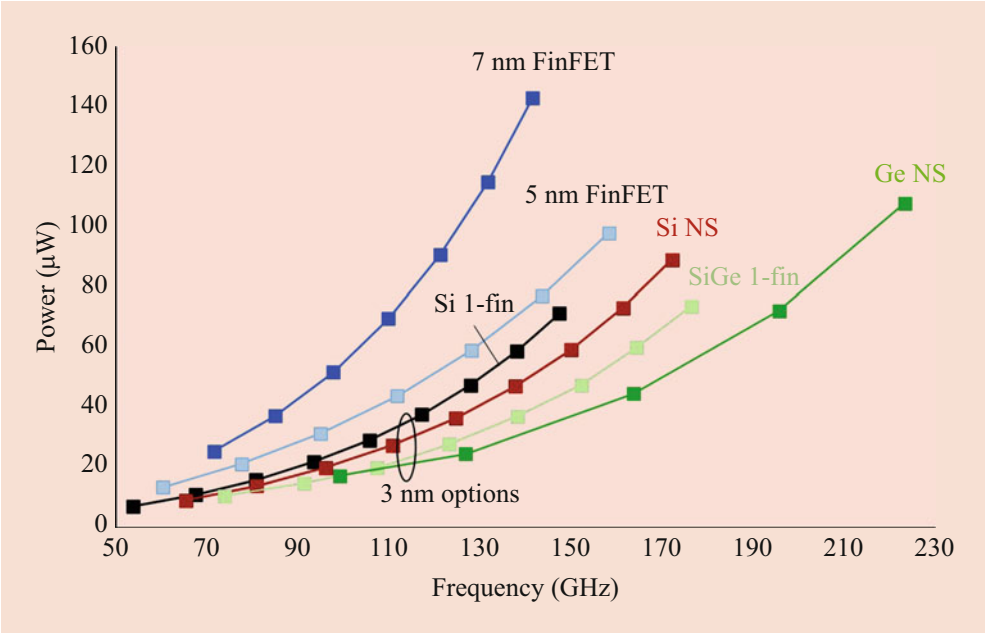

Fig. 7.19 Power versus performance (of a ring oscillator) comparing Si FinFET and Si nanosheets for the 3 nm technology node to a full Ge CMOS nanosheet case and a 1-fin Si/SiGe combination on SRB; the different points represent sweeps at different V_{DD} conditions (starting from $V_{DD} = 0.5$ V, in steps of 50 mV)

less obvious. Moreover, being able to decrease the contact resistivity below 5×10^{-9} Ω.cm^2 and to lower the trap level in the gate stack and the bulk material are key requirements for the comparable performance to Si.

The story for Ge is slightly different. Assuming that a full Ge CMOS solution is possible, 50% higher on-current can be achieved as compared to Si, especially in a GAA structure integrated on a SiGe SRB [43]. Especially the use of Ge nanosheets is interesting and allows even to relax the contact resistivity requirements over Si nanosheet devices. However, the major roadblock for Ge devices remains its high leakage current due to its low bandgap and the enablement of a well-performing nMOS device. The former implies that Ge devices need to be co-integrated with Si devices to enable the low-power device flavors. This can be done by either monolithic integration in the same plane or, even more interesting, using a 3D integration scheme like sequential 3D where the low-T Ge processing is favorable for putting the Ge devices in the top tier.

Alternatively, SiGe has been considered as a pMOS channel material [44]. The higher bandgap allows to target low-power applications while improving mobility and even more importantly the possibility to shift the V_T, enabling a single work function (WF) approach for both Si nMOS and SiGe pMOS and improving the BTI performance [45]. When integrated on a SiGe SRB, a combination of tensile strained Si for nMOS and compressively strained SiGe is possible when the Ge concentration of the pMOS SiGe is higher than the Ge concentration of the SRB [46]. Figure 7.19 shows that the Si and SiGe FinFET devices (on SRB) show better power-performance than Si FinFET. Similar to Ge, the fabrication of a scalable gate stack with low defectivity is, besides the integration of SiGe on a Si platform, one of the key challenges for the introduction of SiGe channels.

7.5 Going 3D: CFET and Sequential 3D Integration

7.5.1 Complementary FET or CFET

One way to continue area scaling is the use of 3D integration. There are different ways of 3D integration: complementary FET (CFET), sequential 3D, through-silicon via (TSV), wafer-to-wafer (W2W) bonding, die-to-wafer (D2W) bonding, or die-to-die (D2D) bonding.

The latter four approaches rely on parallel processing of the different wafers or dies which can contain different devices and technologies and address different functionalities of the system. The density of the interconnections is in these cases not very high and typically allows to connect only at block or (sub)system level. CFET and sequential 3D, however, allow to connect transistors and standard cells over different tiers. However, this comes at the cost of integration complexity.

The CFET is stacking of either nMOS on top of pMOS or vice versa using an integration flow based on GAA integration or even sequential 3D integration (Fig. 7.20). DTCO

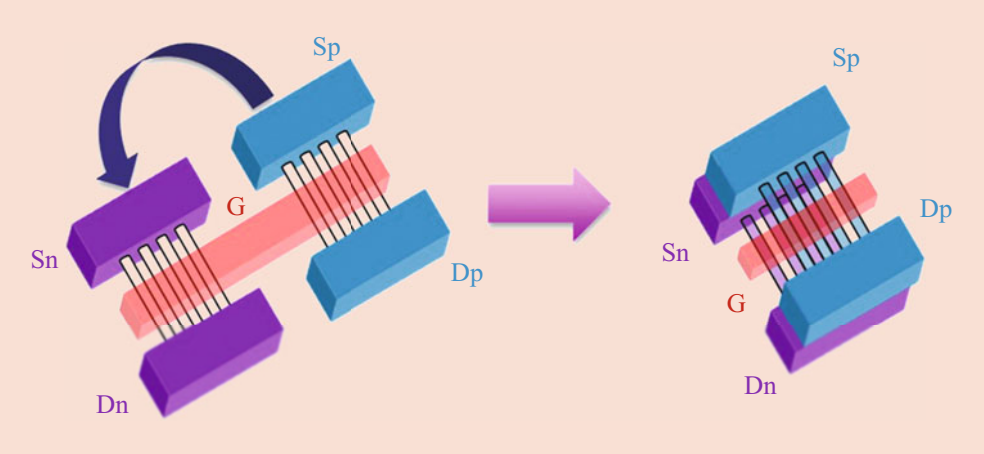

Fig. 7.20 Schematic representation of a CFET device; basically, the nMOS and pMOS devices using a common gate are folded on top of each other; Sp and Sn represent the pMOS and nMOS source, respectively, and Dp and Dn the drain of the pMOS and nMOS, while the gate is common

assessment of this approach has shown a 50% area improvement for both standard cells and SRAM [47], and TCAD simulation predicts that this approach can outperform FinFET and meet the 3 nm technology requirements for speed and power. The area gain is not primarily given by simply stacking the devices but in the first instance by the simplification of the terminals. The complementary nature of CMOS requires pull-up and pull-down networks controlled by common input gates, which the CFET structure uses in its advantage.

The CFET flow can follow a GAA integration flow up to the S/D contact. To separate the top device from the bottom device, the top structure needs to be sealed during S/D growth and bottom contacting. In subsequent processing, the same needs to be done for the top device, while the bottom device is covered with a dielectric layer.

The approach allows to combine different architectures for nMOS and pMOS, e.g., a bulk FinFET bottom pMOS with a GAA top nMOS or a nanosheet top device with a bottom nanosheet device when fabricated on a silicon-on-insulator (SOI) substrate. The top device, however, will always be in essence a GAA structure (nanowire, horizontal or vertical nanosheet).

While the CFET structure brings obvious gains in density scaling and has the potential to improve power and performance, the challenges lie in optimization of the deep vias, highlighting the need for advanced middle-of-line (MOL) integration schemes using, e.g., Ru as an interconnect metal.

7.5.2 Sequential 3D Integration

Sequential 3D integration [48] involves the vertical integration of sequentially processed device layers as shown in Fig. 7.21. After the processing of the bottom-tier devices, the substrate layer for the second tier is transferred, and the process flow continues with the processing of the second-tier devices. Different from the other 3D technologies, where the different tiers are processed in parallel, this integration allows for fine alignment of the top-tier devices to the bottom tier using advanced lithography. As such, a higher density of interconnects can be achieved between the different tiers.

This integration scheme comes in three different flavors. Firstly, in transistor-level stacking (T-S3D), the CMOS level is split into different tiers of pMOS and nMOS. In principle, this is an alternative way of fabricating CFET. The two tiers can be Si devices or use different channel materials. This is especially interesting when one wants to combine, e.g., Ge pMOS devices with Si nMOS devices, materials that have different thermal budget needs. Secondly, in CMOS-level stacking (C-S3D), the 2D standard cells are placed in the different tiers. This means that both tiers require CMOS processing. And thirdly, the partitioning can be done at block level to separate different functional blocks in different tiers, e.g., digital logic and analog and I/O devices or memory blocks and logic. This is referred to as hybrid (or heterogeneous) stacking (H-S3D) where apart from CMOS devices, different flavors of technologies can be combined.

The benefits of the three different flavors of the sequential 3D integration technology have been analyzed through a power-performance-area-cost assessment at 5 nm and 3 nm technology nodes [50, 51] and compared to the respective standard 2D cases where the devices are processed in the same plane. For the hybrid case (H-S3D), the logic and memory part were scaled to the 3 nm node in the bottom tier, and the remaining part (analog and I/O) was assumed to be manufactured in an older 28 nm technology node and put in the top tier. For this particular case, the non-scalable analog and I/O part takes up 30% of the overall circuit area.

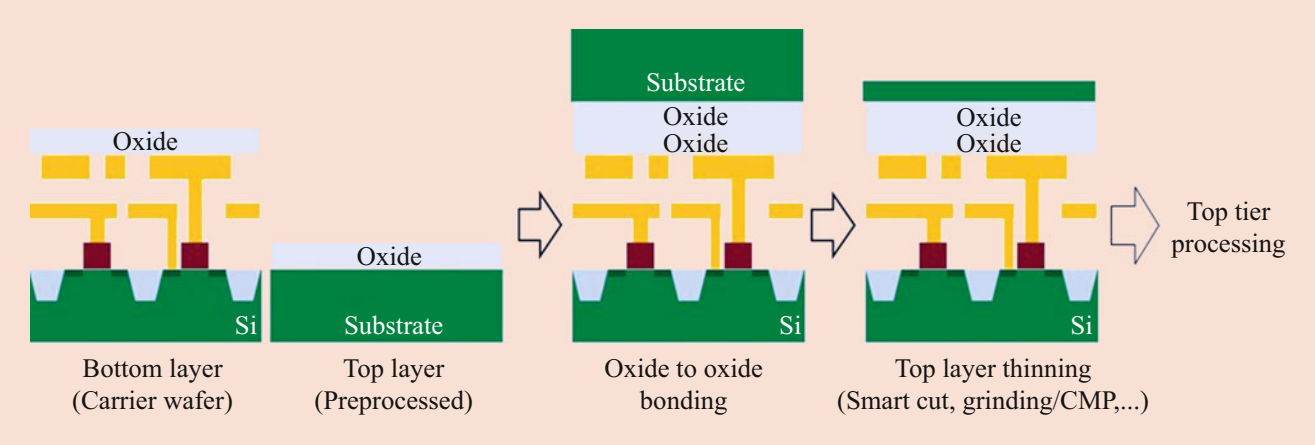

Fig. 7.21 Schematic presentation of sequential 3D processing; in this case, the Si layer for the second tier is transferred using bonding and substrate removal. (©2017 IEEE, reprinted with permission from Ref. [49])

For the T-S3D and the C-S3D cases, little to no cost reduction is obtained compared to the traditional 2D 5 nm and 3 nm implementations (Fig. 7.22). This is mainly due to extra process steps, such as the layer transfer, that significantly add to the cost. Also, depending on the implementation, some of the modules need to be processed twice (e.g., active area patterning, gate patterning, etc.), and this considerably adds to the processing cost of the dies. Next to that, a 50% area shrink is not straightforward to achieve. There is a fundamental limit to the minimum number of tracks needed to enable the cell: at least three to four tracks are required in order to interconnect the transistors (drain/source and gate/gate) and deliver power to the devices. As a consequence, a 50% area gain cannot be achieved for the T-S3D and C-S3D flavors.

Next to possible benefits in area and cost, reduction in RC delay is often seen as one of the advantages of sequential 3D integration. It is expected that stacking of the transistors or cells can relax the cross section of the wires, to some extent. The cell-level S3D case indeed turns out to be beneficial in terms of RC delay, but the results are very much dependent on the process assumptions. When the top tier is as performant as the bottom tier, and the metallization between the two tiers is Cu-based, a 25% reduction in RC delay is expected for the S3D case compared with a 2D implementation. However, due to thermal budget constraints, the performance of the bottom-tier metallization might be degraded as compared to the top tier, especially when Cu cannot be used, and in this case, the reduction in RC delay might be only 15% or even less.

The results of the previously described analysis very much depend on the process assumptions and the technology nodes considered. In [50], the devices are advanced FinFET technologies and mainly FEOL dominated, i.e., heavily dependent on the parasitics in the front-end. With further scaling, devices might become more BEOL dominated, having an increasingly larger RC delay. In this case, due to the gains in RC delay, even for the non-ideal case, the sequential 3D integration at transistor level and cell level might turn out more beneficial over the 2D cases.

T-S3D and C-S3D still are targeted toward overall CMOS scaling. However, applications like 5G, Internet-of-Things (IoT), machine learning (ML), and the increasing demand for data storage will require the enablement of systems with a variety of functionalities. The concept "one device fits all" is increasingly difficult to maintain. For example, while FinFETs are excellent logic devices, their increased parasitics (e.g., increased gate resistance) make them less suitable for high-speed applications, where planar technologies (bulk and FDSOI) outperform the most advanced FinFET technologies from f_t/f_{max} point of view. Hybrid scaling is gaining increasing interest where different technologies come together, leveraging new materials and devices, to enhance and optimize the overall system. This co-integration can be achieved either on the same substrate or through 3D stacking, where sequential 3D brings added value in realizing fine-grained interconnects. This will require system-technology co-optimization (STCO) where optimization is done across many different levels, from process unit steps and integration up to the application level.

A first example was described in [50], combining a 3 nm bottom tier with a 28 nm top tier (H-S3D). For this case, a 33% reduction in die cost was obtained compared to a 5 nm 2D system-on-chip (SoC) implementation (with a 125 mm^2 die size). In the 2D implementation, all devices of the circuit would be fabricated and optimized in the same advanced technology (e.g., 3 nm FinFET technology). With H-S3D, the analog and I/O part can now be moved to a different tier and fabricated with older technologies. This clearly makes the processing less complex and costly. The same holds for the interconnect schemes. The wiring that interconnects the transistors of the scalable parts can be optimized separately from

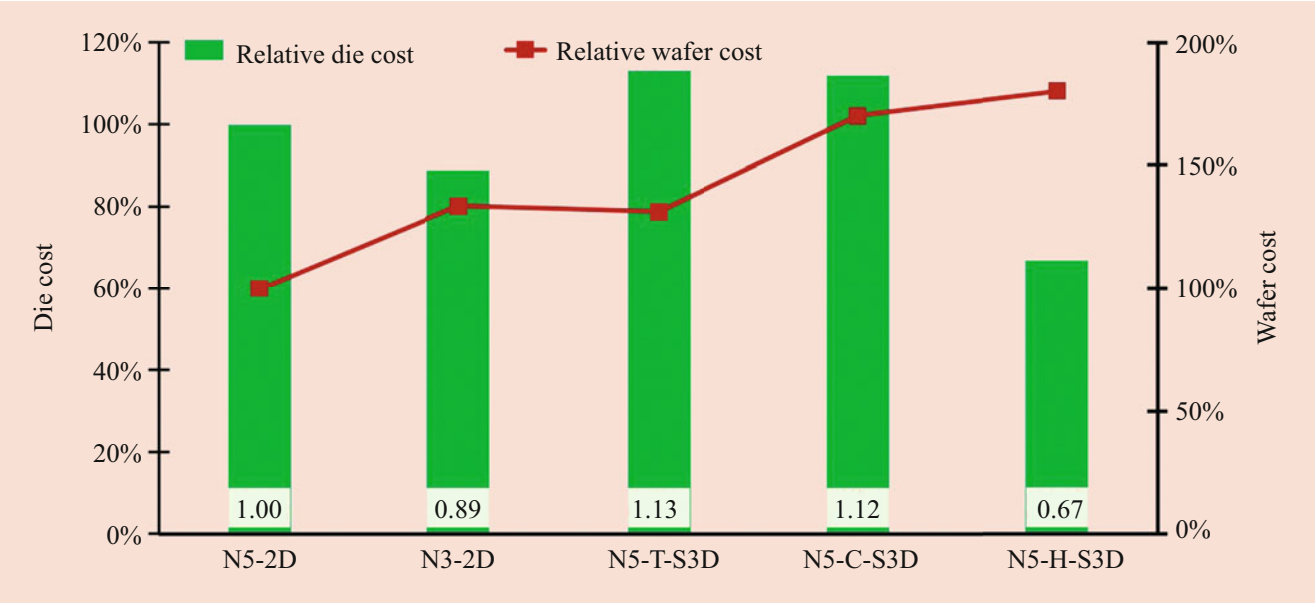

Fig. 7.22 Die cost for different sequential 3D implementations. N5-2D and N3-2D are the 5 nm and 3 nm 2D implementations, respectively; T-S3D, C-S3D, and H-S3D are sequential 3D implementations at transistor, cell, and IP block (hybrid) level, respectively. (©2017 IEEE, reprinted with permission from Ref. [50])

the interconnects of the other tier, and the connection between them can be realized through a regular, dense interconnect scheme, not necessarily in the most advanced technology.

While especially hybrid scaling looks to be an interesting case for sequential 3D integration, there are a number of challenges related to this integration scheme. Layer transfer and the thermal budget constraints are the most pertinent ones. For the layer transfer, approaches based on polycrystalline material deposition and recrystallization or selective epitaxial overgrowth from a seed window have been proposed before in literature. The first approach requires the use of a dedicated ns laser anneal for the recrystallization as the thermal diffusion to the underlying device layer needs to be limited as much as possible. Moreover, the quality of the material after recrystallization is questionable. The selective epitaxial overgrowth approach suffers from limited density, high thermal budget, poor control of thickness, and material defectivity close to the seed windows. The most interesting relies on layer transfer based on wafer-to-wafer bonding (oxide-to-oxide or SiCN-to-SiCN [52]) is an attractive approach. It can be enabled at low temperature (400 °C) and leads to defect-free material with very tight control of the thickness uniformity. As donor wafers, either SOI wafers can be used where the BOX can act as a stopping layer during substrate removal, or a modified SmartCut™ process can be used to transfer only part of the engineered substrate. The latter has the advantage that the donor wafer can be reused several times, making this a more cost-effective process. Stacked planar devices [53] as well as high-density FinFETs [54] have been demonstrated using this bonding approach, as is shown in Fig. 7.23.

The concerns related to thermal budget are twofold: the top-tier device integration needs to avoid high-temperature process steps to reduce possible impact on the bottom-tier devices, while the temperature robustness of the bottom tier needs to be improved to withstand the additional thermal budget coming from the top tier. The process steps with the highest thermal budget for a standard transistor fabrication are typically the anneals (>1000 °C) used for dopant activation, the selective source/drain epitaxial growth (pre-bake ~800 °C and growth ~750 °C) for thin film devices, and, in the case of RMG processing, the dummy a-Si gate deposition (~600–700 °C) and the anneal to improve reliability performance when high-k dielectrics are used (~800–900 °C).

There are a number of integration and device approaches that can be considered to tackle the concerns mentioned above. Junction-less devices have been considered in [53, 54] for the top-tier devices. In this case, the implantation and dopant activation can be done before the layer transfer, while the use of laser anneal, similar to the recrystallization scheme, is a viable alternative to activate the dopants after the layer transfer while limiting the thermal diffusion [55].

Depending on the technology that is envisioned for the bottom- and top-tier devices, there might be a clear concern about the gate stack stability, especially when a gate last process is needed. The issues regarding the gate stack are twofold. For the bottom-tier devices, a thermally stable gate stack is required in order to sustain the total thermal budget

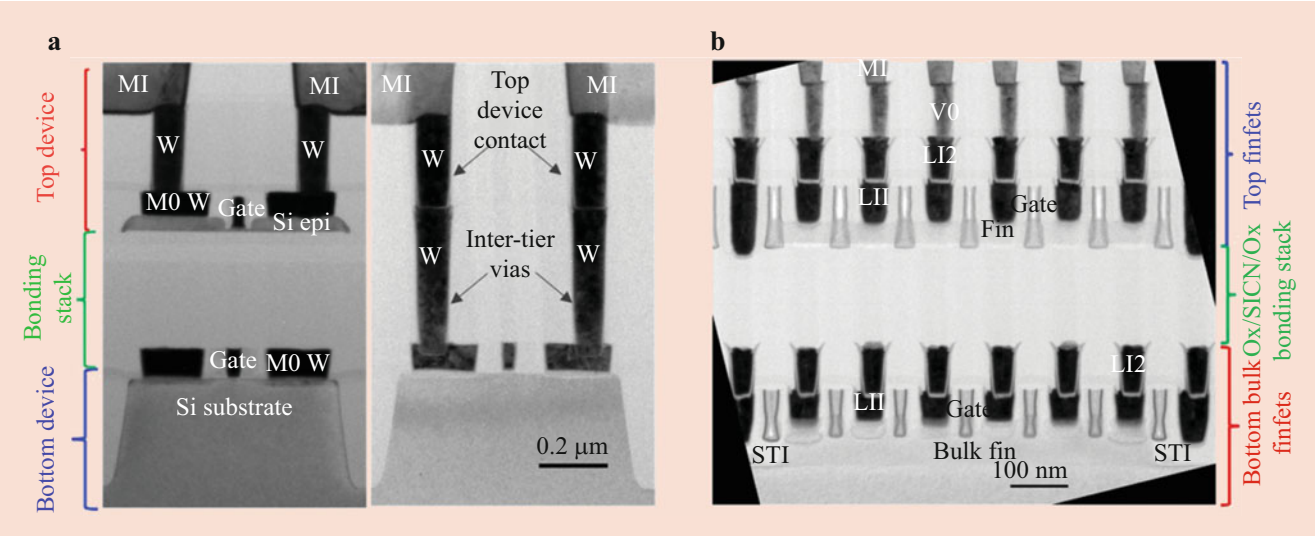

Fig. 7.23 TEM picture of stacked planar devices (**a**), also showing the connections (inter-tier vias) to the bottom tier devices; (**b**), the TEM picture showing the top SOI-based FinFETs stacked on bulk FinFET devices, FP = 45 nm and CPP = 110 nm. (©2018 IEEE, reprinted with permission from Refs. [53, 54])

of the top-tier device processing, which can consist of long anneals at low temperature. The non-ideal thermal budget may lead to shifts of the metal gate work function, metal diffusion in the gate stack, equivalent oxide thickness (EOT) increase, and degraded reliability. The use of proper diffusion barriers is needed to ensure a stable gate stack. In [56], it is shown that when carefully optimized, a limited top-tier thermal budget (in this case 520 °C 2 h) can be as efficient as a dedicated reliability anneal.

For the top-tier devices, low thermal budget processing is required to avoid degrading the bottom devices. But this low-temperature processing typically results in gate stack reliability issues for the top-tier transistor as is shown in Fig. 7.24. When compared to the same high-k/metal gate stack including a reliability anneal, the behavior of the low-temperature gate stacks is much degraded and fails to meet the BTI targets for both nMOS and pMOS.

In [56], two strategies were proposed to improve the reliability performance of the top-tier devices: the use of junction-less devices leads to a lower electric field, thereby reducing the density of charging oxide traps and improving the performance as indicated in Fig. 7.25. This improvement is more pronounced as the doping level in the devices is increased. While there is a clear benefit for device reliability, a trade-off will be needed as the increased doping level leads to reduced mobility and increased variability at the same time. A second approach relates to dipole engineering where a thin layer is introduced between the interfacial SiO_2 and HfO_2 to induce an interfacial dipole which modulates the effective work function and beneficially decouples the high-k defect levels from the channel Fermi level (Fig. 7.26). For nMOS, $LaSiO_x$ is used, while for pMOS, Al_2O_3 can be used. The latter only works in combination with a thin interfacial oxide.

While there are still many challenges ahead to make this a cost-effective integration approach, sequential 3D is gaining more and more attention in the context of heterogeneous integration these days.

7.6 Conclusions

While the industry is moving to the 7 nm and 5 nm technology nodes, the increased pressure on Moore's law is becoming clear. Increased complexity in patterning and process steps, difficulties in scaling of the transistor dimensions, and keeping power dissipation and parasitics under control are the grand challenges that FinFET scaling will be facing in the coming years, moving to 3 nm and beyond. Gate-all-around devices, in the form of either nanowires or nanosheets, can in principle extend the device scaling, but challenges especially in contact resistance and parasitic capacitance reduction will need to be overcome. Replacing the Si channel by higher-mobility materials, especially SiGe and Ge, is at least on paper an interesting scaling booster but addresses only part of the overall system requirements. Ge devices can outperform their Si counterparts but pose a problem for the leakage reduction, where co-integration with Si is a must for the low-power applications. Moreover, to be considered as an interesting option, a full Ge CMOS technology needs to be enabled. Many challenges in gate stack and contact/junction engineering need to be overcome to improve the Ge nMOS device. In that respect, SiGe channel can be seen as a good compromise.

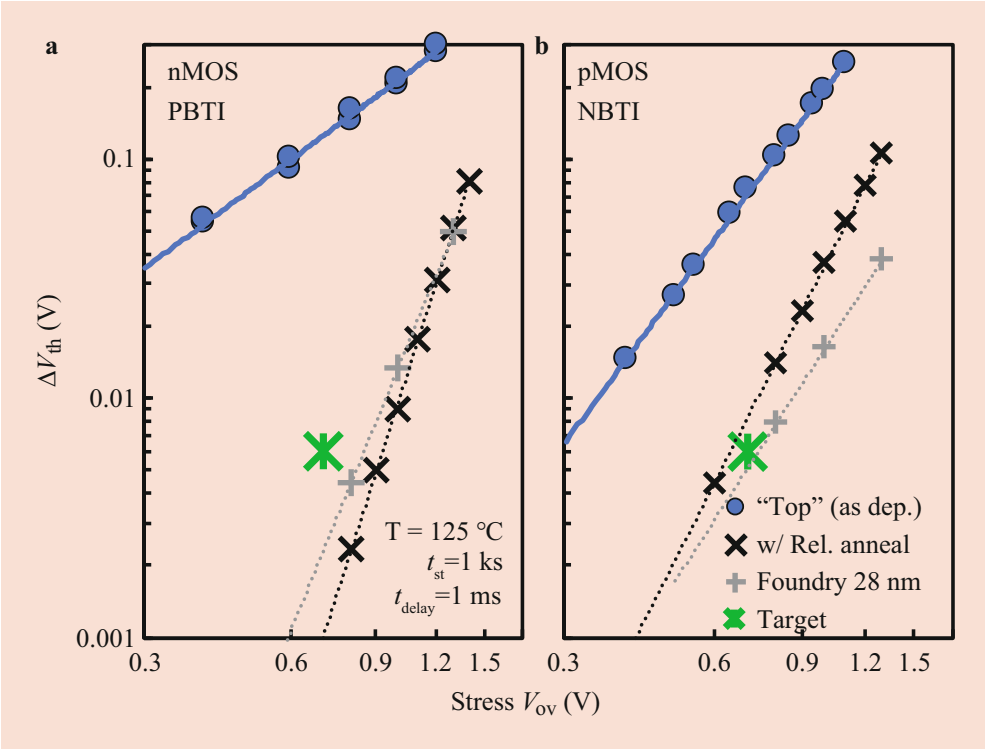

Fig. 7.24 BTI performance of a low-temperature metal gate/high-*k* gate stack for the low-temperature top-tier devices (nMOS in (**a**) and pMOS in (**b**)) compared to devices with the same stack but with a high-temperature reliability anneal and a 28 nm foundry reference. (©2018 IEEE, reprinted with permission from Ref. [56])

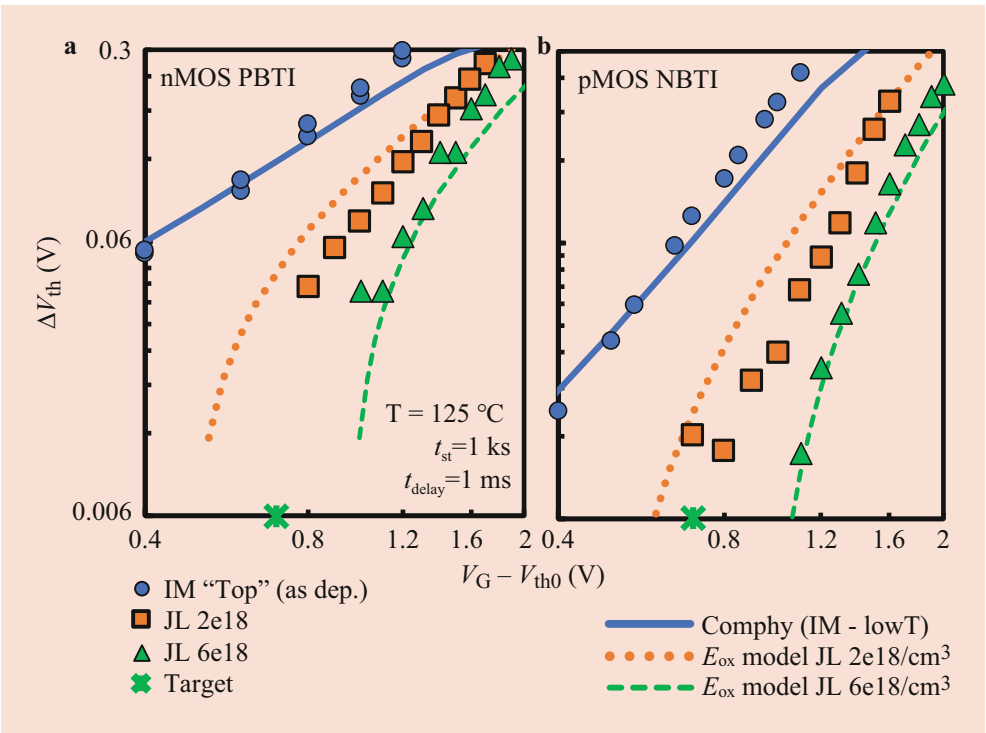

Fig. 7.25 (**a**) nMOS PBTI and (**b**) pMOS NBTI measured in inversion mode and junction-less devices with different doping levels; the same low thermal budget gate stack is used for all cases; the measured results are also compared to the ComPhy simulations [57]. (©2018 IEEE, reprinted with permission from Ref. [56])

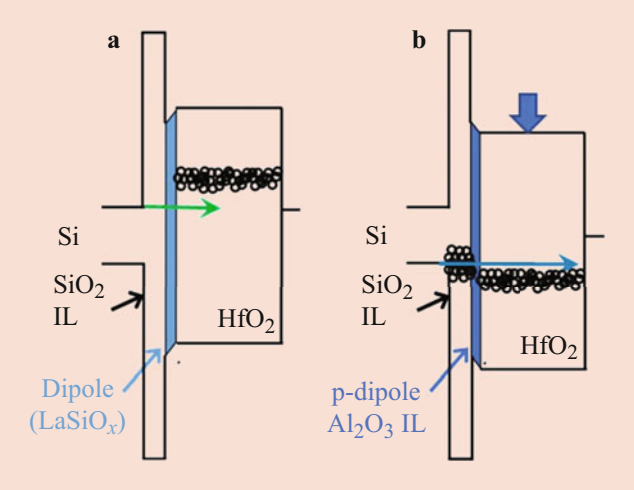

Fig. 7.26 Schematic presentation of the band alignments showing the displacement of the channel carriers with the defects in the high-*k* and interfacial oxide using dipole layers: $LaSiO_x$ for nMOS (**a**) and Al_2O_3 for pMOS (**b**) are used as dipole layers; ©2017 IEEE, reprinted with permission from Ref. [49, 56]

For long, III–V materials have also been considered as replacement of the Si channel, boosting the performance and allowing further V_{DD} scaling. Today, however, there is a clear consensus that these materials lose a lot of their benefits when scaled down below 10–15 nm, to the extent that these devices, even in the most ideal case, do not outperform Si. Nonetheless, these materials are gaining again a lot of interest in the context of photonic applications (III–V laser integration) and RF applications, addressing several challenges of next generation of mobile communication 5G.

Finally, 3D stacking, with several possible implementations, will be key for heterogeneous integration where scaling will be taken at an even higher level of abstraction. The benefits for standard device scaling are not always so straightforward, and while CFET, largely based on a gate-all-around integration flow, seems an interesting candidate to continue 50% area scaling with clear power-performance improvements, the complexity in enabling the different device connections will need to be closely studied in the coming years.

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Advanced Lithography

8

Alberto Roncaglia

Contents

8.1 Lithography Basics 279
8.1.1 Image Formation in Lithography 281
8.1.2 Resolution Enhancement Techniques 284

8.2 Advanced Lithography Based on ArF 193 nm DUV Sources 286
8.2.1 Resist Thickness and Plasma Etching Selectivity 286
8.2.2 Multiple Patterning Techniques in ArF DUV Lithography 288
8.2.3 Photoresists for 193 nm DUV Lithography 290

8.3 Non-optical Lithographic Methods 293
8.3.1 Electron Beam Lithography 293
8.3.2 Nanoimprint Lithography 294

8.4 Extreme Ultraviolet Lithography 294
8.4.1 Requirements for EUVL Photoresists 295
8.4.2 Laser-Assisted Plasma Sources for EUVL 297
8.4.3 EUVL Chemically Amplified Photoresist Chemistry 300

8.5 Conclusion 306

References 307

Abstract

The chapter provides an overview of recent advances in lithography for the production of integrated circuits (ICs). In the first section of the chapter, a brief introduction about lithography basics such as image formation, image resolution in projection systems, and resolution enhancement techniques is provided. In the following section, advanced lithography based on ArF 193 nm deep-UV (DUV) sources is discussed thoroughly, including photoresist requirements and characteristics, plasma etching selectivity, and the multiple patterning techniques commonly adopted for resolution enhancement in these processes. After mentioning some non-optical lithographic methods such as electron beam lithography and nanoimprint lithography, which are mainly employed for mask fabrication or niche applications, a detailed discussion is dedicated to extreme ultraviolet lithography (EUVL), which represents the technology of choice for the future and promises to be able to support a further scaling of ICs' critical size, as required by Moore's law. In particular, the evolution of EUVL laser sources based on Sn plasmas over the years is described, and their role in the diffusion of the technology is discussed. The requirements of EUVL resist are also described along with the role of stochastics, which are especially relevant for this technology because of the lower number of photons involved in resist exposure compared to the former DUV technology. In the end of the chapter, the mechanisms related to EUVL resist development are analyzed, including energy deposition, acid generation, and polymer deprotection.

Keywords

Lithography · EUVL · DUV · ArF · Photoresist · Radiation chemistry · Laser plasma sources

8.1 Lithography Basics

Moore's law, which defines the path for the development of microelectronics, foresees a continuous shrinking of the minimum feature size of integrated circuits (ICs). Such dimensional scaling has a direct impact on requirements of the photolithographic processes. The advanced lithographic systems used nowadays permit to pattern deep-submicrometric geometries in ultraviolet (UV)-sensitive resist layers after exposure in a projection system and subsequent development of the exposed resist.

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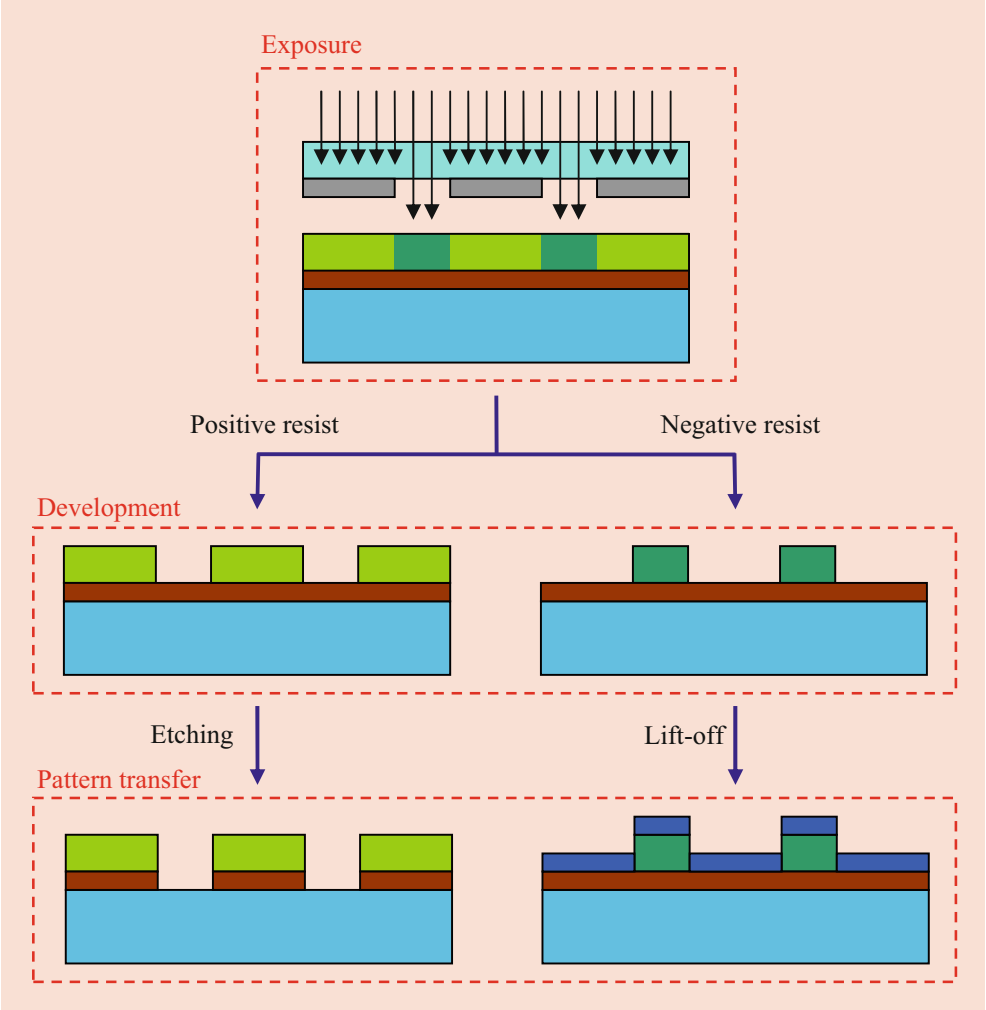

Fig. 8.1 Basic steps of photolithographic patterning procedure

The basic principle of photolithography is simple. A layer of photosensitive material is deposited on the wafer and afterward exposed to light through a patterned optical photomask (or reticle), in which some areas are transparent and other ones opaque. The absorption of light on the exposed parts of the resist layer induces chemical modifications in the material that are exploited to selectively remove exposed (positive resist) or unexposed (negative resist) parts. This selective removal procedure is performed by means of specific chemical solutions named resist developers and is called development. In positive resists, the unexposed material is insoluble in the developer and becomes soluble after being exposed to the light; in negative resists, instead, the material is natively soluble in the developer and becomes insoluble with the exposure. After the development procedure, some parts of the wafer will be still covered by photoresist, whereas other ones will be stripped. In this way, the pattern created on the photoresist can be transferred onto the wafer either using a selective etch that is slow enough on the resist to reach a target depth on the stripped areas without completely uncovering the protected regions (subtractive pattern transfer) or employing the resist as a stencil for a selective deposition (lift-off) process (additive pattern transfer), as illustrated in Fig. 8.1.

The performance of a resist material can be evaluated by measuring its exposure response curve, which is a linear-logarithmic plot reporting the resist thickness remaining after development normalized to the initial thickness (p) versus the exposure dose (D) used in the process.

The contrast parameter is calculated as shown in Fig. 8.2 for positive and negative photoresist and is related to the slope of the linearly variable part of the exposure curve. The resolution that can be achieved with a specific resist is related to contrast, since higher resolution is possible on resists with larger contrast parameter.

The way in which the reticle for selective exposure of the resist, named mask, is utilized in the exposure process distinguishes the two main types of lithography. In contact

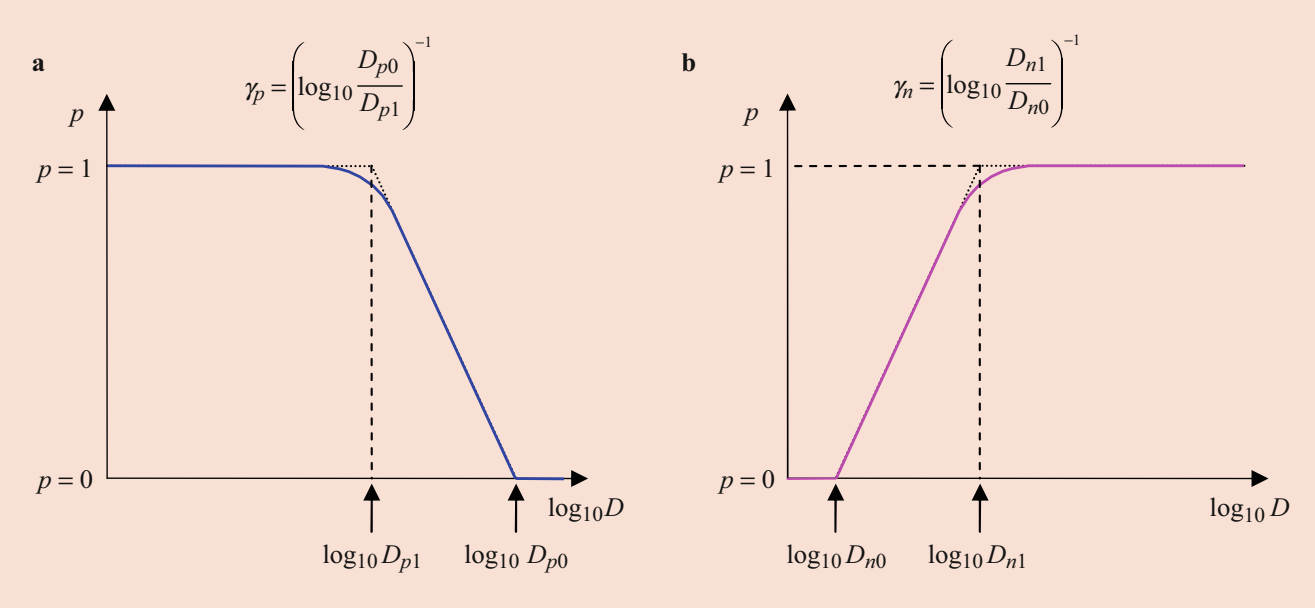

Fig. 8.2 Calculation of contrast parameter (γ) for positive (**a**) and negative (**b**) resist

lithography, the mask is a slab of glass or quartz, on which an opaque pattern is produced using a thin chrome layer. The mask is used during resist exposure after being placed in contact with the resist layer with the chrome-covered face downward. In order to achieve the highest possible resolution, the contact between the mask and the wafer must be performed in such a way that no space remains between them (hard contact), avoiding undesired light diffraction effects that may alter the pattern geometry.

The other possible method to perform the exposure employs the mask to project its transmission pattern onto the resist layer by means of an optical projection system that decreases the original size of the designed geometries in the focal plane, thus increasing the resolution.

With this method, the projected shadow of the mask on the wafer is generally small, and consequently a stepping or step and scanning system is normally needed to replicate the mask geometry several times on the wafer until a full exposure of the wafer is obtained. However, the advantages that projection systems provide in terms of resolution are so significant that contact lithography, which was utilized in the early phases of the development of the technique, has been now completely abandoned in massive IC production in favor of projection lithography. Since scanners used in projection lithography operate by repeating the projection of the mask several times on the wafer after stepping a predefined distance between two adjacent patterns, they are commonly named either step-and-repeat systems (i.e., steppers) or step-and-scan systems (i.e., scanners).

8.1.1 Image Formation in Lithography

Three fundamental methods can be adopted to transfer the image of the pattern from the mask to the photoresist layer (Fig. 8.3): contact, proximity, and projection lithography.

Projection lithography is preferred for production, whereas contact and proximity lithography are often employed in research because they are simpler methods that can be implemented with cheaper equipment.

A key issue in image formation is the achievable resolution (or half-pitch) that can be obtained on the resist after exposure. Since the photoresist needs to receive a sufficient radiation dose in order to change its solubility properties and form the pattern correctly, the light distribution on the resist during exposure needs to be examined carefully in order to evaluate the minimum feature that can be patterned on the resist and the precision of the patterned geometries.

The distribution of light on the resist during exposure is influenced by optical effects such as light diffraction, as a consequence of which the light energy dose on the resist becomes blurred and leads to limitations in patterning accuracy (Fig. 8.4).

The effect of light diffraction on image blurring is schematically represented in Fig. 8.5. For contact and proximity lithography, image blurring is determined by near-field (Fresnel) diffraction, whereas in projection lithography, far-field (Fraunhofer) diffraction is dominant.

The optical resolution of a projection lithography system can be calculated accounting for diffraction through the Airy

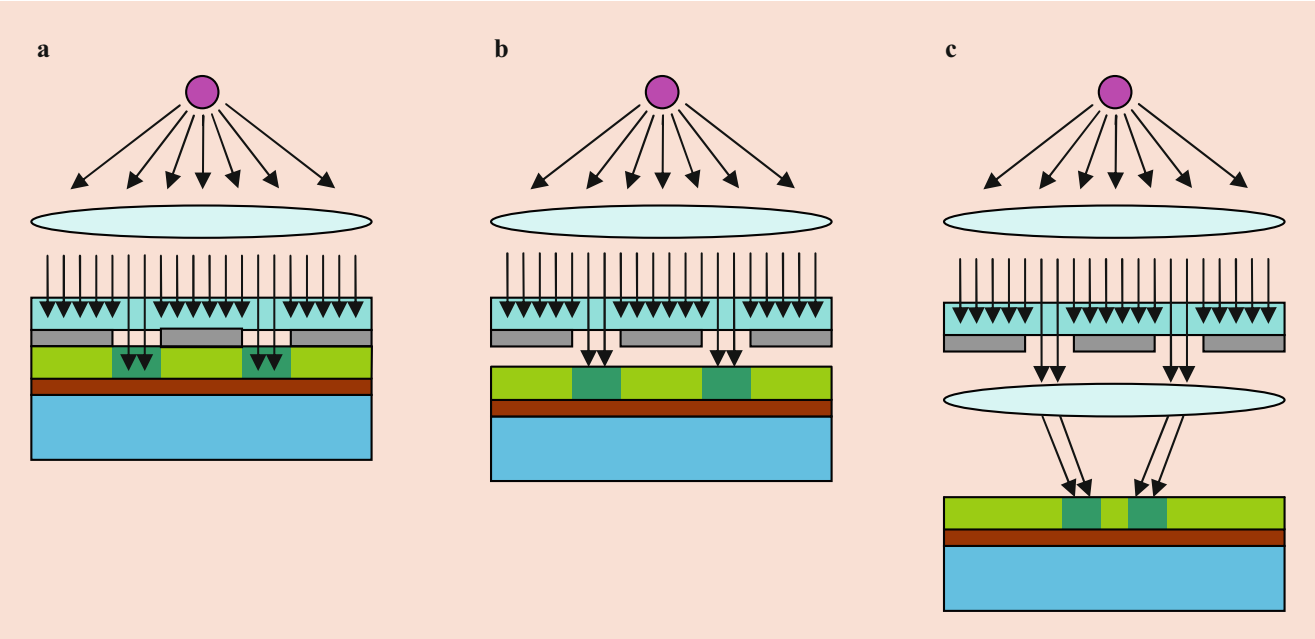

Fig. 8.3 Image formation in contact (**a**), proximity (**b**), and projection (**c**) lithography

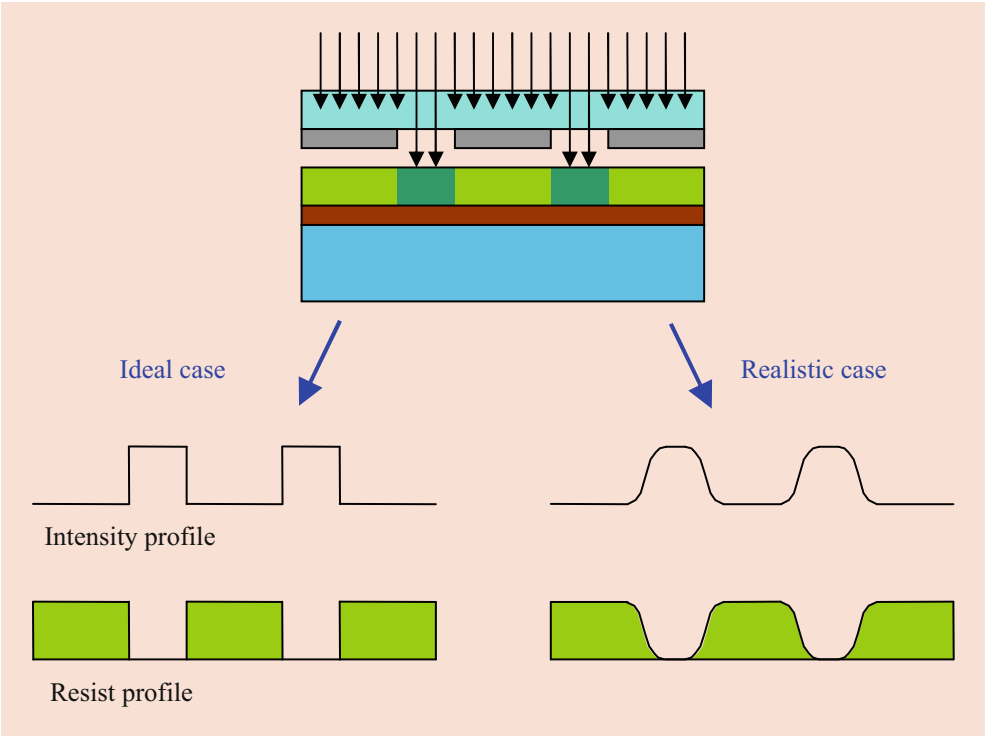

Fig. 8.4 Image and resist profile blurring due to non-ideal effects in lithography

principle, according to which a light point source after projection on the resist plane gives rise to an Airy circular pattern (Fig. 8.6). The diameter of the main lobe of the pattern is 1.22 $\lambda f/d$, with λ light wavelength and f and d focal length and diameter of the focusing lens, respectively.

The size of the Airy diffraction pattern can be taken as a measure to estimate the resolution in projection lithography, according to the Rayleigh principle (Fig. 8.6c). The Rayleigh principle estimates the minimum distance between two point sources (A and B, corresponding to the blue and red traces in

the figure) that can be resolved on the projection plane of the lithographic system as the distance at which the maximum of the Airy pattern generated by point source B is located on the first zero of the Airy pattern generated by point source A.

Through geometrical considerations, it is possible to calculate the resolution on the image plane (R) as:

$$R = 1.22\frac{\lambda f}{d} = 1.22\frac{\lambda f}{n\,(2f\sin\vartheta)} = 0.61\frac{\lambda}{\mathrm{NA}} \tag{8.1}$$

with

$$\mathrm{NA} = n\sin\vartheta \tag{8.2}$$

being n the refraction index of the lens and ϑ half of the acceptance cone angle of the projection system.

The Rayleigh criterion (8.1) can be generalized for lithography by estimating the minimum feature size that can be effectively exposed on the resist layer (MF) as:

$$\mathrm{MF} = k_1\frac{\lambda}{\mathrm{NA}} \tag{8.3}$$

with λ optical wavelength of the light source used in the equipment, NA numerical aperture of the optical projection system, and k_1 a process-dependent parameter.

Equation (8.3) puts into evidence the dependency of the lithographic resolution on the wavelength of the projection system and explains why the need for a continuous im-

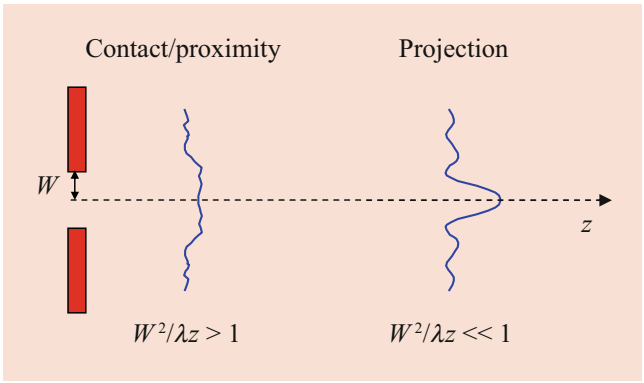

Fig. 8.5 Effect of light diffraction on image formation in lithography

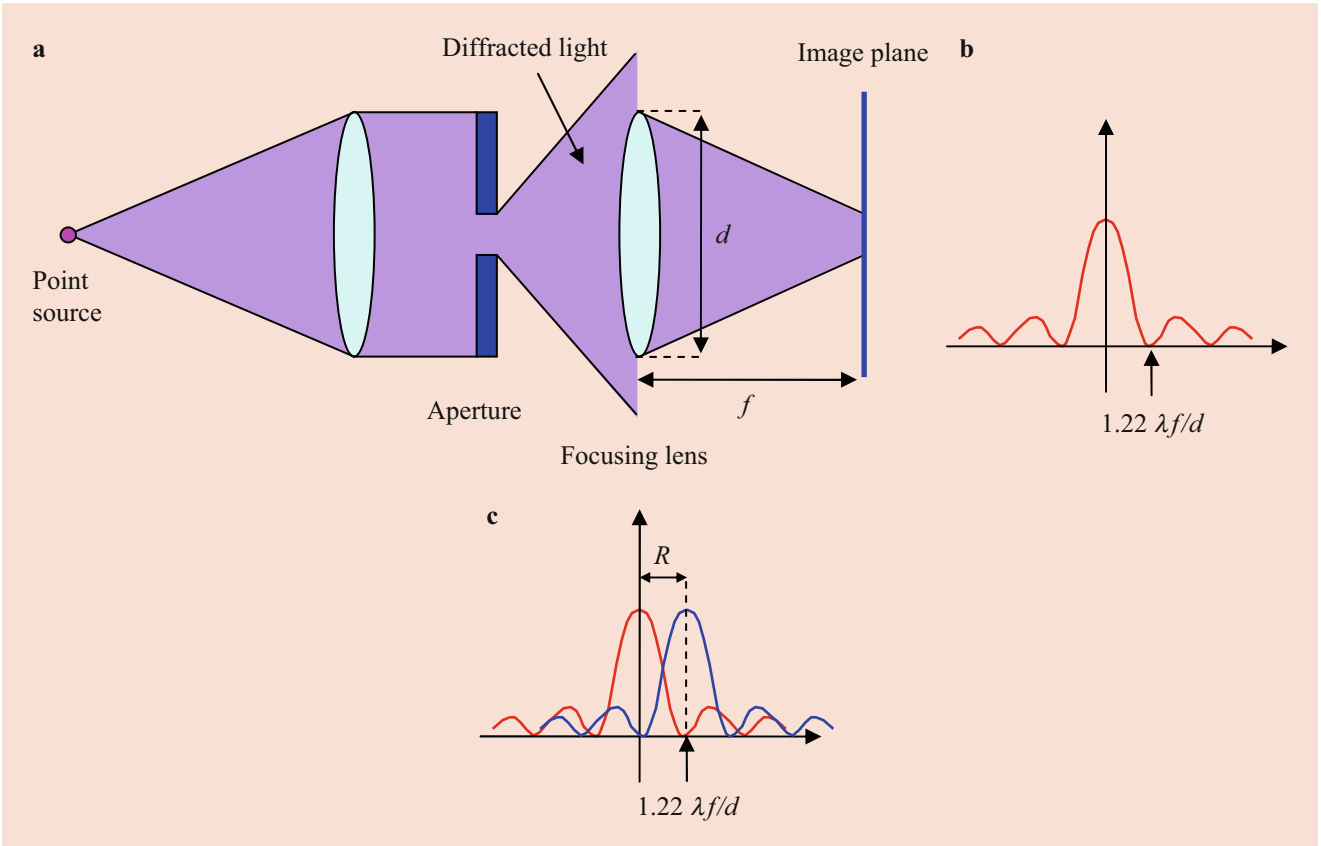

Fig. 8.6 Airy diffraction pattern (**b**) of a light point source (**a**) in projection lithography and Rayleigh resolution criterion for two point sources on the image plane (**c**)

provement of resolution in lithography has determined a constant decrease of the wavelength of the light used for resist exposition over the years and a continuous increase in the NA.

The first lithographic systems used for IC production employed light in the near-UV (NUV) region, produced by Hg lamps. Such lamps were able to emit spectral lines at the wavelengths of 436 (g-line), 405 (h-line), and 365 (i-line) nm, all of which could be used for lithography. Later on, new sources operating in the deep-UV (DUV) region were adopted, with typical wavelengths of 248 and 193 nm. The latest scanners went one step further and are now using a wavelength of about 13 nm, which is commonly referred to as extreme UV (EUV).

Due to the growing throughput requirements of the IC industries, light sources with increasing intensity were desired, in order to decrease the exposure time of the resist and enable the processing of a larger number of wafers per hour (WPH) in the system. Hg lamps were soon considered too weak in intensity for this purpose, and in the next generation of lithography equipment, excimer KrF lasers at 248 nm able to produce DUV radiation with higher intensity were adopted, in order to enhance the process throughput and resolution.

For DUV lithography, fluorine (F_2), krypton fluoride (KrF), and argon fluoride (ArF) lasers, with emission at 157, 248, and 193 nm, respectively, were investigated. Among them, the most successful ones were the KrF and ArF sources, which are still used nowadays for massive IC production in scanner projection systems. KrF-based systems were first utilized for the CMOS 0.25 μm node development and, later on, also adopted for the 0.13 μm node. Subsequently, ArF steppers were preferred to set up the production lines needed for massive IC fabrication with critical lengths of 110, 90, and 65 nm. ArF technology was even pushed beyond and employed in the development of the 45 nm node, thanks to the improvement in numerical aperture of projection systems that proved to be possible with special arrangements such as liquid immersion lithography. At the moment, ArF-based lithography with multiple patterning is the best available option for leading edge lithographic processes down to critical lengths of 22 nm.

As can be seen in Eq. (8.1), the NA of the lithographic system can be an important parameter to enhance resolution, since a better resolution of the lithographic process is expected by increasing the numerical aperture of the projection system. This happens because in a system with high NA, a larger number of diffraction orders are projected on the image plane, increasing the contrast of the pattern image and its intensity.

Considering a lens that is employed in the projection system, its numerical aperture (NA) depends on the index of refraction n of the medium in which the lens operates, according to Eq. (8.2). As can be seen from this formula, a high numerical aperture permits us to exploit a large optical acceptance angle in the optical system. This means that even light rays with relatively large inclination with respect to the lens axis can enter the optical system and contribute to the exposure process. Equation (8.2) also puts into evidence the fact that the numerical aperture of the lens can be readily improved without changing the lens material or design, but simply changing the refraction index of the medium in which the lens operates. In the first projection systems, the equipment operated in air, and consequently the refraction index that had to be used in Eq. (8.2) to calculate the NA was 1.

8.1.2 Resolution Enhancement Techniques

Several resolution enhancement techniques (RET) have been proposed through the years to improve resolution in lithography, such as immersion lithography, off-axis illumination, mask correction methods, and multiple patterning.

Immersion Lithography

In order to improve numerical aperture and take advantage of the term at the denominator of Eq. (8.3), immersion projection lithography was proposed. In this kind of equipment, the projection system is completely filled with an ultrapure liquid, which presents a much higher refraction index than air, such as water. In this way, the image formation of the exposure beam is better, and the resolution of the lithographic process is improved, because the numerical aperture of the system is enhanced according to Eq. (8.2).

In equipment with high NA, such as immersion lithographic systems, another important parameter that has to be considered to evaluate the performance of the process is the depth of focus (DoF). The DoF represents the maximum tolerance of the focal plane distance variation from the mask that can be accepted without appreciable problems on the focusing of the projected image in the resist. This parameter is important because it directly impacts the maximum thickness of the resist film that can be used in the lithographic process and the accuracy required for the wafer placement on the focal plane of the projection system.

Using the Rayleigh principle as in Eq. (8.3), the DoF may be expressed as:

$$\mathrm{DoF} = k_2 \frac{\lambda}{\mathrm{NA}^2} \tag{8.4}$$

in which λ is the operating wavelength of the tool and k_2 an empirical parameter derived from a fit with measured data.

Equation (8.4) shows that the DoF increases linearly with the operation wavelength of the lithographic system and quadratically with the inverse of the NA. Considering the

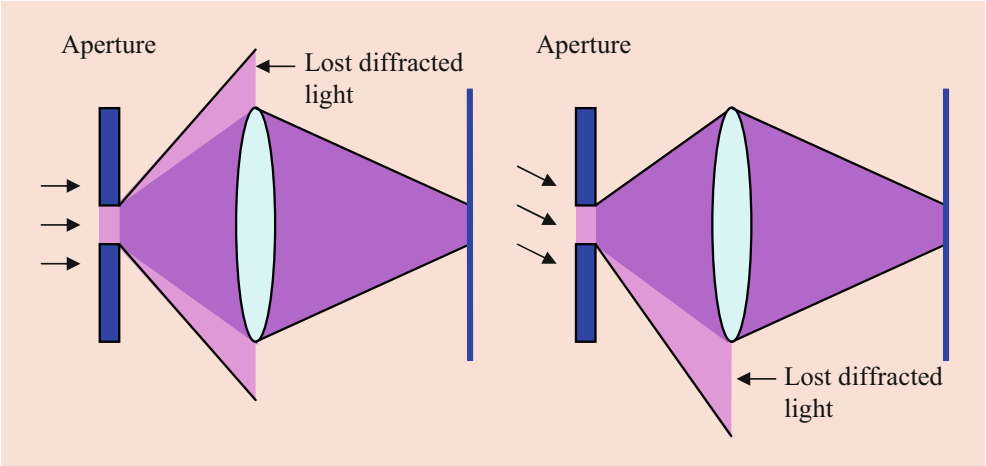

Fig. 8.7 Off-axis illumination principle

trends toward wavelength reduction and numerical aperture enhancement in projection systems to achieve higher resolution, it is worth noticing that both strategies tend to decrease the DoF, leading to more critical requirements on sample planarization, placement, and resist thickness in the process.

Off-Axis Illumination

Off-axis illumination allows to capture higher orders of diffracted light in the projected image, as shown in Fig. 8.7, and consequently improve resolution. Off-axis illumination can be implemented in different ways. Two widely employed techniques are annular and quadrupole off-axis illumination. Quadrupole off-axis illumination is more effective on line/space patterns than on isolated features but is orientation dependent. Annular off-axis illumination is less effective in general but has the advantage of being orientation independent.

Mask Correction Methods

When the patterning performed is in the subwavelength regime, as it happens when using DUV for the production of the more challenging technology nodes, special techniques must be used in order to enhance the masks. One example of RET based on mask correction is optical proximity correction (OPC), which consists of a computer-simulated modification of the mask geometry that can compensate the distortion of the projected pattern coming from the fact that its geometrical dimensions are smaller than the operating wavelength of the lithographic system [1]. Typical examples of these subwavelength pattern transfer effects that may be compensated with OPC are the corner rounding, the shortening of the lines close to their terminations, and the line width changes produced in densely or coarsely patterned areas of the mask.

Another type of RET is the use of phase-shift masks (PSM), a method that can improve the resolution of the pattern by exploiting interference effects induced on the UV light through its transmission across the mask material. In order to obtain this effect, the mask material is designed in such a way that a controllable phase shift can be produced on the transmitted light in different points of the mask, in order to obtain the desired interference effects on the resist [2].

Generally speaking, these mask improvement methods are often named source and mask optimization (SMO) methods, and their scope is obtaining an optimized projected image by modifying the shape of the mask geometries, taking into account the effect of all the diffraction orders collected by the projection system [3]. The final target of these optimization techniques is increasing the process window and improving the resolution of the projected image. Since the diffracted orders of the light source depend on its shape and on the inclination of the laser beam, a joint optimization of the mask geometries and of the source characteristics can be carried out in order to achieve the best result. This joint optimization of the mask and the light source has originated the denomination of the SMO methods. Due to the complexity of task, such optimizations are normally performed by running specific algorithms with a computer routine.

Beyond the modification of the mask geometries, RET techniques may also involve the introduction in the mask of additional features beyond those necessary for the design of the IC that are again used to compensate the negative influence of diffraction effects on image formation. This is particularly important when the mask includes sparse pattern on which the effect of light diffraction may be more difficult to compensate compared to dense patterns. Such additional features that are introduced are not meant to be reproduced on the projected image but are only used for compensation of the diffraction effects on the sparse pattern. They are named sub-

resolution assist features (SRAF) because they are normally designed with a size that is smaller than the resolution of the process. Peculiar examples of SRAFs are scattering bars and inverse scattering bars [4].

Multiple Patterning
When all the other RET techniques fail, multiple patterning can be applied to scale the feature size of lithography below the intrinsic limitations of the process. Different multiple patterning methods exist, and all of them involve the execution of more than one lithographic step, sometimes in combination with other additional processes. A more extended discussion of multiple patterning can be found in the next section devoted to ArF lithography.

8.2 Advanced Lithography Based on ArF 193 nm DUV Sources

In equipment based on ArF laser sources, the NA has been increased through the adoption of water immersion technology from 0.6 to 1.35. The development of the immersion lithography technique allowed to push the application of ArF 193 nm systems to the manufacturing of ICs with critical length scaled down to 45 nm.

Given the negative impact on the DoF that derives from the enhancement of NA, as discussed before, the resist thickness in high-NA ArF projection systems is severely limited, and consequently the resist selectivity to plasma etching processes becomes critical. Moreover, liquid immersion lithography also leads to other special requirements for the process, for instance, the need to develop photoresists that can be utilized in water or in another liquid environment, since all the projection system (including the wafer) needs to be immersed in the same liquid in order to operate correctly.

8.2.1 Resist Thickness and Plasma Etching Selectivity

The very small DoF dictated by the short wavelength and the high numerical aperture of the 193 nm immersion systems and the constraints that derive from the maximum aspect ratio of the resist pattern on the critical features pose severe limitations on the resist thickness in these processes. For example, for the 45 nm IC fabrication node, the maximum possible resist thickness is around 150 nm and is expected to decrease in next-generation technologies.

The main problem with the use of very thin resist layers, which is quite common in advanced lithographic methods, is the poor resistance of the resist layers to the plasma etching processes that are normally carried out after resist development in order to transfer the pattern to the material of interest located under the resist mask (see Fig. 8.1), which in CMOS technology is often silicon or silicon oxide. Besides thickness, the resist chemical composition can also have an impact on its plasma etching resistance.

The resistance of the resist layer to plasma etching processes is normally estimated by determining the etching selectivity of the target material with respect to the photoresist, which is calculated as the ratio between the target material etch rate and one of the photoresists in the same process. If the selectivity is high, the process etches the resist slowly compared to the target material.

To give an example, in a CF_4 plasma process used to etch SiO_2 that presents a rate of 100 nm/min on SiO_2 and 50 nm/min on the resist layer, the selectivity of the etch process toward photoresist is estimated to be 2. The calculation of the selectivity provides a quick measure to estimate the maximum possible depth that can be obtained with the etching process when a resist layer is used as a mask for it, since, for instance, with a selectivity of 2, a resist layer that is at least as thick as one half of the target etching depth will be necessary. If the plasma etching selectivity on resist is high, a thin mask layer can be used for etching a relatively large thickness of the material of interest.

Quite reasonably, the selectivity depends on the characteristics of the plasma etching process adopted and on the material properties of the photoresist layer utilized but, excluding second-order effects, not on its thickness. Since the characteristics of photoresists are specifically designed to give a satisfactory yield in lithographic processes performed at a specific wavelength, it is natural that the composition and consequently the material properties of resist layers developed for different exposition wavelengths may differ. Comparing, for instance, the etching rate in typical plasma etching chemistries used in IC technology (CF_4, Cl_2, HBr, Ar), the photoresist materials used for the 248 and 193 nm technologies show a different behavior, with the 193 nm photoresists providing significantly lower selectivity in these etching processes.

An empirical model has been developed to evaluate the plasma etch rate of photoresist depending on its chemical composition through the Ohnishi parameter P_O, defined as [5]:

$$P_O = \frac{N}{N_C - N_O} \tag{8.5}$$

In the formula, N is the total volume density of atoms in the polymer, whereas N_C and N_O are the volume densities of carbon and oxygen atoms, respectively.

In photoresists, the etching rate in plasmas is roughly proportional to the Ohnishi parameter, so a high P_O is generally associated with a poor selectivity of the etching process toward the resist. This happens because the etch rate in polymers consequent to ion bombardment (which is the main

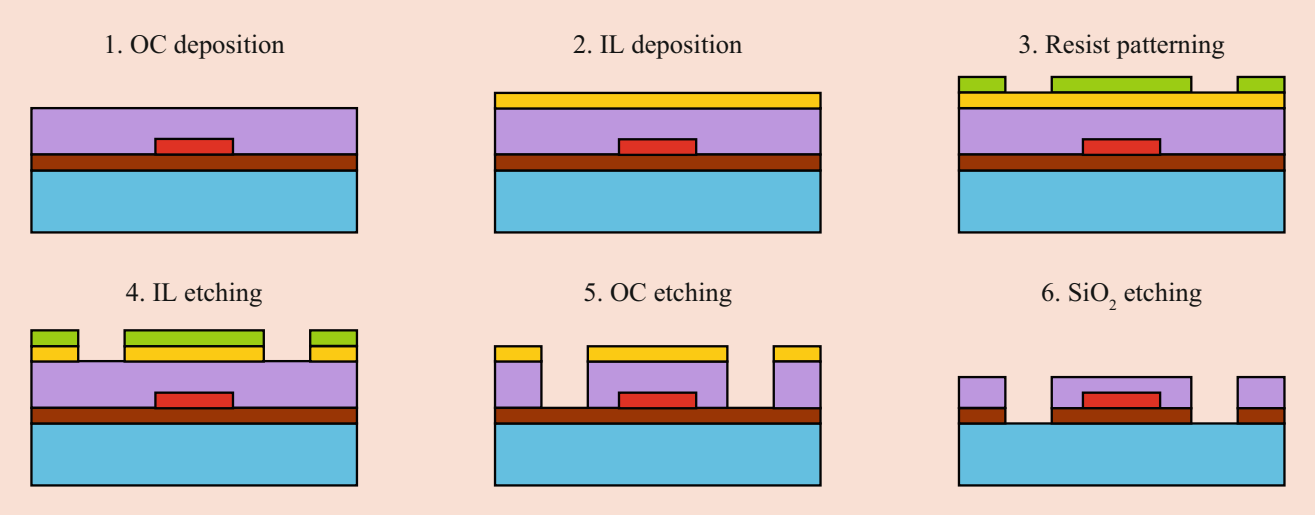

Fig. 8.8 Lithographic patterning procedure based on hard masking

reason for resist etching in plasmas in which ion sputtering is always present) depends on the concentration of C-O groups in the polymer. Polymers containing a high concentration of such groups present a sputter etch rate that is much higher than carbon, because of the presence of oxygen atoms bound to carbon in the material. That is the reason why the Ohnishi parameter reports at the denominator the difference between the carbon and oxygen atom concentrations in the material, since this represents the effective carbon content related to its sputter etching resistance.

In order to increase the effective carbon content of resist layers after development and increase their resistance to plasma etching, peculiar curing processes have been developed, such as the exposition of the patterned photoresist to an HBr plasma before etching. Such kinds of plasma produce an UV light in vacuum that is able to suppress the lactone and ester groups in the resist, increasing its carbon content and consequently reducing the Ohnishi parameter. Another benefit of these treatments comes from the fact that the chemical groups that are removed from the resist by the UV light irradiation in vacuum tend to become volatile in the plasma and redeposit on the resist pattern as graphitic residues. Such residues are deposited on both the horizontal and the lateral surfaces of the patterned resist and consequently increase the resistance of the lateral walls of the pattern to the plasma, helping maintain the critical feature size during etching.

As the shrinking of the critical dimensions of ICs proceeded in history, the methods used to increase the etching selectivity proved to be insufficient to keep using the plain photoresist layer as a mask, and, from a certain point onward, the technique of hard masking was adopted with increasing frequency. Hard masking consists in using a multiple mask composed by overlapped layers, in which the top mask layer is composed by photoresist, as in the traditional soft masking procedure, whereas the layers underneath are used because they provide a higher selectivity than resist in the plasma process that has to be subsequently adopted for the pattern transfer on the material of interest.

The most common hard masking strategy employs alternated organic and inorganic layers within the mask stack, as shown in Fig. 8.8, in which a sample hard masking process for patterning of a SiO_2 layer on a non-planar wafer is schematically illustrated. First the wafer is covered with an organic coating (OC) that is generally thicker than the photoresist layer used for the lithography and can be also used for planarization, improving the focus budget. Afterward, a thin inorganic layer (IL) is deposited on top of the OC, and finally the photoresist is spun and patterned as the third layer of the stack. The function of the inorganic layer, which is typically a silicon-rich material, is to increase the etching selectivity of the mask, providing a better resistance to the plasma etching.

Since it is also used to reduce the reflection of the light during resist exposure, such IL is often named Si-ARC (silicon containing anti-reflective coating). The OC, which is sometimes named OPL (organic planarizing layer), is typically a carbon-rich layer with high plasma etching resistance that can be deposited by spin-On or PECVD technique.

After resist patterning on the top of the stack (step 3 in the figure), the pattern is transferred to the inorganic layer underneath by a highly selective plasma process, such as a fluorine-based plasma, and subsequently to the OC by oxygen- or hydrogen-based plasmas. This technique permits to reach a higher overall selectivity with respect to the application of a plain resist mask because oxygen or hydrogen plasmas have a very slow etch rate on inorganic materials and consequently permit to etch a relatively thick OC without completely consuming the upper IL, on which the pattern is transferred with the first etching step.

On the other hand, the high selectivity of the OC etching process on the IL allows to reduce its thickness, avoiding selectivity problems on the resist with the fluorine-based plasma that is utilized to pattern the IL. Thanks to the much higher overall thickness obtained with the hard mask, and to the slow etch rate the plasmas used for SiO_2 or Si etching on the OC, the pattern can be successfully transferred to the target materials even using very thin resist layers, without major etching selectivity issues.

Immersion lithography with hard mask technology has been utilized for the 80 and 40 nm IC nodes, in which the critical feature size is much below the 193 nm wavelength of the radiation used, but any further shrinking of the pattern dimensions by direct improvement of the resolution of the lithographic equipment seems to be economically impractical, nowadays. For this reason, in order to satisfy the always growing demand for more scaled ICs, alternative solutions have been investigated to decrease the critical size of the pattern without further improving the resolution of the lithographic systems.

8.2.2 Multiple Patterning Techniques in ArF DUV Lithography

One of these techniques is double patterning (DP), which has also been applied to improve the resolution of ArF DUV lithography and is based on the multiple exposure of the resist using two or more patterning procedures that are performed subsequently and with a controlled offset [6–10]. These multiple exposures of the resist are followed by one or more anisotropic etching steps that are used to aid the definition of the differential pattern and transfer it to the wafer. This technique has been fundamental for the development of the 32 and 22 nm IC technology nodes in recent years.

Several techniques can be used to implement the double patterning technology. In the lithography-etch-lithography-etch (LELE) approach, for instance, the resist is exposed twice using a controlled overlay between the two exposure/etch procedures in order to obtain the minimum feature by the partial overlap of two patterns that, individually, present a larger critical size. The LELE approach has been used to extend the application of ArF DUV immersion lithography to the 32 nm technological node.

DP is nowadays the only commercial technology that allows to pattern a critical length of 40 nm. The LELE DP starts by creating a first pattern with a pitch that is approximately twice the final one. After transferring this pattern to an intermediate hard mask layer by plasma etching, a second lithographic step is carried out over the already etched mask layer, using a proper shift of the new pattern with respect to the former one, in order to obtain the critical length desired by the overlap of the two patterned geometries, each characterized by a larger pitch (Fig. 8.9). A cheaper process with only one lithography step, similar to the one represented in Fig. 8.10, may be adopted to reduce the feature size with an isotropic etching, obtaining an improvement on the line width without scaling the line distance. This technique presents the big advantage of being implementable with already established lithographic processes, without any modification of the available equipment, and was utilized to demonstrate the possibility to obtain a 32 nm half-pitch resolution in laboratory tests.

Another option for DP is the self-aligned double patterning (SADP), which is essentially a spacer technology. With this method, a so-called mandrel pattern is first transferred onto the photoresist or onto a hard mask under it; subsequently, a spacer layer (SL) is deposited over it with a conformal deposition method (a method that maintains a homogeneous thickness of the layer independent of the inclination of the deposition surface). After deposition, the SL is etched back maskless to remove it from the horizontal surfaces of the mandrel pattern, leaving spacers on its vertical sidewalls, and the patterned resist or OC is etched selectively, in such a way that the spacers remain on the wafer and can be used as a hard mask to etch small lines on the substrate (Fig. 8.10). With this method, the width of the critical feature does not depend directly on the photoresist patterning resolution, since it is determined by the thickness of the SL.

Different than the LELE method, the spacer technique requires additional processing steps besides the exposure and the development of the resist, since it relies on the deposition of a conformal mask layer on a previous pattern, with specific processing steps such as the SL etchback that are not foreseen in conventional patterning procedures (SiO_2 and SiN_x are often used as spacer layers). The spacer technology or SADP has been widely applied in the fabrication of FinFET devices. Other possible multiple patterning technologies that are even more sophisticated involve the use of SADP twice to increase the density of critical size structures. Such techniques are named self-aligned quadruple patterning (SAQP).

Despite the impressive results reported in recent research works, the industrial implementation of robust SADP or SAQP processes based on ArF DUV lithography presents a number of technical challenges. Most of the problems that are encountered in these techniques are related to the integrity of the spacers during the process. Spacers are generally thin structures with rather high aspect ratio and consequently present a limited mechanical strength. On the other hand, the outcome of the process can be good only in case the spacers are maintained intact and as vertical as possible until the completion of the etching steps in which they are used as hard mask lines.

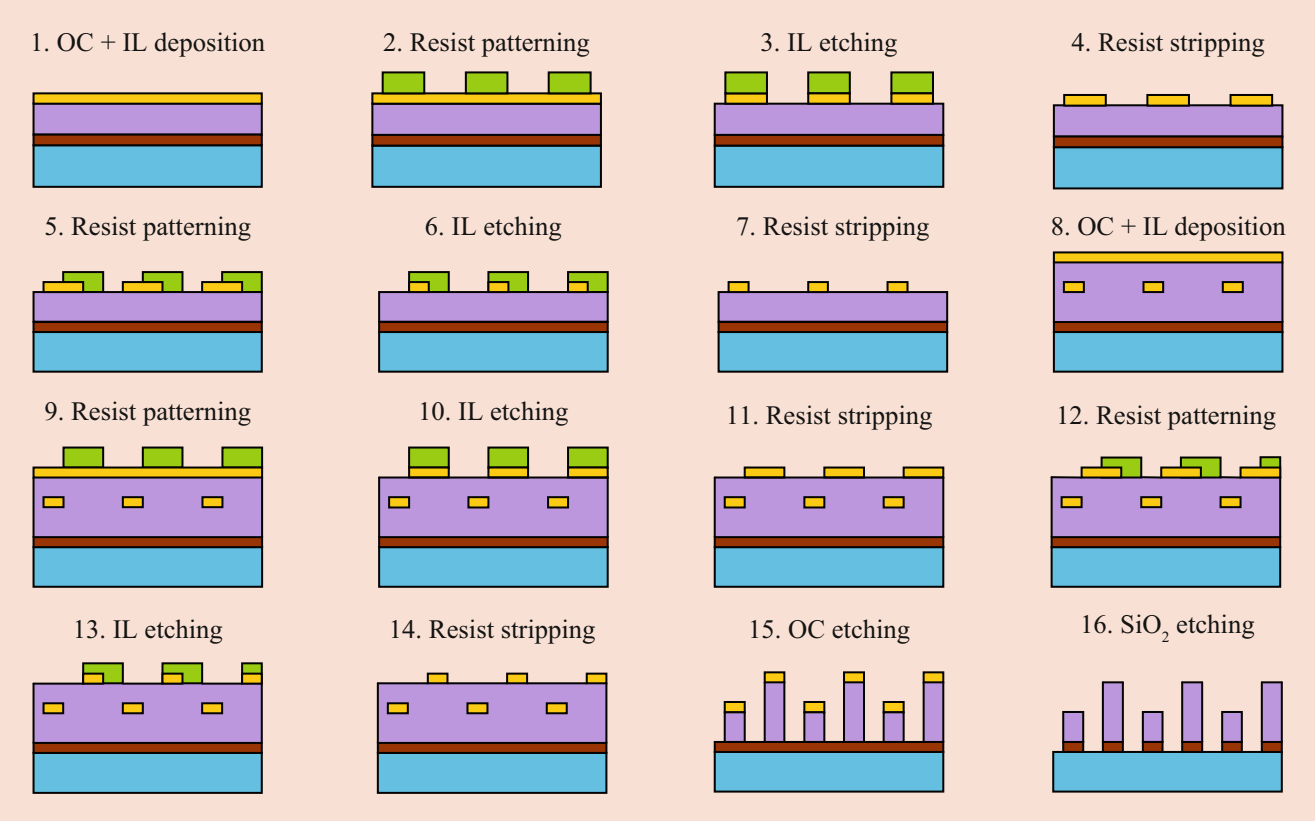

Fig. 8.9 Example of LELE lithographic procedure for full half-pitch resolution doubling

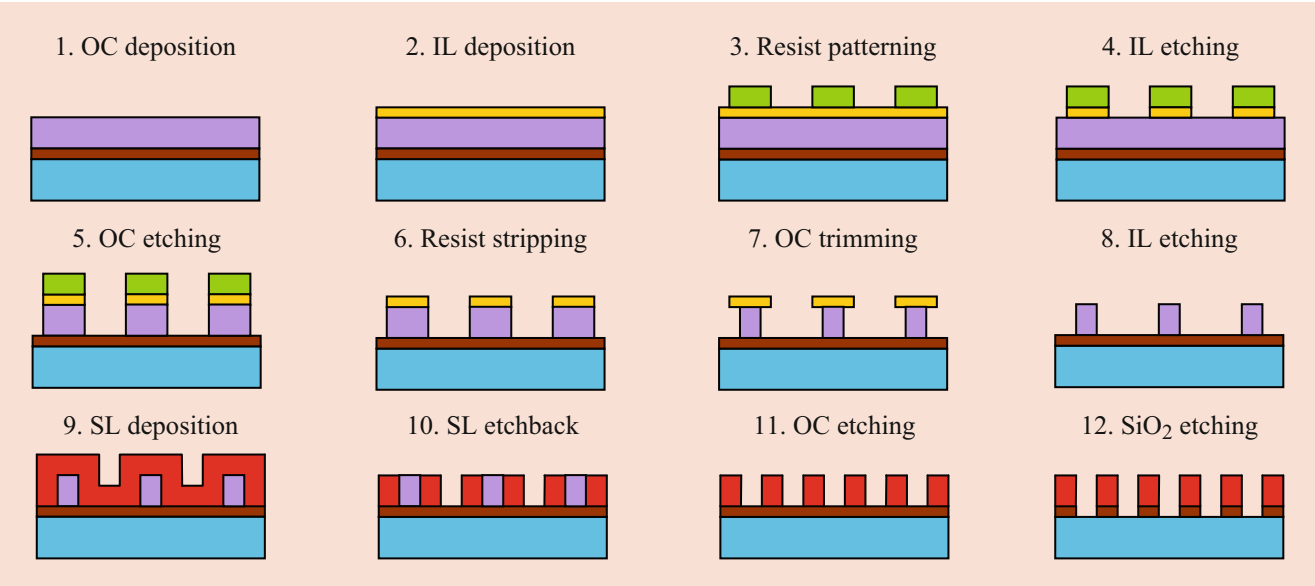

Fig. 8.10 Example of SADP lithographic procedure for full half-pitch resolution doubling

A possible source of damage for spacers are the capillary forces that develop during the various wet cleaning steps needed during the pattern transfer procedures in IC fabrication. In particular, the capillary forces on the two sides of the spacers may not be well compensated in case the pattern is not symmetrical, giving rise to lateral forces that may

bend or break the spacers. Since the intensity of the resulting bending moment that the capillary forces may produce on the pattern depends on the cube of the aspect ratio of the spacers, such forces may easily exceed the yield strength of the spacer material and induce a plastic pattern deformation (pattern collapse) that is not beneficial for the process yield.

The materials that are more often used in SADP processes to realize the spacers are SiN_x or SiO_2 layers deposited at low temperatures on a photoresist or an OC mandrel pattern. When plain photoresist or other organic layers are used for the mandrel, their removal can be simply performed with an O_2 plasma, which is a dry procedure and consequently does not lead to problems related to capillary forces. However, in some cases, an inorganic Si-ARC layer is also used, whose removal may require additional steps. Evidently, when the line width resolution of the patterning process goes below 20 nm, high aspect ratio spacer structures are inevitably necessary to sustain the subsequent pattern transfer by plasma etching as hard masks. Such high aspect ratio structures are unfortunately prone to pattern collapse problems. The presence of the IL is often critical in this respect, since in OC patterns with 20 nm resolution, it has to be removed by wet HF dips, in which capillary forces are developed. As a rule of thumb, wet cleaning procedures should not be applied to patterns with aspect ratio larger than 5.

Other pattern deformation phenomena in SADP processes may appear as a consequence of the residual stress of the material deposited on the mandrel in order to create the spacers. Residual mechanical stress is present in principle in any deposited layer and results in a tendency of the layer to expand or contract more than the underlying substrate after the deposition process, developing a fixed tensile or compressive strain that remains in the film after the growth is completed. Since, while the film grows during deposition, such strain may change in value, a strain gradient may also develop along the film thickness direction, which naturally produces a bending when the layer is released from the substrate.

For the case of the spacers, the residual strain gradient of the film that may be present on the vertical parts of the pattern is particularly dangerous, because it may bend the spacers like capillary forces do during the wet cleaning procedures. The phenomenon of spacer deformation that is purely due to residual strain effects on the deposited spacer material is named wiggling [7]. Young's modulus of the material, besides the residual strain, also plays a role in wiggling, since more rigid materials (such as SiN) tend to bend less when subjected to strain gradients than more slender materials characterized by a lower stiffness (such as SiO_2). In this case also, the presence of a large aspect ratio makes the problem of wiggling more critical, and possible strain changes induced by the chemical processes performed on the spacers during the patterning procedure may more easily affect the final result. Typically, relevant wiggling problems are observed for spacer aspect ratios larger than 7.

Although, in theory, the capabilities of ArF technology with multiple patterning in terms of resolution may be further improved, the fact that additional processes are needed in these methods increases the cost of ownership of the corresponding production lines and makes the economical viability of the technology questionable. Since the cost of these complicated patterning flows mainly depends on the number of process steps involved, new materials have been studied in order to decrease the additional etching or deposition steps needed.

In [8], the cost of several SADP and SAQP processes with critical size scaled down to 5 nm was compared, considering that the number of steps and consequently the process cost generally increase with the downscaling. Since, however, the density of transistors that can be fabricated in the process also increases with the reduction of the critical size, a significant figure to make a sound cost comparison of processes with different scaling level is the cost per transistor, simply calculated dividing the process cost per wafer by the number of transistors that can be fabricated on a single substrate. By calculating such figure, it is found, for instance, that a reduction of the cost per transistor of a factor of 0.71 can be obtained by shifting from the 14 nm to the 10 nm node, whereas from 14 nm to 7 nm, the cost reduction factor is only 0.86. A cost reduction factor higher than 0.8 may be insufficient to motivate the setup of the 5 nm node in massive IC production. For this reason, alternative solutions for the technological generations with critical feature scaling beyond 14 nm are presently under investigation.

8.2.3 Photoresists for 193 nm DUV Lithography

Since photoresist is essentially a material whose solubility in a developer may be enhanced (positive resist) or suppressed (negative resist) by the exposure to an optical or ionizing radiation, the core subject of the development of new photoresist materials is the sequence of chemical reactions initiated by their exposition to a specific type of radiation. As discussed before for the case of optical lithography, different radiation wavelengths have been utilized through the years, with a constant trend toward the use of shorter wavelengths to improve the resolution of the patterning and meet the market demands in terms of scaling of the IC critical size. Independent of the utilized wavelength, the exposure dose required to complete the chemical reactions that are needed to change the resist solubility is always a critical parameter for the throughput of the process measured in number of processed wafer per hour (WPH). Consequently, the irradiation dose of the resist

must be sufficiently low, or, equivalently, the sensitivity of the resist to the light exposure needs to be high enough to allow a short exposure time.

In order to cope with these demanding sensitivity requirements, the development of the resist for the 193 nm wavelength was carried out from the beginning as an extension of the chemically amplified photoresists already developed for the former 248 nm technology. Given that the first ArF exposure systems were similar to the KrF one used until then, the initial challenge for the development of the new photoresists was the need to find a material that could extend to shorter wavelengths the same properties that had been exploited in the phenolic and styrene-acrylate polymers used in the chemically amplified resists (CARs) for the 248 nm lithography.

In these resists, the chemical amplification mechanism was introduced in order to decrease the exposure dose needed and improve the throughput of the lithographic process. Chemical amplification relies on the action of a photoactive molecule that is able to generate a catalyzer for a dissociation reaction in the polymer. Onium salts are a typical example of such molecules. They are added to polymers like polyhydroxystyrene (PHS) that are normally insoluble in water-based developers. Under UV irradiation, the onium salt molecules can interact with a single photon and undergo a dissociation reaction that generates an acid. Such acid molecule acts as a catalyzer of another reaction that is able to modify the structures of the polymer chain, usually removing a molecule group that makes it insoluble in the developer. Since the photon-generated acid molecule is a catalyzer, it is not consumed by the reaction involving the modification of an individual polymer chain and can catalyze a large number of similar reactions in sequence.

These reactions that modify the chain of the polymer making it soluble in the resist developer are often promoted by a high-temperature treatment of the resist that takes place after exposure, which is named post-exposure bake (PEB). Since a single acid molecule generated by the interaction of a photon with the onium salt can catalyze the chemical modification of a large number of polymer chains, it is easy to understand why this type of photon-induced modification of the resist was denominated chemical amplification, since the action of the irradiating photons is amplified by the chemical reaction catalyzed by the acid molecule. The amplification factor of such resists is sometimes calculated by estimating how many groups can be detached from the polymer chain by an individual molecule of catalyzing acid. This factor can exceed 100 in typical CARs. Thanks to the chemical amplification, the new resists developed for the DUV systems were able to work with very low irradiation doses, in the range 10–50 mJ/cm^2, with large benefits on the throughput of the lithographic processes. The chemically amplified resists were also more transparent to the UV radiation compared with the resists that were used with NUV light, generally based on novolak resins. In this way, a better profile of the resist pattern owing to a more uniform irradiation of the layer along its thickness was possible.

During the development of the resists for the new DUV wavelength, the advancement of the equipment was also considered. The first ArF equipment, in fact, operated in air just like the KrF ones used before ("dry" lithography), whereas, later on, in order to improve the numerical aperture and consequently the resolution, water immersion systems were built, in which the space between the last lens of the projection system and the wafer surface was filled with water to increase the refraction index of the environment ("immersion" lithography). Immersion lithography combined with multiple patterning techniques was able to push the application of ArF systems up to scaling levels that were not expected at the beginning of the development of the technology. Considering the differences in the chemical environment and the pattern transfer procedures involved in all these different patterning methods, it is easy to understand how deep the impact of the compatibility with these requirements was on the resist material development.

In order to cope with all the requirements of dry and immersion ArF lithography, including SADP methods, the resist material should ideally:

- Enable the completion of the lithographic procedure with a single layer of material, to limit fabrication costs and keep the process simple.
- Provide high exposure sensitivity and, at the same time, the possibility to obtain vertical pattern profiles after development.
- Assure sufficient adhesion on all the materials of interest for patterning.
- Be thermally curable beyond its glass temperature transition (T_g) in order to provide good etching selectivity after annealing.
- Comply with an exposure dose between 10 and 50 mJ/cm^2.
- Provide a high selectivity to typical SiO_2 and metal plasma etching processes (such as CF_4/O_2 or Cl_2/BCl_3 plasmas).
- Be compatible with the use of standard industrial tetramethylammonium hydroxide (TMAH)-based developers.

The initial investigations about the possible compatibility of 248 nm CARs with shorter wavelengths immediately put into evidence that phenolic polymers were too much absorbing at 193 nm to be used as resist layers, whereas polyacrylate polymers were almost transparent in that range, showing good promises for the application. The first resist technology for ArF light, indeed, was developed at the IBM laboratories and was based on a polymer containing the methyl methacrylate (MMA), t-butyl methacrylate (TBMA),

and methacrylic acid (MAA) monomers in the chain [11]. The resist allowed the creation of positive patterns by means of an acid-catalyzed reaction removing t-butyl groups in the material to create carboxylic acid and showed good compatibility with mixing with acid-generating compounds, fair adhesion to the substrate, and high glass transition temperature. However, some drawbacks were also present, since the resist layer after development presented a rather high oxygen content that decreased its selectivity toward plasma etching and was not compatible with TMAH developing solutions with the standard concentration of 0.26 N, because it required a much higher dilution to work well (0.02 N).

Some improvements were introduced in the next-generation resists, by including alicyclic groups in the polymer to enhance its dry etching resistance, thanks to the presence of carbon atoms in the ring structure of these molecules, according to the Ohnishi principle discussed earlier. Being non-aromatic, alicyclic groups also provided high optical transparency at 193 nm, which was another attractive property for lithography. Another approach followed to improve the plasma etch resistance of the resist was the introduction in the polymer backbone of alicyclic moieties as inert side chain groups.

The only drawback related to the inclusion of alicyclic groups in the resist was the fact that, in high concentration, they increased the hydrophobicity of the material making the development procedure in aqueous solutions (such as the standard alkaline developers) difficult. This problem was addressed including polar groups in the chain and additional methacrylate monomers that were able to solve the development problems in aqueous solutions and achieve the desired compatibility with the 0.26 N developer solutions based on TMAH. The resulting photoresist materials showed good substrate adhesion, T_g larger than 200 °C, and minimum swelling during development, also thanks to the reduced amount of carboxylic acid included in the mixture.

After scaling of the critical size below 100 nm, immersion projection had to be adopted to improve resolution. Ultrapure water was the liquid of choice, providing a refraction index of 1.44 and a very low absorption coefficient at 193 nm. The use of the commercially available CA resist previously developed for 193 dry lithography was the first challenge that had to be faced since the exposition to the water environment could produce undesired effects, such as the dissolution of resist components in aqueous solution, water incorporation in the film, and generation of bubbles that may reflect the UV light because of outgassing from the resist during exposure. These problems were addressed through two main complementary strategies: the development of protective coatings that could be used during resist exposure and the addition of chemical compounds to the resist mixture in order to improve its usability in water.

The coating materials had the main function of preventing in- or out-diffusion of components from the water environment to the resist film and vice versa. The first compositions of such films, which had to be insoluble in water, could only be removed with organic solvents after use, and this was a disadvantage because it required the introduction of additional steps in the patterning process compared to dry lithography. For this reason, a second generation of protective coatings that were soluble in the standard TMAH aqueous solutions was developed. Different chemical compositions of the coating material were utilized, often containing hydrocarbon, fluorocarbon, and organosilicon functional groups in the chain. Among them, acrylic polymers containing fluoroalcoholic groups that had been previously developed as CA resists for F_2 157 nm lithography were particularly successful because they were very transparent at 193 nm and able to provide a very good wettability of most of the mainly used 193 nm photoresists. In general, the main challenge in using protective coatings during immersion lithography was the need to minimize the defect density induced by the additional processing steps needed for the application of the coating and to limit the possible undesired effects during exposition that may affect the subsequent processing steps, such as the formation of post-development skin layers or residual water droplets after exposure.

A possible way to completely avoid such problems consisted of developing new materials that could be directly utilized in water as photoresist layers, without the adoption of any protective coating. The possibility to avoid the additional processing steps required by the application of the protective layers also represented an important driving force for the achievement of this target. However, the initial strategy of introducing hydrophobic monomers in the resist (such as fluorinated alicyclic-based monomers) to reduce its interaction with water and change the acid precursors in such a way that the generated acid products after irradiation were not soluble in water proved to be very challenging. Consequently, a different strategy was preferred in the end, which consisted of adding to the resist mixture some components that may work as in situ self-assembling coatings. The additives used for this purpose were chosen in order to present a lower surface energy than the other components of the mixture and consequently be able to reach a higher concentration on the top surface of the resist layer after spin coating. Such high concentration at the surface of the layer played the role of a protective coating, without the need of any additional deposition steps and with no interface problems, different than the specific coating layers described before.

Among the possible additive formulations, organosilicon- and fluorine-containing polymers were explored, in which low surface energy groups were introduced either in the backbone or in the side chain of the polymer. These mate-

rials were often composed by a polymethacrylate backbone in which silicon- and fluorine-containing additional groups were introduced. Another important aspect was the fact that the self-assembled protective layer had to be easily soluble in the development solution, since possible solubility problems may lead to the creation of surface roughness and defects in the resist after development. The needed solubility in the top part of these photoresists was achieved by adding some non-polar labile acid groups in the chemical formulation of the additive material, in such a way that during exposure and subsequent PEB, the acid-catalyzed deprotection reactions could take place simultaneously in the upper and lower parts of the layer assuring a complete dissolution of the material in the developer solution without creating significant defects. The successful creation of water-compatible photoresist layers incorporating such in situ assembled protective coatings was the key solution to return to the cost-effective single layer resist strategy that was initially developed for the dry processes also in immersion lithography.

Since after scaling to the 22 nm node, multiple patterning techniques such as LELE or SADP had to be adopted to cope with the new resolution requirements, new specifications for the photoresist performance became necessary. The first double patterning technique employed was conceived in order to keep the established processes as much as possible unmodified in the patterning technology. This was possible with a simple double exposure procedure, in which two photoresist layers were exposed subsequently after an intermediate etching step in order to achieve the desired resolution with a controlled shift between the two patterns. In this way, the requirements about the resolution of the two individual patterning procedures could be less demanding, and consequently an established patterning process was expected to be applicable to each of them, with no major modifications introduced in the photoresist composition or in the photolithographic process. From the development of the first plants for the 22 nm node onward, different double exposure processes have been proposed [12, 13].

One of the possible implementations of DP was the LELE approach in which two subsequent lithographic patterning and etching processes with subcritical resolution are performed to etch the critical feature. This approach was adopted rapidly because it could basically use standard approaches for all the processing steps and did not require any modifications of the materials and procedures used for its implementation. Possible variants of the LELE process are the litho-litho-etch (LLE) process, in which the patterning of the second resist layer is made over the first one without any etching process in between [14], and the litho-freeze-litho-etch (LFLE) process, in which after patterning the first resist layer, a chemical procedure name "chemical freezing" is carried out, which induces additional cross-linking of the first resist layer in order to make it insoluble in the solvent utilized in the second resist spinning and improve the yield of the process [15, 16].

Compared to LELE and its variants, the self-aligned double patterning (SADP) technique discussed before provided more advanced performances in terms of scaling and density of the pattern [17]. In this case, after realizing a first patterning on the resist layer, an inorganic coating has to be deposited in order to create spacers on the side of the pattern features that are used for the final patterning. However, the implementation of the SADP is more problematic for the compatibility issues related to the deposition of the inorganic layer on the resist, the polishing process, and the resist removal.

8.3 Non-optical Lithographic Methods

There are also lithographic techniques that are not based on optical exposure, such as electron beam lithography (EBL) and nanoimprint lithography (NIL).

8.3.1 Electron Beam Lithography

Besides UV light, electron beams have also been utilized for resist patterning in electron beam lithography (EBL). The main advantage of EBL is the fact that the wavelength associated with the electrons of the beam (whose energy is typically in the range 10–100 keV) is very short and consequently a high resolution can potentially be obtained, as predicted by Eq. (8.1).

However, EBL is essentially a direct writing method, in which the beam must be scanned from point to point on all the patterns that have to be transferred to the resist, and consequently is basically a slow process that cannot cope with the throughput requirements of modern plants for IC mass production. For this reason, EBL has been so far mainly utilized for the fabrication of the masks used in optical projection systems rather than for the direct pattern transfer on the wafers.

Resists for EBL are different than UV photoresists because they must be sensitive to electron irradiation rather than to light exposure. Electron-sensitive resists with positive and negative tone have been developed, which is important to decrease the e-beam writing time when realizing DUV masks, depending on the density of the clear and dark areas required on them. In these materials, for example, poly(methyl methacrylate) (PMMA), EBR-9 (an acrylate-based resist), PBS (poly(butene-1 sulfone)), and ZEP (a copolymer of chloromethacrylate and methylstyrene), the resist sensitivity to the electron irradiation, related to the exposure time, and the contrast obtained on the pattern, related to the resolution,

are key and sometimes competing properties that have to be tuned for the specific application.

However, although EBL was newly included in the ITRS roadmap as a possible alternative for the implementation of the 32 nm technological generation [18, 19], as the cost of 193 nm UV equipment increased sharply with the progressive decrease of the critical size, the recent advent of extreme ultraviolet lithography (EUVL) has terminated all the efforts toward EBL for IC production.

8.3.2 Nanoimprint Lithography

Nanoimprint lithography (NIL) is actually a molding technique that is employed to pattern the resist by the mechanical action of a master stamp, in which the negative of the desired geometry must be preliminarily impressed [20]. Different than in all the other lithographic methods, the geometry of the resist pattern is not determined by the exposure contrast and by the action of the development process, but, instead, by the resist reflow during the application of a mechanical action to the mask. Consequently, the involved physical processes are quite different compared to all the other lithographic methods. Since some reflow of the resist material is necessary for the NIL procedure, the viscosity of the resist during the imprint must be low enough. After the process, on the contrary, the imprinted resist must provide a sufficient mechanical strength to maintain the acquired shape during the subsequent pattern transfer processing such as plasma etching, just like the patterns obtained by optical and electron beam lithography.

Such control of the viscoelastic properties of the resist layer during NIL can be obtained using either thermal treatments (thermally assisted NIL) or UV curing (UV-assisted NIL). In thermally assisted NIL, the polymer that is used to transfer the pattern from the master stamp to the wafer is heated above its glass transition or fusion temperature, in order to achieve a sufficient fluidity and permit a correct molding of the pattern. After imprint, the wafer is cooled down to solidify the imprint material before detaching the stamp and proceed with the process.

In UV-assisted NIL, the imprint material utilized is actually similar to a negative resist, in which cross-linking can be promoted by UV exposure. Before being irradiated, the resist is sufficiently fluid to allow a correct imprint process, and consequently the stamp can be applied straightforwardly. However, after molding, UV exposure must be performed in order to fix the shape of the resist before removing the stamp. This is usually done by utilizing stamps that are transparent to the UV radiation used. After light exposure, the resist becomes solid, and the stamp can be removed before going on with the subsequent pattern transfer processes.

In NIL, the fabrication of the master stamps is a critical issue since they play the same role of the masks in photolithographic processes. However, different than in projection systems, no size reduction of the mask geometry is allowed, and consequently the stamp must be patterned with the same resolution required on the wafer, involving the use of nanopatterning and nanofabrication techniques. A possible way to produce NI rigid master stamps is resist patterning with EBL followed by high aspect ratio plasma etching on Si or glass substrates. Recently, new UV-assisted NIL techniques based on soft master stamps that are more tolerant to the possible presence of particles on the wafer during the imprint process have been developed, in which the soft stamps are molded from a nanofabricated rigid master using a thermally cured PDMS layer deposited on a thin glass layer.

Compared to projection UV systems, NIL is a potentially cheaper technology and is considered a viable alternative for the future implementation of the fabrication of memories. In order to become competitive, further improvements would be needed on NIL in terms of presence of defects in the pattern. However, the recent improvements achieved have been very fast, and the future of NIL in next-generation advanced patterning processes for memories is considered potentially bright. Due to its low cost, NIL is also a valuable alternative to DUV or EBL for non-IC technologies that may need at least one level of nanopatterning, such as LEDs, MEMS, and displays.

8.4 Extreme Ultraviolet Lithography

The latest frontier in lithography resolution improvement is extreme ultraviolet lithography (EUVL), which is based on light sources operating at a wavelength of 13.5 nm [21, 22]. Such new technology, for the very short wavelength used in the source, promises to solve the resolution issues related to the development of the next IC technology nodes but, at the same time, poses new challenges in several aspects of the lithographic process.

One of these challenges concerns the photoresist, since the EUV radiation is much more energetic than the DUV one, and is likely to produce ionization effects in the material after irradiation, generating free or excited electrons that may affect the irradiation energy deposition in the material and consequently the quality of the pattern. This effect, which might have appeared undesired at first, was actually exploited for the development of EUV photoresist chemistry, which is actually an ionization chemistry rather than a pure photochemistry as in NUV and DUV resists. In the development process, the generation of the acid molecule that changes the solubility of the resist in the developer is initiated by the optical irradiation and mediated by additional molecules such as photoacid generators (PAGs) and quenchers. These

mechanisms will be treated more thoroughly in the next section devoted to EUVL photoresists.

Other very demanding requirements for EUVL come from the need of a stable and powerful light source at 13.5 nm that can be suitable for high-throughput IC production. It was calculated that in order to match the requirement of 125 WPH, a light source of at least 200 W is needed for these systems. The development of EUV sources will be discussed in greater detail in the following in a dedicated section.

Even the mask used in EUV cannot employ the traditional materials used for DUV radiation. Since no material with sufficient transparency at 13.5 nm is available, EUV reticles must work in reflection rather than in the typical transmission mode adopted in the traditional lithographic masks. In order to keep them free from particle contamination, special protection materials have been developed, on which an intense research work is still being carried out.

As discussed before, most modern industrial plants producing ICs are based on scanners containing ArF deep-UV sources that produce monochromatic light at a wavelength of 193 nm, reaching a minimum lithographic pitch resolution around 80 nm, which can be improved by adopting multiple patterning techniques like LELE or SADP. Given the dependency of lithography resolution on wavelength and the importance of scaling of the critical dimension of ICs in Moore's law, it is not surprising that the research on advanced lithography has progressively led to the use of light sources with decreasing wavelength of operation. The ultimate target of wavelength scaling in optical lithography is EUVL.

Dating back to the first experiments carried out in the 1980s [23, 24], the research on EUVL systems has recently produced the first prototypes, which have been in the field for a few years in IC foundries, such as the ASML's 0.33 NA EUV scanner operating at 13.5 nm, which has demonstrated a 13 nm line/space resolution with both CA and non-CA resists [25]. With EUVL, the mask set used for lithography can also be reduced compared to present state-of-the-art processes, in which multiple masks are often needed for a single lithographic step in order to overcome the limitation in resolution, up to using a single mask for the litho step, with evident economic advantages. The development of suitable photoresist materials for the wavelength of 13.5 nm has been a fundamental theme in the research related to the development of EUVL systems.

8.4.1 Requirements for EUVL Photoresists

EUVL photoresists, as almost all photoresists used in IC technology in the last 30–40 years, have been based on the concept of chemical amplification, which was developed between the late 1970s and the early 1980s to handle the limited power of the optical sources used at that time. For EUV, new resists have been developed, also without chemical amplification, to address the specific problems of CARs in extreme ultraviolet lithography, such as low optical absorption, insufficient resolution, stochastics, and risk of resist line collapse.

For the possible industrial use of a new photoresist, several issues must be taken into account. The first characteristic is patterning performance, which is fundamental. Other important issues are edge placement, stochastic control, stability, sensitivity, current specifications of the tool, resolution, and defectivity. Resolution was demonstrated with both chemically amplified and non-chemically amplified resist, as mentioned above. Compared to traditional CARs, the new resist chemistries developed for EUV may have more problems in quality control and manufacturing, since CARs are very well established in current industrial processes and can rely on a large number of manufacturers. Other possible problems may come from the risk of metallic contamination in case the new developed resist chemistry contains metals, which is sometimes the case.

Edge placement error (EPE) is one of the key issues related to patterning quality. It is the superposition error of the pattern that is transferred to the photoresist with respect to a previous pattern already transferred to the substrate. Generally speaking, the edge placement error is composed of two contributions: the overlay error and the critical dimension (CD) error. The overlay contribution is directly related to the placement accuracy of the pattern during the scanning procedure. Using EUV, the overlay error is expected to be improved, thanks to the use of a single mask in place of the multiple masks utilized in ArF scanners. The CD EPE, instead, depends on a number of factors that may affect the critical dimension of the pattern and, consequently, the alignment with the underlying reference, such as mask/projection effects, resist stochastic variation in thickness, roughness, and profile. The acceptable CD stochastic variations in a lithographic process depend on the feature size that has to be transferred on the resist. In [26], for instance, it was reported that the maximum CD variation that can be accepted when fabricating 20-nm-wide vias is 3 nm. Considering the resolution that is possible in EUVL, it is easy to understand the importance of EPE control in this technology.

Considering a die containing N vias, the yield probability of the die (Y) is the complement of the failure probability of any via in the die, since the correct operation of a logic circuit requires all the vias in the die to yield. Consequently, if f_V is the failure probability of an individual via, considered statistically independent from one of any other vias of the die, we may write:

$$Y = (1 - f_v)^N \tag{8.6}$$

because the die yield probability coincides with the probability that no via among the N in the die fails. If the via

failure probability f_V is very small, as it should be in a good lithographic process, we may approximate Eq. (8.6) in the following way:

$$Y = 1 - Nf_v \tag{8.7}$$

By rearranging Eq. (8.7), we may write:

$$f_v = \frac{1 - Y}{N} \tag{8.8}$$

This form of the approximate equation allows to understand how demanding the requirement on the failure probability of the via f_V may be, considering a target die yield Y.

For instance, if a target yield of 99% is sought for the lithographic process and the number of vias in the die is in the order of ten billion (10^{10}), which is not uncommon in modern logic ICs, a failure probably f_V in the order of 10^{-12} is required. Consequently, the lithographic process needs to be very robust.

This challenge brings with it the need to control the stochastic effects in resist patterning, which depend on a number of factors. This challenge has been cyclically faced by the semiconductor industry during the shrinking of the critical dimension of ICs, particularly when shorter wavelengths were explored for the optical source. Chemically amplified resists, for instance, were invented between the late 1970s and the early 1980s to handle the problems related to the low intensity of the new lamps employed in 248 nm lithographic systems. An analogous development path is underway to bring EUV systems to the market.

Since, essentially, all the phases of resist exposure and development may in principle contribute to stochastic effects (photon absorption, generation of secondary electrons, quenchers, development process etc.), the sequence of chemical reactions involved in the development must be carefully investigated for the new photoresists used in EUVL. This is essential to achieve a good control of resist stochastics and consequently a sufficient yield of the patterning process.

In this respect, the chemistry of EUV CARs is peculiar [27], because, different from 193 nm resists, it is not pure photochemistry. EUV photons generate secondary electrons within the photoresist that interact with the photoacid generators (PAGs) to mediate the resist development reactions, so EUV CARs are essentially electron-sensitive resists.

One of the sources of resist stochastics are statistical variations in photon irradiation during exposure. The problem is particularly relevant in EUVL, in which the photon density during exposure is significantly lower than the case of ArF technology. To give an example, considering an exposure intensity of 20 mJ/cm^2, an ArF source develops 194 photons/nm^2, whereas an EUV source at 13.5 nm delivers only 14 photons/nm^2. This is an obvious consequence of the higher energy quantum associated with the single photon in EUVL, due to the shorter wavelength. The lower number of photons increases the impact of photon shot noise on EUV resist stochastics.

Table 8.1 Photon and quencher statistics in chemically amplified EUV resists [29]

Dose	20 mJ/cm^2	50 mJ/cm^2
Area	314 nm^2	314 nm^2
Volume (h = 2*CD)	12,560 nm^2	12,560 nm^2
Absorption	5 μm^{-1}	5 μm^{-1}
Generated electrons (2–4/photon)	1100–2200	2750–5500
PAGs (0.15/nm^3)	1885	1885
Quenchers (0.2/PAG)	377	377
7σ photon variation (%)	30	19
7σ Q variation (%)	36	36

Considering the case of patterning of 20 nm holes, the theoretical stochastic variability can be calculated considering the typical density of photoacid generators (PAGs) and quenchers, which are both essential molecules for the irradiation-induced reaction in EUV resists, within the holes [27, 28]. In Table 8.1, the cases of 20 mJ/cm^2 and 50 mJ/cm^2 are considered.

Due to the small area of the 20 nm hole, the number of quencher molecules within the dot is comparable with the number of absorbed photons during exposition, even though with the higher irradiation dose considered in the Table (50 mJ/cm^2), the number of absorbed photons is high enough to make quencher statistics dominant. In particular, the stochastic variability of the quencher molecules should be considered to characterize the two stochastic processes since they are random processes. With such a high variability in the distribution of the quenchers, it is likely that in some areas of the sample, no reaction at all occurs during resist exposure.

Similar considerations can be done for other resist chemistries. Generally speaking, the dominance of quenchers stochastics makes the effect of a high exposure dose on the critical dimension less effective compared to the situation in which photon stochastics is more important, because even in the presence of a higher number of photons, the variability of the critical dimension may not improve simply because many photons do not produce any secondary electron and consequently do not give rise to any reaction in the resist because of the low density of quenchers within the feature.

Due to these statistical effects, the typical result after development of small features such as a 20 nm hole in a EUV resist is the appearance of some statistical distribution of the feature size, which normally present some tails below and above the nominal value. The control of the tails of such a distribution is very important because it is enough to have one via that is too small (or too large) to produce a failure of the entire circuit, as mentioned before.

Concerning photon shot noise, a possible way to reduce its effect on resist stochastic variations is adopting new resist composition with increased photon absorbance, such as metal oxide resists [30].

In general, in order to bring EUV to the needed standard for industrial IC production, the following improvements will be needed:

- Increase of the photon absorption of the photoresist.
- Enhancement of the efficiency of secondary electron production by the photons in the resist: every photon should be able to produce a secondary electron and initiate the reaction.
- Achievement of an ordered structure of the photoresist in order to decrease stochastic variability of the properties from point to point in the material.
- Enhancement of the resist dissolution process in the developer.

At the present state of the art, no EUV resist developed so far meets all these requirements. In particular, in the literature, researchers concentrate on three requirements, abbreviated as the RLS triangle, in which the scope is minimizing resolution (R), line width roughness (L), and sensitivity (S). There is a trade-off between these parameters, where not all the three metrics can be minimized simultaneously.

In order to reach these goals, a deep understanding of the chemical and physical processes involved in the photoresist exposure and development process will be needed, such as photon absorption, secondary electron generation, energy distribution, and mean free path.

EUV lithography was formerly known as soft X-ray lithography and was developed within research laboratories starting from 1986, initially utilizing synchrotron radiation as a light source. More recently, commercial systems have been produced using laser-assisted plasma sources able to produce a power light of 250 W at intermediate focus, which proved to be necessary in order to overcome the power limitations of synchrotron radiation. In 2019, EUVL systems with NA of 0.33 have entered high-volume IC production, whereas an intense research work is still being done to extend the results obtained so far to 0.55 NA systems and possibly to shorter wavelengths than 13.5 nm. In this research, synchrotron radiation facilities are likely to maintain an important role.

8.4.2 Laser-Assisted Plasma Sources for EUVL

Light sources for massive EUV fabrication need to provide high power (to guarantee the required throughput in terms of number of wafers per hour) and stable irradiation dose for high yield. Moreover, they are required to comply with the specifications about the spectral content of the produced light that are necessary for the process. Nowadays, EUVL scanners are equipped with laser-assisted plasma sources that are the result of a 15-year research development.

EUVL was initially proposed considering the wavelength range 4–40 nm, which spans across the extreme ultraviolet and soft X-ray regions of the spectrum. In the initial development phase of EUV sources, synchrotron radiation and laser-assisted plasmas were competing technologies. In the 1990s, the power requirements for the sources were still low, in the order of 250 mW for the 12.5–15 nm range. With such power requirements, synchrotron radiation was more competitive at that time compared to laser-produced plasmas (LPP) because it was able to generate a much larger power. Another apparent advantage of synchrotron radiation compared to LPP was the fact that one synchrotron could produce more than one light source and potentially feed different lithographic systems.

Later on, it became clear that in order to be able to compete with the 193 nm lithographic systems, EUV source power requirements had to be around 250 W, and this put out of question synchrotron radiation. Moreover, the possibility to have a different source of light for each lithographic system is now considered an advantage because it makes a complete stop of the plant less probable in case of a source stop. From this point of view, the generation of multiple beam lines from a synchrotron equipment for different EUVL systems is no more considered desirable.

During the development of LPP EUV light sources, several types of laser were investigated, such as KrF at 248 nm, XeCl at 308 nm, XeF at 351 nm, CO_2 at 10.6 μm, and Nd:YAG lasers at 1064 nm and 532 nm (which is a solid-state laser). One of the most important criteria for the choice of the laser was the efficiency of the conversion of the excitation laser light into the useful EUV light. From this point of view, Li, Sn, and Xe appeared to be the most promising elements, since Sn and Xe show relatively broad emission bands in the wavelength range 13–14 nm, whereas Li has a sharp emission line at 13.5 nm. The existence of these emission bands (and the reflectivity of the available mirrors for the corresponding wavelength) leads to the choice of 13.5 nm as the preferred wavelength for EUV systems [31].

In Fig. 8.11, a typical LPP EUV system is schematically represented. It is composed by a CO_2 laser in a master oscillator power amplifier (MOPA) configuration, a beam transportation system, a set of focusing optics, and a vacuum chamber containing a Sn droplet generator onto which the CO_2 laser light is focused in order to produce the EUV light by secondary emission from the droplets. The interaction between the CO_2 laser and the Sn plasma occurs in the primary focus of an ellipsoidal mirror, in such a way that the generated EUV light from the plasma is reflected by the mirror and collimated on its secondary focus.

The principle of operation of the plasma is the following. Two pulsed laser beams, a pre-pulse and the main pulse,

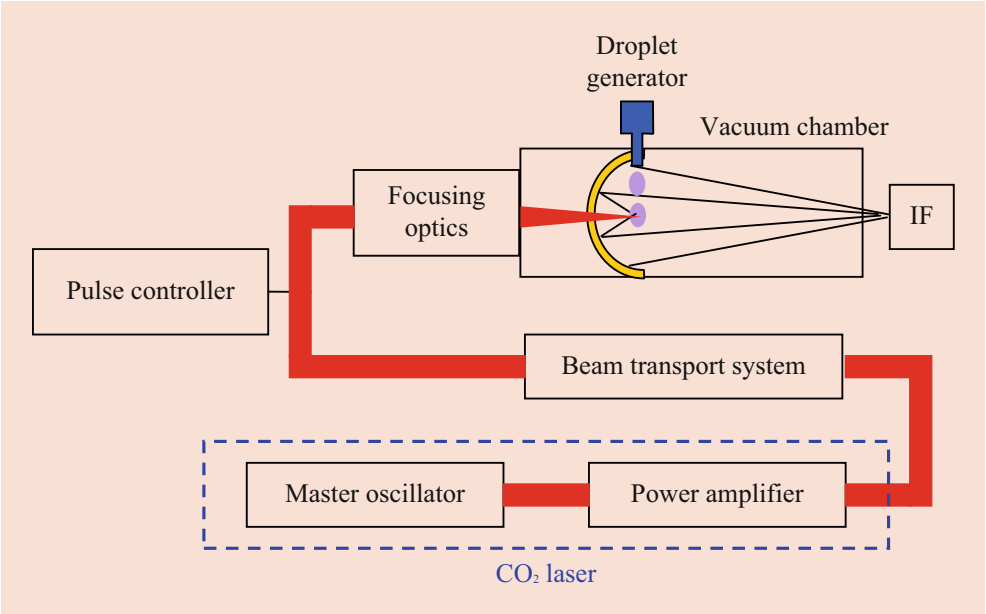

Fig. 8.11 Schematic representation of LPP EUV source

are directed toward the tin droplet plasma and activated at different times. Both lasers are generated by a seed and then amplified before being directed to the plasma chamber through the beam transportation system. The beams are also spatially separated in the chamber, since the function of the first laser pulse is increasing the surface of the Sn droplets by changing their shape, in order to reach an interaction surface of about 500 μm with the subsequent beam. In this way, the efficiency of the secondary emission from the plasma is remarkably enhanced. In order to fully exploit the potential of the method, the second laser beam is focused below the first one, in order to be able to interact with the particles after their shape change.

The setup of the system is designed in such a way that the interaction with the lasers with the particles takes place on one specific droplet at a time. As a consequence of this requirement, the repetition rate of the droplet emission needs to be sufficiently high, and the laser emission must be synchronized with it in order to guarantee that the laser-droplet interaction is repeated frequently enough to produce an intense secondary light emission.

Typical parameters of these systems are a repetition rate of 50 kHz for the droplet production, with a sufficient speed (80 m/s) to assure a relatively large separation between the adjacent droplets (around 1.5 mm). Thanks to the distance maintained, the plasmas generated by different droplets do not disturb each other. The atmosphere of the chamber is low-pressure hydrogen that also acts as a stopping gas for the Sn ions produced by the plasma.

Since the interaction of the primary laser with tin produces undesired effects such as ablation, clusters of particles, and fast Sn ions within the plasma, the system is designed in order to limit the amount of tin used, by reducing the droplet size and carefully controlling the timing of the droplet-laser interactions.

The EUV scanner contains several reflecting surfaces (one of which is the one represented in Fig. 8.11), which are used to collect the produced UV radiation and focus it on the processed wafer. Such reflecting surfaces have a key role in determining the attenuation of the light during the exposure procedure, since at every reflection the originally produced power is reduced. The technology of choice for the reflecting surfaces in EUVL systems is a multilayer Mo/Si technology that reflects around 67% at the Sn emission wavelength of 13.5 nm. This reflectivity is not very high but at the present state of the art is the best one available. As a consequence of the limited reflectivity of the Mo/Si mirrors and the different reflections that are used in the scanners, a very high attenuation of the emitted radiation takes place during the focusing process, leading to a projected power that is only 2% of the one produced by the Sn plasma, considering a number of reflections of 10 in the projection and illumination systems. This limitation in the efficiency of the illumination and projection systems based on Mo/Si mirrors has been the driving force for the development of EUV sources with increasing power, because, as widely discussed formerly, the intensity of the light projected on the wafer is a key issue for the wafer throughput of the lithographic process.

Another important aspect in EUV sources for 13.5 nm is spectral content control. Even though the secondary emission of the Sn plasma is related to the energy of the laser pulse that interacts with the droplets, with increasing secondary

emission power with increasing laser pulse, it is not granted, in general, that the central wavelength of the emission peak is always located at 13.5 nm independent of the energy of the primary laser. Since a well-centered distribution of the spectral power on the wavelength of interest is important for the yield of the lithographic process, the plasma should operate in such a way that the spectral content of the secondary emitted light is essentially independent of the power of the excitation laser pulse.

In the latest generation of EUVL sources, measured spectra of the emitted light for different energies of the laser pulse have been reported [32], showing a very good control of the wavelength of the emission peak, which is always centered at 13.5 nm. In this way, the center of the emission spectrum is also matched with the peak reflectivity of the Mo/Si mirror, which, being a multilayer structure, presents a rapidly decaying reflectivity as wavelength deviates from the peak value.

Concerning conversion efficiency, modern EUVL systems are able to reach a relatively low conversion efficiency around 6% of the pulse laser energy, which is almost constant within a threefold variation of it, considering that all the other parameters of the plasma are kept at a constant level and that only the laser pulse energy is varied.

The required power for the light source in EUV can be quite straightforwardly calculated by taking into account that in order to assure a wafer throughput of 100 wafers per hour (WPH) with the typical duty cycle of 60% used during the scan, a projected power of 550 mW on the wafer is needed. Since the emitted EUV radiation must undergo more than ten reflections in the mask, illumination, and projection system, and considering the reflectance of the Mo/Si multilayer mirrors at 13.5 nm around 67%, a required power of 200 W for the light source can be calculated. This power requirement is somehow more demanding than one of the 193 nm ArF scanners for which a source power around 90 W is enough to fulfill the requirements for 100 WPH throughput.

Since the irradiation dose on the wafer may vary according the requirements of the lithographic process (for instance, for yield issues, as explained before), it can be interesting to calculate the WPH expected by considering different combinations between the source power (measured in W) and the irradiation dose (measured in mJ/cm^2) because, quite reasonably, a larger irradiation dose generally leads to a lower throughput if the source power is constant. A possible way to represent the WPH variation with the source power and irradiation dose is plotting the dependency of the WPH on the ratio source power/irradiation dose, measured in Wcm^2/mJ.

The typical shape of the wafer throughput versus the ratio light power/irradiation dose is reported in Fig. 8.12 [32].

Depending of the numerical aperture (NA) of the projection system, different curves are obtained in which an initial monotonic increasing behavior of the throughput is observed

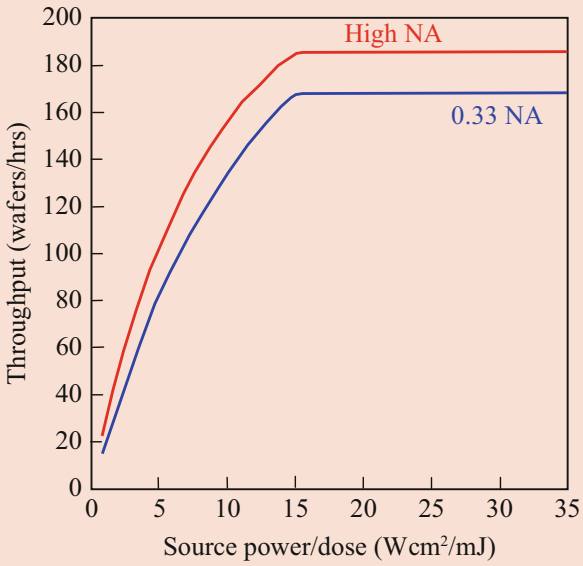

Fig. 8.12 WPH versus ratio source power/irradiation dose [32]

up to a saturation point beyond which a further increase of the source power/dose ratio is no more useful to improve the WPH.

Since the overall power of the plasma depends on the energy of the primary laser pulse and on its repetition rate, the light power produced by the system in the secondary focus of the main reflecting mirror (see Fig. 8.11) is also a function of the laser pulse and in particular of its peak power during plasma generation. Considering the efficiency of the secondary emission from Sn droplets, which is around 6%, and the lost power during exposure, also taking into account the optical transmittance of the plasma gas within the chamber, a peak laser power of 20 kW is needed in order to obtain a plasma laser source power of 200 W in the intermediate focus of the first reflecting mirror of the system.

The adoption of EUVL for high-volume manufacturing (HVM) has been hindered for years by the insufficient power of the sources. The recent achievement of stable emission with power of 250 W in EUV sources has paved the way to the adoption of this technology in HVM. Different laser architectures have been explored during the path toward power upscaling of EUV sources. The first laser architecture adopted was an unseeded laser scheme without master oscillator, named NOMO (no master oscillator) laser. In that scheme, the laser light directed toward the Sn droplets by the power amplifiers was fed back in the laser cavity after reflection from the plasma, exploiting the good reflectivity of the metal droplets. In this way, an unseeded self-sustaining active emission could be achieved. However, the power obtained with this solution was not satisfactory for the throughput requirements discussed before.

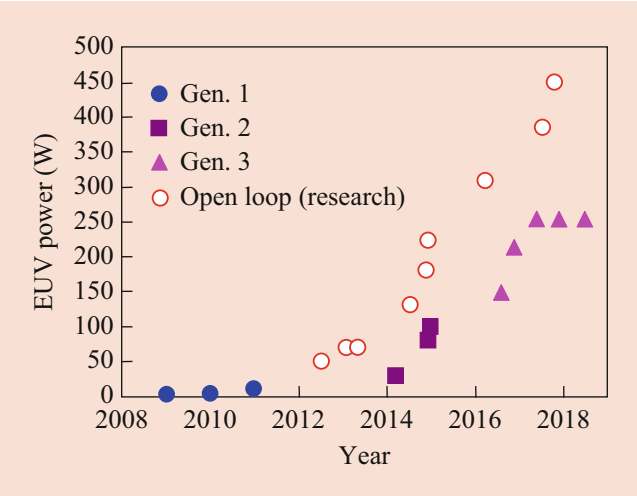

Fig. 8.13 Power scaling of EUV sources through the years [32]

The adoption of a laser seed in the master oscillator power amplifier (MOPA) configuration was a key innovation to increase the conversion efficiency and substantially increase the emission power. Another important innovation was the adoption of the pre-pulse used to increase the interaction area between the seed laser and the droplets. In the end of this development pathway, a tenfold increase of the emission efficiency in the Sn-based EUV source was obtained.

The much larger optical energy accumulated in the Sn plasma with these new system configurations also dictated more stringent requirements on the optical isolation of the laser system toward the external environment. All the technical innovations introduced to improve the optical isolation of the laser were key factors to further increase the power scaling after 2016.

In Fig. 8.13, the power scaling of the EUV source starting from 2009 to nowadays is represented in a plot, in which the potential capability of reaching 500 W for next-generation EUV sources in the near future appears likely.

In particular, the open-loop power obtained without any dose control in research system prototypes is very promising for potential improvement of the emitted power in future commercial equipment.

Another fundamental requirement for the source is power stability, which ultimately determines the irradiation dose reproducibility on the wafer, which is a key issue for the yield of the lithographic process, as discussed before. Recently, in 2017, the stable operation of 250 W power EUVL sources that can be employed to achieve 125 wafers per hour was demonstrated, with both power measurements performed in the source and irradiation dose measurements carried out in the far field of the projection system. In order to reach such stability, the control of the droplet generation and the stability of the pointing laser on the droplets were key issues. In these systems, the fleet average dose of the scanner is more than 99.99%, which means that in 99.99% of the cases, the irradiated dose projected on the wafer by the system is within the specifications required for a correct patterning of the resist.

Another aspect related to the stability of the source is the long-term degradation of the reflectivity of the collector mirror during the operation of the plasma. Such effect is mainly due to the possible deposition of Sn droplets that are produced within the plasma on the mirror surface. In order to maintain the reflectivity of the collector mirror over time, it is important to protect it from tin droplet deposition.

The degradation of the mirror reflectivity due to this phenomenon is normally measured in percentage per gigapulse, which is the percent degradation of the mirror reflectivity that occurs in the system after one billon pulses of light produced by the plasma. Modern mirror protection methods assure a mirror degradation ratio in the range 0.1–0.3%/Gp. Very recent developments reported in the literature have shown that the degradation ratio of the Mo/Si collectors can be reduced by designing the camera in order to bring the particle flow away from the critical region effectively, demonstrating a degradation ratio of only 0.03%/Gp over 32 gigapulses.

8.4.3 EUVL Chemically Amplified Photoresist Chemistry

The chemistry of EUV photoresist is a radiation chemistry that is similar to the one governing the behavior of electron beam (EB) resists. PMMA, for instance, is a material that can be conveniently used as both EB and EUV non-chemically amplified resist. In PMMA, the acid-catalyzed deprotection reaction that makes the polymer soluble in the developer can be initiated by both electron beam irradiation and EUV exposition, since in both cases the interaction with the radiation can induce a decrease of the molecular weight of the polymer within the exposed regions as a consequence of a chain scission straightforwardly induced by the interaction of the polymer with the radiation.

In chemically amplified EUV photoresists (which can be often used also as EB chemically amplified photoresists), the physical and chemical processes involved in the patterning process show some similarities to the mechanisms already described earlier for DUV chemically amplified resists, but are more complicated.

The main reason for these differences comes from the fact that the EUV radiation, whose wavelength is 13.5 nm, is so energetic that its photon energy (92.5 eV) exceeds the ionization threshold of the polymer molecules that constitute the backbone of the material. This was not the case for ArF DUV lithography in which the energy associated with the 193 nm wavelength used was much lower, largely

below the ionization threshold of the polymer molecules. These ionization phenomena, which take place during resist exposure, play a fundamental role in the resist chemical amplification mechanism that governs the patterning process. Indeed, the generation of the acid molecules that catalyze the deprotection reaction of the polymer chain during the PEB and make the material soluble in the developer are closely related to the free electrons created in the material by the ionization of the polymer molecules. This is the reason why, different than in DUV resists, the patterning process of EUV resist is regulated by radiation-induced rather than photon-induced chemical phenomena.

It is worth noticing that, since the photon energy in the ionizing EUV radiation is lower than the energy of electrons utilized in EBL (1–100 keV), the mentioned ionization phenomena can also explain why, generally, EUV photoresists can also be used as EB chemically amplified photoresists, exploiting similar chemical reactions initiated by the electron-induced ionization of the polymer molecules. Consequently, understanding the radiation chemistry of EUV CARs may also lead to the understanding of their sensitivity to electrons and their possible use in EBL. This is important since although EBL is not considered, at the moment, as the main candidate for mass production of next-generation ICs, it remains fundamental for the fabrication of the photomasks used in projection photolithography, such as EUVL. Improving the performance of EBL in photomask fabrication is gaining increasing importance as the requirements on mask quality in advanced projection lithography are becoming more stringent, not only because of the shrinking of the critical dimensions of the pattern but also owing to the adoption of new sophisticated technologies that can improve the projection process, such as optical phase shift [33].

The patterning process in EUV CARs can be summarized as follows. The first step, as in any lithographic exposure, is the selective exposure of the resist to the EUV radiation, which generally takes place through a projection system in which the photomask, different than in DUV and NUV lithography, is used in reflection rather than in transmission mode. The irradiation of the EUV resist, as mentioned before, produces ionization phenomena involving both the polymer molecules and other acid generator molecules, which are added to the mixture in order to produce the acid catalyzers that are necessary in the chemical amplification reaction. Even if the dissociation of the acid generator can be also directly produced by the EUV or the electron irradiation of the resist, it was demonstrated by specific investigations that this phenomenon is statistically unimportant in the acid generation process that takes place after irradiation. Most of the acid generator dissociation in the resist, indeed, occurs by dissociation reactions involving the acid generator molecules and the ionized electrons produced by the ionization of the polymer molecules.

Therefore, the effect of radiation on the acid generator is indirect, since the EUV radiation does not act directly on the acid generator molecule to form the catalyzing acid. Instead, the radiation acts on the polymer molecules, producing free electrons that subsequently give rise to the acid molecule by reacting with the acid generator. These free electrons, after thermalization, interact with the acid-generating species giving rise to the acid catalyzers.

During the dissociation reaction mediated by the thermalized electrons coming from the polymer ionization, the acid generator molecule captures a free electron and releases an acid counteranion, which represents a fixed charge in the polymer matrix. After the latent image constituted by such molecules is formed, the acid counteranions initiate a deprotection reaction on the polymer molecules, usually during a PEB step, which is mediated by the presence of protons (hydrogen ions) provided by other chemical reactions involving the acid anions and the polymer molecules, both in ionized form and in the fundamental state. Such reactions finally allow the material to become soluble in the developer solution.

The same fundamental mechanism is followed in case the resist is exposed using an electron beam instead of EUV radiation, except for the fact that the energy deposition from the radiation that takes place during the ionization of the polymer molecules is governed by different physical phenomena, whereas, after ionization, the sequence of chemical reactions is similar.

Compared to a purely photon-induced chemical amplification, the chemical mechanisms of EUV CARs involve more elements, such as the secondary electrons and the protons, whose impact on the performance of lithography is important and must be evaluated when developing new EUVL materials with chemical amplification.

Thanks to the reduced wavelength utilized for the exposure, EUVL CARs have demonstrated a sub-20 nm patterning capability with high sensitivity to the irradiation (doses in the range 10–20 mJ/cm^2 are sufficient for a successful development process). However, the line width roughness (LWR) is still larger than the value (<1 nm) that would be needed for the node that requires a 20 nm feature size, and a trade-off among resist sensitivity, resolution, and LWR seems to exist in the technology.

The origin of LWR in EUV lithography has been investigated in several studies and appeared to be mainly dependent on the chemical gradient on the borders of the exposed areas, which is the gradient of the chemical species involved in the development, for instance, the concentration of unprotected monomer units in the material that are responsible for its solubility in the developer. In developing EUV photoresists, strategies to enhance the chemical gradient should be elaborated in order to improve LWR without affecting resolution and sensitivity.

In order to analyze in detail the chemistry of EUVL CARs, the following subsequent steps involved in the exposure-development procedure of these resists have to be considered:

- Accumulation of the radiation energy (EUV or EB) in the resist material.
- Formation of a pair composed by a radical cation and a secondary electron as a consequence of ionization phenomena induced by the irradiation.
- Generation of an acid counteranion by dissociative electron attachment of acid generator molecules.
- Proton generation through ion-molecular reactions between the polymer and the radical cations produced by the irradiation.

In the following, each of these steps is analyzed in greater detail.

Accumulation of Radiation Energy Within the Resist

In EUVL, the irradiation on the photoresist transfers energy to the material through atom ionization and electron excitation. This happens because the ionizing radiation loses energy in favor of the valence electrons of the atoms of the resist material, generally a polymer, as a consequence of inelastic interactions of the photons with the atoms. Due to the energy gained during the inelastic scattering events, some electrons may reach a higher energy state than the fundamental one (excitation). If the energy gain is high enough, the electron may be detached from the atom and become a free electron, leaving a positively charged ion in the reticule (ionization). In EB and EUV photoresists, the dominant energy deposition mechanism due to irradiation is ionization.

Like in conventional DUV lithography performed with ArF of KrF lasers, the energy deposition profile of EUV light can be calculated using Lambert's law :

$$\frac{\mathrm{d}I}{\mathrm{d}z} = \alpha I(z) \tag{8.9}$$

where I is the photon irradiation intensity, α the optical absorption coefficient, and z the depth of the path travelled by the photons from the surface of the photoresist layer during irradiation.

Following Eq. (8.9), the acid yield, which is the number or acid molecules generated per incoming photon in the resist, has been studied as a function of thickness in a resist layer constituted by poly(4-hydroxystyrene) (PHS) with 10 wt% triphenylsulfonium triflate (TPS-tf) [34]. This material is a chemically amplified resist that may be used with both EB and EUV exposure.

In order to estimate the acid yield, in this kind of experiments, an acid-sensitive dye (Coumarin 6) was added to the photoresist to observe the concentration of acids after irradiation. Such additive permits to measure the acid yield through the concentration of proton adducts produced by the acid-sensitive dye, which is known to be proportional to the acid yield. By exposing the resist to a 75 keV EB on layers with different thicknesses, it was found that the acid yield was approximately proportional to the thickness of the resist. This is due to the fact that the transmittance of the high-energy electrons on the resist is high and by consequently increasing the resist thickness, the number of scattering events produced by each irradiating electron increases, yielding a higher probability to generate an acid molecule after the whole resist exposition process.

Using EUV radiation instead of electrons, the behavior of the acid yield with resist thickness is completely different, since it rapidly saturates to a constant value as soon as the thickness reaches a critical value around 800 nm. This happens because the absorption of EUV photons in the resist is very high and consequently the penetration depth of the ionizing radiation is limited, different than the case of EB irradiation. Consequently, after the thickness threshold of 800 nm, the number of interactions of the radiation with the resist atoms no longer increases, and the probability to ultimately yield an acid molecule also saturates.

Another finding of these experiments was the fact that the absorption coefficient of the photons in the resist, and consequently the critical thickness for acid yield, was essentially independent of the acid generator concentration in the resist. This was found to be also true for EB adsorption, confirming that the direct interaction of the incoming electrons or photons with the acid generator molecules during the lithographic process is negligible in these types of chemically amplified resists.

It is also important to note that the interaction of photons with the polymer molecules is fundamentally different than one of the primary electrons when using EB.

Actually, whereas a high-energy electron can undergo different scattering events and ionize more than one molecule directly before completely losing its energy and stopping within the material, a photon can be absorbed only once by a molecule, generating a high-energy secondary photoelectron. Such electron, however, may be energetic enough to ionize other atoms, similar to what happens with primary electrons in EB irradiation (this phenomenon can actually take place also with EB irradiation but is less probable). Consequently, the secondary electron tends to interact with other polymer molecules until it loses enough energy to fall below the energy ionization threshold of the molecules and, afterward, initiates a thermalization process slowly losing its remaining energy up to reaching thermal equilibrium.

Since the mean free path of the photoelectrons generated by the EUV radiation is around 1 nm, the ionization and electron excitation events occurring as a consequence

of the photon absorption are quite concentrated around the absorption point. This is not true for EB and X-ray resists, in which secondary electrons can be very energetic, and this is the reason why a higher patterning resolution is expected with EUV, since in this case the generation of high-energy secondary electron is a less important concern. However, the problem of the thermalization distance has to be similarly considered in the two cases.

The problem of radiation absorption from the material molecules is of paramount importance in photoresists. Particularly, it is important to determine which molecule is absorbing the incoming radiation during the exposition process. DUV photoresists, for instance, are designed in order to concentrate the absorption on the acid generator molecules and reduce as much as possible the absorption by the polymer. For ionizing resists, this is not possible, since, as mentioned before, it was verified that the absorption from the acid generator molecules is negligible up to a weight percentage of 20% of them in the mixture, and absorption is mainly owing to the polymer molecules. Consequently, in order to obtain a desired absorption coefficient, it is necessary to rely on the overall polymer composition and not simply on the acid generator. Since the number of secondary electrons generated per unit volume in both EB and EUV resists increases with the absorption coefficient, because more photons absorbed or more interactions with primary electrons give rise to a larger number of secondary electrons, the acid yield in such materials is typically dependent on their absorption coefficient.

The absorption in EUV resist depends on the density of the material and on the absorption cross section of the polymer atoms at the wavelength used. In principle, the absorption coefficient of a material can be calculated by knowing its density and the absorption cross sections of the constituent atoms. Among the atoms that can be used in resists, fluorine is one with the highest cross section for EUV absorption, and this is the reason why the fluorination of polymers is considered a promising strategy to increase the absorption in these materials.

Quite reasonably, the increase of the resist absorption coefficient also increases the gradient of the acid generation through the thickness of the material, since photons are rapidly absorbed while penetrating deep into the material. For this reason, the thickness of heavily absorbing resist layers must be reduced for a good outcome of the lithographic process. Although absorption cannot be increased indefinitely because of the problem of sidewall degradation of the resist pattern (due to insufficient acid generation at the bottom of the layer and consequently to incomplete development of the pattern), it was calculated that with a 20-nm-thick EUV resist, a polymer with an absorption coefficient of 16 μm^{-1} could be used, leading to a sensitivity enhancement of four times in the resist without affecting resolution and line edge roughness (LER) [35].

In order to calculate the number of ionized atoms after resist irradiation, the energy required to ionize an ion-electron pair in the material must be considered. Such parameter, usually indicated with W, is almost independent of the electron energy for ionization energy levels above 1 kV. For electrons, W slightly increases with decreasing electron energies because the ratio between the ionization and excitation probability decreases with the energy. For photons, the effect is also present but is much smaller, excluding the wavelength range slightly above the absorption edge of the atoms. Considering the above mentioned PHS as a resist material, a value of W around 22.2 eV was measured and found approximately the same for irradiation with electrons and photons [36]. Consequently, considering the typical energy of an EUV photon of 92.5 eV, the number of electrons generated on the average by each photon is around 4.

This estimation is motivated by the fact that, after ionization, the secondary electron loses energy through the interaction with the material. Since its initial energy is on the average much higher than the ionization energy of the polymer W, such electron is likely to produce other secondary ionization events up to reaching a residual energy that is below the W of the material. Besides ionization, also electron excitation events without ionization may take place during the energy loss process that involves the ionized electron.

When the energy of the secondary electron decreases below the ionization energy, its residual energy is lost through intramolecular vibration interaction and, in the subvibrational regime, with interaction with intermolecular vibrations and phonons. This phenomenon is very fast in condensed materials, and equilibrium is reached after electron ionization within about 1 ps, preventing any possible direct observation. However, the thermalization distance, that is, the distance that the electron travels during the thermalization process from its initial position, can be estimated starting from the initial energy distribution and applying Onsager's theory. Such distance varies according to the compound considered: it was found to be between 3 and 5 nm in aromatic compounds and between 5 and 7 nm in alkane compounds.

This is a significantly higher distance than the mean free path of electrons in the material with initial energy in the range 20–100 eV, and consequently its effect has to be taken into account. Such relatively high travel distance of electrons during the thermalization process is owing to the fact that the electron energy loss below the excitation energy of the molecules in the material is ineffective and consequently slow.

Once the ionized electron thermalizes, its motion stops at a distance of a few nanometers from the ionized atom, forming a cation-electron pair that is named spur. Considering the typical distribution of thermalized electrons and ions after resist irradiation, the ionized electrons are generally much closer to the generating ion compared to all the other ions.

This means that their diffusion distance from the generating atom is much lower than the Onsager length, which is the length at which the thermal energy of the electron equals the potential energy of the electrostatic force that attracts it back toward its father cation (equal to about 28 nm in benzene derivatives). The reasonable consequence of this situation is the fact that the ionized electron tends to move back toward the cation because of the electrostatic attraction force until the spur finally recombines. Such reaction is named geminate ion recombination and is important because the electrons that recombine with the generating ions are not useful for the acid production process.

The Coulomb interaction between the ions and the electrons can be actually complicated from the description given above by the presence of overlapping spurs in the material, in which the calculation of electrostatic forces is less straightforward. In general, there may be two situations related to overlapping spurs. The first one consists in the overlap of spurs generated by the same electron or photon at a close distance from each other. The second is the possibility that two overlapping spurs are generated by different ionizing electrons or photons, a case that is more probable for high irradiation doses and is expected to depend on the dose of the ionizing radiation.

The possible formation of overlapping spurs within photoresist coming from individual irradiating photons or electrons can be studied by Monte Carlo simulations. The situation is different for EUV and EB resist mainly because the generation of the first electron depends on photon absorption in one case and on inelastic electron-electron interaction in the other case.

Consequently, the probability to create more than one spur is different in the two cases, being much higher for EUV in which the photon absorption always generates a secondary electron with energy gain equal to one of the irradiation photons, and consequently the probability that this secondary electron generates more spurs at a close distance is not negligible. For electrons, the inelastic interaction with the molecule can have a broader range of energy exchange with the ionized molecule, and this naturally determines a lower probability to generate overlapping spurs coming from the same ionizing electron.

From calculated probabilities of overlapping spur generation performed by Monte Carlo simulations, the average number of overlapping spurs generated per ionizing radiation was found to be 1.5 for electrons and 4.2 for EUV photons [37].

Anion Generation

In EUV and EB photoresists, the generation of the acids that are necessary for the resist development takes place through the dissociation of the acid generator molecules. These molecules, in general, may dissociate both through inelastic interaction with a high-energy electron or photon and by reaction with already dissociated electrons coming from the polymer molecules after completion of the thermalization process.

In DUV photoresists, the decomposition of the acid generators mainly occurs by direct absorption of the photons from the acid generator molecule. In ionizing radiation resists, such as EB and EUV resists, the percent of the direct dissociation of the acid molecules upon the overall acid generation process depends on their concentration in the material but is generally low compared to the case of DUV resists.

For a typical acid generator concentration of 10% wt, the direct dissociation of the molecule due to the interaction with the ionizing radiation is responsible for only 10% of the overall acid generator dissociation for EB and between 2% and 8% for EUV resists, and, consequently, the overall phenomenon of acid generation is mainly dependent on an indirect chemical reaction that involves the thermalized electron attachment to the acid generators [38].

The acid yield and distribution after irradiation in the resist can be calculated by solving a diffusion equation describing the diffusion of the thermalized electrons in which the Coulomb attraction from the ions and the electron dissociation reaction by interaction with the acid generator molecules are accounted for [39]. In the equation, the presence of single or multiple spurs can be considered. For EB resists, the simplified calculation that considers only single spurs does not differ much from the one that considers multiple spurs. This is not the case for EUV resist, in which on the contrary the effect of overlapping spurs is more important. This is due to the higher generation probability of multiple spurs close to each other discussed before, which represents an important difference between ionizing EB and EUV radiation.

Considering the multispur effect, generally speaking, the acid generation efficiency decreases because, in this situation, electrostatic forces on electrons are higher and this enhances the recombination probability of the spur, which competes with the acid electron dissociation reaction. The acid generation efficiency, in fact, presents a trade-off with patterning resolution, according to which a low blur of the acid generation is generally needed. In order to decrease blur, the thermalization distance of electrons after ionization should be reduced, because this would positively affect resolution and, at the same time, have no significant influence on the acid generation efficiency.

Considering the acid generator concentration, an increase of it would beneficially affect both resolution and efficiency, so there is no trade-off in this respect. By increasing the acid generator concentration, the resolution blur is found to decrease because the direct decomposition of the acid generator during exposure becomes less relevant [40]. This is the reason why the concentration of the acid generator is

generally much higher in ionizing radiation resists such as EUV and EB compared to DUV resists.

The reaction of thermalized electrons with acid generators discussed so far is not always straightforward since, depending of the type of resist, other elements may be involved, like the polymer molecules. In this respect, it is possible to distinguish three different reaction schemes of thermalized electrons in the formation of the acid anions.

Case (I): The thermalized electrons mainly react with the acid generator molecules to produce the anions. This is the case of resists like PHS and novolak, in which the reactivity of the polymer molecules with thermalized electrons is low.

Case (II): The thermalized electrons react with both acid generator and polymer molecules. This is the case, for instance, of PMMA, in which the interaction of the electrons with the polymer molecules is significant and gives rise to polymer radical cations. After the formation of such cations, some electrons in excess are transferred to the acid generator to form the acid anions. In this situation, the acid generator dissociation is somehow mediated by the reaction of the thermalized electrons with the polymer molecules.

Case (III): The thermalized electrons mainly react directly with the polymer to form the acid anions, without the contribution of any acid generator molecule. This behavior has been observed in single-component photoresists based on a dehalogenation of brominated polymer molecules that consists in the generation of bromine anions by dissociative electron attachment, in which acid protons are produced from the deprotonation of the polymer radical cations.

Proton Generation

As mentioned before, in some photoresists, proton generation after irradiation takes place through deprotonation reactions involving polymer radical cations and not directly by the decomposition of the acid generator molecules, from which only an anion and a neutral radical are produced. The deprotonation mechanism depends on the type of polymer that is used in the resist and is important for the yield of the lithographic process since protons are involved in the acid pattern formation process.

In aromatic polymers, the protons are generated by the hydroxyl groups that are present in the polymer radical cations after irradiation. In these materials (for instance, phenolic compounds), radical cations form as a consequence of irradiation, which subsequently generate protons through a deprotonation reaction. The type of deprotonation reaction that takes place and its efficiency in the proton generation depend on the aromatic polymer considered. In all cases, the acid yield is strongly correlated with the efficiency of the deprotonation reaction involved.

The deprotonation reactions in PHS are supposed to be the following ones [41]:

$$\mathrm{MOH} \rightarrow \mathrm{MOH}^{+} + e^{-} \tag{8.10}$$

$$\mathrm{MOH}^{+} + \mathrm{MOH} \rightarrow \mathrm{MO} + \mathrm{MOH_2}^{+} \tag{8.11}$$

in which MOH is the PHS molecule, MOH^{+} the radical cation of the molecule, MO the phenoxy radical, and $\mathrm{MOH_2}^{+}$ its proton adduct. The reaction has been studied in liquid phase, but it is believed to be valid also for the solid phase of the resist because in solid PHS films, the hydroxyl groups for both intra- and intermolecular connections with other similar groups, like in liquid phase. If a protection molecule for the hydroxyl groups is used in the polymer, the efficiency of the proton generation reaction depends on the chemical structure of the protecting group.

In methacrylate polymers, such as PMMA, the polymer molecules are ionized or excited by the incoming radiation, giving rise to radical cations (ionized molecules), excited neutral molecules, and also radical anions by reaction with the free electrons. All these molecules can react to generate protons by decomposition. The deprotonation reaction in this material takes place after a side chain detaches from the polymer forming a macroradical that subsequently undergoes a β-scission reaction that generates protons. The chain scission is also induced by UV light. Since PMMA after irradiation becomes acidic, the proton generation can take place even without the presence of any acid generator molecules.

Consequently, the proton generation mechanism in PMMA consists of two paths: the reaction that takes place directly from the polymer molecules and the one that involves the acid generator molecules. Since the direct reaction of the polymer molecules depends of the concentration of excited atoms, which are mainly created during the recombination of thermalized electrons with the generating ions, the presence of acid generator molecules in high density tends to suppress it because it decreases the recombination events by capturing most of the thermalized electrons before recombination. This is also true for polymer cations, since the presence of electron scavengers (compounds that tend to bind to a free electron) tends to limit the recombination of the cations with the emitted electrons.

As a consequence of this phenomenon, depending on the concentration of the acid generator in the resist, two different regimes may be distinguished: the polymer-limited regime and the acid generator-limited regime. For instance, at acid generator concentrations below 0.1 mol/l, the yield of trifluoromethanesulfonic acids is completely determined by the reaction of the acid generators with thermalized electrons, because the proton generation reactions are very efficient and the protons are abundant in the irradiated resist. Above this threshold, instead, the proton yield is smaller

than one of the acid anions produced by the acid generator decomposition, and the acid generation efficiency turns out to be limited by the deprotonation efficiency of the radical cations of the polymer. Such deprotonation efficiency is lower in PMMA compared to PHS because the deprotonation reactions are not the same in the two cases. In PMMA, however, the ionized electrons tend to be trapped by the same molecules of the polymer, and consequently the addition of acid generator molecules does not generally affect the acid yield significantly.

Proton Migration

In EUV resists, quencher compounds are normally added to the mixture. Their function in the photolithographic process is limiting the diffusion of the acids produced during the chemical reactions that follow the irradiation of the resist in order to make the resist development profile sharper, reduce LER, and improve the stability of the material in air. In order to produce this effect, quenchers generally act as proton traps or buffers.

The reaction of acids with quenchers is essential for pattern formation in resists. Such reactions are named neutralization reactions, since they produce a deactivation of the acid. Different possible neutralization reaction mechanisms have been proposed to explain the interaction of quenchers with acid molecules [42–45].

However, in spite of the action of quenchers, the protons produced by the chemical reactions initiated by the irradiation in the resist must migrate to their protonation site to complete the pattern formation process. In chemically amplified photoresists, several types of protonation sites exist in the material, such as oxygen atoms, ester or ether groups, hydroxyl groups, amines, and counteranions. Since protons are mainly generated by acid counteranions, which are in turn generated by the reaction of the polymer molecules with electrons that are far from the radical cations (otherwise they would recombine with them before taking part in the reaction), it may be assumed that the generated protons are initially located away from the counteranions. Since counteranions are negatively charged, they attract the protons that are positively charged with a Coulomb force.

The mechanism of proton migration toward the counteranion is believed to take place through the protonation sites mentioned above, until the proton reaches the site with maximum proton affinity in close proximity to the counteranion, in which its position becomes stable. This migration takes place before the post-exposure bake (PEB) of the resist. Since quenchers present a high proton affinity, a certain number of protons tend to stabilize on quencher molecules, while the remaining ones are trapped in the other protonation sites that are present in the exposed resist. Such proton migration mechanisms imply that the quencher-acid neutralization reaction can take place in high activation energy resists even at room temperature, before PEB, which is a process that deactivates the chemical protectors of the material.

This room-temperature neutralization phenomenon allows to improve the image contrast and the quality of the pattern borders by suppressing the deprotection in the areas of the pattern in which the irradiation dose is low (such as the borders of the pattern). In low activation energy resists, on the contrary, both deprotection and quencher neutralization may take place at room temperature, and consequently they are competing phenomena that are initiated by the resist exposure, different from the case in which deprotection is only owing to the PEB procedure. However, even in low activation energy resists, it is possible to enhance the deprotection of high-dose compared to low-dose irradiation regions in the resist and consequently increase the image contrast, by enhancing the deprotection reaction efficiency over the neutralization one. That is the reason why image contrast in low- and high-energy activation resists is not significantly different at the present state of the art.

8.5 Conclusion

The continuous shrinking of the critical size of ICs over the years has pushed the evolution of advanced lithography toward increasingly sophisticated techniques and to a progressive wavelength scaling of the light used for resist exposition. Another driving factor in the evolution of advanced lithography has been the need to improve the productivity of the lithographic systems, measured in terms of processed WPH. These factors have led to the development of the more advanced equipment that are widely spread nowadays in IC mass production plants, which are based on ArF laser projection systems operating at 193 nm. From the point of view of the development of the resist materials, a key innovation to meet the requirements of the market in terms of WPH was the introduction of chemically amplified resists, which allowed for a dramatic decrease of the lithography processing time. Since the critical size needed in modern ICs has decreased largely below the wavelength of 193 nm in recent years, the lithographic processes based on ArF systems had to be complicated in order to be able to obtain deep subwavelength patterning capabilities, with the introduction of techniques like immersion lithography and multiple patterning. After implementing the 40 nm node, advanced lithographic processes based on ArF systems are reaching the limit both in terms of scaling and in terms of cost-effectiveness, and the introduction of a completely new technology seems now necessary to proceed with the scaling of the IC critical size meeting and, at the same time, the cost and throughput requirements of massive industrial production.

The technology of choice for this revolution in advanced lithography is EUVL. This new method shows some continuity with the past since it is always an optical lithography that can be employed in projection systems, just like the ArF scanners. However, the wavelength scaling compared to the nowadays dominant technology is dramatic, shifting from 193 to 13.5 nm, and this leads to a number of technical issues that are entirely new for optical lithography, such as the need to develop resists based on atom ionization similar to those employed in EBL and the use of masks that operate in reflection instead than in transmission mode. Despite these problems, and the several open issues that remain in the technique, the first commercial EUVL systems have already been developed, and the future of the technology in massive IC production appears bright.

Other types of lithography, such as EBL and NIL, may compete with EUVL on the patterning resolution but do not seem to cope with the cost and throughput requirements of industrial IC production. However, EBL remains fundamental for the fabrication of the masks utilized in optical projection systems (including EUVL), and NIL is important in More than Moore applications and in peculiar semiconductor devices like memories.

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Advanced Technologies for Future Materials and Devices

9

Francis Balestra

Contents

9.1 Introduction 310

9.2 Nanoscale CMOS 311
9.2.1 FDSOI 311
9.2.2 Quantum Effects 313
9.2.3 Variability 313
9.2.4 Strained Channels 313
9.2.5 Ultimate Device Architectures 314

9.3 Nanoscale TFET, FE-FET, and Hybrid Devices 317
9.3.1 Tunnel FETs 318
9.3.2 Ferroelectric Gate Devices 325
9.3.3 Hybrid Devices 325

9.4 Conclusion 325

References 326

Abstract

The technology of future nanoelectronic devices faces substantial challenges, in terms of increased power consumption, saturation of performance, large variability, and reliability. In this respect, novel materials and innovative device architectures are necessary for nanoscale FETs.

This chapter presents a number of promising solutions for the "end of the roadmap," with multi-gate devices, nanowires, tunnel transistors, ferroelectric FET, and hybrid nanocomponents using, for instance, phase change materials or nanofilaments. Other alternative materials, like ultra-thin films, 2D and 1D nanostructures, and heterostructures using strained and III–V materials, will allow to boost the performance of advanced nanotransistors.

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Keywords

SOI · Ge · III–V · 2D · 1D · Carbon nanotube · Semimetal · Heterostructures · High k · Phase change material · Resistive material · Nanoscale CMOS · FDSOI · Multi-gate · Nanowire · CNTFET · Small-slope switches: Tunnel FET · Negative capacitance FET · Hybrid devices · TFET-NCFET · PC-FET · Nanofilament FET

9.1 Introduction

Silicon has been until now the leading semiconductor in the electronics industry. A large majority of the integrated circuits is fabricated with Si-based devices. In ultra-large-scale integration (ULSI) circuits, such as processors or memories, the basic component is the metal-oxide-semiconductor field-effect transistor (MOSFET). The first device of this type was proposed and fabricated in the 1960s [1, 2] and extensively developed during the following 50 years. Important advantages of the MOSFET are the quality of the Si/dielectric system and the possibility of realizing high-performance and low-power components. The Si/Si dioxide interface and, more recently, the Si/high-k interface have been improved over these years, leading to high-performance and reliable transistors with a very low defect density. Compared with their bipolar counterparts, the advantages of MOSFETs are low cost, high density, and low-energy consumption. However, bipolar devices are still widely used for some applications needing very high speed and/or low noise.

CMOS, now the dominant MOS technology, uses both n- and p-channel MOSFETs (Fig. 9.1). Historically, the architecture has been adopted due to its potential low-power consumption compared with other ones. The general trends in micro-/nanoelectronics of the last decades have been the

reduction of device geometry, which allows one to obtain an improvement of device performance and integration density. Other very important issues in this field are the decrease in power consumption, the enhancement in reliability, and the reduction in the variability and cost of electronic systems.

However, device scaling in the range of tens of nanometers (decananometer range), which pushes MOSFETs toward their physical and technological limits, faces formidable challenges. Indeed, the scaling scenario put forth in widely accepted industry roadmaps (ITRS/IRDS, NEREID) calls for about 10nm gate length MOSFETs in the next decade. In this range, transistor optimization needs a particularly good control of the electrostatic potential and charge in the active Si region, or in the alternative layer, in order to reduce the parasitic effects (for instance, short-channel effects and leakage currents) and improve the device performance (e.g., in terms of drain current and transconductance).

All these aspects, along with other advantages presented in the next section, are afforded by other Si-based or alternative device types, like the silicon-on-insulator structures, multi-gate devices, ultra-thin channels used as 2D materials, or 1D nanowires or nanotubes.

The significant increase in power consumption and heating, which is one of the main limitations of IC integration and performance, may also require the adoption of beyond-CMOS nanodevices [3] at the end of the IRDS Roadmap, in particular, steep-slope nanoelectronic devices, which in turn require disruptive concepts, nanomaterials, and architectures, like tunnel FETs, negative capacitance FET, or hybrid devices. The next sections show some of the most promising of these alternative devices and materials.

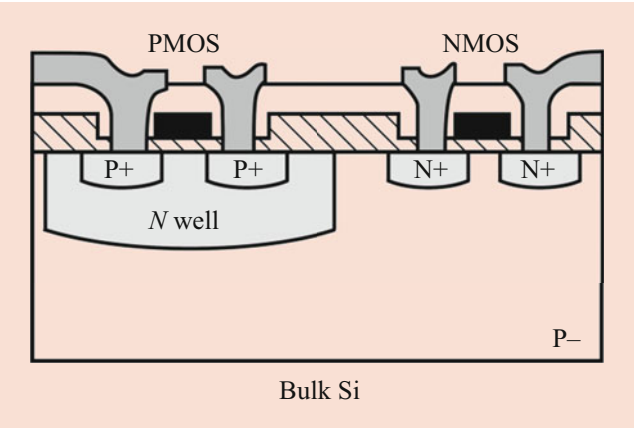

Fig. 9.1 Bulk Si CMOS structure

9.2 Nanoscale CMOS

The trend in micro-/nanoelectronic technology in the last decades has been that of increasing both speed and density by scaling down the electronic devices and of reducing energy dissipation. Future ICs are facing dramatic challenges in performance and power consumption, which must be overcome with the adoption of disruptive concepts, device architectures, technologies, and materials. Promising solutions for the nano-CMOS architecture include ultra-thin films, III–V/Ge channels, 2D layers, multi-gate structures, and nanowires or nanotubes.

The worldwide energy consumption has increased by 40% in the last 20 years. The ICT part represents 15% of the electricity consumption and will likely increase by a factor of 3 in the next 20 years. Therefore, research on the ultimate reduction of power dissipation in computing devices is strongly needed for the development of future low-power and high-performance tera-scale integration and autonomous nanosystems.

9.2.1 FDSOI

Figure 9.2 shows the SOI CMOS structure. A buried insulator is fabricated in the silicon substrate using various methods, the leading one being the Smart Cut technology, using hydrogen implantation and wafer bonding. SOI structure provides a number of advantages, suitable for many applications, and allows us to push back the limits intrinsic to the bulk Si structure [4, 5]; among them are:

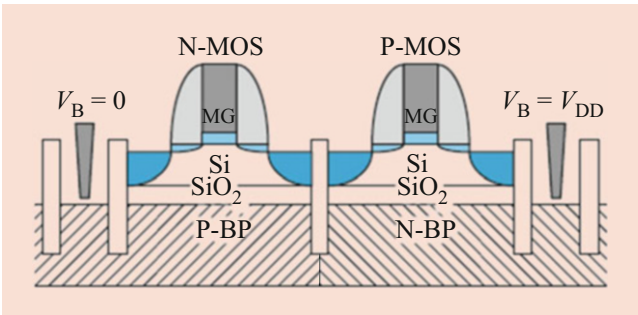

Fig. 9.2 Silicon-on-insulator (SOI) CMOS structure, with possible back gate control for optimizing device performance

1. The parasitic *n-p-n-p* structure (thyristor) which can be triggered in bulk CMOS structures is suppressed by the dielectric isolation available in the SOI technology.
2. Ultra-thin SOI films, inducing a full depletion or inversion ("fully depleted" or "fully inverted" devices, respectively) of the active silicon layer, can easily be fabricated. They have been found to exhibit very interesting behaviors, e.g., low-threshold voltage together with small leakage currents. Another advantage of thin SOI films is related to higher drain current and device speed.
3. The parasitic junction capacitances of source and drain are reduced using thin-film SOI, this opening the possibility of high-frequency operation.
4. The exponential increase in the leakage current with temperature is the main limitation of the circuit functionality in conventional CMOS operation at high temperature. SOI devices are fully functional up to 300 °C and beyond and can be used in analog and digital circuits, for example, in automotive and avionic applications.
5. In the field of memories, the SOI structure improves the performance for the integration of DRAM, SRAM, and non-volatile memories.
6. SOI MOSFETs are of great interest for niche applications, e.g., those requiring radiation hardness [advantage in transient ionizing and single-event upset (SEU)] for both space and nuclear radiation environments, owing to the small active volume. This was in fact the first application of the SOI technology. Other examples are low-temperature electronics and quantum engineering, where the SOI structure prevents some harmful parasitic effects (e.g., the absence of the kink effect for thin-film SOI) observed in the liquid helium temperature range.
7. The dielectric isolation afforded by the buried insulator opens the way to integrate complementary devices into a state-of-the-art CMOS process. Thus, the SOI technology leads to new "system on chip" concepts.
8. The special SOI structure can be advantageously used for developing new devices, like the volume inversion MOSFET with fully inverted channel (with two gates, three gates, or a gate all around the active Si layer), and quantum devices (extremely thin Si film, quantum wires, single electron transistors, etc.).
9. Some process simplifications are made possible by the SOI technology, mainly in the isolation and high-energy implantation.

However, some parasitic effects may be observed also in SOI devices. In this respect, electrical and thermal floating body effects are the main drawbacks of the SOI technology. These phenomena can be reduced or suppressed in advanced technologies by adopting ultra-thin Si film and/or very thin buried oxides.

In the last two decades, the static and dynamic power consumption of advanced nanodevices have strongly increased due to the slowing down in V_{dd} scaling and the parallel increase in the subthreshold leakage. This power challenge is due to the subthreshold swing limit S, which is 60 mV/dec at room temperature using thin-film SOI or multi-gate structures. As shown in [6], there exists a lower limit in energy per operation exists, which is reached for

$$V_{ddmin} \sim S$$

corresponding to the minimum energy:

$$E_{min} \sim C \,.S^2.$$

This shows that the limit depends on the subthreshold swing S and device capacitance C.

The definition of swing S is:

$$S = \frac{\partial V_g}{\partial (\log I_d)} = \underbrace{\frac{\partial V_g}{\partial \Psi_s}}_{m} \underbrace{\frac{\partial \Psi_s}{\partial (\log I_D)}}_{n} = \left(1 + \frac{C_s}{C_{ins}}\right) \frac{kT}{q} \ln\ 10 \tag{9.1}$$

Hence, its reduction may be achieved in two ways:

(i) Reducing m, the transistor body factor, which can be achieved by using ultra-thin body SOI, multi-gate or nanowire MOSFETs, carbon nanotube or 2D channels (this leads to $m \sim 1$), and negative capacitance FETs or MEMS/NEMS structures (this leads to $m < 1$)
(ii) Reducing n, which can be achieved by adopting a low-temperature operation (this solution, however, is not applicable in traditional applications), or using a modification of the carrier injection mechanisms with impact ionization or band-to-band tunneling, or considering hybrid devices combining several physical mechanisms

The MOSFET devices most suitable for obtaining a value of S close to its minimum use fully depleted [7–10] channels (e.g., FD SOI MOSFETs with very thin buried oxide [10]) or fully inverted devices [11]; the latter solution is preferable also because it optimizes the control of the electrostatics in the structure (e.g., double-gate, bulk, or SOI tri-gate/FinFET, gate-all-around MOSFET, or nanowire FET [12]).

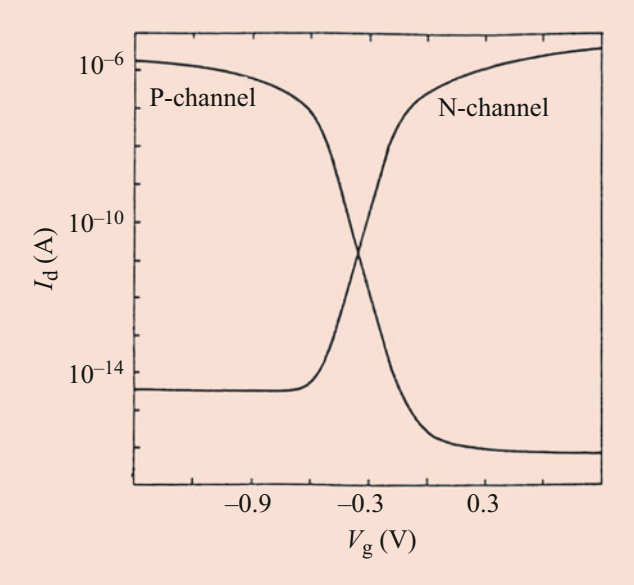

Fig. 9.3 Transfer $I_d(V_g)$ characteristics obtained by numerical simulation for fully depleted N- and P-channel SOI MOSFETs, showing a 60 mV/dec subthreshold swing (10^{14} Si doping, 600 nm Si film)

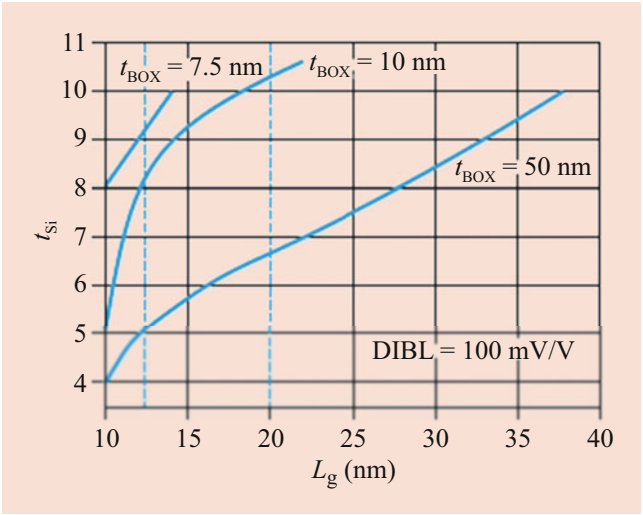

Fig. 9.4 Si film thickness and gate length needed to obtain a drain-induced barrier lowering (DIBL) effect of 100 mV/V for various thicknesses of the buried oxide

The first SOI MOSFETs of the fully depleted type were fabricated on SOS materials [7]; however, the quality of the Si film obtained with this technology was poor. Using simulation, the first fully depleted SOI MOSFET exhibiting an ideal swing of 60 mV/dec (Fig. 9.3) was demonstrated in 1985 [8]. In 1986, the first experimental demonstration of a FD SOI MOSFET showing a swing of about 60 mV/dec was published [9]. The first theoretical and experimental multi-gate MOSFET with volume inversion was shown in 1987 [11].

Considering logic and/or RF applications, in future ULSI circuits, the standard silicon channel could be replaced by other high-mobility materials. From this viewpoint, heterogeneous two-dimensional atomic crystals, in particular transition metal dichalcogenides (TMD), exhibit atomically smooth surface without thickness fluctuations, no dangling bonds, and good mobility in CVD-deposited films; for these reasons, they are very promising for ultimate nanoscale transistors and 3D ICs.

A TMD 3D transistor technology, based on novel hybrid Si/MoS_2 channel FinFET and NWFET, with improved electron mobility and I_{on}, has been demonstrated in [13].

The buried oxide thickness is another important parameter for alleviating short-channel effects. A significant attenuation of the threshold voltage shift by drain-induced barrier lowering (DIBL) in the 10–20 nm gate length range is observed when we reduce the buried oxide thickness down to sub-10 nm (Fig. 9.4) [14].

9.2.2 Quantum Effects

Ultra-thin Si films are a promising architecture for reducing short-channel effects, improving high-speed performance, and eliminating parasitic phenomena; so far, 2-nm-thick silicon films have been realized [15]. In contrast with the standard architectures, in which the electrons form a 3D system, in ultra-thin films, the electron system transits from 3D to 2D, and quantum mechanical effects (energy quantization) appear. Figure 9.5 shows an example of the variation of the threshold voltage V_t due to such a transition [16]. The analysis based on classical mechanics indicates that in fully depleted MOSFETs, the threshold voltage V_t is reduced when the film thickness decreases; this is due to the reduction in the depletion charge. In contrast, the quantum mechanical calculation shows an increase of V_t for thicknesses of the Si film below 10 nm; the phenomenon is explained by the formation of a 2D subband system, in which the ground state of the electrons is above the bottom of the conduction band Ec. Quantum mechanical influences, especially at low temperature, are also present in extremely thin SOI layers (<10 nm), where they have been found to enhance short-channel effects [17]. The quantum effects must be considered for the design of advanced SOI devices. On the other hand, SOI devices can also be fabricated with very small surfaces and volumes, this giving rise to ultra-small capacitances;

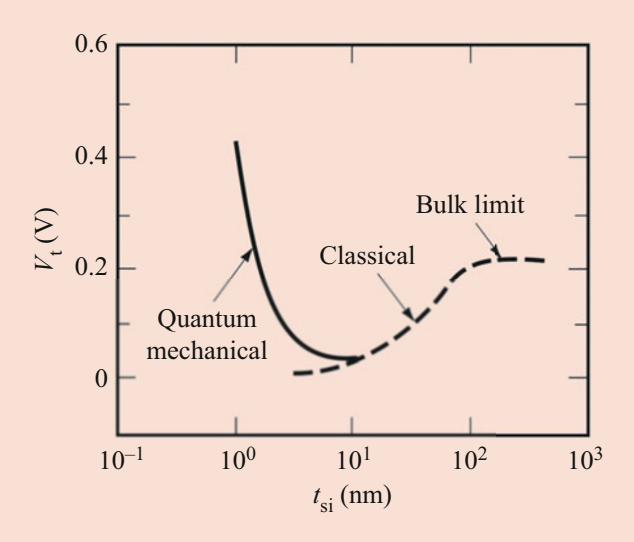

Fig. 9.5 Theoretical threshold voltage variation versus Si layer thickness showing the occurrence of quantum effects for an ultra-thin Si film ($t_{ox1} = 7$ nm, $t_{ox2} = 80$ nm, $N_a = 10^{17}$ cm^{-3}, $N_{sub} = 10^{17}$ cm^{-3}, $T = 300$ K)

for these structures, even at room temperature, the charge quantization regime leads to conductance oscillations due to the Coulomb blockade [18].

9.2.3 Variability

Figure 9.6 shows the impact of doping fluctuations on the threshold voltage variability for various devices. Ultra-thin body SOI and multi-gate devices show the best (i.e., smallest) variability compared with bulk transistors, even for more advanced MOSFETs, due in particular to the possible use of very low channel doping [19].

9.2.4 Strained Channels

The method for modifying the band structure of semiconductors (Ge, III–V, etc.) by means of the application of a suitable strain (uniaxial or biaxial, tensile or compressive), globally indicated with "strain engineering," has extensively been used since the early 2000s. The method has also the effect of boosting electron or hole carrier mobility and velocity.

An example of the effect of strain in a 18 nm gate length, N-channel SOI MOSFET fabricated on ultra-thin SOI films ($t_{si} = 2.5 - 11.8$ nm) is shown in Fig. 9.7. For a given OFF state current, the driving current in strained devices (sSOI) is about 40% higher than in non-strained SOI films, even for ultra-thin Si layers down to 2.5 nm. This behavior is ascribed to a higher carrier injection velocity at the source [20].

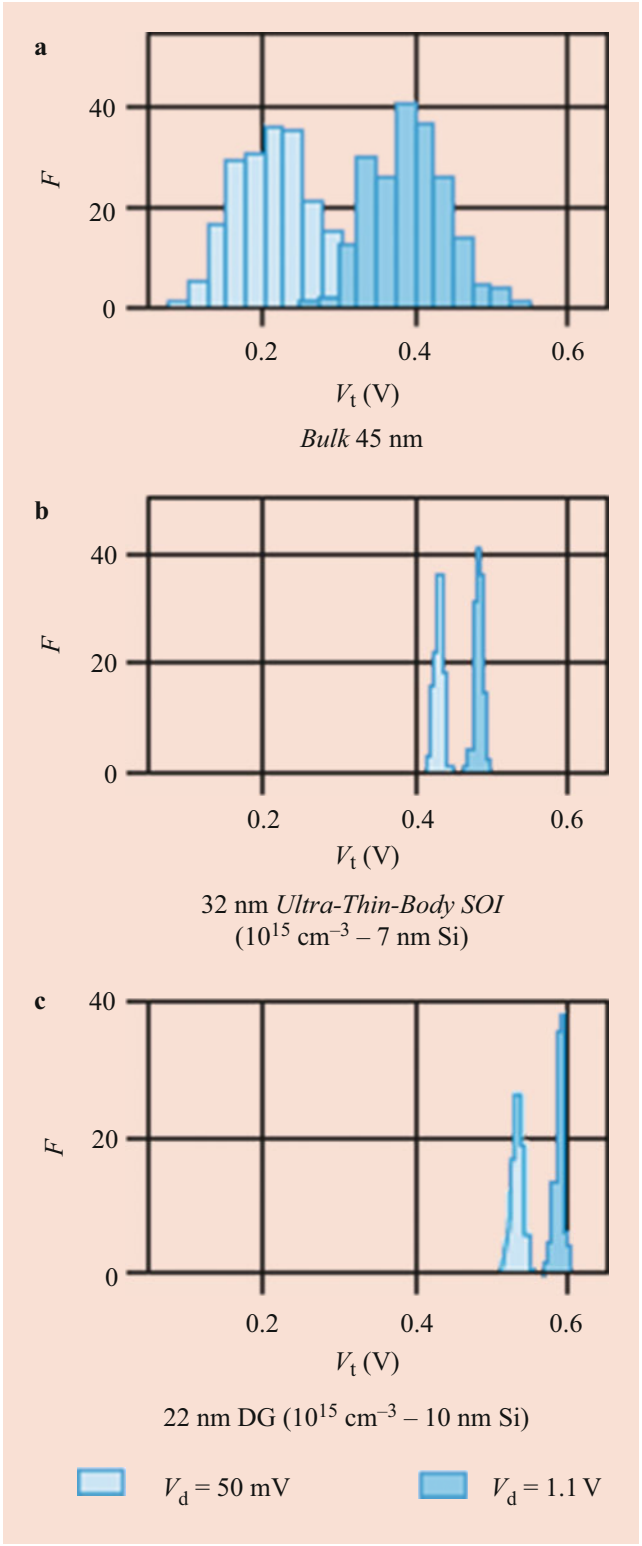

Fig. 9.6 Impact of channel doping fluctuations on threshold voltage variability for various architectures ((**a**) 45 nm bulk, (**b**) 32 nm UTB SOI and 7 nm Si film, (**c**) 22 nm double-gate and 10 nm Si film) and drain biases

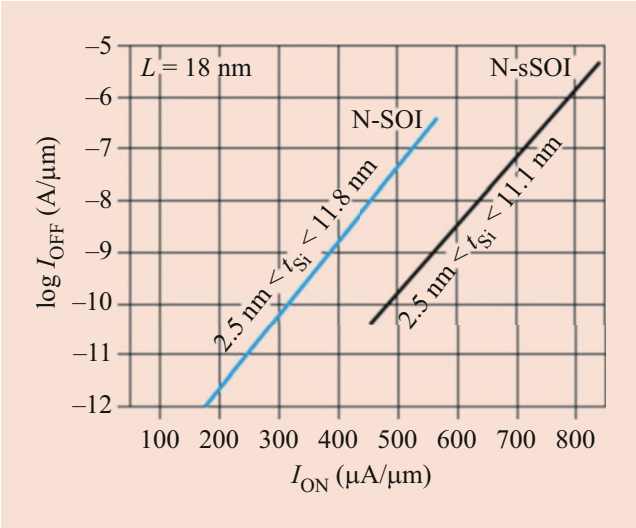

Fig. 9.7 Impact of strained Si on advanced N-channel SOI MOSFETs realized with various Si film thicknesses

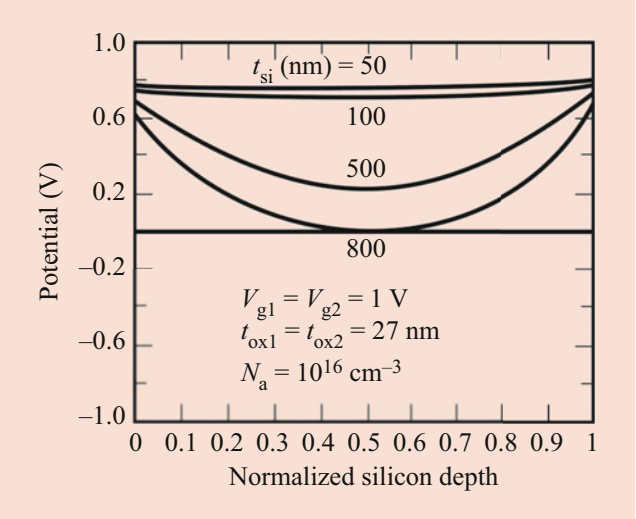

Fig. 9.8 Potential profile inside the Si layer showing the volume inversion regime for thin film (≤100 nm) DG SOI MOSFETs; the occurrence of a volume inversion (with a quasi-constant potential > $2\Phi_F$ in the whole Si layer) depends on the Si film thickness and doping (here a very low doping is used in the numerical simulation)

Another booster for transport parameters is to use alternative channel or substrate orientations [21].

9.2.5 Ultimate Device Architectures

The gate of a MOSFET induces an inversion channel located at the Si/SiO_2-high-k interface, with a typical length of a few nanometers. The multi-gate control of an SOI or bulk MOSFET makes it possible to force the whole silicon film in the strong inversion condition and gives rise to the "volume inversion (VI)" concept for "fully inverted" (or "fully accumulated") devices (Fig. 9.8) [11]. The fact that the current drive of the VI-MOSFET is governed by two, three, or four gates and that carriers are no longer confined at one interface presents remarkable advantages: they are the enhancement of the number of electrons or holes, the increase in carrier mobility and velocity due to reduced influence of scattering associated with oxide charges and surface roughness, the increase in drain current and transconductance, and the reduction of short-channel effects and subthreshold swing [22, 23]. The subthreshold swing S_{vi} and threshold voltage V_t of the VI-MOSFET are calculated using a constant potential in the whole silicon layer [24], which is a very good approximation for $V_g \leq V_t$:

$$S_{vi} = \frac{kT}{q} \ln(10) \left(\frac{C_{ox} + C_{ss}}{C_{ox}} \right) \tag{9.2}$$

$$V_t = V_{FB} + 2\Phi_F + \frac{qt_{si}N_a}{C_{ox}} - \frac{Q_{ss}(2\Phi_F)}{C_{ox}} \tag{9.3}$$

In (9.2, 9.3), C_{ss} (= qN_{ss}) is the interface-state capacitance, C_{ox} the gate oxide capacitance (it is assumed that the interface-state densities $N_{ss} = Q_{ss}/q$ and oxide thickness are similar at the upper and lower Si film interface), V_{FB} the flat-band voltage for both front and back gate, Na the silicon layer doping, Φ_F the Fermi potential, and $Q_{ss}(2\Phi_F)$ the interface-state charge for a surface potential equal to $2\Phi_F$.

It is worth pointing out that, although in general the inversion charge Q_i within the expression of the threshold voltage is neglected with respect to the depletion charge Q_d, this is not possible in the case of volume inversion because, at threshold, it is $Q_i = Q_d$.

A reduction of hot-carrier effects (substrate current, photon emission, and hot-carrier-induced degradation) has also been reported in multi-gate SOI MOSFETs [25, 26]. Various SOI structures (double-gate [27], DELTA or bulk/SOI FinFET [28], GAA (gate-all-around) [29]) have been proposed in order to take advantage of this original feature (Fig. 9.9a, b). Figure 9.10 shows how, in the volume inversion functioning, the performance of the device improves with respect to that of a conventional single-gate SOI operation [29], highlighting a transconductance up to three times larger. The VI-MOSFET proved to be particularly suited for alleviating short-channel effects in ultimate ultra-short-channel MOS transistors [30], affording a substantial decrease of DIBL (Fig. 9.10b) and charge-sharing phenomena [31]. These advantages are obtained together with very large driving current and very small leakage currents for drain bias up to 1.5 V in a wide Si film thickness range. Whatever the architecture, decreasing the thickness of the Si film (down to 5 nm) and

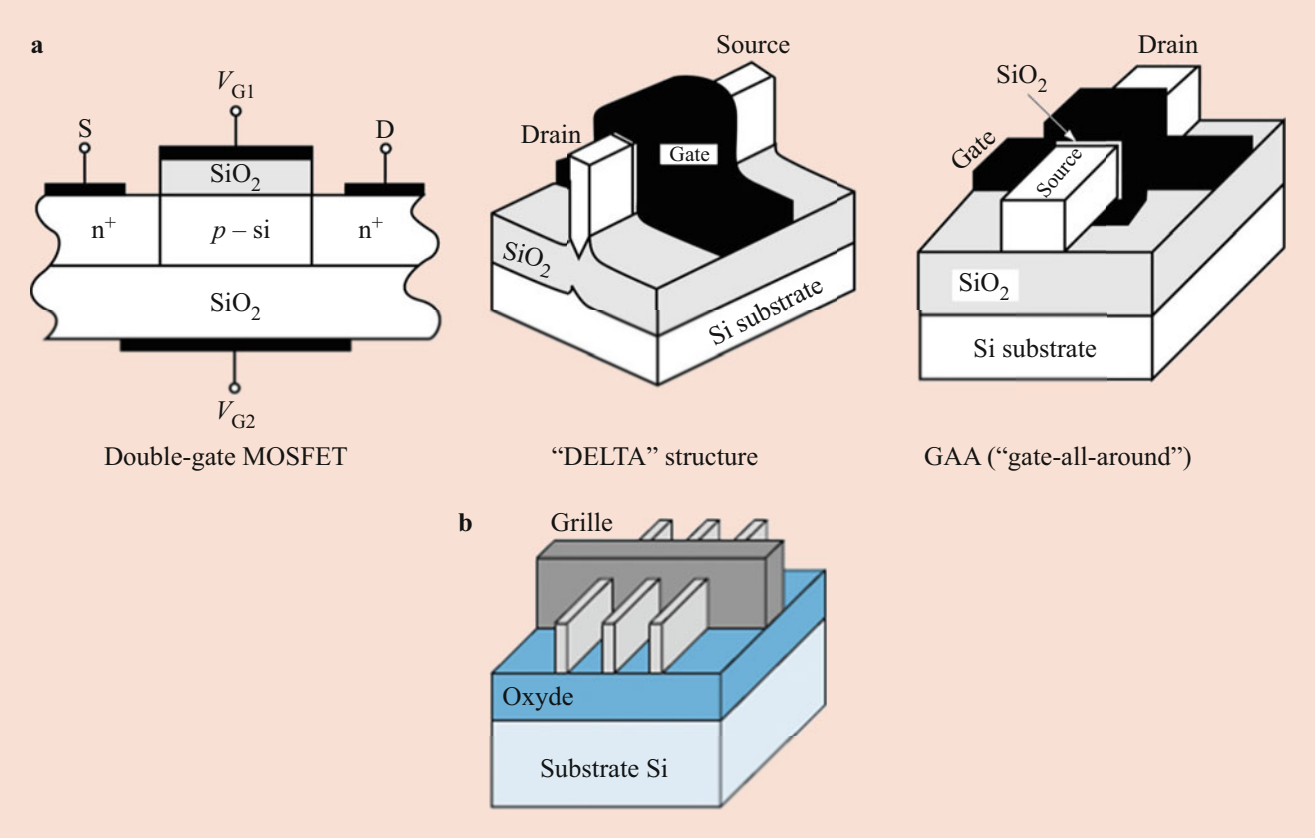

Fig. 9.9 (**a**) Various SOI structures using the concept of volume inversion in order to obtain fully inverted devices: double gate, DELTA or FinFET or tri-gate, and gate-all-around. (**b**) FinFET structure on insulator with parallel fins

the concentration of dopant also reduce the short-channel effects (Fig. 9.10b). A reduced sensitivity on the silicon film thickness and doping is also observed in double-gate devices.

This transistor appears to be the best candidate for the ultimate integration of silicon and could be proposed for fabricating devices down to the sub-10 nm range, even if the IRDS Roadmap currently does not plan an integration in such a range.

Indeed, Fig. 9.11 shows the subthreshold slope for different architectures of ultimate FET nanodevices (Ω-gate nanowires, GAA carbon nanotubes, 2G Si MOSFET for gate lengths beyond the end of IRDS Roadmap down to 5 nm). We can see that multi-gate nanowires with volume inversion overcome short-channel effects down to ultimate lengths while maintaining very good switching behavior between the OFF and ON states ($S \approx 70$ mV / decade) [32].

Multi-channel MOSFETs fabricated with multi-gate devices, realized with the silicon-on-nothing technology, have also been proposed to boost the driving current using several channels. The N- and P-MOS MCFET using high-k TiN/HfO_2 gate oxides provides very good characteristics (Fig. 9.12) [33].

Double-gate devices with gate underlap led also to a very good Idsat, a reduction in the DIBL and drain to gate tunneling current, and a decrease of the gate capacitance, propagation delay, and power consumption [34].

Evaluation of swing and DIBL in DG and SOI structures using 2D materials from one layer to three layers of MoS_2, as well as in Si UTB DG FETs, has shown that MoS_2 FETs have better electrostatics than Si devices due to the minimum thickness of the films (atomic dimension). SOI topology can only present good electrostatics for one-layer TMDs, while DG topology can present interesting performance for up to three layers. The best performance is obtained for a double-gate MOSFET with a single layer of MoS_2, with a similar swing as the previous Ω-gate nanowires (Fig. 9.11) in the 5 nm gate length range (Fig. 9.13) [35].

A theoretical comparison of scaling limit for TMDs, phosphorene/black phosphorus (BP), and Si MOSFETs is carried out in [36]. The best results for scaling properties are obtained for TMDs (MOS_2 and SnS_2) and BP channels due to ultrathin channels (monolayers) and reduced dielectric constant compared with Si (Fig. 9.14).

It has also been shown experimentally that the bandgap of 2D layers can be modulated by transverse electric fields in bilayer graphene ribbon (100 nm) and in bilayer MoS_2 [37].

Another interesting possibility at the end of the roadmap is the use of semimetals for the channel and source/drain

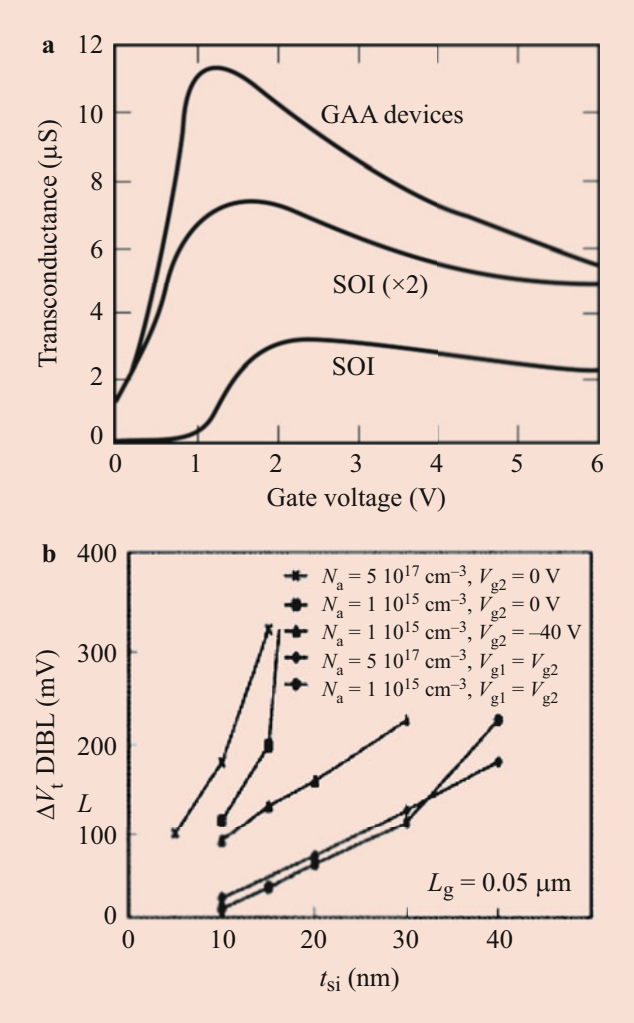

Fig. 9.10 (**a**) Transconductance in a conventional SOI MOSFET, a DG transistor without volume inversion, and a GAA device with volume inversion ($W/L = 3\ \mu m / 3\ \mu m$, $V_d = 100$ mV. (**b**) DIBL effect versus silicon film thickness for 50 nm μm single-gate SOI MOSFETs ($t_{ox2} = 380$ nm, $t_{ox1} = 3$ nm) with high doping ($N_a = 5 \times 10^{17}$ cm^{-3}, $V_{g2} = 0$ V), low doping ($N_a = 10^{15}$ cm^{-3}, $V_{g2} = 0$ V), and back channel accumulation ($N_a = 10^{15}$ cm^{-3}, $V_{g2} = -40$ V) and for DG SOI MOSFETs ($t_{ox1} = t_{ox2} = 3$ nm, $N_a = 10^{15}$ cm^{-3} and $N_a = 5 \times 10^{17}$ cm^{-3} with $V_{g1} = V_{g2}$)

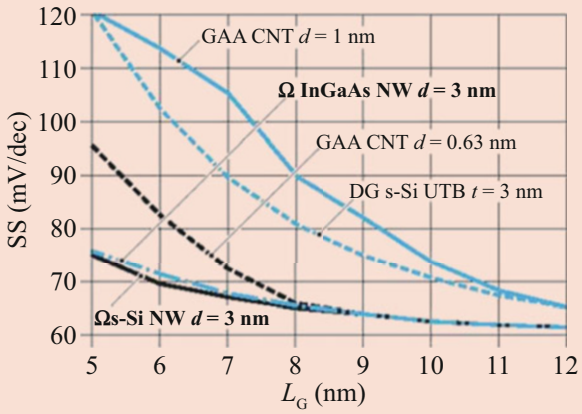

Fig. 9.11 Subthreshold swing obtained by quantum simulations as a function of gate length for various MOSFET architectures: Ω-gate sSi and InGaAs nanowires (3 nm diameter), gate-all-around carbon nanotubes (0.63 and 1 nm diameter), double-gate ultra-thin body MOSFET (3 nm Si film thickness)

regions. Indeed, for 1D devices, the bandgap of semiconductors and semimetals increases when the nanowire diameter decreases. Therefore, a semimetal becomes a semiconductor in the sub-10 nm range (Fig. 9.15). A 1D structure could thus be used for the channel and a thicker source/drain region with the same materials (e.g., Sn, Bi) for source and drain with a metallic behavior, without any doping. Very good electrical properties have been shown by simulations for 1 nm GAA Sn NW with a 2.3 nm gate length, leading to a 72 mV/dec swing and I_{on} of 3 mA/μm at $V_d = 250$ mV [38].

High-performance Si transistors can have gate lengths as short as 5 nm before source-drain tunneling, but below this value, the loss of electrostatic control leads to unacceptable leakage currents when the device is off. The use of MoS_2 as a channel material has recently been studied using a 1 nm physical gate length with a MoS_2 bilayer and a single-walled carbon nanotube as the gate electrode. Very good switching characteristics, swing (~65 mV), and on-off state current ratio of ~10^6 were observed [39].

The electrical characteristics for this 1D2D-FET (Fig. 9.16) show that the MoS_2 extension regions (the underlapped regions between the SWCNT gate and S/D contacts) could be heavily inverted (i.e., n+ state) by applying a positive back-gate voltage of $V_{BS} = 5$ V to the Si substrate. The I_D-V_{BS} characteristics (Fig. 9.17) show that the MoS_2 flake was strongly inverted by the back gate at $V_{BS} = 5$ V. The I_D–V_{GS} characteristics for the device at $V_{BS} = 5$ V and $V_{DS} = 50$ mV and 1 V (Fig. 9.17a) demonstrate the ability of the SWCNT gate to deplete the MoS_2 channel and turn off the device.

9.3 Nanoscale TFET, FE-FET, and Hybrid Devices

In order to reduce static and dynamic power consumption in nanoscale FETs at the end of the roadmap, sub-60 mV/dec subthreshold swing (e.g., TFET, NC/FE-FET) are needed (Fig. 9.18) [40].

Figure 9.18 presents the comparison of the theoretical subthreshold swing vs gate length for the most advanced nanoscale FET architectures and materials available in the literature. The IRDS (International Roadmap for Devices and Systems) needs for logic devices are also shown vs time

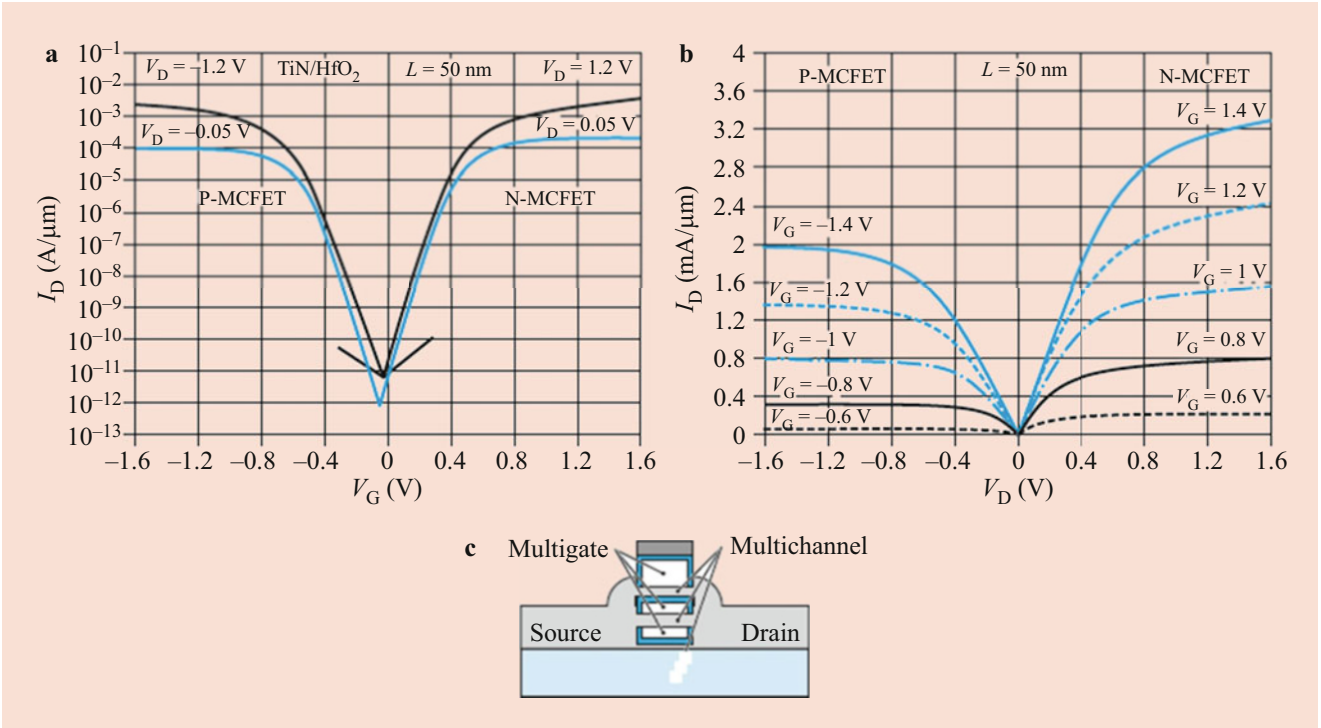

Fig. 9.12 50nm multi-gate and multi-channel (MG-MC) MOSFETs with high-k gate oxide showing very good I_{on} and I_{off}. (**a**) Transfer characteristics. (**b**) Output characteristics. (**c**) MG-MC structure

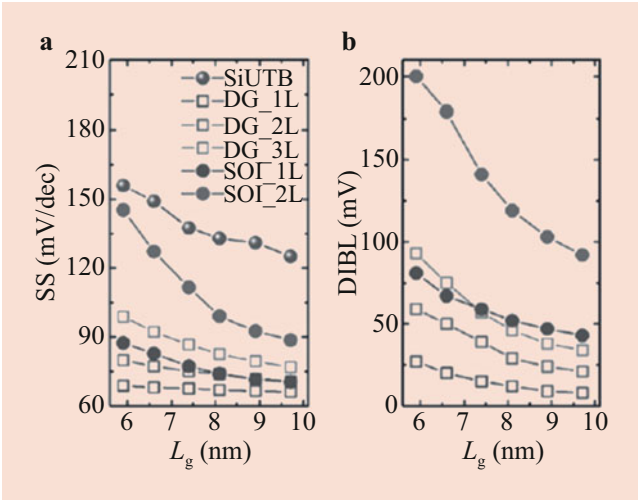

Fig. 9.13 (**a**) Subthreshold swing (SS) and (**b**) drain-induced barrier lowering (DIBL) with gate length scaling for MoS_2 MOSFETs realized with various numbers of layers and Si-based ultra-thin body double-gate MOSFETs with a symmetrical top and bottom gate dielectric; in SOI, the bottom dielectric is a 50-nm-thick SiO_2, and the bottom gate is grounded

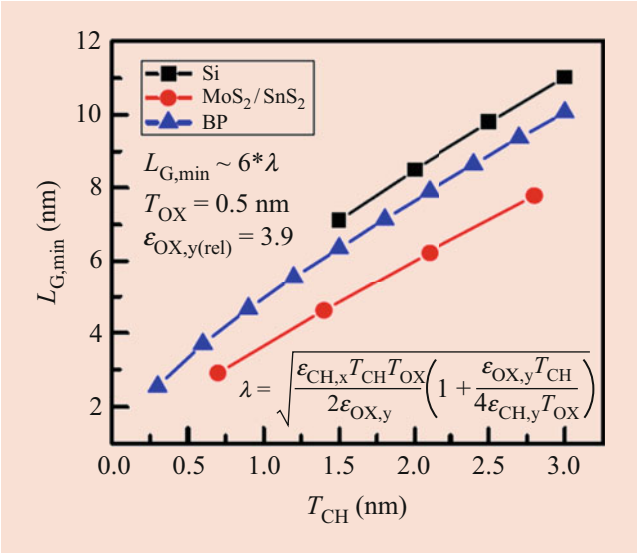

Fig. 9.14 $L_{G,min}$ vs $T_{channel}$ for 2G Si ($\epsilon = 12$), BP ($\epsilon = 9$, $T_{ch} = 0.3$ N), and TMDs ($\epsilon = 4$, $T_{ch} = 0.7$ N) (N = nb of layers)

horizons. The best performances for the swing of CMOS devices at the end of the roadmap (close to 60 mV/dec) are obtained for multi-gate (Ω-Gate in the figure) nanowire FET with very small wire diameter (3 nm) and double-gate MOSFET with TMD (MoS_2 in the figure) channel. However, at the end of the next decade, sub-60 mV/decade swing may be necessary, which are obtainable only with small-slope switches (an example with tunnel FET with III–V or 2D channels in the figure).

To outperform CMOS, these new devices, called the small swing/slope switches (Fig. 9.19), need an I_{on} in the range of

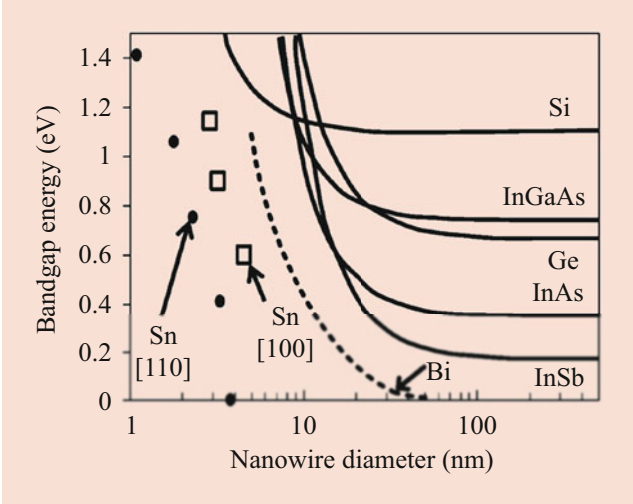

Fig. 9.15 Bandgap as a function of nanowire diameter for various semiconductors and semimetals

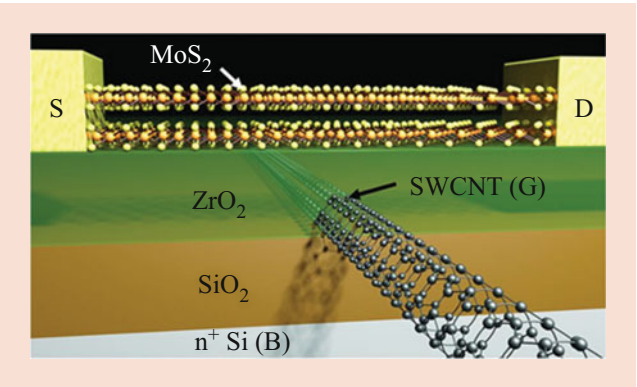

Fig. 9.16 Bilayer MOS_2 1nm gate length controlled by a single-walled carbon nanotube as the gate with ZrO_2 gate oxide

hundreds of μA, an average subthreshold swing far below 60 mV/dec for at least four to five decades of I_d, a ratio I_{on}/I_{off} larger than 10^5, and V_{dd} lower than 0.5 V.

9.3.1 Tunnel FETs

A very interesting option is provided by tunnel FETs exhibiting with source-to-drain tunneling (Fig. 9.20). The same boosters developed for MOSFET can be proposed to boost the performance of TFETs, for which opposite source and drain doping are used (Fig. 9.21). These types of devices are in fact able to overcome the subthreshold swing limit of 60 mV/dec, which is the minimum of MOSFETs at 300 K. Multi-gate, high-k dielectrics, ultra-thin films, alternative materials (Ge, III–V), and strains are leading to improved TFET properties (Fig. 9.21). Numerical simulations demonstrate very good values of the subthreshold swing, showing that low-voltage operation (i.e., in the sub-0.5 V range) is possible, still with small leakage currents. The main challenge is to obtain at the same time high drain currents, which is very difficult experimentally. Therefore, these tunneling devices are very interesting for ultra-low-power operation and low/medium performance.

Figure 9.20 shows the basic operation of a tunnel FET. The tunneling between source, channel, and drain of the TFET, controlled by the gate, allows for low slopes, below 60 mV/dec at room temperature.

The functioning of the TFET devices exploits the interband tunneling that occurs in heavily doped p+n+ junctions; the band bending is controlled by V_g and by a reverse-biased p-i-n junction. The suppression of the ambipolar effect is suppressed by making the transistor structure asymmetric. In order to maximize the band-to-band tunneling, the transmission probability is optimized by reducing the effective tunnel mass m^*, the source bandgap E_g, and/or the tunneling length λ and by increasing the band offset $\Delta\Phi$ between the conduction/valence band of the source/channel, to enhance I_{on} and reduce S for several decades of current.

Optimizing E_g, m^*, and $\Delta\Phi$ requires a change in the materials. In turn, λ can be decreased by a change of device dimension, doping, gate capacitance, gate overlap on tunnel region, and bandgap using a reduced t_{ox} and t_{si}, a high-k gate, an abrupt doping profile, a high source doping, a multi-gate structure, or other materials than Si.

It is also worth noticing that a TFET with a heterostructure is preferable (small bandgap at S and large bandgap at D) and that complementary TFETs are needed for logic circuits.

Figure 9.22a shows the experimental characteristics of SOI TFETs. A very good subthreshold swing down to 42 mV/dec is obtained for p-channel operation [41]. Using SGOI and GOI TFETs yields a strong increase of I_d, up to several thousand times, with respect to SOI transistors (Fig. 9.22b). I_{off} is very low, but I_{on} is only of the order of several μA/μm for the best GOI TFETs, which is very small compared with MOSFETs.

As in the case of MOSFETs, technology boosters can also be used for TFETs. The results obtained by numerical simulation are illustrated in Fig. 9.23, where we can see that short-channel, thin Si film double-gate TFETs with high-k gate dielectrics and stress at the source junction lead to the best performance with a substantial increase of I_{on} and reduction of S [42].

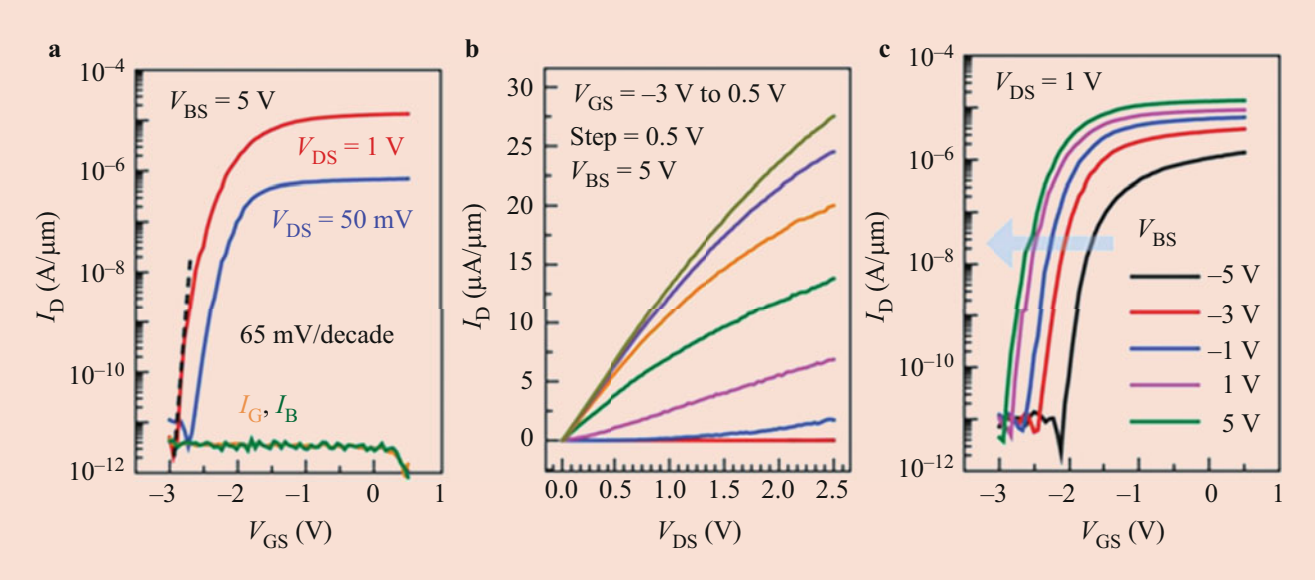

Fig. 9.17 Electrical characterization and TCAD simulations of 1D2D-FET (**a**) I_D–V_{GS} characteristics of a bilayer MoS_2 channel SWCNT gated FET at V_{BS} = 5 V and V_{DS} = 50 mV and 1 V. The positive V_{BS} voltage electrostatically dopes the extension regions n^+. (**b**) I_D–V_{DS} characteristic for the device at V_{BS} = 5 V and varying V_{GS}. (**c**) I_D–V_{GS} characteristics at V_{DS} = 1 V and varying V_{BS} illustrating the effect of back-gate bias on the extension region resistance

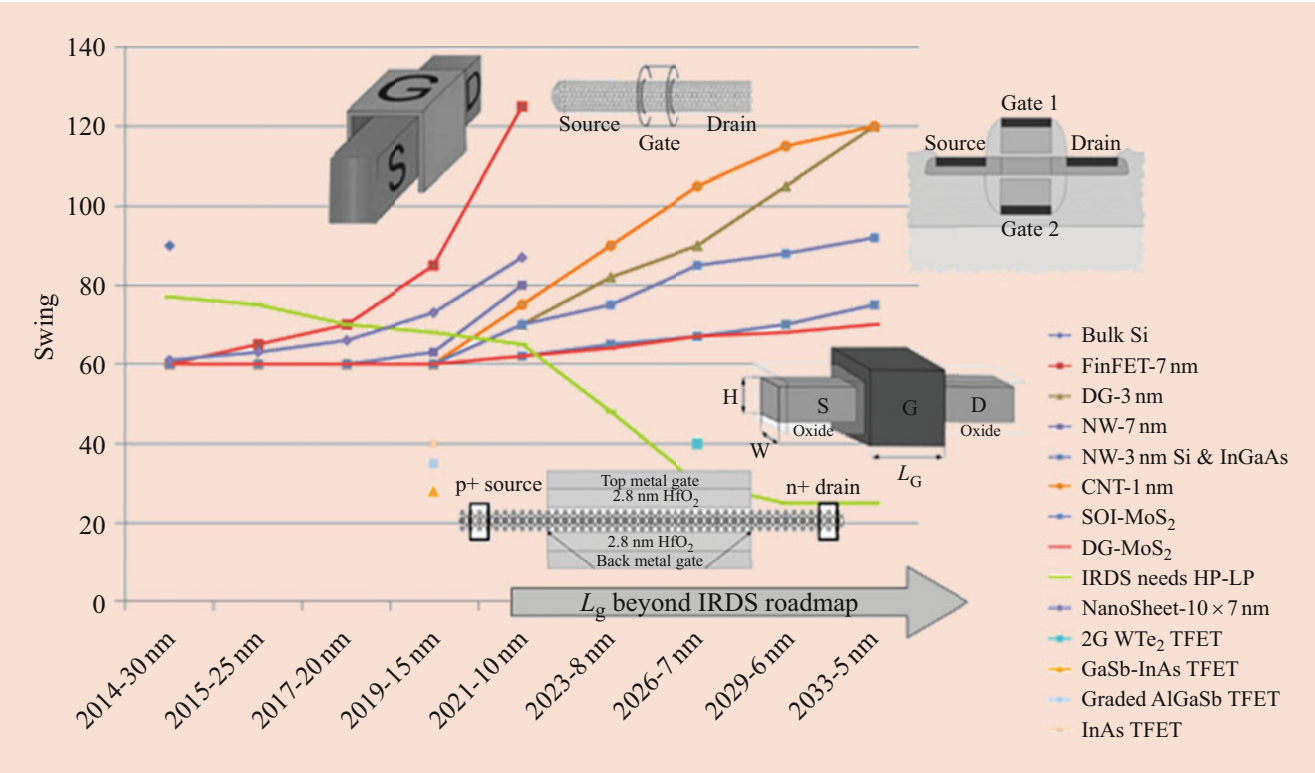

Fig. 9.18 Advanced simulations of subthreshold swing (mV/decade) vs gate length (beyond the IRDS Roadmap for the gate length). Time horizon for various device architectures (bulk Si, FinFET, double gate, nanowire with various diameters, carbon nanotube, MOSFET on insulator, nanosheet) and channel materials (Si, InGaAs, InAs, heterojunction GaSb-InAs, graded AlGaSb, MoS_2, WTe_2), compared with IRDS needs (2017) for the next 15 years

Better performances than those of Ge TFETs have been obtained using GeSn TFETs (Fig. 9.24) that exhibited a strong increase of the I_d along with a substantial reduction of S [43].

Experiments carried out on feedback TFETs [44] and Z2-FET [45], with a forward-biased PiN diode, showed a very small swing (a few mV/dec) along with good driving currents; this happens, however, for biases larger than 0.5 V.

Good performances have also been demonstrated by strained Ge double-gate TFETs with asymmetric S/D structure, exhibiting values of swing down to 50 mV/dec and I_{on} up to 300 μA/μm for high V_d [46]. However, due to the presence of different front- and back-gate oxides, the experiments have been carried out using different biases for the front and back gates; we have shown that an application of V_{g2}/V_{g1} proportional to t_{ox2}/t_{ox1} gives an overestimation of the device performance [47].

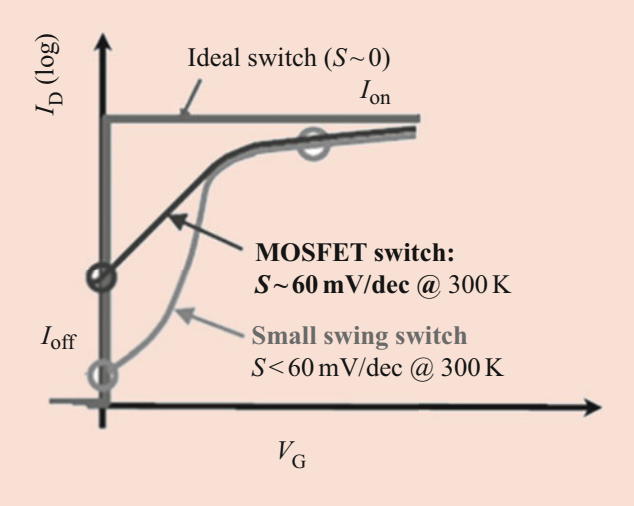

Fig. 9.19 Comparison between the MOSFET switch, the small swing/slope switch, and the ideal switch

Single-gate, double-gate, and GAA InAs TFETs exhibit very good theoretical results (for $V_g = V_d = 0.2$ V), with S lower than 20 mV/dec for small wire diameter (down to 2 nm), thanks to the small effective masses and bandgap of these III–V materials.

For very short gate lengths, small wire diameters are also needed, down to 5 nm or below, as in the case of MOSFETs, in order to obtain a good subthreshold swing (Fig. 9.25) [48].

High performances, with I_d up to 1 mA/μm at low V_d, have been demonstrated by quantum transport simulation on strained InAs NW TFET (Fig. 9.26), the best result being obtained for a biaxial strain [48].

However, if traps are present, the improvements in I_{on} are limited by the degradation of the swing due to trap-assisted tunneling. Both traps and surface roughness can also be a relevant source of device variability for tunnel FETs [49].

The first experimental demonstration of a swing lower than 60 mV/dec (on less than one decade of I_d) using III–V materials has been shown with InGaAs heterojunction 150 nm gate length TFETs using thin EOT and high source doping, with I_{on} of only a few μA/μm [50].

Carbon-based tunnel FETs were the first devices in which S <60 mV/dec was experimentally demonstrated, down to 40 mV/dec, albeit with a very low I_{on} (<1 nA) [51]. The advantages of carbon materials are many, in particular, small effective mass, small and direct bandgap, and excellent elec-

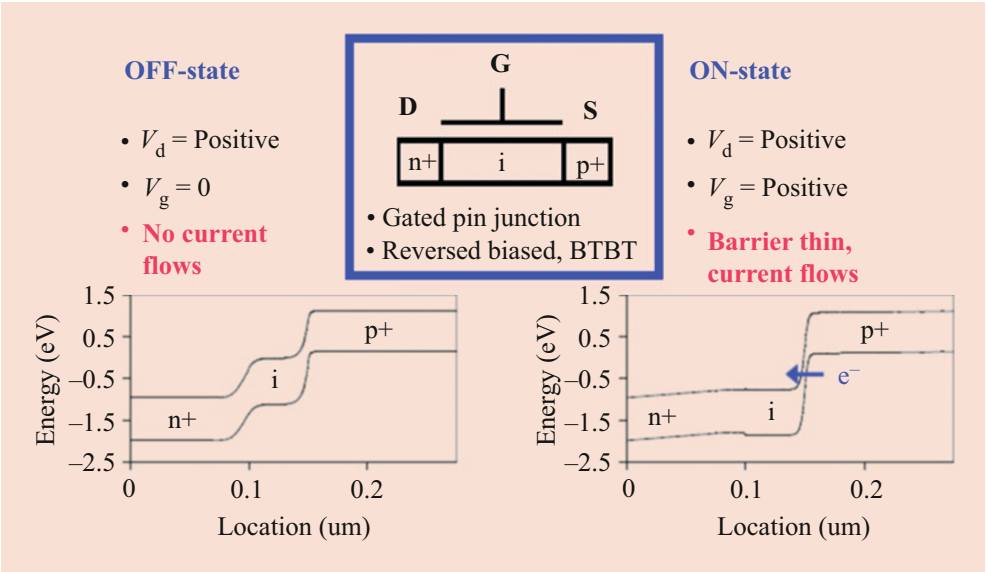

Fig. 9.20 Basic operation of a tunnel field-effect transistor with source-to-drain tunneling

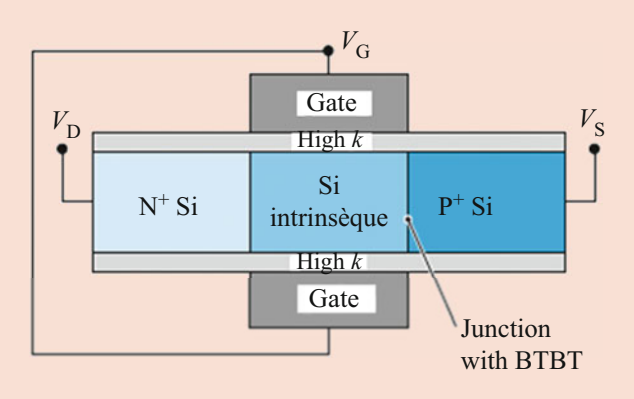

Fig. 9.21 Multi-gate tunnel FET, using source-to-drain band-to-band tunneling, realized with high-k gate dielectrics

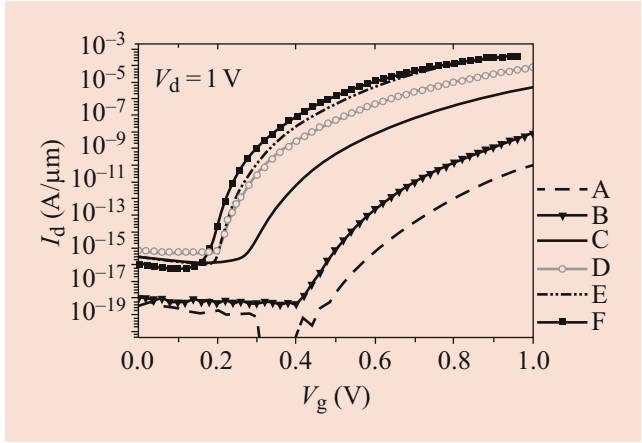

Fig. 9.23 Curves: (A) single-gate SOI, $L_g = 100$ nm, 3 nm SiO_2, (B) 4 GPa stress at source junction, (C) high-k gate dielectrics, (D) double gate, (E) oxide aligned to i-region, (F) $L_g = 30$ nm

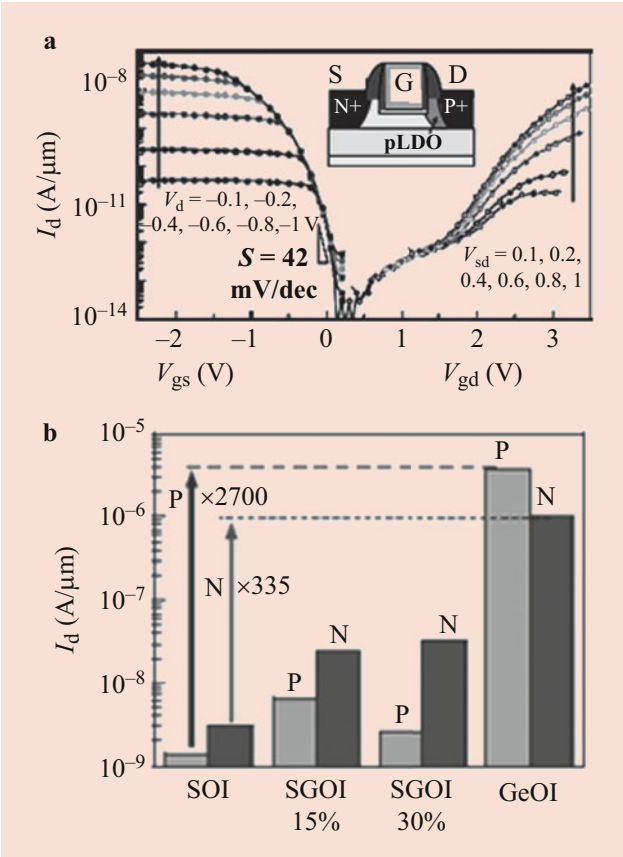

Fig. 9.22 (**a**) Transfer $I_d(V_g)$ characteristics of 100 nm gate length n- and p-channel TFETs ($t_{si} = 20$ nm), (**b**) I_{on} of 400 nm L_g SOI, SGOI and GOI n- and p-TFETs ($t_{SiGe} = 20$ nm, $t_{Ge} = 60$ nm, $V_d = \pm 0.8$ V, $V_g = \pm 2$ V)

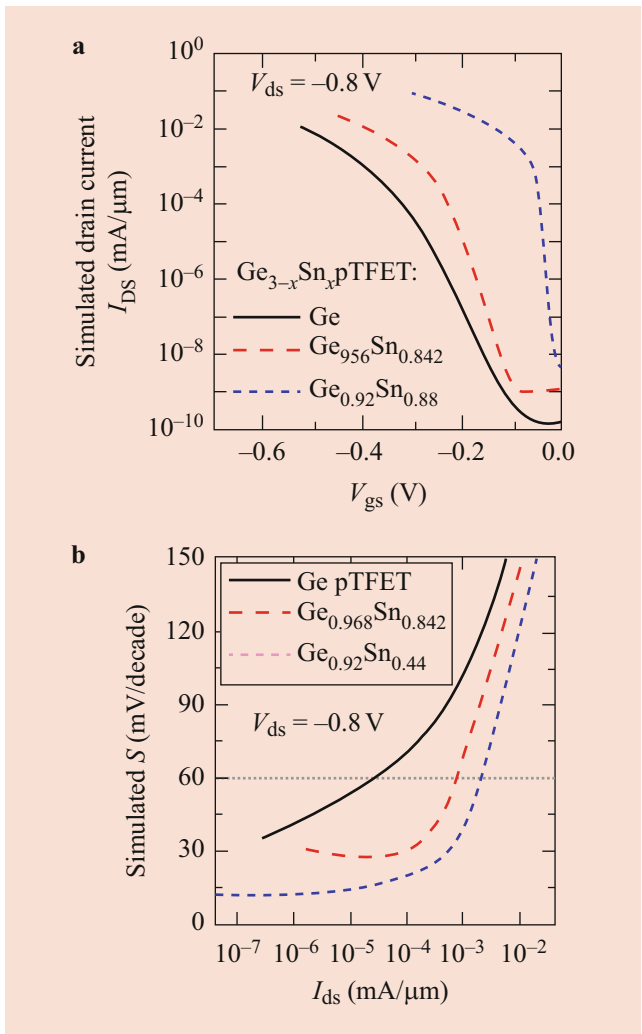

Fig. 9.24 (**a**) Drain current vs gate bias and (**b**) subthreshold swing vs drain current for GeSn TFETs as compared to Ge TFETs obtained by numerical simulation

trostatic control due to thinness of the layers; therefore, such materials could be the best choice. Graphene has similar properties as CNT, but with planar processing compatibility. However, only theoretical studies have been performed up to now. The high potential of graphene nanoribbons or bilayers

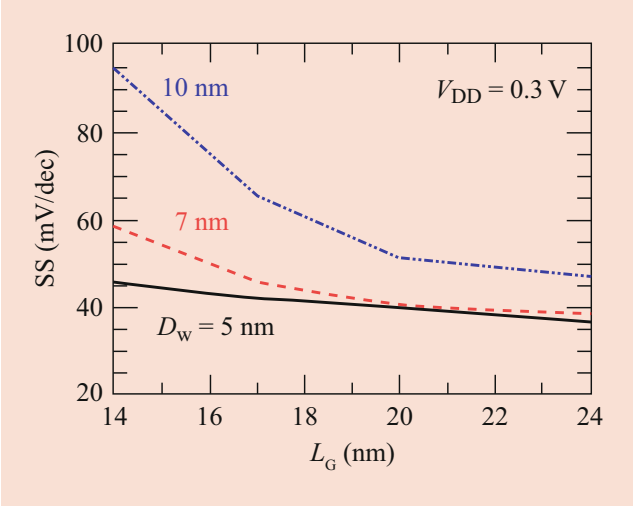

Fig. 9.25 Subthreshold swing vs gate length for GAA InAs nanowire TFETs for various wire diameters obtained by quantum simulation

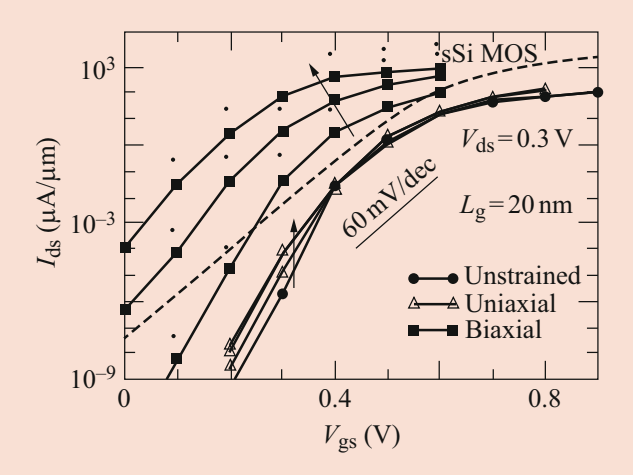

Fig. 9.26 20 nm gate length InAs NW TFET with 5 nm diameter and different strains obtained by quantum simulations

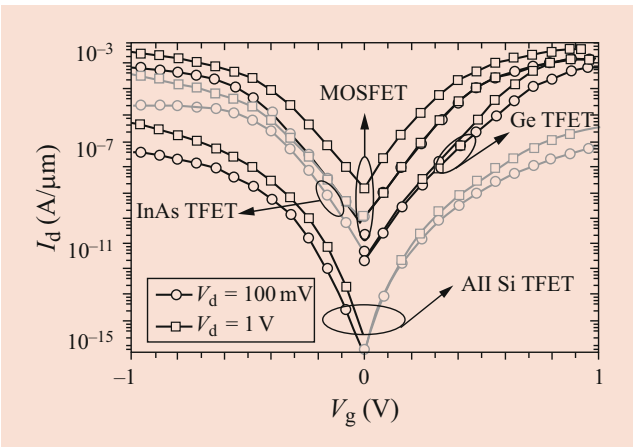

Fig. 9.27 InAs/Ge C-TFETs compared with all-Si TFETs and MOSFETs

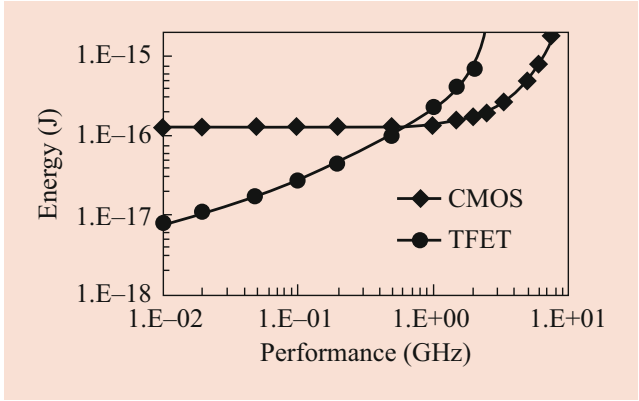

Fig. 9.28 Comparison of energy-frequency between CMOS and TEFT

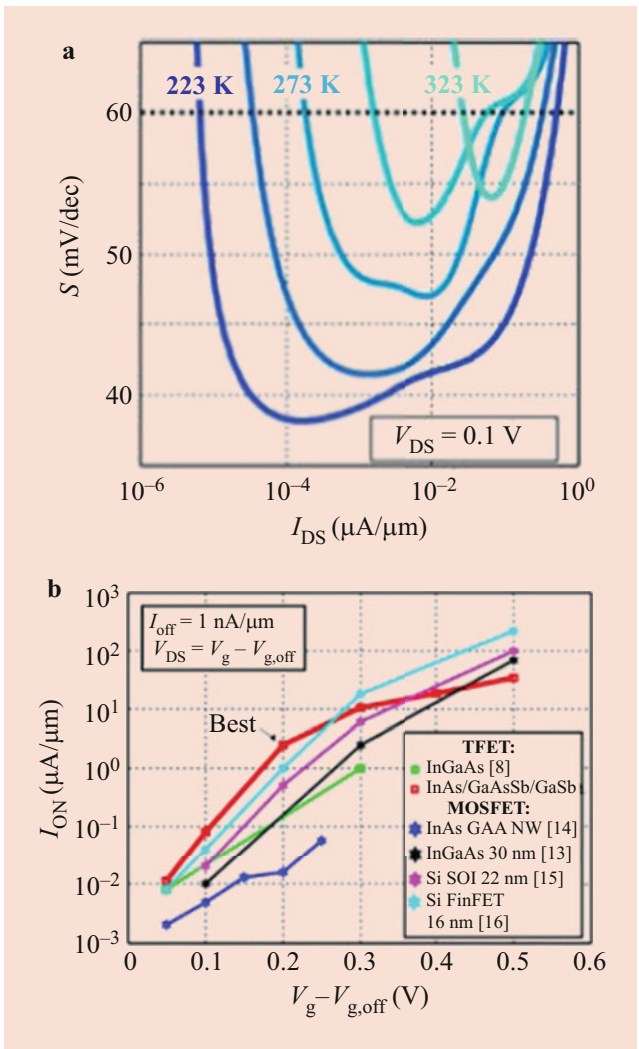

Fig. 9.29 (**a**) Subthreshold swing vs I_{ds} and temperature for InAs/-GaAsSb/GaSb NW TFET (d = 20 nm, L_g ~ 100 nm). (**b**) Driving current vs gate bias for various TFET and MOSFET architectures

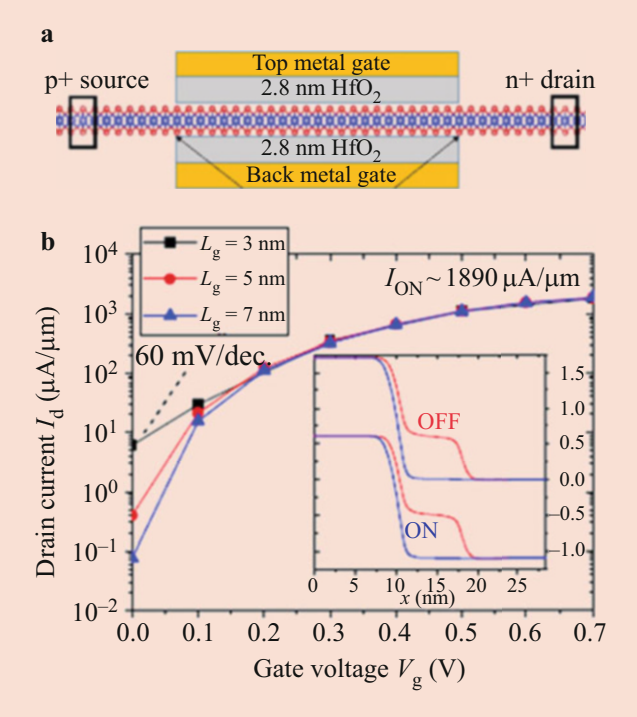

Fig. 9.30 (**a**) Structure and (**b**) $I_d(V_g)$ transfer characteristics of TFET with double-gate WTe_2 layer as a function of L_g (V_d = 0.5 V, S/D doping: 10^{13} cm^{-2})

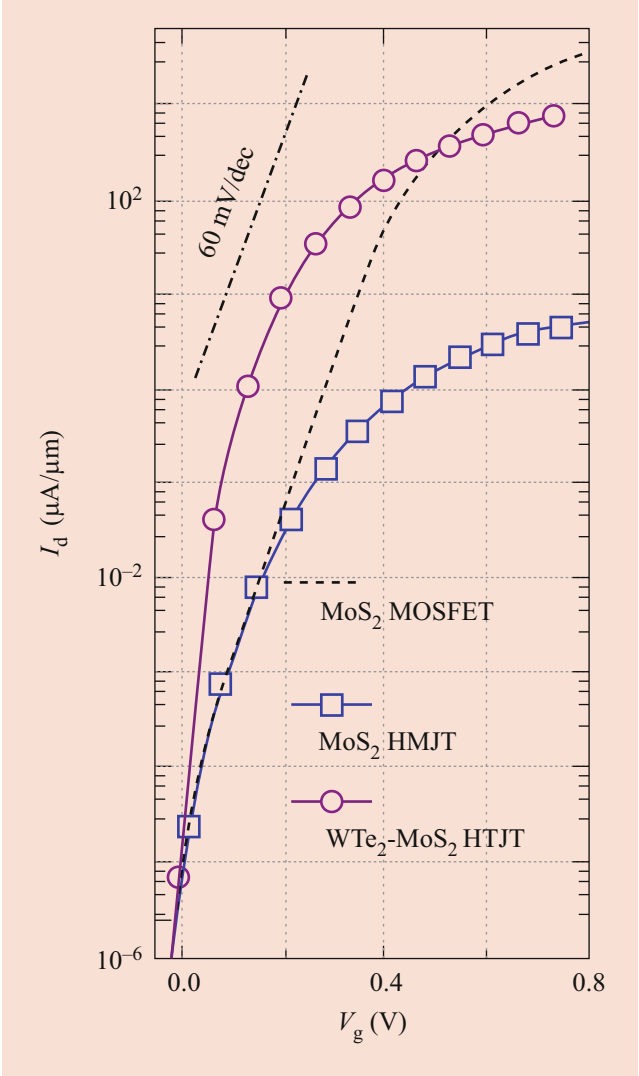

Fig. 9.31 $I_d - V_g$ transfer characteristics for homojunctions MoS_2 and heterojunction WT2-MoS_2 TFETs compared with MoS_2 MOSFET, V_d = 0.5 V, L_g = 12 nm

has been shown by simulation [52] (I_{on}= 100 s of µA/µm, I_{off} = few pA/µm, S = 20 mV/dec, E_{gap} = 200–300 meV, $I_{on}/I_{off} > 10^3$ at V_d = 0.1 V) but has not been replicated experimentally.

The best trade-off obtained by simulation for complementary TFET performance has been shown with Ge/InAs TFETs, leading to an increase of I_d by several hundreds compared to Si TFETs (Fig. 9.27) [53].

However, the experimental results are today very poor compared with numerical simulation. No experimental demonstration of TFET with $I_{on} > 100$ µA/µm and $S < 60$ mV/dec has been shown so far.

Comparisons have been carried out between CMOS and TFET inverters. The Ge/InAs TFET heterostructure showed an abrupt transition from the 1 to the 0 state with the highest differential gain and best noise margins. However, large Miller effects are obtained due to the special capacitance behavior in TFET, leading to larger effective load capacitance and increased delay time. The best power-delay product has been shown so far for CMOS compared with TFETs [54].

Tunnel FETs seem presently better in energy efficiency for applications with frequency lower than 1 GHz (Fig. 9.28) [55].

Recently, a substantial improvement of TFET performance has been experimentally reported in III–V devices using a vertical InAs/GaAsSb/GaSb NW TFET (Fig. 9.29) [56].

The maximum current for which a 60 mV/dec swing is obtained (I_{60}) is 0.056 µA/µm and 0.31 µA/µm at V_{ds} = 0.1 and 0.3 V, respectively, representing an experimental record. The minimum swing is $S_{min} \sim 50$ mV/dec at 300 K (Fig. 9.29a), and the best driving current is obtained for these nanowires for $V_g < 0.25$ V, compared with other TFETs and MOSFETs (Fig. 9.29b).

Very good simulated performances have also been obtained for double-gate 2D TMD TFETs based on WTe_2 [57], WTe_2/MoS_2 heterojunctions [58], and van der Waals-bonded materials [59].

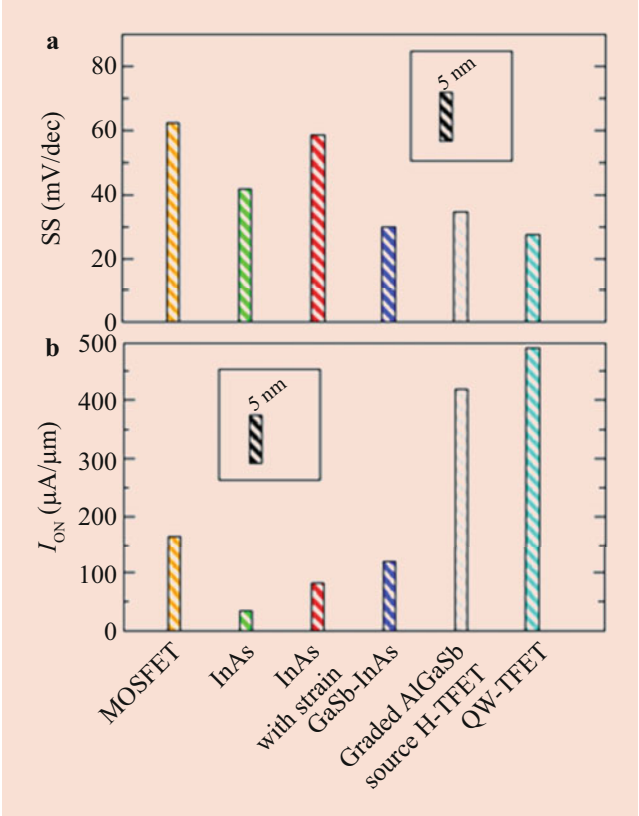

Fig. 9.32 (**a**) Subthreshold slope and (**b**) I_{on} for different nanowire architectures (d = 5 nm, L_g = 17 nm, I_{on} at I_{off} = 5 nA/μm): MOSFET, TFET InAs, TFET InAs with strain, TFET with GaSb-InAs heterostructure, graded source heterostructure TFET with T_{grad} = 5 nm, quantum-well InAs-GaSb-InAs TFET with T_{well} = 3 nm

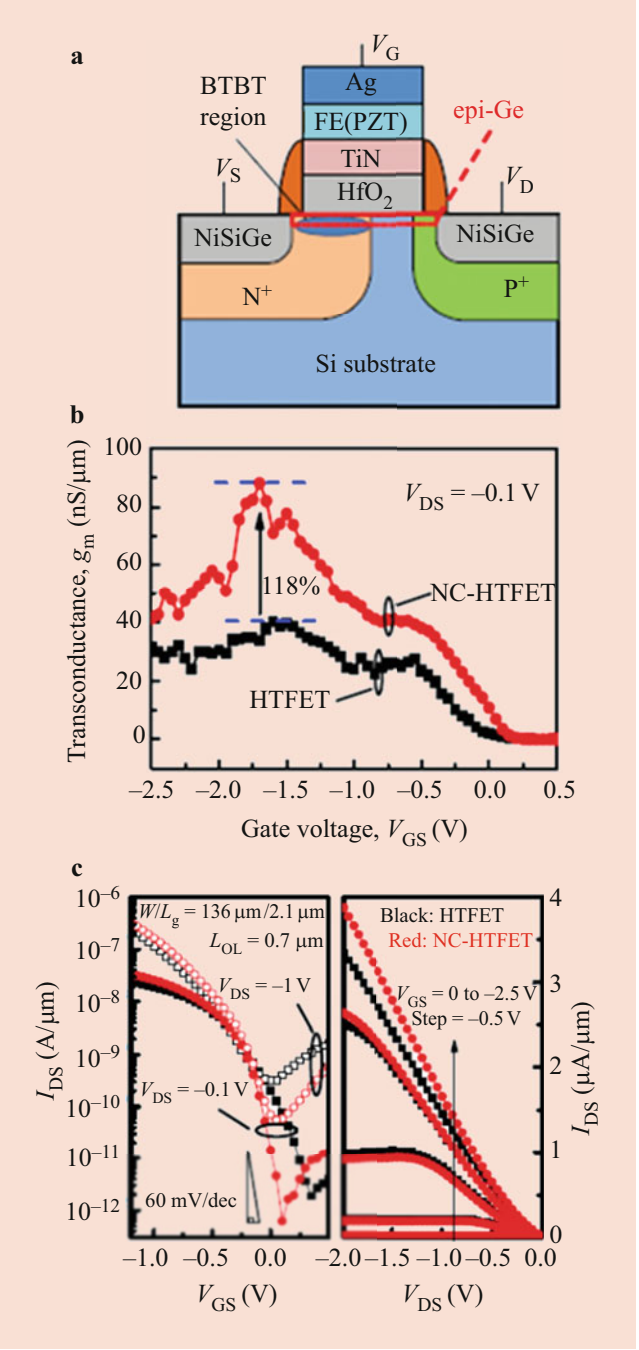

Fig. 9.33 (**a**) Hybrid device FeTFET combining a tunneling transport between source and drain tunneling (TFET) and a ferroelectric gate for improving the subthreshold slope (**c**), the drain current (**c**) at the ON state, and the transconductance (**b**)

The integration limits of TFETs made on a 2D WTe_2 layer have been studied by quantum simulation (Fig. 9.30). A WTe_2 dual-gate TFET shows a possible integration down to 7 nm gate length with very good I_{on}. Below this value, a substantial degradation of the swing results, with a value that goes above 60 mV/dec [57].

The comparison between homojunction and heterojunction 2D TFETs by quantum simulation is shown in Fig. 9.31. The WTe_2-MoS_2 heterojunction leads to a better I_{on} than the homojunction MoS_2 TFET, and a better ON current compared with MoS_2 MOSFET for a gate bias lower than 0.4 V [60], showing the interest of these devices for ultra-low-power operation.

Figure 9.32 shows a comparison, obtained by quantum numerical simulation, of different TFET nanowires made on III–V materials with silicon MOSFET. The best electrical properties are obtained for a quantum-well TFET at the InAs-GaSb-InAs source, leading to a slope of the order of 30 mV/dec and a drain current at the ON state of the order of 500 mA/μm [61]. However, these technologies have to face many challenges, e.g., integration of new III–V materials, innovative architectures of components, and reduction of the densities of defects, in order to eliminate the trap-assisted tunneling that degrades the slope in weak inversion and the current in the ON state.

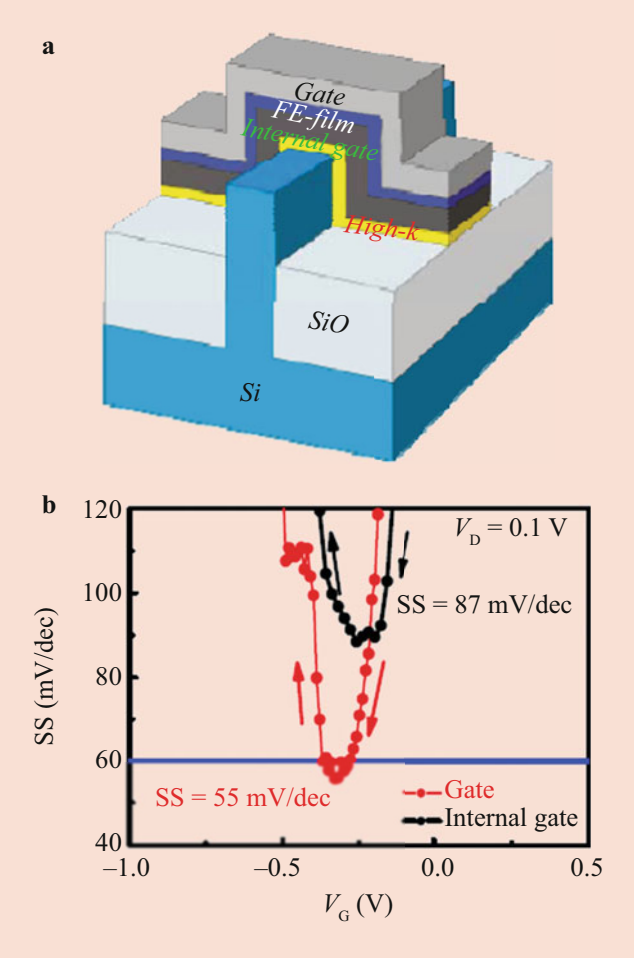

Fig. 9.34 Ferroelectric gate FinFET (**a**) showing a significant improvement of the swing (**b**) compared with traditional FinFET

9.3.2 Ferroelectric Gate Devices

Since it is currently difficult to obtain good experimental performance in drain current at the ON state of tunnel FETs, an interesting option is to combine the tunnel transport between source and drain with a gate using a ferroelectric material, this leading to a possible negative capacitance of the MOS structure. Such a combination significantly improves the subthreshold slope, the drain current, and the transconductance compared to the TFET with a traditional gate (Fig. 9.33) [62].

An improvement in the subthreshold slope, namely, a decrease with respect to the 60 mV/dec limit of traditional MOSFETs, is possible also by combining a ferroelectric gate material and an advanced MOSFET architecture (FinFET), as shown in Fig. 9.34 [63].

Recent experiments have shown that FinFETs using a ferroelectric gate ($HfZrO_2$) and a Ge channel, and therefore a negative capacitance, exhibit a sub-60 mV slope, down to 43 mV/dec, which could lead to larger driving current than TFETs (Fig. 9.35) [64].

SOI MOSFETs realized with PZT and HfO_2/SiO_2 gate in order to obtain a non-hysteretic ferroelectric SOI FET with positive Ctotal have recently been fabricated. A swing down to 20 mV/dec has been found (Fig. 9.36) [65].

9.3.3 Hybrid Devices

Other hybrid devices have also recently shown interesting properties, such as a swing of 4 mV/dec in phase-change

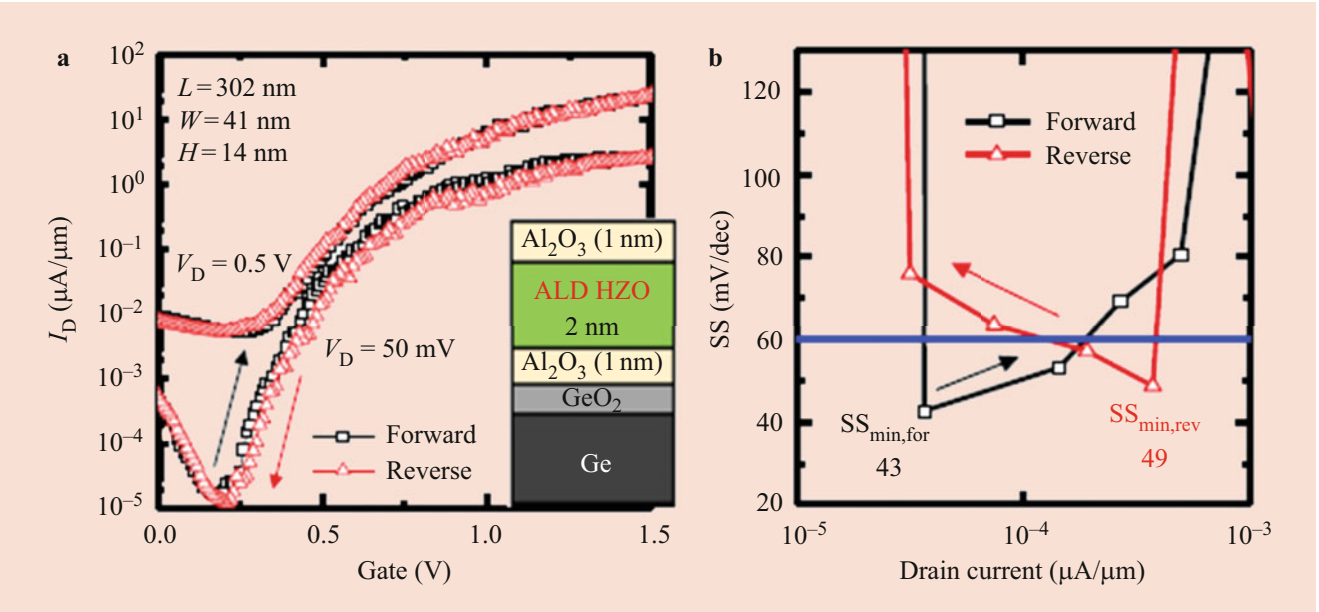

Fig. 9.35 (**a**) Ge channel FE-FET with HfZrO ferroelectric gate showing the transfer characteristics (**b**) and the sub-60 mV/dec subthreshold swing in forward and reverse modes

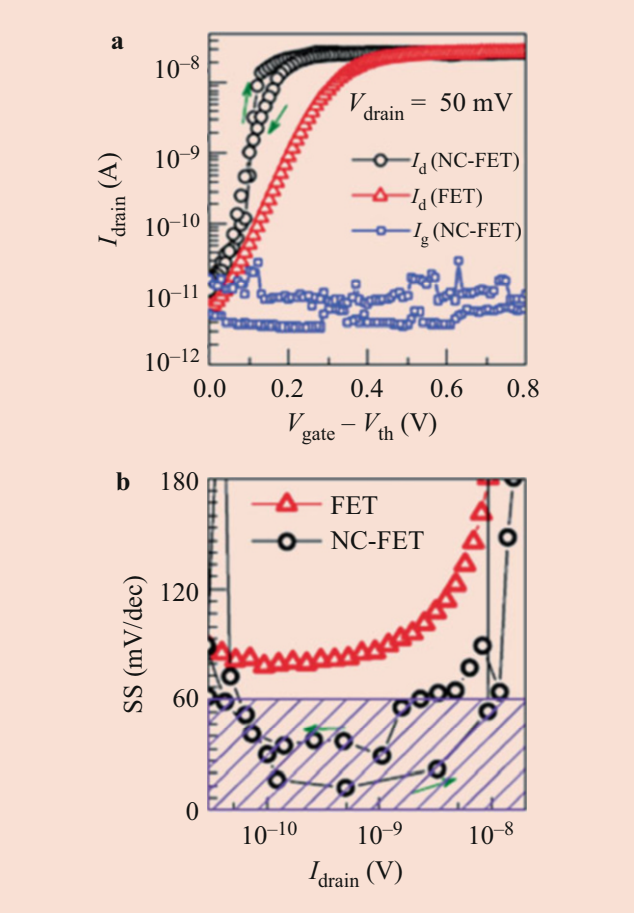

Fig. 9.36 Large surface SOI MOSFET, $t_{si} = 30$ nm, $t_{ox2} = 145$ nm, with PZT + HfO_2/SiO_2 gate for non-hysteretic FE SOI FET with positive C_{total}, (**a**) transfer characteristics, (**b**) subthreshold swing

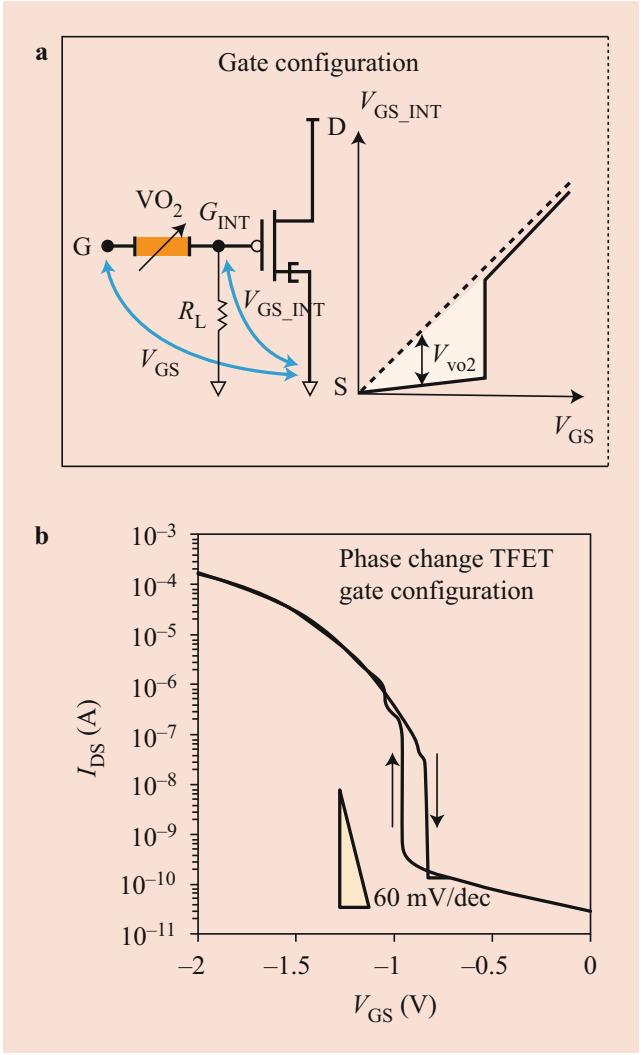

Fig. 9.37 Phase change tunnel FET (**a**) with $S \sim 4$ mV/dec at 300 K for three decades of drain current (**b**), using a vanadium dioxide exhibiting a metal-insulator transition by electrical excitation

TFET with a vanadium dioxide layer in the gate (Fig. 9.37) [66].

Another hybrid device using a metal filament (Ag or Cu) formed at the drain of a Si MOSFET under a sufficiently high applied bias led to a sharp subthreshold swing for several decades of I_d (Fig. 9.38) [67].

9.4 Conclusion

Nanoelectronic devices of future generations face substantial challenges: the most important are increased power consumption, performance saturation, large variability, and reliability limitation. To cope with these challenges, novel materials and innovative architectures are necessary for realizing nanoscale FETs.

This chapter has presented the more promising technologies for advanced materials and devices for the end of the roadmap with multi-gate nanodevices, nanowires, tunnel transistors, ferroelectric FET, and hybrid nanocomponents using, for instance, phase change materials and nanofilament. Other alternative materials, as ultra-thin films, 2D and 1D nanostructures, and heterostructures using strained or III–V materials, also allowing to boost the performance of these advanced nanotransistors, have been described.

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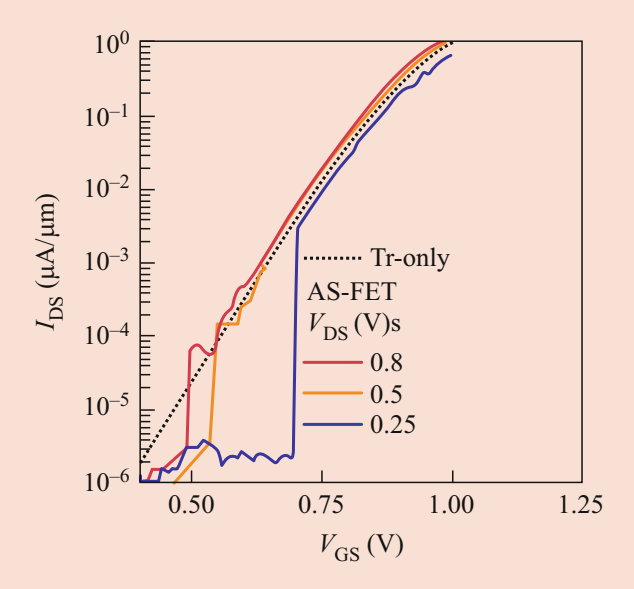

Fig. 9.38 Metal filament (Ag, Cu) formed in Si at the drain with a sufficiently high bias; $S \sim 5$ mV/dec for atom-scale metal filament MOSFET at $V_d = 0.25$ V and 300 K for several decades of I_d

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BALESTRA Francis CNRS Research Director at IMEP-LAHC, has been director of several laboratories, IMEP and LPCS, for a total of 10 years and director of the European Sinano Institute during 6 years. Within FP6, FP7, and H2020, he coordinated several European projects (SINANO, NANOSIL, NANOFUNCTION, NEREID) that have represented unprecedented collaborations in Europe in the field of nanoelectronics. He is member of the AENEAS Scientific Council, of the European Academy of Sciences, of the Advisory Committee of several international journals, and of European Working Groups for Roadmapping activities. He founded (ULIS, WOLTE, INC) or organized many international conferences and has co-authored a large number of books and publications. He is currently vice-president of Grenoble INP, in charge of European activities.

Part II

Basic Devices and Applications

MOS Capacitors, MOS Transistors, and Charge-Transfer Devices

10

Massimo Rudan, Susanna Reggiani, and Giorgio Baccarani

Contents

10.1 Metal-Insulator-Semiconductor Capacitor 332
10.1.1 Surface Potential: p-Type Substrate 333
10.1.2 Relation Between Surface Potential and Gate Voltage 334

10.2 Capacitance of the MOS Structure: p-Type Substrate 336

10.3 Simplified Expression of the Inversion Charge 337
10.3.1 Flat-Band Voltage 338
10.3.2 Quantitative Relations in the MOS Capacitor 339

10.4 MOS Photocapacitor 339

10.5 MOS Capacitor: n-Type Substrate 342

10.6 Insulated-Gate Field-Effect Transistor: MOSFET 343

10.7 n-Channel MOSFET: Current-Voltage Characteristics 343
10.7.1 Gradual-Channel Approximation 345
10.7.2 Differential Conductances and Drain Current, n-Channel 346
10.7.3 MOSFET Theory Including the Subthreshold Current 347

10.8 p-Channel MOSFET: Current-Voltage Characteristics 350
10.8.1 Differential Conductances and Drain Current, p-Channel 350

10.9 Saturation of the Drift Velocity 352
10.9.1 Effective Mobility and Drain-Induced Barrier Lowering 353

10.10 Charge-Transfer Devices 354
10.10.1 Charge-Coupled Devices 354
10.10.2 Transfer Efficiency 356
10.10.3 Charge-Injection Devices 356
10.10.4 Floating-Gate Operation 357

10.11 Applications of CCDs 358
10.11.1 Applications to Analog Filtering 358
10.11.2 Applications to Optical Sensing 359

10.12 Performances of Image Sensors 361
10.12.1 Spatial Resolution 361
10.12.2 Miscellany 362

10.13 Appendix 363
10.13.1 The Poisson Equation in the MOSFET Channel 364
10.13.2 Inversion-Layer Charge and Mobility Degradation 364
10.13.3 Exact Charge Partitioning in the MOS Capacitor 365
10.13.4 Scaling Rules for MOSFETs 366

References 368

Abstract

The chapter has two main parts: the first one addresses the functioning of the MOS capacitor and MOS transistor, considering the case of a p-type substrate. The description of the MOS capacitor is extended to that of the photocapacitor, to be later applied to the case of solid-state imagers. The transistor structure considered in this chapter is simple (i.e., planar); the analysis, however, is carried out in detail, leading to models for the drain current applicable to different functioning regimes of the channel (depletion, weak and strong inversion, saturation). From this, the simpler linear-parabolic model is derived, for both the p- and n-type substrates, necessary to set up the elementary theory of the CMOS inverter. A brief analysis of the scaling rules for MOSFETs is carried out as well.

The second part illustrates the functioning of two important types of charge-transfer devices, CCD and CID, along with some applications, of which the most important are in the field of optical sensing. The architecture of imagers using CCD or CID is illustrated, and different aspects of their performance are analyzed.

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Keywords

MOS architecture · MOS capacitor · MOS photocapacitor · Insulated-gate field-effect transistor · MOS transistor · Charge-transfer devices · Charge-coupled devices · Charge-injection devices · Optical sensors

10.1 Metal-Insulator-Semiconductor Capacitor

The metal-insulator-semiconductor (MIS) capacitor, sketched in one dimension in Fig. 10.1, is the basic ingredient of the field-effect transistor used in the integrated-circuit production. It is also an important tool for investigating the semiconductor-surface properties [1]. The device is realized by placing (using deposition or thermal growth) an insulator layer over a semiconductor substrate; then, the gate and bulk contacts (indicated in the following with the generic term "metal") are deposited onto the insulator and the substrate, respectively.

In the standard silicon technology, the insulator layer is made of thermally grown silicon dioxide: this explains why t_{ox} is the typical symbol for the insulator thickness; accordingly, the insulator permittivity is indicated with ε_{ox}, and the device is called *MOS* capacitor. In fact, silicon dioxide has been used as gate material for decades; in last-generation devices, due to progressive scaling down and to the need of preventing dielectric breakdown and leakage by tunneling, silicon dioxide is being replaced by materials affording larger permittivities (*high-k dielectrics*).

The theory is expounded with reference to a one-dimensional structure, aligned with the x-axis (Fig. 10.1); the semiconductor-insulator interface coincides with the origin. A spatially constant dopant distribution in the semiconductor is considered, and the non-degeneracy and complete-ionization conditions are assumed to hold [2]. The dopant is of the p-type; with suitable changes in the symbols, the analysis carried out here applies also to a semiconductor of the n-type.

With reference to Fig. 10.2, the gate metal, oxide, and semiconductor are initially considered separate from each other and in the equilibrium condition. Symbols E_C^m and E_F^m indicate the lower edge of the conduction band and the Fermi level of the metal; the minimum energy necessary for an electron to transit from the metal into vacuum is the metal work function $W = E_0 - E_F^m$, with E_0 the vacuum level (left part of Fig. 10.2). For an insulator or a semiconductor, the minimum energy necessary for transiting into vacuum (*electron affinity*) is $A^{ox} = E_0 - E_C^{ox}$ or $A = E_0 - E_C$, respectively. When the materials are brought into contact, they form a single, non-uniform system where the Fermi levels align with each other. As the vacuum levels align as well, the bands adapt

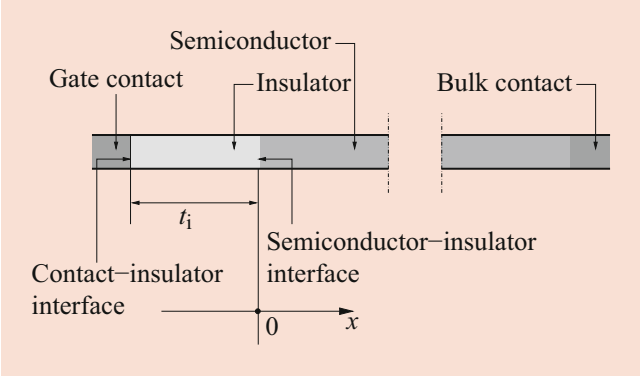

Fig. 10.1 Cross-section of the MIS capacitor (the layer thicknesses are not in scale; after [2])

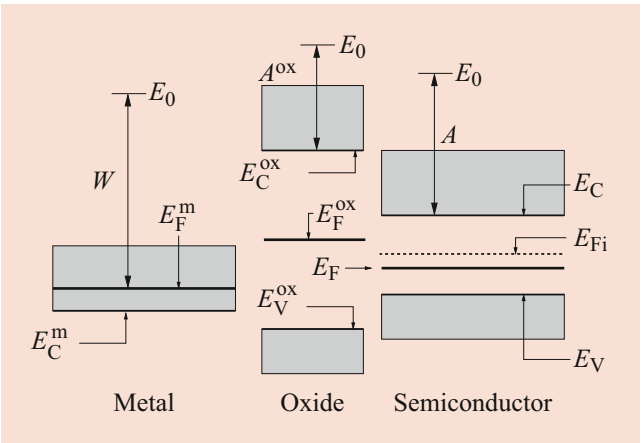

Fig. 10.2 The three materials forming the MOS capacitor shown separately (see text). Symbol E_{Fi} indicates the Fermi level of the intrinsic case. (After [2])

to compensate for a possible charge redistribution occurring when the materials contact each other. The values of W, A in Fig. 10.2 have been selected as to fulfill

$$W - A = E_C - E_F, \tag{10.1}$$

whence, in this case, the bands do not deform; this is visible in Fig. 10.3, representing the situation after the materials have been brought into contact: the bands are everywhere parallel to the Fermi level (*flat-band condition*); as shown later, the more realistic case $W - A \neq E_C - E_F$ is easily incorporated into the analysis.

When the bulk contact is considered, Figs. 10.2 and 10.3 are completed by adding the band structure of the metal on the right of the semiconductor; for simplicity, it is assumed that the gate and bulk contacts are made of the same metal. In the interior of each material, the electric potential is constant due to spatial uniformity, and the electric field is zero.

Let now a voltage V_G be applied between the gate and bulk contacts, such that $V_G > 0$ when the electric potential of the gate contact is larger than that of the bulk contact. In steady-state conditions, the insulator prevents a current from flowing

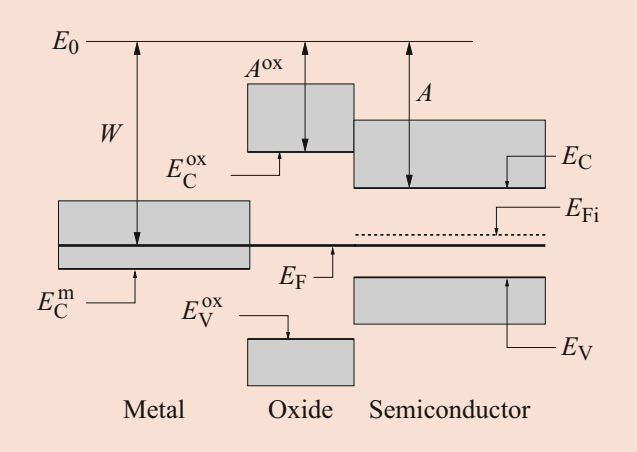

Fig. 10.3 The structure of the MOS capacitor obtained by bringing into contact the three materials of Fig. 10.2. (After [2])

through the device; therefore, during the transient consequent to the application of V_G, the electric charge adjusts itself to the new boundary conditions. At the end of the transient, the device is again in an equilibrium condition, while the form of the bands is different from that of Fig. 10.3. Similarly, the electric potential in the oxide and semiconductor is not constant any longer; its form is found by solving the Poisson equation in each region.

10.1.1 Surface Potential: p-Type Substrate

The solution of the Poisson equation in the uniformly p-doped region is carried out here; the region extension along the x-axis is large, so that, far away from the semiconductor-insulator interface, the semiconductor behaves as if it were isolated. This fixes the carrier-equilibrium concentrations in the bulk; the asymptotic value of the electric potential is set to zero, $\varphi(+\infty) = 0$ whence, remembering that the non-degeneracy and complete-ionization conditions hold, and letting N_A be the constant dopant concentration, it is

$$p^{(0)} = p(+\infty) = p_{p0} \simeq N_A, \quad n^{(0)} = n(+\infty) = n_{p0} \simeq \frac{n_i^2}{N_A}, \tag{10.2}$$

where p and n are the concentrations of holes and electrons, respectively, and n_i is the intrinsic concentration. Indicating the derivatives with primes, the Poisson equation in the semiconductor then reads

$$u'' = \frac{1}{L_A^2} A(u), \qquad A(u) = \frac{n_i^2}{N_A^2} \left[\exp(u) - 1\right] + 1 - \exp(-u), \tag{10.3}$$

with $u = q\varphi/(k_B T)$ the normalized electric potential and $L_A^2 = \varepsilon_{sc} k_B T/(q^2 p_{p0})$, where k_B is the Boltzmann constant, T the lattice temperature, and q the absolute value of the electron charge. The normalized charge density $A(u)$ has the same sign as u; apart from the trivial case where $u = 0$ identically, it is $u' \neq 0$ whence multiplying by u' both sides of the first equation in (10.3) and integrating from $x \geq 0$ to $+\infty$ yield

$$\left(u'\right)^2 = \frac{2}{L_A^2} B(u),$$

$$B(u) = \frac{n_i^2}{N_A^2} \left[\exp(u) - 1 - u\right] + u + \exp(-u) - 1. \tag{10.4}$$

One finds that B is non-negative and u monotonic; the sign of u' is fixed by the boundary condition V_G, which in turn may be either positive or negative. In conclusion,

$$u' = \pm \frac{\sqrt{2}}{L_A} F(u),$$

$$F(u) = \sqrt{\frac{n_i^2}{N_A^2} \left[\exp(u) - 1 - u\right] + u + \exp(-u) - 1}, \tag{10.5}$$

where the sign must be found on a case-by-case basis. Much information is gained directly from (10.5), without the need of another integration. To this purpose, one notes that the electric potential is continuous at the semiconductor-oxide interface; in fact, the normalized charge density in the semiconductor (10.3) has no charge layers in it; hence, it cannot contribute to a double charge layer at the interface. As a consequence, one can adopt the same symbol φ_s for the electric potential at $x = 0$, without distinguishing between the two sides of the interface; φ_s is called *surface potential*, while $u_s = q\varphi_s/(k_B T)$ is the *normalized surface potential*. In contrast, the electric field is discontinuous at the same interface; for this reason, one defines

$$u_s' = \lim_{x \to 0^+} \frac{du}{dx}, \qquad E_s = -\frac{k_B T}{q} u_s', \qquad E_{ox} = -\lim_{x \to 0^-} \frac{d\varphi}{dx}. \tag{10.6}$$

The relation between E_s and E_{ox} is found from the continuity of the electric displacement across the interface and reads

$$\varepsilon_{sc} E_s = \varepsilon_{ox} E_{ox}. \tag{10.7}$$

To find E_{ox}, one observes that in a one-dimensional medium free of charge, the electric potential is linear, whence E_{ox} is given by the negative potential drop across the oxide divided by the oxide thickness t_{ox}. To complete the analysis, it is then necessary to consider the interface between oxide and gate metal. In the interior of the metal, the electric potential is uniform; its value with respect to the metal of the bulk contact is V_G. However, in the solution of the Poisson equation within the semiconductor, the asymptotic condition $\varphi(+\infty) = 0$ has been chosen, which holds inside

the semiconductor region; the surface potential φ_s is referred to such a zero as well. If (10.1) holds, the distinction between bulk contact and bulk semiconductor does not matter because the electric potential is the same; however, in the realistic cases, it is not so, whence V_G and φ_s are referred to two different zeros. Assuming that the interior of the oxide and the semiconductor-oxide interface are free of charge and that the gate and bulk contacts are made of the same material, the difference between the external zero (namely, that within the bulk contact) and the internal zero (given by the asymptotic condition) is the built-in potential Φ_{mp} between the bulk contact and the p-type semiconductor; thus, the gate voltage referred to the internal zero is $V'_G = V_G - \Phi_{mp}$. Also, the electric potential is continuous across the interface between the oxide and the gate metal, because no double layer is present there. In contrast, as $E = 0$ within the metal while $E_{ox} \neq 0$, the electric field is generally discontinuous; in fact, a charge layer of density

$$\rho_m = Q_m \, \delta(x + t_{ox}^-), \tag{10.8}$$

with Q_m the charge per unit area of the metal, builds up at the gate-metal surface. In conclusion, the electric field within the oxide reads

$$E_{ox} = \frac{V'_G - \varphi_s}{t_{ox}}. \tag{10.9}$$

10.1.2 Relation Between Surface Potential and Gate Voltage

Combining (10.5), (10.6), (10.7), and (10.9), one finds

$$C_{ox}\left(V'_G - \varphi_s\right) = \mp \varepsilon_{sc} \frac{k_B T}{q} \frac{\sqrt{2}}{L_A} F(\varphi_s), \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \tag{10.10}$$

where C_{ox} is the *oxide capacitance per unit area* and $F(\varphi_s)$ is obtained by replacing u with $q\,\varphi_s/(k_B T)$ in the second relation of (10.5). The left-hand side of (10.10) is the charge per unit area Q_m in the gate metal. This is easily found by integrating $\mathrm{d}D/\mathrm{d}x = \rho$ across the metal-oxide interface, using (10.8), and observing that the metal interior is equipotential; one finds

$$Q_m = C_{ox}\left(V'_G - \varphi_s\right). \tag{10.11}$$

Due to the global charge neutrality, the following relation holds between the charge per unit area in the gate metal, Q_m, and that within the semiconductor, Q_{sc}:

$$Q_m + Q_{sc} = 0, \qquad Q_{sc} = \int_0^\infty q\,(p - n - N_A)\;\mathrm{d}x = -C_{ox}\left(V'_G - \varphi_s\right). \tag{10.12}$$

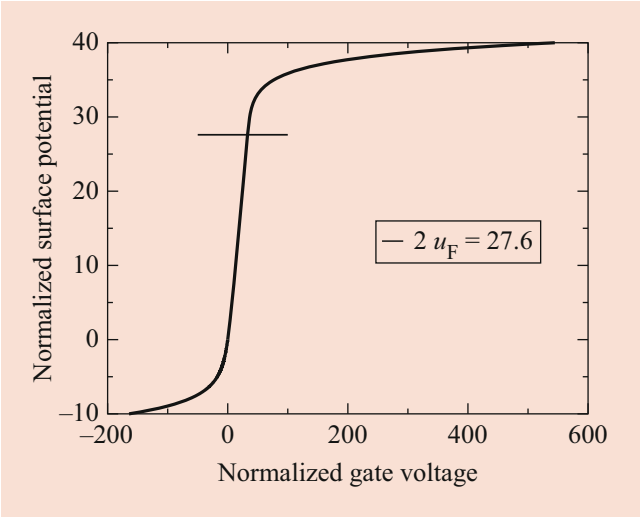

Fig. 10.4 Normalized surface potential u_s in an MOS capacitor with a p-type substrate ($N_A = 10^{16}$ cm^{-3}), as a function of the normalized gate voltage u'_G. (After [2])

In conclusion, (10.10) provides the relation between surface potential and gate voltage. When $\varphi_s = 0$, the electric potential vanishes everywhere in the semiconductor, namely, $V'_G = 0$ corresponds to the flat-band condition. When $V'_G > 0$, the charge in the gate metal is positive; as a consequence, the left-hand side of (10.10) is positive as well, whence $V'_G > \varphi_s$ and the positive sign must be chosen at the right-hand side. The opposite happens when $V'_G < 0$. An example of the $\varphi_s = \varphi_s(V'_G)$ relation is given in Fig. 10.4, showing the normalized surface potential u_s in an MOS capacitor as a function of the normalized gate voltage $u'_G = q\,V'_G/(k_B T)$. The semiconductor's doping is of the p-type with $N_A = 10^{16}$ cm^{-3}, corresponding to $2\,u_F = 2\,q\,\varphi_F/(k_B T) = \log(p_{p0}/n_{p0}) \simeq 27.6$.

The $\varphi_s = \varphi_s(V'_G)$ relation lends itself to identifying different functioning regimes of the MOS capacitor. This identification can be carried out more accurately basing upon the values of the electron and hole concentrations at the semiconductor surface, $n_s = n(x = 0)$ and $p_s = p(x = 0)$. In the non-degenerate conditions considered here, the expressions of the surface concentrations read

$$n_s = n_{p0}\,\exp(u_s) = n_i\,\exp(u_s - u_F), \qquad p_s = p_{p0}\,\exp(-u_s) = n_i\,\exp(u_F - u_s). \tag{10.13}$$

Depending on the value of u_s, several functioning regimes are identified, which are listed in Table 10.1. The regimes' designations are given by comparing the carrier concentrations at the surface with the intrinsic and asymptotic ones. When $u_s < 0$, the majority-carrier surface concentration (holes, in the example used here) exceeds the asymptotic one; the regime is called *accumulation*. When $u_s = 0$, both majority-

Table 10.1 MOS capacitor, p substrate – Functioning regimes (after [2])

Norm. surface potential	Concentrations	Designation
$u_s < 0$	$n_s < n_{p0} < n_i < p_{p0} < p_s$	Accumulation
$u_s = 0$	$n_s = n_{p0} < n_i < p_{p0} = p_s$	Flat band
$0 < u_s < u_F$	$n_{p0} < n_s < n_i < p_s < p_{p0}$	Depletion
$u_s = u_F$	$n_{p0} < n_s = n_i = p_s < p_{p0}$	Mid gap
$u_F < u_s < 2\,u_F$	$n_{p0} < p_s < n_i < n_s < p_{p0}$	Weak inversion
$u_s = 2\,u_F$	$n_{p0} = p_s < n_i < n_s = p_{p0}$	Threshold
$2\,u_F < u_s$	$p_s < n_{p0} < n_i < p_{p0} < n_s$	Strong inversion

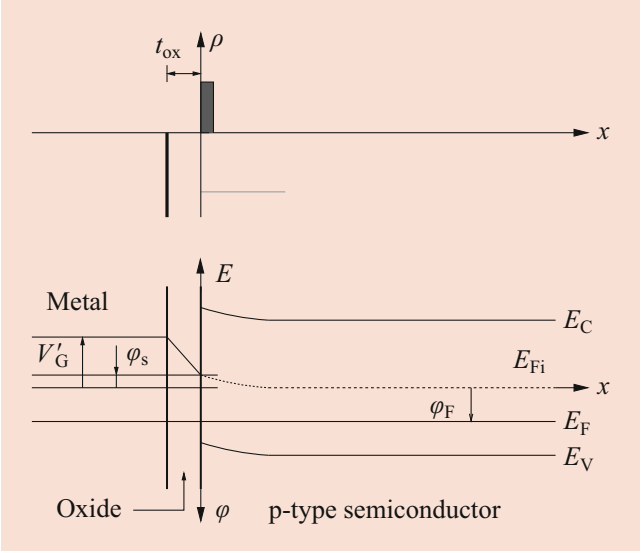

Fig. 10.5 Schematic representation of the charge density and electric potential in a p-substrate MOS capacitor in the accumulation regime. (After [2])

and minority-carrier concentrations equal the corresponding asymptotic concentrations everywhere, and the already-mentioned *flat-band condition* holds. For $0 < u_s < u_F$, the majority-carrier concentration is smaller than the asymptotic one, while the minority-carrier concentration is smaller than the intrinsic one. By continuity, the majority-carrier concentration is smaller than the asymptotic one not only at the semiconductor's surface but also in a finite region of width x_d, which is therefore depleted from carriers; for this reason, the condition $0 < u_s < u_F$ is called *depletion regime*, and x_d is called *depletion width* (the depletion width x_d is conceptually the same thing as the extension l_p of the space-charge region on the p side of a p-n junction; a different symbol is used to avoid confusion in the analysis of the MOSFET (Sect. 10.7)). When $u_s = u_F$, both majority- and minority-carrier concentrations at the surface equal the intrinsic concentration; remembering that in an intrinsic semiconductor the Fermi level practically coincides with the gap midpoint, this regime is called *mid gap*. When $u_F < u_s < 2\,u_F$, the minority-carrier concentration at the surface exceeds that of the majority carriers; however, it is still lower than the asymptotic concentration of the majority carriers: the regime is called *weak inversion*. When $u_s = 2\,u_F$, the surface concentration of the minority carriers equals the asymptotic concentration of the majority carriers, and vice versa; the regime is called *threshold of the strong inversion*, or simply *threshold*. Finally, when $u_s > 2\,u_F$, the minority-carrier concentration at the surface exceeds the asymptotic concentration of the majority carriers, and the regime is called *strong inversion*. In Fig. 10.4, the normalized surface potential at threshold, $2\,u_F$, is marked by the horizontal bar; one notes that in the strong-inversion regime, the surface potential rapidly saturates as the gate voltage increases.

The form of the electric potential and charge density is shown in Fig. 10.5 for the accumulation regime. The upper part of the figure shows the charge density, which is schematically represented by a negative charge layer at the metal-oxide interface and by the thicker, positive layer at the semiconductor-oxide interface. The lower part of the figure shows the electric potential along with the band structure of the semiconductor; note that two different vertical axes are used, in such a way that energy increases upward and the electric potential increases downward. The zero of the electric potential coincides with the horizontal part of the dashed line (in fact, here it is $V'_G < \varphi_s < 0$). The mid-gap condition, $V'_G > 0, \varphi_s = \varphi_F$, is illustrated in Fig. 10.6, whose general description is similar to that of Fig. 10.5; here, the charge layer on the gate metal is positive and balances the negative charge of the semiconductor. Due to the depletion that occurs in the region adjacent to the semiconductor-oxide interface, the charge density is dominated by the contribution from the negative acceptor ions, $\rho \simeq -q\,N_A$. In the figure, the charge density of the semiconductor is schematically indicated by the shaded area that corresponds to a charge per unit area equal to $-q\,N_A\,x_d$. Finally, Fig. 10.7 shows the form of the electric potential and charge density for the threshold condition, $V'_G > 0, \varphi_s = 2\,\varphi_F$. Again, the general description is similar to that of Figs. 10.5 and 10.6; here, there are two contributions to the negative charge of the semiconductor: the first one comes from the negative acceptor ions, whose charge density is schematically indicated by the shaded area of width x_d (note that, due to the larger value of V_G, the depletion width is larger than that of the mid-gap condition). The second contribution to the semiconductor's charge is due to the electrons, whose concentrations at the interface or near it is sufficiently large to be significant; they form a negative layer, called *inversion layer*, whose width, albeit larger than that of the positive layer located at the metal-oxide interface, is much smaller than x_d (the width of the charged layer at the metal-oxide interface is of the order of 1 nm; that of an inversion layer is of the order of 5 nm; an example is given below, with reference to Fig. 10.12).

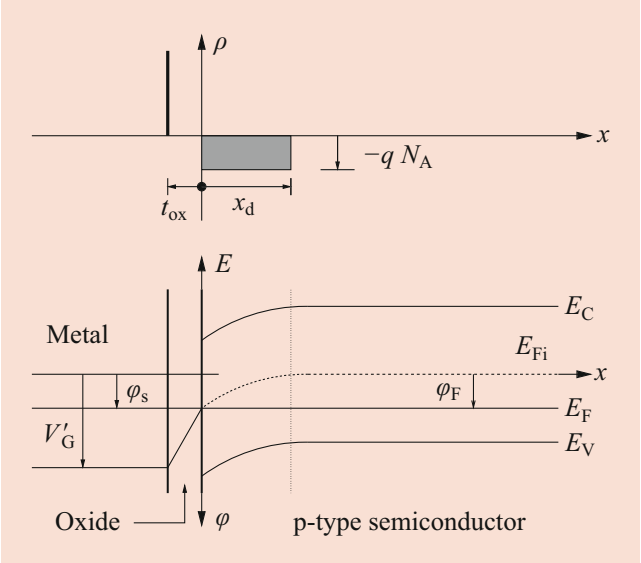

Fig. 10.6 Schematic representation of the charge density and electric potential in a p-substrate MOS capacitor in the mid-gap condition. (After [2])

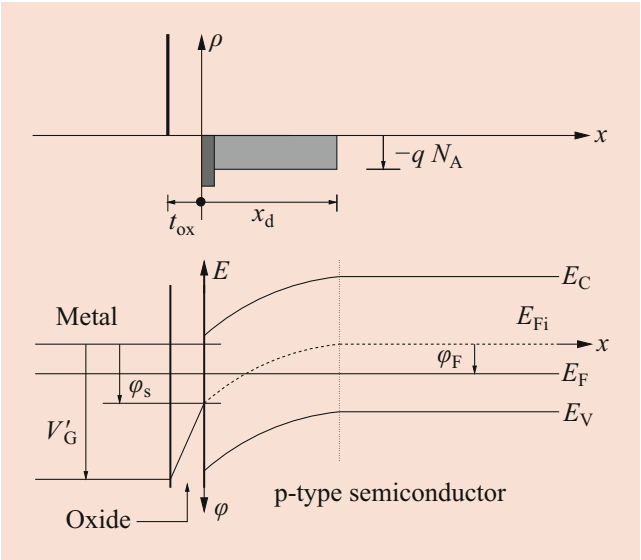

Fig. 10.7 Schematic representation of the charge density and electric potential in a p-substrate MOS capacitor at threshold. (After [2])

Numerical solutions of the semiconductor device model show that, with the exception of the accumulation regime, the semiconductor region of a uniformly doped MOS capacitor can be partitioned into a space-charge and a quasi-neutral region; the quasi-neutral region behaves as a uniform semiconductor, whereas in the volume of the space-charge region, the charge density is essentially dominated by the ionized dopants (with reference to MOS devices, the space-charge region is also called *depleted region*). In the threshold and strong-inversion regimes, also the electrons near the semiconductor-oxide interface give a significant contribution, which must be accounted for; it can be approximated as that of a charge layer at the interface. Considering the range $\varphi_s > 0$ only, namely, excluding the accumulation regime for the p-substrate MOS capacitor, the charge per unit area in the semiconductor is found to be

$$Q_{sc} = \int_0^\infty \rho \, dx \simeq \int_0^{x_d} \rho \, dx \simeq -q \int_0^{x_d} (n + N_A) \, dx = Q_i + Q_b, \tag{10.14}$$

where the first approximation is due to neglecting the charge of the quasi-neutral region and the second one to neglecting the holes in the space-charge region. Quantities Q_i, $Q_b < 0$ are, respectively, the integral of $-q\,n$ and $-q\,N_A$; they are called *inversion charge per unit area* and *bulk charge per unit area*.

10.2 Capacitance of the MOS Structure: p-Type Substrate

The MOS structure exhibits a capacitance C given by

$$C = \frac{dQ_m}{dV_G} = \frac{dQ_m}{dV'_G}, \qquad \frac{1}{C} = \frac{d\left(V'_G - \varphi_s\right) + d\varphi_s}{dQ_m},$$
$$= \frac{1}{C_{ox}} + \frac{d\varphi_s}{d(-Q_{sc})}. \tag{10.15}$$

Like in the case of the depletion capacitance of the *p-n* junction, definition $C = dQ_m/dV_G$ is coherent with the choice of the voltage reference described in Sect. 10.1; the units of C are $[C] = \mathrm{F\,m^{-2}}$. Then, one defines the *semiconductor capacitance per unit area*

$$C_{sc} = -\frac{dQ_{sc}}{d\varphi_s} = -\frac{q}{k_B T} \frac{dQ_{sc}}{du_s} = \pm \frac{\sqrt{2}\,\varepsilon_{sc}}{L_A} \frac{dF}{du_s} > 0, \tag{10.16}$$

where the positive (negative) sign holds for $u_s > 0$ ($u_s < 0$), to eventually find

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{sc}}, \tag{10.17}$$

with $C_{ox} = \text{const}$ and $C_{sc} = C_{sc}(u_s)$. The limiting cases of (10.17) are found from (10.5) and $\exp(-2\,u_F) = n_i^2/N_A^2 \ll 1$, which holds in a *p*-substrate capacitor

$$F \simeq \exp(u_s/2 - u_F), \quad u_s \gg 1,$$
$$F \simeq \exp(-u_s/2), \quad u_s \ll -1, \tag{10.18}$$

$$F^2 \simeq \frac{1}{2}\left[1 + \exp(-2\,u_F)\right] u_s^2 \simeq \frac{1}{2} u_s^2, \qquad F \simeq \pm \frac{u_s}{\sqrt{2}},$$
$$|u_s| \ll 1. \tag{10.19}$$

Then, from (10.16),

$$C_{sc} \simeq \frac{1}{\sqrt{2}} \frac{\varepsilon_{sc}}{L_A} \exp(u_s/2 - u_F), \qquad u_s \gg 1, \tag{10.20}$$

$$C_{sc} \simeq \frac{1}{\sqrt{2}} \frac{\varepsilon_{sc}}{L_A} \exp(-u_s/2), \qquad u_s \ll -1, \tag{10.21}$$

so that

$$C = \frac{C_{ox}\, C_{sc}}{C_{ox} + C_{sc}} \simeq C_{ox}, \qquad |u_s| \gg 1. \tag{10.22}$$

Near the origin, one finds instead

$$C_{sc} \simeq \frac{\varepsilon_{sc}}{L_A}, \qquad |u_s| \ll 1. \tag{10.23}$$

The *flat-band capacitance per unit area* turns out to be

$$C_{FB} = \lim_{u_s \to 0} C = \frac{C_{ox}}{1 + C_{ox}\, L_A/\varepsilon_{sc}} < C_{ox}, \qquad |u_s| \ll 1. \tag{10.24}$$

Examples of capacitance-voltage curves are shown in Fig. 10.8.

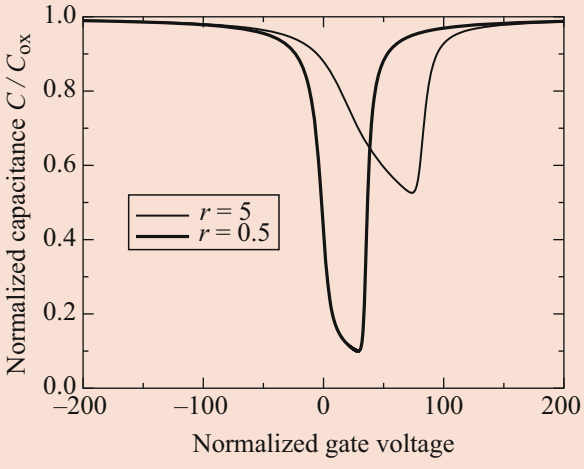

Fig. 10.8 Normalized capacitance C/C_{ox} as a function of the normalized gate voltage u'_G, in a p-substrate MOS capacitor with $N_A = 10^{16}$ cm^{-3}, for different values of $r = \varepsilon_{sc}\, t_{ox}/(\varepsilon_{ox}\sqrt{2}\, L_A)$. (After [2])

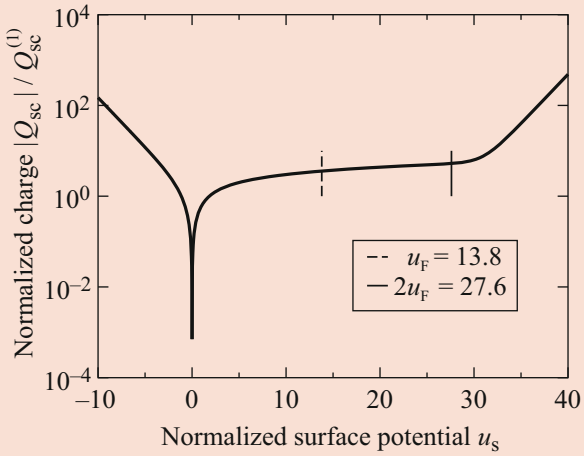

Fig. 10.9 Normalized charge per unit area as a function of the normalized surface potential, in a p-substrate MOS capacitor with $N_A = 10^{16}$ cm^{-3}. (After [2])

10.3 Simplified Expression of the Inversion Charge

A simplified form of the inversion-layer charge of the MOS capacitor is worked out here, to be later applied to the analysis of the MOS transistor. The simplified form holds in all functioning regimes except accumulation. Combining (10.10) and (10.11), one finds for the semiconductor charge per unit area

$$Q_{sc} = \pm Q_{sc}^{(1)}\, F(u_s), \qquad Q_{sc}^{(1)} = \varepsilon_{sc} \frac{k_B\, T}{q} \frac{\sqrt{2}}{L_A}, \tag{10.25}$$

where the negative (positive) sign applies when $u_s > 0$ ($u_s < 0$) and $Q_{sc}^{(1)}$ is the value of Q_{sc} corresponding to $F = 1$. The relation $Q_{sc} = Q_{sc}(u_s)$ is shown in normalized units in Fig. 10.9. The contributions of electrons, holes, and bulk charge to $F^2 = [Q_{sc}/Q_{sc}^{(1)}]^2$ are $\exp(-2\,u_F)\,[\exp(u_s) - 1]$, $\exp(-u_s) - 1$, and $[1 - \exp(-2\,u_F)]\,u_s$, respectively (Fig. 10.10). The first contribution dominates for $u_s > 2\,u_F$, the second one dominates for $u_s < 0$, and, finally, the third one dominates for $0 < u_s < 2\,u_F$.

In a p-substrate capacitor, excluding accumulation entails the inequality $u_s > 0$; thus, an approximation for F is easily derived from (10.5), whose limiting case in the depletion and weak-inversion regimes is $F \simeq \sqrt{u_s}$, $0 < u_s < 2\,u_F$. Combining the latter with (10.25) yields

$$Q_{sc} \simeq -\frac{\sqrt{2}\,\varepsilon_{sc}\, k_B\, T}{q\, L_A} \sqrt{\frac{q\,\varphi_s}{k_B\, T}} = -C_{ox}\,\gamma\,\sqrt{\varphi_s},$$
$$\gamma = \frac{\sqrt{2\,\varepsilon_{sc}\, q\, p_{p0}}}{C_{ox}}, \tag{10.26}$$

where the units of γ are $[\gamma] = \mathrm{V}^{1/2}$. A relation identical to (10.26) is obtained using the full-depletion and the abrupt space-charge edge (ASCE) approximations; in fact, letting $\rho = -q\,N_A$ for $0 < x < x_d$ and $\rho = 0$ for $x > x_d$ (compare, e.g., with Figs. 10.6 and 10.7) yields for $0 < x < x_d$ a simplified form of the Poisson equation, $\varphi'' \simeq q\,N_A/\varepsilon_{sc}$, with boundary conditions $\varphi(x_d) = 0$, $\varphi'(x_d) = 0$; the so-

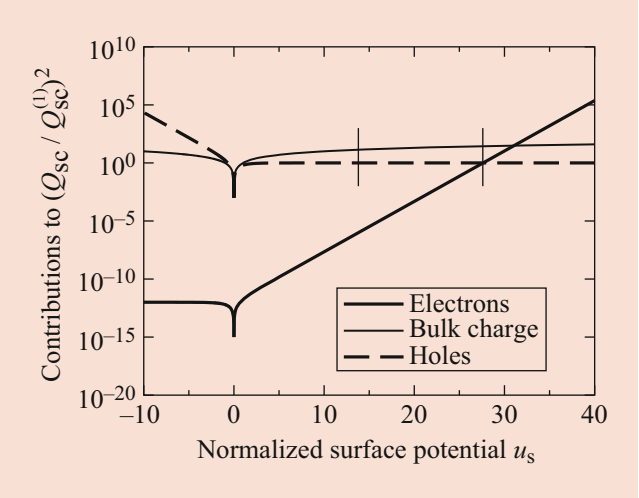

Fig. 10.10 Individual contributions of electrons, holes, and bulk charge to $F^2 = [Q_{sc}/Q_{sc}^{(1)}]^2$, as a function of the normalized surface potential u_s, in a p-substrate MOS capacitor with $N_A = 10^{16}$ cm^{-3}. (After [2])

lution of the simplified form is $\varphi(x) = q\,N_A\,(x - x_d)^2/(2\,\varepsilon_{sc})$. Setting $x = 0$ yields a relation between the surface potential and the depletion width; in turn, in the full-depletion and ASCE approximations, the bulk charge per unit area is $Q_b = -q\,N_A\,x_d$ (Figs. 10.6 and 10.7). In conclusion,

$$\varphi_s = \frac{q\,N_A}{2\,\varepsilon_{sc}}\,x_d^2\,, \qquad Q_b = -q\,N_A\,x_d = -\sqrt{2\,\varepsilon_{sc}\,q\,N_A\,\varphi_s}\,. \tag{10.27}$$

When $0 < u_s < 2\,u_F$, it is $Q_{sc} \simeq Q_b$; as a consequence, the second relation in (10.27), using $N_A \simeq p_{p0}$, coincides with the first one in (10.26). Combining $Q_{sc} \simeq Q_b$ with (10.26) and with the general expression (10.12) yields $V'_G - \varphi_s = \gamma\,\sqrt{\varphi_s}$; inverting the latter and discarding the negative sign in front of the square root yield

$$\sqrt{\varphi_s} = \sqrt{V'_G + (\gamma/2)^2} - \gamma/2\,, \tag{10.28}$$

which applies in the depletion and weak-inversion conditions. The contribution of electrons to the semiconductor charge per unit area, $Q_i = -q\int_0^{x_d} n\,dx$, becomes relevant from the threshold condition on. Like in Sect. 10.1.2, the electron charge is approximated with $-q\,n \simeq Q_i\,\delta(x^+)$, so that the space charge is still considered as entirely due to the ionized acceptor atoms also when $\varphi_s > 2\,\varphi_F$, and (10.27) still holds. From (10.14), one then finds the simplified form of the inversion-layer charge of a *p*-substrate MOS capacitor,

$$Q_i = Q_{sc} - Q_b = -C_{ox}\left[(V'_G - \varphi_s) - \gamma\,\sqrt{\varphi_s}\right] < 0. \tag{10.29}$$

applicable in the depletion, weak-inversion, and strong-inversion conditions (an analysis of the MOS capacitor that avoids partitioning the semiconductor volume into regions is feasible (Sect. 10.13.3), at the expense of the analytical representation).

10.3.1 Flat-Band Voltage

The theory of the previous paragraph must be completed by disposing of the hypothesis on which (10.1) is based and supposing instead that a fixed charge density $\rho_{ox}(x)$ is present in the oxide. This gives the Poisson equation the form $-\varepsilon_{ox}\,\varphi'' = \rho_{ox}$, whence

$$C_{ox}\,(V'_G - \varphi_s) = -\varepsilon_{ox}\,\varphi'(-t_{ox}^+) - Q_{ox}, \qquad Q_{ox} = \int_{-t_{ox}}^{0} \frac{\xi}{t_{ox}}\,\rho_{ox}(\xi)\,d\xi\,, \tag{10.30}$$

with $\varphi(0) = \varphi_s$ and $\varphi(-t_{ox}) = V'_G$. Combining with $-\varepsilon_{ox}\,\varphi'(-t_{ox}^+) = Q_m$ yields $Q_m = C_{ox}\,(V'_G + Q_{ox}/C_{ox} - \varphi_s)$, and, from $V'_G = V_G - \Phi_{mp}$, it finally follows

$$V'_G + \frac{Q_{ox}}{C_{ox}} = V_G - V_{FB}\,, \qquad V_{FB} = \Phi_{mp} - \frac{Q_{ox}}{C_{ox}}\,, \tag{10.31}$$

with V_{FB} the *flat-band voltage*. The designation is due to the fact that letting $V_G = V_{FB}$ establishes the flat-band condition in the semiconductor. If a fixed layer of charge is also present in the oxide, in addition to ρ_{ox}, its effect on V_{FB} is readily incorporated by adding to ρ_{ox} a term of the form $Q_f\,\delta(x - h)$, with Q_f the charge per unit area of the layer and h its position.

Definition (10.31) of V_{FB} does not account for the fact that, besides the fixed charge, mobile charges may be present within the oxide or at the semiconductor-oxide interface. The mobile charges within the oxide make V_{FB} unstable, whence the threshold voltage (10.82) or (10.121) of the MOS transistor becomes unstable as well. The charge at the semiconductor-oxide interface is due in turn to a distribution of interfacial electronic states, called *surface states*, whose energy belongs to the band gap. Such states are due to the disruption of periodicity caused by the finiteness of the crystal size. In a bare silicon crystal, the surface concentration of surface states turns out to be equal to that of the atoms themselves [2]; in silicon, the latter is about $(5.0 \times 10^{22})^{2/3} \simeq 1.36 \times 10^{15}$ cm^{-2}. When the semiconductor-oxide interface is considered, instead, the concentration of surface states is much smaller; the typical figures for the silicon-oxide interface range from 10^9 to 10^{11} cm^{-2}, depending on the quality of the oxide-growth process and on the subsequent annealing steps.

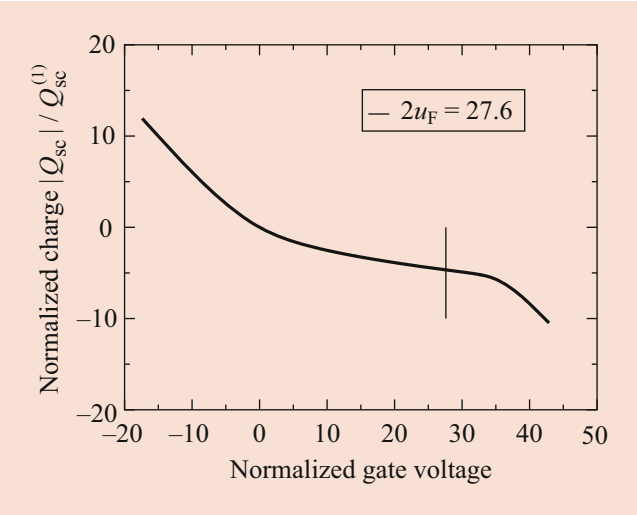

Fig. 10.11 Normalized semiconductor charge $Q_{sc}/Q_{sc}^{(1)}$ as a function of the normalized gate voltage u'_G, for a p-substrate MOS capacitor with $N_A = 10^{16}$ cm^{-3}. (After [2])

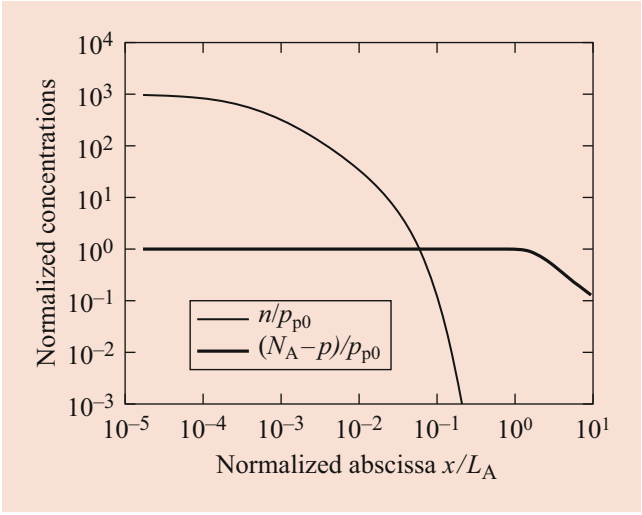

Fig. 10.12 Normalized concentrations n/p_{p0} and $(N_A - p)/p_{p0}$ as a function of position x/L_A, for a p-substrate MOS capacitor with $N_A = 10^{16}$ cm^{-3} in strong inversion ($u_s = 2.5\, u_F$). (After [2])

In the following, it is assumed that the effect of the mobile charges described here is negligible. Also, the analysis carried out in this section shows that the presence of a fixed charge density ρ_{ox} merely shifts V'_G by a constant amount. For this reason, from now on, symbol V'_G will be given the more general meaning $V'_G = V_G - V_{FB}$.

10.3.2 Quantitative Relations in the MOS Capacitor

In the p-type silicon substrate considered so far in the examples, it is $p_{p0} \simeq N_A = 10^{16}$ cm^{-3} and, at room temperature, $n_i \simeq 10^{10}$ cm^{-3}. In turn, the asymptotic minority-carrier concentration is $n_{p0} = n_i^2/N_A \simeq 10^4$ cm^{-3}; it follows $\exp(-2\,u_F) = n_{p0}/p_{p0} \simeq 10^{-12}$ and, as shown, e.g., in Fig. 10.4, $2\,u_F \simeq 27.6$. Using $k_B\,T/q \simeq 26$ mV then yields $2\,\varphi_F \simeq 0.72$ V. As $\varepsilon_{sc} \simeq 11.7 \times 8.854 \times 10^{-14} = 1.036 \times 10^{-12}$ F cm^{-1}, one finds

$$L_A = \sqrt{\frac{\varepsilon_{sc}\, k_B\, T}{q^2\, p_{p0}}} \simeq 4.1 \times 10^{-2}\,\mu\text{m}, \tag{10.32}$$

$$Q_{sc}^{(1)} = \frac{\sqrt{2}\,\varepsilon_{sc}\, k_B\, T}{q\, L_A} = \sqrt{2\,\varepsilon_{sc}\, k_B\, T\, p_{p0}} \simeq 9.3 \times 10^{-9}\ \text{C cm}^{-2}. \tag{10.33}$$

The relation $Q_{sc}(V'_G)$ is found from $Q_{sc} = -C_{ox}\,[V'_G - \varphi(V'_G)]$, where $\varphi(V'_G)$ is obtained from (10.10). The result is shown in normalized form in Fig. 10.11.

The results obtained so far have been obtained without the need of integrating (10.4). The result of a numerical integration of (10.4) is shown in Fig. 10.12, where the dependence on position of n and $N_A - p$ is drawn for a p-substrate MOS capacitor with $N_A = 10^{16}$ cm^{-3} in the strong-inversion regime ($u_s = 2.5\, u_F$). The term $(N_A - p)/p_{p0}$ is significant in a surface region of the semiconductor, whose thickness is several units of x/L_A. The term n/p_{p0} is much larger, but only in a much thinner region near the surface. If the width of the inversion layer is conventionally taken at the intersection between the two curves of Fig. 10.12, which occurs at $x/L_A \simeq 0.1$, one finds from (10.32) a width of about 5 nm.

With reference to Fig. 10.2, and using aluminum as metal and silicon as semiconductor, one has [3, Sect. 8.1] $W = 4.1$, $A = 4.05$, and $A^{ox} = 0.95$ eV. The band gap of the thermally grown silicon dioxide is about 9 eV.

10.4 MOS Photocapacitor

The operation of the *MOS photocapacitor* is readily described basing on the analysis of the MOS capacitor carried out in Sect. 10.1. The device is sketched in Fig. 10.13, where the case of a uniform, p-substrate capacitor is considered with a constant concentration N_A of acceptor dopants. For simplicity, a one-dimensional structure is analyzed, with a partially transparent contact. The incoming radiation is described by the arrows, while the black dots indicate the electrons, and the white dot indicates a hole. The resistor shown in the figure stands for the input resistance of the circuit measuring the device current.

The gate voltage $V(t)$ periodically alternates between V_{FB} and a value V_{GI} that would correspond to strong inversion in a steady-state condition. The duration T_s along which the gate voltage equals V_{FB} is termed *sampling time*, while

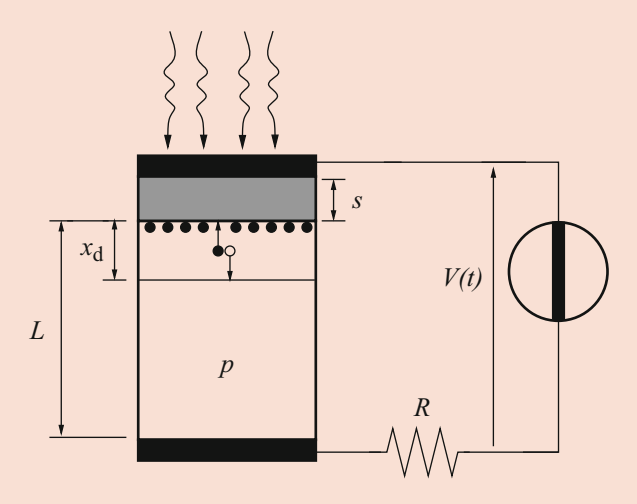

Fig. 10.13 One-dimensional sketch of the MOS photocapacitor with a uniform, p-type substrate. The relative thicknesses of the different layers shown in the figure are not realistic. (After [2])

integration time is the duration T_i along which it equals V_{GI}. It is assumed that at the beginning of the integration time, the earlier transients have vanished, so that the net local charge is negligible (this charge would be exactly zero if the illumination were missing). When the gate voltage switches from V_{FB} to V_{GI}, the majority carriers (holes) are pushed away from the semiconductor-insulator interface, and a depleted region of width x_d is formed in a negligible time; the inversion-layer charge Q_i is not present yet, so that, combining (10.27) with (10.28), one finds

$$x_d = \sqrt{\frac{2\,\varepsilon_{sc}}{q\,N_A}\,\varphi_s}\,, \qquad \sqrt{\varphi_s} = \sqrt{V_{GI} - V_{FB} + (\gamma/2)^2} - \gamma/2. \tag{10.34}$$

The value (10.34) of x_d is considerably larger than the one that would correspond to the equilibrium condition; in fact, the inversion layer is still missing. This layer builds up during the integration time, made of the combined contributions of thermal and optical generations in the depleted region; thus, x_d gradually decreases, while the modulus of Q_i increases. When the applied voltage is switched back to V_{FB}, the holes flood the depleted region and make it to disappear in a negligible time, without affecting the inversion layer. The disappearing of the depleted region makes the electric field to vanish, so that the electrons of the inversion layer start diffusing toward the substrate; in parallel, they recombine with the holes, this giving origin to a current in the external circuit. For typical operating conditions, the contribution of optical generation to the inversion layer dominates over thermal generation; thus, the measured current is essentially due to the illumination, while the effect of thermal generation is to be considered as a noise superimposed to the signal.

An estimate of the sampling time is important. For this, one solves the electron-continuity equation in one dimension,

$$\frac{\partial n}{\partial t} + \frac{n - n_{p0}}{\tau_n} - \frac{1}{q}\,\frac{\partial J_n}{\partial x} = G_s\,\exp(-k\,x)\,, \tag{10.35}$$

assuming that the weak-injection condition applies and that the absorption coefficient k is constant. The coefficient G_s of the optical-generation term reads $G_s = \eta\,\Phi_B\,k\,\exp(-k\,s)$, with Φ_B the photon-flux density on the inside edge of the contact-oxide interface and $\exp(-k\,s)$ a factor accounting for the absorption within the oxide, whose thickness is s (the origin is placed at the semiconductor-oxide interface). The excess charge Q per unit area at time t is found by integrating the minority-carrier excess concentration $n - n_{p0}$ over the semiconductor thickness L; in calculating the integral, one lets $J_n(x = 0) = 0$ due to the presence of the oxide and $J_n(L) \simeq J_n(\infty) = 0$ due to the large extent of L: in conclusion,

$$\frac{\mathrm{d}Q}{\mathrm{d}t} + \frac{Q}{\tau_n} = q\,\frac{G_s}{k}\,, \qquad Q = \int_0^L q\,\left(n - n_{p0}\right)\,\mathrm{d}x. \tag{10.36}$$

Let $t = 0$ be the instant at which the gate voltage V_G is brought from $V_G(0^-) = V_{GI}$ to $V_G(0^+) = V_{FB}$; when integrating (10.36), one observes that the minimum period of variation of Φ_B is large with respect to τ_n, so that G_s is taken constant. One finds

$$Q(t) - q\,\tau_n\,\frac{G_s}{k} = \left[Q_0 - q\,\tau_n\,\frac{G_s}{k}\right]\,\exp(-t/\tau_n)\,, \tag{10.37}$$

with Q_0 the excess minority charge per unit area at $t = 0$. This result shows that the approach to the asymptotic condition is dominated by the minority-carrier lifetime τ_n; note that in the asymptotic limit, the excess charge does not vanish; in fact, it is $Q(\infty) = q\,\tau_n\,G_s/k$. The process is considerably shortened if the photocapacitor is built within a p-type epitaxial layer of thickness a grown over an n-type substrate (Fig. 10.14): the heavily doped n^+ substrate behaves like a contact, and the excess charge vanishes in the much shorter time during which the electrons diffuse across a. As in this case the asymptotic condition $J_n(L) = 0$ does not hold any more, the time decay of Q is found by solving the continuity equation in the form

$$\frac{\partial n}{\partial t} + \frac{n - n_{p0}}{\tau_n} - D_n\,\frac{\partial^2 n}{\partial x^2} = G_s\,\exp(-k\,x)\,, \tag{10.38}$$

whose initial condition reads $n(x, 0) - n_{p0} = Q_0\,\delta(x^+)$. In (10.38), the drift term of J_n is neglected due to the vanishing of the electric field discussed above. The boundary condition at $x = 0$ is $\partial n/\partial x = 0$ at all times, equivalent to $J_n(0) = 0$, while the boundary condition at $x = a$ is $n(a, t) = n_{p0}$ because the heavily doped substrate acts as a contact. Letting $f = (n - n_{p0})\,\exp(t/\tau_n)$ transforms (10.38) into

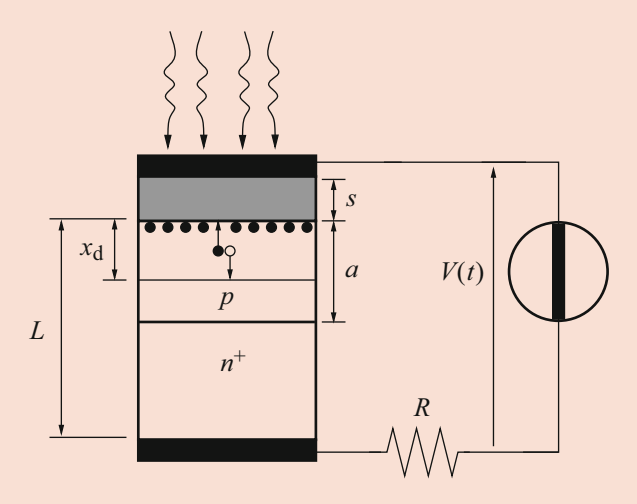

Fig. 10.14 One-dimensional sketch of the MOS photocapacitor built in a p-type epitaxial layer. The relative thicknesses of the different layers shown in the figure are not realistic. (After [2])

$$\frac{\partial f}{\partial t} = D_\mathrm{n}\,\frac{\partial^2 f}{\partial x^2} + G_\mathrm{s}\,\exp(-k\,x + t/\tau_\mathrm{n})\,, \tag{10.39}$$

whose initial condition is $f(x,0) = Q_0\,\delta(x^+)$, while the boundary conditions are $\partial f/\partial x = 0$ and $f(a,t) = 0$. The solution of (10.39) is found by Fourier expanding the unknown: let ω be a function defined in $-2\,a \le x \le 2\,a$ and even in such an interval: $\omega(-x,t) = \omega(x,t)$; also, let $\omega(x,t) = f(x,t)$ in the interval of interest, $0 \le x \le a$. Due to the evenness of ω, one writes

$$\omega = \sum_{k=0}^{\infty} \chi_k(t)\,\gamma_k(x)\,, \quad \chi_k = \frac{1}{2\,a}\int_{-2\,a}^{+2\,a} \gamma_k\,\omega\;\mathrm{d}x,$$
$$\gamma_k = \cos\left(k\,\pi\,\frac{x}{2\,a}\right). \tag{10.40}$$

By construction, the auxiliary function ω verifies the boundary condition $\partial\omega/\partial x = 0$ at $x = 0$, but not $\omega(a) = 0$. To verify the latter, one restricts the choice to those ω that are odd in the interval of length $2\,a$ centered at $x = a$, that is, $\omega(2\,a - x) = -\omega(x)$ for $0 \le x \le a$. Prescribing $\gamma_k(2\,a - x) = -\gamma_k(x)$, it follows $\cos(k\,\pi) = -1$, that is, $k = 2\,i + 1$ with $i = 0, 1, 2, \ldots$; letting $g_i = \cos[(i + 1/2)\,\pi\,x/a]$ and using the properties of ω and g_i provide

$$c_i = \frac{1}{2\,a}\int_{-2\,a}^{+2\,a} g_i\,\omega\;\mathrm{d}x = \frac{1}{a}\int_0^{2\,a} g_i\,\omega\;\mathrm{d}x = \frac{2}{a}\int_0^{a} g_i\,\omega\;\mathrm{d}x\,. \tag{10.41}$$

As $f = \omega$ in the interval $0 \le x \le a$, the Fourier expansion of f reads

$$f = \sum_{i=0}^{\infty} c_i(t)\,g_i(x)\,, \qquad c_i = \frac{2}{a}\int_0^a f\,\cos\left(\frac{x}{L_i}\right)\mathrm{d}x, \tag{10.42}$$

with $1/L_i = (i + 1/2)\,\pi/a$. From $g_i = \cos[(i + 1/2)\,\pi\,x/a]$, it follows $g_i'(0) = 0$, $g(a) = 0$, and $g_i'' = -g_i/L_i^2$; also,

$$\int_0^a g_i\frac{\partial f}{\partial t}\;\mathrm{d}x = \frac{\mathrm{d}}{\mathrm{d}t}\int_0^a g_i f\;\mathrm{d}x = \frac{a}{2}\,\frac{\mathrm{d}c_i}{\mathrm{d}t} \tag{10.43}$$

and, integrating by parts and using the boundary conditions,

$$\int_0^a g_i\,\frac{\partial^2 f}{\partial x^2}\;\mathrm{d}x = \int_0^a \frac{\mathrm{d}^2 g_i}{\mathrm{d}x^2} f\;\mathrm{d}x = -\frac{1}{L_i^2}\int_0^a g_i f\;\mathrm{d}x = -\frac{a}{2}\,\frac{c_i}{L_i^2}. \tag{10.44}$$

Multiplying by g_i both sides of (10.39), integrating from 0 to a, and using (10.43), (10.44), finally provide a first-order differential equation for c_i

$$\frac{\mathrm{d}c_i}{\mathrm{d}t} + \frac{c_i}{\tau_i} = \alpha_i\,\exp(t/\tau_\mathrm{n})\,, \quad \tau_i = \frac{L_i^2}{D_\mathrm{n}},$$
$$\alpha_i = \frac{2}{a}\int_0^a g_i\,G_\mathrm{s}\exp(-k\,x)\;\mathrm{d}x\,, \tag{10.45}$$

with the initial condition

$$c_i(0) = \frac{2}{a}\int_0^a g_i f(x,0)\;\mathrm{d}x = \frac{2}{a}\int_0^a g_i\,Q(0)\,\delta(x^+)\;\mathrm{d}x = \frac{2}{a}\,Q_0, \tag{10.46}$$

independent of i. Integrating (10.45) yields

$$c_i(t)\,\exp(t/\tau_i) - c_i(0) = \alpha_i\,\tau_i^\star\,\left[\exp(t/\tau_i^\star) - 1\right],$$
$$\frac{1}{\tau_i^\star} = \frac{1}{\tau_\mathrm{n}} + \frac{1}{\tau_i} \tag{10.47}$$

whence, turning to the original unknown $n - n_{\mathrm{p}0} = f\,\exp(-t/\tau_\mathrm{n})$,

$$n - n_{\mathrm{p}0} = \sum_{i=0}^{\infty} g_i\,\left[\alpha_i\,\tau_i^\star + \left(c_i(0) - \alpha_i\,\tau_i^\star\right)\,\exp(-t/\tau_i^\star)\right]. \tag{10.48}$$

Like in the case of the uniform substrate, the excess charge per unit area $Q(t) = q\int_0^a (n - n_{\mathrm{p}0})\;\mathrm{d}x$ does not vanish for $t \to \infty$ as long as $G_\mathrm{s} \neq 0$. Using $\tau_i = L_i^2/D_\mathrm{n}$ and the definition of the minority-carrier diffusion length $L_\mathrm{n} = \sqrt{\tau_\mathrm{n}\,D_\mathrm{n}}$, one finds

$$\tau_i = \tau_\mathrm{n}\,\frac{L_\mathrm{i}^2}{L_\mathrm{n}^2} = \tau_\mathrm{n}\,\frac{a^2}{[\pi\,L_\mathrm{n}\,(i + 1/2)]^2}\,. \tag{10.49}$$

For typical values of a and L_n, the largest decay time obtained from (10.49), τ_0, is much shorter than that found for a uniform substrate: $\tau_0/\tau_\mathrm{n} = 4\,a^2/(\pi^2\,L_\mathrm{n}^2) \ll 1$.

10.5 MOS Capacitor: n-Type Substrate

This section briefly illustrates the theory of the n-substrate MOS capacitor, which is "dual" to that of the p-substrate one. Letting N_D be the constant concentration of donor atoms, such that the non-degeneracy and complete-ionization conditions apply, and letting $\varphi(\infty) = 0$, one finds (compare with (10.2))

$$n^{(0)} = n(+\infty) = n_{n0} \simeq N_D\,, \quad p^{(0)} = p(+\infty) = p_{n0} \simeq \frac{n_i^2}{N_D}\,. \tag{10.50}$$

The Poisson equation in the semiconductor takes the form (compare with (10.3))

$$u'' = \frac{1}{L_D^2}\,A(u)\,, \qquad A(u) = \exp(u) - 1 + \frac{n_i^2}{N_D}\,[1 - \exp(-u)]\,, \tag{10.51}$$

with $L_D^2 = \varepsilon_{sc}\,k_B\,T/(q^2\,n_{n0})$, and its solution is

$$u' = \pm\frac{\sqrt{2}}{L_D}\,F(u),$$
$$F = \sqrt{\exp(u) - 1 - u + \frac{n_i^2}{N_D^2}\,[u + \exp(-u) - 1]}\,. \tag{10.52}$$

Noting that (10.7) and (10.9) hold for both the p- and n-type substrates (here, however, Q_{sc} is the integral of $q\,(p - n + N_D)$, instead of $q\,(p - n - N_A)$, over the semiconductor domain), one finds

$$C_{ox}\,(V'_G - \varphi_s) = \mp\varepsilon_{sc}\,\frac{k_B\,T}{q}\,\frac{\sqrt{2}}{L_D}\,F(\varphi_s). \tag{10.53}$$

Also in this case $\varphi_s = 0$ marks the flat-band condition. Like in the p-substrate case, from the $\varphi_s = \varphi_s(V'_G)$ relation, one identifies the functioning regimes that are listed in Table 10.2. The analysis of the functioning regimes, depletion width, form of the electric potential and charge density, and differential capacitance is similar to that of the p-substrate case. By the same token, one finds the simplified form of the inversion-layer charge that holds in all the functioning regimes with the exception of accumulation; one starts from (10.53) in the form

$$Q_{sc} = \pm Q_{sc}^{(1)}\,F(u_s)\,, \qquad Q_{sc}^{(1)} = \varepsilon_{sc}\,\frac{k_B\,T}{q}\,\frac{\sqrt{2}}{L_D}\,, \tag{10.54}$$

shown in normalized units in Fig. 10.15. The limiting case of (10.52) in the depletion and weak-inversion regimes is

$$F \simeq \sqrt{-u_s}\,, \qquad 2\,u_F < u_s < 0. \tag{10.55}$$

Table 10.2 MOS capacitor, n substrate – Functioning regimes (after [2])

Norm. surface potential	Concentrations	Designation
$u_s > 0$	$p_s < p_{n0} < n_i < n_{n0} < n_s$	Accumulation
$u_s = 0$	$p_s = p_{n0} < n_i < n_{n0} = n_s$	Flat band
$u_F < u_s < 0$	$p_{n0} < p_s < n_i < n_s < n_{n0}$	Depletion
$u_s = u_F$	$p_{n0} < p_s = n_i = n_s < n_{n0}$	Mid gap
$2\,u_F < u_s < u_F$	$p_{n0} < n_s < n_i < p_s < n_{n0}$	Weak inversion
$u_s = 2\,u_F$	$p_{n0} = n_s < n_i < p_s = n_{n0}$	Threshold
$u_s < 2\,u_F$	$n_s < p_{n0} < n_i < n_{n0} < p_s$	Strong inversion

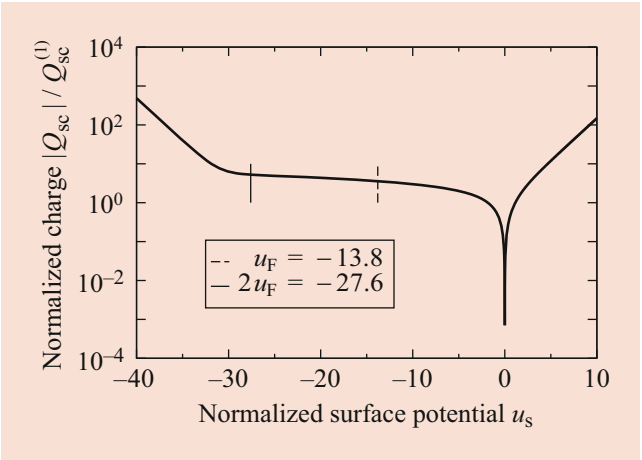

Fig. 10.15 Normalized charge per unit area as a function of the normalized surface potential, in an n-substrate MOS capacitor with $N_D = 10^{16}$ cm^{-3}. (After [2])

Introducing (10.55) into (10.54) yields, for $2\,u_F < u_s < 0$ (compare with (10.26)),

$$Q_{sc} \simeq \frac{\sqrt{2}\,\varepsilon_{sc}\,k_B\,T}{q\,L_D}\,\sqrt{-\frac{q\,\varphi_s}{k_B\,T}} = C_{ox}\,\gamma\,\sqrt{-\varphi_s},$$
$$\gamma = \frac{\sqrt{2\,\varepsilon_{sc}\,q\,n_{n0}}}{C_{ox}}. \tag{10.56}$$

The same relation as (10.56) is obtained using the full-depletion and ASCE approximations

$$-\varphi_s = \frac{q\,N_D}{2\,\varepsilon_{sc}}\,x_d^2\,, \qquad Q_b = q\,N_D\,x_d = \sqrt{-2\,\varepsilon_{sc}\,q\,N_D\,\varphi_s}. \tag{10.57}$$

When $2\,u_F < u_s < 0$, it is $Q_{sc} \simeq Q_b$; letting $N_D \simeq n_{n0}$ makes the second relation in (10.57) to coincide with the first of (10.56); then, using $Q_{sc} \simeq Q_b$ in (10.56) and combining the result with the general expression $Q_{sc} = -C_{ox}\,(V'_G - \varphi_s)$ yield $V'_G - \varphi_s = -\gamma\,\sqrt{-\varphi_s}$, namely, after discarding the negative sign in front of the square root,

$$\sqrt{-\varphi_s} = \sqrt{-V'_G + (\gamma/2)^2} - \gamma/2\,, \qquad V'_G < 0\,, \tag{10.58}$$

applicable in the depletion and weak-inversion conditions. From the threshold condition on, the contribution of holes to the semiconductor charge per unit area $Q_i = q \int_0^{x_d} p \, dx$ becomes relevant; approximating the hole charge with a layer, proceeding as for the p-substrate case (Sect. 10.1.2), and using $Q_{sc} = Q_i + Q_b$, one finds

$$Q_i = Q_{sc} - Q_b = C_{ox} \left[\left(-V'_G + \varphi_s \right) - \gamma \sqrt{-\varphi_s} \right] > 0 , \tag{10.59}$$

that holds in the depletion, weak-inversion, and strong-inversion regimes (compare with (10.29)).

10.6 Insulated-Gate Field-Effect Transistor: MOSFET

Acronym IGFET stands for *insulated-gate field-effect transistor*: the concept of insulated-gate device was proposed in the 1930s of the last century [4–7] and [1, Chap. 10]. The bipolar transistor was in fact discovered experimentally, in 1947, during the investigations about IGFETs. The first experimental FET was realized in 1948 [8]: until that time, the idea was that of exploiting the electric field to modulate the conduction of majority carriers near the device surface [9]. The use of the field to control the minority carriers was proposed in 1955 [10]; the idea of using a thermally grown oxide as gate dielectric came about in the 1960s [11], whence the more common designation MOSFET derives. This concept gave rise to the extraordinary progress of integrated circuits in the last decades; an important ingredient of this progress is the possibility to scale down the device's size. The scaling rules are briefly addressed in Sect. 10.13.4. An outline of the historical development of the device is in [12, 13]; device modeling was developed in the mid-1960s of the last century [14–16].

The device current is carried by one type of carriers only that form a charge layer at the semiconductor-insulator interface (*channel*); for this reason, the device is called *unipolar*. Such carriers are electrons in a p-doped substrate (n-*channel* MOSFET) or holes in an n-doped substrate (p-*channel* MOSFET). A view of an n-*channel* MOSFET is shown in Fig. 10.16; starting from a p-type silicon substrate with an $N_A = \text{const}$ dopant concentration, the gate insulator is formed by growing a layer of silicon dioxide, onto which the gate contact (G) is deposited. The horizontal extension L_g of the latter is the *geometrical length* of the gate. The source and drain regions are obtained by implanting a heavy dose of dopant (of the n-type in this case) and then performing an annealing step; lateral diffusion makes the gate oxide to partially overlap the n-doped regions.

The source (S) and drain (D) contacts are deposited on the two n^+ regions, while the bulk (B) metal is deposited on the p-type substrate. The three independent biases are indicated

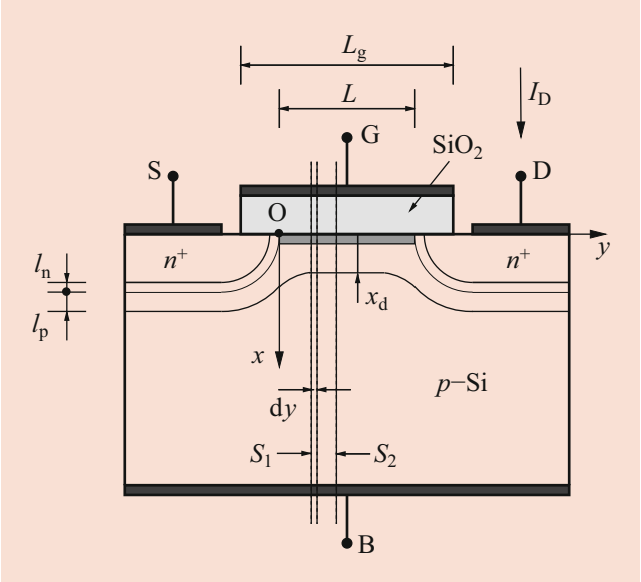

Fig. 10.16 Cross-section of an n-channel MOSFET. The black areas are the metal contacts. (After [2])

with letters, the standard choice for an n-channel MOSFET being $V_{GB} = V_G - V_B$, $V_{SB} = V_S - V_B$, and $V_{DB} = V_D - V_B$. In the typical operating regime of the device, the source-bulk and drain-bulk junctions are never forward biased, whence $V_{SB} \geq 0$ and $V_{DB} \geq 0$ (for the n-channel MOSFET), with $V_{DB} - V_{SB} = V_{DS} \geq 0$.

10.7 n-Channel MOSFET: Current-Voltage Characteristics

Purpose of this section is deriving the relations between the currents at the contacts and the applied voltages. The analysis is based on Fig. 10.16, in which the x-axis is taken normal to the semiconductor-insulator interface, with the origin (O) placed at the intersection of the source p-n junction with the interface. Symbol L indicates the intersection, along the y-axis, of the drain p-n junction with the interface and is called *electric length* of the gate, or *channel length*. The device is uniform in the z direction, with W indicating the width.

To begin, it is assumed that V_{GB} is such that at all positions y along the channel, the strong-inversion condition applies (*well-formed channel*); the layer of electrons is indicated with the shaded area in Fig. 10.16 under the oxide. In steady state, no current flows through the gate contact due to the presence of the gate insulator, and the current through the bulk contact is negligible because the source and drain junctions are never forward biased. The layer of electrons in the channel connects two heavily doped regions of the n-type: when a drain-source voltage $V_{DS} > 0$ is applied, a current I_D flows through the

channel from the drain to the source contact (the reference of I_D is visible in Fig. 10.16); given V_{DS}, the drain current I_D depends on the quantity of charge present in the channel, such a quantity being controlled by V_{GB}. In essence, the device is an electronic valve whose gate-bulk port controls the current flowing into the drain-source port; also, in steady state, the control port does not absorb energy, because the gate current is zero; this, among other things, explains the success of the MOSFET concept. The electron and hole current densities read

$$\mathbf{J}_n = J_{nx}\,\mathbf{i} + J_{ny}\,\mathbf{j}\,, \qquad \mathbf{J}_p = J_{px}\,\mathbf{i} + J_{py}\,\mathbf{j}\,, \tag{10.60}$$

with $\mathbf{i}$ and $\mathbf{j}$ the unit vectors of the coordinate axes. Due to the presence of the insulator, it is $J_{nx} = J_{px} = 0$; also, the condition of well-formed channel makes the hole concentration negligible with respect to that of the electrons (compare with Fig. 10.12; although the equilibrium condition is considered in the figure, the situation is similar). It follows $|J_{ny}| \gg |J_{py}|$, whence $\mathbf{J} = \mathbf{J}_n + \mathbf{J}_p \simeq \mathbf{J}_n = J_{ny}(x, y)\,\mathbf{j}$. Equality $\mathbf{J} = \mathbf{J}_n$ translates into symbols the property of the MOSFET being unipolar; another consequence is $\mathrm{div}\mathbf{J} = \mathrm{div}\mathbf{J}_n$ so that, observing that in a steady-state condition it is $\mathrm{div}\mathbf{J} = 0$, then it is also $\mathrm{div}\mathbf{J}_n = 0$, and the channel current

$$I = \int_{z=0}^{W} \int_{x=0}^{x_d} \mathbf{J}_n \cdot \mathbf{j}\ \mathrm{d}x\ \mathrm{d}z = W \int_0^{x_d} J_{ny}\ \mathrm{d}x \tag{10.61}$$

does not depend on y. The non-vanishing component J_{ny} in (10.61) is conveniently expressed in the monomial form

$$J_{ny} = -q\,\mu_n\,n\,\frac{\partial \varphi_n}{\partial y}\,, \tag{10.62}$$

with φ_n the electron quasi-Fermi potential. As shown above, it is $J_{nx} = 0$ so that, being $n \neq 0$ in the channel, it must be $\partial\varphi_n/\partial x = 0$; in other terms, in the channel, φ_n depends on y only (far from the channel, it does depend on x because $\varphi_n \to \varphi_F$ as x increases toward the bulk contact; however, in the bulk region where the dependence of φ_n on x is significant, the electron concentration is negligible; as a consequence, the integral in (10.61) is not affected). In conclusion,

$$I = W\,\frac{\mathrm{d}\varphi_n}{\mathrm{d}y} \int_0^{x_d} -q\,\mu_n(x, y)\,n(x, y)\ \mathrm{d}x. \tag{10.63}$$

Introducing in (10.63) the *effective electron mobility*

$$\mu_e(y) = \frac{\int_0^{x_d} -q\,\mu_n\,n\ \mathrm{d}x}{\int_0^{x_d} -q\,n\ \mathrm{d}x} > 0\,, \tag{10.64}$$

provides

$$I = W\,\frac{\mathrm{d}\varphi_n}{\mathrm{d}y}\,\mu_e(y)\,Q_i(y)\,, \qquad Q_i = \int_0^{x_d} -q\,n\ \mathrm{d}x < 0\,, \tag{10.65}$$

with $Q_i(y)$ the inversion-layer charge per unit area. As factors μ_e and Q_i in (10.65) have always the same sign, and I and W are constant, the derivative $\mathrm{d}\varphi_n/\mathrm{d}y$ has always the same sign as well. Using the inverse function $y = y(\varphi_n)$ makes the first of (10.65) separable whence, integrating over the channel,

$$\int_0^L I\ \mathrm{d}y = L\,I = W \int_{\varphi_n(0)}^{\varphi_n(L)} \mu_e(\varphi_n)\,Q_i(\varphi_n)\ \mathrm{d}\varphi_n. \tag{10.66}$$

It will be shown in Sect. 10.13.2 that the dependence of μ_e on y is weak; this simplifies (10.66) as

$$I = \frac{W}{L}\,\mu_e \int_{\varphi_n(0)}^{\varphi_n(L)} Q_i(\varphi_n)\ \mathrm{d}\varphi_n. \tag{10.67}$$

The integration limits of (10.67) are

$$\varphi_n(0) = V_{SB} + \varphi_F\,, \qquad \varphi_n(L) = V_{DB} + \varphi_F\,, \tag{10.68}$$

due to the fact that the shift in the quasi-Fermi potential on the two sides of a *p-n* junction equals the applied voltage [1, Sect. 10.2] and that $\varphi_n \to \varphi_F$ at equilibrium. To complete the calculation, it is then necessary to determine Q_i and $\mathrm{d}\varphi_n$. The former is expressed as $Q_i = Q_{sc} - Q_b$ where, in turn, the semiconductor charge per unit area Q_{sc} is found by generalizing the procedure leading to (10.29); for this, one considers Fig. 10.17, which shows an expanded view of the elementary portion of the channel, of width $\mathrm{d}y$, visible in Fig. 10.16. The Gauss theorem is applied to a volume of width W in the z direction, whose boundary in the x, y plane is the red line; the bottom part of the volume is inside the neutral region, whose boundary (the thick black line) is not aligned with the y-axis due to the lateral non-uniformity produced by the application of $V_{DS} \neq 0$. For the semiconductor charge within the volume, one finds

$$\begin{aligned} Q_{sc}\,W\,\mathrm{d}y &= \varepsilon_{sc}\,(E_b - E_s)\,W\,\mathrm{d}y \\ &\quad + \varepsilon_{sc}\,W \left(\int_0^{x_d} E_{yL}\ \mathrm{d}x - \int_0^{x_d + \mathrm{d}x_d} E_{yR}\ \mathrm{d}x \right). \end{aligned} \tag{10.69}$$

In (10.69), one lets $E_b = 0$ because the bottom of the volume is inside the neutral region and neglects the infinitesimal portion (from x_d to $x_d + \mathrm{d}x_d$) of the last integral; observing that $E_{yL} - E_{yR} = -(\partial E/\partial y)\,\mathrm{d}y$ and dividing both sides by $(W\,\mathrm{d}y)$ yield

$$Q_{sc} = -\varepsilon_{sc}\,E_s - \varepsilon_{sc} \int_0^{x_d} \frac{\partial E}{\partial y}\ \mathrm{d}x. \tag{10.70}$$

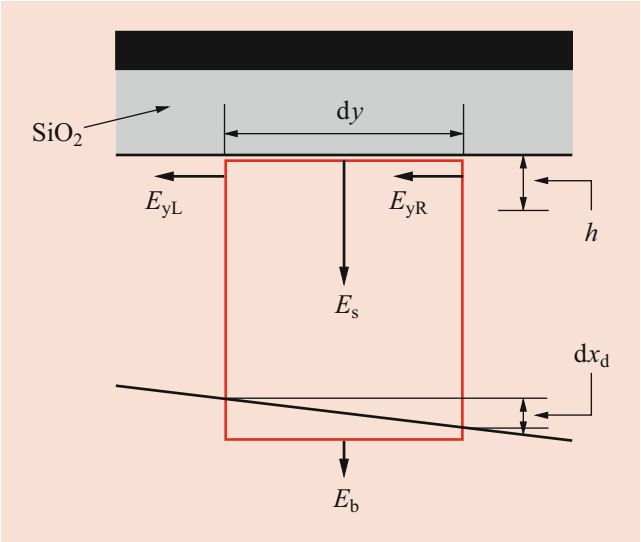

Fig. 10.17 The red line is the intersection with the x, y plane of the volume used for the application of the Gauss theorem, Eq. (10.69). Symbols $E_s, \ldots$ indicate the vertical or horizontal components of the electric field. Symbol h qualitatively indicates the thickness of the inversion layer (the scales of the drawing are not realistic)

Neglecting again the contribution of $\mathrm{d}x_\mathrm{d}$, and remembering that a p-type substrate is considered, one finds for the bulk charge per unit area the relation $Q_\mathrm{b} = -q\,N_\mathrm{A}\,x_\mathrm{d}$. Finally, the expression of $\mathrm{d}\varphi_\mathrm{n}$ is taken from (10.96) and reads

$$\mathrm{d}\varphi_\mathrm{n} = \left[1 + \frac{k_\mathrm{B}\,T}{q}\,\frac{2\,r^2\,\left(V'_\mathrm{GB} - \varphi_\mathrm{s}\right) + k_\mathrm{B}\,T/q}{r^2\,\left(V'_\mathrm{GB} - \varphi_\mathrm{s}\right)^2 - k_\mathrm{B}\,T\,\varphi_\mathrm{s}/q}\right]\,\mathrm{d}\varphi_\mathrm{s},$$
$$r = \frac{1}{\sqrt{2}}\,\frac{\varepsilon_\mathrm{ox}}{\varepsilon_\mathrm{sc}}\,\frac{L_\mathrm{A}}{t_\mathrm{ox}}, \qquad (10.71)$$

with $\varphi_\mathrm{s}(y) = \varphi(x = 0, y)$. The relation between φ_n and φ_s given by (10.71) applies, at each position y, in the depletion, weak-inversion, and strong-inversion cases, that are the working conditions of interest.

10.7.1 Gradual-Channel Approximation

To complete the calculation of (10.67), one exploits the inequality $|\partial E_\mathrm{x}/\partial x| \gg |\partial E_\mathrm{y}/\partial y|$ to reduce the Poisson equation to a one-dimensional form (the details are in Sect. 10.13.1); in this way, each elementary portion of the channel (like $\mathrm{d}y$ in Figs. 10.16 or 10.17) is treated like an MOS capacitor having $\varphi_\mathrm{s}(y)$ as surface potential, and (10.70) reduces to $Q_\mathrm{sc} = -\varepsilon_\mathrm{sc}\,E_\mathrm{s}$. This simplification is designated with *gradual-channel approximation* (GCA).

Next, one describes each elementary MOS capacitor using the full-depletion and ASCE approximations; in other terms, the inversion charge is approximated as a layer at $x = 0^+$, so that the volume charge is due only to the ionized dopants, which contribute to the bulk charge Q_b with a term proportional to $\sqrt{\varphi_\mathrm{s}}$ like in equilibrium. In this way, the inversion-layer charge per unit area at any position y in the channel is given by (10.29), namely,

$$Q_\mathrm{i} = -C_\mathrm{ox}\,\left[\left(V'_\mathrm{GB} - \varphi_\mathrm{s}\right) - \gamma\,\sqrt{\varphi_\mathrm{s}}\right] < 0\,, \qquad (10.72)$$

and (10.67) becomes

$$I = -\beta\,\int_{\varphi_\mathrm{s}(0)}^{\varphi_\mathrm{s}(L)}\,\left[\left(V'_\mathrm{GB} - \varphi_\mathrm{s}\right) - \gamma\,\sqrt{\varphi_\mathrm{s}}\right]\,\frac{\mathrm{d}\varphi_\mathrm{n}}{\mathrm{d}\varphi_\mathrm{s}}\,\mathrm{d}\varphi_\mathrm{s},$$
$$\beta = \frac{W}{L}\,\mu_\mathrm{e}\,C_\mathrm{ox}\,, \qquad (10.73)$$

where the units of β are $[\beta] = \mathrm{A\ V^{-2}}$. The above expression, where $\mathrm{d}\varphi_\mathrm{n}/\mathrm{d}\varphi_\mathrm{s}$ is given by (10.71), applies to the depletion, weak-inversion, and strong-inversion regimes. The integration limits in (10.73) are obtained numerically as shown in Sect. 10.7.3, and, being $V_\mathrm{DS} > 0$, it is found $\varphi_\mathrm{s}(L) > \varphi_\mathrm{s}(0)$; as the integrand is negative, it follows $I < 0$, whence $I_\mathrm{D} = -I$ due to the reference chosen for I_D (Fig. 10.16).

Despite the unwieldy appearance, (10.73) can be integrated analytically; the result is shown in Sect. 10.7.3. Prior to that, it is convenient to illustrate an approximation commonly used for the device description, which consists in neglecting the second term in brackets in (10.71), namely, in letting $\mathrm{d}\varphi_\mathrm{n} \simeq \mathrm{d}\varphi_\mathrm{s}$. The approximation provides an analytic expression for the integration limits, which read (Sect. 10.7.3)

$$\varphi_\mathrm{s}(0) = V_\mathrm{SB} + 2\,\varphi_\mathrm{F}\,, \qquad \varphi_\mathrm{s}(L) = V_\mathrm{DB} + 2\,\varphi_\mathrm{F}\,; \qquad (10.74)$$

on the other hand, it restricts the applicability of the result to the strong-inversion regime only. The approximate expression of I_D reads

$$I_\mathrm{D} = \beta\,\int_{V_\mathrm{SB}+2\,\varphi_\mathrm{F}}^{V_\mathrm{DB}+2\,\varphi_\mathrm{F}}\,\left[\left(V'_\mathrm{GB} - \varphi_\mathrm{s}\right) - \gamma\,\sqrt{\varphi_\mathrm{s}}\right]\,\mathrm{d}\varphi_\mathrm{s}\,; \qquad (10.75)$$

it is used in Sect. 10.7.2 to discuss some features of the n-channel device and in Sect. 10.8, after suitable modifications, for the p-channel device.

Before concluding this section, it is worth noting that the application of GCA is not limited to MOSFETs; in fact, it is a widely used method for finding an approximate solution of the Poisson equation when the geometry and bias configuration of the device are such that the variation of the electric field in the direction of the channel is much weaker than in the other directions. Formally, the approximation consists in eliminating a part of the Laplacian operator, in such a way as to leave a differential relation for one variable (or a separable operator for some variables), whereas the dependence on the remaining variables becomes algebraic.

10.7.2 Differential Conductances and Drain Current, n-Channel

The simplified expression of the drain current of the *n*-channel MOSFET, given by (10.75), is a relation of the form $I_D = I_D(V_{GB}, V_{DB}, V_{SB})$, with $V_{GB} = V'_{GB} + V_{FB}$. From it, the *differential conductances* of the device are readily calculated as the derivatives with respect to the voltages. In circuit applications, it is more convenient to refer the applied voltages to the source contact instead of the bulk contact; this is easily accomplished by the transformation

$$V_{DS} = V_{DB} - V_{SB} > 0\,, \qquad V_{GS} = V_{GB} - V_{SB}\,,$$
$$V_{BS} = -V_{SB} \leq 0\,. \tag{10.76}$$

Then, the *drain conductance* g_D (also called *output conductance*, g_o) is defined as

$$g_D = \left(\frac{\partial I_D}{\partial V_{DB}}\right)_{V_{SB}, V_{GB}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{BS}, V_{GS}}\,, \tag{10.77}$$

namely, from (10.75),

$$g_D = \beta \left[\left(V'_{GB} - V_{DB} - 2\,\varphi_F\right) - \gamma \sqrt{V_{DB} + 2\,\varphi_F}\right]; \tag{10.78}$$

then, using (10.74) and (10.29), one finds

$$g_D = \beta \left[\left(V'_{GB} - \varphi_s(L)\right) - \gamma \sqrt{\varphi_s(L)}\right] = \frac{W}{L}\,\mu_e\,\left[-Q_i(L)\right]\,, \tag{10.79}$$

showing that g_D is proportional to the inversion charge per unit area at the drain end of the channel. In (10.79), it is $Q_i(L) \leq 0$; the zero of $Q_i(L)$ corresponds to the value of $\varphi_s(L)$ obtained from (10.28) and is indicated with φ_s^{sat} (*saturation surface potential*). Combining (10.74) with (10.76) provides the *saturation voltage* in the bulk and source references, respectively:

$$V_{DB}^{sat} = \varphi_s^{sat} - 2\,\varphi_F\,, \qquad V_{DS}^{sat} = V_{DB}^{sat} - V_{SB}\,. \tag{10.80}$$

Correspondingly, the *saturation current* is $I_D^{sat} = I_D(V_{DS}^{sat}, V_{GS})$. The right-hand side of (10.78) becomes negative if a value of V_{DS} larger than V_{DS}^{sat} is used; this unphysical result shows that the approximation leading to (10.75) is not applicable for $V_{DS} > V_{DS}^{sat}$. An important limiting case of (10.78) is

$$g_D(V_{DS} \to 0) = \beta \left[\left(V'_{GB} - V_{SB} - 2\,\varphi_F\right) - \gamma \sqrt{V_{SB} + 2\,\varphi_F}\right], \tag{10.81}$$

or, using (10.76),

$$g_D(V_{DS} \to 0) = \beta\,\left(V_{GS} - V_T\right)\,,$$

$$V_T = V_{FB} + 2\,\varphi_F + \gamma\,\sqrt{2\,\varphi_F - V_{BS}} \tag{10.82}$$

with $V_{BS} \leq 0$. The above defines the *threshold voltage* $V_T = V_T(V_{BS})$; the dependence of V_T on V_{BS} is the *body effect*. Near $V_{DS} = 0$, the current-voltage characteristics reduce to $I_D = \beta\,(V_{GS} - V_T)\,V_{DS}$, namely, to straight lines whose slope, for a given V_{BS}, is prescribed by V_{GS}; for a larger V_{DS}, the slope of the $I_D = I_D(V_{DS})$ curves decreases, to eventually vanish at $V_{DS} = V_{DS}^{sat}$. Since I_D is non-negative, the theory outlined here applies as long as $\beta\,(V_{GS} - V_T) \geq 0$; thanks to this observation, it is possible to better specify the condition of a well-formed channel: from the formal standpoint, such a condition is $V_{GS} > V_T$.

Integrating (10.75) yields $I_D = I'_D - I''_D$, where I'_D is the integral of $\beta\,(V'_{GB} - \varphi_s)$, which reads

$$I'_D = \beta \left[(V_{GS} - V_{FB} - 2\,\varphi_F)\,V_{DS} - \frac{1}{2}\,V_{DS}^2\right], \tag{10.83}$$

and I''_D is the integral of $\beta\,\gamma\,\sqrt{\varphi_s}$,

$$I''_D = \beta\,\frac{2}{3}\,\gamma\,\left[(V_{DS} + 2\,\varphi_F - V_{BS})^{3/2} - (2\,\varphi_F - V_{BS})^{3/2}\right]. \tag{10.84}$$

Comparisons with experiments show that the model $I_D = I'_D - I''_D$, based on (10.83) and (10.84), gives a fair description of I_D up to V_{DS}^{sat}; as shown by the derivation above, this is essentially due to the fact that in this region, the electric field along the channel is small. Beyond saturation, the model is not consistent with the experiments: the terms with a negative sign produce a negative slope g_D, whereas the experiments show that for $V_{DS} > V_{DS}^{sat}$, the current tends to saturate. This explains why the model based on (10.75) is presented in a regional form: given V_{GS} and V_{BS}, the model separates, first, the *on* condition $V_{GS} > V_T$ from the *off* condition $V_{GS} \leq V_T$; second, the *on* condition is further separated into the *linear region* $0 < V_{DS} \leq V_{DS}^{sat}$, where the expression $I_D = I'_D - I''_D$ derived above is used, and the *saturation region* $V_{DS} > V_{DS}^{sat}$; in the latter, the model lets $I_D = I_D^{sat}$. Finally, in the *off* region, one sets $I_D = 0$. It is worth adding that the designation *linear* is due to the behavior of g_D near the origin; the term is used to describe the characteristics up to V_{DS}^{sat} despite the fact that near saturation the curves are not linear any more.

Depending on the materials, V_{FB} may have either sign; it follows that V_T, given by (10.82), may have either sign as well (in a p-type substrate, instead, it is always $2\,\varphi_F = (k_B\,T/q)\,\log(p_{p0}/n_{p0}) > 0$, and vice versa). One must then distinguish two types of n-channel MOSFETs, the *enhancement type*, having $V_T(V_{BS} = 0) > 0$, and the *depletion type*, having $V_T(V_{BS} = 0) < 0$. To obtain a well-formed channel in the enhancement type, one must set $V_{GS} > V_T > 0$, while $V_{GS} = 0$ corresponds to the *off* condition; in the depletion type, instead, a well-formed channel is present when V_{GS}=0,

whereas the *off* condition is achieved with $V_{GS} \leq V_T < 0$. For a given V_{BS}, the $I_D = I_D(V_{DS})$ curves corresponding to different values of V_{GS} are called *output characteristics*; other types of characteristics are also used: for instance, the *transfer characteristics* are the $I_D = I_D(V_{GS})$ curves drawn using V_{BS} as a parameter and letting $V_{DS} = \text{const}$, with a value of V_{DS} small enough to let the limiting case (10.82) hold.

Besides the drain conductance (10.77), two more differential conductances are defined in a MOSFET: the first one is the *transconductance*

$$g_m = \left(\frac{\partial I_D}{\partial V_{GB}}\right)_{V_{SB},V_{DB}} = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS},V_{BS}} = \beta\, V_{DS}\,, \tag{10.85}$$

and the second one is the *bulk transconductance*

$$g_B = \left(\frac{\partial I_D}{\partial V_{BS}}\right)_{V_{DS},V_{GS}} = -\left(\frac{\partial I''_D}{\partial V_{BS}}\right)_{V_{DS}}. \tag{10.86}$$

The small-signal circuit of an n-channel MOSFET is shown in Fig. 10.18, with v_{DS}, v_{GS}, and v_{BS} indicating the small-signal voltages; it holds at low frequencies only because it derives from the steady-state model. The gate and bulk contacts are left open because the corresponding currents are zero; as a consequence, $i_D = i_S$ is the only non-zero small-signal current of the circuit. The small-signal relation reads

$$i_D = g_D\, v_{DS} + g_m\, v_{GS} + g_B\, v_{BS}\,, \tag{10.87}$$

and describes three parallel branches as shown in the figure.

The body effect mentioned above is an inconvenience, as it introduces a complicated dependence of I_D on V_{BS}, which must be accounted for in the circuit design; the effect is suppressed by letting $V_{BS} = 0$, namely, by shorting the bulk and source contacts, which reduces the original four-contact device to a three-contact device (letting $V_{BS} = 0$ also makes g_B to vanish). This solution is adopted whenever the circuit architecture allows for it.

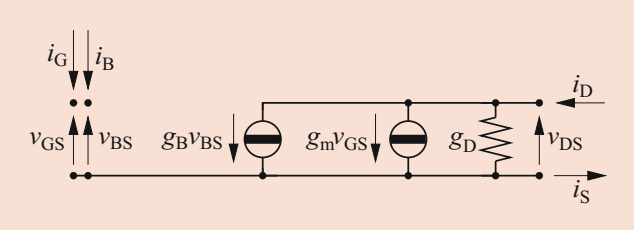

Fig. 10.18 Low-frequency, small-signal circuit of an n-channel MOSFET. (After [2])

Linear-Parabolic Model, n-Channel

In simplified circuit analyses, the term I''_D is expressed as $I''_D \simeq \beta\,\gamma\,\sqrt{2\,\varphi_F - V_{BS}}\,V_{DS}$, this providing a simplified model called *linear-parabolic model*. The approximation consists in replacing $\sqrt{\varphi_s}$ in (10.75) with $\sqrt{2\,\varphi_F - V_{BS}}$; this is equivalent to assuming that the width of the depleted region is constant along the channel and equal to the value taken at source. The expression of the current simplifies to

$$I_D \simeq \beta\,[(V_{GS} - V_T)\,V_{DS} - V_{DS}^2/2]\,, \tag{10.88}$$

with V_T still given by (10.82). In turn, from (10.88), the drain conductance becomes

$$g_D \simeq \beta\,(V_{GS} - V_T - V_{DS})\,, \tag{10.89}$$

whence

$$V_{DS}^{sat} = V_{GS} - V_T. \tag{10.90}$$

The transconductance g_m is the same as in the general case. In the linear-parabolic model, the drain current may also be written $I_D \simeq \beta\,(V_{DS}^{sat}\,V_{DS} - V_{DS}^2/2)$, with V_{DS}^{sat} given by (10.90). Thus,

$$I_D^{sat} \simeq \beta\left[\left(V_{DS}^{sat}\right)^2 - \frac{1}{2}\left(V_{DS}^{sat}\right)^2\right] = \frac{1}{2}\,\beta\,(V_{GS} - V_T)^2\,. \tag{10.91}$$

Finally, the expressions for the saturation region become

$$I_D = I_D^{sat}\,, \qquad g_D \simeq 0\,, \qquad g_m \simeq \beta\,(V_{GS} - V_T)\,. \tag{10.92}$$

The output characteristics of an n-channel MOSFET obtained from the linear-parabolic model are exemplified in Fig. 10.19, using $V_T = 1$ V and $\beta = 0.3$ A V^{-2}. The dashed curve represents (10.91). The symbol of the enhancement-type device is shown in Fig. 10.20 (other symbols are also used in the literature).

10.7.3 MOSFET Theory Including the Subthreshold Current

The results of Sect. 10.13.1 are readily exploited to calculate the general expression (10.73) of the drain current; using the normalized potentials, the expression reads

$$I_D = \beta\left(\frac{k_B\,T}{q}\right)^2 \int_{u_s(0)}^{u_s(L)} \left[\left(u'_{GB} - u_s\right) - (1/r)\,\sqrt{u_s}\right] \frac{d\chi_n}{du_s}\,du_s\,, \tag{10.93}$$

with $u'_{GB} = q\,V'_{GB}/(k_B\,T)$ and $\chi_n = u_n - u_F$. Remembering that the accumulation condition is excluded and that, at each channel position y, it is $E_{sx} = -Q_{sc}/\varepsilon_{sc}$, one recasts (10.169) as

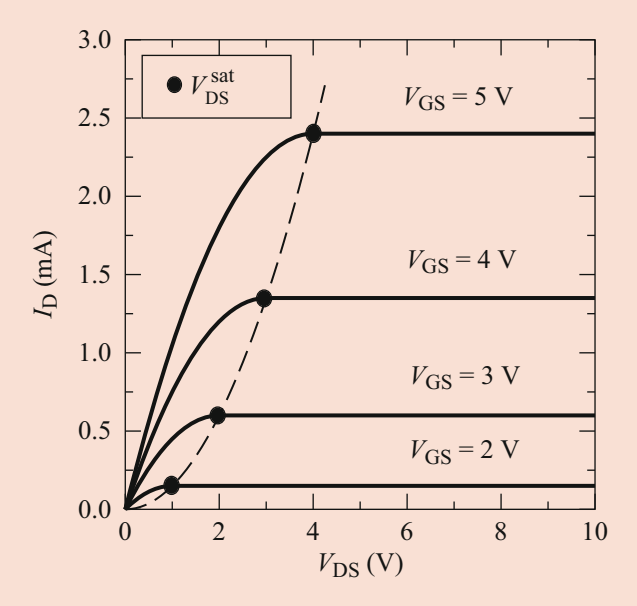

Fig. 10.19 Output characteristics of an n-type MOSFET obtained from the linear-parabolic model, with $V_T = 1$ V and $\beta = 0.3$ A V^{-2}. The dashed curve represents (10.91). (After [2])

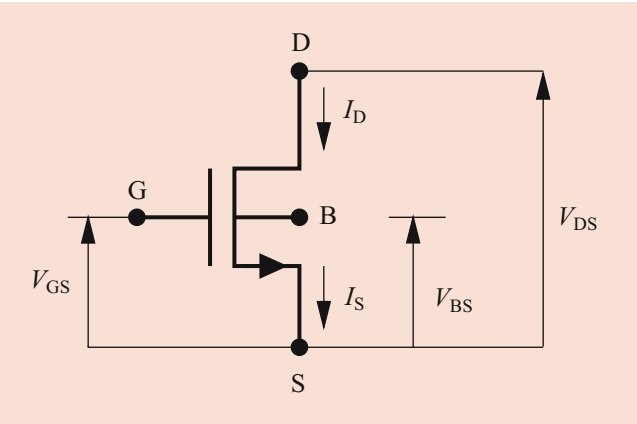

Fig. 10.20 Symbol of the n-channel MOSFET of the enhancement type. (After [2])

$$r^2\,\left(u'_{GB}-u_s\right)^2=\exp(-\chi_n-2\,u_F)\,\left[\exp(u_s)-1\right]+u_s,$$
$$r=\frac{1}{\sqrt{2}}\,\frac{\varepsilon_{ox}}{\varepsilon_{sc}}\,\frac{L_A}{t_{ox}} \tag{10.94}$$

(from (10.26), one notes that $r\,\gamma = \sqrt{k_B\,T/q}$). Observing that when u_s exceeds a few thermal units one can neglect the unity, the $\chi_n = \chi_n(u_s)$ relation in (10.94) simplifies to

$$\chi_n = u_s - 2\,u_F - \log\left[r^2\,\left(u'_{GB}-u_s\right)^2-u_s\right]. \tag{10.95}$$

The integration limits of (10.93) are found by numerically inverting (10.95) after letting $\chi_n(0) = q\,V_{SB}/(k_B\,T)$ and $\chi_n(L) = q\,V_{DB}/(k_B\,T)$; factor $\mathrm{d}\chi_n/\mathrm{d}u_s$ in the integrand of (10.93) is conveniently expressed as

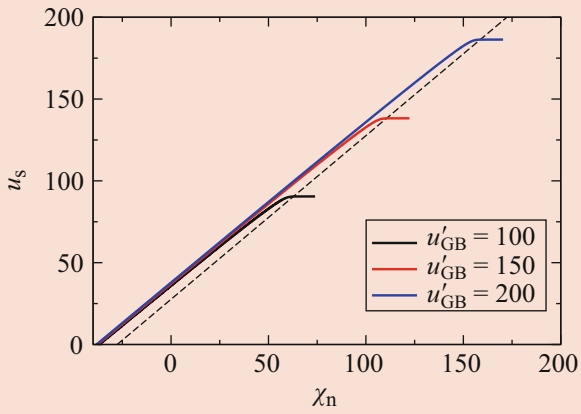

Fig. 10.21 The $u_s = u_s(\chi_n)$ relation (10.95) with u'_{GB} as a parameter, using a dopant concentration $N_A = 10^{16}$ cm^{-3} ($2\,u_F \simeq 27.6$), is compared with the $u_s = \chi_n + 2\,u_F$ approximation (*dashed line*). (After [2])

$$\frac{\mathrm{d}\chi_n}{\mathrm{d}u_s}=1+\frac{2\,r^2\,\left(u'_{GB}-u_s\right)+1}{r^2\,\left(u'_{GB}-u_s\right)^2-u_s}. \tag{10.96}$$

As mentioned in Sect. 10.7, (10.93) applies to all working conditions with the exception of accumulation and, therefore, incorporates the subthreshold current in the analysis; inequality $\mathrm{d}\chi_n/\mathrm{d}u_s \neq 1$ in (10.96) indicates that the transport is not uniquely of the drift type. Also, (10.96) shows that I_D is made of two contributions: the first one comes from the unity at the right-hand side of (10.96) and is similar to the current $I'_D - I''_D$ derived in Sect. 10.7.2, the only difference being that the integration limits must be calculated numerically from (10.95) instead of being $V_{SB} + 2\,\varphi_F$ and $V_{DB} + 2\,\varphi_F$. The remaining contribution to the current is due to the second term at the right-hand side of (10.96); its analytical calculation, a little more elaborate, is provided below (Sect. 10.7.3).

The $u_s = u_s(\chi_n)$ relation given by (10.95) is shown in Fig. 10.21 with u'_{GB} as parameter and is compared with the approximate form $\chi_n = u_s + 2\,u_F$ (dashed line). The approximation is good as long as u_s is smaller than the lower zero of the logarithm argument in (10.95). Then, u_s saturates at the value corresponding to such a zero; this shows that (10.93) provides a smooth transition from the linear to the saturation region: when V_{DB} is such that $\chi_n(L) = q\,V_{DB}/(k_B\,T)$ enters the saturation region, the upper limit $u_s(L)$ of the integral (10.93) is pinned to the saturation value; as a consequence, the current does not increase any more from that value of V_{DB} on.

General Form of the MOSFET Current

As mentioned above, a part of the integral (10.73) derives from the first term (i.e., the unity) at the right-hand side of (10.93) and reads

$$I'_{\mathrm{D}} - I''_{\mathrm{D}} = \beta\ (k_{\mathrm{B}}\,T/q)^2 \left[\left(u'_{\mathrm{GB}}\,u_{\mathrm{s}} - u_{\mathrm{s}}^2/2\right) - (2/3)\,(1/g)\,u_{\mathrm{s}}^{3/2}\right]_{u_{\mathrm{s}}(0)}^{u_{\mathrm{s}}(L)}. \tag{10.97}$$

As for the second term in (10.96), the zeros of the denominator are found to be $u_{\mathrm{s}}^{\pm} = u'_{\mathrm{GB}} + (1 \pm \sqrt{1 + 4\,r^2\,u'_{\mathrm{GB}}})/(2\,r^2)$, so that (10.96) becomes

$$\frac{\mathrm{d}\chi_{\mathrm{n}}}{\mathrm{d}u_{\mathrm{s}}} - 1 = \frac{1}{u_{\mathrm{s}}^{+} - u_{\mathrm{s}}} + \frac{1}{u_{\mathrm{s}}^{-} - u_{\mathrm{s}}}, \qquad u_{\mathrm{s}} < u_{\mathrm{s}}^{-} < u_{\mathrm{s}}^{+}. \tag{10.98}$$

The latter diverges when $u_{\mathrm{s}} \to u_{\mathrm{s}}^{-}$; however, this zero is canceled by another zero belonging to the other factor in (10.93), so that the integrand related to the second term of the current reads

$$Y(u_{\mathrm{s}}) = \left[\left(u'_{\mathrm{GB}} - u_{\mathrm{s}}\right) - \frac{1}{r}\sqrt{u_{\mathrm{s}}}\right]\left(\frac{\mathrm{d}\chi_{\mathrm{n}}}{\mathrm{d}u_{\mathrm{s}}} - 1\right) = 2\,\frac{r\left(u'_{\mathrm{GB}} - u_{\mathrm{s}}\right) + 1/(2\,r)}{r\left(u'_{\mathrm{GB}} - u_{\mathrm{s}}\right) + \sqrt{u_{\mathrm{s}}}}. \tag{10.99}$$

If u_{s}^{-} is replaced into the right-hand side of (10.99), no divergence occurs. After a short manipulation, one finds $Y(u_{\mathrm{s}}) = 2 - 2\,[\sqrt{u_{\mathrm{s}}} - 1/(2\,r)]/[r\,(u'_{\mathrm{GB}} - u_{\mathrm{s}}) + \sqrt{u_{\mathrm{s}}}]$ which, multiplying by $\mathrm{d}u_{\mathrm{s}}$ and letting $w = \sqrt{u_{\mathrm{s}}} - 1/(2\,r)$, provides

$$Y(w) = \left(w + \frac{1}{2\,r}\right)\left(4 + \frac{2/r}{k + w} - \frac{2/r}{k - w}\right)\mathrm{d}w, \qquad k^2 = u'_{\mathrm{GB}} + \frac{1}{4\,r^2}, \tag{10.100}$$

whose integration is elementary.

Subthreshold Approximation

The theory outlined in Sect. 10.7.3 disposes of the hypothesis of a strong-inversion regime at each point of the channel; depending on the values of χ_{n} and u'_{GB}, at a chosen position y in the channel, the condition may hold or not (in the latter case, one speaks of *subthreshold condition* at y). If V_{DB} and V_{SB} are such that the whole channel is in the subthreshold condition, expression (10.93) of the drain current simplifies to

$$I_{\mathrm{D}} \simeq \beta\,\frac{\exp(u_{\mathrm{s}}^{-} - 2\,u_{\mathrm{F}})}{q^2/(k_{\mathrm{B}}\,T)^2}\,\frac{\exp[-\chi_{\mathrm{n}}(0)] - \exp[-\chi_{\mathrm{n}}(L)]}{\omega - 1}, \tag{10.101}$$

with $\omega = (1 + 4\,r^2\,u'_{\mathrm{GB}})^{1/2}$ and $u'_{\mathrm{GB}} - u_{\mathrm{s}}^{-} = (\omega - 1)/(2\,r^2)$. The derivation of (10.101) is based on the observation that in this working condition, the channel is everywhere near saturation; one then calculates (10.93) by letting $u_{\mathrm{s}}(0) \simeq u_{\mathrm{s}}^{-}$ and assuming that u_{s} varies little along the channel, so that the integral is approximated as the product of the integrand calculated at $u_{\mathrm{s}}(0)$ times the integration interval $u_{\mathrm{s}}(L) - u_{\mathrm{s}}(0)$. The latter is determined from (10.95) written in the form

$$r^2\,\left(u'_{\mathrm{GB}} - u_{\mathrm{s}}\right)^2 - u_{\mathrm{s}} - \exp(u_{\mathrm{s}} - 2\,u_{\mathrm{F}} - \chi_{\mathrm{n}}) = 0, \tag{10.102}$$

where the exponential is small because in saturation it is $\chi_{\mathrm{n}} > u_{\mathrm{s}} - 2\,u_{\mathrm{F}}$; for the same reason, the exponential slowly varies along the channel, so one fixes $u_{\mathrm{s}} = u_{\mathrm{s}}^{-}$ in it and solves (10.102) for $u_{\mathrm{s}} - u'_{\mathrm{GB}}$; discarding the solution with the positive sign, and expanding the square root to first order, yields $u_{\mathrm{s}} \simeq u_{\mathrm{s}}^{-} - (1/\omega)\,\exp(u_{\mathrm{s}}^{-} - 2\,u_{\mathrm{F}} - \chi_{\mathrm{n}})$, whence

$$u_{\mathrm{s}}(L) - u_{\mathrm{s}}(0) \simeq \frac{\exp[-\chi_{\mathrm{n}}(0)] - \exp[-\chi_{\mathrm{n}}(L)]}{\omega\,\exp(2\,u_{\mathrm{F}} - u_{\mathrm{s}}^{-})}, \tag{10.103}$$

with $\chi_{\mathrm{n}}(0) = q\,V_{\mathrm{SB}}/(k_{\mathrm{B}}\,T)$ and $\chi\,(L) = q\,V_{\mathrm{DB}}/(k_{\mathrm{B}}\,T)$. The analysis is completed by calculating the integrand of (10.93) after letting $u_{\mathrm{s}} = u_{\mathrm{s}}(0) = u_{\mathrm{s}}^{-}$. The first part of the integrand derives from the first term (i.e., the unity) at the right-hand side of (10.93); it is found by inspection that this part vanishes for $u_{\mathrm{s}} = u_{\mathrm{s}}^{-}$. Thus, the remaining part is $Y(u_{\mathrm{s}}^{-})$ (compare with (10.99)); observing that $\sqrt{u_{\mathrm{s}}^{-}} = r\,(u'_{\mathrm{GB}} - u_{\mathrm{s}}^{-})$, one finds $Y(u_{\mathrm{s}}^{-}) = \omega/(\omega - 1)$, whence (10.101) ensues.

This result expressed by (10.101) is important because it provides the $I_{\mathrm{D}}(V_{\mathrm{GB}})$ dependence below threshold, namely, when the channel is about to transit from the *off* to the *on* condition; this dependence must be strong in order to make the device reliable as a switch. The strongest dependence of (10.101) on u'_{GB} is the exponential one embedded in u_{s}^{-} so that, when the other voltages are kept fixed, the subthreshold current reads $I_{\mathrm{D}} \simeq \text{const} \times \exp[q\,V_{\mathrm{GB}}/(k_{\mathrm{B}}\,T)]$. In fact, in the subthreshold condition, the experimental $\log(I_{\mathrm{D}})$ vs. V_{GB} relation is to a good approximation a straight line; the *subthreshold swing* (indicated with S or SS) is defined as

$$S = \frac{\mathrm{d}V_{\mathrm{GB}}}{\mathrm{d}\log_{10}(I_{\mathrm{D}})} = \frac{k_{\mathrm{B}}\,T}{q}\,\log(10)\,\frac{\mathrm{d}u'_{\mathrm{GB}}}{\mathrm{d}\log(I_{\mathrm{D}})}, \tag{10.104}$$

and is evaluated from (10.101) by inverting the derivative of $\log(I_{\mathrm{D}}) = u_{\mathrm{s}}^{-} - \log(\omega - 1) + \text{const}$ with respect to u'_{GB}, with $u_{\mathrm{s}}^{-}(u'_{\mathrm{GB}})$ and $\omega(u'_{\mathrm{GB}})$ defined above. One finds

$$S = \frac{k_{\mathrm{B}}\,T}{q}\,\log(10)\,\frac{\mathrm{d}u'_{\mathrm{GB}}}{\mathrm{d}u_{\mathrm{s}}^{-}}\,\frac{\mathrm{d}u_{\mathrm{s}}^{-}}{\mathrm{d}\log(I_{\mathrm{D}})} \tag{10.105}$$

where, after neglecting the weaker term $\log(\omega - 1)$, the last derivative equals unity. The other derivative is expressed in

compact form by considering that in the subthreshold condition, it is $Q_{sc} \simeq Q_b$, with Q_b the bulk charge per unit area, so that $Q_b \simeq -C_{ox}\,(V'_{GB} - \varphi_s)$ and $C_{sc} \simeq -\mathrm{d}Q_b/\mathrm{d}\varphi_s = C_b$, with C_b the depletion capacitance per unit area. Combining the two above yields $V'_{GB} = \varphi_s - Q_b/C_{ox}$ whence, using again the relation $u_s \simeq u_s^-$,

$$\frac{\mathrm{d}u'_{GB}}{\mathrm{d}u_s^-} = 1 + \frac{C_b}{C_{ox}}, \qquad S = \frac{k_B\,T}{q}\,\log(10)\,\left(1 + \frac{C_b}{C_{ox}}\right). \tag{10.106}$$

The extension of the above calculation to the case of short-channel MOSFETs is shown in [17]. From the above result, it follows that $(k_B\,T/q)\,\log(10)\,(1 + C_b/C_{ox})$ is the variation ΔV_{GB} that makes I_D to vary by a factor 10; if $C_b \ll C_{ox}$, at room temperature, it is $\Delta V_{GB} \simeq 60$ mV.

The definition of subthreshold swing is not limited to the MOS transistor, but applies in general to the devices where a conductive channel is controlled by a gate. The value of 60 mV per decade calculated from (10.106) is the minimum (i.e., the most favorable one); in real devices, S is larger (i.e., worse).

10.8 p-Channel MOSFET: Current-Voltage Characteristics

The structure of the p-*channel* MOSFET is dual to that of the n-channel type; with reference to Fig. 10.16, the cross-section is obtained by exchanging the "p" and "n" letters. As the source-bulk and drain-bulk junctions are never forward biased, it is $V_{SB} \le 0$, $V_{DB} \le 0$, and $V_{SB} - V_{DB} = V_{SD} > 0$. It is assumed that a layer of holes is present at each point of the channel, this realizing the condition of a well-formed channel. The current I_S flows from the source to the drain contact (Fig. 10.22); following the same reasoning as that leading to (10.61), one finds for the channel current (compare also with (10.63), (10.64), and (10.65))

$$\begin{aligned} I &= \int_{z=0}^{W}\int_{x=0}^{x_d} \mathbf{J}_p \cdot \mathbf{j}\;\mathrm{d}x\;\mathrm{d}z = W\int_0^{x_d} J_{py}\;\mathrm{d}x \\ &= -W\,\frac{\mathrm{d}\varphi_p}{\mathrm{d}y}\int_0^{x_d} q\,\mu_p\,p\;\mathrm{d}x. \end{aligned} \tag{10.107}$$

$$\begin{aligned} &I = -W\,\frac{\mathrm{d}\varphi_p}{\mathrm{d}y}\,\mu_h(y)\,Q_i(y), \quad Q_i = \int_0^{x_d} q\,p\;\mathrm{d}x, \\ &\mu_h = \frac{\int_0^{x_d} q\,\mu_p\,p\;\mathrm{d}x}{\int_0^{x_d} q\,p\;\mathrm{d}x}, \end{aligned} \tag{10.108}$$

where $Q_i(y) > 0$ is the inversion-layer charge per unit area and $\mu_h(y) > 0$ the effective hole mobility at position y in the channel. Integrating over the channel,

$$\int_0^L I\;\mathrm{d}y = L\,I = W\int_{\varphi_p(L)}^{\varphi_p(0)} \mu_h(\varphi_p)\,Q_i(\varphi_p)\;\mathrm{d}\varphi_p \tag{10.109}$$

(compare with (10.66)), and, considering that the dependence of μ_h on y is weak (Sect. 10.13.1),

$$I = \frac{W}{L}\,\mu_h\int_{\varphi_p(L)}^{\varphi_p(0)} Q_i(\varphi_p)\;\mathrm{d}\varphi_p \tag{10.110}$$

(compare with (10.67)). Using the same approximation as that leading to (10.75) for the n-channel device yields $\mathrm{d}\varphi_p \simeq \mathrm{d}\varphi_s$, whence

$$\varphi_s(0) = V_{SB} + 2\,\varphi_F, \qquad \varphi_s(L) = V_{DB} + 2\,\varphi_F, \tag{10.111}$$

so that (10.110) becomes

$$I = \frac{W}{L}\,\mu_h\int_{V_{DB}+2\,\varphi_F}^{V_{SB}+2\,\varphi_F} Q_i(\varphi_s)\;\mathrm{d}\varphi_s, \tag{10.112}$$

with

$$Q_i = C_{ox}\left[\left(-V'_{GB} + \varphi_s\right) - \gamma\,\sqrt{-\varphi_s}\right] > 0, \tag{10.113}$$

and

$$V'_{GB} = V_{GB} - V_{FB}, \qquad \gamma = \frac{\sqrt{2\,\varepsilon_{sc}\,q\,n_{n0}}}{C_{ox}}. \tag{10.114}$$

Being $V_{SB} + 2\,\varphi_F > V_{DB} + 2\,\varphi_F$ and $Q_i > 0$, one finds $I > 0$, whence $I_S = I$ due to the reference chosen for the source current (Fig. 10.22). In conclusion (compare with (10.73)),

$$\begin{aligned} &I_S = \beta\int_{V_{DB}+2\,\varphi_F}^{V_{SB}+2\,\varphi_F}\left[\left(-V'_{GB} + \varphi_s\right) - \gamma\,\sqrt{-\varphi_s}\right]\mathrm{d}\varphi_s, \\ &\beta = \frac{W}{L}\,\mu_h\,C_{ox}. \end{aligned} \tag{10.115}$$

10.8.1 Differential Conductances and Drain Current, p-Channel

To calculate the differential conductances, it is convenient to use the source contact as a voltage reference; the transformations read

$$\begin{aligned} &V_{SD} = V_{SB} - V_{DB} > 0, \qquad V_{SG} = V_{SB} - V_{GB}, \\ &V_{SB} = -V_{BS} \le 0. \end{aligned} \tag{10.116}$$

The *source conductance*, or *output conductance*, is given by

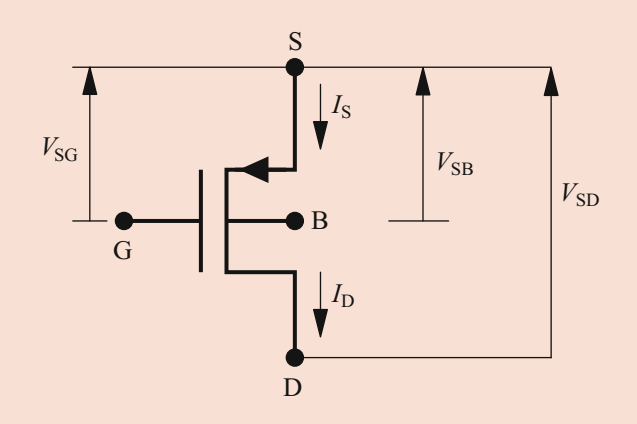

Fig. 10.22 Symbol of the p-channel MOSFET of the enhancement type. (After [2])

$$g_S = \left(\frac{\partial I_S}{\partial V_{BS}}\right)_{V_{BD},V_{BG}} = \left(\frac{\partial I_S}{\partial V_{SD}}\right)_{V_{BD},V_{GD}}, \qquad (10.117)$$

whence

$$g_S = \beta\left[\left(-V'_{GB} + V_{SB} + 2\,\varphi_F\right) - \gamma\sqrt{-V_{SB} - 2\,\varphi_F}\right] = \frac{W}{L}\,\mu_h\,Q_i(0). \qquad (10.118)$$

Letting $g_S = 0$ yields the *saturation surface potential* (compare with (10.28))

$$\sqrt{-\varphi_s^{sat}} = \sqrt{-V'_{GB} + (\gamma/2)^2} + \gamma/2\,; \qquad (10.119)$$

the *saturation voltage* in the bulk and source references is then found to be

$$V_{SB}^{sat} = \varphi_s^{sat} - 2\,\varphi_F\,, \qquad V_{SD}^{sat} = V_{SB}^{sat} - V_{DB}\,, \qquad (10.120)$$

respectively, whence the *saturation current* $I_S^{sat} = I_S(V_{SD}^{sat}, V_{SG})$. The limit of the source conductance for $V_{SB} \to V_{DB}$, or $V_{SD} \to 0$, is

$$g_S(V_{SD} \to 0) = \beta\,(V_{SG} - V_T)\,,$$
$$V_T = -V_{FB} - 2\,\varphi_F + \gamma\sqrt{V_{BS} - 2\,\varphi_F}\,, \qquad (10.121)$$

with $V'_{GB} = V_{GB} - V_{FB}$ and $V_{BS} \geq 0$. The $V_T = V_T(V_{BS})$ voltage defined in (10.121) is the *threshold voltage* of the p-channel MOSFET; the condition of a well-formed channel in a p-channel MOSFET is $V_{SG} > V_T$.

Integrating of (10.115) yields $I_S = I'_S - I''_S$, with

$$I'_S = \beta\left[\left(V_{SG} + V_{FB} + 2\,\varphi_F\right)\,V_{SD} - \frac{1}{2}\,V_{SD}^2\right] \qquad (10.122)$$

and

$$I''_S = \beta\,\frac{2}{3}\,\gamma\,\left[(V_{SD} - 2\,\varphi_F + V_{BS})^{3/2} - (-2\,\varphi_F + V_{BS})^{3/2}\right]. \qquad (10.123)$$

Given V_{SG} and V_{BS}, the regional model separates the *on* condition $V_{SG} > V_T$ from the *off* condition $V_{SG} \leq V_T$; the *on* condition is further separated into the *linear region* $0 < V_{SD} \leq V_{SD}^{sat}$, where the source current is described by the $I_S = I'_S - I''_S$ model worked out above, and the *saturation region* $V_{SD} > V_{SD}^{sat}$, where the regional model lets $I_S = I_S^{sat}$. Finally, in the *off* condition, the model lets $I_S = 0$.

The *enhancement-type* p-channel transistors have $V_T > 0$, so that a gate voltage $V_{SG} > V_T > 0$ is necessary to achieve the condition of a well-formed channel, whereas the transistor is in the *off* condition when $V_{SG} = 0$; the *depletion-type* transistors have $V_T < 0$, so that the condition of a well-formed channel is already present when $V_{SG} = 0$, whereas a gate voltage $V_{SG} \leq V_T < 0$ is necessary to put the device in the *off* condition.

The *output characteristics* of the p-channel MOSFET are the $I_S = I_S(V_{SD})$ curves corresponding to different values of V_{SG}, for a given bulk-source voltage V_{BS}; the *transfer characteristics* are the $I_S = I_S(V_{SG})$ curves drawn using V_{BS} as a parameter and letting $V_{SD} = \text{const}$, with a value of V_{SD} small enough to let the limiting case (10.121) hold. The *transconductance* of the p-channel MOSFET is given by

$$g_m = \left(\frac{\partial I_S}{\partial V_{BG}}\right)_{V_{BS},V_{BD}} = \left(\frac{\partial I_S}{\partial V_{SG}}\right)_{V_{SD},V_{SB}} = \beta\,V_{SD}\,, \qquad (10.124)$$

and the *bulk transconductance* is given by

$$g_B = \left(\frac{\partial I_S}{\partial V_{SB}}\right)_{V_{SD},V_{SG}} = -\left(\frac{\partial I''_S}{\partial V_{BS}}\right)_{V_{SD}}. \qquad (10.125)$$

Like in the n-channel device, the body effect is suppressed by letting $V_{BS} = 0$; this is done whenever the architecture of the circuit makes it possible.

Linear-Parabolic Model, p-Channel

The expression of the current in a p-channel MOSFET is simplified by letting $I''_S \simeq \beta\,\gamma\,\sqrt{V_{BS} - 2\,\varphi_F}\,V_{SD}$, this yielding the *linear-parabolic model*. The reasoning is the same as in the n-channel MOSFET. The expression of the current becomes

$$I_S \simeq \beta\,[(V_{SG} - V_T)\,V_{SD} - V_{SD}^2/2]\,, \qquad (10.126)$$

with V_T still given by (10.121). In turn, from (10.126), the source conductance becomes

$$g_S \simeq \beta\,(V_{SG} - V_T - V_{SD})\,, \qquad (10.127)$$

whence

$$V_{SD}^{sat} = V_{SG} - V_T. \tag{10.128}$$

The transconductance g_m is the same as in the general case. Note that the linear-parabolic expression of the drain current may be recast as $I_S \simeq \beta\,(V_{SD}^{sat}\,V_{SD} - V_{SD}^2/2)$, with V_{SD}^{sat} given by (10.128). As a consequence,

$$I_S^{sat} \simeq \beta\left[\left(V_{SD}^{sat}\right)^2 - \frac{1}{2}\left(V_{SD}^{sat}\right)^2\right] = \frac{1}{2}\beta\,(V_{SG} - V_T)^2\,. \tag{10.129}$$

The linear-parabolic model then yields for the saturation region

$$I_S = I_S^{sat}\,, \qquad g_S \simeq 0\,, \qquad g_m \simeq \beta\,(V_{SG} - V_T)\,. \tag{10.130}$$

10.9 Saturation of the Drift Velocity

The MOSFET theory worked out so far is based on the assumption of a constant effective mobility μ_e along the channel. Actually, the drift velocity v_d of the carriers is proportional to the electric field E only for relatively small values of the latter and tends to saturate when E increases above a critical value of the order of 5×10^4 V cm^{-1}. A widely accepted model of the $v_d(E)$ relation dates back to the 1960s of the last century [18] and reads

$$v_d = \frac{\mu_e\,E}{\left[1 + (\mu_e\,E/v^{sat})^m\right]^{1/m}}\,, \tag{10.131}$$

where μ_e is the small-field carrier mobility, v^{sat} the saturation velocity of the carriers, and m an empirical parameter equal to 2 for electrons and approximately 1 for holes. For electric-field values $E \ll E_c = v^{sat}/\mu_e$, the drift velocity is proportional to E, while, in the opposite limit, $v_d \simeq v^{sat}$. The form of (10.131) suggests that the MOSFET drain current may be expressed heuristically as

$$I_D = \frac{I_D^{lin}}{\left[1 + \left(I_D^{lin}/I_D^{sat}\right)^m\right]^{1/m}}\,, \tag{10.132}$$

with

$$I_D^{lin} = \beta\,(V_{GS} - V_T)\,V_{DS}\,, \qquad I_D^{sat} = W\,C_{ox}\,(V_{GS} - V_T - V^{sat})\,v^{sat}. \tag{10.133}$$

In (10.133), I_D^{lin} is the drain current in the linear region, I_D^{sat} is the saturation current, and V^{sat} is the saturation voltage, i.e., the voltage value beyond which carriers move at saturated velocity. It is worth noting that, from the experimental standpoint, V^{sat} is an ill-defined parameter for two reasons: first, the drain current approaches saturation smoothly; next, the finite output conductance due to the short-channel effects does not allow for a clear identification of the saturation voltage. Even from the theoretical standpoint, it should be remembered that the second of (10.133) is based on the gradual-channel approximation (Sect. 10.7.1), which is not entirely valid at the saturation point due to the occurrence of two-dimensional effects near the drain. The intercept of I_D^{lin} with I_D^{sat} occurs at a voltage V_A such that

$$\beta\,(V_{GS} - V_T)\,V_A = W\,C_{ox}\,(V_{GS} - V_T - V^{sat})\,v^{sat}\,, \tag{10.134}$$

which establishes a relation between V_A and V^{sat}. On the other hand, for a long-channel MOSFET, (10.134) reduces to $\beta\,(V_{GS} - V_T)\,V_A = \beta\,(V_{GS} - V_T)^2/2$, whence

$$V_A = (V_{GS} - V_T)/2 = V^{sat}/2\,, \tag{10.135}$$

where the last equality is found by observing that for a long-channel device, V^{sat} identifies with V_{DS}^{sat} of (10.90). To proceed, one assumes that relation (10.135) between V_A and V^{sat} holds in general and not just for long-channel MOSFETs. Replacing (10.135) into (10.134) yields the following expression for V_A:

$$V_A = \frac{V_{GS} - V_T}{2 + \alpha\,(V_{GS} - V_T)}\,, \qquad \alpha = \frac{\mu_e}{v^{sat}\,L}. \tag{10.136}$$

It is easily found that when $\alpha\,(V_{GS} - V_T) \ll 2$, which occurs in long-channel MOSFETs and/or small values of $V_{GS} - V_T$, (10.136) becomes equivalent to (10.135). In the opposite limit, instead, V_A tends to saturate to $1/\alpha$. Using the first of (10.133) and the left-hand side of (10.134) yields $I_D^{lin}/I_D^{sat} = V_{DS}/V_A$; the drain current (10.132) then becomes

$$I_D = \beta\,\frac{(V_{GS} - V_T)\,V_{DS}}{\left[1 + (V_{DS}/V_A)^m\right]^{1/m}}\,, \tag{10.137}$$

which holds in both the linear and saturation regions, with V_A expressed by (10.136), and tends smoothly to the saturation current given by

$$I_D^{sat} = \beta\,\frac{(V_{GS} - V_T)^2}{2 + \alpha\,(V_{GS} - V_T)}. \tag{10.138}$$

Again, the impact of the saturated drift velocity becomes important when $\alpha\,(V_{GS} - V_T) \gg 2$, which typically occurs in short-channel MOSFETs at relatively large driving voltages. Under the above conditions, the growth of the drain current is no longer quadratic but, rather, linear with $V_{GS} - V_T$. Assuming by way of example $\mu_e = 200$ cm^2/(V s), $v^{sat} = 10^7$ cm/s, and $L = 100$ nm, corresponding to $\alpha = 2$ V^{-1}, the saturation current I_D^{sat} is halved at $V_{GS} - V_T = 1$ V with respect to the constant-mobility value $\beta\,(V_{GS} - V_T)^2/2$.

Figure 10.23 compares the output characteristics resulting from the linear-parabolic model (10.88), which assumes con-

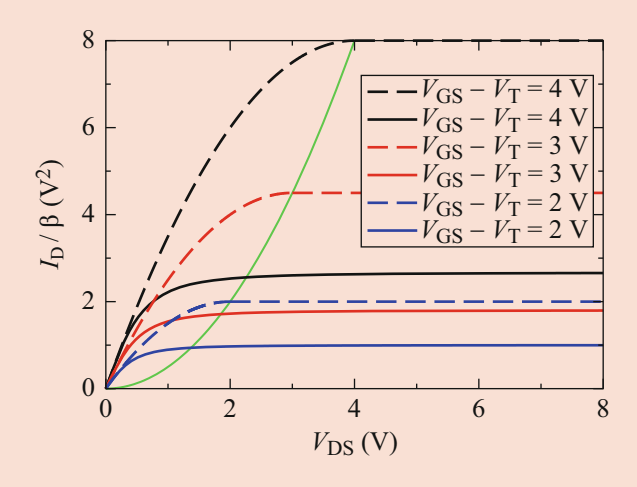

Fig. 10.23 The continuous lines have been obtained from (10.137) letting $\alpha = 1$ and $n = 2$. The dashed lines have been obtained from the linear-parabolic model (10.88). Curves corresponding to the same value of $V_{GS} - V_T$ are drawn in the same color. The green curve envelopes the saturation points of the dashed lines (compare with Fig. 10.19)

stant mobility along the channel, with those of the present model, accounting for the saturation of the drift velocity, and quantifies the strong discrepancies between the two. In order to check the model against experimental data, however, two more aspects must be taken into account. First, it is necessary to model the effective carrier mobility μ_e; next, the drain-induced barrier lowering (DIBL), i.e., the sensitivity of threshold to the drain voltage, must be taken into account. These issues are briefly discussed in Sect. 10.9.1.

10.9.1 Effective Mobility and Drain-Induced Barrier Lowering

The low-field mobility in MOSFET channels was widely investigated in the past. It was found to be essentially independent of channel doping and to follow a universal curve if plotted against the *effective normal field* E_{eff} [19–21]. This fundamental property was first demonstrated in [19] for n-channel MOSFETs and was later confirmed and extended to p-channel devices in [20,21]. More specifically, it was found that the room-temperature carrier mobility is mainly influenced by acoustic-phonon scattering at low normal fields and by surface-roughness scattering at the largest fields. The latter scattering effect turns out to depend on crystal orientation and exhibits different behaviors for electrons and holes. Therefore, different mobility models must be used for the two carrier types. The electron effective mobility μ_{ne} reads

$$\mu_{ne} = \frac{\mu_{n0}}{1 + \theta_{n1} E_{eff}^{0.3} + \theta_{n2} E_{eff}^{2}}, \qquad (10.139)$$

where the effective normal field is given by

$$E_{eff} = (Q_b + Q_i/2)/\varepsilon_{sc} = C_{ox} \left[(V_{GS} + V_T)/2 - (\Phi_{ms} + 2\varphi_F)\right]/\varepsilon_{sc}, \qquad (10.140)$$

Φ_{ms} being the metal-semiconductor work function difference. In turn, the hole effective mobility μ_{pe} reads

$$\mu_{pe} = \frac{\mu_{p0}}{1 + \theta_{p1} E_{eff}^{0.3} + \theta_{p2} E_{eff}}, \qquad (10.141)$$

with

$$E_{eff} = (Q_b + Q_i/3)/\varepsilon_{sc} = C_{ox} \left[|V_{GS} + V_T|/3 + (\Phi_{ms} + 2\varphi_F)\right]/\varepsilon_{sc}. \qquad (10.142)$$

In (10.139) and (10.141), θ_{n1}, θ_{n2}, θ_{p1}, and θ_{p2} are empirical parameters, whose units are such as to make the denominators of (10.139) and (10.141) dimensionless. It is worth noting that terms $\theta_{n1} E_{eff}^{0.3}$ and $\theta_{n2} E_{eff}^{2}$ in (10.139) account for acoustic-phonon and surface-roughness scattering, respectively, and so do the corresponding terms $\theta_{p1} E_{eff}^{0.3}$ and $\theta_{p2} E_{eff}$ in (10.141). These equations show that the surface-roughness dependence of the inverse mobility on the effective normal field is quadratic for electrons and linear for holes. Another important difference between electrons and holes appears in (10.140) and (10.142): the definition of effective normal field within the inversion layer given by the first of (10.140) is consistent with physical intuition; in contrast, the use of $Q_i/3$ rather than $Q_i/2$ in the first of (10.142) is just an empirical choice which gives the best fitting to experimental data [20,21].

The next point to be considered is drain-induced barrier lowering. In this case, the threshold change with drain voltage is approximately linear, i.e.,

$$V_{Tn} = V_{Tn}^{(0)} - \eta_n V_{DS}, \qquad V_{Tp} = V_{Tp}^{(0)} - \eta_p V_{SD}, \qquad (10.143)$$

where η_n and η_p depend on the gate length and are typically expressed in mV/V; for a good device design, they should be as small as possible. Figure 10.24 compares the model (10.137), supplemented with the first of (10.143), with the experimental output characteristics of an n-channel MOSFET having a gate length $L = 130$ nm, an oxide thickness $t_{ox} = 2$ nm, and a nominal threshold voltage $V_{Tn}^{(0)} = 315$ mV. The model fits the experimental curves nicely.

It is worth adding that the model shown here contains a minimal number of parameters; most of them are physical or geometrical parameters, e.g., Φ_{ms}, φ_F, ε_{ox}, ε_{sc}, v^{sat}, W, L, and t_{ox}, and their values are kept fixed. The parameters adjusted for a best fit are those related with mobility and DIBL, namely, μ_{n0}, θ_{n1}, θ_{n2}, η_n, and the like for holes. The mobility parameters are, to some extent, process dependent

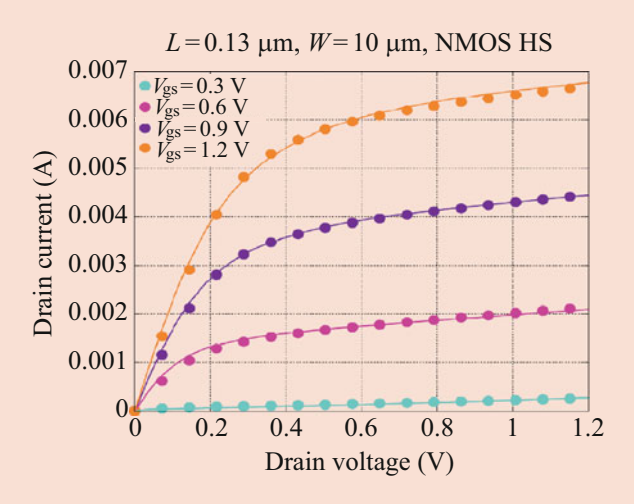

Fig. 10.24 Comparison of the model of (10.137) with experiments. The details about the device are given in the text

and must be determined from a best fit of the device under examination; in turn, the drain-induced barrier lowering factors η_n and η_p depend on two-dimensional effects that are not treated in this context.

The drain conductance g_D and transconductance g_m are derived from (10.137); considering by way of example the n-channel device, one uses definitions (10.77, 10.85) to find

$$g_D = \beta \frac{V_{GS} - V_T}{[1 + (V_{DS}/V_A)^m]^{1+1/m}}, \tag{10.144}$$

whose $V_{DS} \ll V_A$ limit coincides with (10.82). The form of g_D in the other limiting case, $V_{DS} \gg V_A$, is $g_D \simeq \beta (V_{GS} - V_T) (V_A/V_{DS})^{m+1}$ and vanishes when V_{DS} becomes very large. The expression of the transconductance g_m is somewhat unwieldy and is not reported here; its $V_{DS} \ll V_A$ limit coincides with (10.85), whereas the form of the other limiting case, $V_{DS} \gg V_A$, is

$$g_m \simeq \beta V_A \left[1 + \frac{2}{2 + \alpha (V_{GS} - V_T)}\right]. \tag{10.145}$$

10.10 Charge-Transfer Devices

The development of solid-state sensors has intensively been pursued since the late 1960s of the last century, due to the advantages of this class of devices over the then-standard cathode-ray tubes, specifically, (a) low bias voltages and small power absorption; (b) reliability, durability, and compactness; (c) immunity from e.m. fields; and (d) low noise even at moderate illumination levels. Another advantage must be mentioned, related to the architecture of color cameras for video applications: in a cathode-ray camera, it is necessary to guarantee, besides a precise alignment of three tubes (respectively, sensing the red, green, and blue colors), also a perfect – and constant in time – alignment of three electron beams. In a solid-state camera, instead, the transformation of the video signal into a discrete sequence, along with the application of a single clock signal to three sensors, automatically synchronizes the signals associated with the color components; therefore, only the alignment of the three sensors must be cared for.

The first implementations of solid-state optical sensors were made by assembling in matrix form a number of independently addressable elementary sensors; however, this architecture is inadequate, because a separate addressing entails:

1. High output capacitance due to the address lines.
2. Spurious coupling among the signals, still due to the address lines.
3. Lack of uniformity, impossible to avoid, due to the fact that each signal is read at a different output.

Consequences of the above are a modest signal-to-noise ratio, and the presence of fixed patterns in the output signal, due to the lack of uniformity. Such patterns cannot be eliminated by filtering.

A breakthrough came from the introduction of the charge-transfer device (CTD), which is the object of the next paragraphs. The name of the device derives from its capability of transferring a charge packet, in a controlled manner, from the potential-energy well underneath a gate to the well underneath a neighboring gate. The two most important CTD architectures, both able to eliminate the inadequacies listed above, are the Charge-Coupled Device (CCD), described in Sect. 10.10.1, and the Charge-Injection Device (CID), described in Sect. 10.10.3. Some applications are illustrated in Sect. 10.11 and, finally, the performance of image sensors is briefly discussed in Sect. 10.12.

10.10.1 Charge-Coupled Devices

To describe the functioning of a Charge-Coupled Device (CCD) it is convenient to start with a pair of MOS capacitors placed side by side, like those shown in Fig. 10.25. The two gates are labeled 1 and 2, respectively, and the corresponding voltages are indicated with Φ_1 and Φ_2 (in this context the gate voltages are referred to as *phases*). The description of each capacitor is the same as that given in Sect. 10.4 with reference to the photocapacitor; it is assumed that the substrate is of the p-type and that the phases are periodically switched between the flat-band voltage (indicated here with V_L) and another voltage (indicated with V_H) that, in the

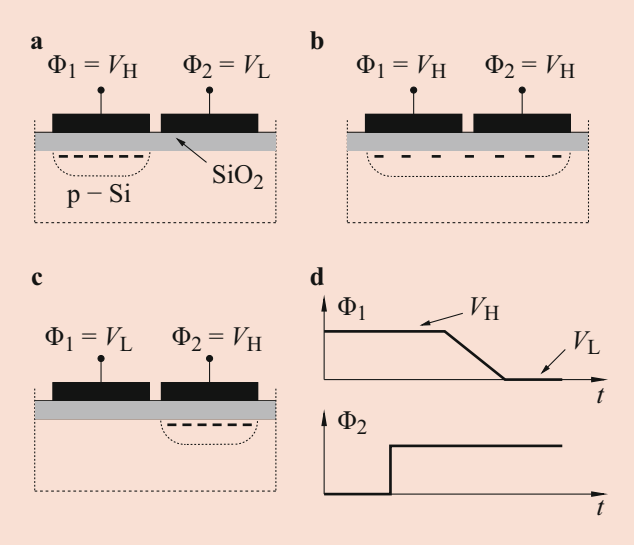

Fig. 10.25 Cross-section of a pair of MOS capacitors forming the basic element of a CCD: parts (**a**-**c**) illustrate the charge-transfer mechanism, part (**d**) sketches the form of the phases

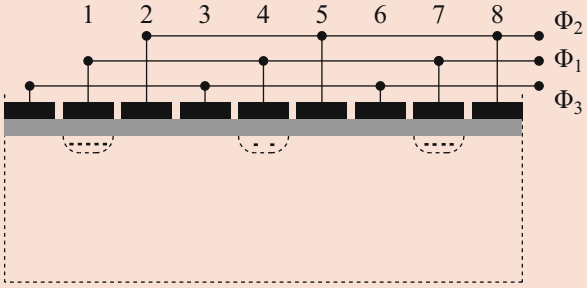

Fig. 10.26 A portion of a three-phase CCD

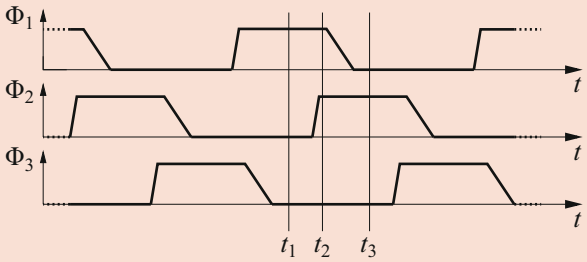

Fig. 10.27 Time dependence of the three phases of the CCD shown in Fig. 10.26

steady-state condition, corresponds to strong inversion. Voltage V_H produces a potential-energy well in the semiconductor region which is underneath gate 1 near the interface with the insulator; an inversion layer is present at the interface, with a charge per unit area that in this context represents a signal; in turn, Φ_2 is kept at V_L (part (a) of Fig. 10.25). If, at a later time, Φ_2 is brought from V_L to V_H, another well forms underneath gate 2; due to the proximity of the two gates, the two wells merge and form a single well in which the charge originally present under gate 1 distributes uniformly (part (b) of the figure). If, then, Φ_1 is gradually brought to V_L, the charge that is still under gate 1 is pushed by the electric field into the well of gate 2 (part (c)). Globally, the result is the transfer of a mobile-charge packet from capacitor 1 to capacitor 2; the transfer is controlled in space by the geometry of the electrodes and in time by the form of the phases (the latter is sketched in part (d) of Fig. 10.25).

The principle of charge transfer illustrated above is easily extended to a succession of equal capacitors, close to each other, whose gates are biased by a three-phase system of voltages (*clock*). This succession of capacitors is the *three-phase CCD*; a portion of it is shown in Fig. 10.26, and the time dependence of the three phases is shown in Fig. 10.27.

With reference to the figures, it is easily found that, at time t_1, being $\Phi_1 = V_H$ and $\Phi_2 = \Phi_3 = V_L$, the charge packets are placed under gates 1, 4, and 7, respectively; at time t_2, being $\Phi_1 = \Phi_2 = V_H$ and $\Phi_3 = V_L$, the charge packets equally distribute under the pairs of gates (1, 2), (4, 5), and (7, 8); at time t_3, being $\Phi_1 = \Phi_3 = V_L$ and $\Phi_2 = V_H$, the transfer of the charge packets under gates 2, 5, and 8 is completed; and so on.

The above description shows that in a three-phase CCD, the elementary cell of the device is made of three capacitors and that the charge packets perform three transfers in a clock period T. It is easily understood that the three-phase architecture is necessary to ensure the one-directional transfer of the packets (from left to right in the examples); architectures featuring cells made of four capacitors have also been implemented. One may wonder whether a two-phase architecture is feasible; the answer is obviously in the negative for symmetric electrodes: in this case, in fact, when $\Phi_1 = \Phi_2 = V_H$, the charge packets would mix, and the information associated with them would be lost. If, instead, a suitable asymmetry of the electrodes is introduced, able to force the one-directional transfer of the packets, the two-phase architecture is feasible (details about the CCD architectures are found, e.g., in [22, 23]).

In the CCD described in Figs. 10.25 and 10.26, the charge packets are placed at the semiconductor-insulator interface; for this reason, the device is also called "surface-channel CCD" (SCCD); by adding a suitable epitaxial layer (here an n-type layer grown over the p-type substrate), it is possible to place the charge packets far from the insulator interface: this implementation, called "buried-channel CCD" (BCCD), although more complicated from the technological viewpoint, provides a better transfer efficiency with respect to SCCD (transfer efficiency is discussed in Sect. 10.10.2).

A CCD as a whole is made of three sections: an input section in which an electric or optical signal is sampled and transformed into a sequence of charge packets; a transfer section, a portion of which has been described above; and an output section, in which the charge packets are converted back into a sampled electric signal. Observing that the CCD is intrinsically an analog delay line carrying a sampled signal, it is possible to exploit the device for realizing analog filters. Another application derives from the idea of considering a well full (empty) of electrons as representative of the logic level 1 (0): in this way, the CCD may be used as a shift register (serial memory). Still another application considers the CCD as a device able to transfer optically generated charge packets into a single output section; this makes the realization of image sensors possible. Some of these applications are briefly addressed in Sect. 10.11.

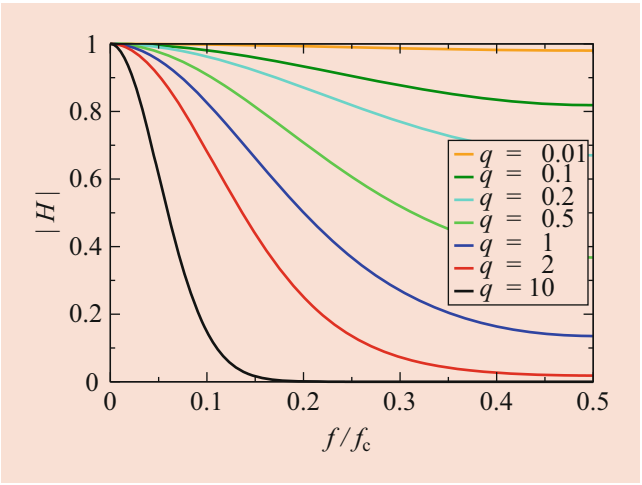

Fig. 10.28 Transfer function (10.150) in terms of f/f_c for different values of parameter $q = N\,p\,\varepsilon$

10.10.2 Transfer Efficiency

Due to the limited time available for the charge packet to leave a well and transfer into the next, some electrons are left behind and eventually mix with the new packet entering the well; this produces a degradation of the quality of the signal. Another degradation mechanism, typical of SCCDs, is that some electrons may temporarily be trapped in the surface states, to be subsequently released into the incoming packet. The fraction ε of electrons left behind for any reason, in a single transfer, is called *transfer inefficiency*; typical figures are $\varepsilon = 10^{-4}$ in SCCDs and $\varepsilon = 10^{-5}$ in BCCDs. Letting p be the number of phases, the inefficiency associated with a full-cell transfer is $p\,\varepsilon$, and the charge present at time t_n in the kth cell reads [24]

$$Q_k(t_n) = (1 - p\,\varepsilon)\,Q_{k-1}(t_{n-1}) + p\,\varepsilon\,Q_k(t_{n-1}). \quad (10.146)$$

The impulse response associated with the transfer from the $(k-1)$th to the kth cell is

$$\begin{aligned} h_k(t_n) &= (1 - p\,\varepsilon)\,(p\,\varepsilon)^{n-1}\,, \quad n > 0\,; \\ h_k(t_n) &= 0\,, \quad n \le 0\,, \end{aligned} \quad (10.147)$$

whose discrete Fourier transform reads [25, p. 257–262]

$$\begin{aligned} F_k(\mathrm{i}\,\omega) &= \sum_{n=1}^{\infty} (1 - p\,\varepsilon)\,(p\,\varepsilon)^{n-1} \exp(-\mathrm{i}\,\omega\,n\,T) \\ &= \frac{(1 - p\,\varepsilon)\,\exp(-\mathrm{i}\,\omega\,T)}{1 - p\,\varepsilon\,\exp(-\mathrm{i}\,\omega\,T)}. \end{aligned} \quad (10.148)$$

For an N-cell device, the full transfer function is $H(\mathrm{i}\,\omega) = [F_k(\mathrm{i}\,\omega)]^N$, namely, using the approximation $(1-\theta)^N = \exp[N\,\log(1-\theta)] \simeq \exp(-N\,\theta)$ holding for $|\theta| \ll 1$,

$$\begin{aligned} H(\mathrm{i}\,\omega) &\simeq \exp(-\mathrm{i}\,\omega\,N\,T)\,\exp\{-q\,[1 - \exp(-\mathrm{i}\,\omega\,T)]\}, \\ q &= N\,p\,\varepsilon. \end{aligned} \quad (10.149)$$

Letting $f_c = 1/T$ be the clock frequency, the modulus of (10.149) reads

$$|H| = \exp\{-q\,[1 - \cos(\omega\,T)]\} = \exp\{-q\,[1 - \cos(2\,\pi\,f/f_c)]\}. \quad (10.150)$$

The form of $|H|$ obtained from (10.150) is shown in Fig. 10.28 for different values of q. When q increases, the transfer function quickly deteriorates, introducing a strong attenuation in the spectral components near $f_c/2$. Remembering Shannon's sampling theorem, such a frequency represents the maximum extension allowed for the spectrum of the input signal.

10.10.3 Charge-Injection Devices

A schematic cross-section of the elementary cell of a charge-injection device (CID) is shown in Fig. 10.29a. An image sensor of the CID type is made of an array of identical cells; in turn, each cell is made of a pair of MOS photocapacitors, whose gate voltages are indicated with V_r and V_c, respectively; like in Sect. 10.10.1, a p-type substrate is assumed, and the two possible levels of gate voltages are indicated with V_H and V_L. During the integration time, one or both gate voltages are kept at V_H, so that a potential-energy well is available to collect the optically generated charge; by way of example, in Fig. 10.29, it is $V_c = V_H$ and $V_r = V_L$. The reading of the integrated charge is carried out by setting both gates to V_L; in this way, the charge is injected through the substrate into the bulk contact B and then brought to the output section of the array.

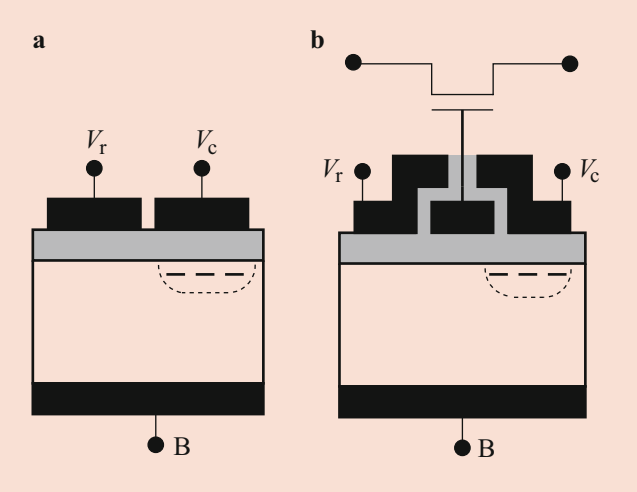

Fig. 10.29 (**a**) Elementary cell of a CID; the two photocapacitors are subjected to independent gate voltages V_r and V_c. (**b**) The same cell with the addition of a floating gate between the two gates; the connection of the floating gate to the gate of an MOS transistor is shown as an example of charge reading

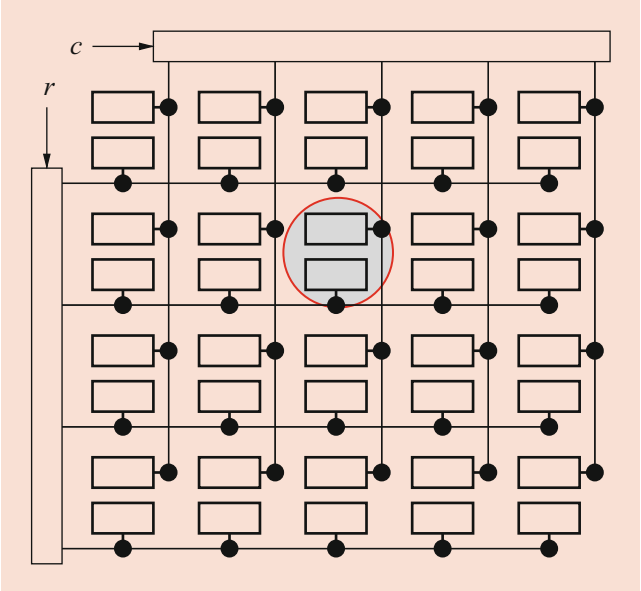

Fig. 10.30 Top view of a CID array. The reading of the marked cell is described in the text

Besides the injection into the substrate, another operation is possible in the CID cell, namely, the right-to-left transfer of a charge packet or vice versa. This is accomplished in the same manner as in a CCD: assume, for instance, that a packet is stored under the right gate, so that $V_c = V_H$ and $V_r = V_L$; first, V_r is brought to V_H, this making the charge to equally distribute under the two gates; finally, V_c is brought to V_L, this completing the transfer. If the packet is initially stored under the left gate, the left-to-right transfer is accomplished by the sequence $V_c \rightarrow V_H$, $V_r \rightarrow V_L$. The transfer feature of the CID cell makes it possible to separately read each cell of the array, in any order. This is easily understood by examining a top view of the array (Fig. 10.30); to read the charged stored, e.g., in the cell marked with a circle, it suffices to operate on the column control c and the row control r: the V_c voltage of the column to which the marked cell belongs is set to V_L, and the V_r voltage of the row of the marked cell is also set to V_L; all remaining columns and rows are set to V_H. In this way, each cell apart from the marked one has at least one gate set at V_H, so that the charge packet either remains under the same gate, or transfers into the other one, or distributes between the two; in contrast, both gates of the marked cell are set to V_L, so the charge is injected into the bulk.

Image sensors using CIDs have demonstrated very good performance and provided a valid alternative to CCDs. It is worth adding that some CIDs, instead of reading the packets by injecting them into the bulk, adopt a reading scheme based on the floating gate. The structure of a CID with the floating gate is shown in Fig. 10.29b; in the figure, the floating gate is connected to the gate of an MOS transistor to show an example of how to detect the variations in the floating-gate voltage without perturbing the operation of the CID (the voltage-charge relation of the floating gate is derived in Sect. 10.10.4). Being non-destructive, the reading based on the floating gate can be carried out repeatedly, with beneficial effects in terms of noise reduction. In low-temperature experiments, the reading of an image has been performed more than 30,000 times without any appreciable degradation; this corresponds to the average loss of less than one electron per reading [26].

10.10.4 Floating-Gate Operation

The analysis of the floating-gate operation is carried out following the theory of the MOS capacitor of Sects. 10.1, 10.2, and 10.3. The symbols used here are visible in Fig. 10.31, where Q_x are charges per unit area and C_x capacitances per unit area; in essence, the device is based on the structure of the MOS capacitor, to which another metal-insulator pair of layers is added. As the state of the intermediate capacitor C_L and so the value of its gate voltage V'_F are determined by electrostatic induction, the metal layer between C_U and C_L is termed *floating gate*; this layer is accessed via a zero-admittance line, in order to detect the voltage V'_F without perturbing the working conditions of the device.

As usual, $V'_G = V_G - V_{FB}$, with V_{FB} the flat-band voltage, indicates the potential difference between the external gate and the semiconductor bulk; similarly, $V'_F = V_F - V_{FB}$ indicates the potential difference between the floating gate and the same bulk (V_G and V_F are referred, instead, to the bulk contact). A p-type substrate is considered; remembering

that the range of gate voltages to be used here is such that the depletion, weak-inversion, or strong-inversion regimes hold, the simplified expression (10.29) of the inversion-layer charge applies,

$$Q_\mathrm{i} = -C_\mathrm{L}\left(V'_\mathrm{F} - \varphi_\mathrm{s} - \gamma\sqrt{\varphi_\mathrm{s}}\right), \qquad \varphi_\mathrm{s} \geq 0. \tag{10.151}$$

If no net charge is present in the floating gate, it is $Q_\mathrm{U} = Q_\mathrm{L}$, whence

$$C_\mathrm{U}\left(V'_\mathrm{G} - V'_\mathrm{F}\right) = \frac{C_\mathrm{U}\,C_\mathrm{L}}{C_\mathrm{U} + C_\mathrm{L}}\left(V'_\mathrm{G} - \varphi_\mathrm{s}\right). \tag{10.152}$$

Solving (10.152) for φ_s or $V'_\mathrm{F} - \varphi_\mathrm{s}$ after letting $r = C_\mathrm{U}/C_\mathrm{L}$ yields $\varphi_\mathrm{s} = (1+r)\,V'_\mathrm{F} - r\,V'_\mathrm{G}$ and $V'_\mathrm{F} - \varphi_\mathrm{s} = r\left(V'_\mathrm{G} - V'_\mathrm{F}\right)$. As the above expressions hold only for $\varphi_\mathrm{s} \geq 0$, it follows $r\,V'_\mathrm{G}/(1+r) \leq V'_\mathrm{F} \leq V'_\mathrm{G}$; replacing the expressions into (10.151) yields the relation between the inversion-layer charge and the floating-gate voltage,

$$-\frac{Q_\mathrm{i}}{C_\mathrm{L}\,V'_\mathrm{G}} = r\,(1 - V'_\mathrm{F}/V'_\mathrm{G}) - \alpha\sqrt{(1+r)\,V'_\mathrm{F}/V'_\mathrm{G} - r},$$
$$\alpha = \frac{\gamma}{\sqrt{V'_\mathrm{G}}}, \tag{10.153}$$

which is shown in Fig. 10.32 for different values of r and α. The curves show that with $\alpha = 0.01$, the $Q_\mathrm{i}(V'_\mathrm{F})$ relation exhibits good linearity; the linearity is still fair for $\alpha = 0.2$, which is a more realistic value in modern technologies. It is worth observing that a similar procedure is feasible also when some charge per unit area is stored in the floating gate, e.g., $Q_\mathrm{L} - Q_\mathrm{U} = Q_0 \neq 0$; in this case, letting $q_0 = Q_0/(C_\mathrm{L}\,V'_\mathrm{G})$, (10.153) is replaced with

$$-\frac{Q_\mathrm{i}}{C_\mathrm{L}\,V'_\mathrm{G}} = r\,(1 - V'_\mathrm{F}/V'_\mathrm{G}) + q_0 - \alpha\sqrt{(1+r)\,V'_\mathrm{F}/V'_\mathrm{G} - r - q_0}. \tag{10.154}$$

10.11 Applications of CCDs

Among the applications mentioned in Sect. 10.10.1, those related to the implementation of memories or analog filters have been attempted in the early 1970s of the last century, but have soon been superseded by more efficient architectures. The realization of image sensors, instead, has been more successful, although other architectures eventually proved more efficient also in this field (an example is the CID matrix illustrated in Sect. 10.10.3). The scheme for realizing an analog filter is briefly illustrated in Sect. 10.11.1, while typical implementations of image sensors using CCDs are described in some detail in Sect. 10.11.2.

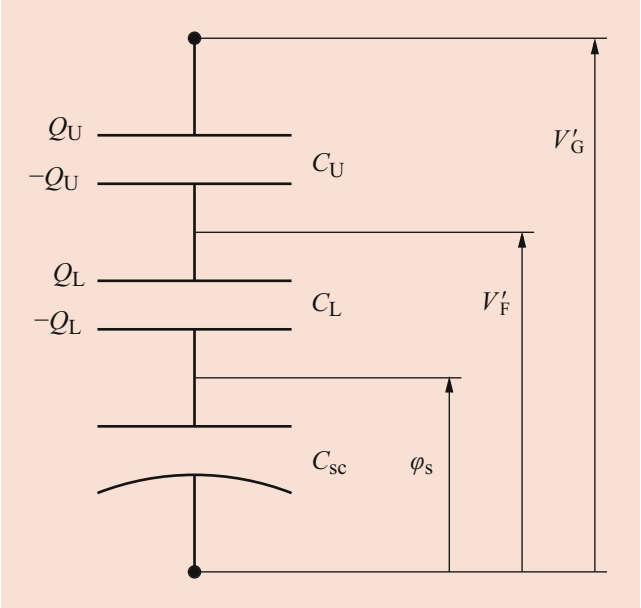

Fig. 10.31 Equivalent circuit of the floating-gate scheme based on an MOS capacitor. The lower plate of the semiconductor capacitance C_sc is bent to indicate that this capacitance is nonlinear

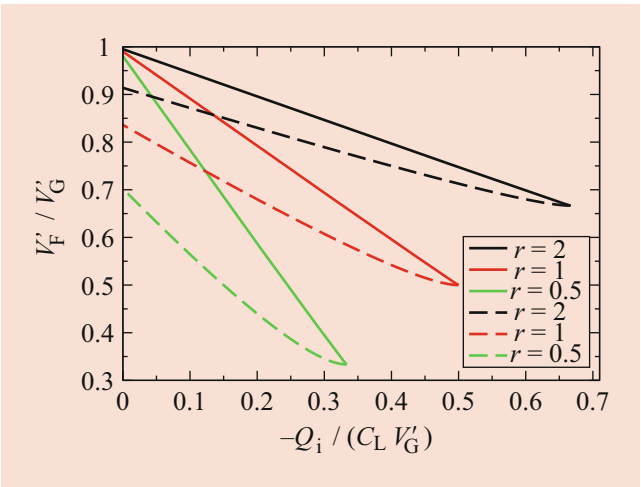

Fig. 10.32 The floating-gate voltage as a function of the inversion-layer charge for different values of $r = C_\mathrm{U}/C_\mathrm{L}$. All curves fulfill the constraint $V'_\mathrm{F}/V'_\mathrm{G} \geq r/(r+1)$. Parameter α has been fixed to 0.01 (*continuous lines*) or 0.2 (*dashed lines*)

10.11.1 Applications to Analog Filtering

As mentioned in Sect. 10.10.1, the realization of an analog filter with a CCD is based on the observation that the device is an analog delay line carrying a sampled signal; the goal is to implement with it a prescribed transfer function $H(\omega)$ acting on the input signal $w(t)$ of the CCD. It can be shown that, if one succeeds in performing a non-destructive reading of the samples, a suitable linear combination of the samples provides a convolution of the input signal with the antitrans-

form $h(t)$ of $H(\omega)$; the antitransform depends only on the coefficients of the combination, which are easily controlled. In this way, it is possible to construct the transfer function sought. This application of CCDs has been the first, and very elegant, example of realization of a filter within the integrated-circuit technology. The main reason why it has not been pursued further is the insufficient attenuation in the stopband.

The input function $w(t)$ is transformed by the input section of the filter into a sequence of charge packets whose size depends linearly on the input signal itself (some indications about the linearity of input sections are given in Sect. 10.12.2); it follows that the charge packets may be considered as samples of w taken at different times 0, T, $2T$, and so on, with T the clock period. The filtering operation is based on the properties of the Fourier transform,

$$W(\omega) = \mathscr{F}w = \int_{-\infty}^{+\infty} w(t)\, \exp(-\mathrm{i}\,\omega\, t)\, \mathrm{d}t\,, \qquad (10.155)$$

and of the convolution integral describing the output signal $u(t)$,

$$u(t) = h(t) * w(t) = \frac{1}{2\,\pi} \int_{-\infty}^{+\infty} h(t')\, w(t-t')\, \mathrm{d}t' = \mathscr{F}^{-1}(H\, W), \qquad (10.156)$$

with $H(\omega) = \mathscr{F}h$ the transfer function of the filter. For the physical realizability of H, it must be $h(t') = 0$ for $t' < 0$, whence $\int_{-\infty}^{+\infty}$ of (10.156) must be replaced with $\int_{0}^{+\infty}$. Observing that the discrete form of (10.156) is

$$u(t) = \frac{1}{2\,\pi} \sum_{k=0}^{\infty} h(t'_k)\, w(t-t'_k)\, T \simeq \sum_{k=0}^{n} a_k\, w(t-k\,T)\,, \qquad (10.157)$$

with $t'_k = k\,T$ and $a_k = h(t'_k)\, T/(2\,\pi)$, the issue is using a CCD to construct the last expression on the right in (10.157). The procedure is understood with the aid of Fig. 10.33, showing that the signal is sampled at the end of each cell, so that the time distance between two neighboring samples is the clock period T. To avoid deteriorating the signal, the sampling operation must be performed in a non-destructive way; this is achieved by the floating-gate scheme illustrated in Sect. 10.10.4 which renders, for each cell, a voltage $w(t-k\,T)$ that depends linearly on the charge of the packet that has crossed the cell. Then, each sampled signal is given an amplification equal to a_k, and, finally, the amplified voltages are added up to form the output signal $u(t)$. It is manifestly inconvenient to associate an amplifier to each cell; this is avoided by observing that (10.157) can be recast as

$$u(t) = \sum_{k=0}^{n} a_k\, w(t-k\,T) = a_{\mathrm{M}} \sum_{k=0}^{n} \frac{a_k}{a_{\mathrm{M}}}\, w(t-k\,T),$$

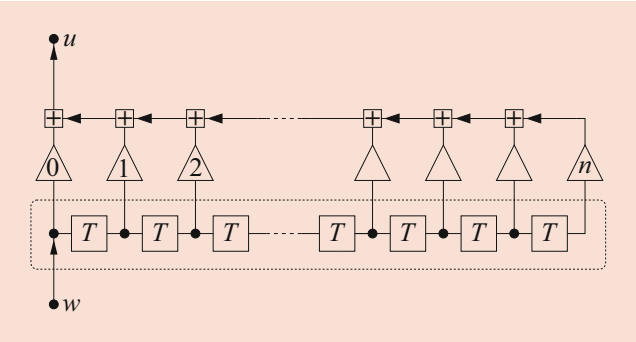

Fig. 10.33 Scheme of the analog filter using a delay line. The CCD is inside the dashed line, with the squares indicating the cells; the charge packets travel from left to right (input and output sections not shown). The triangles represent the amplifications a_k of (10.157) and (10.158)

$$a_{\mathrm{M}} = \max(a_k)\,, \qquad (10.158)$$

so that the problem reduces to implementing n attenuations $0 \le a_k/a_{\mathrm{M}} \le 1$ and a single amplification with gain a_{M}. Achieving the attenuations is relatively easy: it suffices in fact to shorten the width of the kth floating gate ($k = 1, \ldots, n$) from the original value W to $a_k\, W/a_{\mathrm{M}}$, so that only the fraction a_k/a_{M} of the packet that has traveled across the kth cell is detected. The shortening of the floating-gate widths is achieved with a single mask during the fabrication process.

10.11.2 Applications to Optical Sensing

Image sensors based on CCDs belong to two main categories: linear sensors and two-dimensional sensors. The most efficient organizations of the linear sensors are shown in Fig. 10.34; both types are made of a one-dimensional array of MOS photocapacitors, but differ in the method with which the charge packets are transferred to the output section. For simplicity, the oblique arrows visible in Fig. 10.34, which sketch the incoming light, are drawn only on some locations of the sensors; obviously, the radiation impinges everywhere on the sensor surface.

Considering a three-phase organization like that shown in Fig. 10.26, in the linear sensor indicated with (a) in Fig. 10.34, the phases are kept fixed in time during the integration period; one of them, say, Φ_1, is kept at V_{H}, so that the potential-energy wells of the corresponding photocapacitors integrate the optically generated charge. Phases Φ_2 and Φ_3 are kept at V_{L} to prevent the generated packets from mixing. At the end of the integration period, the clock is operated, and the charge packets are transferred along the CCD (here from left to right) and brought to the output section (sketched by the triangle in the figure). This organization is simple, but has the disadvantage that, during

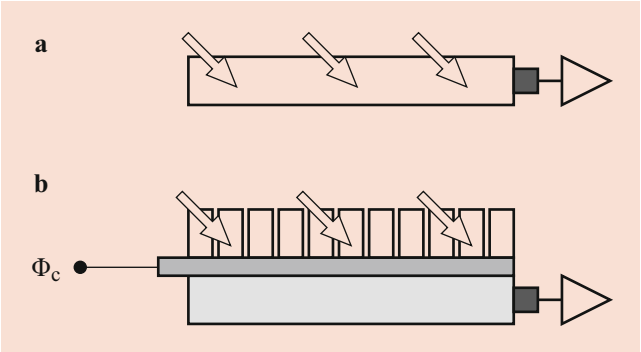

Fig. 10.34 Top view of the two typical organizations of linear image sensors using CCDs

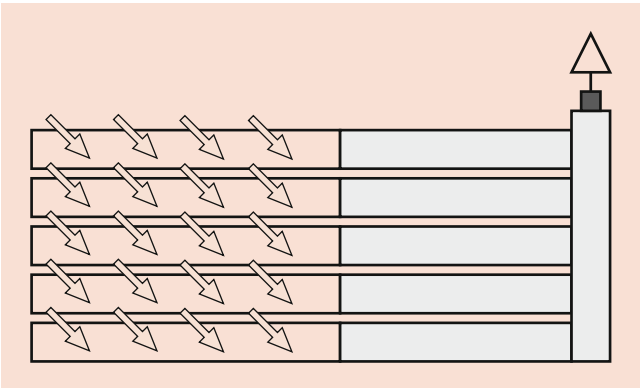

Fig. 10.35 Top view of a frame-transfer image sensor using CCDs

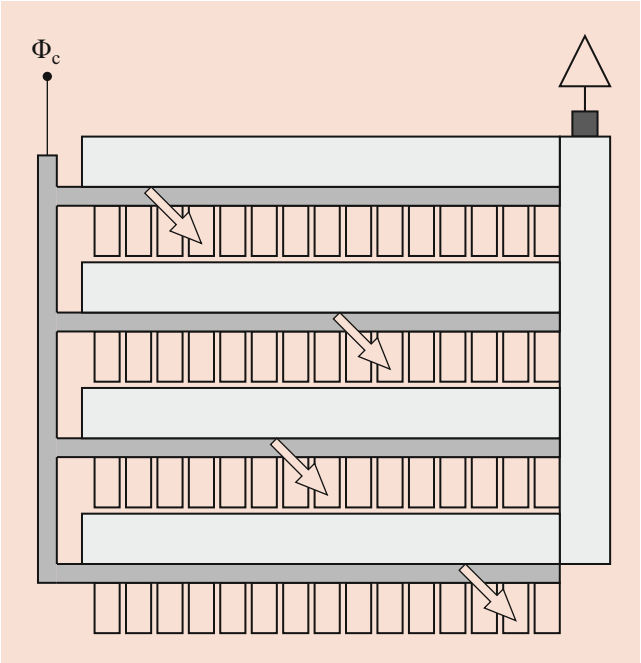

Fig. 10.36 Top view of a line-transfer image sensor using CCDs

the transfer of the packets to the output section, the impinging light keeps generating new charges: the latter add up to the transiting packets and degrade the quality of the image. To minimize the effect, it is necessary to use a high clock frequency.

A more effective solution is shown in part (b) of Fig. 10.34; here, the array of photocapacitors (the white rectangles in the figure) integrates the charge until the integration period is complete; then, by applying a signal Φ_c to the longitudinal gate (the dark-gray strip), the packets are transferred in parallel into the CCD below, which is screened from the radiation by a protective coating. The CCD transfers the packets to the output section. This organization, although more complicated than that of (a) and more onerous in terms of area occupancy, has the advantages of eliminating the spurious generation and of providing a duty cycle practically equal to 100%; moreover, it is less demanding as far as the clock frequency is concerned, because the transfer of the charge packets to the output section takes place during the integration period.

Array image sensors based on CCDs are essentially two-dimensional replicas of the architectures illustrated above. The array corresponding to case (a) of Fig. 10.34 is shown in Fig. 10.35 and is termed *frame-transfer sensor*. At the end of the integration period, the charge packets present in the integration area (the white part on the left) are transferred into the storage area (the gray part); the portion of each CCD belonging to the storage area is screened from the radiation by a protective coating. Then, the charge packets at the right end of the storage area are transferred into the vertical CCD, which finally transfers the packets (in the bottom-up direction) into the output section. To achieve this, the clock frequency of the vertical CCD is a multiple of that of the horizontal ones, the multiplicative factor being the number of rows of the array; in summary, the reading operation introduces a parallel-to-series conversion of the order of the packets.

The array corresponding to case (b) of Fig. 10.34 is shown in Fig. 10.36 and is termed *line-transfer sensor*. At the end of the integration period, a suitable signal Φ_c is applied to the common gate, and the charge packets integrated in each of the one-dimensional arrays of photocapacitors are transferred in parallel into the corresponding CCD, which is screened from the radiation. Then, the horizontal CCDs transfer the packets (left to right) into the vertical CCD, which in turn transfers them (bottom-up) into the output section. Also in this case, the clock frequency of the vertical CCD is a multiple of that of the horizontal ones, and a parallel-to-series conversion of the order of packets takes place.

The advantages or disadvantages of the two implementations of Figs. 10.35 and 10.36 are the same as in the one-dimensional case described earlier. It is worth adding that the frame-transfer scheme provides an easy and elegant solution

to the problem of video interlacing, present in some types of displays. It suffices in fact to control the clock in such a way that, from one integration period to the next, the gates subjected to V_H are swapped with those subjected to V_L; besides solving the interlacing problem, this method practically doubles the spatial frequency of the sampling, this improving the resolution of the image. The gate swapping is not possible, instead, in the line-transfer scheme; considering this aspect, it is found that the performance of the two schemes is substantially the same for a given area of the sensor.

Before concluding the paragraph, it is important to mention a different architecture for imagers, the active-pixel sensor (APS), in which each individual photodetector is supplemented with one or more active devices used as amplifiers; in the typical implementation based on the MOS technology, the amplifier is of the CMOS type. An early and detailed comparison between the performance of CCD and APS imagers is carried out in [27], with a shorter section devoted to CIDs.

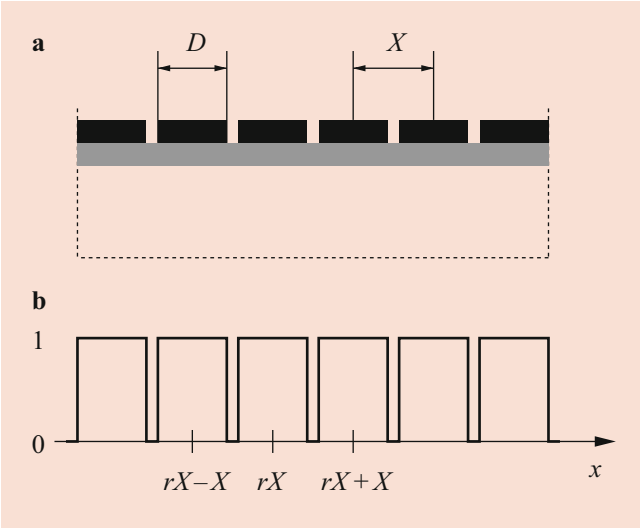

Fig. 10.37 (**a**) Cross-section of a linear image sensor and (**b**) corresponding sampling function

10.12 Performances of Image Sensors

The first part of this section addresses a fundamental aspect of image sensors, namely, spatial resolution; the second part briefly illustrates other aspects, still related to the image-sensor performances: dynamics, linearity, *blooming* effect, spectral responsivity, and sensitivity.

10.12.1 Spatial Resolution

A fundamental property of an image sensor is spatial resolution. Considering for simplicity a linear sensor (Fig. 10.37a), it is readily understood that the device performs a spatial sampling of the image, whose period X is the distance between the midpoints of the individual sensors; due to Shannon's theorem, the maximum spatial frequency that can be resolved is $f_M = 1/(2X)$. When a signal $n(x)$ is sampled with a series of pulses δ of frequency $f_0 = 1/X = 2f_M$, the spectrum of $n(x)$ is replicated periodically with the same frequency f_0; as a consequence, the frequencies of the spectrum of $n(x)$ that are larger than f_M are reflected into the bandwidth and, therefore, cannot be eliminated by filtering. The effect, termed *aliasing*, is shown in Fig. 10.38. In image sensors, the effect is made more complicated by two factors:

(i) The sampling function is not a series of δ pulses; to first order one may describe it as a square wave (Fig. 10.37b).
(ii) The output signal is not the product of the input signal and the sampling function but, rather, the integral of this product.

Basing on the considerations above, the analysis of the sampling operation is carried out by observing that, here, $n(x)$ is the number of charges generated per unit length during the integration period; it follows that the signal associated with the rth elementary sensor is the total charge present in it, given by

$$q\,s(rX) = q\int_{x_-}^{x_+} n(x)\,\mathrm{d}x\,, \qquad x_\pm = rX \pm D/2. \quad (10.159)$$

The output of the image sensor is therefore the discrete sequence $s(rX)$, whose spectrum is calculated following [28]. If $N(k)$ is the Fourier transform of $n(x)$, with $k = 2\pi f$, from (10.159), one obtains

$$s(rX) = \frac{1}{2\pi}\int_{-\infty}^{+\infty} N(k)\,H(k)\,\exp(\mathrm{i}\,k\,rX)\,\mathrm{d}k\,, \quad (10.160)$$

with $H(k) = D\,\sin(kD/2)/(kD/2)$. Letting $W(k) = N(k)\,H(k)$, and parting the integration interval into segments of length $2\pi/X$ after defining $k_\pm = (2m \pm 1)\,\pi/X$, one obtains

$$\begin{aligned} s(rX) &= \sum_{m=-\infty}^{+\infty}\int_{k_-}^{k_+} W(k)\,\frac{\exp(\mathrm{i}\,k\,rX)}{2\pi}\,\mathrm{d}k \\ &= \frac{X}{2\pi}\int_{-\pi/X}^{+\pi/X} S(k)\,\exp(\mathrm{i}\,k\,rX)\,\mathrm{d}k\,, \end{aligned}$$

$$S(k) = \frac{1}{X}\sum_{m=-\infty}^{+\infty} W(k + m\,2\pi/X). \quad (10.161)$$

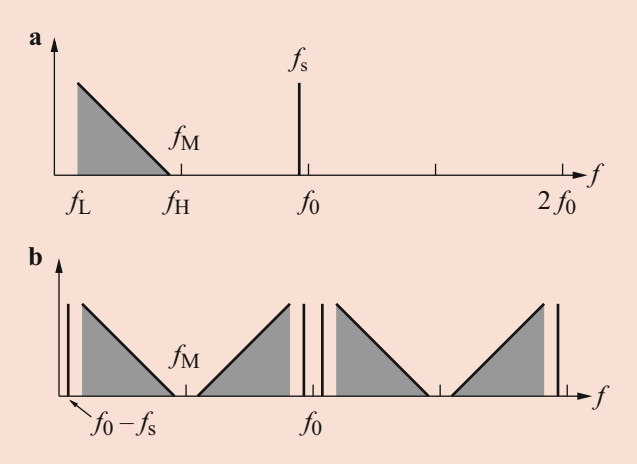

Fig. 10.38 Example of aliasing. The gray area in (**a**) is the spectrum of the input signal, ranging from f_L to f_H; the line at f_s in (**a**) is a spurious signal. The sampling duplicates the input signal producing the signal shown in (**b**), where the line at $f_0 - f_s$ is one of the duplicates of the spurious signal of (**a**): this duplicate cannot be eliminated by filtering because it belongs to the $[0, f_M]$ band

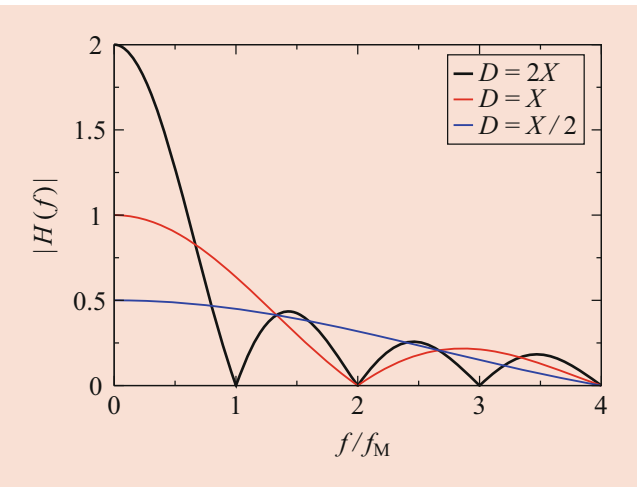

Fig. 10.39 Modulus of H drawn as a function of f/f_M, using different ratios D/X in (10.162)

In conclusion, the spectrum S of the output signal is still periodic with frequency $f_0 = 1/X$, and, therefore, aliasing may occur. Another issue is that the portion of spectrum located around harmonic $mf_0 = 2\,mf_M$ is multiplied by the transfer function

$$H = \frac{D}{X}\,\frac{\sin(\pi\,Df)}{\pi\,Df} = \frac{D}{X}\,\sin\left(\frac{\pi}{2}\,\frac{D}{X}\,\frac{f}{f_M}\right) \Big/ \left(\frac{\pi}{2}\,\frac{D}{X}\,\frac{f}{f_M}\right), \tag{10.162}$$

with $2\,m - 1 \le f/f_M \le 2\,m + 1$. The modulus of (10.162) is drawn in Fig. 10.39 for different ratios D/X. Given that the minimum of X (whence the resolution) is prescribed by the technological process, one must select the D/X ratio in such a way as to obtain the best tradeoff between elimination of aliasing and degradation of contrast; in fact, increasing D/X attenuates the frequencies larger than f_M but, at the same time, eliminates the upper part of the signal spectrum, and vice versa. Considering, for instance, the Nyquist limit $f = f_M$, one finds that the transfer function reduces to $2/\pi = 64\%$ for $D = X$, while it reduces to $\sqrt{2}/\pi = 45\%$ for $D = X/2$ and to zero for $D = 2X$ (the odd-looking condition $D > X$ occurs, for instance, in a frame-transfer device working in the interlaced format). In some applications like commercial television, some loss of contrast is preferable because aliasing produces disturbing effects on the image (*moiré fringes*); in other applications, where the operator is trained to analyze the contents of an image when disturbances are present, it is preferable to accept the presence of moiré fringes to keep that maximum amount of information.

With reference to the pattern noise, it is important to cite [29], which provides a clear description of the characterization methods for noise sources in CCD or CMOS cameras. The paper analyzes the issue from both viewpoints of theory and experiment; Figs. 10.3 and 10.8 of it show measures of nonlinearities and, respectively, compare a number of contributions to noise in CCDs.

10.12.2 Miscellany

The next paragraphs briefly address some other issues related to architecture and performances of CTDs. The interested reader may refer to the original papers. The architecture of the input circuit of a CCD depends on the application. For imaging applications (considering a case in which the CCD is not the sensor itself), the input device consists of a photocapacitor with a semi-transparent gate (typically made of heavily doped polycrystalline silicon). At the end of the integration period, a suitable clock operation transfers the charge packet into the CCD. When the input signal is of the electric type, the input circuit is made of an n^+-p junction and of a pair of electrodes. Different schemes may be adopted to operate the input circuit [30].

The purpose of the output circuit is revealing the charge packet; possible architectures are based on the floating gate, whose functioning is described in Sect. 10.10.4, or, alternatively, on an MOS transistor kept in the *off* condition. This architecture is termed *floating diffusion* because the junction of the MOS transistor nearest to the CCD is floating [31].

Dynamics and Linearity

In a CCD, dynamics is essentially dictated by the maximum signal-to-noise ratio. The analysis of noise is carried out in detail in [32–35]. As for the signal amplitude, the latter is given by the amount of charge within each potential-energy well; for given values of V_H and V_L, the ratio between the

maximum charge of the packet in a SCCD and in a BCCD is $r = 1 + (d/t_{ox})\,(\varepsilon_{ox}/\varepsilon_{sc})$, with t_{ox} the oxide thickness, d the epitaxial-layer thickness, and ε_{ox} and ε_{sc} the permittivities of the oxide and semiconductor, respectively. From the viewpoint of signal amplitude, SCCDs are preferable.

Linearity of CCDs depends on the performance of the input and output circuits. In optical applications, linearity is rather good, typically of the order of 0.3%, and is limited by the nonlinearity of the depletion-region capacitance present in the circuits. When, instead, the charge is injected electrically, linearity is more strongly affected by the architecture of the input circuit; optimal values of second-harmonic attenuation that have been achieved are in the $40 \div 45$ dB range [36]. An analysis of linearity in CIDs is given in [37], where the model and a number of experimental results on these devices are provided; both the destructive and non-destructive reading schemes are considered.

Blooming

All image sensors exhibit, to some degree, the *blooming* effect, which consists in an apparent increase in size of an object whose luminous intensity saturates the device. In CCD sensors, the phenomenon is due to the excessive charge generation occurring in some of the potential-energy wells: the excess charge diffuses laterally into the neighboring wells and produces the apparent enlargement of the object. In a two-dimensional sensor, charges diffuse preferably into the wells belonging to the same channel; thus, a highly illuminated spot produces a bright stripe in the output image. An effective method for eliminating blooming consists in absorbing the excess charges by interspersing conductive areas among the channels; in some implementations, the voltage of the conductive areas is externally controlled.

In CID sensors, the effect of lateral diffusion of the charge is relatively unimportant, because the excess charges are drained by the *p-n* junction formed by the epitaxial layer and the substrate; however, another type of blooming exists in CIDs, which produces stripes similar to those of CCDs. The phenomenon occurs when reading, e.g., a column where a saturated element is present: when another element of the same column is read, the charge of the saturated element transfers into the other gate of the same CID cell, and the excess part of it is injected into the substrate; the effects of the excess charges add up in the output circuit and produce a bright stripe in the column being read. The blooming effect in CIDs is fully eliminated by the non-destructive reading using a floating gate (Sect. 10.10.4).

Spectral Responsivity, Sensitivity, and Recent Developments

The spectral response of an image sensor is the ratio between the number of charges collected at the output circuit per unit time and the optical power density impinging on the sensor at a given frequency. This quantity depends on the optical properties of the semiconductor; in silicon, using back illumination and anti-reflecting coatings, a spectral response near the theoretical limit has been reached in the visible and near-infrared ranges [38]. When front illumination is used, the spectral response is negatively influenced by reflection at the surface and absorption by the polysilicon electrodes. To limit these drawbacks, thin electrodes and anti-reflecting coatings are used; yet, a fraction of the radiation is absorbed by polysilicon at small wavelengths (blue range). Also, multiple reflections at the Si-SiO_2 interfaces produce interferences, this introducing a non-negligible dependence of the spectral response on the layer's thickness.

A new family of back-illuminated CCD, with a very low dopant concentration to achieve depletion regions in the range $[200, 300]\,\mu$m, is presented in [39]. The devices have been used within the Supernova Cosmology Project. Among the reported modeling aspects are the theory of the absorption coefficient for energies below 2.5 eV, accounting for the effect of phonons, and a section devoted to the analysis of spatial resolution. Among the experimental issues are the quantum-efficiency measurements and the pictures of the Dumbbell Nebula, taken with the new type of CCD and compared with those taken with commercial CCDs. An ample description of the state of the art of CCD and CMOS sensors is given in [40]; details are given about the scaling trend of the CCD technology and the improvement in sensitivity; the evolution of the fabrication processes is also analyzed.

An application of CCDs as registers, to the purpose of analyzing the noise associated with the injection of extremely small charge packets, is presented in [41], where the interesting possibility of X-ray detection using CCDs is described. The transfer inefficiency ε of a novel implementation of CCDs is the focus of [42] (transfer inefficiency is defined in Sect. 10.10.2), where a model for ε is discussed and a comparison of the latter with a set of measurements is given; the relative importance of the fringing field and of charge trapping is discussed for both SCCDs and BCCDs. Schemes for response-time optimization in CCD imagers are addressed in [43]. Architectures of imagers combining photodiodes as active area and CCDs as transfer registers have shown able to strongly improve resolution; an example of a 35 mm chip with a 4.5 μm photodiode and a maximum operation speed of 60 MHz is given in [44]. To date, the most recent contribution to the subject is [45].

10.13 Appendix

This appendix illustrates a number of important aspects that were not accommodated in the main part of chapter lest their presence interrupted the fluidness of the presentation.

10.13.1 The Poisson Equation in the MOSFET Channel

To tackle the Poisson equation in non-equilibrium, it is convenient to use the quasi-Fermi potentials φ_n and φ_p, whose normalized form is $u_n = q\,\varphi_n/(k_B\,T)$ and $u_p = q\,\varphi_p/(k_B\,T)$; the carrier concentrations read $n = n_i\,\exp(u - u_n)$ and $p = n_i\,\exp(u_p - u)$, respectively. In equilibrium, $u_n, u_p \to u_F$, with u_F the normalized Fermi potential; one defines

$$\chi_n = u_n - u_F\,, \qquad \chi_p = u_p - u_F\,, \tag{10.163}$$

so that

$$n = n_{p0}\,\exp(u - \chi_n)\,, \qquad p = p_{p0}\,\exp(\chi_p - u)\,, \tag{10.164}$$

with $\chi_n, \chi_p \to 0$ in equilibrium. In non-equilibrium, at any position y in the channel, it is $\lim_{x\to\infty} \chi_n, \chi_p = 0$ as observed in Sect. 10.7, whence $\varphi_n, \varphi_p \to \varphi_F$ when x increases. Considering an n-channel MOSFET (Sect. 10.7), the charge density in the semiconductor reads $\rho = q\,[p_{p0}\,\exp(\chi_p - u) - n_{p0}\,\exp(u - \chi_n) - N_A]$, with $\lim_{x\to\infty} \rho(x, y) = 0$. Using the limiting values of χ_n and χ_p and the boundary conditions on u (shown below) yields $N_A = p_{p0} - n_{p0}$; it follows

$$\rho = -q\,p_{p0}\,A(u, \chi_n, \chi_p)\,, \quad A = \frac{n_i^2}{N_A^2}\,[\exp(u - \chi_n) - 1] + 1 - \exp(\chi_p - u) \tag{10.165}$$

with $n_i^2/N_A^2 = \exp(-2\,u_F) \ll 1$ (compare with (10.3)), and the Poisson equation reads

$$\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} = \frac{1}{L_A^2}\,A\,, \tag{10.166}$$

with $L_A^2 = \varepsilon_{sc}\,k_B\,T/(q^2\,p_{p0})$. Also, it is $u = u(x, y)$, $\chi_n = \chi_n(y)$, and $\chi_p = \chi_p(y)$ (the latter two relations hold because the x-component of the current density is zero). The boundary conditions for u with respect to x are $u(\infty, y) = 0$, $u'(\infty, y) = 0$ due to the charge neutrality of the bulk region; in practice, u and u' vanish at the end $x_d(y)$ of the depletion width.

If the channel is well formed, one simplifies (10.166) by noting that the modulus of $\partial E_x/\partial x = -\partial^2 u/\partial x^2$ is large, because E_x changes from E_{sx} (which is also large because it forces the strong-inversion condition at the surface) to zero in the short distance $x_d(y)$. In contrast, for relatively low values of V_{DS} and in long-channel MOSFETs, the y-dependence of E_{sy} (and also of E_{sx}) on y is weak, whence $\partial E_y/\partial y = -\partial^2 u/\partial y^2$ is small at the semiconductor-insulator interface. In conclusion, (10.166) is approximated as

$$\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} \simeq \frac{\mathrm{d}^2 u}{\mathrm{d}x^2} = \frac{1}{L_A^2}\,A. \tag{10.167}$$

where the dependence of A on y is of the parametric type. From this point on, the solution procedure becomes the same as in equilibrium (Sect. 10.1.1) and provides $[q\,E_{sx}/(k_B\,T)]^2 = (2/L_A^2)\,F^2$, with

$$F^2 = \{\exp(-\chi_n - 2\,u_F)\,[\exp(u_s) - 1]\} - \{\exp(\chi_p)\,[1 - \exp(-u_s)]\} + \{[1 - \exp(-2\,u_F)]\,u_s\}\,. \tag{10.168}$$

The first, second, and third terms in braces of (10.168) derive from the concentration of electrons, holes, and dopants, respectively; like in the equilibrium case, the flat-band condition $u_s = 0$ corresponds to $F = 0$ (note that the derivation of (10.168) entails a multiplication by $\mathrm{d}u/\mathrm{d}x$ of both sides of $\mathrm{d}^2u/\mathrm{d}x^2 = A/L_A^2$, which is acceptable if χ_n and χ_p are such that $\mathrm{d}u/\mathrm{d}x$ never vanishes). When the accumulation regime is excluded, the contribution of the holes is negligible, and, using also $\exp(-2\,u_F) \ll 1$, a simpler form of (10.168) is found, applicable in the depletion, weak-inversion, and strong-inversion regimes:

$$F^2 = \exp(-\chi_n - 2\,u_F)\,[\exp(u_s) - 1] + u_s\,, \qquad u_s(y) \geq 0. \tag{10.169}$$

In this case, it is $F^2 \geq 0$ for any χ_n, still with $F = 0$ when $u_s = 0$. In strong inversion, the electron charge (proportional to $\exp(u_s) - 1$ in (10.169)) dominates, corresponding to positive values of $u_s - \chi_n - 2\,u_F$; thus, the onset of the strong-inversion condition is identified by $u_s = \chi_n + 2\,u_F$ or, using the definition (10.163) of χ_n,

$$u_s = u_n + u_F\,, \qquad 0 \leq y \leq L. \tag{10.170}$$

Relation $u_s = \chi_n + 2\,u_F$ is coherent with the definition of threshold of the MOS capacitor (Table 10.1), corresponding here to $\chi_n = 0$. Also, as shown in [1, Sect. 10-2] and in Sect. 10.7.3, specifying $u_s = \chi_n + 2\,u_F$ at the source and drain ends of the channel provides the integration limits (10.74).

10.13.2 Inversion-Layer Charge and Mobility Degradation

In the simplified model (10.75) for the drain current worked out in Sect. 10.7.1, when $V_{DS} \to V_{DS}^{sat}$, the inversion-layer charge Q_i vanishes at the drain end of the channel. Considering that the MOSFET current is carried by the inversion-layer charge, the vanishing of the latter occurring at the drain end of the channel when $V_{DS} \to V_{DS}^{sat}$ may seem an oddity. However, it is important to remember that a number of approximations are necessary to reach the result expressed by (10.83) and

(10.84); such approximations make the theory applicable only in the linear region and in the condition of a well-formed channel.

When $V_{DS} \to V_{DS}^{sat}$, the vertical component of the electric field at the interface, E_{sx}, is made weaker by the interplay between the voltages applied to the gate electrode and to the nearby drain electrode; for this reason, at the drain end of the channel, the flow lines of $\mathbf{J}_n$ do not keep close to the interface any longer, but spread into the substrate, this decreasing the carrier density. The phenomenon is better understood with the aid of Fig. 10.40, where the linear-parabolic model is used with, e.g., $V_T = 0.5$, $V_S = 0$, $V_{GS} = 1.5$, and $V_{DS} = 2$ V. As $V_{DS}^{sat} = 1$ V, the saturation condition $V_{DS} > V_{DS}^{sat} = 1$ holds. Along the dash-dotted line enclosed in the right oval, the direction of the electric field is that shown in the vector diagram in the upper-right part of the figure; in particular, the vertical component of the field at the position marked by the vertical dashed line points upward. As a consequence, the channel electrons are repelled downward, and the flow lines of the current density detach from the interface. On the source end of the channel, instead, the vertical component of the field points downward. By continuity, a position within the channel exists where, in saturation, the vertical component of the field vanishes; such a position (not shown in the figure) is called *inversion point*. Also, the large component of the electric field along the y direction, which exists within the space-charge region of the reverse-biased drain junction, makes the average velocity of the carriers to increase at the drain end of the channel; as the total current is constant, a further decrease in the carrier concentration occurs. The two effects briefly illustrated above are not accounted for by the simplified model and require a more elaborate approach in which the two-dimensional structure of the electric field is accounted for.

Another comment is useful, this time related to the *off* condition. When $V_{GS} \to V_T$, the current of a real device does not actually vanish; in fact, a current (called *subthreshold current*), due to the carriers present in the channel in the weak-inversion condition, flows for $V_{GS} < V_T$. Also in this case, a more elaborate theory is necessary, showing that the subthreshold current vanishes exponentially as V_{GS} decreases (Sect. 10.7.3).

It is worth concluding this appendix by commenting the simplification used in (10.67), where the effective electron mobility μ_e is assumed to be independent of the position y along the channel. The factors that affect mobility in a MOSFET are collisions with phonons, ionized impurities, and semiconductor-oxide interface; in macroscopic models, the electron mobility $\mu_n(x, y)$ is made to depend on the lattice temperature T, concentration of ionized impurities N_A, and x-component of the electric field $E_x(x, y)$. The first two parameters, T and N_A, do not introduce a dependence on position because they are themselves constant. The x-dependence

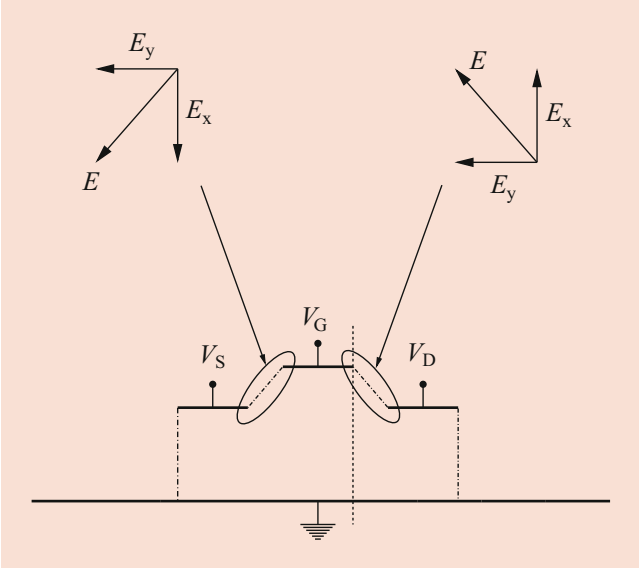

Fig. 10.40 Illustration of the electric-field components at the channel ends in the saturation condition (after [2])

of E_x is absorbed by the integral (10.64) that defines μ_e; it follows that the average mobility depends on y because E_x does. Such a dependence, in turn, is relatively weak in the strong-inversion condition as remarked in Sect. 10.13.1. Therefore, the dependence of μ_e on position is considered negligible.

10.13.3 Exact Charge Partitioning in the MOS Capacitor

In treating the MOS capacitor, the charge distribution has been so far approximated with (10.29), which is applicable whenever accumulation is excluded (Sect. 10.3, with reference to the p-type substrate). The same approximation has then been used for treating the MOSFET. A more precise analysis is possible, which avoids partitioning the semiconductor volume into regions; it is based on the integral expression (10.12) of the semiconductor charge per unit area, in which the individual charge contributions are considered. In the analysis, care must be taken to avoid possible divergences due to the artifact of an infinite extent of the integration domain. In fact, the integral as a whole,

$$Q_{sc} = \int_0^\infty q\,(p - n - N_A)\;\mathrm{d}x = \int_0^\infty q\,[(p - p_{p0}) - (n - n_{p0})]\;\mathrm{d}x\,, \tag{10.171}$$

converges (see below), while the integral of N_A alone obviously diverges. In a p-type substrate, (10.5) holds, with the negative sign because accumulation is excluded; in turn, the charge density reads $\rho = -q\,p_{p0}\,A(u)$, with A given by (10.3); changing the integration variable in (10.171) by let-

ting $\mathrm{d}x = \mathrm{d}u/u' = -L_\mathrm{A}\,\mathrm{d}u/(\sqrt{2}\,F)$, and using the integration limits $u(0) = u_\mathrm{s}$ and $u(\infty) = 0$, yields

$$Q_\mathrm{sc} = -Q_\mathrm{sc}^{(1)} \int_0^{u_\mathrm{s}} \frac{A(u)}{2\,F(u)}\,\mathrm{d}u\,, \tag{10.172}$$

with $Q_\mathrm{sc}^{(1)}$ given by (10.25). The asymptotic condition in the x coordinate corresponds to $u \to 0$; it is easily found that the $u \to 0$ limit of A/F is finite, whence the integral converges. Similarly, if one replaces A with $(n_\mathrm{i}^2/N_\mathrm{A}^2)\,[\exp(u) - 1]$ or, separately, with $1 - \exp(-u)$, the corresponding integrals converge; when the normalization is eliminated, these terms (whose sum is A) correspond to $n - n_\mathrm{p0}$ and $N_\mathrm{A} - p$, respectively. Considering that in the depletion, weak-inversion, and strong-inversion regimes it is $n \gg n_\mathrm{p0}$ and $N_\mathrm{A} \gg p$ in the channel region, one lets

$$Q_\mathrm{i} = -Q_\mathrm{sc}^{(1)}\,\exp(-2\,u_\mathrm{F}) \int_0^{u_\mathrm{s}} \frac{\exp(u) - 1}{2\,F(u)}\,\mathrm{d}u\,,$$

$$\exp(-2\,u_\mathrm{F}) = \frac{n_\mathrm{i}^2}{N_\mathrm{A}^2}\,, \tag{10.173}$$

$$Q_\mathrm{b} = -Q_\mathrm{sc}^{(1)} \int_0^{u_\mathrm{s}} \frac{1 - \exp(-u)}{2\,F(u)}\,\mathrm{d}u. \tag{10.174}$$

These definitions fulfill $Q_\mathrm{sc} = Q_\mathrm{i} + Q_\mathrm{b}$ and yield a more precise charge partitioning in the MOS capacitor, avoiding at the same time the complicacy of placing the neutrality condition at a finite distance. The same analysis applies to the n-type substrate. Although relations (10.173) and (10.174) cannot be integrated analytically, their sum (10.172) is integrable: combining (10.25) with (10.172) yields in fact

$$F(u_\mathrm{s}) = \int_0^{u_\mathrm{s}} \frac{A(u)}{2\,F(u)}\,\mathrm{d}u\,, \tag{10.175}$$

which can also be found through a direct calculation. Using (10.173) and (10.174), it is possible to check the accuracy of the approximations of Sect. 10.3; as shown in [46], when accumulation is excluded, the approximations are sufficiently accurate and can also be extended to the non-equilibrium case (Sect. 10.7.3).

10.13.4 Scaling Rules for MOSFETs

The integrated circuits (ICs) have been introduced in the 1960s; since then, their storage capacity, computing power, and speed have increased exponentially. It has been observed that the number of transistors in an integrated circuit approximately doubles every 2 years (*Moore law*); it is therefore possible to identify "generations" of the IC technology, also referred to as *nodes*: each node is defined by the value of a characteristic length (typically the *half-pitch*, i.e., half the distance between contacts in a DRAM array). The exponential growth in the number of elementary devices in the chip, and, consequently, its augmented performance, derives from the continuous decrease, from one generation to the next, in the radius of the elementary devices and from the parallel increase in the radius of the chip; such improvements, in turn, are due to the steady refinement in the resolution and quality of the fabrication processes. Also, smaller devices absorb less power; in parallel, the clever circuit design made possible by complexity helps in keeping the consumption of the whole chip low. Another advantage is that, when the size of a transistor decreases, its switching time decreases as well.

If the applied voltages are left unchanged from one generation to the next, the decrease in size of a device makes the electric field in its interior to increase; this may eventually give rise to, e.g., junction breakdown due to avalanche or gate-oxide breakdown; to prevent these phenomena, it is then necessary to modify the applied voltages: the schemes by which this goal is obtained are known as *scaling rules*. Different classes of scaling rules exist, and, among them, those in which the electric field in the new-generation device is kept equal to that of the old-generation one are called *constant-field scaling rules*. No matter what class is adopted, for implementing a scaling rule, it is necessary to investigate the behavior of the Poisson equation $-\varepsilon\,\nabla^2\varphi = \rho$ under scaling; the equation, in fact, describes the spatial dependence of the electric field (it is assumed that new-generation devices are made of the same material as the old ones, so permittivity does not change). The device shrinking is described as a variable transformation, from the old-generation to the new-generation set, involving spatial coordinates and electric potential; namely, $x_i^\mathrm{old} \leftarrow x_i^\mathrm{new} = x_i^\mathrm{old}/\lambda$, with $\lambda > 1$ the coordinate scaling factor, and $\varphi^\mathrm{old} \leftarrow \varphi^\mathrm{new} = \varphi^\mathrm{old}/\kappa$, with $\kappa > 1$ the scaling factor of the potential. For the moment, one assumes that λ and κ are independent from each other; this scheme is the most general one and is known as *generalized scaling theory* [47]. The electric-potential transformation does not involve the interfaces between different materials (e.g., contact-semiconductor interfaces); the work-function differences, in fact, do not scale and are dealt with separately. Transforming the Poisson equation yields

$$-\varepsilon \sum_{i=1}^{3} \frac{\mathrm{d}^2(\varphi^\mathrm{old}/\kappa)}{\mathrm{d}(x_i^\mathrm{old}/\lambda)^2} = \rho^\mathrm{new}. \tag{10.176}$$

In order to map the electric potential of the new-generation device over that of the old-generation one (assuming that the boundary conditions are scaled correctly), one must take $\rho^\mathrm{new} = \rho^\mathrm{old}\,\lambda^2/\kappa$. In turn, the electric-field components transform as

$$E_i^{\text{new}} = -\frac{\partial(\varphi^{\text{old}}/\kappa)}{\partial(x_i^{\text{old}}/\lambda)} = \frac{\lambda}{\kappa} E_i^{\text{old}}. \tag{10.177}$$

From (10.177), one finds that the generalized theory yields the constant-field scaling rules when $\kappa = \lambda = x_i^{\text{old}}/x_i^{\text{new}}$; as a consequence, the charge density scales as $\rho^{\text{new}} = \lambda\,\rho^{\text{old}}$. The above relation is obviously fulfilled in insulators ($\rho_{\text{ox}} \simeq 0$) while, in principle, is not fulfilled in a semiconductor, where $\rho = q\,(p - n + N)$, because p and n do not scale. On the other hand, in the standard operating conditions of a device, the semiconductor can be parted (Sect. 10.1.2) into neutral regions, where $\rho \simeq 0$, and space-charge regions, where $\rho = q\,(p - n + N) \simeq q\,N$; therefore, the scaling rule is fulfilled if

$$N^{\text{new}} = \lambda\,N^{\text{old}}\,. \tag{10.178}$$

A very successful application of the scaling rules pertains to the MOS technology; their application to the case of an n-channel transistor is shown in the following. The linear-parabolic model (Sect. 10.7.2) yields for the drain current

$$I_{\text{D}} = \beta\,[(V_{\text{GS}} - V_{\text{T}})\,V_{\text{DS}} - V_{\text{DS}}^2/2]\,, \qquad \beta = \frac{W}{L}\,\mu_{\text{e}}\,\frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}}\,; \tag{10.179}$$

one may argue that (10.179), where the contact voltages appear, involves interfaces between the semiconductor and other materials; however, if one assumes that the contacts are made of the same material, it is found that the non-scalable constants are eliminated because V_{GS} and V_{DS} are in fact voltage differences. The only exception is V_{T}, which is non-scalable; its effect is made less important by taking $V_{\text{GS}} \gg |V_{\text{T}}|$. To summarize, the term in brackets of (10.179) is the square of a scalable voltage. As for the scaling of β, permittivity does not change, while the geometrical factor scales like $W^{\text{new}}/(L^{\text{new}}\,t_{\text{ox}}^{\text{new}}) = \lambda\,W^{\text{old}}/(L^{\text{old}}\,t_{\text{ox}}^{\text{old}})$. Finally, mobility may suffer some degradation due to the increase in the doping concentration dictated by (10.178) (some indications about mobility modeling are in Sect. 10.9.1); neglecting for the moment this phenomenon, and using symbol V_X to collectively indicate the voltages in (10.179), yields

$$I_{\text{D}}^{\text{new}} = \text{const} \times \frac{\left(V_X^{\text{new}}\right)^2}{t_{\text{ox}}^{\text{new}}} = \text{const} \times \frac{\left(V_X^{\text{old}}/\lambda\right)^2}{t_{\text{ox}}^{\text{old}}/\lambda} = \frac{I_{\text{D}}^{\text{old}}}{\lambda}\,. \tag{10.180}$$

The power dissipation in an MOS transistor occurs at the source-drain port (Sect. 10.7); the scaling behavior of the power P dissipated by a single transistor is

$$P^{\text{new}} = V_{\text{DS}}^{\text{new}}\,I_{\text{D}}^{\text{new}} = \frac{V_{\text{DS}}^{\text{old}}}{\lambda}\,\frac{I_{\text{D}}^{\text{old}}}{\lambda} = \frac{P^{\text{old}}}{\lambda^2}\,. \tag{10.181}$$

From the viewpoint of circuit design, it is important to determine the power $\tilde{P}$ dissipated per unit area of the chip; if the number of transistors per unit area is ζ, then in a planar technology, it is $\zeta^{\text{new}} = \lambda^2\,\zeta^{\text{old}}$; the latter expression, combined with (10.181), yields

$$\tilde{P}^{\text{new}} = \zeta^{\text{new}}\,P^{\text{new}} = \lambda^2\,\zeta^{\text{old}}\,\frac{P^{\text{old}}}{\lambda^2} = \zeta^{\text{old}}\,P^{\text{old}} = \tilde{P}^{\text{old}}\,, \tag{10.182}$$

that is, $\tilde{P}$ is invariant under the constant-field scaling. This is a fundamental result, because it shows that a suitable choice of the scaling rules allows the designer to concentrate a larger number of devices in the same area without producing an excessive heat. Another advantage of smaller transistors is that their switching time is shorter. Using the CMOS architecture by way of example, consider the charging or discharging process of the capacitive load that represents the fan-out. Letting A be the capacitor area, and considering a linear capacitor for simplicity, one finds $C^{\text{new}} = \varepsilon_{\text{ox}}\,A^{\text{new}}/t_{\text{ox}}^{\text{new}} = \varepsilon_{\text{ox}}\,(A^{\text{old}}/\lambda^2)/(t_{\text{ox}}^{\text{old}}/\lambda) = C^{\text{old}}/\lambda$. In both charging and discharging processes, current I is the drain (source) current of an MOS transistor, whose scaling rule is (10.180); the circuit equation is $I = C\,\mathrm{d}V/\mathrm{d}t$, in which the scaling factors of V and I cancel each other. With these premises, one finds

$$\mathrm{d}t^{\text{new}} = C^{\text{new}}\,\frac{\mathrm{d}V^{\text{new}}}{I^{\text{new}}} = \frac{C^{\text{old}}}{\lambda}\,\frac{\mathrm{d}V^{\text{old}}}{I^{\text{old}}} = \frac{\mathrm{d}t^{\text{old}}}{\lambda}\,, \tag{10.183}$$

namely, within the constant-field scaling rules, the scaling factor of time is the same as that of lengths.

As mentioned before, the current-voltage characteristics of the devices embed non-scalable quantities, typically due to the presence of interfaces; the problem is not restricted to the device boundaries: for instance, the electric field in a reverse-biased, abrupt p-n junction reads

$$E_0 = -\sqrt{\frac{2\,q}{\varepsilon_{\text{sc}}}\,\frac{\psi_0 - V}{1/N_{\text{D}} + 1/N_{\text{A}}}}\,, \qquad \psi_0 = \frac{k_{\text{B}}\,T}{q}\,\log\left(\frac{N_{\text{D}}\,N_{\text{A}}}{n_{\text{i}}^2}\right), \tag{10.184}$$

where ψ_0 increases under scaling by the additive term $(2\,k_{\text{B}}\,T/q)\,\log\lambda$; only when $|V| \gg \psi_0$, the scaling factors of V and $1/N_{\text{D}} + 1/N_{\text{A}}$ compensate each other and make E_0 invariant under scaling. Another example is the threshold voltage given, e.g., in an n-channel transistor by (10.82); it embeds the Fermi potential $\varphi_{\text{F}} = (k_{\text{B}}\,T/q)\,\log(N_{\text{D}}/n_{\text{i}})$, the work-function difference at the interface between bulk contact and semiconductor (through the flat-band voltage, Sect. 10.3.1), and, possibly, the fixed oxide charge and the surface-state charge.

It is expected that the miniaturization of the present device architecture will attain the end, brought about by fundamental physical limits; for instance, when the insulator becomes too thin, dielectric breakdown or leakage due to tunneling becomes inevitable: for these reasons, in advanced devices, silicon dioxide is being replaced with high-k dielectrics. Another limit made worse by miniaturization is

statistical variability; for instance, implanting a dopant with a 6×10^{18} cm^{-3} concentration into a channel whose size is $40 \times 20 \times 20$ nm^3 yields about 100 implanted atoms, so that treating the dopant profile as a continuous function becomes unrealistic. In turn, practical problems are related to the (exponentially increasing) cost of investments necessary to pass from one generation to the next and from the increasing complexity of the circuit design: the latter issue is in fact tackled by means of advanced techniques for automatic design and of sophisticated models describing each phase of the design (detailed information about device modeling is found in Part IV of this Handbook).

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Electrostatic Doping and Devices

11

Raymond J. E. Hueting and Gaurav Gupta

Contents

11.1 Introduction 372

11.2 The Concept of Electrostatic Doping 372
11.2.1 Schottky Barrier-Based Devices 373
11.2.2 Workfunction-Induced Doping 375
11.2.3 Bias-Induced Doping 380

11.3 Electrostatic Doping Approaches: Discussion 383
11.3.1 Potential ED Devices for Future CMOS 384
11.3.2 ED: Limitations and Drawbacks 385

11.4 Conclusion 386

References 386

Abstract

Electrostatic doping is widely emerging as an alternative approach to overcome the limitations of traditional chemical doping to provide high charge carrier densities in nanometer-scale semiconductor devices. In this chapter (this work is partly based on Gupta et al. (IEEE Trans Electron Devices 64(8):3044–3055, 2017) and has been expanded with latest insights and developments), various reported approaches on electrostatic doping and related device architectures in different material systems are discussed. It is shown that for the induced electrostatic doping, the role of the metal workfunction, specific semiconductor properties (i.e., electron affinity and energy bandgap), the applied electric field, and the interplay between them are important. The effect of interface traps on the induced charge is also highlighted. In addition, both the performance benefits and major bottlenecks of electrostatic doping for potential future CMOS technology are discussed.

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11.1 Introduction

For device dimensions of only several nanometers, conventional chemical (or impurity) doping [1] faces several challenges. In practice it is difficult to form junctions with extremely high doping gradients (e.g., a few nm/decade) [2, 3], especially important for tunnel field-effect transistors (TFETs) realized in ultrathin semiconductor bodies (UTBs) [4, 5]. Moreover, in case of nanometer-scale semiconductor bodies, such as nanowires, doping levels above their solid solubility limit would be required for obtaining sufficiently low body and contact resistances, while accurate control of the doping type, level, and spatial distribution in such nanostructures is also challenging because of their complex growth dynamics and geometrical constraints [6, 7]. In addition, variability induced by random (chemical) doping fluctuation has been the major concern for manufacturing high yield nanometer-scale devices and circuits [8–10].

It appears that for any nanometer-scaled device, the requirement of having a high carrier density along with unintentional, and possibly undesired, ionized dopants in its active semiconductor body points toward impurity-free doping solutions, such as electrostatic doping.

Other than geometrical aspects, electrostatic doping has a strong potential for various alternative emerging material systems as well.

For example, in wide bandgap semiconductors, such as gallium-nitride (GaN), silicon-carbide (SiC), and zinc-oxide (ZnO), chemical doping employed for specific p-type (GaN, SiC) or n-type (ZnO) regions remains difficult. This can be attributed to the deep donor or acceptor levels or dopant passivation via complex formation [11–14].

It is also not straightforward to adopt chemical doping for realizing electronic switches in other types of semiconductor

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materials, such as carbon nanotubes (CNTs) and emerging two-dimensional (2-D) materials (graphene, phosphorene, silicene, and transition metal dichalcogenides (TMDs) [15, 16]. For example, tunnel field-effect transistors (TFETs) and 2-D materials (or a combination of those) are potentially attractive for beyond-CMOS (complementary metal oxide semiconductor) devices for their sub-thermal subthreshold slope [17]. However, there are still several technological hurdles left to reach their full potential since realizing highly doped junctions with a steep profile combined with a low defect density, essential for an efficient tunneling process [16, 18], is difficult.

Consequently, in recent years various approaches have been proposed to control the charge carrier density by other means than chemical doping. In many of these approaches, electrostatic interaction between the semiconductor and a different material at the interface, in most cases a metal or a metallic compound, governs the carrier density. Such approaches are therefore referred to as "electrostatic doping".

Device examples based on these approaches are manifold: Schottky barrier (SB) metal-oxide-semiconductor field-effect transistors (MOSFETs) [19, 20], charge plasma (CP)-based ultra-thin body (UTB) devices [21–24], reconfigurable UTB devices such as silicon (Si) nanowire FETs [25–27] and fully depleted silicon-on-insulator (FD-SOI) devices [28, 29], FETs based on graphene [30–33], CNT [34–36] and 2-D materials [37, 38], and electron-hole bilayer based TFETs [39–41]. Electrostatic doping potentially offers well-controlled, possibly ultra-sharp, carrier density profiles with a reduced defect density and therefore could be an attractive alternative to conventional chemical doping for a broad range of electron devices.

In this chapter an overview of various device concepts based on electrostatic doping (ED) is presented and is organized as follows. First, in Sect. 11.2 several ED approaches are summarized which are subdivided into three categories based on the nature of the underlying electrostatics. Thereafter, various types of electrostatically doped devices are discussed focussing on the electrostatics for different types of metal-semiconductor systems. Further, in Sect. 11.3 the performance of potential electrostatically doped devices for future CMOS technology is discussed, and the major challenges and possible drawbacks of the ED techniques are addressed. Finally, in Sect. 11.4 a summary is given.

11.2 The Concept of Electrostatic Doping

As a replacement for conventional chemical doping, electrostatic doping (ED) can generally be considered as a technique to induce charge carriers (electrons or holes) in a semiconductor material resulting from the band alignment near its interface with another (semi)conducting material. This chapter focusses on metal (or metallic compound)-induced ED; other heterostructure-based doping like polarization doping, e.g., in III-nitrides [42], is beyond the scope of this chapter. However, some alternative approaches are discussed in Sect. 11.3.

The carrier concentration in the close vicinity of a metal-semiconductor (MS) interface is largely controlled by the electrostatic condition at that interface, rather than by the chemical impurities as for the case of conventional chemical doping. This interfacial electrostatic condition, which influences the band alignment, is a strong function of the metal workfunction (ϕ_M), the semiconductor's energy bandgap (E_G), and its electron affinity (χ_S) or alternatively the semiconductor workfunction (ϕ_S). In addition, the applied electric field, if any, also influences the electrostatic properties near the interface.

The ED approaches can be subdivided into three categories: (1) Schottky barrier-based devices, (2) workfunction-induced doping, and (3) bias-induced doping. In the following subsections, these ED approaches, as applied to different devices and material systems, are discussed.

11.2.1 Schottky Barrier-Based Devices

In Schottky barrier (SB)-based devices, the current is limited by one or more Schottky contacts. The physics of a Schottky barrier formed at the MS interface has been thoroughly described in good reference books [1, 43].

An SB with height $q\phi_B$ is obtained when $\phi_M > \phi_S$ for an n-type semiconductor (Fig. 11.1a) and $\phi_M < \phi_S$ for a p-type semiconductor, where q is the elementary charge.

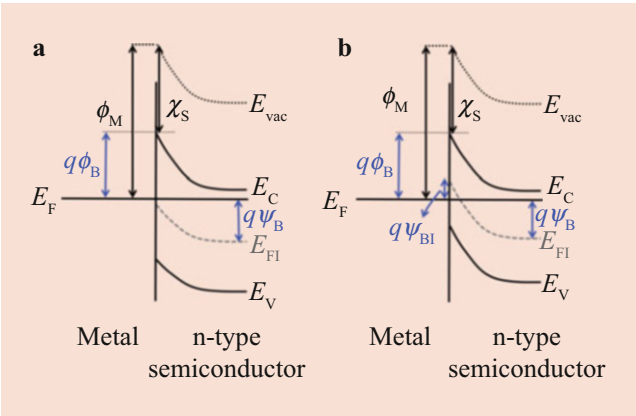

Fig. 11.1 Schematic energy band diagrams for (**a**) a traditional n-type Schottky contact where a depletion layer is formed at the MS interface and (**b**) an n-type Schottky contact with large MS workfunction difference. The excessive band-bending near the interface results in hole inversion in an n-type semiconductor. Consequently, a shallow p-n junction is formed near the MS interface. Similarly, electron inversion could be obtained for Schottky contacts on a p-type semiconductor

The Schottky barrier height (SBH) at the MS interface, $q\phi_B$, equals $(\phi_M - \chi_S)$ for an n-type and $(E_G - \phi_M + \chi_S)$ for a p-type semiconductor. There is a fundamental difference in the operation of SB devices from (chemically doped) p-n junction devices. In case of SB devices, the MS interface, hence ϕ_B, fully controls the majority unipolar current [43]. The electron or hole current flow in SB devices is governed by thermionic emission over the barrier and (thermionic) field emission through the barrier contrary to p-n junction-based devices, where transport mechanisms such as drift-diffusion and band-to-band tunneling (BTBT) will determine the current.

For an ideal unipolar Schottky type operation, the band bending at the MS interface is such that, for example, in an n-type semiconductor, the intrinsic Fermi level E_{Fi} lies below the Fermi level E_F which means that $\phi_B \leq u_T \cdot \ln(N_C/n_i)$. Here N_C represents the conduction band effective density of states, n_i is the intrinsic carrier concentration, and u_T is the thermal voltage ($= kT/q$, where k is the Boltzmann constant and T is the temperature). Excessive band bending at the MS interface on the other hand may result in an electrostatically doped p-n junction type operation as discussed in Sect. 11.2.2.

Therefore, for a unipolar Schottky type operation at the MS interface ($x = 0$) holds that

$$(E_C - E_F)|_{x=0} = q\phi_B \leq kT \cdot \ln\left(\frac{N_C}{n_i}\right) \tag{11.1}$$

for an n-type semiconductor, and

$$(E_F - E_V)|_{x=0} = q\phi_B \leq kT \cdot \ln\left(\frac{N_V}{n_i}\right) \tag{11.2}$$

for a p-type semiconductor. E_C and E_V are the conduction and valence band edges, respectively, and N_V represents the valence band effective density of states. The terms $kT{\cdot}\ln(N_C/n_i)$ and $kT{\cdot}\ln(N_V/n_i)$ are approximately equal to $E_G/2$ for most semiconductor materials.

Next, several examples of SB devices are discussed which could be interesting for future CMOS but also for electro-optical devices.

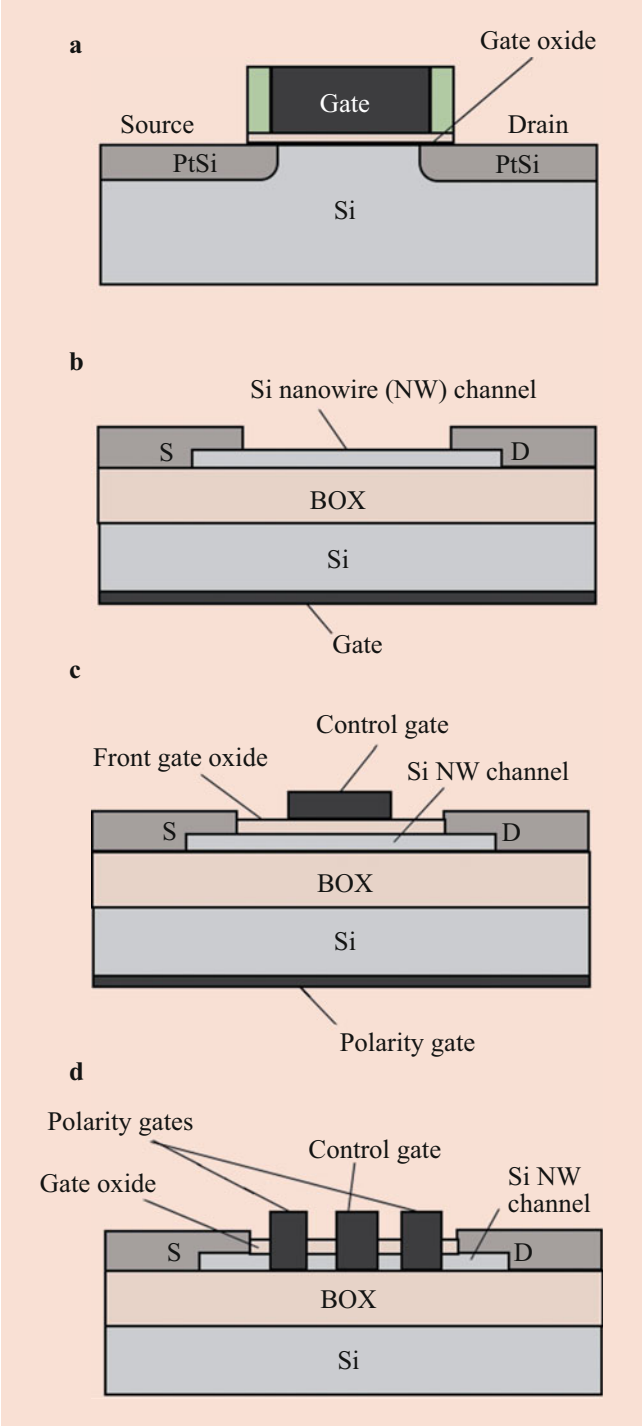

Fig. 11.2 Schematic cross section of (**a**) an Si-based SB-MOSFET [20], (**b**) an Si Nanowire-based SB-MOSFET with a single backgate design [45], an Si Nanowire-based reconfigurable SB-MOSFET, (**c**) with a front and back dual gate design [27] and (**d**) with a dual gate-all-around design [25]

Schottky Barrier (SB) MOSFETs

In 1966 Nishi [44] first proposed to replace chemically doped source/drain regions in conventional MOSFETs with metal. In 1968 Lepselter and Sze [19] reported for the first time the realization of an Si p-type MOSFET (pMOS), in which the source/drain regions were formed by platinum-silicide (PtSi). Thereafter, a series of developments resulted in the metal source/drain region SB-MOSFET technology (Fig. 11.2a) where basically chemically doped source/drain regions in conventional MOSFETs have been replaced with metal, typically silicide.

During the SB-MOSFET operation, charge carriers are injected from the metal into the semiconductor channel through

thermionic(-field) emission as in a Schottky diode. However, in the former, the gate potential can be used to tune the effective barrier height and width further, as illustrated in Fig. 11.3a, b. SB-MOSFET technology potentially offers several benefits for sub-30-nm scaling, such as a low parasitic source/drain resistance, sharp junctions (needed for down-scaling), better control over the off-state leakage current, suppressed parasitic bipolar action, and that along with low thermal budget processing [20]. Further, as required for CMOS technology, SB-PMOS and SB-NMOS devices can be realized by adopting mid-gap silicides. In addition, SB-FINFETs were realized featuring a 6 mV/dec subthreshold swing at room temperature [46]. The SB-MOSFET concept has also been widely adopted in CNTs [35, 36, 47] partly because chemical doping is not straightforward there. For an elaborate review on SB-MOSFET technology, refer to [20].

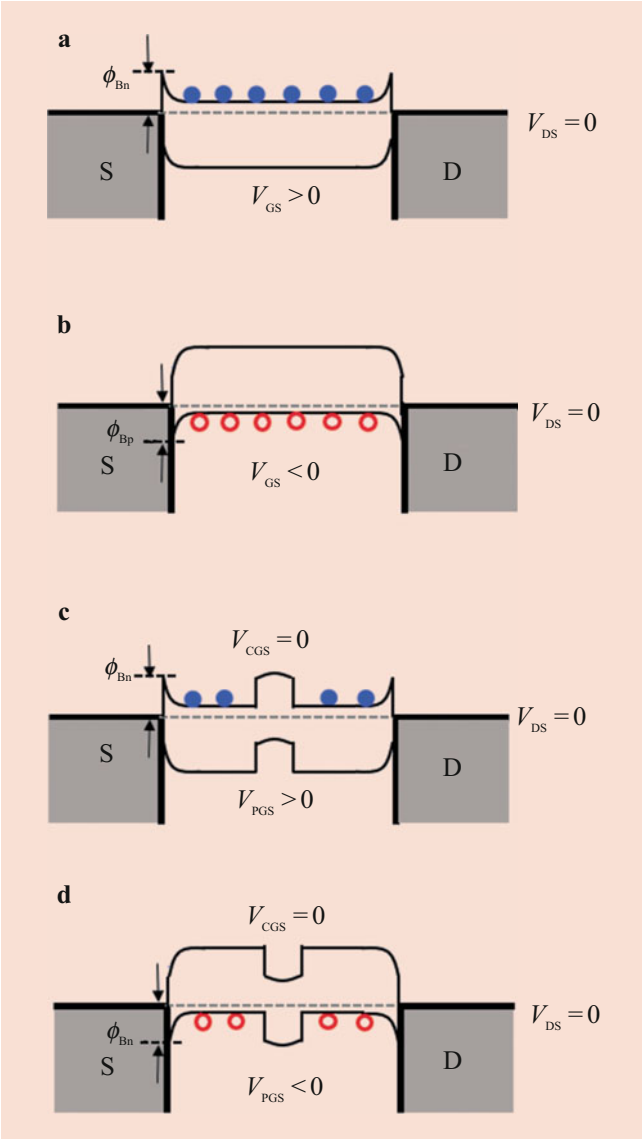

Fig. 11.3 The schematic energy band diagram of an Si-based SB-MOSFET [20] (Fig. 11.2a) for (**a**) n-type operation ($V_{GS} > 0$ V) and (**b**) p-type operation ($V_{GS} < 0$ V). Also, the schematic energy band diagram of an Si Nanowire-based reconfigurable SB-MOSFET [27] (Fig. 11.2c) for (**c**) n-type operation ($V_{PGS} > 0$ V) and (**d**) p-type operation ($V_{PGS} < 0$ V). V_{PGS} and V_{CGS} denote the polarity gate and control gate bias, respectively. An electron channel is formed for a positive $V_{(P)GS}$, while a hole channel is formed for a negative $V_{(P)GS}$. The V_{CGS} controls the current through the channel. Filled circles represent electrons; open circles represent holes

Reconfigurable SB-MOSFETs

Typically, the $I_D - V_{GS}$ (drain current – gate-source voltage) characteristics in symmetric SB-MOSFETs reach relatively high currents for both negative and positive V_{GS}. This effect, the so-called ambipolar effect, is caused by a gate modulated SB junction tunneling current. It is obviously not desirable, and therefore it should be suppressed.

There are several ways to suppress this ambipolarity. For example, Fig. 11.2b shows a device schematic of a nanowire (NW) SB MOSFET that exhibited ambipolar characteristics [45] with a symmetric SB source and drain. Its ambipolarity was successfully suppressed by the introduction of an additional terminal, referred to as the polarity gate (Fig. 11.2c, d).

Interestingly, however, this additional terminal also offers a new degree of freedom in the device. The device can be operated both as an n-type and a p-type MOSFET by modulating this polarity gate: a reconfigurable FET operation is obtained in which the polarity of conduction can be controlled [25–27, 48]. Basically, in these reconfigurable, or polarity controlled, devices, the conduction through the channel is controlled by a so-called control gate, while the other gate (i.e., polarity gate) controls the polarity of conduction; see Fig. 11.3c, d.

SB Electro-optical Devices

Misewich et al. [49] demonstrated polarized infrared light emission from a CNT SB-MOSFET structure as illustrated in Fig. 11.4a. The simultaneous injection of electrons and holes at the source and drain Schottky barrier junctions resulted in radiative recombination and thus light emission. The gate electrode was biased such that $V_{GS} > 0$ but $V_{GS} < V_{DS}$. In this way band bending was formed in the opposite direction at source and drain electrodes which facilitated simultaneous injection of electrons and holes at those source and drain electrodes, respectively, via narrow tunneling barriers, as shown in Fig. 11.4b.

SB contacts have also been utilized to collect photo-generated carriers in solar cells [50]. SB-based solar cells are interesting as they can be realized using only a single type (n or p type) of chemical doping unlike conventional p-i-n type cells which require both a p-type and n-type region to function. Other than in conventional Si-based material, the SB-based solar cell has also been demonstrated in CNTs [51], cadmium sulfide (CdS) [52], and molybdenum disulfide

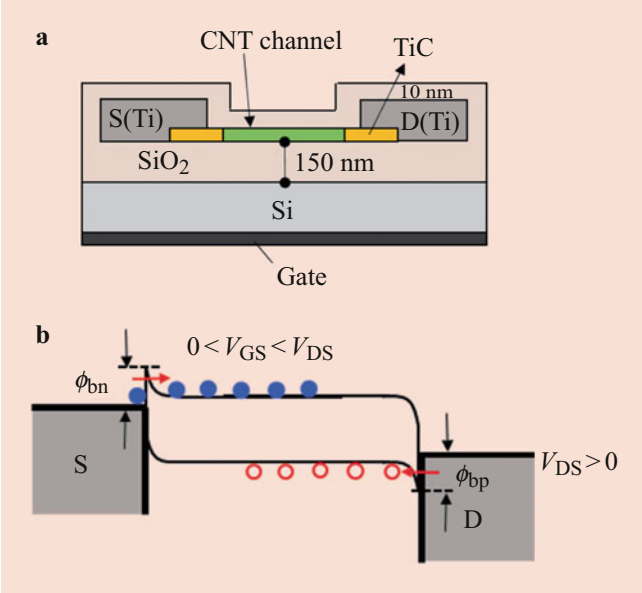

Fig. 11.4 CNT SB light emitting FET, schematic of (**a**) device cross section (**b**) energy band diagram. Electrons are injected in the CNT channel at the source electrode, while holes are injected from the drain electrode into the channel [49]

(MoS_2) [53]. In addition, an SB-based solar cell has been demonstrated in the GaInN/GaN material system without any p-type doping [54, 55].

The actual SBH for electrons (ϕ_{Bn}) and for holes (ϕ_{Bp}) at the MS junction is determined by the choice of the electrode metal. For conventional SB-FETs, unipolar operation ($\phi_{Bn} \neq \phi_{Bp}$) is desirable, while for polarity controlled SB-MOSFETs and light emitting devices [49], for instance, ambipolar operation ($\phi_{Bn} \approx \phi_{Bp}$) is interesting to adopt. Importantly, for the devices described so far, the SBH limits the current.

11.2.2 Workfunction-Induced Doping

The Nobel laureates Brattain and Bardeen [56] first reported bipolar-like current amplification in a Schottky point-contact transistor realized in n-type bulk germanium (Ge). It is believed that this amplification was attributed to a thin layer of p-type conductivity induced near the surface of the Ge via the Schottky point-contact. The formation of that layer could be explained as workfunction-induced doping or metal-induced doping.

Some years later, Bradley [57] proposed the surface-barrier transistor in which a p-type inversion layer was formed by metal-induced doping via both the emitter and collector electrode, while an ohmic contact was formed with the base electrode. This non-planar transistor was realized [58] in uniform n-type Ge without any chemically doped p-n junctions. Functional circuits with such transistors were realized as well [59]. Since then there have not been many reports specifically on this surface-barrier transistor.

However, later on many reports actually followed Brattain and Bardeen's "scaled point-contact transistor" concept as discussed further in this section.

In this section the basic theory of workfunction-induced doping in one dimensional (1-D) Schottky contacts is discussed. Thereafter, the electrostatics of 2-D gated Schottky contacts is discussed, which is important for future CMOS devices such as electrostatically doped TFETs.

1-D Schottky-Based Devices

Similar to the formation of a gate-induced inversion layer in MOSFETs, excessive band bending near the MS interface could ultimately also result in strong inversion, as illustrated in Fig. 11.1b. Such an MS junction will then show a bipolar-type conduction behavior different from the otherwise traditionally formed unipolar Schottky diode, which could be interesting for, e.g., tunnel devices.

As in a MOS capacitor [1], the onset of strong inversion can be defined when the inversion charge density equals the background doping concentration (i.e., donor concentration N_D for n-type and acceptor concentration N_A for p-type) of the semiconductor. From this definition the conditions for its occurrence can be derived.

In case of an n-type semiconductor, shown in Fig. 11.1b, strong inversion at the interface occurs when E_F lies below the E_{Fi} with an energy difference equal to $q\psi_{BI} \geq q\psi_B$, where $q\psi_B = kT \cdot \ln(N_D/n_i)$. The last term is governed by the relative position of E_F from E_{Fi} in the bulk region as defined by the background doping. This results in an SBH at the interface of $\phi_B \geq u_T \cdot \ln(N_C/n_i) + \psi_B$. Consequently, for strong inversion and thus more effective bipolar-type behavior, the following conditions hold.

For the SBH in an n-type semiconductor

$$\phi_B = (\phi_M - \chi_S)/q \geq u_T \cdot \ln\left(\frac{N_D}{n_i}\right) + u_T \cdot \ln\left(\frac{N_C}{n_i}\right), \quad (11.3)$$

and that in a p-type semiconductor

$$\phi_B = (E_G - \phi_M + \chi_S)/q \geq u_T \cdot \ln\left(\frac{N_A}{n_i}\right) + u_T \cdot \ln\left(\frac{N_V}{n_i}\right). \quad (11.4)$$

For the hole density at the MS interface in n-type semiconductors holds that

$$p = n_i \cdot \exp\left(-\frac{\psi_{BI}}{u_T}\right) = n_i \cdot \exp\left(\frac{\phi_B - E_G/2q}{u_T}\right)\sqrt{\frac{N_V}{N_C}}. \quad (11.5)$$

Likewise, for the electron concentration in p-type semiconductors

$$n = n_i \cdot \exp\left(\frac{\psi_{BI}}{u_T}\right) = n_i \cdot \exp\left(\frac{\phi_B - E_G/2q}{u_T}\right)\sqrt{\frac{N_C}{N_V}}. \quad (11.6)$$

For Eqs. (11.5) and (11.6) the semiclassical Boltzmann approximation has been used, assuming $n \ll N_C$ or $p \ll N_V$.

Hence, charge carriers of opposite polarity from the background doping can be induced near the interface of a 1-D Schottky contact provided that a suitable ϕ_M, that governs ϕ_B, is chosen. In this way an ultra-shallow p-n junction near the MS interface is formed where drift-diffusion, or possibly even band-to-band tunneling (BTBT), processes govern the current, which is different from conventional SB-based counterparts where ideally ϕ_B solely controls the charge carrier emission.

In case of an intrinsic semiconductor where $\psi_B = 0$, Eqs. (11.3) and (11.4) reduce to the following equations for p-type doping:

$$\phi_M \geq \chi_S + \frac{E_G}{2}, \quad (11.7)$$

and n-type doping:

$$\phi_M \leq \chi_S + \frac{E_G}{2}. \quad (11.8)$$

In other words, by adopting metals with a different workfunction from that of the semiconductor, it is possible to make an intrinsic semiconductor locally p-type or n-type. The position of the intrinsic Fermi level E_{Fi} is essentially described by the term $\chi_S + (E_G/2)$, i.e., the workfunction ϕ_S of the intrinsic semiconductor.

Earlier, Wittmer [60, 61] reported high barrier vertical Schottky diodes using silicided contacts on bulk n-type Si and analyzed their conduction mechanisms. Such a high ϕ_B, in case of iridium-silicide (IrSi) ~0.982 V, would result in inversion charge. Despite such high SBH, the author concluded that thermionic emission was the main mechanism for the current flow.

In [62] high barrier vertical Schottky diodes were realized by depositing aluminum (Al) on top of a p-type Si substrate with a bottom ohmic contact, for which the extracted SBH was $\phi_B = 0.77$ V. The basic idea was to experimentally verify whether the device characteristics show bipolar-type behavior instead of conventional unipolar characteristics. For this reason reference Schottky diodes were realized by depositing Al on top of an n-type Si substrate, offering a $\phi_B = 0.53$ V. The ϕ_B value of 0.77 V is not high enough for having an dominant bipolar-type behavior, but it was considered to be sufficient for the objective. Technology computer-aided design (TCAD) simulations predicted that when using thick substrates, the (minority) diffusion current and the thermionic emission current can reach equally high levels for higher ϕ_B. Moreover, the simulation results highlighted that the bipolar-type behavior hence diffusion becomes dominant for smaller dimensions, as would be the case in UTB devices, or at elevated temperatures [62]. It is therefore likely that the use of relatively thick substrates and moderate temperature range (200 K $\leq T \leq$ 300 K) in the experiments of Wittmer [60, 61] could have led to the conclusion that thermionic emission was the main mechanism.

In [62] the approach was different from that reported in [60, 61]. One of the methods to determine the bipolar effectiveness of the devices used in [62] was the so-called two-diode electrical test method [63,64]. This method makes it possible to distinguish the operation of a (Schottky-like) ultra-shallow p-n junction diode from that of a conventional Schottky diode. The experimental outcome of [62] indicated indeed that the minority carrier injection in the Al/p-Si diode is important unlike its low barrier counterpart. In addition, from the carefully designed hexagonal Schottky diodes, infrared electroluminescence experiments were carried out. The high barrier Schottky diode showed a faint glow of infrared light emission, while for its low barrier counterpart, this could not be observed, reconfirming that there is more minority charge in the former because of the higher electron emitter efficiency.

TCAD-based simulation studies have been reported before where such 1-D Schottky based p-n junctions were proposed to be utilized in a vertical Si bipolar junction transistor (BJT) structure [65] and in a gallium-arsenide (GaAs) tunnel diode [66]. For the latter, however, Fermi-Dirac statistics were applied, and therefore in principle Eqs. (11.5) and (11.6) do not hold. Nonetheless, this does not change the fact that for an effective bipolar-type behavior, a suitable ϕ_M is required.

Gated Schottky-Based Ultrathin-Body Devices

In this section, the ED concept is discussed for devices in which a dielectric layer is placed between the metal and a fully depleted (FD) semiconductor ultrathin-body [67]. In such a FD-UTB device, the depletion charge can be practically ignored. Note that for clarity sake, a long device structure is considered so that 1-D electrostatics can be used for the discussion.

Figure 11.5 shows a schematic cross section of such a gated Schottky-based FD-UTB device which is similar to an FD 2-D MOSFET. In such an FD-UTB device, assuming ideal interfaces, the potential drop in direction perpendicular to the gate electrode can be written as

$$V_{GB} = V_{ox} + \psi_s + \phi_M/q - \chi_S/q - (E_C - E_{Fi})/q \quad (11.9)$$

where V_{GB} is the applied potential difference between the gate and semiconductor body, V_{ox} is the potential drop across the oxide, and ψ_s is the surface potential, i.e., the Fermi-level shift from its intrinsic position.

Equation (11.9) can be simplified by considering not too high carrier concentrations ($n, p \ll N_C, N_V$), resulting in

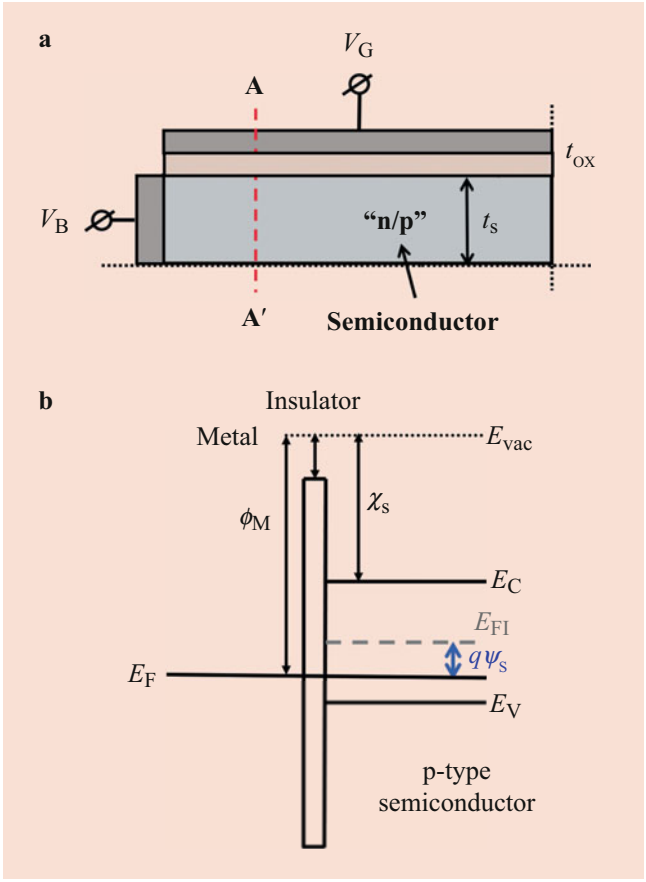

Fig. 11.5 (**a**) Schematic cross-section of a UTB device with a 2-D gated Schottky contact for workfunction or bias-induced electrostatic doping. (**b**) The energy band diagram of a p-type formed region perpendicular to the gate along the red dashed line

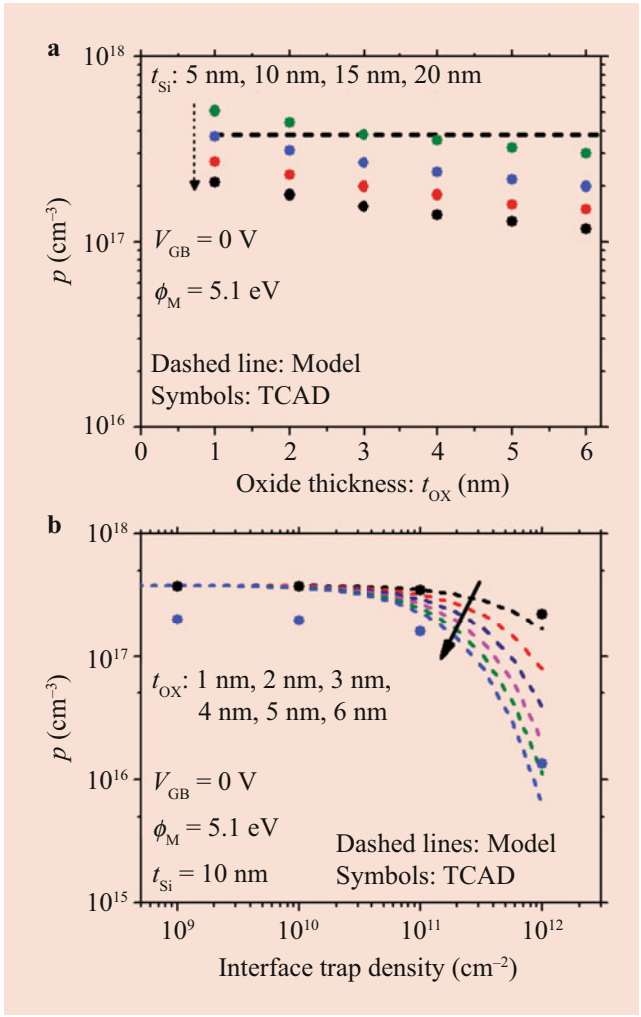

Fig. 11.6 Induced surface hole density for an Si/SiO_2 gated Schottky structure (see Fig. 11.5) with $\phi_M = 5.1$ eV as a function of the (**a**) oxide thickness with ideal interfaces and (**b**) the interface trap density [70]. A uniform distribution of both donor and acceptor traps across the bandgap [1] has been considered in the TCAD simulations [68], and the carrier density was extracted at a lateral distance of 0.5 µm from the Schottky sidewall contact

$V_{ox} \approx 0$ in an FD-UTB device, and by focussing on pure workfunction-induced doping which implies that $V_{GB} = 0$.

For this case it can be stated that

$$\psi_s = (E_{Fi} - E_F)/q = \chi_S/q - \phi_M/q - u_T \cdot \ln\left(\frac{n_i}{N_C}\right). \quad (11.10)$$

It is clear that Eq. (11.10) is the condition for workfunction-induced doping in a gated Schottky-based FD-UTB device which is equivalent to Eq. (11.7) for p-type doping ($\psi_s < 0$) and to Eq. (11.8) for n-type doping ($\psi_s > 0$). Similar to the p-n junction formation in a 1-D Schottky contact, the induced surface charge concentration can be expressed as

$$p = n_i \exp\left(\frac{-\psi_s}{u_T}\right), \quad (11.11)$$

for the hole density and for the electron density

$$n = n_i \exp\left(\frac{\psi_s}{u_T}\right). \quad (11.12)$$

In Fig. 11.6a the induced surface hole density against the oxide thickness is depicted for an Si/SiO_2 gated Schottky structure (Fig. 11.5) for $\phi_M = 5.1$ eV. According to Eq. (11.10) the induced hole density in FD-UTB devices does not depend on the insulator and semiconductor thicknesses as $V_{ox} \approx 0$ is assumed here. However, TCAD simulations [68] show different results, which can be attributed to a finite V_{ox} (~30 mV at $t_{ox} = 6$ nm and $t_S = 10$ nm) caused by a relatively high surface charge density. For studying physical trends, the model is still useful though. For obtaining more accurate results, a numerical model need to be derived [69], perhaps one that even includes quantum confinement in case of UTB layer thicknesses of less than the Broglie wavelength

(for Si this corresponds to ∼15 nm), which is not part of this discussion.

By including the effect of the interface trap charge (Q_{it}), Eq. (11.10) can be modified as

$$\psi_s = \chi_S/q - \phi_M/q - u_T \cdot \ln\left(\frac{n_i}{N_C}\right) + \left(\frac{Q_{it}}{C_{ox}}\right), \quad (11.13)$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the areal oxide capacitance. In Eq. (11.13) a uniform interface trap density is assumed, i.e., $Q_{it} = -C_{it}\psi_s$, with $C_{it} = q^2 D_{it}$ represents the areal interface trap capacitance, and D_{it} is the interface trap density [1].

After rearranging Eq. (11.13), the following condition for the workfunction-induced doping that includes the effect of interface states is obtained:

$$\psi_s = \frac{\left(\chi_S/q - \phi_M/q - u_T \cdot \ln\left(\frac{n_i}{N_C}\right)\right) \cdot C_{ox}}{(C_{it} + C_{ox})}. \quad (11.14)$$

The condition for induced electrostatic doping in a gated Schottky device including interface trap charge is basically described by Eqs. (11.11), (11.12), and (11.14). Hence, the ED effect is adversely affected by a higher interface trap density, and therefore process control is essential. Figure 11.6b shows the induced charge concentration plotted against the interface trap density using Eq. (11.14). As can be seen, the interface traps affect the ED more strongly for a larger oxide thickness: the surface hole density is reduced by a maximum of two orders in magnitude when the trap density is increased to $10^{12}/cm^2$ for an oxide thickness of 6 nm.

Charge Plasma Devices

One example of a gated Schotty device is the so-called charge plasma (CP) p-n junction diode as proposed by Hueting et al. [21, 22], shown in Fig. 11.7. The CP diode comprises a gated anode and a gated cathode with metals of a different (preferably extreme) workfunction ϕ_M. Both the anode and cathode also form sidewall contacts with the intrinsic or (unintentionally) doped semiconductor body. The basic idea is by introducing two different workfunction metals; a bipolar-type behavior in the semiconductor body can be obtained, as in a conventional (chemically doped) p-n junction. Depending on the values of the workfunctions, the rectification (or "effectiveness" of the bipolar-type behavior) of the CP diode can be improved. During operation the device is in abundance of charge carriers, hence the name "charge plasma".

For obtaining a relatively high rectification according to Eqs. (11.11) and (11.14) for the anode region, a high ϕ_M is required, while the opposite holds for the cathode region.

At a first glance, the energy band diagram of a CP diode along the lateral direction depicted in Fig. 11.7, obtained from 2-D TCAD simulations, is similar to that of a conventional p-n junction. However, there are some key

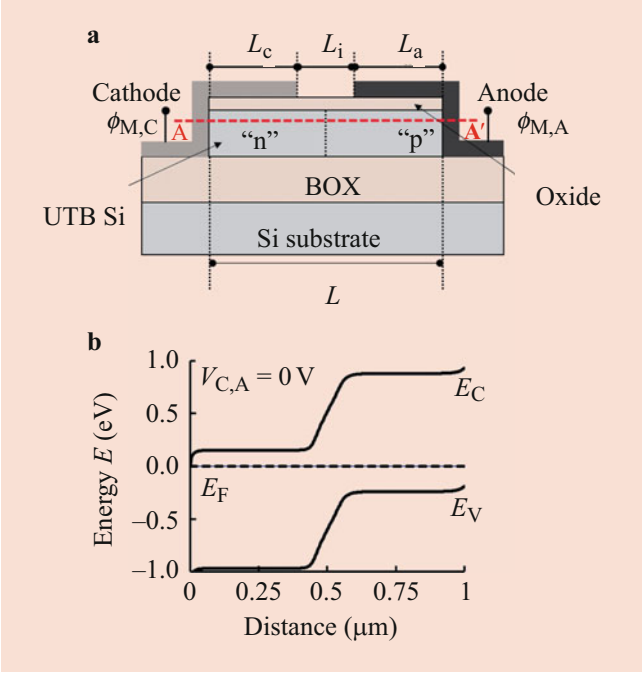

Fig. 11.7 (**a**) Schematic cross section of the CP p-n diode and (**b**) its energy band diagram along the dotted red line at equilibrium. $\phi_{M,C}$ = 4.17 eV and $\phi_{M,A}$ = 5.1 eV are cathode and anode metal workfunctions, respectively. L_c and L_a denote cathode and anode gate lengths, respectively. L_i denotes the length of the intrinsic region, i.e., the gap between the two electrodes. The thickness of UTB Si (t_{Si}) is 20 nm, and gate oxide thickness (t_{ox}) is 5 nm [21]

differences [34]. One difference is that the quasi-neutral regions of the CP diode are formed by the gates, unlike in a conventional p-n junction where the donor and acceptor ions form the space charge region. In addition, the lateral configuration shows a linear potential distribution in the intrinsic gap region because of the absence of impurities, instead of a parabolic potential profile in the conventional counterpart. For the latter the built-in electric field is formed by fixed donor or acceptor ions near the junction to balance drift and diffusion components at equilibrium. There is also a built-in field in the CP diode, but that is primarily formed by the workfunction difference at the edges of the gated regions. The band bending at the sidewall contacts is attributed to the 2-D fringe field-effect. Note that analytically derived $I-V$ models for the CP diode, based on drift-diffusion, also reproduced the $I-V$ characteristics of the CP diode obtained from TCAD simulations [71].

For the realization of the CP diode [22], palladium (Pd) was adopted for the anode electrode and erbium (Er) for the cathode. Good rectifying behavior was obtained, showing an on/off-current ratio of $\sim 10^7$ (on-current taken at $V_D = 1$ V forward bias) and room temperature, combined with a low leakage current of 1 fA/μm. Figure 11.8a shows experimental $I-V$ characteristics of various fabricated CP diodes with different anode/cathode metal combinations. From the ex-

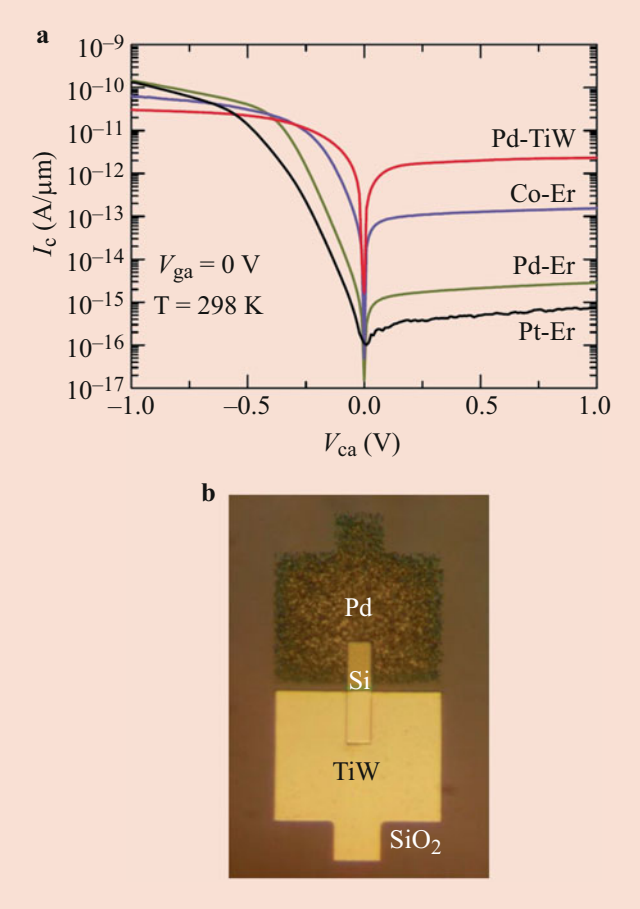

Fig. 11.8 (**a**) $I_c - V_{ca}$ characteristics for various valence and conduction level metal combinations Pt−Er, Pd−Er, Co−Er, and Pd−TiW on either side of silicon. $L_a = L_c = 0.9\,\mu m$, $L_i = 3\,\mu m$ (see Fig. 11.7). The substrate potential (V_{ga}) was kept at 0 V. (**b**) Top view of a realized CP diode showing the effect of placing a wafer with high workfunction (Pd) and low workfunction (TiW) metal islands in a chemical etching solution. The combination of the metals with the solution formed an electrolyte cell which resulted in the corrosion of highest workfunction (Pd) metal [22]

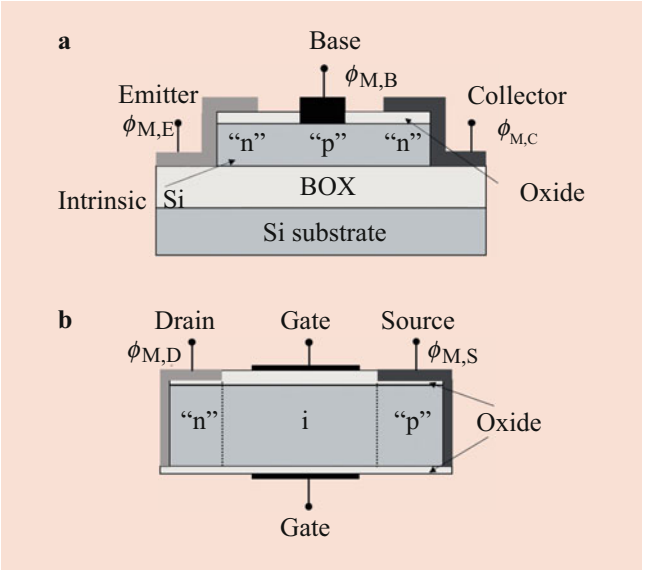

Fig. 11.9 Schematic cross section of the CP based (**a**) Lateral BJT [23], (**b**) TFET [24]. The "n" and "p" indicate electrostatically doped regions

perimental observations, it can be concluded that the hole and electron current are equally important for the CP diode: the total current increases when the anode workfunction is reduced by replacing platinum (Pt) with Pd or cobalt (Co), or conversely, the cathode workfunction is increased by replacing Er with titanium-tungsten (TiW). In the same experimental work [22], MOSFET characteristics were obtained with a symmetric gated anode/cathode electrode structure where the substrate was used as a back gate.

The charge plasma concept has been extended to other types of devices. Kumar and Nadda [23] proposed and investigated the charge plasma-based lateral bipolar junction transistor (BJT) incorporating electrostatically doped regions in the emitter, base, and collector regions of a conventional BJT using metals with different workfunctions, as shown in Fig. 11.9a. The authors proposed to use hafnium (Hf) ($\phi_{M,E} = 3.9\,eV$) for the emitter, Pt ($\phi_{M,B} = 5.65\,eV$) for the base, and Al ($\phi_{M,C} = 4.28\,eV$) for the collector electrode, resulting in an n^+-p-n configuration. This 2-D TCAD simulation study shows device characteristics similar to that of the conventional chemically doped counterpart but with improved current gain.

Another, high potential, charge plasma-based device is the doping-less TFET, proposed by Kumar and Janardhanan [24]; see Fig. 11.9b. Similar to the CP-BJT, in this TFET electrostatically doped regions were incorporated by employing metals with a different workfunction: Hf for the n-type drain and Pt for the p-type source. The performance of this charge plasma-based TFET was found to be similar to the conventionally doped TFET with the same device geometry.

Unfortunately, so far most of these charge plasma-based architectures have not been experimentally verified. Table 11.1 summarizes other proposed charge plasma devices reported in the literature. Interestingly, similar ideas for electrostatically doped graphene via metal electrodes have also been reported [30–33, 72–74].

11.2.3 Bias-Induced Doping

For the electrostatics at the MS interface, hence the charge in the UTB, the externally applied electric field is also important. Even though this appears to be similar to the conventional field-effect, one important different aspect should be taken under consideration. In conventional FETs the charge carriers originate from (chemically) doped semiconductor regions (i.e., source/drain regions) in close vicinity of a chan-

Table 11.1 Summary of various reported electrostatically doped materials and device concepts till date. The abbreviation (exp.) highlights reports that experimentally demonstrated device concepts, other reports concern modeling, and TCAD simulation studies only

Material	SB-based devices	Workfunction-induced ED	Bias-induced ED
Si, Si UTB, and Si Nanowire	SB-MOSFETs (exp.) [19,20], FinFET (exp.) [46], Si nanowire based SB-MOSFETs (exp.) [45], reconfigurable FETs (exp.) [25–27], reconfigurable devices (exp.) [28,29]	CP based p-n diode (exp.) [21,22], BJTs [23,65,89,90], TFET [24], IMOS [91], Junctionless transistor [92], Biristor [93], SiGe-on-insulator MOSFET [94], graded channel MOSFET [95]	EH bilayer TFET [39,40], EH bilayer TFET (exp.) [41]
CNT	SB-MOSFETs [35,36,47], Light emitting SB-FET (exp.) [49], solar cell (exp.) [51]		p-n diode (exp.) [34], FET (exp.) [75]
Graphene		Graphene ED [32]	Graphene ED [72], Graphene FET (exp.) [30,31,33,73,74]
III-V materials	GaN n-type SB-MOSFET (exp.) [96], GaInN/GaN solar cell (exp.) [54,55]	GaAs Tunnel diode [66], GaN n-MOSFET [97], InAs TFET [98]	GaAs EH Bilayer (exp.) [99], InAs/-GaSb EHB-TFETs [87,88]
Polycrystalline materials, others	CdS solar cell (exp.) [52]	CP based poly-Si TFT [100], IGZO TFT (exp.) [101]	
2-D materials	n-type, p-type SB-MOSFET (exp.) [102,103], MoS_2-based solar cell (exp.) [53]		2-D transistors [37,38]

nel, whereas in case of the electrostatically doped concept, the charge carriers originate from metal electrodes directly contacting the semiconductor body. These metal electrodes are not necessarily forming a gate, but they are important as a source of charge carriers. Refer to the gate region shown in Fig. 11.5. For this type of ED, i.e., the bias-induced doping, similar conditions apply compared to the workfunction-induced doping (Eq. 11.10), though a non-zero V_{GB} term should be accounted for

$$\psi_s = V_{GB} + \chi_S/q - \phi_M/q - u_T \cdot \ln\left(\frac{n_i}{N_C}\right). \tag{11.15}$$

Using a non-zero V_{ox} term in Eq. (11.9), similar relations can be obtained for a bulk or partially depleted semiconductor device. The workfunction difference $(\phi_M - \phi_S)/q$ actually corresponds to the term $(\chi_S/q - \phi_M/q - u_T \cdot \ln(n_i/N_C))$, which is zero for a purely bias-induced doping. In this case it is clear that a positive V_{GB} will induce n-type doping, while a negative V_{GB} will induce p-type doping. Furthermore, the effect of interface traps can be included as well

$$\psi_s = V_{GB} + \chi_S/q - \phi_M/q - u_T \cdot \ln\left(\frac{n_i}{N_C}\right) + \left(\frac{Q_{it} + Q_{inv}}{C_{ox}}\right), \tag{11.16}$$

where Q_{inv} is the areal mobile inversion charge. Again, it can be concluded that the interface traps affect the ED effect: both the gate and interface traps control the mobile charge. Note that earlier modeling work on I–V characteristics of asymmetric double-gate (DG) devices [69] could be used for modeling bias-induced doping including interface traps.

Importantly, for devices based on bias-induced doping, side metal contacts with a midgap (or solely p- or n-type) workfunction or doped regions are needed for a successful operation. Alternatively, the charge carriers could also be supplied via thermal generation but that will only work for narrow bandgap semiconductors ($\lesssim$1 eV).

For a simultaneous formation of p-type and n-type charged regions in a semiconductor body via an externally applied field, a double (or multiple) gate UTB device could be employed. By biasing two gates with opposite polarities, electrons and holes can be simultaneously generated in a semiconductor body as expressed by Eqs. (11.15) and (11.16). The relative position of those gates will then play an important role [34,39], as discussed in the next section.

Lateral p-n Junction

For the first time, bias-induced electrostatic doping was experimentally demonstrated in a CNT system [34] where a lateral p-n junction diode was formed adopting a split gate configuration as shown in Fig. 11.10. An n-type doping of the CNT channel region adjacent to the first gate electrode was obtained by biasing this electrode with a positive voltage with respect to the CNT body. Similarly, a negative voltage with respect to the CNT body at a second gate resulted in a p-type doping. As a result, an electrostatically doped lateral p-n junction diode was formed in the CNT channel. The fabricated device showed rectifying characteristics with an ideality factor close to one. In addition, biasing both gate electrodes with the same polarity resulted in either an n-channel or a p-channel FET. BTBT was also observed in CNTs [75] basically demonstrating an electrostatically doped p-n junction tunnel diode, which laid the foundation for the CNT-TFET.

Also experiments have been reported showing the strong potential of bias-induced doping in an advanced and mature FD-SOI process [28,29] that also includes a unique back gate feature. The authors demonstrated for the first time that their reconfigurable device can be transformed into multiple (i.e.,

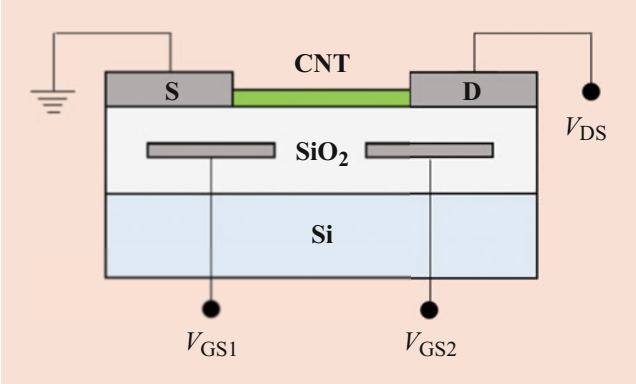

Fig. 11.10 Schematic cross section of the CNT p-n diode [34]. The split gate configuration was used to electrostatically induce a lateral p-n junction. Biasing $V_{GS1} < 0$ would give a p-type region in the adjacent CNT channel, and $V_{GS2} > 0$ would result in an n-type region

nine) types of devices with different functionalities, such as virtual diodes, TFETs, p-i-n diodes, and band-modulation FETs. Their device structure had a five terminal configuration, among which two back gates and a single (front) gate. The authors even went further: they experimentally demonstrated an electrostatically doped Esaki diode at low temperatures ($T = 77$ K) in the same FD-SOI process [76]. As stated earlier (though with a focus on FETs) [77], the authors emphasized that their work could open a new route toward reconfigurable circuits, but they also highlighted that this feature could be interesting for device or layer characterization.

Vertical p-n Junction: Electron-Hole Bilayer (EHB)

Another type of a potentially attractive device configuration is the bias-induced electron-hole bilayer (EHB) formed by two vertically faced gates with an opposite bias polarity, as illustrated in Fig. 11.11. As a first demonstration, a double-gate (DG) SiO_2/Si/SiO_2 structure with a 22 nm thick silicon layer was realized [78, 79].

This structure is interesting for, e.g., tunnel FETs [39, 40] but in some semiconductor material systems for light-emitting devices as well [80], though there are different requirements. For example, in tunnel FETs a relatively narrow overlap between an ultra-high electron and hole density profile in the semiconductor body is required that should be strongly controlled by the gate. For light-emitting devices on the other hand, a relatively wide overlap between moderately to high electron and hole density profiles is needed.

The performance of the EHB concept strongly depends on the thickness of the semiconductor body. For example, for a relatively thick semiconductor with a partially depleted channel, there is no electrostatic coupling between the metal gates, and therefore at both sides of the body, the bias-induced charge near each gate can be described with Eq. (11.15) (for $n, p \ll N_c, N_v$). For an FD-UTB configuration with a double

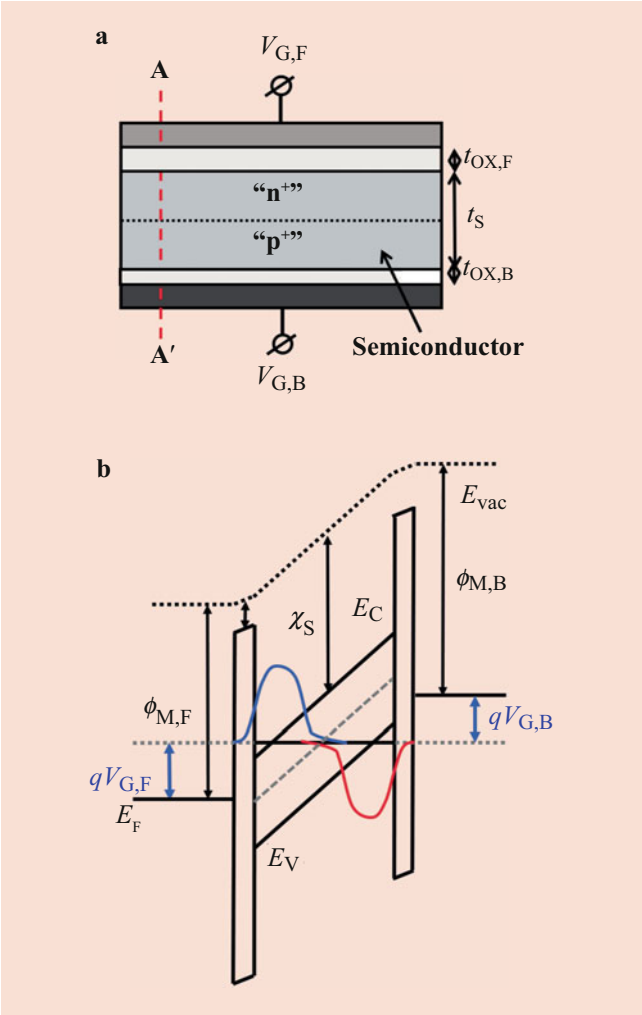

Fig. 11.11 (**a**) A schematic cross section of the electron-hole bilayer (EHB) concept. (**b**) The energy band diagram perpendicular to the gates along the red dashed line indicated in the left figure. By enforcing a bias with an opposite polarity between the top and bottom gate, a tunnel junction can be formed. The wave function curves represent the electron (**a**) and hole (**b**) distribution in the EHB structure for illustration purposes

asymmetric gate structure however, the electrostatic coupling between the gates needs to be taken care of. Following the early work of Lim and Fossum [81] and assuming a not too high charge carrier concentration, for a coupled EHB double gate structure, the following relation for the vertical electric field in the semiconductor body can be derived:

$$\mathcal{E}_s = \frac{(V_{G,F} - V_{G,B}) - (\phi_{M,F} - \phi_{M,B})}{\frac{\varepsilon_S}{\varepsilon_{ox}}(t_{ox,F} + t_{ox,B}) + t_S}, \tag{11.17}$$

and for the surface potentials at both interfaces

$$\psi_{s,F/B} = V_{G,F/B} \mp \frac{\varepsilon_S \mathcal{E}_s}{C_{ox,F/B}} - \Delta\phi_{M,F/B}, \tag{11.18}$$

where the subscripts F and B refer to the front and back of the structure, respectively. $\Delta\phi_{M,F/B}$ is the gate-body workfunction difference, and $C_{ox,F/B}$ is the areal oxide capacitance; t_{ox} and t_S are the oxide and semiconductor thickness, respectively. In Fig. 11.12a $\mathcal{E}_s$ is plotted as a function of the semiconductor body thickness t_S for an $HfO_2/Si/HfO_2$ EHB structure, also showing that Eq. (11.17) is in good agreement with the TCAD simulations [68]. Semi-classically, $\psi_{s,F} > 0$ results in an induced electron channel at the front gate electrode with density $n = n_i \exp(\psi_{s,F}/u_T)$ (refer to Eq. (11.12)). Similarly, if $\psi_{s,B} < 0$ a hole density near the back gate electrode at the interface is formed according to $p = n_i \exp(-\psi_{s,B}/u_T)$. It is however rather difficult to obtain closed form solutions for $\psi_{s,F}$ and $\psi_{s,B}$. Moreover, quantum effects should also be included as this will change this picture [82] as qualitatively shown in Fig. 11.12b using TCAD simulation. The effect of fixed or interface charge can also be included which obviously counteracts the ED effect [70].

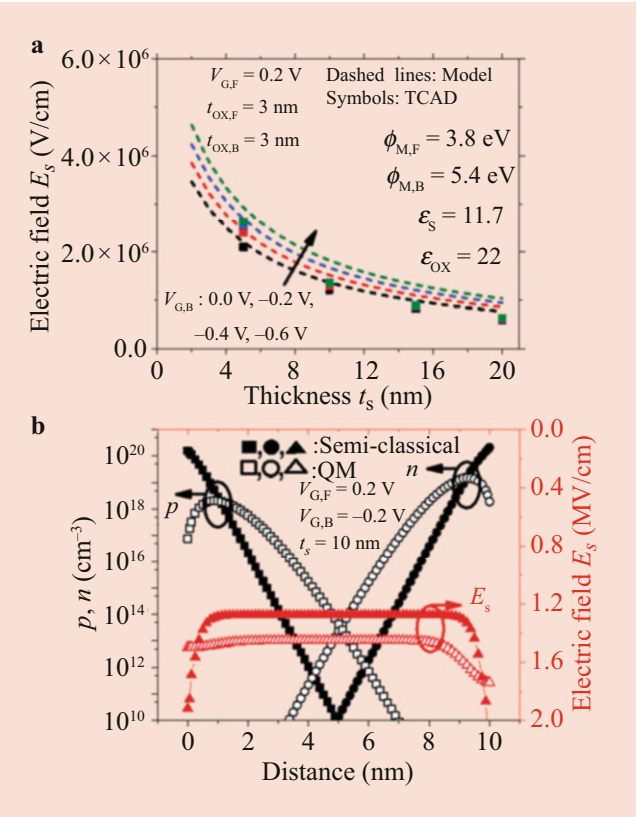

Fig. 11.12 (**a**) The vertical electric field in the $HfO_2/Si/HfO_2$ EHB structure (refer to Fig. 11.11) for various semiconductor body thicknesses. Quantum mechanical (QM) effects have not been taken into account both in the model (Eq. 11.17) and TCAD simulation [68]. (**b**) TCAD simulation of charge carrier distribution and electric field profile in the vertical direction along the red dashed line of Fig. 11.11 with $t_s = 10$ nm and $V_{G,F} = 0.2$ V and $V_{G,B} = -0.2$ V. TCAD simulation of the induced electron and hole bilayer at vertically opposite interfaces of a dual gate structure is shown using both semi-classical (using Poisson only) and QM (density-gradient model [83]) approaches. The detailed quantitative calibration of the QM model in TCAD was not the focus of this work

Lattanzio et al. [39,40] proposed a DG TFET based on the EHB concept and adopted TCAD simulations to investigate the device behavior. They reported the formation of a vertical EH bilayer in the UTB device by asymmetrically biasing the opposite gates. Eventually for a specific front-back gate bias difference (~0.1 to 0.5 V), the drain current was shown to increase via the BTBT mechanism of charge carriers in the EHB p-n junction [82]. In this case the direction of tunneling is parallel to the gate field, i.e., line tunneling [85]. Because of the relatively large tunneling surface area and a stronger electrostatic control over both n-type and p-type regions in the subthreshold region, this results in a higher on-state tunneling current compared to, e.g., the doping-less TFET [24]. The effectiveness of such an EHB formation however has been debated [41, 86]. Experimentally realized EHB-TFET structures have been reported [41] for which the trade-off between the applied field (or electrostatic doping) and quantum confinement was discussed. According to this work, the condition to have both an efficient BTBT and the formation of the EHB cannot be simultaneously satisfied.

However, so far only a single semiconductor layer in the UTB region of the EHB-TFET has been considered. This ED-quantum-confinement trade-off could be broken, for example, by employing heterostructures in the UTB region in which a broken gap in the energy band diagram has been formed. Elaborate TCAD simulations on InAs/GaSb EHB-TFETs [87, 88] have shown that in fact due to quantum confinement the broken gap at the InAs/GaSb interface closes, i.e., becomes staggered, improving the BTBT behavior which results in extreme steep-subthreshold slopes.

11.3 Electrostatic Doping Approaches: Discussion

Table 11.1 summarizes and classifies various electrostatically doped device concepts. Based on this literature survey, it can be concluded that a high carrier density of both p- and n-type (~10^{18} – 10^{20} cm^{-3}) can be formed by ED in nanometer-scale (i.e., UTB) devices, particularly for narrow bandgap semiconductors. Figure 11.13 shows the induced charge carrier concentration using Eqs. (11.10), (11.11), and (11.12) for gated Schottky regions in the CP-UTB device (refer to Fig. 11.5) for various semiconductor materials. Note that an experimental effective charge carrier density of ~10^{19} cm^{-3} in electrostatically doped Si nanowire devices has been reported [77].

For most semiconductor materials, a high electron density in their UTB can be obtained relatively easy, by adopting a suitable workfunction for the gate electrode such that

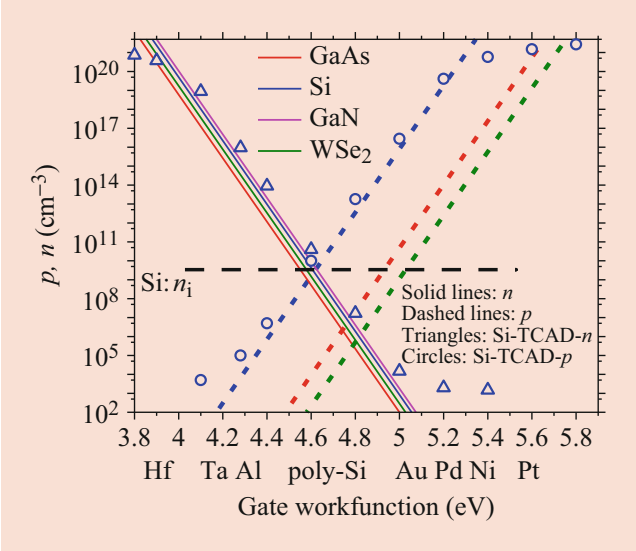

Fig. 11.13 Calculated induced carrier concentration (Eq. (11.10)) in "n" and "p" type gated Schottky regions of the CP diode structure (refer to Fig. 11.7) with a varying workfunction of the gate electrode. The calculation is performed for different semiconductor channel materials (Si ($E_g = 1.12$ eV, $\chi_s = 4.07$ eV), GaAs ($E_g = 1.42$ eV, $\chi_s = 4.07$ eV), GaN ($E_g = 3.39$ eV, $\chi_s = 4.1$ eV), WSe_2 ($E_g = 1.56$ eV, $\chi_s = 4.03$ eV) [84]) in the UTB device. TCAD simulation (symbols) for Si shows good agreement with the model. In both the model and TCAD simulations, ideal interfaces have been assumed

Eq. (11.8) is fulfilled. For electrons the electrostatic doping is governed by the electron affinity of the semiconductor body and the metal workfunction, and in practice there are many conventional metals or pure metal elements available to fulfill this [1, 43, 104]. The range of workfunctions of pure metal elements varies roughly between 2.14 eV Cesium (Cs) and 5.65 eV for Platinum (Pt).

However, to obtain a high hole density in UTB devices is for some, particularly wide bandgap, semiconductor materials more difficult. This can be attributed to the fact that the semiconductor bandgap plays an important role here; see Eq. (11.7). For obtaining a sufficiently high hole density metals with workfunctions, above 5.65 eV are needed, and those do not exist in the form of a pure elemental metal. Alternatively, other materials than traditional metals could be employed for this.

MoO_x has been reported [105, 106] to be a semiconductor with a wide bandgap (~3.3 eV). However, because of possible internal oxygen vacancies, which could arise in case of evaporated films ($x < 3$), defect band formation occurs near its conduction band which imparts it high conductivity. Provided that a layer thicknesses of less than 20 nm is used, MoO_x can be considered as a metal with a workfunction varying between ~5.5 to 6.6 eV [107]. This material has been applied for Si solar cells [105, 106] as a "hole selective" layer but could possibly be implemented with other semiconductor materials as well.

There have been reports in using MoO_x for transistors as well. Other than the mostly reported n-type MoS_2 device [102], recently a p-type MoS_2 transistor [103] was demonstrated with an I_{on}/I_{off} ratio of 10^4 employing a Schottky contact with a high workfunction MoO_x for efficient hole injection.

Either way, for this kind of alternative materials, more research is needed.

In the following the potential of electrostatic doping for future CMOS is discussed and compared with chemical doping. This also includes the possible drawbacks that go along with it.

11.3.1 Potential ED Devices for Future CMOS

Out of many various electrostatically doped devices that have been reported so far, there are three types that appear to be the most promising for future CMOS: (1) the SB-MOSFET, (2) the reconfigurable FET, and (3) the TFET.

In this category, so far the SB-MOSFET has been the most experimentally investigated device. A detailed review has been reported [20] that elaborated on the competitiveness of this device concept for ultimately scaled CMOS. The SB-MOSFET offers improved performance in terms of the off-current (I_{off}) and elimination of the parasitic bipolar action, in addition to its technology benefits in terms of scalability to sub-30-nm gate lengths and lower temperature processing along with less lithography steps. The low parasitic source/drain resistance (that represents ~1% of its total resistance) of the SB-MOSFET also makes it attractive for high-speed analog applications. The incorporation of metal source/drain regions in UTB SB-MOSFETs helps in reducing the parasitics, and it is claimed [108] that for relatively low SBHs, those devices get better performance than conventional MOSFETs. In addition, the SB-MOSFET concept has been experimentally demonstrated in alternative materials like CNTs but also in different geometries such as nanowires and FinFETs. Albeit that the SBH in the SB-PMOS and NMOS devices needs to be further optimized from view point of improved I_{on} and I_{off} to become CMOS competitive. Barrier height lowering techniques such as the implementation of a thin interfacial layer are being explored but are challenging from process integration view point [20].

Because of its tunable functionality, the reconfigurable nanowire FET (RFET) [26, 77] is also conceptually attractive for future CMOS. The performance of various RFETs has been experimentally demonstrated, and their operation in logic circuit applications has been evaluated in [77]. In addition to the polarity control, for low-power CMOS, it is important to have a symmetric transfer characteristic for both n-type and p-type FET operation. This could be obtained by fine-tuning the metal workfunctions in the devices. The I_{off} in the RFET can be suppressed by its extra gate, i.e., the control

gate [26], which is especially important for narrow bandgap channel materials for which high leakage currents form a big concern.

In their RFET-based CMOS inverter, the same authors [77] extracted a propagation delay of 35 ps at $V_{DD} = 5\,V$ which could be further optimized. They also demonstrated a reconfigurable NAND/NOR logic operation with a lower amount of FETs than would have been required for the same functionality in conventional CMOS [77]. It is clear that the RFET concept is not only limited to nanowires. Provided an efficient electrostatic control, it can be adopted to any other low-dimensional (preferably CMOS compatible) material, such as FD-SOI [109]. However, in the high-level RFET-based CMOS circuitry managing, a large amount of programming gate signals could become too complex and hence could be a concern.

Generally, the TFET has been considered to be the potential candidate for future low-power CMOS switches [4, 5]. And particularly for this type of device, doping control is the key. ED therefore offers an potential solution. Although mainly based on TCAD simulation studies, novel electrostatically doped TFET concepts such as the CP-TFET [24] and the EHB-TFET [110] have been reported to be competitive to conventionally doped counterparts, and those could therefore be interesting for future CMOS. For example, Lattanzio et al. [110] concluded from their calculations that Ge-based EHB-TFETs outperform doped DG-TFETs in terms of intrinsic delay. They estimated that the intrinsic delay for a single EHB device was less than 1 ns at $V_{DD} = 0.25\,V$ with a theoretically maximum operating frequency of 1.39 GHz. Also, other types of EHB-TFETs, such as the InAs/GaSb EHB-TFET [87,88], have a high potential because of the predicted extreme subthreshold slopes. On the other hand, many technological challenges will then have to be overcome.

Cristoloveanu et al. [28, 29] demonstrated one essential feature of ED: tunable transformation of device functionality. For the first time they reported a reconfigurable TFET and even a band-modulation FET obtained from a single five terminal electron device realized in a mature FD-SOI process. If carefully optimized, such a reconfigurable TFET could open a new route toward low-power reconfigurable CMOS circuits, although, as stated before, such a reconfigurable circuit could eventually become too complex, especially when multiple back gates are used. The same research group also recently presented an overview about this work [111].

Other recently proposed electrostatically doped TFET designs [38,98] also offer distinct advantages. Ilatikhameneh et al. [38] proposed to enhance the field in a lateral electrostatically doped tunnel junction using low-κ dielectric spacers in between high-κ dielectrics in the gated regions. The device performance of such a dielectric engineered TFET (DE-TFET) is also less sensitive to the gate dimensions compared to previously discussed electrostatically doped TFETs [24, 84].

Pan and Chui [98] proposed to adopt a gate design in their electrostatically doped TFET structure that comprises two different metal workfunction electrodes which are physically and electrically shorted. They highlighted that, unlike in their proposed gate design, the minimal tunneling width of previous TFET designs is limited by the lithography resolution of the inter-gate spacing. They also claimed that their design overcomes the limitations of bias-induced quantum confinement effects which could have a counteracting effect on the device performance as in the EHB-TFET [82]. On the other hand, it could be technologically challenging to obtain the essential feature in this design, an abrupt transition between the gate metals (i.e., metal heterojunction) by preventing metal intermixing, in addition to avoiding workfunction pinning.

Then there is also a wide span of choice in materials. Transistors based on 2-D materials such as transition-metal dichalcogenides (TMDs) [37, 84, 102, 103] and graphene [33, 74] are interesting candidates for future low-power and high-speed CMOS [16]. In this class of materials, ED is the most applied doping technique. The key challenge for the technology development here however is to obtain an MS interface with a low contact resistance.

In summary, provided that the quality of all interfaces has been taken care of, the performance of electrostatically doped devices could be highly competitive with chemically doped devices. On the other hand, more extensive experimental research is needed to confirm whether ED could ultimately replace chemical doping in mainstream CMOS technology. Nevertheless, the ED techniques is the potential solution for alternative materials such as graphene, CNTs, TMDs, and nanowires, where chemical doping faces a big challenge. Particularly innovative device concepts such as EHB-TFETs and reconfigurable devices, which could not be realized using chemical doping, have a strong potential which could open a new route toward future CMOS technology.

11.3.2 ED: Limitations and Drawbacks

Although ED appears to be very promising, there are still some limitations and drawbacks from a technology perspective that need to be considered when adopting it for device applications.

First, for adopting the ED concept in new device designs, generally ideal MS contacts or interfaces have been considered. However, many experimental data indicate that the observed "effective" workfunctions on various MS systems deviate from their bulk values. Consequently, the linear relationship between ϕ_B and ϕ_M may not always be valid [43]. The assumption of an ideal, abrupt, and non-reactive MS interface does not hold in practice. The possible chemical reaction between a metal and a semiconductor, interdiffusion, and the presence of interface dipoles cause a differently observed ϕ_B than that predicted from the ideal Schottky-Mott relation [112] where ϕ_B has a linear relationship with

ϕ_M. In that respect, the detailed review on the physics and chemistry of SBHs at MS interfaces reported by Tung [113] is interesting, among which its overview of various strategies for modifying ϕ_B. For example, the review paper describes that by an insertion of a thin ($\approx$2 nm) interfacial layer at the MS interface, chemical interdiffusion is avoided and that it also decouples the electron states in the semiconductor from the influence of the metal [43]. Typically, the ϕ_B obtained from such an metal-insulator-semiconductor (MIS) system shows a much stronger dependence on the metal workfunction than an MS interface without an intentionally grown interfacial layer [113, 114]. Such a thin interfacial layer could therefore be a solution for the realization of workfunction-induced electrostatically doped devices [115]. Since most electrostatically doped devices can be realized via low temperature processing, the metastability of the thin interfacial layer is not of a major concern. For future 2-D electronics on the other hand, the formation of a van der Waals MS contact [116] has a strong potential. In such an MS contact an atomically flat metal thin film is laminated onto a 2-D material, so that there is no direct chemical bonding. This creates an MS interface essentially free from defects and Fermi-level pinning. In this way the ideal Schottky-Mott relation can be obtained.

Second, the local workfunction variation of a metal layer could be a concern [117, 118], particularly for metal nitride gates like titanium-nitride (TiN) [119] caused by their polycrystalline nature. This could be deteriorating the effectiveness and uniformity of workfunction-induced doping and may induce device variability.

Third, during wet processing of electrostatically doped devices, the incorporation of different metals in galvanic contact may lead to corrosion [22]. Therefore rather than wet etching, alternative metal patterning approaches are recommended, such as dry etching, damascene, or lift-off.

Fourth, the effect of geometrical scaling in electrostatically doped devices may be different from chemically doped counterparts [37]. Atomistic simulations of such an electrostatically doped 2-D material transistor showed a different behavior from devices with the same EOT (equivalent oxide thickness) for a wide span of physical oxide thicknesses. Therefore, a new scaling theory and design guidelines were proposed [37] for such electrostatically doped devices where the actual physical oxide/dielectric thickness is more critical. The authors proposed to employ ultra-thin wide bandgap oxides for the gate dielectric for obtaining both an optimized ED and suppressed gate leakage.

Fifth, for wide bandgap semiconductors such as GaN with $E_G = 3.4$ eV and electron affinity $\chi_S = 4.1$ eV, the condition for the workfunction-induced n-type doping, i.e., $\phi_M < (\chi_S + E_G/2)$, can be satisfied with a lower workfunction metal like Al. However, for p-type ED in GaN a workfunction higher than 5.8 eV (see Fig. 11.13) would be required, which is not realistic. A possible solution to this problem could be the bias-induced doping approach with a metal having a reasonably high workfunction and polarization doping or to employ alternative materials such as MoO_x (or a combination of those).

Further, generally in any material system, for the optimal performance of an electrostatically doped device, a minimal lateral spacing between the gates is desired [37] which is mainly limited by the lithographic resolution. For wide bandgap materials, this forms a more critical aspect as the highly resistive intrinsic gap between the two electrostatically doped regions could lead to a reduced I_{on} and high turn-on voltages. As discussed earlier, Pan and Chui [98] proposed to overcome this limitation in their new electrostatically doped TFET design making use of a gate electrode comprising two different metal workfunction electrodes. Such ideas can be explored for other electrostatically doped devices as well.

Finally, interface traps could counteract the electrostatic (doping) control as discussed before. For gate dielectrics this remains to be an issue and can only be carefully controlled in a mature technological process. For forming contacts however, incorporating a thin interfacial layer is a potential solution to minimize the effect of interface traps on induced charge [113, 115].

11.4 Conclusion

Electrostatic doping offers an alternative solution to chemical doping in nanometer-scale devices, irrespective of the type of material systems ranging from ultrathin-body bulk semiconductors to carbon nanotubes, graphene, and other 2-D semiconductors.

It can be concluded that for an effective electrostatic doping, several physical parameters, and the interplay between them, play a key role: (1) the metal workfunction, (2) the energy bandgap and the electron affinity of the semiconductor material, and (3) the applied bias. From the literature and the developed physical understanding, it can be concluded that the electrostatic doping techniques can be adopted to induce high charge carrier concentrations, in particular for forming n-type doping, in active ultrathin-body devices. For obtaining high p-type doping levels, generally this technique is more effective for narrow bandgap ($\lessapprox$1.1 eV) semiconductors.

The relatively low temperature processing with a fewer lithography steps makes electrostatic doping attractive as well. Electrostatically doped devices, especially SB-MOSFETs, reconfigurable devices, and TFETs, offer a great potential for future CMOS. However, many of these device architectures, in particular TFETs, are based on TCAD simulation studies. Consequently, much more experimental research is needed in evaluating the true merit of these device ideas in alternative material systems and innovative device concepts for future CMOS.

In addition, the current major limitations of the electrostatic doping techniques are the presence of interface traps, the local metal workfunction variation, processing with multiple metals, and to some extent the applicability to wide bandgap materials. These need to be extensively addressed to meet the expectations for future CMOS technology.

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Planar MOSFETs and Their Application to IC Design

12

Salim El Ghouli and Denis Rideau

Contents

12.1 Introduction . . . 391

12.2 Planar MOSFET Evolution . . . 392
12.2.1 From Bulk MOSFETs to UTBB FDSOI . . . 392
12.2.2 Analog and Digital Design Needs . . . 394

12.3 Model for Drain Current and First-Order Parameter Extraction . . . 395
12.3.1 UTBB FDSOI Device Cross Section . . . 395
12.3.2 Drain Current Model . . . 396
12.3.3 Parameter Extraction from Measurements . . . 398
12.3.4 Do We Need a Quantum Approach for Ultimate Silicon-Based UTBB FDSOI? . . . 401
12.3.5 Back Biased UTBB FDSOI MOSFET . . . 403

12.4 MOSFETs in Analog Design . . . 405
12.4.1 Inversion Level Metric . . . 405
12.4.2 MOSFET g_m/I_D Invariance . . . 406
12.4.3 MOSFET Efficiency at High Frequency . . . 410
12.4.4 Small-Signal Equivalent Circuit . . . 412
12.4.5 High-Frequency Modeling . . . 414

12.5 Application Example: LNA Analog Design in MI Regime . . . 415
12.5.1 LNA Circuit Characteristics . . . 416
12.5.2 Passives-Related Constraints and Length Selection . . . 416
12.5.3 IC Selection . . . 417
12.5.4 Width and V_{GS} Calculations . . . 417

12.6 Conclusions . . . 418

References . . . 419

Abstract

Planar MOSFETs are widely recognized as key drivers of the semiconductor industry. This chapter presents analytical models and useful charts for IC design using the most advanced planar MOSFET technological nodes. After a brief review of the progress in MOSFET architectures, the state-of-the-art UTBB FDSOI technology advantages are compiled, and some important designer needs are reminded. The main physical ingredients involved in the MOSFET strong inversion operation are reviewed and generalized to the UTBB FDSOI transistors with a particular focus on the back-gate voltage impact. For better insight into the weak inversion and moderate inversion regimes, both the low-frequency g_m/I_D FoM and the high-frequency y_m/I_D FoM are presented. A modeling of the UTBB FDSOI MOSFET is proposed for low-frequency and high-frequency operations and compared to measurements considering distributed effects in both the gate and the channel. The results show excellent agreement across all regimes of operation including very low bias conditions and up to 110 GHz. Finally, an LNA circuit first-cut sizing procedure using presented charts is proposed for an expected operation at 35 GHz.

Keywords

UTBB FDSOI · MOSFET · Drain current · gm/ID · Analog design

12.1 Introduction

The metal-oxide-semiconductor field-effect transistor (MOSFET) is by far the most used semiconductor device in analog and digital integrated circuits (ICs). In digital ICs including logic and memory, the MOSFET is mainly used as a switch (i.e., ON state when gate voltage is high and OFF state when gate voltage is low) or a logic gate in order to execute Boolean logic operation, while it is used as a transconductance for signal amplification and conversion in analog ICs. Silicon technologies have been driven for years by downscaling the MOSFET dimensions dictated by the high-performance integrated digital circuits [1]. Recently, further reduction of MOSFET dimensions has

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become critical due to intrinsic limitations such as short-channel effects (SCEs). To overcome these challenges, the semiconductor industry has developed successful strategies such as the use of new materials and revolutionary device architectures, including planar double-gate (DG) ultra-thin body and box (UTBB) fully depleted (FD) silicon-on-insulator (SOI) MOSFET, vertical DG FinFET, and multiple-gate (MG) MOSFET [2–4].

With the aggressive downscaling of the MOSFET, it has become gradually more subtle to understand the key device physical parameters entering in the drain current model. Analytical models using first-order parameters (e.g., mobility, saturation velocity, etc.) and invariant charts help IC designers in their hand calculations to gain insight into the device operation prior to the necessary SPICE simulations using compact models. In this chapter, after a brief history of the MOSFET architecture in Sect. 12.2, a drain current model using first-order parameters in planar MOSFETs operating in the strong inversion (SI) regime is presented in Sect.12.3. In Sect.12.4, the g_m over I_D charts are presented and generalized to all the frequency spectrum for analog applications. Low- and high-frequency non-quasi-static (NQS) models are also proposed. Application of planar MOSFETs is exemplified in Sect.12.5 by the paradigmatic case of an LNA analog circuit.

12.2 Planar MOSFET Evolution

In the last five decades, the semiconductor industry was mainly governed by Moore's law with a main focus on scaling IC component geometry gradually down to the nanoscale. Moore's law is mainly about cost reduction, and the economic aspect resulted in electronics widespread. Recently, the downscaling of the planar bulk MOSFET has reached fundamental limits, and new materials and architectures have been developed to overcome SCEs and drain-induced barrier lowering (DIBL).

12.2.1 From Bulk MOSFETs to UTBB FDSOI

In order to increase the gate control over the channel, high-k materials were introduced since 45 nm technology node. This has enhanced the gate capacitance without increasing the tunneling leakage [5]. Additionally, the mobility degradation due to scattering in the channel has been partially compensated by means of mobility enhancement in strained channels [6, 7].

Initially developed for its radiation hardness properties, the SOI technology is one of the first identified solutions to extend Moore's law for MOSFETs [8]. In SOI technology, a silicon layer is used on top of an insulator layer which is in turn put on top of a Si substrate. This layered planar architecture improves performance by considerably reducing parasitic capacitances and reduces power consumption. Thanks to a complete isolation from the substrate, SOI MOSFETs are inherently latch-up resistant. Depending on the thickness of the silicon film on top of the buried oxide layer, two SOI device categories can be defined: the partially depleted SOI with thick silicon film and the fully depleted SOI with thin silicon film. In the partially depleted SOI, only the top part of the silicon film is depleted, while the bottom part is neutral which is commonly called floating body (FB). The FB is causing severe kinks in the output characteristics of the MOSFET, and the partially depleted region is too sensitive to the source and the drain voltage variations. In order to mitigate the FB effects, the silicon film has been thinned down in the fully depleted MOSFET so that the silicon film is fully depleted. A back gate is obtained by thinning the buried oxide in the UTBB FDSOI transistor and by adding an underlying ground plane (GP) underneath the BOX. With this architecture, the influence of the drain electric field on the channel is reduced as the most electrical field lines from the drain terminate on the buried GP. Figure 12.1 summarizes the architecture evolution of the planar MOSFET devices from bulk to UTBB FDSOI.

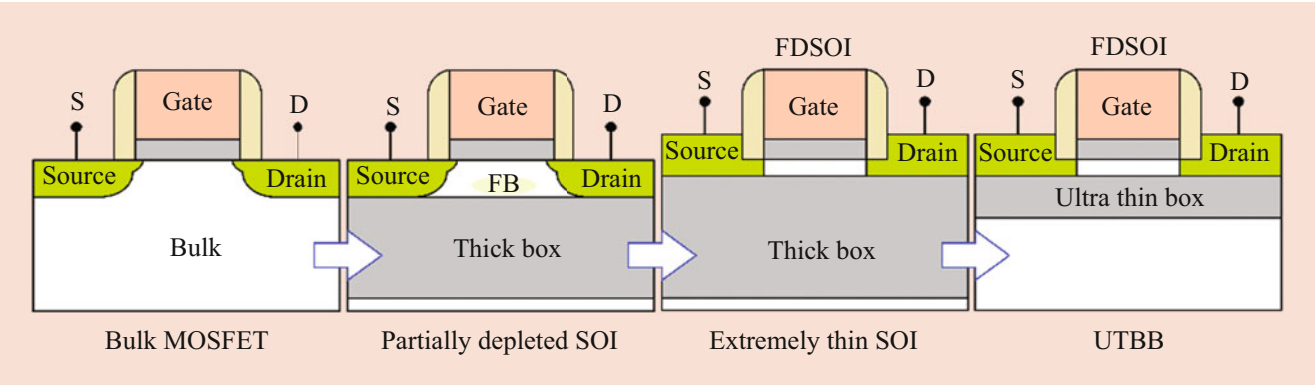


Fig. 12.1 Evolution of planar MOSFET

All enhancement techniques that were used in previous nodes hit their limit when approaching the 20 nm technology node. The mobility degradation due to scattering limited the doping concentration in the channel, and the lattice maximum stress limited the mobility enhancement in strained channels [6, 7]. With the above limitations, novel device architectures with multiple gates such as the UTBB FDSOI described above were foreseen to continue device scaling. The first published work on the double-gate MOSFET [8], shows significant SCE reduction in FDSOI MOSFETs, thanks to the bottom or back gate. With this architecture, the influence of the drain electric field on the channel is reduced. However, the first manufactured double-gate MOSFET was the fully depleted lean-channel transistor (DELTA) which is similar to FinFET but without the top hard mask [9]. The two leading technology contenders, FinFET and UTBB FDSOI, have been adopted and are in mass production today. The two basic differences between UTBB FDSOI and FinFET technologies are the gates and the channel orientation and the two gates' connection. FinFET is basically a 3-D vertical double-gate in which the two gates are connected together. However, in a UTBB FDSOI MOSFET, the two gates are not connected and can be biased differently. Otherwise, FinFET and UTBB FDSOI look the same as depicted in Fig. 12.2.

Other MOSFET architectures were also proposed such as silicon-on-nothing (SON) [10], the tri-gate FET [11], and the gate-all-around FET [12]. The choice of the architecture depends on several criteria, notably the manufacturing complexity and cost, the targeted type of applications and markets, the circuit portability from previous technologies, the circuit area, and the impact of the intrinsic parasitic elements. For instance, in the applications taking advantage of a bias controlled threshold voltage for power control, the independent gate architectures such as UTBB FDSOI are preferred.

Thanks to a thin silicon body, all aforementioned architectures can be fully depleted and consequently have very strong potential for both digital and analog applications [13, 14]. This chapter will focus on the UTBB FDSOI technology solution where the channel(s) mainly lays horizontally.

The UTBB FDSOI MOSFET is considered as a planar low-cost and a straightforward solution to continue shrinking the complementary metal-oxide-semiconductor (CMOS) transistor for low-power and high-speed very-large-scale integration (VLSI) circuits [15]. The advantages of the UTBB FDSOI MOSFETs include steep subthreshold slope (close to the room temperature Boltzmann limit of 60 mV/dec for long channels), thanks to the better control of the channel potential [16], lower DIBL (Fig. 12.3a), low channel doping, and excellent control of short-channel effects (SCE). With a steep subthreshold slope, lower threshold voltages and OFF current are obtained in comparison to bulk. Another considerable advantage of the UTBB FDSOI for design is the fact that same bulk technology design flows are applicable as both technologies are planar [15]. Buried oxide isolation is known to give birth to temperature increase because of self-heating effect [17]; however, thanks to a thinner BOX in the UTBB FDSOI, thermal effects' influence on device parameters is limited in comparison with standard SOI [18]. Similar to SOI devices, UTBB FDSOI MOSFET displays excellent radiation hardness to the detrimental alpha particles, neutrons, and other particles that generate electron-hole pairs after Si penetration [19].

While UTBB FDSOI can provide comparable digital performances with tri-dimensional FinFET [20], the RF behavior of FinFET is however affected by larger parasitic

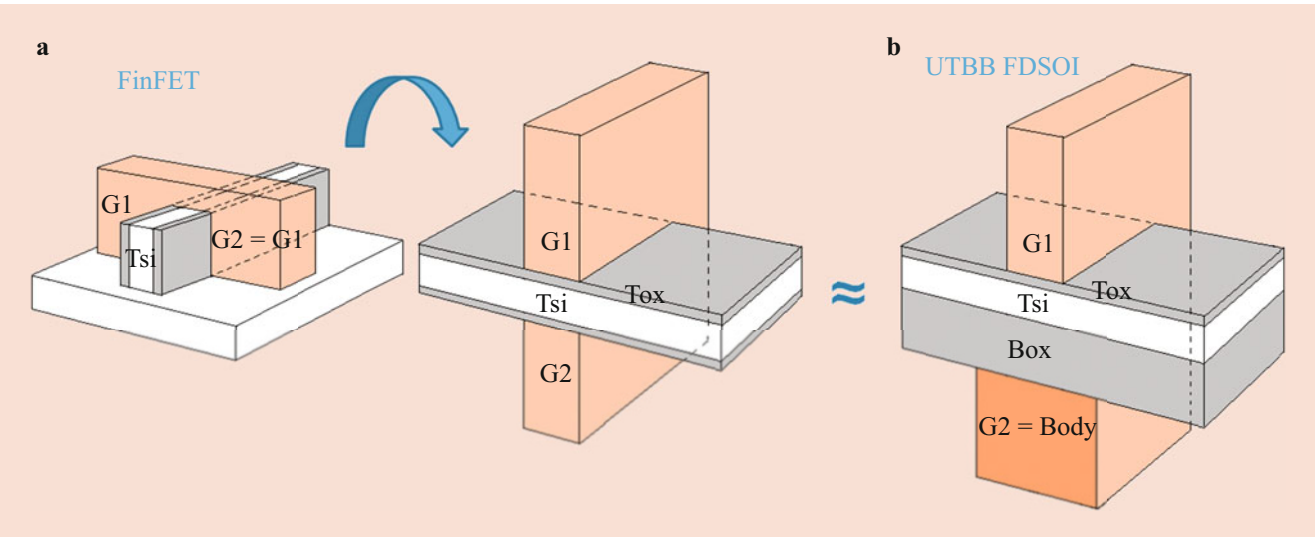


Fig. 12.2 FinFET (**a**) and UTBB FDSOI (**b**) similarity

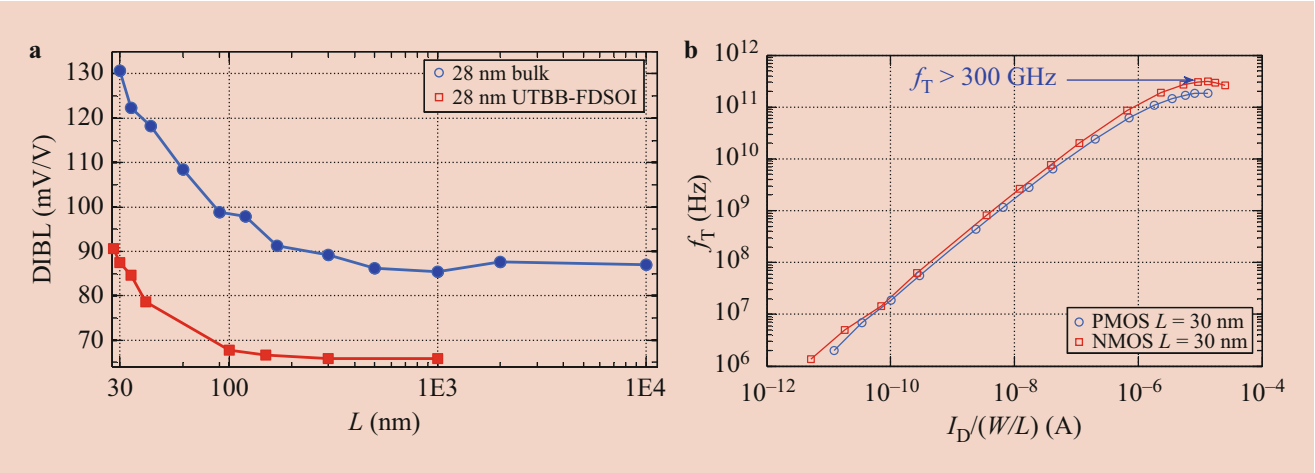


Fig. 12.3 (**a**) Comparison of DIBL between FDSOI and bulk 28 nm technology nodes in saturation ($V_{DS} = 1$ V) and $V_{bG} = 0$ V. (**b**) Measured f_T versus normalized drain current $I_D/(W/L)$ for FDSOI NMOS and PMOS ($L = 30$ nm)

elements [21–24]. The benchmarking of the transit frequency f_T for various state-of-the-art MOSFETs shows that UTBB FDSOI presents higher f_T versus FinFET, thanks to the reduced parasitic resistance and capacitance elements [24]. Moreover, the ITRS (International Technology Roadmap for Semiconductors) expectations are meet by UTBB FDSOI and confirmed experimentally in Fig. 12.3b for NMOS and PMOS devices.

12.2.2 Analog and Digital Design Needs

Circuit simulation using electronic design automation (EDA) tools is essential for IC design. Prototyping and debugging a circuit before the first hardware prototype is undeniably the most cost-effective way of achieving a first-cut design. Therefore, one of the main designer's needs to successfully complete the design is accurate simulations during the final step of verification over process, voltage, and temperature variations. Obviously, the accuracy of these simulations depends on the accuracy of the MOSFET models involved.

The MOSFET models fall into two well-defined categories according to the role in the design flow. The first category is composed of highly accurate, scalable, and continuous compact models suitable for SPICE simulations. The electrical SPICE compact model serves as a bridge between process and circuit design. It is a compact mathematical description of the complex device physics with a trade-off between accuracy and calculation efficiency, but also continuity and numerical robustness as required by SPICE simulators. Compact models are physically based and allow to predict circuit design behavior and performance beyond the measured data used to extract the model. Compact model simulations are nowadays systematically used for IC simulation earlier to an expensive production process. Moreover, compact models are flexible enough to describe MOSFETs fabricated in different foundries. Standard compact models go through extensive qualification within semiconductor foundries and fabless industrials that are organized into an industry consortium, namely, Compact Model Coalition (CMC) [25]. It should be noted that the valuable contributions from universities are key for innovative compact modeling solutions. Several SPICE compact model industry standards coexist, such as the threshold voltage (V_{TH})-based BSIM4 model from UC Berkeley and the surface potential-based PSP model originated from Philips and Pennsylvania State University, as far as bulk MOSFETs are concerned. For UTBB FDSOI MOSFET, several core models have been proposed such as BSIM-IMG and L-UTSOI. A practical modeling approach in the semiconductor industry is the use of sub-circuit build using passive element network on top of core MOSFET models that have been qualified for DC and low-frequency operation. The high-frequency behavior of MOSFETs is captured using additional lumped elements to end up with complex sub-circuits. Lumped elements are commonly added to each MOSFET terminal to account for high-frequency behavior (e.g., gate and substrate passive RC networks). The SPICE compact models will not be thoroughly treated in this chapter.

The chapter will rather focus on the second category of models which consists of simpler models, charts, and equivalent circuits appropriate for hand calculations. Nowadays, SPICE compact models due to the increasing complexity of the transistor physics tend to become difficult to use for both technology prospection by process engineers and device sizing by analog designers. Prior to the lengthy SPICE verifications, simple device models or charts are commonly used in order to predict circuit performance and perform preliminary circuit analysis, despite lower accuracy. Moreover, equivalent

circuits are also useful in order to gain practical insight into the contributors to the small-signal frequency behavior.

12.3 Model for Drain Current and First-Order Parameter Extraction

Modeling plays an increasingly important role in the development of integrated circuits. The accuracy of circuit simulations depends on the quality of the models used to predict the integrated devices' behavior, particularly the omnipresent MOSFET devices. Huge advances have been made in recent years to predict the electrical behavior of MOSFETs taking into account complex physical phenomena. The new miniaturized MOSFETs with novel architectures have made the modeling task more challenging.

Although the intrinsic electrostatic behaviors of the different architectures have been accurately modeled in several commercial standard models, variability and local layout effects are still important challenging issues for semiconductor foundries.

As for the single-gate MOSFET models, compact models for multiple-gate MOSFETs rely on long-channel core on the top of which various physical effects are added such as short-channel effects (SCE), mobility degradation, velocity saturation, and quantum mechanical effect (QME). The 3-D electrostatic behavior of the multiple-gate architectures is generally simplified and modeled using comparable formulations under reasonable assumptions regarding involved geometries [26]. Symmetrical architecture models have been reduced into single-gate-like formulations. Difficulties to model some architectures such as asymmetrical and independent gate MOSFETs have been reported and recently resolved [27, 28]. For instance, multiple threshold voltages and mobilities have been proposed to circumvent the complexity of multiple gate control [29]. In an asymmetric double-gate MOSFET, the resolution of Poisson equation with boundary conditions is not an easy task. Partitioning of inversion charge between source and drain is classically calculated using front interface potential in bulk. However, for asymmetric DG MOSFET where more than one interface is available, the classical way is not relevant.

Yet, the I–V characteristic in SI for multigate MOSFETs is close to the square law derived for early bulk technologies when mobility reduction, velocity saturation, and series resistance have lower impact. It should be noted that for thin silicon body such as the fins in FinFET, the series resistance is high and the current deviates from the ideal square law unless source and drain access is improved.

Even though the simple analytical models are somehow less accurate, they are extremely useful tools for circuit modeling and computer-aided design (CAD) application. These MOSFET models rely on a limited number (typically ten) of physical parameters (often called "first-order parameters"), such as the channel mobility μ, mobility degradation θ, velocity saturation v, and source and drain external resistances.

The aim of this section is to provide a set of simple equations in order to analyze the behavior of the overthreshold drain current in the linear regime but also in the saturation regime.

12.3.1 UTBB FDSOI Device Cross Section

In the UTBB FDSOI technology, MOSFET channel is formed in a thin silicon film separated from the substrate by an oxide film called buried oxide (BOX) as depicted in Fig. 12.4. In 28 nm FDSOI technology from STMicroelectronics, final silicon film is 7 nm thick, and BOX is 25 nm thick after a few process steps [2]. In contrast with the most advanced bulk transistor, the channel of the UTBB FDSOI devices is un-doped, and no pockets of counter-doping are introduced in order to enhance the electrostatic control and to limit the punch-through in the shortest devices.

Figure 12.4 shows a cross section of the device with an emphasis on the access region. This access region tends to have an increasing impact on the drain current [30]. As shown in Fig. 12.4, it is composed not only of the highly doped source and drain region itself (a) but also of the low-doped drain (LDD) region below the spacer (b). Unlike region (a), this latter overlap region (b) depends on gate voltage, and a simple model detailed in [30] can accurately describe the regions (a) and (b) as a series resistance (independent of the channel length) as:

$$R = 2 \cdot R_0 + 2 \cdot \sigma \cdot (V_G - V_{TH})^{-1} \qquad (12.1)$$

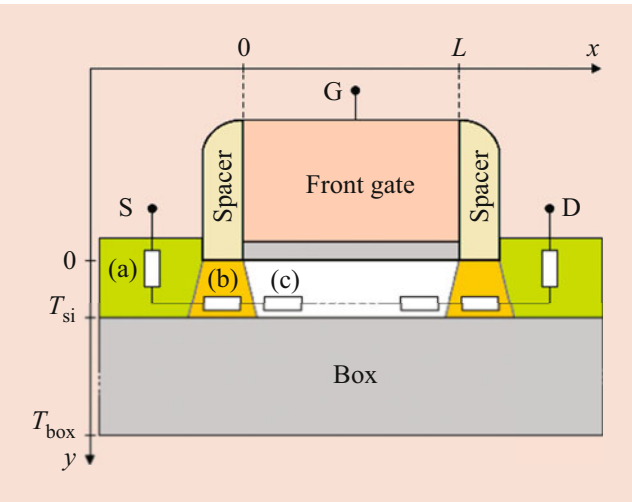


Fig. 12.4 Cross section of the UTBB FDSOI MOSFET with a lumped resistance model

where R_0 and σ are two model parameters whose extraction strategy will be described later.

12.3.2 Drain Current Model

A closed-form exact analytical drain current expression is derived from the Pao and Sah integration [31] and assuming the proportionality between the inversion charge and the gate voltage overdrive. The derived drain current model considers mobility degradation, velocity saturation, and access resistances.

Reference to the Pao and Sah Approach

Region (c) in Fig. 12.4 corresponds to the part of the device where the channel is considered to be homogenous. This part's effective length $L_{\text{eff}} = L - \Delta L$ can be either longer or shorter than the drawn gate length L depending on the source, drain, and LDD architecture. In what follows, for simplicity, we will drop the explicit reference to L_{eff} keeping in mind the meaning of this quantity. Similarly, due to access voltage drop in the (a) and (b) regions, a pseudo source voltage and a pseudo drain voltage have to be considered instead of the external applied voltages.

Above threshold voltage, the current in region (c) can be expressed using the quasi-Fermi level ϕ by:

$$I_{\text{D}} = \frac{W}{L}\int_{\text{S}}^{\text{D}} \partial x \cdot (\mu_{\text{eff}} \cdot Q_{\text{i}}) \cdot \frac{\partial \phi}{\partial x} = \frac{W}{L}\int_{\phi_{\text{s}}}^{\phi_{\text{D}}} \partial \phi \cdot (\mu_{\text{eff}} \cdot Q_{\text{i}}) \tag{12.2}$$

with L the effective channel length, W the MOSFET width, μ_{eff} the effective mobility, and Q_{i} the inversion charge. The integration along the channel direction starts at the position in the channel $x = 0$ corresponding to the pseudo source and ends at the pseudo drain corresponding to $x = L$. Within the Pao and Sah approach, the integral over x is transformed into an integral over the pseudo-Fermi levels, from source to drain. According to (12.2), one needs to express the inversion charge as a function of the gate voltage V_{G} and the channel threshold voltage V_{TH}, (12.2) being valid for $V_{\text{GT}} = (V_{\text{G}} - V_{\text{TH}}) > 0$. For bulk transistors, it is well known that the inversion charge density depends on the oxide capacitance C_{ox} as:

$$Q_{\text{i}} = C_{\text{ox}} \cdot (V_{\text{G}} - V_{\text{TH}} - \phi/A) \tag{12.3}$$

where $A = C_{\text{ox}}/(C_{\text{ox}} + C_{\text{d}}) \approx 1$ and C_{d} stands for the depletion capacitance [32]. This expression is also valid for the FDSOI with $V_{\text{bG}} \leq 0$ V (see latter) knowing that an additional inversion charge can appear when the back gate is forward biased (e.g., $V_{\text{bG}} > 0$ V) [33].

Let us first introduce the mobility degradation using the well-known empirical model [32, 34]:

$$\mu_\theta = \mu_0/(1 + |Q_{\text{i}}|/Q_{\text{c}}) = \mu_0/(1 + \theta \cdot (V_{\text{G}} - V_{\text{TH}} - \phi/A)) \tag{12.4}$$

where Q_{c} is a "critical" charge from which the mobility starts to decrease and θ is the mobility degradation parameter. It is generally more convenient to use θ instead. The non-saturated current (accounting for the mobility degradation due to vertical field) can be written as:

$$I_{\text{D0}} = \frac{\mu_0 C_{\text{ox}} W}{L}\int_{\phi_{\text{s}}}^{\phi_{\text{D}}} \partial \phi \cdot \frac{(V_{\text{G}} - V_{\text{TH}} - \phi/A)}{(1 + \theta \cdot (V_{\text{G}} - V_{\text{TH}} - \phi/A))} \tag{12.5}$$

To evaluate the current, one needs to perform the integration over the pseudo-Fermi levels. This can be done evaluating the integral [32]: $\delta = \int_{\phi_{\text{s}}}^{\phi_{\text{D}}} \partial\phi/\,(1+\theta \cdot (V_{\text{G}} - V_{\text{TH}} - \phi/A))$. Using trivial algebra, one can easily re-write the current as:

$$I_{\text{D0}} = \frac{\mu_0 C_{\text{ox}} W}{L} \cdot \frac{V_{\text{DS}}\,(1 - \delta/V_{\text{DS}})}{\theta} \tag{12.6}$$

with $\delta = \frac{A}{\theta} \ln\left[\frac{1+\theta \cdot (V_{\text{G}} - V_{\text{TH}} - V_{\text{S}}/A)}{1+\theta \cdot (V_{\text{G}} - V_{\text{TH}} - V_{\text{D}}/A)}\right]$.

Let us now introduce the saturation velocity in the mobility as:

$$\mu_{\text{eff}} = \mu_\theta / \left(1 + \frac{\mu_\theta}{v^*} \cdot \frac{\partial \phi}{\partial x}\right) \tag{12.7}$$

Using the electrostatic potential ψ and the approximation $F_x = \frac{\partial \psi}{\partial x} \approx \frac{\partial \phi}{\partial x}$, which is well justified in the drift regime, the current writes:

$$I_{\text{D}} = \frac{W}{L}\int_0^{\text{L}} \partial y \frac{\mu_0 C_{\text{ox}} \cdot (V_{\text{G}} - V_{\text{TH}} - \phi/A) \cdot \frac{\partial \phi}{\partial y}}{(1 + \theta \cdot (V_{\text{G}} - V_{\text{TH}} - \phi/A)) \cdot \left(1 + \frac{\mu}{v^*} \cdot \frac{\partial \phi}{\partial y}\right)} \tag{12.8}$$

which implies that:

$$\begin{aligned} &\frac{W}{L}\int_0^L \partial x \cdot I_{\text{D}} \cdot \left(1 + \frac{\mu}{v^*} \cdot \frac{\partial \phi}{\partial x}\right) \\ &\quad = \frac{W}{L}\int_0^L \partial x \cdot \frac{\mu_0 C_{\text{ox}} \cdot (V_{\text{G}} - V_{\text{TH}} - \phi/A) \cdot \frac{\partial \phi}{\partial x}}{(1 + \theta \cdot (V_{\text{G}} - V_{\text{TH}} - \phi/A))} \end{aligned} \tag{12.9}$$

and finally using (12.6):

$$I_{\text{D}} = \frac{I_{\text{D0}}}{\left(1 + \frac{\mu_0}{v^* L}\delta\right)} \tag{12.10}$$

Equation (12.10) is valid below saturation voltage, the value of which can be obtained when the derivative vs V_{DS}

of the current is zero. This can be done analytically for I_{D0}, and it can be shown that whatever the degradation parameter is, the saturation drain voltage is $V_{DSAT} = A.(V_G - V_{TH})$. Some more complex analytical models for V_{DSAT} accounting for the velocity saturation can be found in [32, 35]. However, the general case considering, mobility degradation, velocity saturation, and source and drain resistances are subtler, and in what follows, V_{DSAT} is obtained from the derivative of the drain current which must be done numerically and self-consistently since the voltage drops in the drain and the source resistances also depend on the current.

Saturation Drain Voltage

Figure 12.5 shows that V_{DSAT} as a function of the channel length can increase significantly when series resistances and saturation velocity are accounted for unlike the long-channel case in which $V_{DSAT} = (V_G - V_{TH})$. The behavior is more pronounced at high V_G where drain current is important. The trend can be inversed due to saturation velocity. In that case, neglecting the series resistances, the saturation voltage tends to be zero in the shortest devices [35]. In a more realistic case, when both saturation velocity and external resistances are accounted for, the decrease of V_{DSAT} observed in the shortest devices (due to the saturation velocity) tends to be compensated by the impact of the external resistances, and V_{DSAT} remains closer to $V_G - V_{TH}$ for all channel lengths.

R_{on}-L Model

The drain current expressed with (12.10) is still quite complex, and some simplifications are welcome. The linear regime without external resistance can be simplified as (assuming also $A = 1$):

$$I_D \cdot \frac{L}{W} = \frac{C_{OX} \cdot \mu_0}{(1 + \theta \cdot (V_{GS} - V_{TH} - V_{DS}/2))} (V_{GS} - V_{TH} - V_{DS}/2) \cdot V_{DS} \tag{12.11}$$

Similarly, with the external resistance R, the current writes [32]:

$$I_D = \frac{W}{L} \frac{C_{OX} \cdot \mu_0 \cdot (V_{GS} - V_{TH} - V_{DS}/2) \cdot V_{DS}}{\left(1 + \left(\theta + \frac{R \cdot C_{OX} \cdot \mu_0}{L}\right) \cdot (V_{GS} - V_{TH} - V_{DS}/2)\right)} \tag{12.12}$$

In other words, the resistance can be seen "internally" as a supplementary contribution to the effective mobility degradation parameter.

A simple account for the velocity saturation consists in using the same derivation as in (12.10) (with $\theta = 0$):

$$I_D = \frac{I_{v*=\inf}}{\left(1 + \frac{\mu_0}{v^* L} V_{DS}\right)} \tag{12.13}$$

Additional complexity can be added considering the mobility degradation and recasting the series resistances into θ:

$$I_D = \frac{\frac{W}{L} \frac{C_{OX} \cdot \mu_0 \cdot (V_{GS} - V_{TH} - V_{DS}/2) \cdot V_{DS}}{\left(1 + \left(\theta + \frac{R \cdot C_{OX} \cdot \mu_0}{L}\right) \cdot (V_{GS} - V_{TH} - V_{DS}/2)\right)}}{\left(1 + \frac{\mu_0 \cdot V_{DS}}{v^* L \cdot \left(1 + \left(\theta + \frac{R \cdot C_{OX} \cdot \mu_0}{L}\right) \cdot (V_{GS} - V_{TH} - V_{DS}/2)\right)}\right)} \tag{12.14}$$

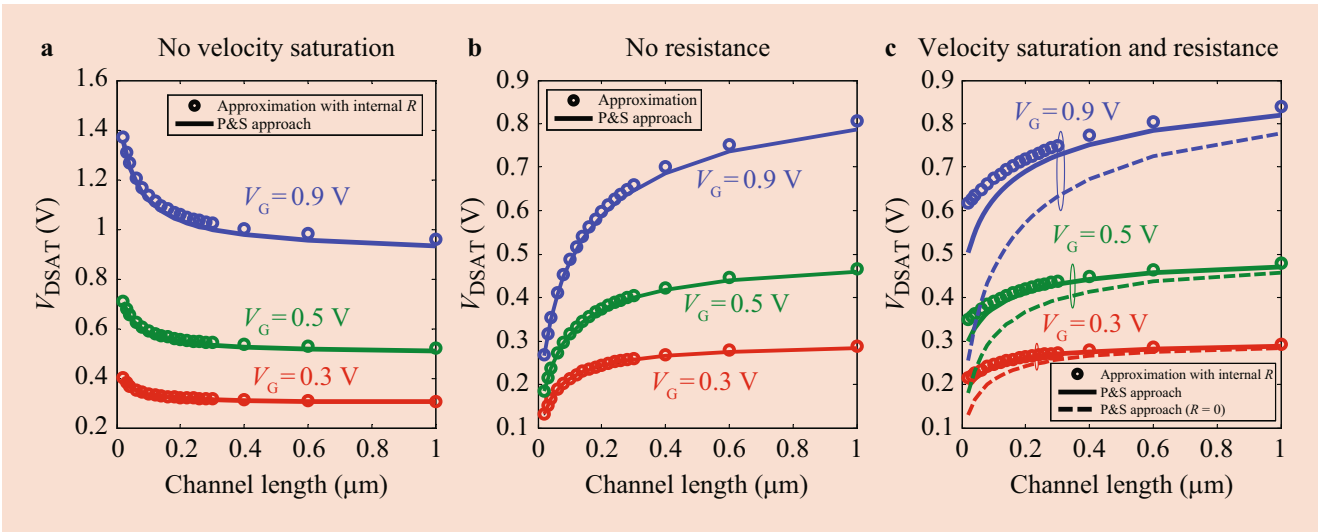


Fig. 12.5 Simulation of the saturation voltage for various V_G (considering for simplicity $V_{TH} = 0$). (**a**) Impact of the series resistances with $R = 100\ \Omega$, (**b**) impact of the velocity saturation with $v = 1e5$ m.s^{-1}, and (**c**) impact of both velocity saturation and series resistance ($v = 1e5$ m.s^{-1}, $R = 100\ \Omega.\mu m$). Solid line: Pao and Sah-based model in (12.10) with $C_{OX} = 0.025$ F.m^{-2}, $\mu_0 = 0.04$ m^2/(V.s), $\sigma = 0\ \Omega.\mu m.V$, and $\theta = 0.15$ V^{-1}. Symbol: a simplified model where series resistance effect is treated as an additional mobility degradation (cf. (12.12))

The saturation drain voltage obtained from the derivative of the drain current vs V_{DS} is shown in Fig. 12.5.

Equation (12.14) allows us to compute the device resistance R_{on} from the inverse of the current and using (12.1) in an explicit and useful way:

$$R_{LIN} = L \cdot \left\{ \frac{1}{\mu_0 C_{OX} (V_{GS} - V_{TH})} + \frac{\theta}{\mu_0 C_{OX}} \right\} + \frac{1}{(V_{GS} - V_{TH})} \cdot \left\{ 2 \cdot \sigma + \frac{V_{DS}}{v^* C_{OX}} \right\} + 2 \cdot R_0 \tag{12.15}$$

As mentioned previously, the simplification consisting in using $V_{DSAT} = V_G - V_{TH}$ is reasonable in practice over a large range of channel lengths and in the saturation regime R_{SAT} writes:

$$R_{SAT} = L \cdot \left\{ \frac{2 \cdot V_{DS}}{\mu_0 C_{OX} (V_{GS} - V_{TH}) \cdot (V_{GS} - V_{TH})} + \frac{\theta \cdot V_{DS}}{\mu_0 C_{OX} \cdot (V_{GS} - V_{TH})} \right\} + \frac{2 \cdot V_{DS}}{(V_G - V_{TH})} \cdot \left\{ \frac{\sigma}{V_{GS} - V_{TH}} + \frac{1}{v^* C_{OX}} \right\} + 2 \cdot R_0 \cdot \frac{V_{DS}}{V_{GS} - V_{TH}} \tag{12.16}$$

Figure 12.6 compares the R_{on} in the linear and saturation regimes calculated using various models. One can notice differences between the predictions of the model using "internal" or "external" resistance. In fact, the approximation consisting in recasting the series resistances into θ can lead to unphysical results since in that case Kirchhoff's law is not satisfied at the source and drain nodes. One notes that this can be even more pronounced in the linear regime due to the presence of the V_{DS} term in the denominator (assuming v^* is not zero).

Despite their simplicity, Eqs. (12.15) and (12.16) allow a useful breakdown of the total resistance splitting the L-dependencies and the V_G-dependencies. Based on these equations, a direct extraction of the first-order model parameters is in principle possible from simple current measurements at various $V_G - V_{TH}$ overdrives. In particular, an effective access resistance can be extracted from the $R_{on} - L$ curve intersect with the Y-axis, while the intrinsic "channel" current and the mobility parameters can be obtained from its slope.

12.3.3 Parameter Extraction from Measurements

The proposed drain current and R_{on} models allow a straightforward extraction of the main physical ingredients, namely, the threshold voltage, the mobility degradation parameter, the access resistance, and the saturation velocity.

The Threshold Voltage Extraction

The determination of threshold voltage from measurements has a long history, and several conflicting definitions and extraction methods are proposed in the literature [36]. In the first series of methods, the threshold voltage is rather a fitting parameter that will depend on the chosen model for the linear and the saturation regimes. Alternatively, the threshold voltage can be extracted from the gate voltage corresponding to the maximum of the gate capacitance derivative. As explained in [37], we have the following relation:

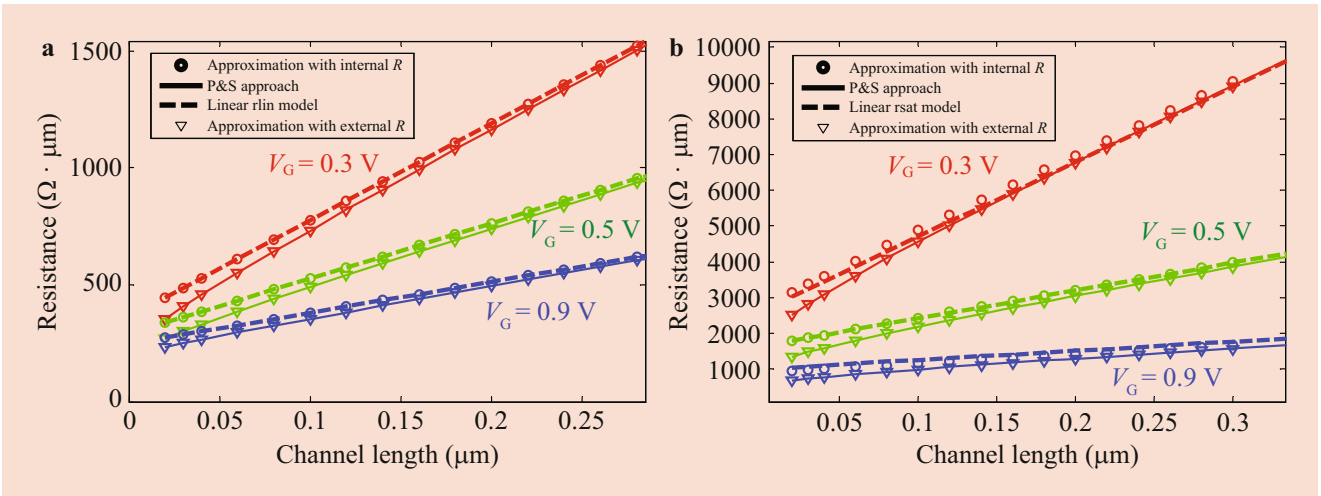


Fig. 12.6 Device resistance R_{on} in the linear ((**a**): $V_{DS} = 0.05$ V) and saturation regimes ((**b**): $V_{DS} = 0.9$ V) for various V_G (considering for simplicity $V_{TH} = 0$). Model described in the text with $C_{OX} = 0.025$ F.m^{-2}, $\mu_0 = 0.04$ m^2/(V.s), $\theta = 0.15$ V^{-1}, $R = 100$ Ω.µm, and $v = 1e5$ m.s^{-1}

$$C_{gc} \equiv \frac{\partial Q_{inv}}{\partial V_{GS}} = \frac{\partial \left(C_{ox} \cdot V_{ox}\right)}{\partial V_{GS}} = C_{ox}\frac{\partial V_{ox}}{\partial V_{GS}} = C_{ox}\frac{\partial \left(V_{GS} - \Psi_s\right)}{\partial V_{GS}} = C_{ox}\left(1 - \frac{\partial \Psi_s}{\partial V_{GS}}\right) \tag{12.17}$$

where Q_{inv}, C_{ox}, V_{ox}, and ψ_s are, respectively, the inversion charge, the oxide capacitance, the oxide voltage drop, and the surface potential. If we derive (12.17) with respect to V_{GS}, we get:

$$\frac{\partial C_{gc}}{\partial V_{GS}} = -C_{ox}\frac{\partial^2 \Psi_s}{\partial V_{GS}^2} \tag{12.18}$$

This quantity maximizes at the inflection point of the surface potential plot with respect to V_{GS} and corresponds to the inversion charge rise.

One other direct extraction of the threshold voltage, which provides comparable results to the *C-V* derivative, is the g_m/I_D derivative method proposed in [38]. The agreement between the two aforementioned methods in bulk is explained using:

$$\frac{\partial \left(\frac{g_m}{I_D}\right)}{\partial V_{GS}} = \frac{1}{U_T}\frac{\partial^2 \Psi_s}{\partial V_{GS}^2} \tag{12.19}$$

In bulk, the g_m/I_D derivative is proportional to the quantity expressed in (12.18) and also determines the inversion charge rise when maximized. It can be noted that in FDSOI devices in which the charge is composed of front and back inversion charges (see latter), some slight discrepancies between these two latter methods can exist.

In Fig. 12.7, the *Y*-function-based, the H-function-based, and the normalized reciprocal H-function (NRH)-based methods [36] are compared to the g_m/I_D derivative-based method for several FDSOI MOSFET lengths. The several methods provide different values in particular for short channels in saturation regime. Thus, inversion level metric based on threshold voltage concept (e.g., gate voltage overdrive $V_{GT} = V_{GS} - V_{TH}$) can be inaccurate as being closely tied to the threshold voltage extraction method.

The Apparent Channel Mobility Degradation and the Access Resistance

The finite number of available sub-bands carrying the current puts a lower fundamental limit to the total drain current. Even in the absence of contact and spreading resistances, the intersect of the R_{ON} (L) plot for $L = 0$ exhibits a finite value, which is often referred to as quantum or "ballistic" resistance [30, 39–44]. The quantum resistance, the value of which does not significantly change with the channel thickness, acts as a series resistance and can be expressed as:

$$R_Q \approx \sqrt{2\pi \cdot m \cdot kT}/\left(q \cdot C_{ox} \cdot \left(V_{GS} - V_{TH}\right)\right) = 2 \cdot \sigma_B \cdot \left(V_{GS} - V_{TH}\right)^{-1} \tag{12.20}$$

with $\sigma_B \approx 8.4$ in silicon N-type MOSFETs. In realistic silicon MOSFETs, featuring spacers and S/D regions, the impact of the quantum resistance on the drain current is nevertheless relatively small. This is shown in Fig. 12.8a–c in which the extracted series resistance values are more than four times larger than the theoretical quantum resistance ones. As shown in [30], the near-spacer/LDD region exhibits a large resistance (that does not depend on L and therefore can be considered as a series resistance in the lumped elements model in Fig. 12.4). We found out that the "apparent" mobility degradation observed in short devices can be inferred from the impact of this V_G-dependent resistance on the device current. The "apparent" channel length dependency of the mobility in nanometric devices has been long discussed [39–45], and some additional scattering mechanisms localized near the LDD junction have been suspected to give rise to an "average" decrease of the mobility (considered as a model parameter) in the shortest devices. We believe that systematic errors in the characterization procedures may also be at the origin of this "apparent" decrease of the mobility.

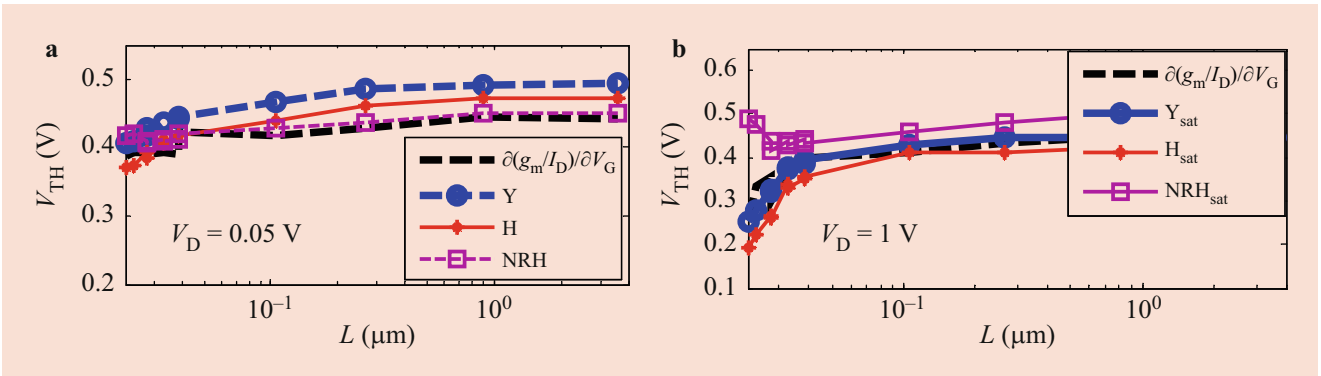


Fig. 12.7 Threshold voltage versus length for NFDSOI devices in linear (V_{DS} = 50 mV) and saturation (V_{DS} = 1 V)

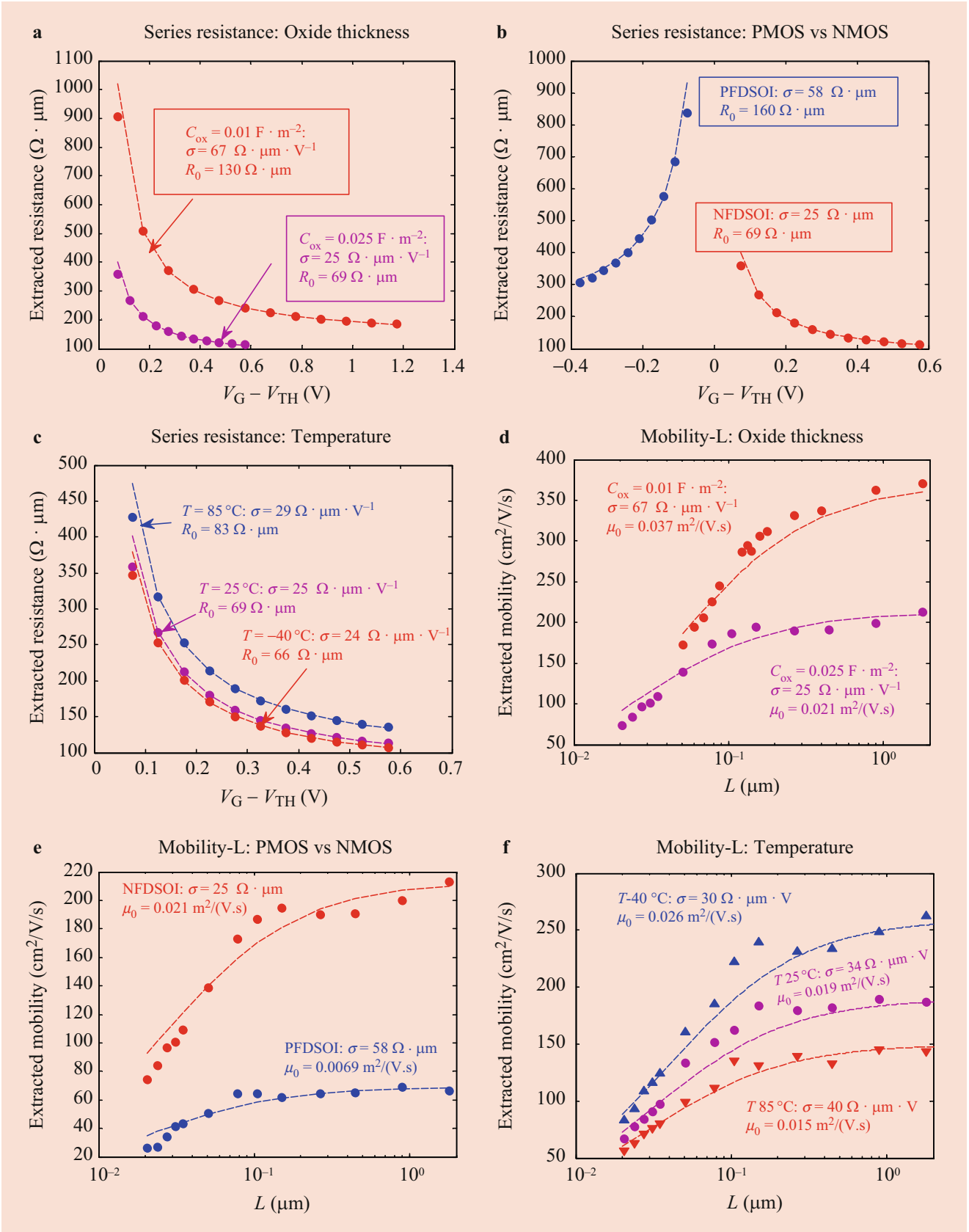


Fig. 12.8 (continued)

In the shortest device, series resistances significantly reduce the drain current, even in the linear regime. Series resistance extraction methods have been extensively discussed in literature [41, 43]. We reported in [30] that the usage of the Y-function [41] can introduce large errors when the resistances are extracted from R_{ON} $(1/\beta_{eff})$ plots. With some algebra, it can be proven that in the linear regime (and considering $L_{eff} = L$), the inverse of the gain factor $\beta_{eff} = \mu_{eff} \cdot C_{ox} \cdot W/L$ extracted from the slope of the Y-function $Y = I_D/\sqrt{g_m} \approx \sqrt{(\beta_{eff}. V_{DS})} \cdot (V_G - V_{TH})$ writes $1/\beta_{eff} = 1/(\mu_0 \cdot C_{ox}. W) \cdot L + 2 \cdot \sigma/W$, where μ_0 is the long-channel mobility. This implies that the extracted effective mobility μ_{eff} becomes L-dependent as $\frac{1}{\mu_{eff}} = \frac{1}{\mu_0} + 2 \cdot \sigma \cdot C_{ox}/L$. The coefficient σ can be significantly larger than σ_B because of the V_G-dependent part of the access resistance. This is shown in Fig. 12.8a–c reporting the series resistance extracted using the $R_{ON}(L)$ intersect with the Y-axis. Also shown is the mobility extracted from Y-function [41]. It can be noted that the apparent mobility degradation is correctly modeled using the σ value extracted from $R_{acc} - V_{GT}$ (please notice that for simplicity, we did not distinguish here the LDD-related threshold voltage from the channel one V_{TH}).

The Pinch-OFF and the Velocity Saturation

Figure 12.9 shows the experimental R_{on}-L together with a linear R_{on}-L model fit in N-type FDSOI MOSFET device at $V_{DS} = 0.05$ V and $V_{DS} = 1$ V for various temperatures. As already mentioned, the channel length corresponds to the gate length L corrected by a small offset ($L_{eff} = L - \Delta L$) [40]. In the most advanced industrial technological nodes, where the channel length is aggressively scaled, the device source and drain architecture is optimized in order to reduce ΔL as much as possible (typically $\Delta L < 1$ nm).

As can be seen, the extracted resistance exhibits a nearly linear behavior versus effective channel length. The observed deviations from the linear model (in particular at high temperature in the saturation regime) can have several origins. This can come from the simplified model for $V_{DSAT} = V_{GT}$ that we have shown to be accurate for long devices only. Additionally, the accuracy of the extracted resistance depends on the gate voltage overdrive accuracy that must be carefully controlled (i.e., the accuracy of the threshold voltage extraction).

In recent technologies, the linear R_{on}-L model shown in Fig. 12.9 seems to be rather a good approximation and has been applied with a relatively good accuracy in P-type FDOSI MOSFET, in thick and thin oxide technologies (see, e.g., Fig. 12.8), but also in 28 nm bulk transistors featuring no pocket implants. However, we would like to mention that the carrier transport has been considered homogeneous along the channel. This is well verified in, e.g., 28 nm UTBB FDSOI devices, but can be untrue in 20 nm UTBB FDSOI technological nodes featuring, e.g., source and drain stressors whose impacts are more pronounced in the shortest devices [20].

Figure 12.10a shows the experimental access resistance extracted from the R_{on}-L Y-axis intercept at V_{DS}=0.05 V and $V_{DS} = 1$ V. A model $\frac{\sigma_{eff}}{(V_G - V_{TH})}$ allows a good fitting of the measurements. According to (12.16), the extracted value of the V_G-dependent part of the access resistance that increases with temperature can be approximated at high gate voltage overdrive by $\sigma_{eff} \approx V_{DS} \cdot \left\{R_0 + \frac{1}{v^* C_{OX}}\right\}$. Considering that the contribution R_0 (extracted using the Y-function method) only varies by 30% on the considered temperature range, this suggests that v^* decreases with temperature.

To gain more insight into the drain current, we can use Eqs. (12.15) and (12.16) and extract from the R_{on}-L slope that can be referred to as the "channel" contribution to the resistance. Figure 12.10b shows this quantity at $V_{DS} = 0.05$ V and $V_{DS} = 1$ V for various temperatures. The "channel" resistance of the short device is compared to the total resistance of the long device. This figure tends to show that the short device current "de-embedded" from its access resistances exhibit the same quadratic V_G-dependent resistance than the long-channel one (in which the access resistances have a much lower impact). We believe that this constitutes an evidence of the fact that the short-channel device is in pinch-off regime in agreement with the measurement of drain current with negative drain voltage showing no saturation of the total current [45].

12.3.4 Do We Need a Quantum Approach for Ultimate Silicon-Based UTBB FDSOI?

Non-equilibrium Green function (NEGF)-based simulations [30] have been performed on 28 nm FDSOI devices, with a view to comparing the results to the classical P&S approach. Figure 12.11a shows the structure as obtained from TCAD (technology computer-aided design) process simulation. NEGF structures have been obtained randomizing the dopant distribution and the interfaces. Figure 12.11b, c shows the charge densities and the quasi-Fermi levels (calculations from the NEGF density are obtained from a fit of a heated

Fig. 12.8 (**a**) to (**c**) Extracted series resistance from R_{on}-L Y-axis intersect. Lines show best fit with a model: $\sigma . V_{GT}{}^{-1} + R_0$. (**d**) to (**f**) Extracted mobility using the Y-function compared to model predictions (see text for details). Measurements in the linear regime ($|V_{DS}| = 0.05$ V) in N-type FDSOI MOSFETs featuring various oxide thicknesses, in N- and P-type MOSFETs, and in N-type FDSOI MOSFET at various temperatures

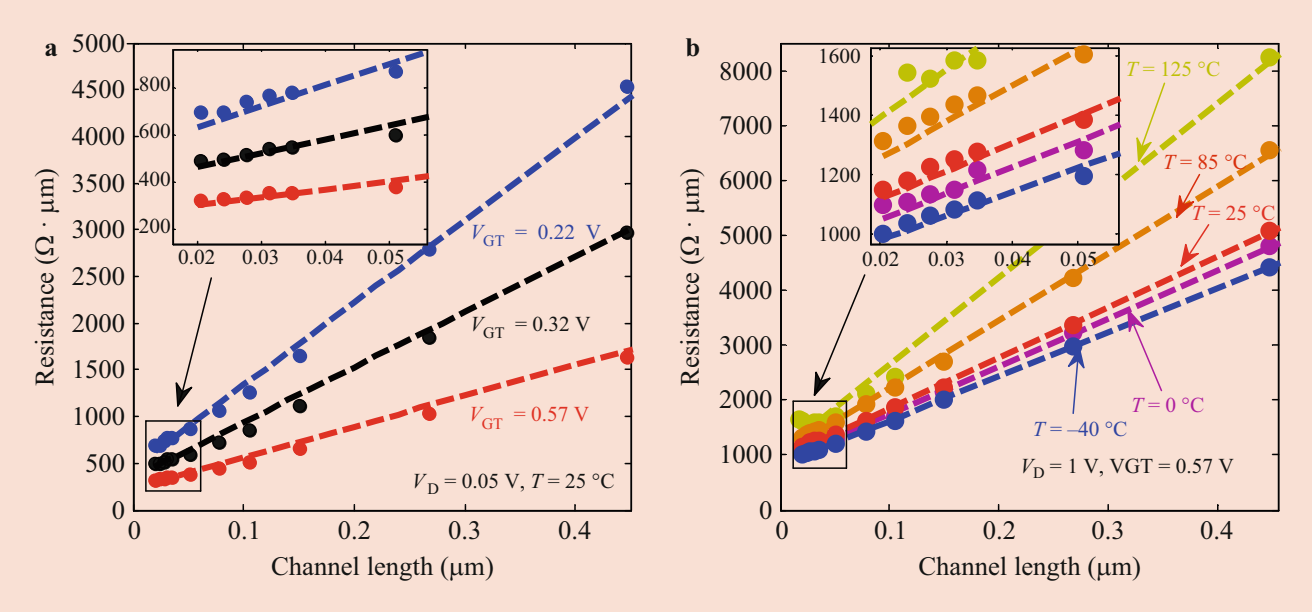


Fig. 12.9 Experimental R_{on}-L and model predictions in the linear (**a**) and saturation (**b**) regimes in a thin oxide FDSOI device: $C_{OX} = 0.025$ F.m^{-2}; $\mu_0 = 0.023$ m^2/(V.s); $\theta = 0.07$ V^{-1}; $R = 50$ Ω.μm; $\sigma = 35$ Ω.μm.V; $\nu = 2.3$e5 m.s^{-1}

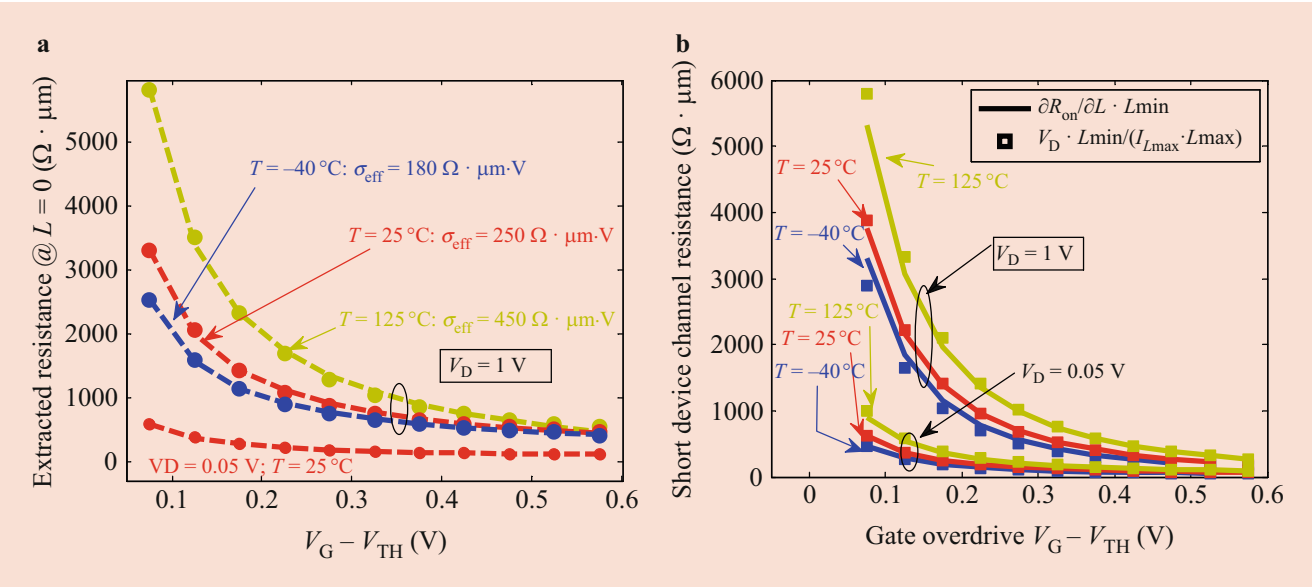


Fig. 12.10 (**a**) Experimental access resistance at $V_{DS} = 0.05$ V and $V_{DS} = 1$ V. (**b**) Experimental channel resistance extracted from the R_{on}-L slope at $V_{DS} = 0.05$ V and $V_{DS} = 1$ V (see text for details)

Maxwellian carrier distribution). It can be noticed that despite some statistical oscillations originated from the random placement of the dopant atoms and the surface roughness, a significant quasi-Fermi level drop in the near-LDD region is observable, while the channel operates in a diffusive regime as testified by the nearly linear voltage drop occurring in this region. Also shown are the computationally less demanding TCAD device simulations within the hydrodynamics approach (see [30] for details).

Figure 12.12 compares R_{on}-L (a) and its interest at $L = 0$ (b) obtained from NEGF. As expected, NEGF results depend on the models and approximations during the simulation. NEGF simulations are performed considering scattering with phonon only including or not the additional scattering mechanisms: surface roughness and remote Coulomb in the high-K gate stack. Additionally, simulations have been performed within the effective mass approximation (EMA) and the two bands' k.p model (featuring non-parabolic band structures).

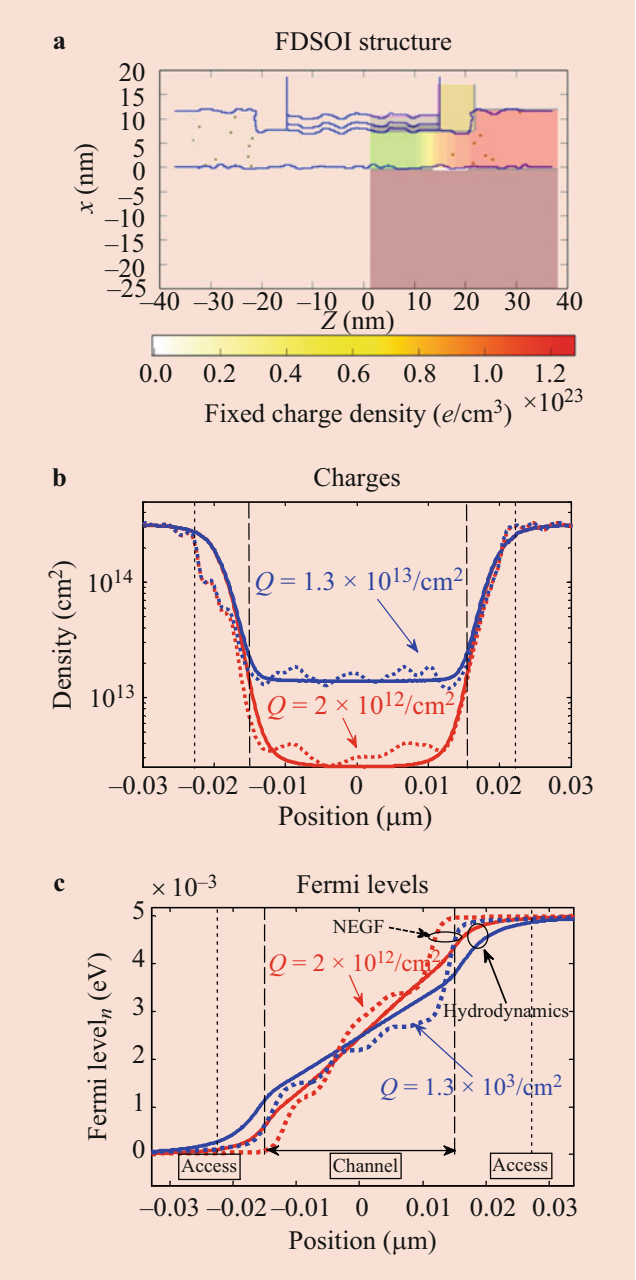


Fig. 12.11 Simplified FDSOI structure (**a**) featuring SiON/HfO2/metal gate with remote Coulomb interfacial charges (QHK = 3e13/cm^2), surface roughness, and discrete LDD dopants. NEGF (dashed) compared to density-gradient-corrected hydrodynamics-based simulations. (**b**) Inversion charges 1.3e13/cm^2 and 2e12/cm^2. (**c**) Quasi-Fermi levels calculated along the channel

We can see in Fig. 12.12 that the mobility μ_0 (as extracted from the R_{on}-L slope) and the σ value (best fit using (12.20)) largely depend on the choice of the models used during the NEGF simulation.

Figure 12.13 compares R_{on}-L predictions using the classical P&S to the NEGF results. The relatively large value of the velocity saturation used in the models can be inferred from the approximations used in the NEGF simulations (EMA and phonon only) which tends to overestimate the velocity saturation.

The classical P&S approach results compare well with the NEGF results, even in the saturation regime. We believe that, in a certain way, for a certain usage, the classical models are able to account for the observed and simulated overthreshold currents in UTBB FDSOI devices. However, some discrepancies can remain and are inevitable. In particular, discrepancy can come from the fact that we have considered the saturation velocity to be constant vs channel length. Saturation velocity overshoot phenomena have been highlighted in a theoretical viewpoint, and experimental results [41] tend to suggest that v^* increases by up to 50% in the shortest devices. Alternatively to classical approaches, the quantum approaches [46, 47] have pointed out that for the shortest devices, one may need quasi-ballistic models. In that case, the current can be expressed at the virtual source injection point, and the saturation of the velocity v^* is interpreted as an "injection" thermal velocity $v_T \approx \sqrt{2 \cdot kT/(\pi \cdot m)} \approx 1.2 \times 10^5$ m/s whose value is close to the saturation velocity in silicon [47]. Although such drain current models lead to similar current equations in saturation, the temperature dependence is different. Indeed, the thermal velocity is expected to increase with temperature, while the saturation velocity is expected to decrease with temperature (as suggested in Fig. 12.10).

12.3.5 Back Biased UTBB FDSOI MOSFET

One major advantage UTBB FDSOI has in comparison to bulk technology is the possibility to control the threshold voltage (V_{TH}) using the back-gate bias voltage as shown in Fig. 12.14 for both N- and P-type MOSFETs with a coupling factor of $\frac{C_{BOX}}{C_{OX}} \sim$ 70–100 mV/1 V for BOX thicknesses of 20–25 nm. The parasitic substrate coupling is avoided in the UTBB FDSOI by the introduction of the ground plane which is a highly doped region underneath the thin BOX [48]. This highly doped layer underneath the BOX opens various possibilities to tune the device threshold voltage (V_{TH}) [49] and extends the usage of the MOSFET back-gate biasing V_{bG} to dynamically optimize the power consumption [50].

Figure 12.15a shows the measured drain current for N-type MOSFET versus the front-gate voltage V_{GS} for various back-gate voltages V_{bG}. The transfer characteristic I_D–V_{GS} significantly shifts toward lower or higher V_{GS} value, but the subthreshold slope is nearly unchanged (cf. Sect. 12.4.2). The increase of V_{bG} is commonly called forward back biasing (FBB), and lowering V_{bG} is called reverse back biasing (RBB). It should be noted that, thanks to a ~25-nm-thick buried oxide, high voltages can be applied to the back gate (typically –10 V to 10 V range without stressing the buried oxide). Figure 12.15b shows the measured front-gate

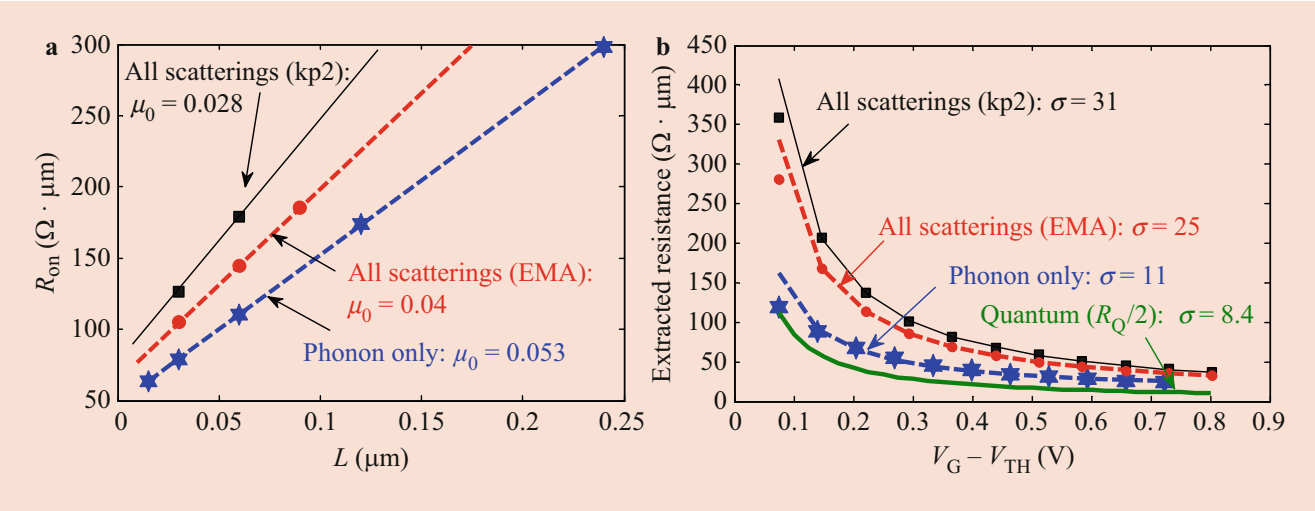


Fig. 12.12 (**a**) Device resistance R_{on} in the linear regime ($V_{DS} = 0.001$ V) for $V_{GT} = 0.8$ V, simulated using various approximations (see text for details). (**b**) Extracted series resistance from R_{on}-LY-axis intersect. Lines show best fit with a model: $\sigma.V_{GT}{}^{-1} + R_0$

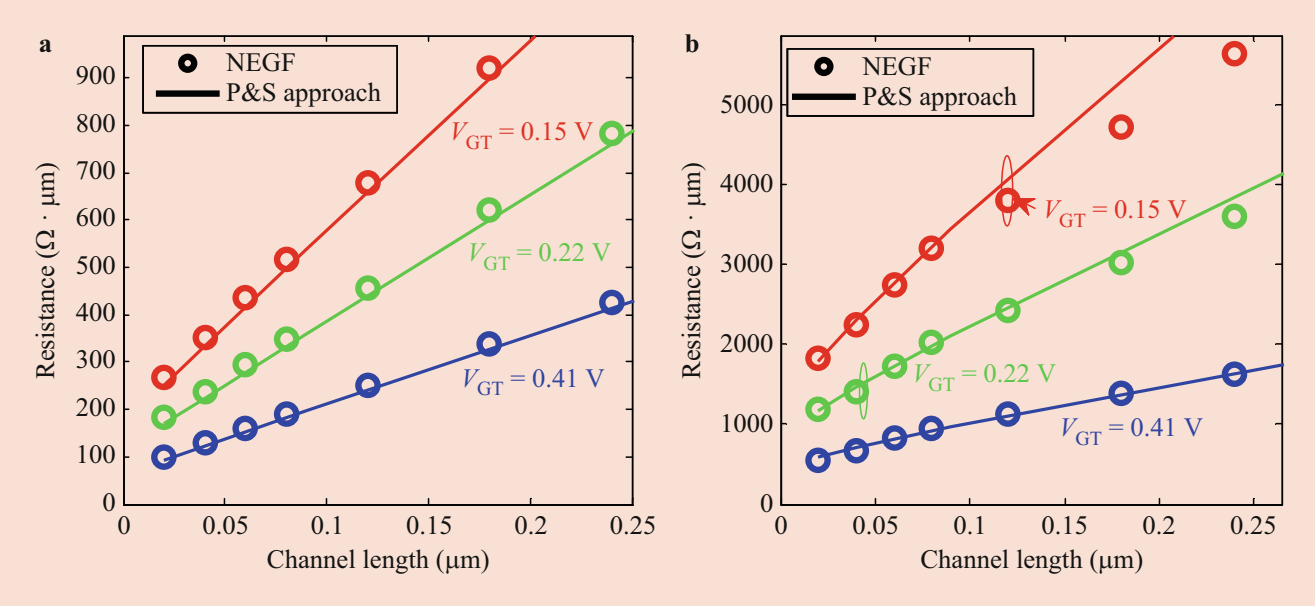


Fig. 12.13 Device resistance R_{on} in the linear ((**a**): $V_{DS} = 0.01$ V) and saturation ((**b**): $V_{DS} = 0.8$ V) regimes for various V_{GT}. Best fit with P&S approach ($C_{OX} = 0.025$ F.m^{-2}; $\mu_0 = 0.069$ m^2/(V.s); $\theta = 0$, $v = 2.1$e5 m/s) using an external overlap resistance model: $R = 0$ Ω.µm, $\sigma = 13$ Ω.µm.V. NEGF simulations within the EMA and with phonon only

to channel capacitance C_{gc} normalized using the front oxide capacitance C_{ox} with respect to the front-gate voltage V_{GS} for various back-gate voltages V_{bG}. A clear change of the capacitance shape can be observed for high back bias. In this case, the inversion charge shifts toward the back oxide for negative gate voltage and gradually shifts back to the front interface when increasing the gate voltage. This situation is depicted in Fig. 12.16 where band diagrams are extracted for an effective surface of $|E_{eff}| \sim 0.65$ MV/cm for at either $V_G = 1$ V and $V_B = 0$ or $V_G = -1$ V and $V_B = 8$ V.

Figure 12.17a shows the extracted threshold voltage (from the maximum of $\frac{\partial\left(\frac{g_m}{I_D}\right)}{\partial V_G}$ with current curves shown in Fig. 12.15). As well known [33], the slope of V_{TH} vs V_{bG} (namely, the coupling factor) changes for high back-gate biasing values. This is due to the back inversion in which the silicon layer capacitance C_{Si} has to be considered:

$\Delta V_{TH} = -\frac{C_{BOX}}{C_{OX}} \cdot \alpha \cdot (V_B)$ with $\alpha = 1$ for front inversion and $\alpha = \frac{C_{OX}+C_{Si}}{C_{Si}}$ for back inversion.

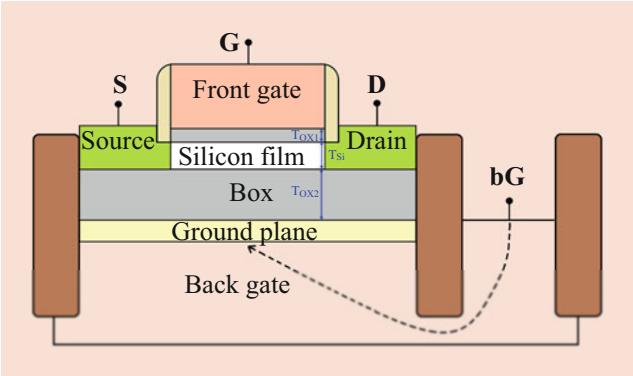


Fig. 12.14 Back biasing in UTBB FDSOI MOSFET

Figure 12.17a shows the inversion charge density (obtained integrating the capacitance curves of Fig. 12.15) as a function of gate voltage. The total inversion charge is composed of the sum of the back and the front inversion charges, and a change of the slope versus V_G is clearly visible in high FBB. Equation (12.3) remains valid provided that we define two threshold voltages for the front and back inversion charges and keeping in mind that the back inversion charge remains constant for $V_G > V_{TH2}$ due to the screening by the front inversion charge.

12.4 MOSFETs in Analog Design

In recent low-power and high-performance circuits such as those implemented in FDSOI for the Internet of Things (IoT) market, one needs to operate MOSFETs from weak inversion (WI) to SI regimes [51]. MOSFET compact models should accurately reproduce transistor behavior in all regions of operation including in WI and MI regimes. Considering only digital figures of merit (FoMs) such as ION and I_{OFF} is not sufficient to assess analog behavior of a MOSFET. Moreover, analog applications such as amplification need accurate prediction of continuous and higher-order MOSFET metrics and FoMs in all levels of inversion. It is worth pointing that moderate inversion region has been found to be a good compromise, while power consumption and speed are valued equally [23, 52, 53]. The MI provides higher transconductance for lower current and still acceptable bandwidth for low-power and low-voltage applications. It is worth noting that all parameters used in the model derivation in (12.10) are fitting parameters extracted in SI regime. Therefore, the derived analytical model in the previous section is very useful when MOSFET channel is strongly inverted and obviously not valid in WI and MI regimes where some analog applications find a valuable trade-off between gain, power consumption, and speed.

For hand calculations, although classical WI exponential law and SI square law models can be carefully used, the transconductance efficiency (g_m/I_D) charts briefly presented hereafter are more convenient to predict UTBB FDSOI MOSFET capability in all levels of inversion. The transconductance efficiency is an interesting figure of merit which can be used to gain insight into the transfer characteristic of a MOSFET for all levels of inversion. It is also defined as the slope of the transfer characteristic in its semi-logarithmic scale as it is expressed as:

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_{GS}} = \frac{\partial \ln I_D}{\partial V_{GS}} \tag{12.21}$$

The transconductance efficiency is used in Fig. 12.18 to compare the efficiency of three generations of planar MOSFET, highlighting at the same time the semiconductor industry smooth transition from bulk to UTBB FDSOI.

The plateau of the g_m/I_D plots (i.e., maximum g_m/I_D) in Fig. 12.18, which represents the WI regime, is inversely proportional to the subthreshold slope. The 28 nm FDSOI technology provides a near-ideal subthreshold slope (1.08) versus 65 nm bulk (1.13) and 28 nm bulk (1.17). The downscaling from 65 nm to 28 nm bulk clearly shows the electrostatic control degradation due to SCEs, which results in higher leakage. Moreover, the SCEs, responsible of the departure from the ideal square law current trend, are worst for bulk technologies as shown in the inset of Fig. 12.18. In particular, the velocity saturation and series resistances are responsible for the decrease of g_m/I_D at high current density and departure from the $\sim 1/\sqrt{I_D}$ trend. The main advantage of 28 nm bulk versus 65 nm bulk is the higher g_m/I_D in SI region, thanks to a higher $C_{ox}.\mu_0$, which results in a higher transconductance efficiency for the same current value (analog and RF applications) and a higher I_{ON} current (digital applications).

12.4.1 Inversion Level Metric

We have seen that the transfer characteristic of a MOSFET is used to extract a threshold voltage of the inversion phenomena taking place in the channel and is generally used to determine the level of the inversion of the MOSFET. In particular, the gate overdrive voltage (i.e., $V_{GT} = V_{GS} - V_{TH}$) is usually taken as a metric for this inversion phenomenon. However, the threshold voltage concept is not accurately defined, and the overdrive voltage loses its physical meaning below threshold (i.e., $V_{GS} - V_{TH} < 0$ V). Therefore, another metric, namely, the inversion coefficient (IC), has been introduced by Vittoz [54] and validated for a double-gate MOSFET in our published work [55]. IC is nothing else than the normalized drain current using the technology current

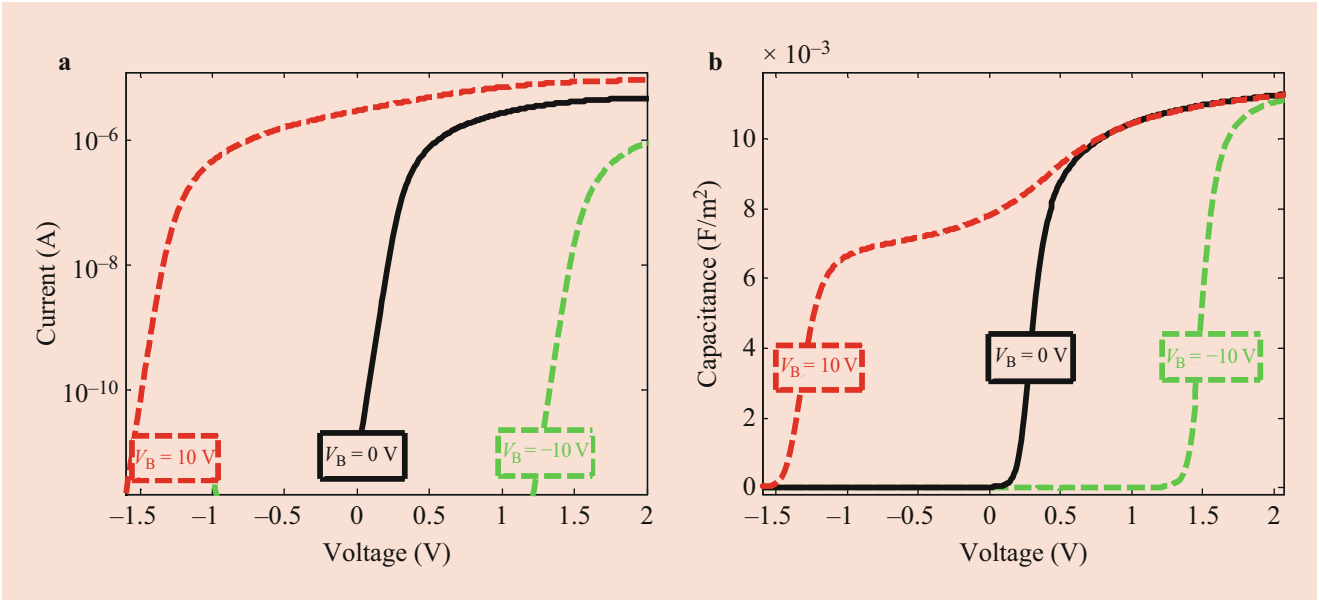


Fig. 12.15 (**a**) Measured and normalized linear drain current $I_D/(W/L)$ versus front-gate voltage V_{GS} for various back-gate voltages V_{bG}. (**b**) Measured and normalized front-gate capacitance versus front-gate voltage for various back-gate voltages. NFDOSI with $L = 10$ µm, $W = 2$ µm. Test structures for capacitance measurements performed on 30 identical devices in parallel

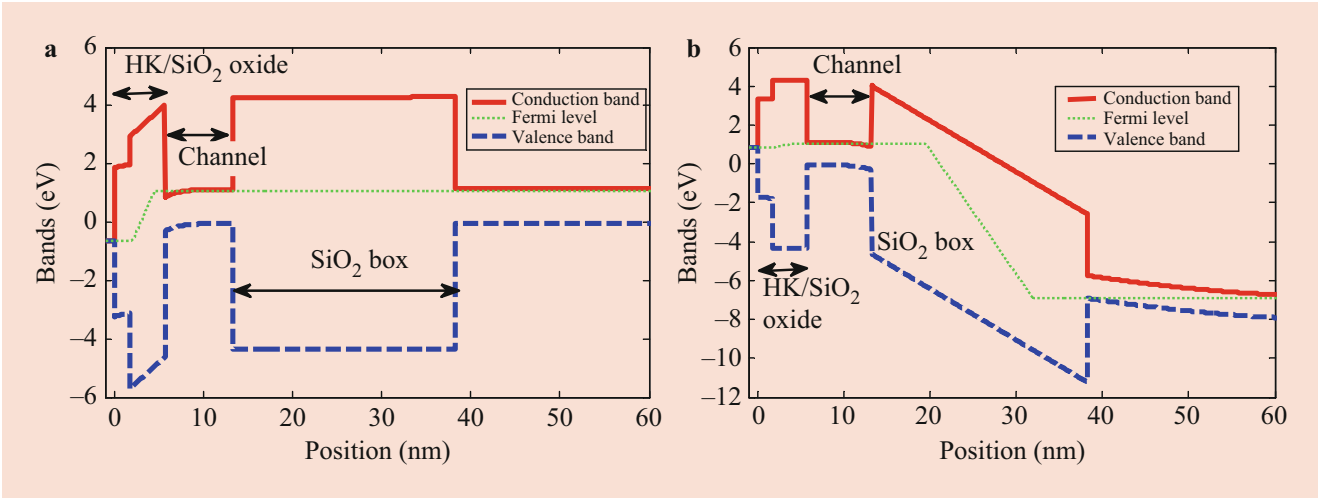


Fig. 12.16 Simulated band diagrams of the thick oxide FDSOI device when (**a**) the back terminal is grounded and (**b**) with 8 V back bias. The effective channel field is +0.652 MV/cm and –0.65 MV/cm, respectively

I_i which is located at the intersection of the WI (i.e., the plateau representing the Boltzmann limit) and the saturation SI square law asymptotes of the g_m/I_D plot versus normalized current $I_\square = I_D \cdot (L/W)$ for a long-channel MOSFET as depicted in Fig. 12.18. The *IC* expression is given as:

$$\mathrm{IC} = \frac{I_\square}{I_i} = \frac{I_D/(W/L)}{I_i} \tag{12.22}$$

Inversion coefficient concept is helpful to easily identify the MOSFET level of inversion from WI to deep SI. Unlike relaxed bulk technologies, in advanced technologies such as FDSOI, MI covers more than two decades of the drain current as depicted in Fig. 12.19a. IC will be used instead of the gate voltage overdrive $V_{GS} - V_{TH}$ while dealing with analog applications in order to cover all levels of inversion including MI.

12.4.2 MOSFET g_m/I_D Invariance

The drain current expression is complex in an asymmetric double-gate MOSFET and cannot be easily used for hand calculations in analog design. However, we have shown that

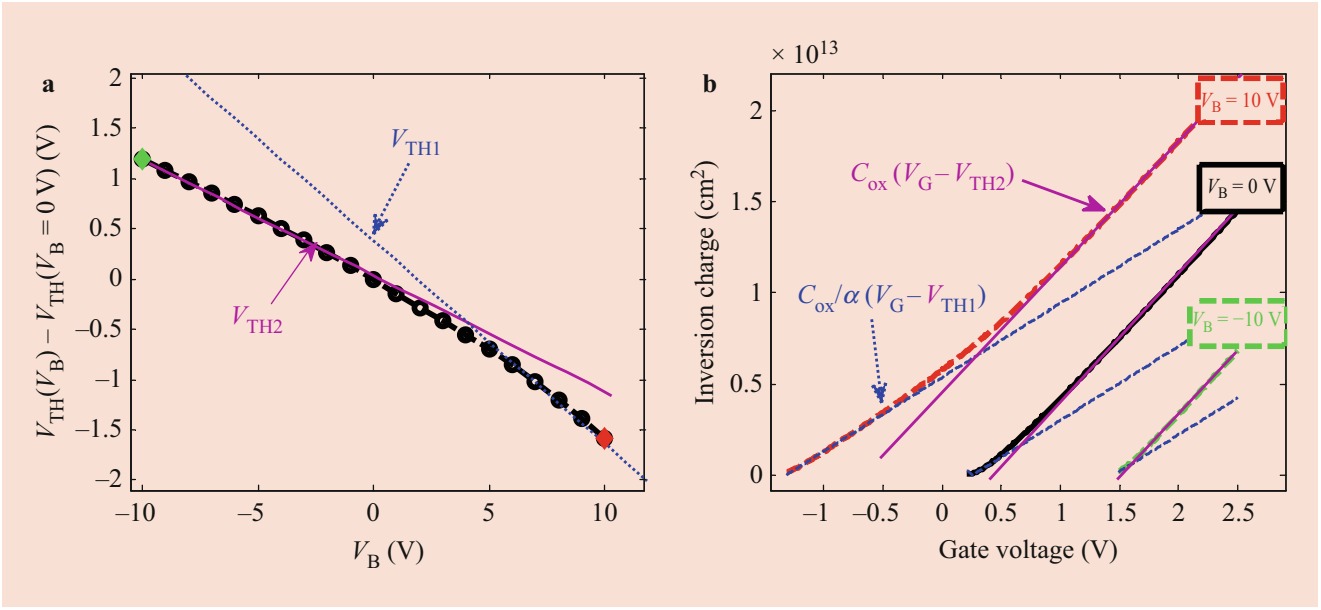


Fig. 12.17 Extracted threshold voltage (**a**) and inversion charge density (**b**). Model with $C_{OX} = 0.0114$ F.m^{-2}; $C_{BOX} = 0.0013$ F.m^{-2}; $C_{SI} = 0.015$ F.m^{-2}

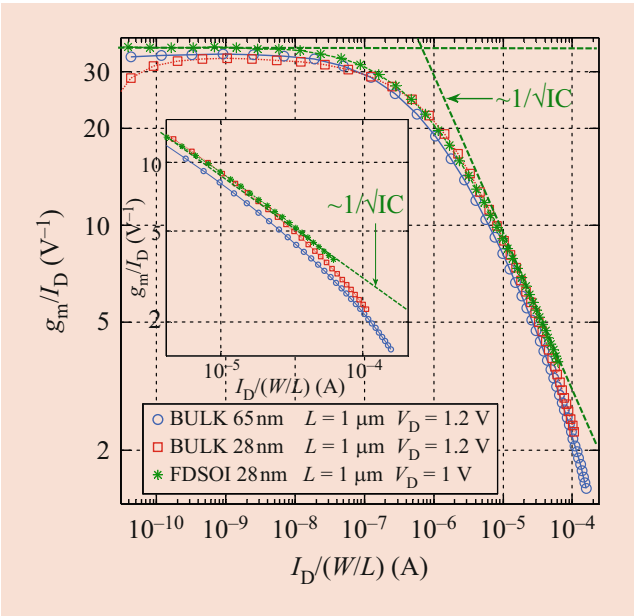


Fig. 12.18 Measured transconductance efficiency g_m/I_D versus normalized drain current $I_D/(W/L)$ for long channels $L = 1$ µm in saturation for bulk 65 nm, bulk 28 nm, and UTBB FDSOI 28 nm planar MOSFETs

a threshold voltage-based approach similar to bulk can be used to get a first insight into the main physical ingredients in SI regime. In MI where the simple models fail or for the case of short channels where complex physical phenomena occur, measured g_m/I_D charts can be used to estimate the analog performance of the device. In particular, the UTBB FDSOI transconductance efficiency charts are shown to be predictable and generally invariant. Indeed, if we plot the front transconductance g_{m1} over the drain current I_D characteristics with respect to IC for various V_{bG} in a log-log scale, we get the interesting invariance property shown in Fig. 12.19 where g_{m1}/I_D is normalized using the thermal voltage U_T and the front-gate slope factor n_1 (i.e., all g_{m1}/I_D plots superpose for various back-gate voltages V_{bG}). This property is assessed in [55] using measurements with respect to geometry, back-gate voltage, temperature, drain to source voltage, and process variations. In SI, all the long-channel plots tend to the square law characteristic which varies as the inverse of the square root of the current as can be predicted using (12.10). For WI, the measured plateau corroborates the exponential law of the drain current with respect to V_{GS}.

As shown in Fig. 12.19 for a long transistor, transconductance efficiency is maximum in weak inversion, decreases rather slowly in moderate inversion, and decreases as the inverse square root of IC in strong inversion. At the onset of strong inversion (i.e., IC = 10), transconductance efficiency is 70% lower than its maximum value.

The g_m/I_D invariance property can be used to predict the transconductance provided that W/L and level of inversion (i.e., IC) are given. Moreover, as a substitute to the analytical drain current model, one can predict drain current provided that W/L, V_{TH}, and gate voltage V_{GS} are provided. This calculation requires an additional chart of IC with respect to the gate voltage overdrive $V_{GS} - V_{TH}$ as shown in Fig. 12.19b, noting that a bijective relation exists between the two inversion metrics. This can allow designers to predict MOSFET DC properties without the need of an analytical model including in MI which is difficult to capture.

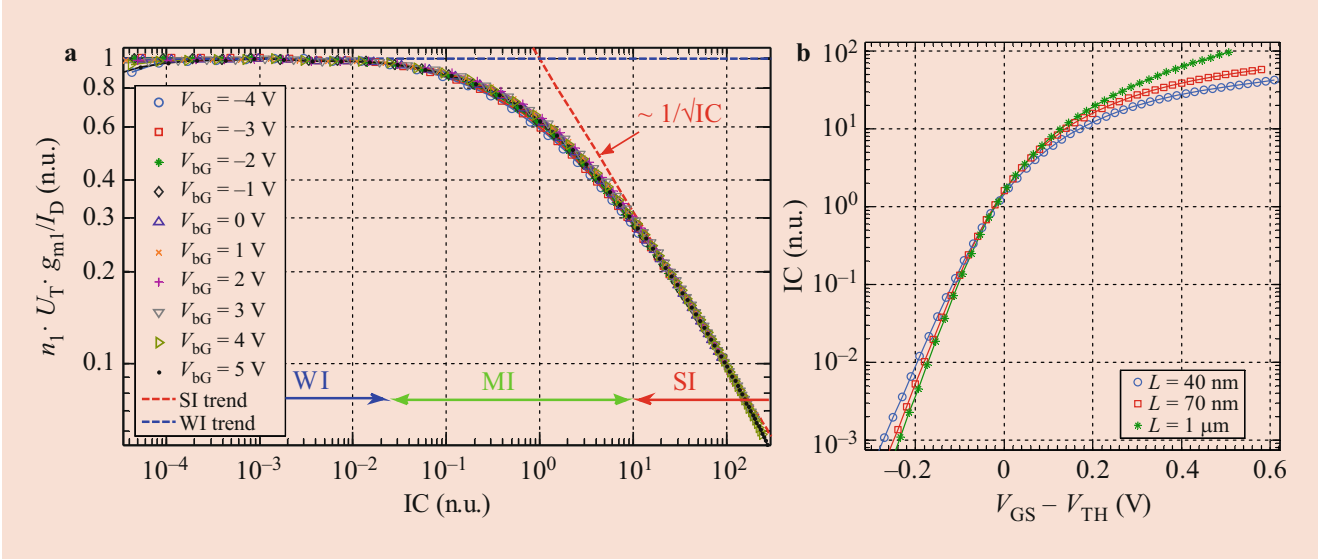


Fig. 12.19 (**a**) Measured and normalized g_{m1} over I_D as a function of the inversion coefficient at different V_{bG} for NMOS ($L = 1$ µm and $W = 1$ µm) in saturation ($V_{DS} = 1$ V) at $T = 25$ °C along with the WI and SI trends. (**b**) Inversion coefficient vs gate voltage overdrive for three lengths $L = 40$ nm, $L = 70$ nm, and $L = 1$ µm

Physical Insight

Both electrostatic and transport contribute to the g_m over I_D characteristic as:

$$\frac{g_m}{I_D} = \frac{\partial \ln I_D}{\partial V_{GS}} = \frac{1}{Q_{inv}} \frac{\partial Q_{inv}}{\partial V_{GS}} + \frac{1}{v} \frac{\partial v}{\partial V_{GS}} \tag{12.23}$$

noting that $I_D = Q_{inv} \cdot v$, where v is the average velocity of the charge carrier. In order to assess the transport contribution to the g_m over I_D characteristic, we propose to use a simple mathematical operation based on (12.23) and given as:

$$\frac{1}{v} \frac{\partial v}{\partial V_{GS}} = \frac{g_m}{I_D} - \frac{1}{Q_{inv}} \frac{\partial Q_{inv}}{\partial V_{GS}} \tag{12.24}$$

The mathematical operation in (12.24) is applied to data obtained from measured transfer characteristics $I_D - V_{GS}$ and gate to channel capacitance characteristics $C_{gc} - V_{GS}$ for various V_{bG} values in linear regime. Inversion charge Q_{inv} is extracted using a careful integration of the $C_{gc} - V_{GS}$ characteristics. The contribution of the transport to the g_m over I_D is finally depicted in Fig. 12.20 with respect to V_{GS} for various back-gate voltages V_{bG}. We clearly observe the impact of the V_{bG} on carrier velocity. The transport quantity $1/v \; \partial v/\partial V_{GS}$ which is equal to the derivative of $\ln(v)$ with respect to V_{GS} has its minimum at higher velocities. Therefore, for intermediate V_{bG} values close to –0.5 V, thanks to the volume inversion strength, the maximum apparent carrier velocity is higher. The term "apparent" stands for the fact that the extracted transport metrics (i.e., carrier velocity or mobility) using drain current characteristic represent an average on all carriers in the silicon film (i.e., in all its volume). Thanks to a lower vertical field, while volume inversion is taking place, more carriers in the Si volume are contributing to the transport, and this is interpreted as being an increase of the mobility at the back interface in various publications such as in Ohata [56] and Rudenko [57]. Although the transport contribution slightly depends on the back-gate voltage V_{bG} and the level of inversion, the impact on the variation of the normalized g_m/I_D plots is negligible.

Short Channels

Figure 12.21a shows normalized transconductance efficiency as a function of IC for different transistor lengths for N-type MOSFET. g_m/I_D is normalized using the slope factor n_1 of the long-channel MOSFET in order to highlight the slope degradation of short channels. Transfer characteristics of short channels also depart from the SI asymptotic trend because of mobility reduction, velocity saturation effects, and series resistance. The deviation from SI trend is more important for N type than P type because of the higher carrier mobility. Transconductance efficiency curves overlay in weak and moderate inversion for the 120 nm to 4 µm range of channel lengths. SI degradation ceases when carrier's velocity saturates completely and a ~1/IC dependence (i.e., linear dependence in $V_{GS} - V_{TH}$) is obtained. An additional degradation with respect to the linear asymptote (~1/IC) occurs when series resistance and mobility degradation add to velocity saturation for short-channel transistors. The long-channel transistor unique chart can be used in weak and moderate inversion to predict transconductance efficiency

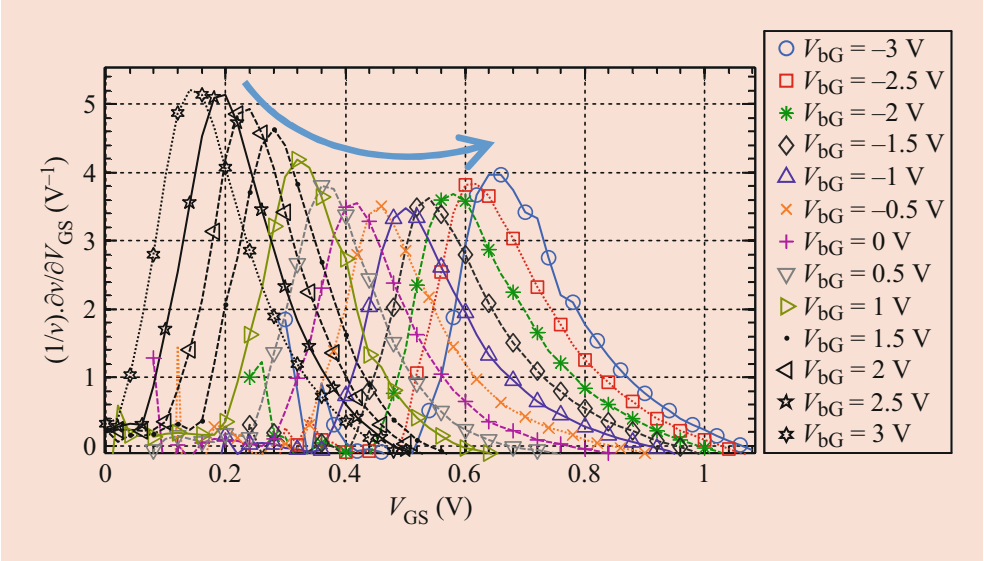


Fig. 12.20 Measurements showing the transport term $\partial \ln(v)/\partial V_{GS}$ versus gate voltage V_{GS} for various V_{bG} values (from –3 V to 3 V) in linear regime ($V_{DS} = 50$ mV)

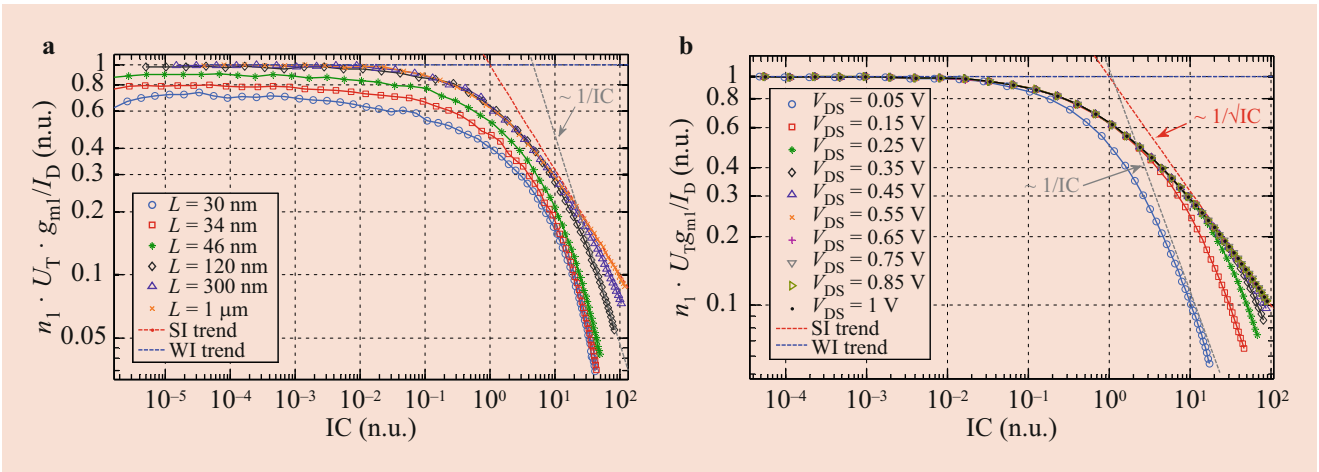


Fig. 12.21 (**a**) Measured and normalized g_{m1} over I_D as a function of the inversion coefficient for different lengths for NMOS ($W = 1$ µm) in saturation ($V_{DS} = 1$ V) at $T = 25$ °C. (**b**) Measured and normalized g_{m1} over I_D as a function of the inversion coefficient for different V_{DS} for NMOS ($W = 1$ µm and $L = 1$ µm) at $T = 25$ °C

for all transistors with a length greater than 120 nm, while error is kept lower than 5%.

Linear Versus Saturation

The g_m/I_D invariance should be considered in priority for saturation regime, and it is worth assessing the limit of drain potential below which the invariant breaks down in the onset of strong inversion. This information is useful in modern low-voltage low-power design since high transconductance efficiency is obtained in moderate inversion with lower drain to source saturation voltage V_{DSAT}. Figure 12.21b shows normalized transconductance efficiency versus IC for different drain to source voltages. In linear regime, the g_{m1}/I_D curve departs from the saturation and strong inversion asymptotic behavior and follows the 1/IC asymptote instead (i.e., linear dependence in $V_{GS} - V_{TH}$) as seen in the previous section. The transconductance efficiency chart defined at $V_{DS} = 1$ V can be used for lower drain to source voltages down to $V_{DS} = 250$ mV in weak and moderate inversion with an error of less than 4%.

The g_m over I_D charts clearly can be beneficial to the hand calculation-based analog design. Other important parameters such as gate-to-drain capacitance C_{gd} can easily be linked to the g_m over I_D through the powerful normalized IC instead of the questionable gate voltage overdrive. Thus, the g_m/I_D as a metric of the transconductance efficiency of the MOSFET can be accurately predicted for all inversion levels at low-frequency operation where transconductance g_m can

be considered as invariant versus frequency. Yet, the g_m/I_D FoM quantitatively favors gain and power consumption at the expense of operation speed. The g_m/I_D FoM can be used in conjunction with other metrics such as the transit frequency f_T in order to consider operation speed. In particular, the new FoM $f_T.g_m/I_D$ introduced in [58] captures decently both the transconductance efficiency and RF performance noting that the maximum value of this RF FoM represents the best trade-off between gain, power consumption, and speed and lays in the MI regime close to the SI onset. The aforementioned FoMs (i.e., g_m/I_D and $f_T.g_m/I_D$) are valid in low frequency and assume the g_m over I_D is invariant with regard to operation frequency.

12.4.3 MOSFET Efficiency at High Frequency

Because of a crowded up to 5 GHz spectrum with many interferers, some applications such as automotive radar started to tackle the mm-Wave spectrum looking for more bandwidth [59]. Other applications are under active investigation and design in mm-Wave spectrum such as low-power portable radars demonstrated in [60] and high data rate wireless USB-like communication prospected in [61]. The nanoscale CMOS device architectures display very high transit frequencies practically beyond the millimeter-wave (mm-Wave) spectrum as shown in Fig. 12.3b and can be clearly used for these mm-Wave applications. To be ready to take full advantage of the advanced nanoscale CMOS devices, the CAD tools must be updated with accurate descriptions of their behavior in all operation conditions including low voltage. Therefore, advanced nanoscale MOSFET models for high-frequency (HF) and low-voltage (LV) applications are required.

The simulation of advanced high-precision mixed-mode analog circuits including A/D converters, switched-capacitor circuits, and RF amplifiers requires accurate device models in a large frequency spectrum including mm-Wave. At high-frequency operation, the input signal may have rise or fall times comparable or smaller than the transit time of the transistor. Most compact models available so far are low-frequency quasi-static operation models with no or simplified high-frequency effects. The quasi-static (QS) operation is defined when an applied small signal varies sufficiently slowly that the carriers in the channel can follow the variation simultaneously.

High-Frequency Distributed Effects

Y-parameters are obtained from *S*-parameters' measurements and usually used to assess the high-frequency behavior of RF devices. An equivalent of the transconductance g_m at high frequency is the mutual transadmittance defined as:

$$y_m = Y_{21} - Y_{12} \tag{12.25}$$

where Y_{21} and Y_{12} are, respectively, the gate-to-drain transadmittance and the drain to gate transadmittance. At low frequency, the imaginary part of the complex y_m tends to zero. Consequently, the modulus or the real part of y_m is equal to the transconductance g_m at low frequency.

Figure 12.22a shows the real part of y_m (denoted Re(y_m)) for a long-channel MOSFET compared with a QS model (e.g., the MOSFET equivalent circuit proposed hereafter) which assumes constant transconductance over frequency. The QS model is clearly valid only up to 1 GHz and does not reproduce the performance degradation (i.e., "transconductance" decrease) at high frequency. Clearly, the real part of y_m decreases beyond a critical frequency F_{crit} that is defined

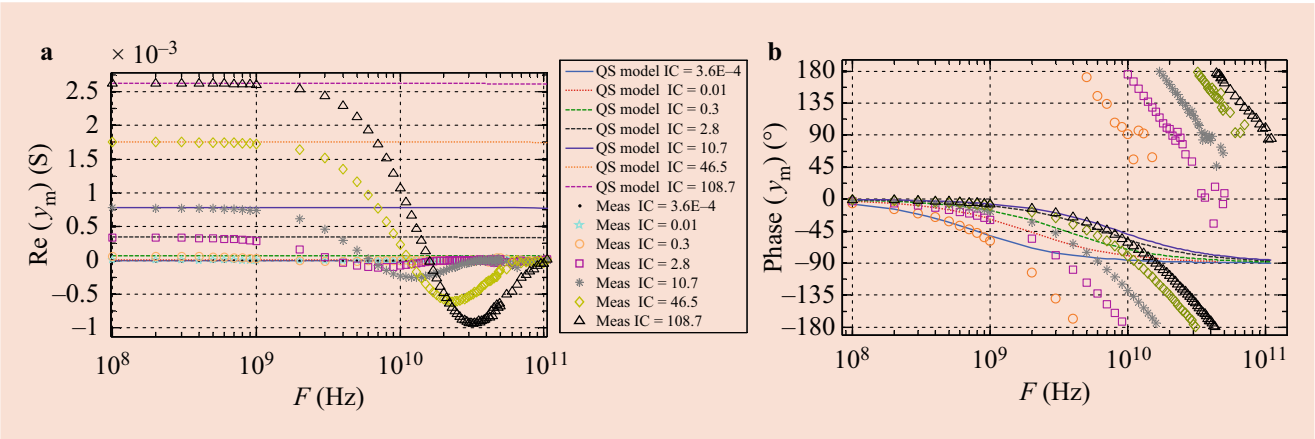


Fig. 12.22 (**a**) The real part of the measured and simulated mutual transadmittance y_m of a long channel $L = 1$ µm for various gate-to-source voltages from WI to SI in saturation ($V_{DS} = 1$ V). (**b**) The phase of the measured and simulated mutual transadmittance y_m of a long channel $L = 1$ µm for various gate-to-source voltages from WI to SI in saturation ($V_{DS} = 1$ V)

hereafter. Moreover, measurements show negative Re(y_m) at high frequency, which means that the phase shift is greater than 90°. This is confirmed in Fig. 12.22b where y_m phase is shown versus frequency. With regard to phase shift, the QS model is valid up to 1 GHz for $V_{GS} = 0.4$ V (i.e., IC = 0.3) and up to 8 GHz for $V_{GS} = 1$ V (i.e., IC = 109). The QS simulation phase tends to −90° for WI and SI, while measurements show a clear antiphase phenomenon (i.e., a difference in phase of 180°). The phase shift decreases faster than the modulus from initial value of zero up to more than 270° (i.e., antiphase 180° + 90° noting that phase continues to decrease even beyond the –180° and discontinuities in the plots are only due to the phase axis unit convention).

The critical frequency F_{crit} clearly depends on V_{GS} and consequently on the channel inversion level. For long-channel devices, the critical frequency is lower for lower inversion levels. However, for short-channel devices, the y_m phase decreases faster for stronger levels of inversion (i.e., F_{crit} is lower for SI) as the higher gate capacitance contributes to a higher signal delay in the gate [62]. The performance degradation at high frequency is observed for all geometries and bias conditions, in particular for long-channel devices. The phase shift of y_m means that the voltage excitation at the gate terminal lags behind the generated current at the drain terminal. This delay is due to the distributed effects that are taking place in the MOSFET structure and that are not modeled in QS compact models. Two distribution effects are competing in a MOSFET structure: (1) the NQS effect occurring in the channel [63] and (2) the longitudinal distribution effect taking place in the gate fingers [64]. The two distribution phenomena are confused in some research works noting that the consequences of the two effects on the Y-parameters are comparable. An enhancement of the model considering the two distributed effects is proposed in the following for high-frequency operation.

Transadmittance Efficiency (Y_m/I_D)

The low-frequency transconductance efficiency (g_m/I_D) is generalized to high frequency. More specifically, the transadmittance efficiency (y_m/I_D) offers a practical insight to help MOSFET performance assessment in all frequency ranges [62]. On top of the harmful impact of the high channel inversion level upon the transconductance efficiency, the trend is amplified due to the distributed effects described above. This impact is shown in Fig. 12.23 which reports the measured transadmittance efficiency modulus and phase versus operation frequency (F) for various inversion levels.

At any frequency, the y_m/I_D FoM defines the gain and phase shift for a given inversion level IC. The evolution of the transadmittance efficiency versus frequency provides a very valuable insight in terms of power performance and efficiency at high frequency in the presence of NQS effects. As shown in Fig. 12.23, at high frequency, the NQS operation degrades the efficiency expected at low frequency and in particular for weak and moderate inversion (IC < 10). The higher efficiency of the moderate and weak inversion modes (i.e., $g_{m1}/I_D > 10$) does not hold anymore beyond $F = 4$ GHz for $L = 1$ µm. Moreover, beyond 13 GHz and unlike low-frequency operation, the SI performs better with regard to the transadmittance efficiency. Plotting the integral of each curve in Fig. 12.23a over the interval [0, F_{NQS}] versus IC where F_{NQS} is an onset frequency of NQS effect (cf. expression in (12.26)), the maximum is found in SI (IC > 10) for $L = 1$ µm, while it is located in MI for $L = 300$ nm and shorter devices. This integral is a FoM for the trade-off between performance, power consumption, and speed and is a general case of the $f_T.g_m/I_D$ FoM which considers f_T as the maximum possible operation frequency.

$$\mathrm{FoM_{HF}} = \int_0^{F_{NQS}} \frac{|y_{mi}|}{I_D} \mathrm{d}F \tag{12.26}$$

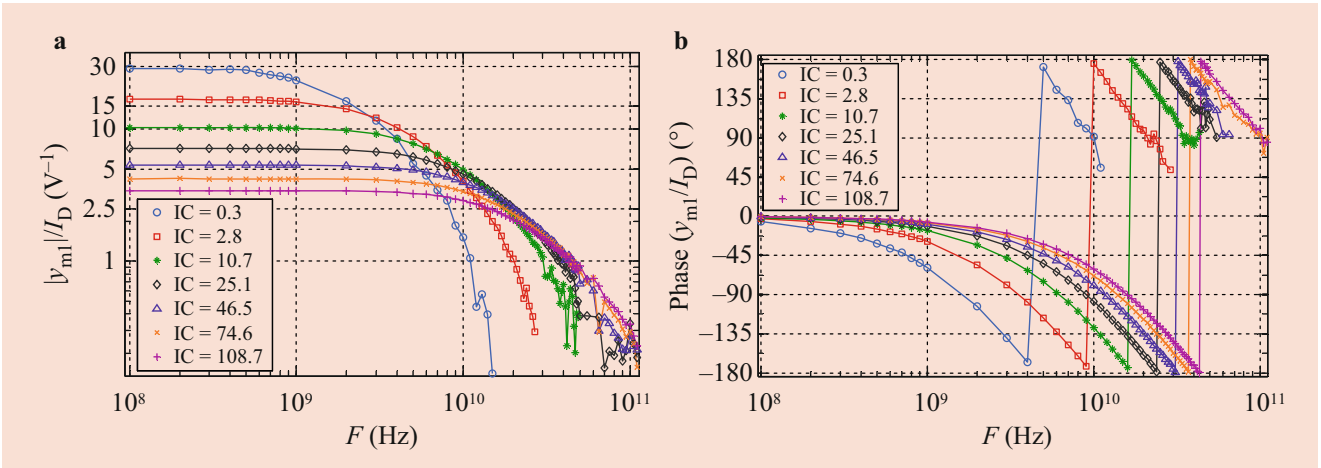


Fig. 12.23 Measured transadmittance efficiency modulus (**a**) and phase (**b**) versus the frequency for different IC for a NMOS ($L = 1$ µm) in saturation ($V_{DS} = 1$ V) and back-gate voltage $V_{bG} = 0$ V

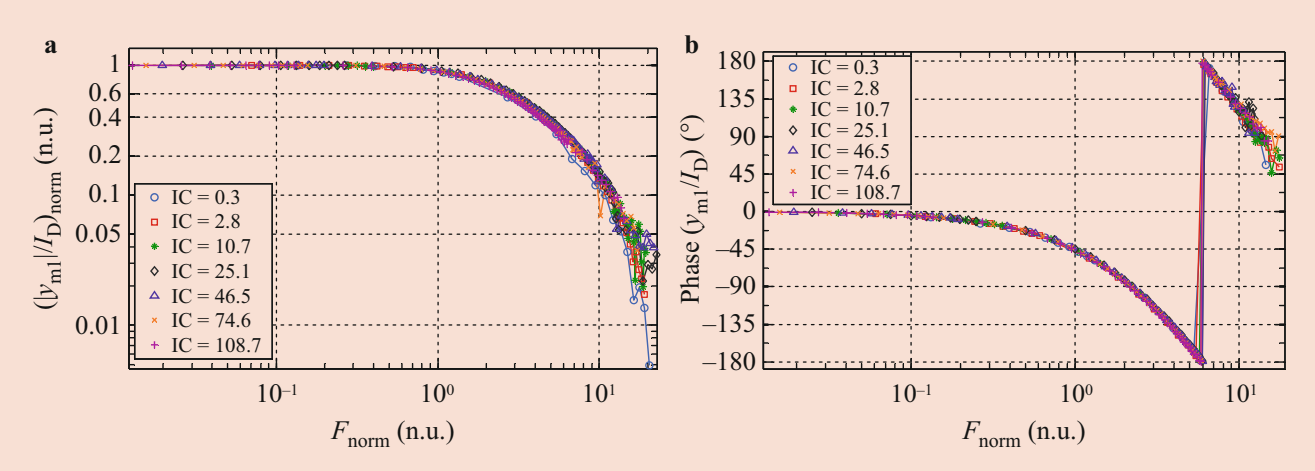


Fig. 12.24 Normalized transadmittance efficiency modulus (**a**) and phase (**b**) versus normalized frequency F_{norm1} at different IC for NMOS ($L = 1$ µm and $W = 1$ µm) in saturation ($V_{DS} = 1$ V) and back-gate voltage $V_{bG} = 0$ V (measurements)

Having a clear definition for the onset frequency of NQS operation is needed to provide a more realistic insight into the high-frequency performance of MOSFETs. Exact small-signal analytical expressions for NQS operation are presented in [63] for single-gate bulk MOSFETs and simplified in [65] to derive a compact model. The critical frequency F_{crit} expression, which corresponds to the first pole of the frequency characteristic of the device, as a function of the inversion coefficient IC is:

$$\mathrm{F_{crit}} = \frac{1}{2\pi}\frac{15}{4}\cdot\frac{\mu_{eff}U_T}{L^2}\cdot\frac{2+6\,\mathrm{IC}+3\sqrt{\mathrm{IC}+\frac{1}{4}}+4\left(\sqrt{\mathrm{IC}+\frac{1}{4}}\right)^3}{1+2\,\mathrm{IC}+3\sqrt{\mathrm{IC}+\frac{1}{4}}} \tag{12.27}$$

$$\approx \frac{15}{4\pi}\times\frac{\mu_{eff}U_T}{L^2}\cdot\sqrt{\mathrm{IC}}\ \text{(in SI)} \tag{12.28}$$

where μ_{eff} and U_T are, respectively, the effective mobility and the thermal voltage. Equation (12.28) approximates (12.27) while neglecting smaller terms in strong inversion, with less than 1% error on F_{crit} for IC > 2. It should be noted that F_{crit} is proportional to the effective mobility and U_T is inversely proportional to the square of gate length and accounts for the dependence of NQS on the inversion coefficient IC. This critical NQS frequency will be used for frequency normalization as in (12.29), while a further normalization of $|y_{m1}|/I_D$ is applied using the low-frequency transconductance efficiency g_{m1}/I_D as in (12.30).

$$F_{norm} = \frac{F}{F_{crit}} \tag{12.29}$$

$$\left(\frac{|y_{m1}|}{I_D}\right)_{norm} = \left(\frac{|y_{m1}|}{I_D}\right)/\left(g_{m1}/I_D\right) \tag{12.30}$$

All normalized moduli plotted in Fig. 12.24a from weak to strong inversion are almost superposed as a result of the frequency normalization in (12.29) and (12.30) (despite the very-high-frequency disturbance of the measurement parasitic elements). The invariance is also evidenced for the phase in Fig. 12.24a up to a phase shift as large as 270°.

If we consider the additional pole due to the gate-distributed effect which is the main cause of the transconductance degradation at high frequency for short MOSFETs, a new normalization frequency is used. The first pole of the gate distribution effect is captured using a simple $R_g.C_g$ model where R_g and C_g are the gate resistance and average gate capacitance, respectively. For a short-channel MOSFET, the normalization taking into account NQS effect and gate distribution effect leads to similar conclusions as for the $L = 1$ µm case [62].

These results are of prime importance for modeling NQS effects in UTBB FDSOI MOSFETs. A simple but powerful analytical model can predict the gate transconductance, magnitude, and phase, during highly non-static operation of the intrinsic channel and in all the regions of operation. Additional normalizations in terms of the inversion coefficient and critical frequency were used to derive a kind of abacus, paving the way to a simple and efficient high-frequency design methodology where device parameters, biasing conditions, and frequency are treated on the same ground.

12.4.4 Small-Signal Equivalent Circuit

High-frequency operation of a MOSFET is closely linked to its bias condition and consequently to its DC operation. The high-frequency QS operation can be seen as an assessment of the multiple derivations of the DC operation, in that it scans a part of the *I*–*V* characteristic and "senses" its variations.

When terminal voltage variations are sufficiently small, the small-signal assumption can be considered, and linear relations between produced current variations and input voltage variations can be used. Consequently, only one derivation of the I–V characteristic is sufficient to predict the behavior of the MOSFET in small-signal assumption. Acceptable prediction of the derivatives of the DC characteristic obviously relies on accurate DC model (e.g., the simple drain current model in (12.10) or the g_m/I_D charts).

In order to allow a simpler access to the different contributors to the small-signal frequency operation, equivalent circuits of the MOSFET devices are usually proposed. For high-frequency operation, the device core model (e.g., a compact model or a lumped small-signal equivalent circuit) is enriched to capture parasitic and distribution effects.

One of the frequently used MOSFET equivalent circuits is the Meyer (1971) one based on reciprocal capacitances (C_{gs}, C_{gd}, and C_{gb}). Besides the problem with the charge conservation, this model is still acceptable for hand calculation with small errors at low-frequency operation. An augmented version of the Meyer model used hereafter to model the UTBB FDSOI MOSFET small-signal equivalent circuit valid in low-frequency operation is depicted in Fig. 12.25. It includes intrinsic MOSFET components such as the front and back transconductances g_{m1} and g_{m2}, respectively, and extrinsic elements such as source and drain series resistances (i.e., R_S and R_D, respectively). Gate-to-source (C_{gs}), gate-to-drain (C_{gd}), and front-to-back-gate (C_{gb}) reciprocal capacitances are also included as shown in Fig. 12.25. By a reciprocal C_{xy} capacitance, we mean that the following condition is verified:

$$\frac{\partial Q_x}{\partial V_y} = \frac{\partial Q_y}{\partial V_x} \tag{12.31}$$

It should be noted that the equivalent circuit elements (i.e., capacitances and resistances) include both intrinsic and extrinsic parts. It is important to distinguish between the intrinsic (denoted by "i") and extrinsic (denoted by "e") contributions that have different origins. The intrinsic part is related to the device itself and mainly useful for channel current modulation, while the extrinsic part is related to parasitic elements unnecessary for the device operation. The extrinsic part can be optimized using proper layout technics such as multi-finger layout but cannot be completely removed. At high-frequency operation, the extrinsic elements gain particular importance and must be carefully modeled. At mm-Wave operation, these parasitic elements can even dominate the device performance. In general, the electrostatic couplings between the MOSFET terminals are not reciprocal, and for the dynamic operation modeling, 16 transcapacitances are required to agree with the charge conservation rule. Recent MOSFET compact models such as L-UTSOI account for the charge conservation, and the 16 transcapacitances are provided as part of the simulators DC operating point (OP) information.

In the MOSFET device, the C_{gd} and C_{dg} capacitances are not reciprocal due to the gate impact on the channel inversion. The modeling of the non-reciprocal C_{gd} and C_{dg} capacitance effect is done by adding an imaginary part C_m to the transconductance g_m (i.e., drawn in parallel to it in the equivalent circuit as shown in Fig. 12.25). The mutual capacitance is defined as [66]:

$$C_m = \frac{\partial Q_d}{\partial V_G} - \frac{\partial Q_g}{\partial V_D} = C_{dg} - C_{gd} \tag{12.32}$$

The mutual capacitance is playing an important role although it is usually neglected for low frequency.

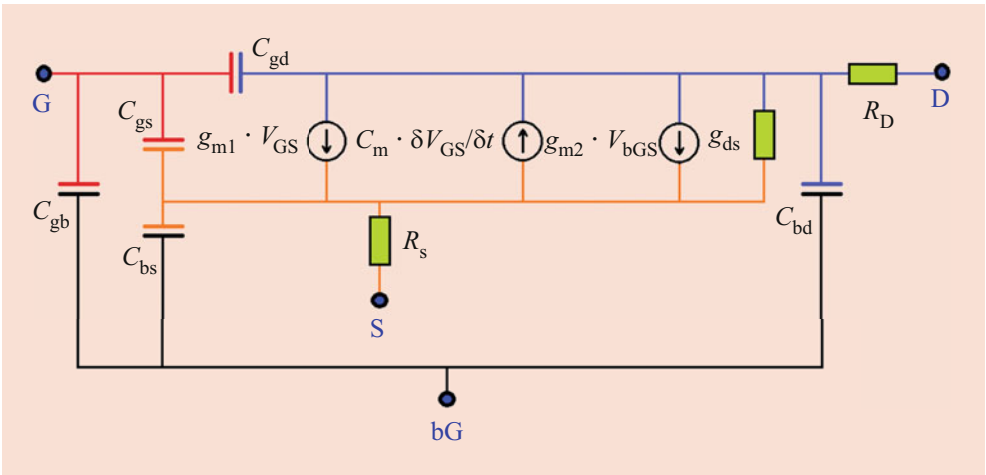


Fig. 12.25 Small-signal equivalent circuit for quasi-static operation of the UTBB FDSOI MOSFET including series resistances R_S and R_D ($C_{gd} = C_{gdi} + C_{gde}$ and $C_{gs} = C_{gsi} + C_{gse}$). C_{sd} is neglected here

All the coupling effects represented in the proposed equivalent circuit in Fig. 12.25 are extracted and validated under QS operation. For high-frequency operation, non-quasi-static effects (e.g., the lateral and longitudinal distribution effects) must be considered and modeled.

12.4.5 High-Frequency Modeling

The small-signal equivalent circuit in Fig. 12.25 is a QS model valid in low-frequency and unable to predict the high-frequency performance degradation due to the distribution effects. This limitation is shown in Fig. 12.22 for a long-channel device. The equivalent circuit parameters are determined using extraction routines applied to low-frequency measured characteristics performed on dedicated DC test structures. Only DC-based extraction leads to RF performance overestimation; therefore, RF extraction is required to multigate real high-frequency performances. The characterization using S-parameter measurements and de-embedding procedures is a method of choice for RF and mm-Wave spectrum operation assessment. S-parameters are practical metrics and are frequently used by microwave engineers and RF designers as the open or short circuit assumptions are not required. Instead, adapted terminations are used. However, S-parameters are generic and generally not practical to gain a deeper insight into the MOSFET physics. The measured S-parameters are transformed into Y-parameters and compared with the simulated counterparts for several inversion levels from WI to SI. Moreover, all equivalent circuit parameters as well as extrinsic elements such as gate resistance can be expressed using Y-parameters and easily evaluated at high frequency.

Gate Resistance

For DC and low-frequency operation, no gate resistance is required as the gate leakage current is very low (i.e., typically lower than 10 nA/μm^2). However, for high-frequency operation, the gate resistance should be considered, noting that high dynamic (AC) current is generated at the gate terminal. Moreover, the gate resistance in series with the gate capacitance will contribute a pole in the transadmittance function, and this will decrease the transadmittance as shown in Fig. 12.23. The gate resistance model accounts for the distributed aspect composed of the contact resistance, the horizontal resistance along the gate finger, and finally the vertical gate stack or interface resistance contributions.

The series and parallel RC-based front-gate network is developed using the pole-zero compensation technique. The gate network thus developed and integrated in the complete non-quasi-static model of Fig. 12.26a is convenient to simulate the gate distribution effect of short channels where the channel NQS effect contribution is multigated. In summary, besides the NQS effect that is modeled hereafter using channel segmentation, the gate-distributed effect can be modeled using series and parallel RC network. In addition to the overlap capacitances included in the core MOSFET model (i.e., in C_{gs} and C_{gd} capacitances), the gate network accounts for the distributed lateral fringing capacitance (i.e., $C_{frwS} + C_{frwD}$ and $C_{frlS} + C_{frlD}$) which is mainly dependent on the MOSFET width (i.e., finger length) [67].

NQS Modeling Using Channel Segmentation

At high-frequency operation, charge carrier's inertia in a long channel limits the device performance and induces admittance and transadmittance phase shifts. The channel can be viewed as a transmission line at high frequency and should be modeled accordingly. An accurate and physically based charge model for NQS effects has been proposed by Sallese [63] based on Bessel functions. Other NQS formulations based on spline collation method are also proposed [68, 69]. However, the proposed models are valid for small-signal analysis only (i.e., no time domain transient) or difficult to efficiently implement on top of the proposed models unless a simplification is used (need of additional nodes). Several simplified NQS models are also proposed in the literature to capture the first order and used in standard models such as the relaxation time approximation (RTA)-based method or the widely used Elmore model [70, 71]. However, these simplified models are only valid up to a maximum of 1 to 2 f_T. The segmentation of the channel proposed in [72] is adapted to the UTBB FDSOI MOSFET architecture and used for NQS modeling. The method is valid for small-signal as well as large-signal analysis, in frequency and time domains. The MOSFET device channel is split into several segments. Each segment is modeled using a compact model such as L-UTSOI or the equivalent QS circuit in Fig. 12.25 which provides comparable results. Only five elements provided accurate results with respect to measurements and chosen as a trade-off between accuracy and computational time. All segments have the same model parameters that represent the core behavior.

In order to model the DIBL effect, two voltage-dependent voltage sources are added in series with the two gate terminals. The DIBL is implemented as a threshold voltage shift. The overlap and fringe capacitances are added on top of the segmented channel and can also be modeled using a sixth parallel MOSFET with a mobility set to zero. The advantage of using a MOSFET shell for parasitic capacitances is the compatibility with the QS compact model parameters in particular the overlap capacitance term. In order to account for the diode formed between the well under

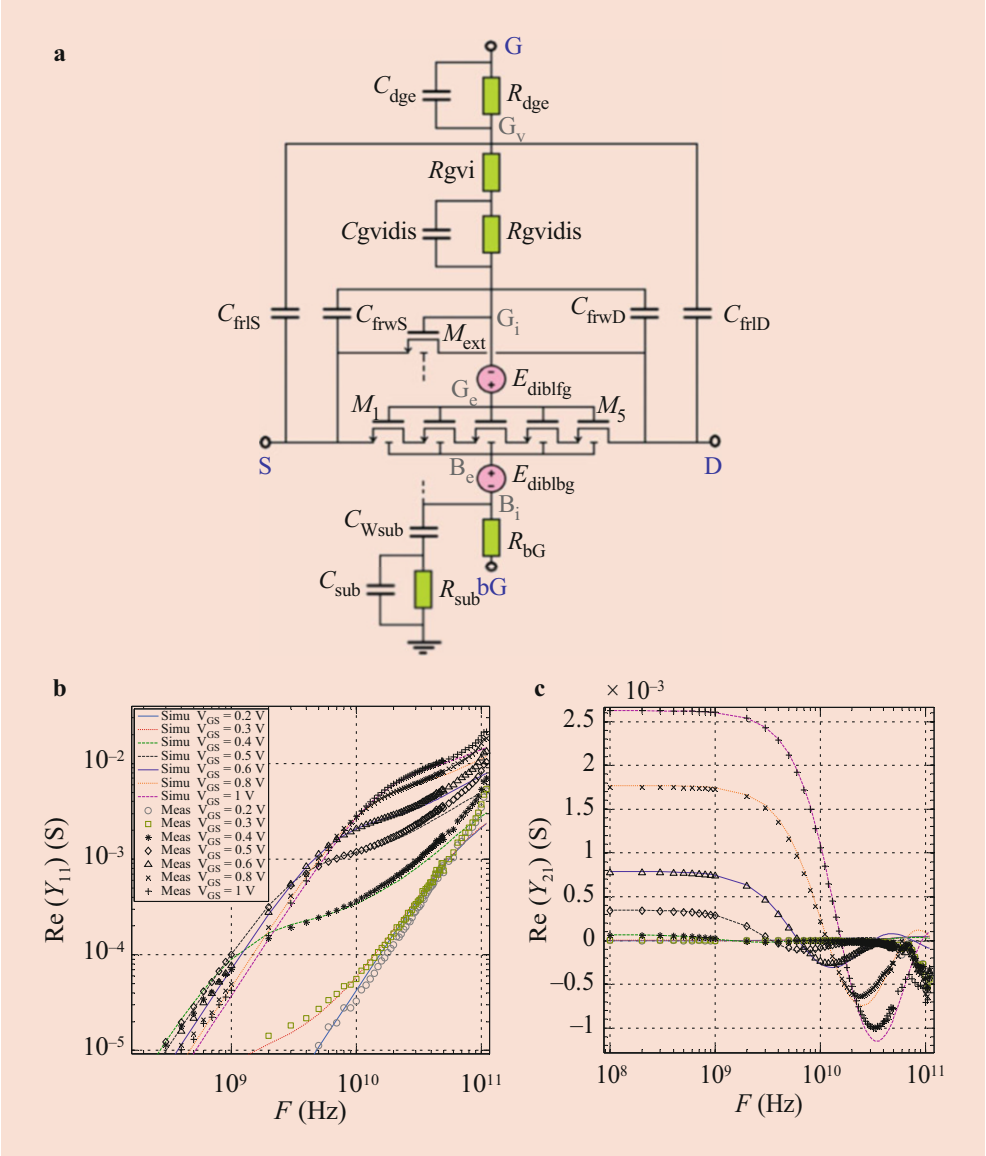


Fig. 12.26 (**a**) Complete non-quasi-static model. Simulation and measurements of the real parts of the input transadmittance Re(Y_{11}) (**b**) and input-to-output transadmittance Re(Y_{21}) (**c**) of 1-μm-long NMOS vs frequency for various gate-to-source voltages from WI to SI in saturation ($V_{DS} = 1$ V)

the BOX and the substrate, a simple lumped circuit is added to the model for the comparison with the measured data. The final proposed non-quasi-static model is shown in Fig. 12.26a along with *Y*-parameters' model-hardware correlation results (Fig. 12.26b, c). The proposed high-frequency non-quasi-static model is well suited for modeling UTBB FDSOI MOSFET operation. Validation conditions include length scaling down to nominal value, a wide frequency range up to 110 GHz, and operation under different channel inversion levels down to low-current and low-voltage regime. An excellent agreement is shown over more than eight decades of current density for DC and four decades for RF and mm-Wave.

12.5 Application Example: LNA Analog Design in MI Regime

The common architecture of mixed analog-digital systems consists of digital processing cores surrounded by A/D and D/A converters, which separate the digital part from the analog blocks. The mixed analog-digital systems are integrated into one IC known as the system-on-a-chip (SoC). The analog part role is to sense and communicate with the external world which is a key and sensitive role. In digital CMOS circuits, static power consumption is mainly

related to the leakage current. However, in analog circuits, biasing current is the main contributor for circuit power consumption. Thus, the devices used in analog blocks need to be permanently biased in the appropriate region. Besides power supply voltage lowering in recent technology nodes, the current budget should be reduced as well.

Several circuit topology-based techniques such as current reuse are proposed in analog design to optimize performance and power consumption [73]. These techniques are out of this chapter scope. Here, the focus will be on another design challenge which is the transistor sizing in MI regime to achieve a good trade-off between speed and low current budget. The RF designer dilemma is to calculate transistor geometry and current in order to get maximum amplification, minimum degradation of the signal-to-noise ratio, and minimum power consumption. The goal is to provide an illustration of an analog design method mainly based on the charts and properties described in previous sections. The UTBB FDSOI MOSFET characteristics are used for first-cut analog sizing method. In particular, the g_m/I_D versus inversion coefficient IC is used to determine the width of the MOSFET, while the transit frequency (f_T) versus IC charts are used for length selection. The design method, using relaxed length and MI regime, provides a valuable trade-off between gain, power consumption, and performance, while MOSFET width is kept reasonably large, and short-channel effects are multigated. An eye is also kept on passive devices' limitations from the very beginning of the sizing flow.

One of the key building blocks in a wireless system is a low-noise amplifier (LNA). The LNA circuit amplifies the input signal with minimum degradation of the signal-to-noise ratio. One of the challenges RF designers face is the simultaneous matching of the noise and the input impedance for the same source impedance. This challenge is beyond the scope of this chapter; therefore, ideal impedance matching is considered here. However, a constraint on the value of the inductors is considered in order to account for integrated inductors with acceptable quality factors.

12.5.1 LNA Circuit Characteristics

One of the most used circuit topologies for an LNA is the narrowband cascode. The cascode transistor is used to isolate the input from the inductive load. In particular, the Miller effect is reduced for the input transistor. However, using a cascode topology leads to a minimal room for drain to source voltage required to set both transistors in saturation. This also corroborates the need for MI operation as V_{DSAT} is lower in this regime. The circuit of the cascode LNA is shown in Fig. 12.27. The transistor M_1 is the input transistor, and M_2 is the cascode transistor. Both transistors are chosen to have the same geometry. Degeneration inductor L_s and input series inductor L_g are used for input impedance matching.

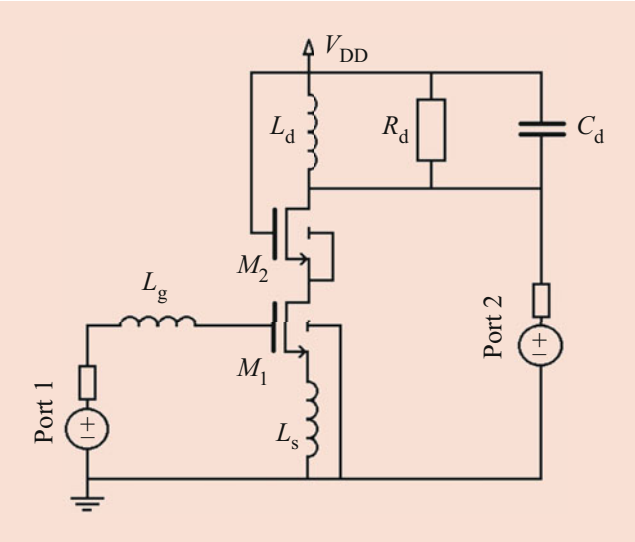


Fig. 12.27 LNA cascode circuit

The following specifications are taken as an example: Drain current is 2 mA, power gain is greater than or equal to 8, operation frequency is $F_0 = 35$ GHz, minimal noise figure NF_{min} is no more than 2 dB, and input impedance is matched for 50 Ω.

In order to size the circuit components and meet the specifications, the following three steps are followed:

12.5.2 Passives-Related Constraints and Length Selection

Inductance values are constrained and chosen within the integrated mm-Wave inductance values [25–100 pH] to favor higher-quality factors Q as in [74]. The real part of the LNA input impedance is mainly tuned using degeneration inductor L_s. The expression of this real part is given in (12.33), provided that M_1 intrinsic conductance influence on input impedance is neglected:

$$\mathrm{Re}\,[Z_{in}] = \frac{g_m L_s}{C_{gs}} \approx 2\pi f_{Ti} L_s \tag{12.33}$$

where C_{gs} and f_{Ti} are the gate-source and intrinsic transit frequency of M_1, respectively. According to the target specification related to impedance matching, the real part of Z_{in} is equal to 50 Ω. Thus, (12.33) links the transit frequency of M_1 to the inductance L_s. If we consider a maximum L_s inductance of 100 pH, M_1 transit frequency f_{Ti} should be greater than 80 GHz.

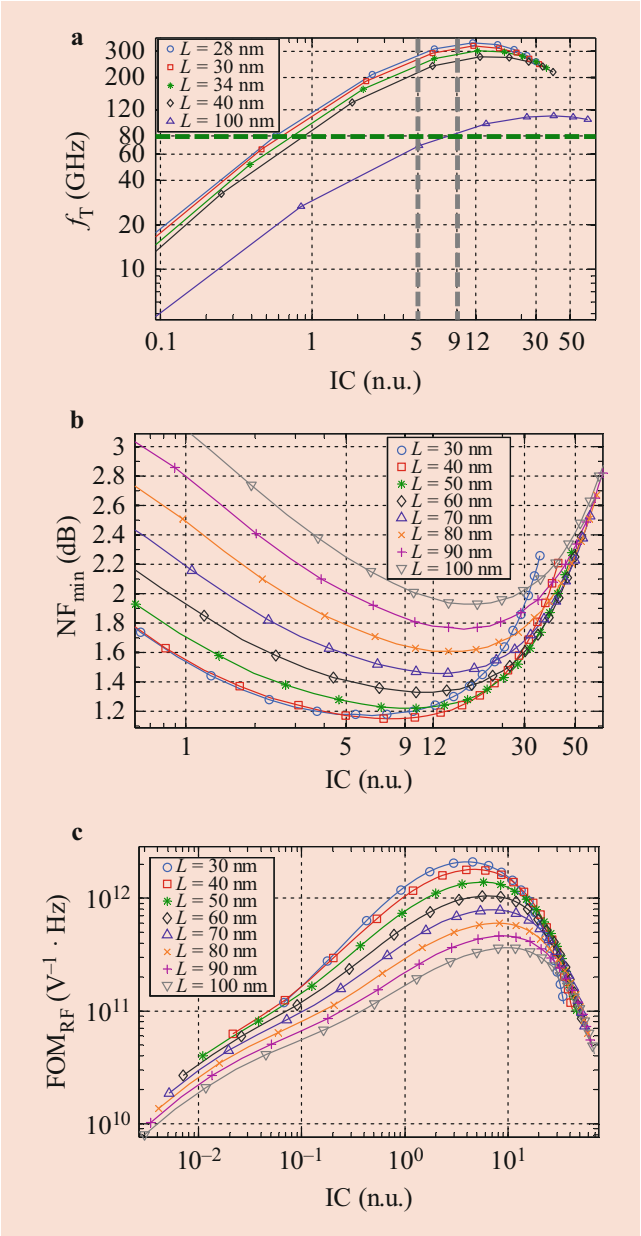


Fig. 12.28 (**a**) Measured f_T versus IC for various MOSFET lengths in saturation ($V_{DS} = 1$ V). (**b**) NF_{MIN} noise figure vs IC for various lengths in saturation. (**c**) FoM_{RF} versus IC for several short-channel lengths

According to Fig. 12.28a, for operation within MI, the MOSFET length that guarantees the required f_T is strictly lower than $L = 100$ nm. To obtain acceptable noise figures and using NF_{min} versus IC charts shown in Fig. 12.28b, length should also be lower than 100 nm. For illustration purpose, we will consider two channel lengths $L = 40$ nm and $L = 70$ nm with acceptable high-frequency performances and less subject to DIBL and mismatch than minimal length (cf. Fig. 12.3).

12.5.3 IC Selection

The maximum value of the RF FoM given in (12.34) and representing the trade-off between gain, high-frequency performance, power consumption, and noise figure is located in the upper part of the MI region for short channels as shown in Fig. 12.28c for several short-channel lengths (i.e., from $L = 30$ nm to 100 nm).

$$\mathrm{FoM_{RF}} = \frac{g_m}{I_D} \cdot \frac{f_T}{\mathrm{NF_{min}}} \tag{12.34}$$

For the selected lengths (i.e., $L = 40$ nm and $L = 70$ nm), FoM_{RF} is maximizing, respectively, at IC = 5 and IC = 9. In general, optimal IC for RF applications lays between IC = 1 and IC = 10.

Knowing the inversion level and length, one can calculate the degeneration inductor L_s based on (12.33). Thus, L_s values of 33 pH and 39 pH for, respectively, $L = 40$ nm and $L = 70$ nm MOSFET-based LNAs are found.

The LNA is designed to operate at $F_0 = 35$ GHz, and consequently, to cancel the input impedance imaginary part at this resonance frequency, the input inductor L_g is tuned with a target value given by [75]:

$$L_g = \frac{1}{(2\pi F_0)^2 \cdot C_{in}} - L_s \tag{12.35}$$

where C_{in} is including the total M_1 gate capacitance C_{gg} and the Miller effect of the gate-drain capacitance (C_{gd}).

12.5.4 Width and V_{GS} Calculations

The width is calculated using the expression (12.36) and the drain current is given by:

$$W = \frac{I_D}{\mathrm{IC} \cdot I_i} \cdot L \tag{12.36}$$

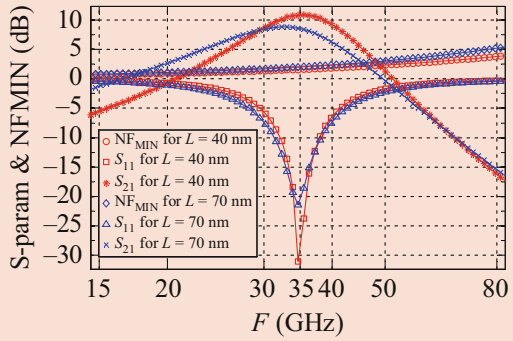
Close width values of 22.8 µm and 22.1 µm are found for, respectively, $L = 40$ nm and $L = 70$ nm based LNA circuits.

The gate voltage overdrive with respect to IC charts shown in Fig. 12.19 (**b**) is used to retrieve the gate-to-source voltage corresponding to the two IC values for each length. The calculated V_{GS} values are, respectively, 0.49 V and 0.55 V.

The results of the above sizing flow are shown in Fig. 12.29 versus frequency and summarized in a table for the operation frequency $F_0 = 35$ GHz.

Power gain is lower for the $L = 70$ nm based LNA because of the higher IC and consequently lower transconductance efficiency. The input impedance matching is acceptable for both LNA circuits. The NF_{min} value is higher for the

a



b

At F_0 = 35 GHz	S_{21}	S_{11}	NF_{min}
LNA (L = 40 nm)	10.9	–31	1.5
LNA (L = 70 nm)	8.6	–21.5	2

Fig. 12.29 (**a**) Power gain S_{21}, input match S_{11}, and minimal noise figure NF_{min} with respect to frequency for two LNA circuits (first with MOSFET length of 40 nm and second with 70 nm). (**b**) Summary table of the two LNA parameters at $F_0 = 35$ GHz

longer-channel-based LNA as expected; however, this can be lowered using optimized layout. The power consumption of both LNAs is 2 mW which is excellent for low-power applications.

The constrained sizing methodology proposed for the LNA at an operating frequency of 35 GHz is based on f_T versus IC measured or simulated curves for the length selection and on the invariance property of the g_m over I_D versus IC charts for the width calculation. The inversion coefficient is fixed to a value where the MOSFET optimum performance is expected, making this analysis dependent only on the channel current and "independent" of the front- and back-gate biases, a great simplification in terms of analysis. The methodology considers the passive components' limitations and thus requires less if not minimal iterations.

12.6 Conclusions

Silicon-based planar MOSFETs have had an impressive impact on our lives. The success was mainly based on the aggressive downscaling dictated by the high-performance integrated digital circuits. This chapter briefly reviews the evolution of the MOSFET architecture from single gate to double gate in the last few decades.

The detrimental SCEs have been controlled by brilliant scientists and creative engineers using new device architectures and new materials. Control of the channel using multiple gates appears to be a straightforward solution. The new architectures such as the UTBB FDSOI presented in this chapter allow for excellent electrostatic control, high level of integration, reduced power consumption, and very high operation frequency.

The extraction of the main physical parameters of the MOSFET, thanks to a simple SI analytical model, allows to gain insight into the device operation. The analytical model is accurate enough to predict the device behavior in SI regime which defines the ON current for digital applications. Analog applications need accurate prediction of the MOSFET performance in all inversion regimes particularly in MI where optimum MOSFET operation is expected. In the case of analog applications, the y_m/I_D charts versus (IC, F) can be used to predict and optimize the MOSFET operation and therefore favor the high-frequency and low-power operation. The simple models and charts presented in this chapter are essential tools for circuit performance prediction and first-order circuit optimization. Yet, the advanced compact models are necessary for final circuit verification over process, voltage, and temperature variations.

With the recent advances in silicon MOSFET technology, IoT network is becoming more of a reality in terms of their widespread use in various aspects of life. Although IoT already brings more capability in our daily life in terms of sensing and communicating using planar MOSFET RF systems, higher performance along with more autonomy is still to be explored. A need of faster and energy-efficient communication between sensors using 5G mobile network, for example, is emphasized by the industry today for a functioning IoT. Therefore, profound skills still have to be developed in the following two key areas: (1) silicon-based CMOS technology usage in mm-Wave spectrum and beyond and (2) transistor operation at lower applied voltages and in lower levels of inversion.

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Silicon Power Devices

13

Noriyuki Iwamuro

Contents

13.1 Introduction 424

13.2 Power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) 425
13.2.1 Power MOSFETs 425
13.2.2 The VDMOSFET Structure 427
13.2.3 UMOSFET Structure 437
13.2.4 Superjunction MOSFET 440
13.2.5 MOSFET Body Diode 443
13.2.6 Edge Terminations for Silicon Power Devices 444
13.2.7 Epitaxial Layers and Substrate Wafers 447

13.3 Insulated Gate Bipolar Transistors (IGBTs) 448
13.3.1 Background of IGBT Development 448
13.3.2 IGBT Structure and Operation 450
13.3.3 IGBT Safe Operating Area 458
13.3.4 Evolution of the IGBT Structure and Design Concept 463
13.3.5 IGBT Module Technologies 466
13.3.6 P-ch IGBT Devices 468
13.3.7 State-of-the-Art IGBTs 469
13.3.8 Future Prospects of IGBT Devices 473

13.4 MOS Gate Thyristors 474
13.4.1 The MOS-Controlled Thyristor (MCT) 475
13.4.2 The Base Resistance-Controlled Thyristor (BRT) 476
13.4.3 The Emitter-Switched Thyristor (EST) 476
13.4.4 MOS Gate Thyristors and IGBT Competition 477

13.5 Power Rectifiers 477
13.5.1 Unipolar Devices 477
13.5.2 Bipolar Devices 480

References 486

Abstract

According to a recent market survey and forecast on power devices (Fuji Keizai Co., Ltd website. https://www.fuji-keizai.co.jp/, 5 Jun 2019 (in Japanese)), the global device market in 2018 stood at about 3.0 trillion Japanese yen (about 27.3 billion USD); and of this total, SiC (silicon carbide) and GaN (gallium nitride) power devices accounted for slightly less than 41 billion Japanese yen (about 373 million USD), or as little as roughly 1.4% of the silicon power semiconductor device market. Despite numerous reports that SiC and GaN power devices exhibit far better characteristics than silicon power devices, the latter make up by far the largest segment of the power devices market. In the same forecast, by 2030, while the global power device market will grow by about 66% to 4.9 trillion Japanese yen (about 44.9 billion USD), the SiC and GaN power device market will not even make up 12% of the global market. Why would the silicon power device market maintain such a large market segment? Rapid technological advancement in silicon power devices has led to improvement in cost performance, which has dampened the motivation to adopt SiC and GaN power devices. In this chapter, the device structure and design concept of a variety of silicon power devices, and salient features and drawbacks of these devices are analyzed. In addition, it will present a brief history of their development and wrap up the state-of-the-art structures and characteristics of such devices.

Keywords

Power metal-oxide-semiconductor field-effect transistors (power MOSFETs) · U-MOSFETs · Superjunction · Insulated gate bipolar transistors (IGBTs) · Safe operating areas (SOAs) · Junction temperature · Injection enhancement effect · Field-stop or soft punch-through structures · MOS gate thyristors · Power rectifiers

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13.1 Introduction

Nowadays, there are a wide range of power electronics converters, utilized in vehicles, heavy industry, power supply, and home appliances. These converters, which are indispensable for achieving an energy efficiency society, can be classified into four types such as AC-to-DC, DC-to-DC, DC-to-AC, and AC-to-AC conversions. Power electronics technologies enable the conversion of electrical energy. AC-to-AC conversion is mostly performed by rectifier and inverter circuits connected in series, though there are a few exceptions, such as direct conversion using matrix converters. Hence, converters have usually one DC link, in which the energy is stored temporarily. Based on the DC link, the converters can be further classified into two types, a current source converter and a voltage source converter [2].

In the case of a current source converter, the power devices must have blocking capability in both reverse and forward direction. The reverse blocking capability is achieved by connecting or integrating diodes in series with switching power devices in actual applications, but high forward conducting dissipation must be tolerated in this case. Since the converter is suitable for extremely high-power applications, some high-power converter still utilized symmetrical devices like a gate commutated turn-off thyristor in the current source converter with high power capability. Since a current source converter utilizes inductors to store energy, and operate with an almost constant current in the DC link, the main advantage is fault tolerance in the case of short circuiting.

Voltage source converter, on the other hand, needs a reverse conducting power semiconductor device because it operates inductive loads at the AC terminal. When power semiconductor devices turn off the current, a free-wheeling path is required to avoid generating a high voltage spike, which may lead to destructive device failure. This reverse conducting or free-wheeling operation of the power device can be achieved by connecting or integrating an anti-parallel diode for switching the power devices. Therefore, unlike in the case of current source converter, no additional diode is in series with the power device, and additional forward voltage drop does not take place in the current path of the converter. Therefore, though a voltage source converter requires protection against load short circuiting, it shows more efficiency than current source converter. Therefore, voltage source converter is more popular in modern power electronics applications.

Many kinds of power semiconductor devices have been developed and manufactured thus far, and each device structure exhibits specific advantages. The current power device structures are thyristors, bipolar transistors, metal-oxide-semiconductor field-effect-transistors (MOSFETs), and insulated gate bipolar transistors (IGBTs). Figure 13.1 shows the range of power semiconductor devices and their applications. It is clear from this figure that power devices are required for applications that operate over a wide range of current and voltage levels. In voltage levels of relatively low (<300 V), typical applications are power supply for personal computers and automotive applications. Silicon power MOSFETs give the best performance for the applications due to their low on-resistance and fast switching characteristic. In the case of higher power levels, where the operating voltage is from 600 to 6500 V, typical examples are home appliances, heavy industry utilizing motors, and electric vehicle drives. In silicon power MOSFETs, the on-resistance is so high that the devices cannot be used in these applications, which instead utilize silicon IGBTs. HVDC transmission and power lines are typical examples of applications with extremely high power levels, where the operating voltage is in excess of 6500 V; and here, silicon thyristors still provide the best performance. It is worth noting that silicon MOSFETs and IGBTs are mostly seen in voltage-controlled devices with high voltage current saturation features, in modern power electronics applications. Voltage-controlled operation and high voltage current saturation features are attractive for their easy drive and ability to protect power semiconductors from accidental load short circuiting; therefore, through the utilization of MOSFETs and IGBTs, voltage source converters have been widely used over a broad power range.

An ideal power device must enable to control power to loads without power loss. The delivered power is often controlled by periodically activating the power device. In an ideal power device, the forward voltage drop is zero, leading to no power loss. Likewise, the there is no leakage current in the device during the off-state, leading to no power loss. Moreover, it is assumed that an ideal power device switching between the on-state and off-state in a flash, leading to no power dissipation. MOSFET and IGBT use depends on the required voltage and current levels of the power device in question. Among low-power applications, power supply for battery chargers and electronic ballasts in lighting systems represents a major global market. In automobile applications, many small drives are fed from 12 or 24 V on-board power sources; thus, MOSFETs are most common in these applications. IGBTs are suitable, on the other hand, for medium- and high-power applications, such as consumer and industrial applications that use motors, and electric vehicle drives, with further applications being high-power motor drive in traction for railway cars. The IGBT structure exhibits MOS-bipolar integration, combining the MOSFET physics with the bipolar transistor operation. In IGBT operation, the n-channel (n-ch) MOSFET is utilized to supply the base current for the wide-base pnp bipolar transistor, to be in conductivity modulation of the n-drift region of the MOSFET; thus, IGBT devices can achieve greatly reduced on-resistance. One notable result is that the bipolar transistor structure can be modified to form a wide-base pnp transistor in the IGBT structure, and the

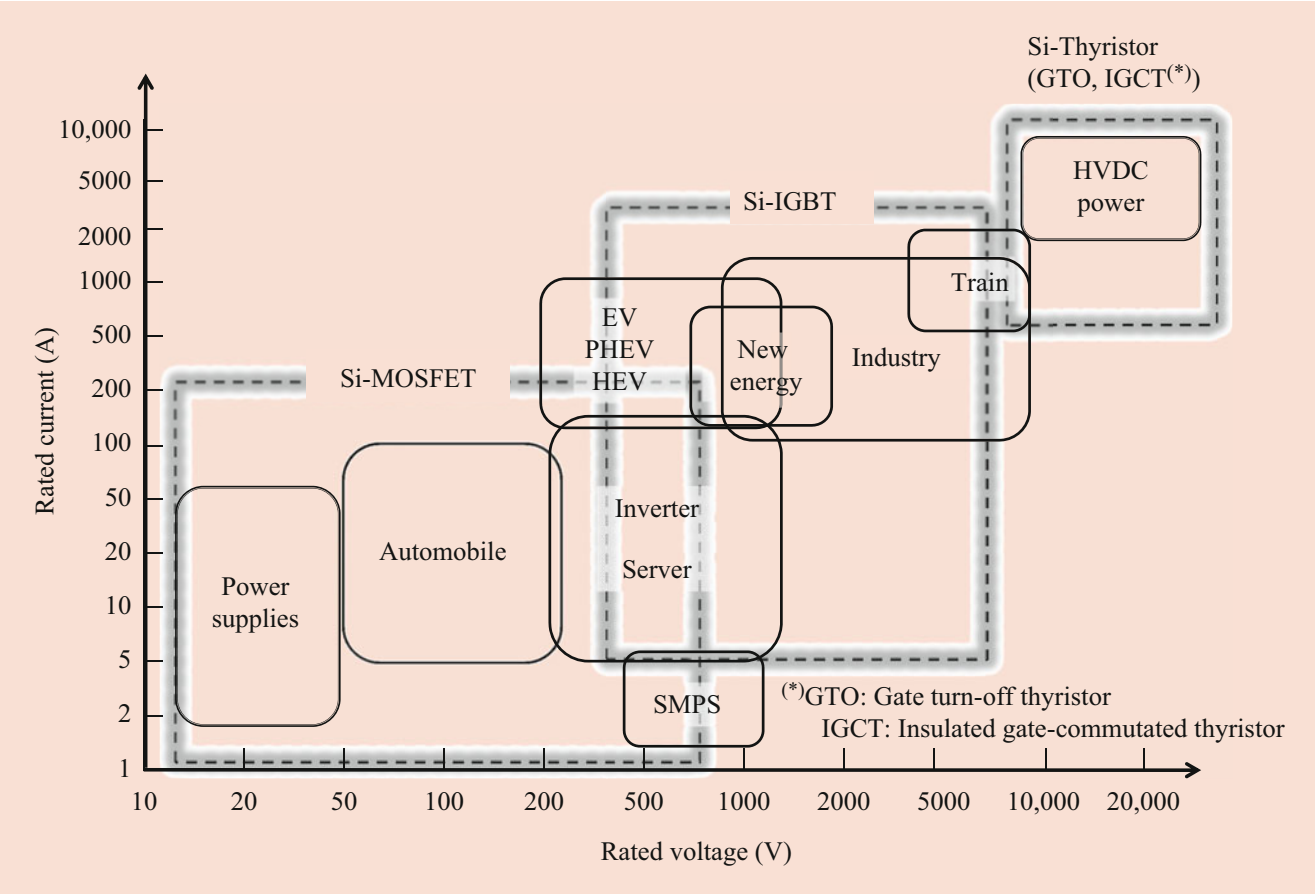


Fig. 13.1 Power semiconductor devices and their applications

withstanding capability of the IGBT can be improved; thus, as aforementioned, many IGBTs with a breakdown voltage of 400–6500 V have been manufactured and utilized in a variety of applications.

In this chapter, the author focuses on the device structure, operation, and design concept of silicon power devices with diodes, MOSFETs, IGBTs, or MOS-gated thyristors and the features of such unipolar and bipolar devices. In addition, it will present a brief history of the devices' development and summarize the state-of-the-art structures and characteristics of silicon MOSFET and IGBT devices.

13.2 Power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs)

Silicon power MOSFETs are power device structures designed to handle high electric power with fast switching characteristics and are widely used in contexts such as switching power supply and DC-DC converters, in the relatively low breakdown voltage region from roughly 20 to 300 V. With the recent development of new structural devices, however, the breakdown voltage range has been expanded to about 700 V and more. Power MOSFETs will continue to play a leading role in supporting high-efficiency operation of power electronic devices, as their element structures evolve.

13.2.1 Power MOSFETs

There have been many unipolar power devices, such as junction field effect transistors (JFETs) and static induction transistors (SITs) [3]; but, these have not been utilized for many power electronics applications because these show a normally on operation. Power MOSFETs can be classified into depletion and enhancement mode types. In a depletion mode MOSFET, the gate threshold voltage V_{th} is below zero volts, the device is normally on, and it cannot block the leakage current at gate voltage $V_{gs} = 0$. In the enhancement mode MOSFET, the gate threshold voltage is positive, the device is normally off, and it blocks the leakage current at $V_{gs} = 0$. In addition, when V_{gs} is set higher than the threshold voltage V_{th}, an inversion layer is formed.

Enhancement mode power MOSFETs are mainly utilized in power electronics because of their normally off characteristics; and n-channel MOSFETs, in particular, are utilized

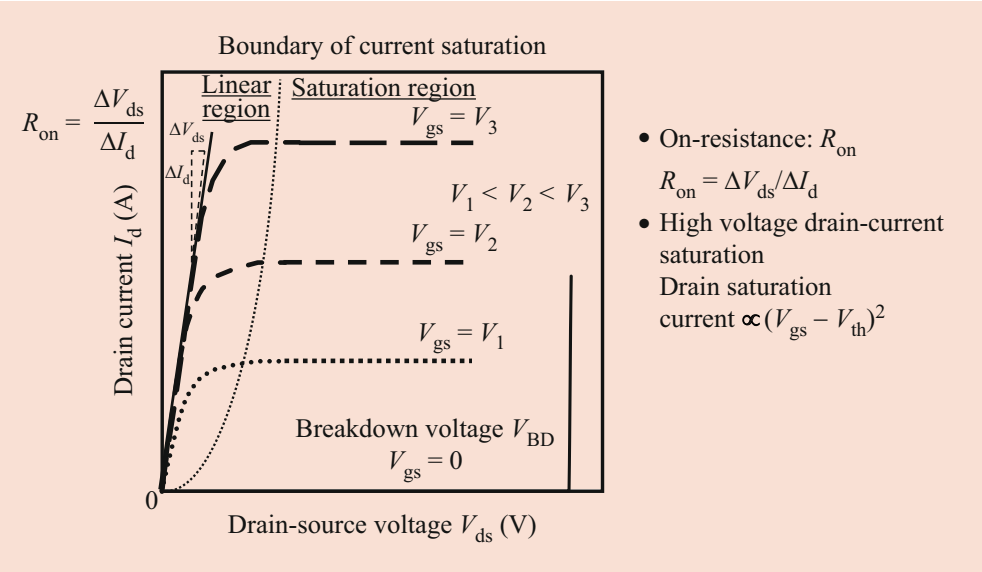


Fig. 13.2 Current and voltage characteristics of typical MOSFET

because the electrons mobility is much higher than holes mobility. The gate threshold voltage V_{th} of a silicon power MOSFET is typically adjusted to between about 2 V and 4 V at room temperature; and power MOSFETs typically exhibit a low on-state voltage drop and a negligible off-state leakage current level. Further, they exhibit power loss during transition between the on- and off-state. The current and voltage characteristics of a typical power MOSFET are shown in Fig. 13.2. We can see that the "breakdown voltage" has a finite level. The typical MOSFET can operate with high current and voltage in the active region; and the device exhibits high voltage drain-current saturation, owing to the pinch-off at the channel, which is especially useful in power electronics applications such as motor controls. The basic structures of silicon power MOSFETs and lateral MOSFETs are shown in Fig. 13.3. Lateral DMOSFET (LDMOSFET) transistors are frequently used in several types of power ICs; however, they have the disadvantage of low current capacity because the current flows mainly through the surface of the n-drift region, which occupies a large part of the semiconductor surface.

When higher power levels must be operated by a semiconductor, vertical MOSFETs (VDMOSFETs) are often employed, with control being achieved by establishing a vertical region for the electric field. As a result, the overall semiconductor region is efficiently used, and the MOSFET surface can be utilized for the striped, square, or hexagonal cells formation. Vertical power MOSFETs were developed in the middle of 1970s, for improved characteristic compared to silicon bipolar power transistors, which suffered from low current gain (or base-to-collector current amplitude factor) when designed to show high blocking voltage. Further, the

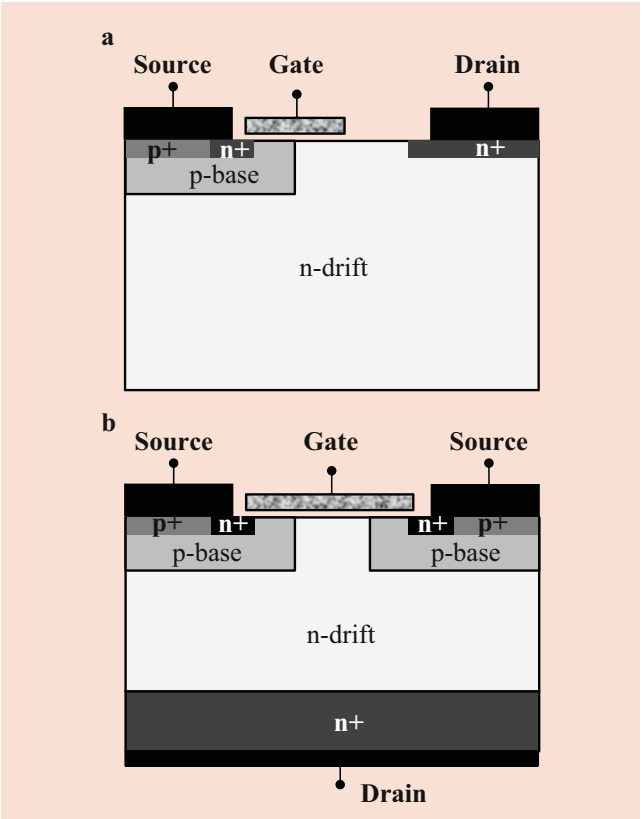


Fig. 13.3 Cross section of (**a**) LDMOSFET and (**b**) VDMOSFET structures

bipolar transistors cannot be switched in high frequency operation, because of the large storage time resulting from the injected and stored charges in the drift regions. So,

replacing current-controlled devices with voltage-controlled varieties was thus attractive from the application point of view. Vertical power MOSFETs are further divided into low breakdown voltage (approximately 200 V or less) and high breakdown voltage (200 V or more) devices.

Three types of MOSFETs (LDMOSFETs, vertical DMOSFETs with low breakdown voltage, and vertical DMOSFETs with high breakdown voltage) were independently developed in pursuit of performance improvement. Two common targets for such improvement are reduction in the drain-source on-resistance and reduction in the gate-source and gate-drain capacitances; with the former aimed at minimizing power loss in the device conduction state, and the latter necessary for reducing power loss during high-speed switching. In addition, efforts are made to ensure breakdown tolerance and reliability.

The power MOSFET was developed with a V-groove structure in which the channel is formed along (111) crystallographic planes [4]. U-groove structures were also designed and fabricated via a similar processing technique. The difference is that, in the fabrication of the U-groove structure, the anisotropic etching process is halted prior to the formation of a V-groove [5]. Improved current spreading and reduced electric fields are advantages of the U-grooved structure. The fabrication process and structure of the U-groove MOSFET differs from those of the UMOSFET and trench MOSFET, described below and in Sect. 13.2.3, respectively. As a next stage, vertical planar double-diffused structures were developed, which achieved a higher packing density than the V-groove and U-groove structures, without the need for a three-dimensional structure. These successful vertical power MOSFETs, created using the double-diffused process, and referred to as vertical DMOSFETs (or VDMOSFETs), were introduced in the market in the 1970s [6]. In them, the p-base and n+ source regions are formed to be self-aligned to the edge of the gate polysilicon layer, utilizing boron and phosphorous (or arsenic) ion implantation followed by the respective annealing and drive-in process. The MOSFET channel is defined by the difference in the lateral diffusion length of the implanted dopants under the gate electrode, and the MOSFET can sustain positive-bias voltage to the drain electrode by the p-n junction of p-base and n-drift layer. The blocking voltage is primarily determined by the doping concentration and thickness of the n-drift layer. Low-voltage MOSFETs have low on-resistance, but the resistance in n-drift layer increases rapidly with the blocking voltage; therefore, the operation of silicon power VDMOSFETs is limited to a blocking voltage of roughly 700 V or less in modern power electronics applications.

To enhance the operational capability of drain current in the VDMOSFET, its components of resistance were reduced through the use of many advanced structural designs involving finer cell dimensions. However, it soon became clear that the devices contained fundamental parasitic resistances that blocked more improvement in reducing the resistance. Thus, during the 1980s, a superior device structure was developed, based on the technology for trench structure that had developed for DRAM (dynamic random access memory). The name "UMOSFET" is derived from the device's gate structure with U-shaped geometry, but the term "trench MOSFET" is also frequently utilized. According to [7], the silicon UMOSFET became commercially available in the late 1980s. The UMOSFET structure can increase channel density significantly and eliminate the contribution of JFET resistance, leading to great enhancement of low-voltage (<200 V) MOSFET performance.

The on-resistance in these devices becomes dominant, due to the high resistance of n-drift region, when the breakdown voltage is designed to exceed about 500 V. In MOSFET with high breakdown voltages, its on-resistance typically exceeds 50 mΩ cm^2 and an on-state voltage drop is more than 1.0 V. To overcome this, IGBTs were born in the 1980s, for use in medium- and high-voltage/current power electronics apparatus. The superior characteristics of IGBTs in medium- and high-voltage applications resulted in MOSFET use focusing on application field with an operation voltage of less than roughly 200 V.

Silicon superjunction (or SJ) MOSFETs, which utilize charge coupling, have enabled an extension of the power MOSFET breakdown voltage to the 600–700 V level; and a heavily doped drift region in the SJ-MOSFET can be utilized, in comparison with the VDMOSFET and UMOSFET. The latter factor enables to reduce resistance in n-drift region resistance greatly in devices capable of sustaining high drain voltage. To achieve a superior charge coupling characteristic, the n-type and p-type drift regions must be in a complete depletion when the drain voltage increases and gets closer to the breakdown voltage, and the SJ design has been attractive in high breakdown voltage devices in excess of 500 V.

13.2.2 The VDMOSFET Structure

Figure 13.3b shows a cross-sectional view of VDMOSFET. A vertical device structure was developed to achieve high operational current capability by placing electrodes on both a top and bottom surfaces of the wafer. Device fabrication begins with an n-epitaxial layer grown on an n+ substrate with high impurity concentration. As aforementioned, the term "VDMOSFET" is derived from its vertical structure, with the p-base and n+ source regions formed by n-type and p-type doping through the same photomask opening, followed by thermal diffusion. The p-base and n+ source regions are self-aligned to the left- and right-hand sides of the gate electrode during ion implantation. The channel is

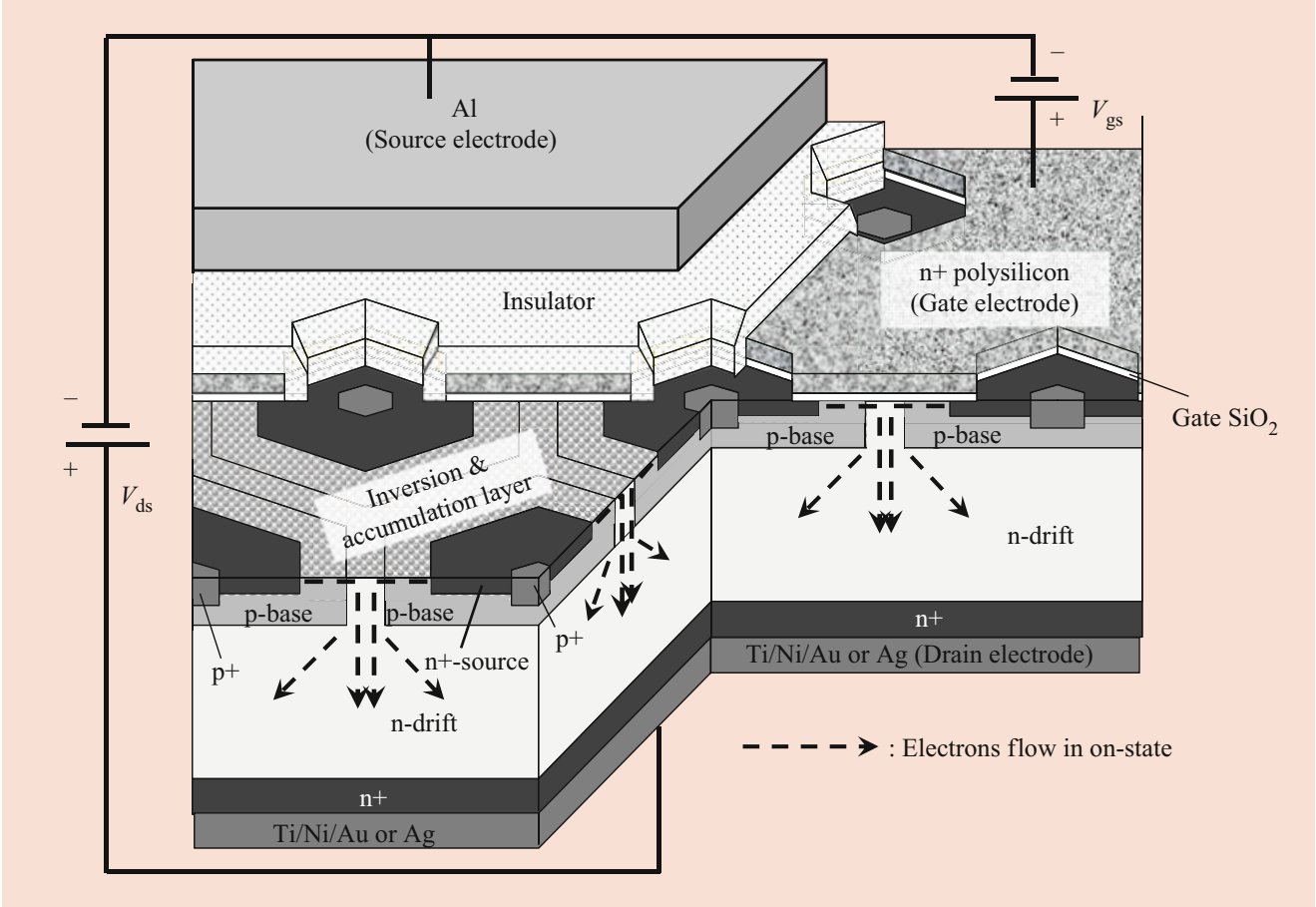


Fig. 13.4 Schematic bird's eye view of VDMOSFET structure in a hexagonal form arranged in a hexagonal pattern

defined by the extension difference in lateral diffusion of the p-base and n+ source regions. The p-base region is connected to the source electrode such that the parasitic npn transistor (n+ source/p-base/n-drift) is completely shorted. To ensure very low resistance in the short region, the doping concentration is increased by adding a p+ implanted region, followed by the thermal diffusion. In addition, an n+ doped polysilicon gate is used to enable the fabrication of devices that allow diffusing the dopants under a gate electrode at high temperatures. The VDMOSFET consists of a MOSFET fabricated on an n-drift region, with the thick n+ substrate, and can sustain a high voltage across the p-n junction of p-base and n-drift region.

A main current must flow through the inversion layer; therefore, a lot of individual cells are formed to extend the width of the MOS channel. Figure 13.4 shows an example. Here, the individual cells are hexagonal and set up in a hexagonal pattern; a design that has been utilized even more effectively in so-called HEXFET structures [8].

Blocking Characteristics

In the off-state, the blocking voltage is sustained by not only the p-n junction of the p-base and n-drift regions, but also the MOS capacitor, consisting of the gate and the drift region. A blocking voltage can be determined when the peak electric field reaches equal to the critical field for breakdown at the reverse biased p-n junction. In this case, it is important that an operation of the parasitic npn bipolar transistor is completely suppressed by the shorted p-base and n+ source regions via the source electrode, as shown in Fig. 13.3. Further, we have to pay attention that a large leakage current could take place if the depletion layer in the p-base region extends and touches the n+ source region (reach-through). To avoid this "reach-through" phenomenon, the thickness and doping concentration of the p-base region must be carefully designed [6].

If the doping is assumed to be uniform on both sides, the positive bias to the drain electrode is sustained by the p-n junction (the p-base/n-drift region), with a triangular-shaped electric field (Fig. 13.5). The peak of electric field is located

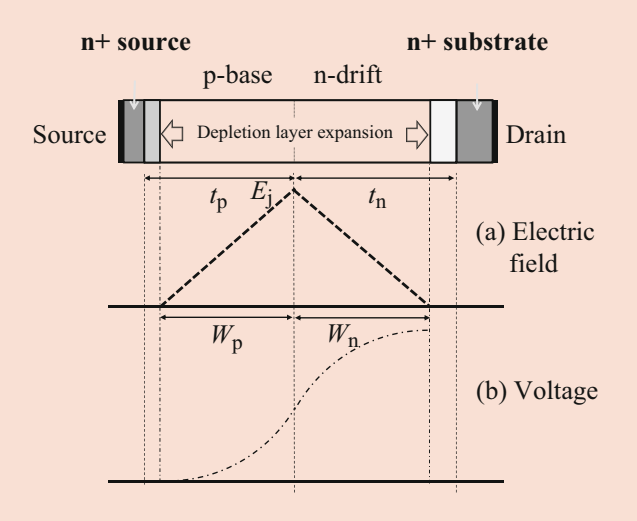


Fig. 13.5 Triangular electric field and voltage distribution at p-base/n-drift junction in a power VDMOSFET structure

at the junction, and the depletion layer width in the p-base region W_p is given by

$$W_p = \frac{\varepsilon_s E_j}{qN_A}, \tag{13.1}$$

where E_j is the maximum field, N_A is the doping density in the p-base region, q is the charge on the electrons, and ε_s is the dielectric constant. The minimum p-base thickness required to prevent the breakdown due to the reach-through can be calculated with the assumption that the E_j at the junction becomes the critical field for breakdown E_c:

$$t_p = \frac{\varepsilon_s E_c}{qN_A}. \tag{13.2}$$

In [6], the minimum thickness of p-base region for silicon power MOSFETs was calculated and compared with that for 4H-SiC MOSFETs; and it was found that the thickness for silicon was roughly six times less than for 4H-SiC, implying that the channel length for silicon MOSFETs is much less than for SiC MOSFETs, leading to decreased on-resistance. Increasing the doping concentration reduces the minimum thickness of the p-base region for preventing the reach-through breakdown; however, the p-base region with the higher doping concentration results in increase of the threshold voltage and decrease of the mobility of the inversion layer.

Assuming that the p-base layer concentration is much higher than the n-drift layer one (see Fig. 13.6), the following equation holds in the p-n junction of the p-base and n-drift layers:

$$\frac{d^2V}{dx} = -\frac{dE}{dx} = -\frac{qN_D}{\varepsilon_{Si}}, \tag{13.3}$$

where $V(x)$ is the voltage distribution in the device, and N_D is the donor concentration in the n-drift layer. This is Poisson's equation for a single-step junction. When this equation is integrated with respect to distance x, to obtain the electric field $E(x)$, based on the boundary condition $E(W_{dep}) = 0$, the electric field $E(x)$ can be expressed as

$$E(x) = -\frac{qN_D}{\varepsilon_{Si}}\left(W_{dep} - x\right), \tag{13.4}$$

where W_{dep} is the depletion layer width. Further, integrating the above equation for x, voltage $V(x)$ can be obtained based on the boundary condition of $V(0) = 0$:

$$V(x) = \frac{qN_D}{\varepsilon_{Si}}\left(W_{dep}x - \frac{x^2}{2}\right). \tag{13.5}$$

When the applied drain voltage V_{ds} is sufficiently high, and the built-in potential of p-n junction is low enough to be ignored, the V_{ds} and depletion layer width W_{dep} can be given by

$$V\left(W_{dep}\right) = V_{ds} = \frac{qN_D W_{dep}^2}{2\varepsilon_{Si}} \tag{13.6}$$

and

$$W_{dep} = \sqrt{\frac{2\varepsilon_{Si}V_{ds}}{qN_D}}. \tag{13.7}$$

Thus, the breakdown voltage V_B of a power MOSFET is given using the depletion layer width $W_{dep,B}$ under the breakdown, as

$$V_B = \frac{E_c \times W_{dep,B}}{2} \tag{13.8}$$

and

$$W_{dep,B} = \sqrt{\frac{2\varepsilon_{Si}V_B}{qN_D}}. \tag{13.9}$$

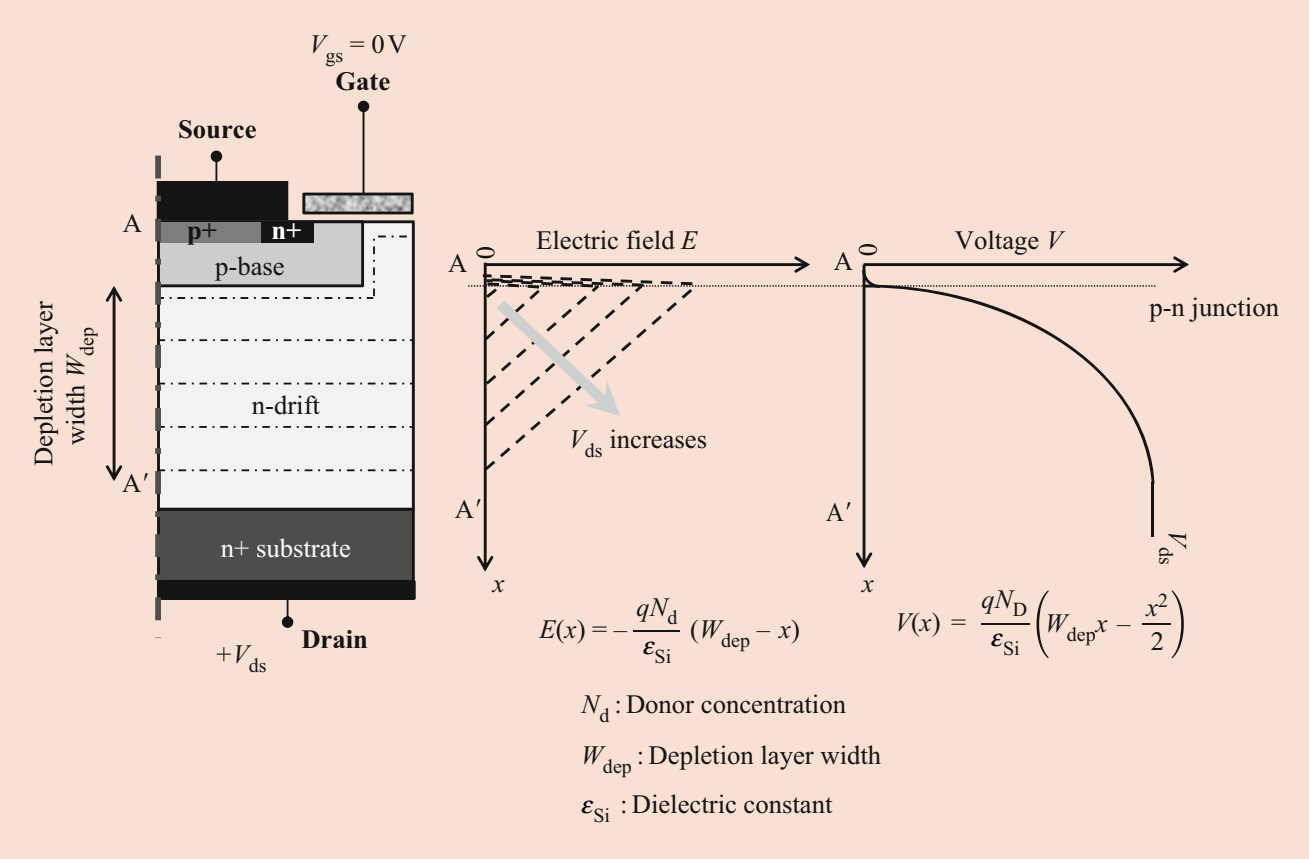


Fig. 13.6 Electric field and voltage distributions and depletion layer expansion in a VDMOSFET forward-blocking state

Using Eqs. 13.8 and 13.9, the breakdown voltage V_B of a power MOSFET is obtained:

$$V_B = \frac{\varepsilon_{Si} E_c^2}{2qN_D}. \tag{13.10}$$

This equation shows that the breakdown voltage V_B is proportional to the reciprocal of the impurity concentration N_D in the n-drift layer; thus, this concentration should be reduced to increase the MOSFET breakdown voltage. However, reducing N_D leads to the increase of on-resistance of the MOSFET, meaning that, in power MOSFETs, the breakdown voltage and on-resistance are in a trade-off relation.

Threshold Voltage

The VDMOSFET threshold voltage is an important design parameter for applications. The threshold voltage must be kept at 1–2 V and more for most power electronics systems, to provide the characteristics of being unaffected against turn-on owing to voltage spikes caused by disturbance signals and noise. At the same time, a high threshold voltage is undesirable, because the voltage for inducing the inversion layer in the MOSFET channel is defined by $V_{gs} - V_{th}$, where V_{gs} is the gate bias and V_{th} is the threshold voltages. In most power electronics systems designed for high-voltage operation, a gate voltage is set of 15 V, meaning that the threshold voltage should be maintained less than 5 V, for example, to obtain a low resistance from the MOSFET channel.

The threshold voltage can be expressed by modeling it as the gate voltage at which the strong inversion layer begins to form in the MOSFET channel. The voltage is given by

$$V_{th} = \frac{\sqrt{4\varepsilon_s kTN_A \ln\left(\frac{N_A}{n_i}\right)}}{C_{ox}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right), \tag{13.11}$$

where C_{ox} is the specific capacitance of the oxide in the MOS structure, N_A is the p-base doping concentration, k is Boltzmann's constant, n_i is the intrinsic carrier concentration, and T is the absolute temperature [6]. When there is an effective positive charge in the oxide (Q_{ox}), which is assumed to be located at the metal-oxide interface [6], the threshold voltage shifts to negative and given by

$$\Delta V_{th} = -\frac{Q_{ox}}{C_{ox}} \tag{13.12}$$

In addition, by utilizing highly doped n+ polysilicon as the gate electrode, a further negative threshold voltage shift can be achieved.

The threshold voltage in a VDMOSFET decreases with temperature because of an increase in the n_i. The dependence of the threshold voltage on temperature was analyzed in detail in [6]. According to [6], the threshold voltage varies by a factor of roughly two, over the temperature range of −50 to 200 °C. This threshold voltage decrease at elevated temperatures must be considered in VDMOSFET design.

On-Resistance

The on-resistance of a VDMOSFET is expressed as the total amount of MOSFET channel resistance plus the n-drift region and substrate resistance. The drain current in a VDMOSFET is provided by the positive gate bias, which induces an inversion layer at the surface of the p-base region under the gate electrode, resulting in a formation of electron path from the n+ source to the n+ substrate in a positive drain voltage application. After flowing through the inversion layer, the electrons reach the n- drift region at the upper region of the MOSFET, where they flow through a limited space of JFET region between p-base regions. This constriction of the electron flow through this region increases the JFET resistance considerably, and design optimization such as the width between the p-base regions is required to lower the overall resistance of the MOSFET. Further, the higher doping concentration in the JFET region is typically utilized to increase the conductance for flowing electrons through this section. After transportation through this region, the electrons reach the n-drift region and flows below the p-n junction, and the electrons spread toward the entire n-drift region of the cell. This non-uniform electron transportation in the n-drift region increases the resistance, making the on-resistance of the VDMOSFET greater than the ideal level of on-resistance in the n-drift region; and this increased internal resistance has encouraged the development of trench power MOSFETs and superjunction MOSFETs.

Figure 13.7 shows the VDMOSFET structure. In this figure, components of its internal resistance are also shown [6]. There are eight resistances components and these must be investigated, in order to find the total on-resistance between the source and drain electrodes. The total on-resistance for a VDMOSFET is obtained by totaling these resistances:

$$R_{ON} = R_{CS} + R_{n+} + R_{ch} + R_{acc} + R_{JFET} + R_D + R_{SUB} + R_{CD}. \quad (13.13)$$

The goal is to achieve a minimization of the on-resistance while keeping a specific blocking voltage, and this involves optimizing the device design parameters, such as the doping density, and the thickness and dimensions of each layer and

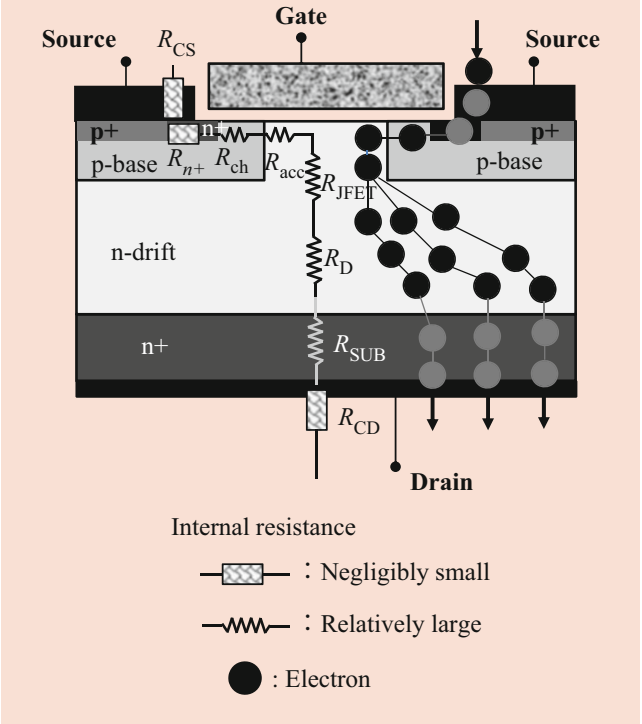


Fig. 13.7 Internal resistances and electron flow path in VDMOSFET structure

region. Further, a comprehensive study must include the two-dimensional effects because of current crowding and field concentration. The former corresponds to the end of the inversion layer as electrons spread into the JFET region and the bottom edge of the JFET region as electrons spread into the n-drift region. Field crowding takes place, in the forward blocking mode, at the corners of the p-n junction of p-base and n-drift region in the vertical transistor cell, and at the edge termination region of the VDMOSFET. These two dimensional effects are commonly analyzed through TCAD (technology computer aided design) device simulations. The pursuit of minimal resistance, minimal area, and keeping the blocking voltage has led to the development of several innovations that have been utilized in modern silicon power MOSFETs; among them, a self-aligning sub-micron MOS channel, a JFET region with higher doping concentration, p-base contacts that are segmented along the three dimensional direction of the stripe cells, and the fine pitch trench-gate structure. The resistances of the source contact (R_{CS}), n+ source region (R_{n+}), and drain contact (R_{CD}) are negligibly small in the VDMOSFET. Figure 13.8 shows the relative contribution of various resistance components in a 30 V and 600 V VDMOSFET with planar gate cells [9]. The resistance of package (R_p) is included in this figure. In MOSFETs with a blocking voltage below 50 V, many attempts are made to minimize the MOSFET channel resistance by improving the

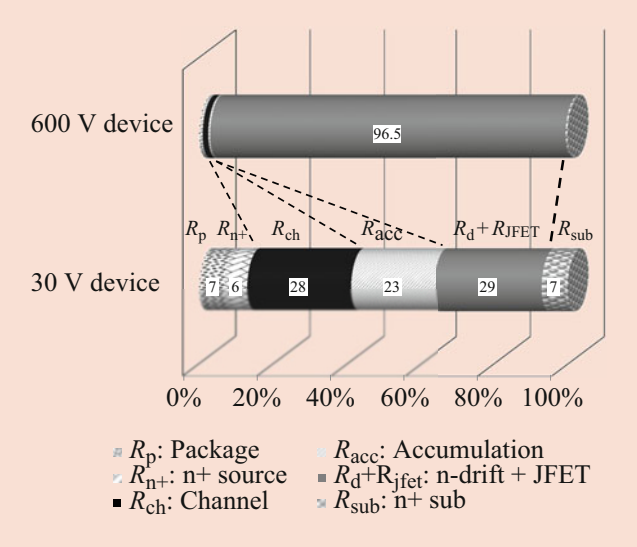


Fig. 13.8 Relative contribution to on resistance in devices of different voltage rating

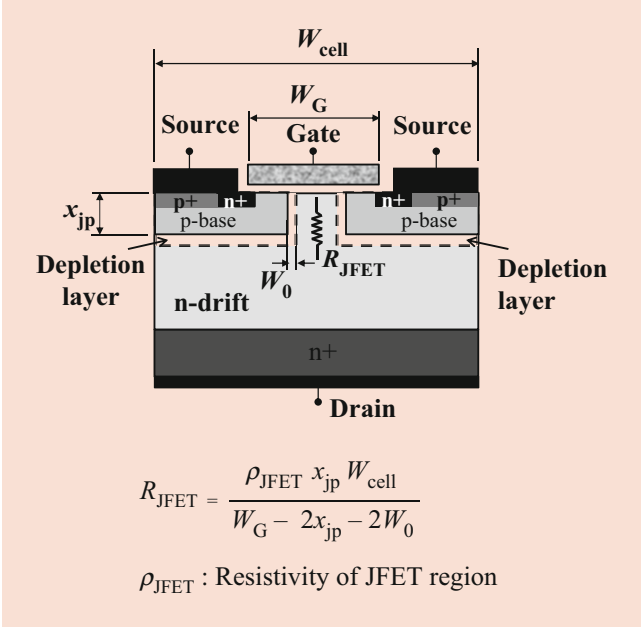


Fig. 13.9 VDMOSFET structure for modeling the JFET resistance

components near the device surface through the cell density enhancement.

The resistance R_D of the n-drift region with low doping concentration is given by

$$R_D = \frac{W_D}{q\mu_n N_D}, \tag{13.14}$$

where W_D is the thickness of the n-drift layer, N_D is the doping concentration of the n-drift region, and μ_n is the electron mobility.

The depletion layer width under the breakdown is expressed by

$$W_{dep,B} = \frac{2V_B}{E_C}, \tag{13.15}$$

where V_B is the breakdown voltage. The doping concentration of the n-drift layer to obtain this breakdown voltage is expressed by

$$N_D = \frac{\varepsilon_s E_C^2}{2qV_B}, \tag{13.16}$$

where q is the charge on the electrons. From these equations, the on-resistance of the n-drift region is calculated:

$$R_D = \frac{4V_B^2}{\varepsilon_s \mu_n E_C^3}. \tag{13.17}$$

The denominator in Eq. 13.17 is usually referred to as Baliga's Figure of Merit for power devices [10], a number showing the effect of the material properties of semiconductor on the resistance of the drift region. If the device is designed for higher voltages, W_D must be set higher and N_D must be lower.

The resistance in the JFET regions is an important component when a MOSFET is designed with fine cell structure. The JFET resistance was modeled using the schema in Fig. 13.9 and is given by [11]

$$R_{JFET} = \frac{\rho_{JFET} x_{jp}\, W_{cell}}{W_G - 2x_{jp} - 2W_0}, \tag{13.18}$$

where ρ_{JFET} is the JFET region resistivity, x_{jp} is the diffusion depth of the p-base region, W_{cell} is the unit cell width of the MOSFET, W_G is the width of the gate electrode, and W_0 is the depletion width at the zero bias. From this equation, it is clear that use of a more heavily doped JFET region (as described above) to reduce ρ_{JFET} and a shallow p-base region to lower the values of x_{jp} is an effective method for improving JFET resistance.

The specific on-resistance in the channel in a VDMOSFET is given by

$$R_{ch} = \frac{L_{ch} W_{cell}}{2\mu_{nch} C_{ox} (V_G - V_{th})}, \tag{13.19}$$

where μ_{nch} is the channel mobility, C_{ox} is the specific capacitance of the MOS, L_{ch} is the channel length, and W_{cell} is the unit cell width. According to [11], for example, in 30 V VDMOSFETs used for power supply applications, when the gate oxide thickness is set at 0.05 μm, the threshold voltage is 2 V, and a channel mobility of 450 cm^2/Vs is assumed, the calculated on-resistance in the channel is 0.245 $m\Omega\ cm^2$ when the gate voltage is set to 10 V (at $W_{cell} = 12\ \mu m$).

Switching Characteristics

Since power MOSFETs are unipolar devices, fast switching can be achieved (unlike in the case of IGBTs), due to the absence of minority carrier accumulation. The switching characteristics of power MOSFETs are strongly dependent on the gate circuit and the kind of connected loads. To activate the devices, the MOS capacitance must be charged by a gate voltage higher than a threshold voltage of V_{th}. To deactivate them, it is necessary to extract the charge accumulated in the MOS capacitance. Therefore, the switching speed of power MOSFETs is characterized by the rapidity with which the MOS capacitance is charged and discharged, and reducing the gate resistance and MOS capacitance is effective for improving the switching characteristics. Figure 13.10 shows the parasitic capacitance in a power MOSFET. The input capacitance C_{iss}, output capacitance C_{oss}, and reverse transfer capacitance C_{rss} are defined as follows:

$$C_{iss} = C_{gs} + C_{gd}, \tag{13.20}$$

$$C_{oss} = C_{gd} + C_{ds}, \tag{13.21}$$

$$C_{rss} = C_{gd}, \tag{13.22}$$

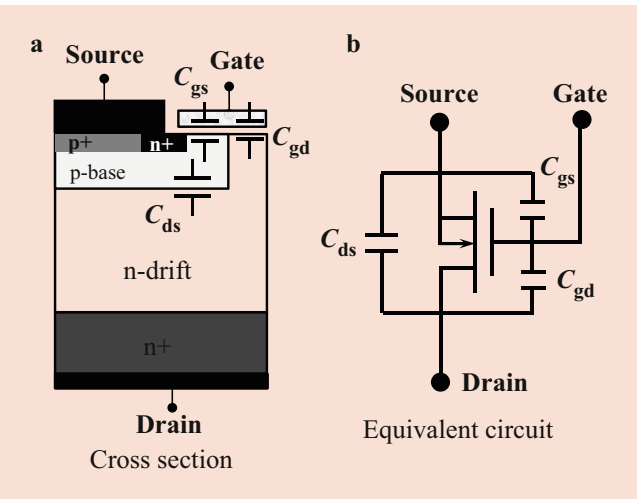


Fig. 13.10 Parasitic capacitance in VDMOSFET structure. (a) Cross section. (b) Equivalent circuit

where C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance, and C_{ds} is the drain-source capacitance. The C_{iss}, C_{oss}, and C_{rss} have nonlinear characteristics with respect to the drain voltage, and these values increase when a low drain voltage is applied. In power MOSFETs, the gate voltage and drain voltage waveforms are completely opposite to each other; the C_{rss} impedes charging through the C_{iss} by feeding back to the gate voltage waveform; and as a result, the effective capacitance during this switching period increases. Figure 13.11 shows the schematic gate charge waveform when a MOSFET is activated. Initially, the MOSFET is assumed to be in an off-state with a full line voltage of V_{ds} applied across the drain-source electrode. At time zero, the gate current starts to flow in the device. The C_{iss} is charged at a constant rate:

$$\frac{dV_{gs}}{dt} = \frac{I_g}{C_{iss}} = \frac{I_g}{C_{gs} + C_{gd}}, \tag{13.23}$$

where I_g is the gate current. When the drain-source voltage is high, the C_{iss} is similar to the C_{gs}; therefore, the gate current I_g is used for charging the C_{gs} in this initial period. When the V_g reaches the gate threshold voltage V_{th}, the MOSFET operates in its active region and the drain current starts to flow. The drain current I_d in this period can be expressed as

$$I_d = g_m \left(V_{gs} - V_{th}\right), \tag{13.24}$$

where g_m is the transconductance, which is defined by

$$g_m = \frac{\partial I_d}{\partial V_{gs}}. \tag{13.25}$$

When the drain current increases and gets to the load current I_{load}, the drain voltage V_{ds} starts to fall. Thus, the constant gate current discharge of the reverse transfer capacitance (or Miller capacitance) C_{rss} is given by

$$\frac{dV_{ds}}{dt} = -\frac{I_g}{C_{rss}}. \tag{13.26}$$

After this, the C_{rss} increases with decreasing drain voltage V_{ds}. When the drain voltage falls to the level of the on-state voltage, the gate voltage starts to increase, and continues to increase as long as the gate current I_g flows. During this period, dV_{gs}/dt decreases due to the increase in C_{gd}. Figure 13.11 shows that the changes in I_d influence the gate-source charge of Q_{gs} and changes in V_{ds} affect the gate-drain charge of Q_{gd}, so that the reduction of C_{rss} (=C_{gd}) is especially important for improving the switching character-

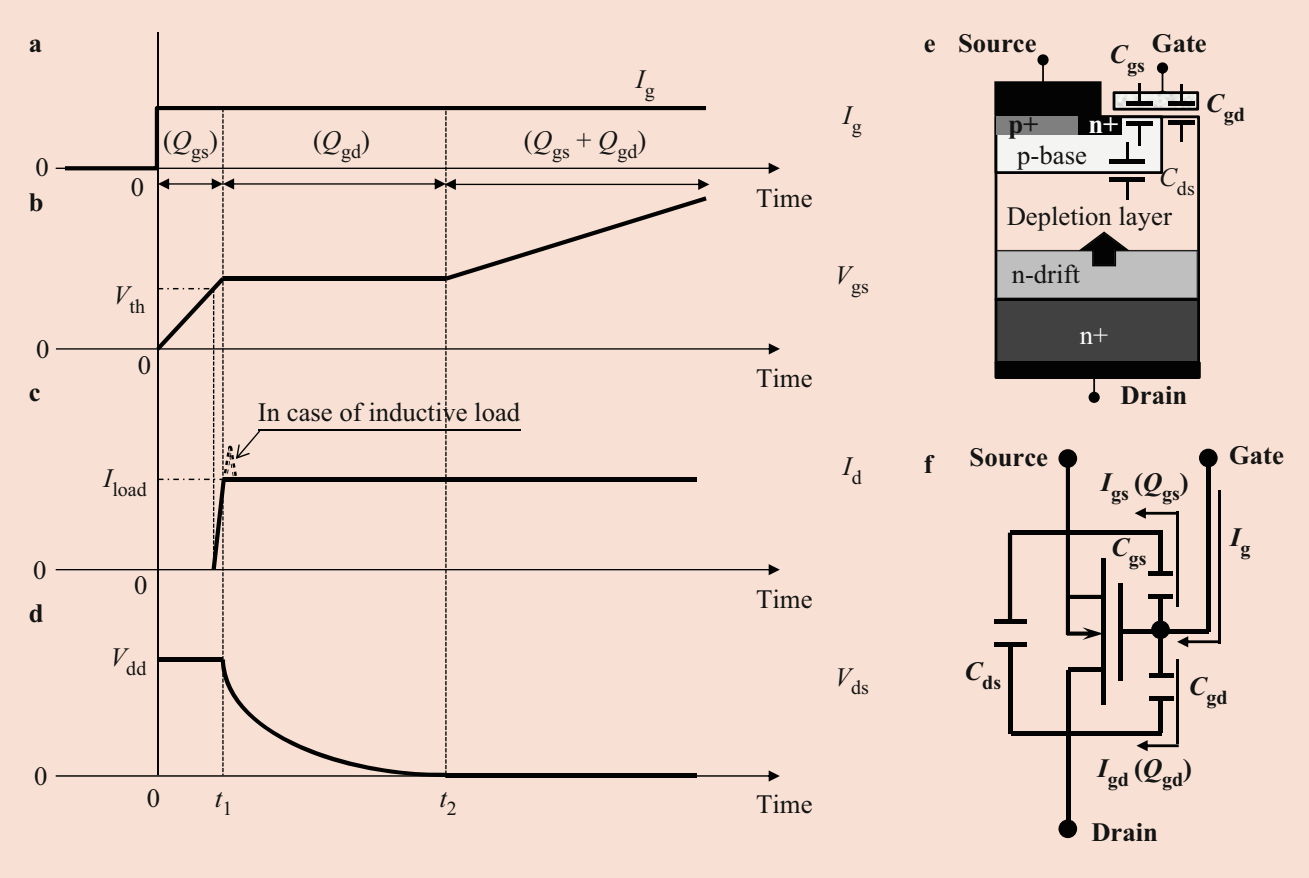


Fig. 13.11 Schematic gate charge waveform at turning on the MOSFET. (**a**) Gate current, (**b**) gate voltage, (**c**) drain current, (**d**) drain voltage, (**e**) depletion layer dynamics (from t_1 to t_2 in (**d**)), and (**f**) gate current flow

istics. The power consumption of the gate drive circuit is expressed by $V_{gs} \times (Q_{gs} + Q_{gd}) \times f$, where f is the switching frequency. When designing gate drive circuits for especially high frequency application, it is very important to minimize the gate charge.

Power MOSFETs are often utilized to control the current in inductive loads for motor control; and their switching operations in such circuits have been analyzed and discussed in several works, such as [6].

The typical circuit configuration is illustrated in Fig. 13.12. The circuit is comprised of the power MOSFET and an inductive load, connected in series with the power source by a free-wheeling diode. The turn-on current and voltage waveforms for an inductive load are shown in Fig. 13.13. With power MOSFET turn-on, the free-wheeling current still flows through the diode. When the gate bias is switched on ("A" in Fig. 13.13), the gate voltage V_{gs} begins to slowly increase due to the capacitance components of the power MOSFET and the connected gate resistance R_g. Since the gate-drain capacitance C_{gd} remains constant owing to the constant drain voltage, the time constant for charging the gate of the power MOSFET is expressed by $R_g \times (C_{gs} + C_{gd})$. Thus, the gate voltage V_{gs} is given by

$$V_{gs}(t) = V_{GS}\left[1 - \exp\left\{-t/R_g\left(C_{gs} + C_{gd}\right)\right\}\right]. \quad (13.27)$$

When the drain-source voltage is high, the C_{iss} $(= C_{gs} + C_{gd})$ is similar to the C_{gs}; therefore, the gate current I_g is used for charging the C_{gs} in this initial period.

The drain current increases while the load is clamped to the source voltage by the conducting free-wheeling diode. When the V_{gs} reaches the threshold voltage V_{th}, the power MOSFET operates in the active region and the drain current starts to flow. In this regime, the MOSFET supports a high drain voltage by expanding the depletion layer in the n- layer ("B" in Fig. 13.13). The drain current density is given by

$$I_d(t) = g_m \times \left(V_{gs}(t) - V_{th}\right) = \frac{\mu_{nch} C_{ox}}{2L_{ch} W_{cell}}\left(V_{gs}(t) - V_{th}\right)^2, \quad (13.28)$$

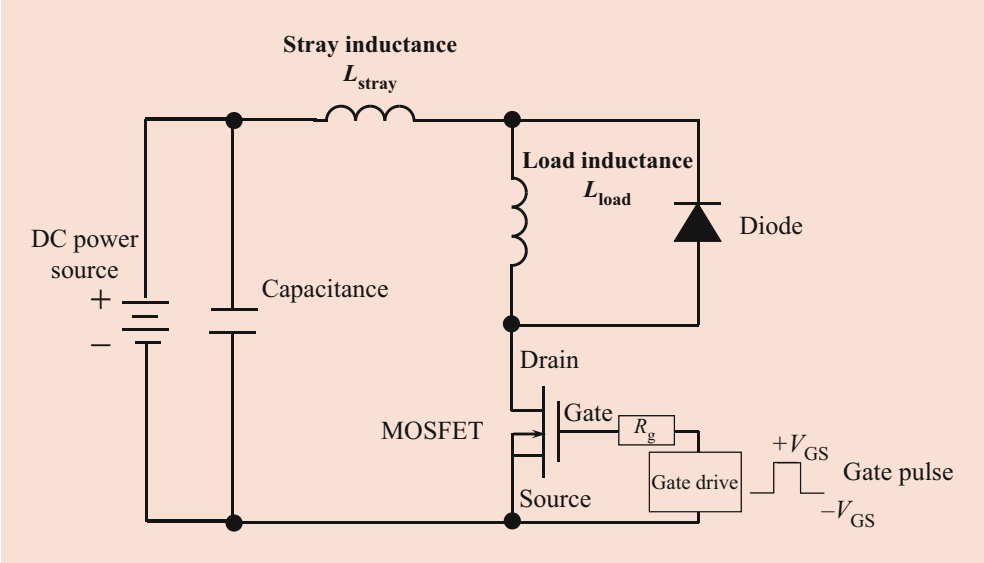


Fig. 13.12 Inductive load circuit configuration

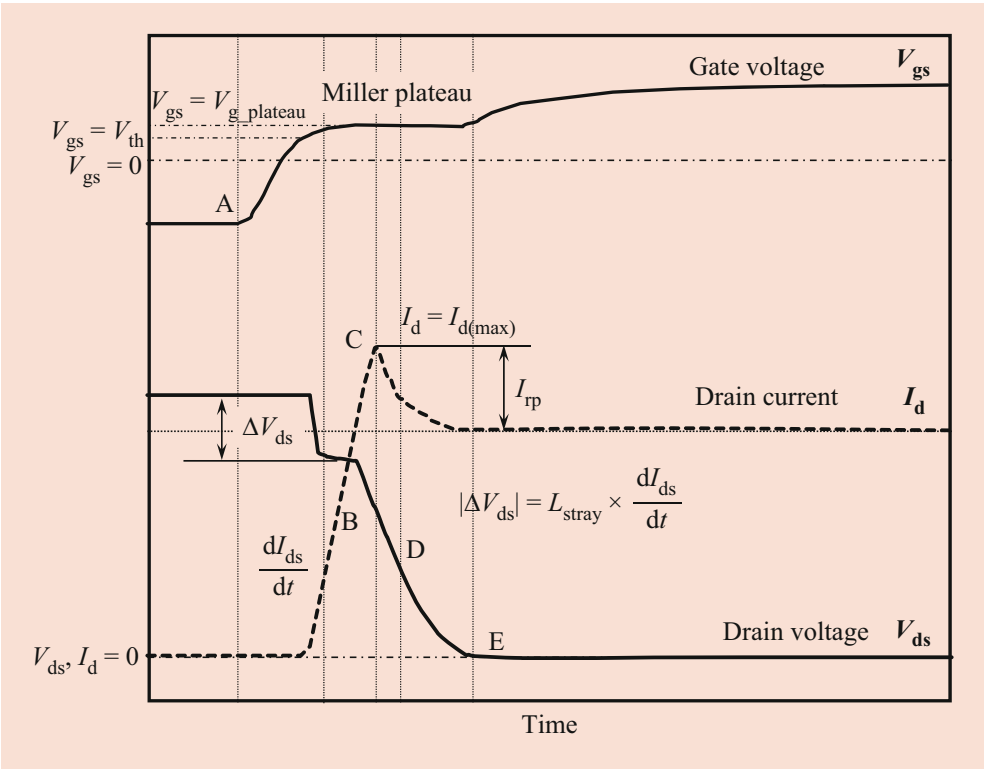


Fig. 13.13 MOSFET turn-on waveforms with an inductive load

where μ_{nch} is the channel mobility, C_{ox} is the specific capacitance of the oxide in the MOS structure, L_{ch} is the channel length, and W_{cell} is the unit cell width. Figure 13.13 shows the drain voltage drop ΔV_{ds} in this period. The voltage drop is caused by a constant increase in the MOSFET drain current (dI/dt), multiplied by the stray inductance L_{stray} in the circuit ($L_{stray} \times dI/dt$). The MOSFET current increases until it reaches the apex $I_{d(max)}$, defined by the total amount of the load current and the peak reverse recovery current in the free-wheeling diode ("C" in Fig. 13.13), and then the drain current is reduced to a load current.

Since the gate voltage V_{gs} is constant during this period, all the gate current I_g is utilized to charge the gate-drain

capacitance $C_{gd}(=C_{rss})$. The gate current I_g in this gate-plateau region is given by

$$I_g(t) = \frac{\left(V_{GS} - V_{g_plateau}\right)}{R_g}. \tag{13.29}$$

From Eq. 13.26, the dV_{ds}/dt is given by

$$\frac{dV_{ds}}{dt} = -\frac{I_g}{C_{rss}} = -\frac{\left(V_{GS} - V_{g_plateau}\right)}{R_g C_{gd}}. \tag{13.30}$$

The drain voltage V_{ds} then starts to fall ("D" in Fig. 13.13), and the voltage continues to fall until it reaches the on-state value ("E" in Fig. 13.13). The gate voltage V_{gs} is constant at $V_{g_plateau}$ during this time, and the gate-drain capacitance increases with the decrease in the V_{ds}. Finally, the gate voltage starts to increase and continues to do so as long as the gate current I_g flows.

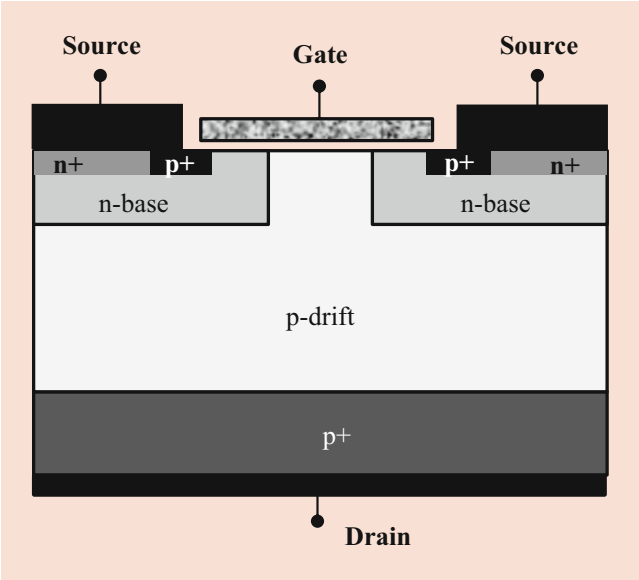


Fig. 13.14 Cross section of p-channel VDMOSFET structure

P-Channel (P-ch) MOSFETs and Their Value for Power Electronics Applications

Figure 13.14 shows the structure of a p-ch VDMOSFET, which can be fabricated simply be reversing the dopant type. The on-resistance increases by a factor of three, compared to the n-ch counterpart, because the channel and bulk mobility of the holes are roughly three times less than that of the electrons. However, when complementary p-ch and n-ch MOSFETs are available, a considerable advantage in circuit simplicity can be achieved in the power electronics field, as in the case of CMOS (complementary MOS) integrated circuits. Figure 13.15 shows leg configuration examples. Figure 13.15a is a commonly utilized leg, consisting of two n-ch MOSFETs (conventional type). In such legs, the reference voltages of the two MOSFETs have different value; hence, two independent gate drive circuits are required to control the MOSFETs. The possible operational states are the following:

(i) MOSFET in upper arm turned on
(ii) MOSFET in lower arm turned on
(iii) MOSFETs in both arms turned off
(iv) MOSFETs in both arms turned on

The last state leads to shoot-through of the DC voltage, and this is forbidden in voltage source inverter circuits, but could take place due to the discrepancy in the signal delay between the two gate control circuits when dead time is not set. That is why dead time with a certain period is required, and it is usually set in advance. Current technologies, such as digital isolators and opto-couplers, can reduce the dead time to roughly 0.1 μs; however, for reliability, the dead time is generally kept at least 1 μs and more in actual power electronics apparatus. An alternative approach to leg driving, instead of the utilization of two independent gate drive circuits, is required to minimize the dead time.

The complementary legs can minimize the dead time beyond the limit of the current technologies by using a p-ch MOSFET. An n-ch MOSFET is activated by the application of positive gate voltage (V_{gs}) and deactivated by the application of negative one to V_{gs}. A p-ch MOSFET, on the other hand, is activated by the application of negative voltage to $V_{gs,}$ and deactivated by applying positive one to V_{gs}. Figure 13.15b shows a complementary leg configuration, similar to the logic inverter circuit in an LSI (large-scale integrated circuit). This configuration has a p-ch MOSFET in the upper arm and an n-ch MOSFET in the lower arm. In the p-ch MOSFET, the reference voltage is the positive side, and in the n-ch MOSFET, the reference voltage is the negative side of the DC voltages. When the gate terminals are not connected with each other, which means that each arm switch operates independently, two gate drive circuits are required, as in the case of conventional leg. The source voltage in a p-ch MOSFET is constant when the device acts as a high-side switch. On the other hand, the source voltage of an n-ch MOSFET utilized as a high-side switch changes between the low side and the input side of the DC bus voltage in the conventional configuration. Therefore, when controlling an n-ch MOSFET, an insulated gate circuit or pulse transformer must be utilized. However, the gate circuit requires an additional power supply, and the transformer can occasionally induce faulty operation. Therefore, the p-ch

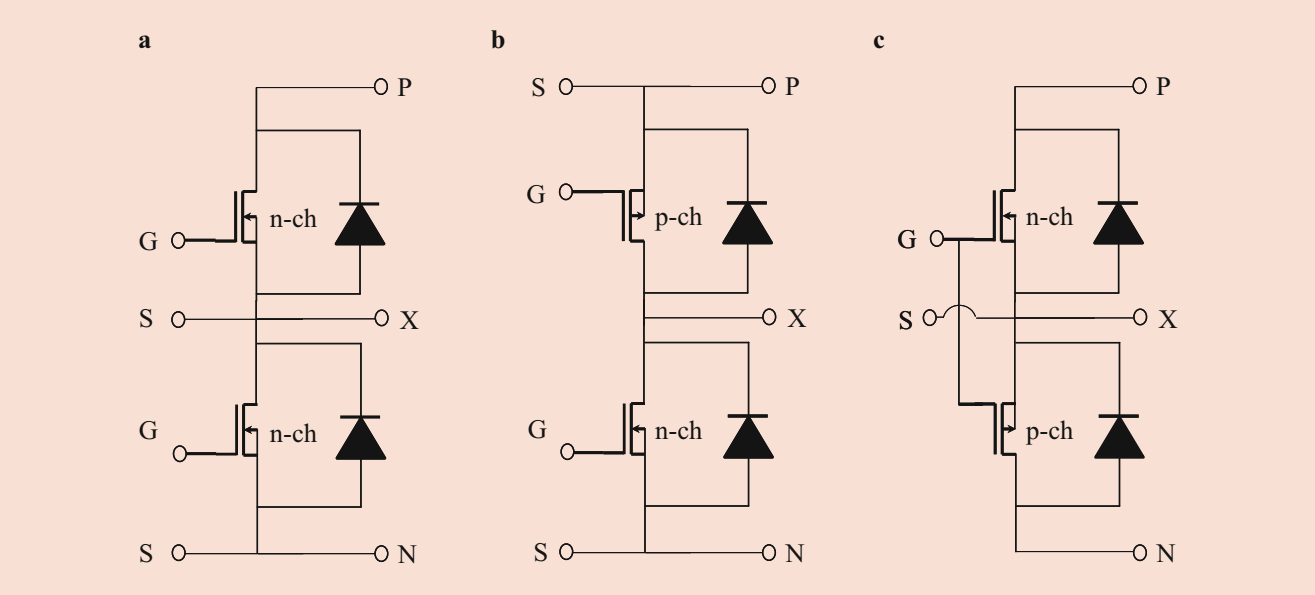


Fig. 13.15 Leg configurations: (**a**) conventional, (**b**) CMOS type, (**c**) source common type

MOSFET has the advantage of enabling reduction in the number of components, and this simplifies the circuit, enhances reliability, and enables a reduction in the size and weight of the overall system.

When the gate terminals are connected with each other, on the other hand, one gate circuit can control both MOSFET, making it possible to reduce the dead time. However, in the CMOS-type configuration, a voltage similar to the DC voltage level could be applied to the gate-source terminals as V_{gs} in the upper arm of the p-ch MOSFET; and in power electrics applications, as the DC voltage level is usually much higher than the rated voltage for V_{gs}, the MOSFET may well not withstand it. In addition, this configuration may experience the shoot-through when the leg state is changed. Therefore, this configuration cannot be used in high voltage power electronics applications. The configuration in Fig. 13.15c has a p-ch MOSFET in the lower arm and an n-ch MOSFET in the upper arm, with a common reference voltage in both MOSFETs, so that one gate circuit can control both MOSFETs in the leg by connecting the gate terminals with each other. In addition, shoot-through hardly occurs, because it is impossible for both MOSFETs to be in the on-state, simultaneously. Therefore, the dead time set in advance can be minimized by employing the gate control circuit. The advantage of minimum dead-time operation in such a complementary topology was confirmed by utilizing the device in a grid-tied inverter of 400 W and switching frequency of 100 kHz and impedance in the grid-connection inductor reduced to 1.5%, which resulted in current THD (total harmonic distortion) of only 2.3% [12].

13.2.3 UMOSFET Structure

In planar VDMOSFETs, the JFET resistance R_{JFET} fundamentally limits the beneficial cell dimension scaling [13]. Specifically, as the polysilicon gate width is reduced below a certain value when shrinking the device cell pitch, an unavoidable increase in the R_{JFET} occurs and the overall device resistance increases. The trench power MOSFET in silicon was developed late in the 1980s [7] via applying the trench process technology primitively developed for DRAMs. In a V-groove trench MOSFET, a channel is formed along the surface of an anisotropically etched groove which forms a 54.7° angle with the surface [13]. To prevent an electric field crowding, the top of the V-grooved etching must be prematurely terminated to form a flat-bottomed groove. Furthermore, since the groove is too wide to refill and planarize, the deposited gate electrode must coat the nonplanar shape, leading to fabrication difficulties such as source metal coverage. Thus, instead of the V-grooved gate structure, a new type of trench MOSFET with a steeper rectangular-shaped groove was proposed [14]. This device utilized a polysilicon gate that, in combination with a steep and wide rectangular groove profile, led to an even larger step height.

A number of technological fabrication innovations, such as planarizing trench refill technology, resulted in the mass production of a trench MOSFET. Figure 13.16 shows a trench or UMOSFET structure, along with its components of internal resistance [6]. The UMOSFET structure can increase the channel density significantly and eliminate the JFET resistance, leading to an enhanced performance of low-voltage (<200 V) power MOSFET. The total on-resistance of a power

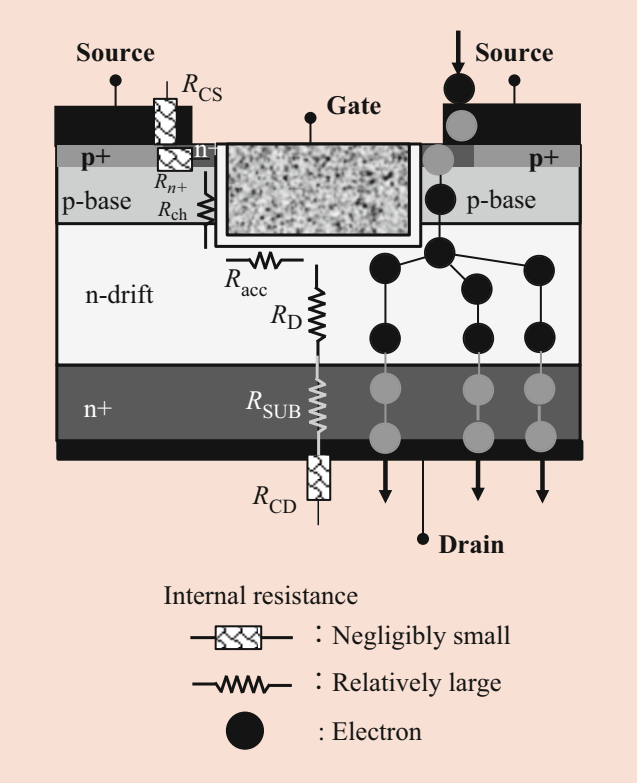


Fig. 13.16 Cross section, internal resistances, and electron flow path in trench MOSFET structure

UMOSFET is obtained by totaling the contributions of all the resistance components:

$$R_{ON} = R_{CS} + R_{n+} + R_{ch} + R_{acc} + R_D + R_{SUB} + R_{CD}. \tag{13.31}$$

Stripe cell surface topology is utilized in power UMOSFETs because of its elimination of the bottom trench corner, which otherwise exhibits high electric field concentrations. Furthermore, by utilizing the stripe cell topology, the surface of trench sidewalls can be oriented in the suitable direction to produce high-quality etched surfaces. In UMOSFETs, the resistances of the source contact (R_{CS}), n+ source region (R_{n+}), and drain contact (R_{CD}) are negligibly small.

The UMOSFET has channels formed on both the vertical sidewalls, and the specific on-resistance in channel is obtained by

$$R_{ch} = \frac{L_{ch} W_{cell}}{2\mu_{nch} C_{ox} \left(V_{gs} - V_{th}\right)}, \tag{13.32}$$

where μ_{nch} is the channel mobility, C_{ox} is the specific capacitance of the MOS, L_{ch} is the channel length, and W_{cell} is the UMOSFET cell width. According to [11], for example, in a 30 V UMOSFET with a cell width (W_{cell}) of 3 μm and gate oxide thickness of 0.05 μm, the calculated on-resistance in channel is 0.057 mΩ cm^2, when a gate voltage is set at 10 V. This value is much less than the channel resistance in the VDMOSFET described above (0.245 mΩ cm^2). The reduction in the channel resistance in the UMOSFET is because of the fourfold enhancement in channel density (W_{cell} ratio: 12 μm/3 μm = 4). The UMOSFET has thus become the main power semiconductor device for low-voltage regions, with reduced on-resistance due to cell structure optimization and finer cell pitch utilization, as a result of the introduction of nano-fabrication technologies. However, the chance of further on-resistance improvement appears to be limited, even when advanced forms of existing technologies are employed.

State-of-the-Art UMOSFETs

The field-plate trench MOSFET [15] is a UMOSFET with a buried electrode, surrounded by a thick insulating film, under the gate electrode of a conventional trench MOSFET, or a split-gate or shielded-gate trench MOSFET, as shown in Fig. 13.17. This structure has recently been reported as suitable for use with low breakdown voltage (about 200 V or less). In conventional low-voltage UMOSFETs, the channel resistance is reduced by reducing the cell pitch; however, this does not reduce the drift layer resistance, resulting in the increase of relative contribution of the drift layer resistance, and this has been a problem for UMOSFETs, even in the low breakdown voltage range. In the field-plate trench structure, on the other hand, the doping concentration in the drift layer can be increased by the field-plate effect of the buried electrode, and the drift layer resistance is thereby reduced. Therefore, along with superjunction technology, much attention has been paid to this structure as a means of extending the limits of silicon MOSFET capability. Since the mesa doping concentration is determined by the mesa width, and the concentration can be increased in roughly inverse proportion to the mesa width, the drift layer resistance can be lowered by pitch shrinkage. In [16], Park et al. reported 60 V class split-gate trench MOSFET fabrication results. The on-resistance in n-drift layer constituted roughly 60% of the overall resistance, even in 60 V class devices; thus, minimization in the on-resistance in the drift region is attractive in this voltage class. The fabricated device exhibited an on-resistance of 10.9 mΩ mm^2, gate charge Q_g of 73.9 nC, and $R_{on} \times Q_g$ of 85 mΩ nC due to its fine field-plate trench structure (the result of chemical mechanical polishing (CMP)) and tungsten plug technology, which enhance its performance compared to devices fabricated using previous-generation technologies (see Table 13.1). Further, this device was utilized in the synchronous rectifier of an isolated-type DC-DC converter and showed high efficiency as well as advantages of the field-plate trench structure, such as low dV_{ds}/dt and low peak drain voltage.

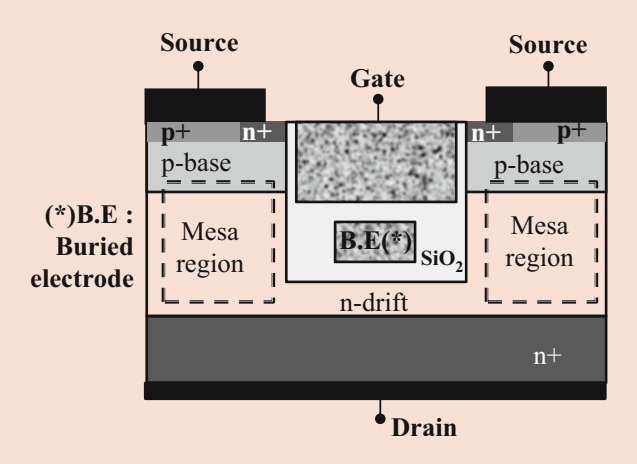


Fig. 13.17 Cross section of field-plate trench MOSFET

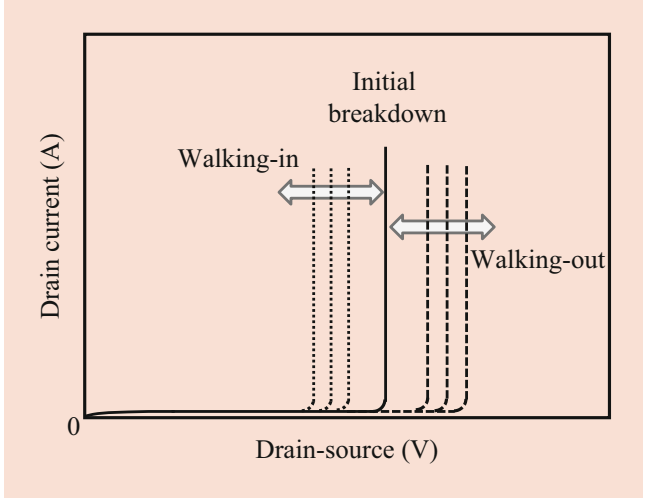


Fig. 13.18 An example of breakdown instability characteristics in trench field plate MOSFET

Table 13.1 Comparison of electrical characteristics (60 V class MOSFETs)

	Split gate trench MOSFET	Conventional device
Specific on resistance (mΩ mm^2)	10.9	17.8
Q_g (nC)	73.9	66
$R_{on} \times Q_g$ (mΩ · nC)	85	145

Another approach to reducing the on-resistance involves increasing the field-plate effect and doping concentration in the mesa. Kobayashi et al. gradually thickened the oxide film in the depth direction of the trench in a so-called multiple stepped oxide field-plate trench MOSFET (MSO-FP-MOSFET) and showed that the longitudinal electric field in the mesa was maintained even at a higher doping concentration than before and that the breakdown voltage could be maintained and the on-resistance reduced [17]. The study confirmed that a breakdown voltage of 114.8 V can be obtained, even with a 1.5 times greater doping concentration in the drift layer with respect to the field-plate trench structure of a conventional 100 V class device, by fabricating a diode TEG (test element group) with the trench structure mentioned above. Based on the device simulation results, it was inferred that this device structure could exhibit an on-resistance of 28.5 mΩ mm^2, 25% lower than the conventional structure. It is strongly expected that the device's on-resistance will continue to be improved in the future, due to miniaturization and refinement of the gate structure in the trench.

On the other hand, as a problem peculiar to this structure when using a Si/SiO_2 interface, there is instability in the breakdown voltage; however, there have been reports of improvement in stability resulting from analysis of this phenomenon and the device design. In the field-plate trench structure that improves the breakdown voltage by using Si/SiO_2, variation in the breakdown voltage due to charge trapping or interface degradation (also termed "walking-in and walking-out"; see Fig. 13.18), which is presumed to be caused by hot carriers during avalanche generation, has been reported in recent years. Yedinak et al. reported that the breakdown voltage is stabilized by lowering the doping concentration in the drift layer of the cell to a level slightly lower than the concentration at which charge balance can be obtained [18]. Hossain et al. noted that the charge balance design, not only of the cell component but also of the termination component, is important for stabilizing the breakdown voltage; and by optimizing the distance between the termination trench and the cell trench, it was confirmed that the breakdown voltage fluctuation could be suppressed [19]. Furthermore, Hossain et al. calculated the charge balance in the termination structure using three-dimensional TCAD simulation and provided a more detailed explanation of this phenomenon [20]. To optimize the charge balance in the cell, Deng et al. performed an analysis based on the integration value of the space charge in the depth direction, and the average space charge, for an element in which the doping concentration in the drift layer changed in the depth direction [21]. The results suggested that it is desirable to use a slightly lower doping concentration in the drift layer, which can nonetheless ensure charge balance, in order to suppress the degradation of breakdown voltage due to the walking-in phenomenon.

Several technologies have been developed for suppressing breakdown voltage fluctuation by optimizing designs such as those described above, but the physical mechanism of breakdown voltage fluctuation continues to be discussed. A common conclusion of the published studies, however, is that there is a high possibility that positive charges are generated at the Si/SiO_2 interface of the trench. Nishiwaki et al. [22] showed that the breakdown voltage fluctuation has a power

relationship with respect to time, by evaluating the time and avalanche current dependence of such fluctuation, and proposed a model to explain the origination of the positive charge. The model suggested that due to the holes caused by avalanche breakdown, trap levels were generated by the desorption and diffusion of hydrogen atoms terminating at the Si/buried-SiO_2 interfaces at the bottom of the trench, and became positive. This proposed model was similar to the Negative Bias Temperature Instability (NBTI) test results for the p-ch MOSFET. In this way, the physical understanding of the breakdown voltage fluctuation is being gradually deepened by measurement and simulation.

A characteristic feature of the field-plate trench structure is that the feedback capacitance (C_{rss} or C_{gd}) between the gate and the drain is low, because the gate electrode is shielded from the drain by the buried electrode, called a shield gate. Further, the capacitance between the buried electrode and the drain, and the embedded wiring resistance, equivalently form a snubber circuit, meaning that this element itself has the function of suppressing noise and is a suitable structure for high-speed switching. On the other hand, the capacitive coupling between the buried electrode and the gate electrode may cause shoot-through or self-turn-on operation.

In light of this, modeling technology using TCAD and SPICE (simulation program with integrated circuit emphasis) is becoming increasingly important. In [23], analysis of the equivalent circuit in the field-plate trench structure, represented by the parasitic capacitance around each terminal, the gate electrode wiring resistance, and the buried electrode wiring resistance, showed that the potential of the embedded electrode is transiently increased by the displacement current. This result suggested that the field-plate effect was suppressed and that the breakdown voltage of the device was transiently lowered enough to cause a dynamic avalanche, which could lead to shoot-through. In addition, using TCAD mixed-mode simulation and experimentation, Roig et al. proposed a configuration designed to optimize the trade-off characteristics of the shoot-through and ringing, through the use of a built-in snubber [24].

13.2.4 Superjunction MOSFET

In 1982 [25] and 1988 [26], Coe et al. introduced the concept of alternate n- and p-stripes in power devices. A device structure with a RESURF (reduced surface field) device was presented with lateral structures in 1979 [27]. The RESURF junction incorporated in an LDMOSFET enables more efficient depletion layer expansion in the drift region and enhanced doping concentration in the n-drift region, utilizing the interaction of the depletion layers expansion from two p-n junctions. The name "superjunction" was introduced in [28], and a theoretical analysis of this structure was presented in

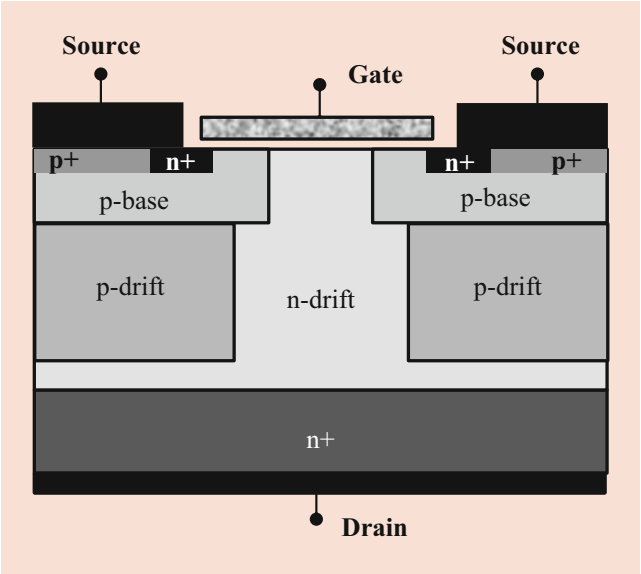


Fig. 13.19 Planar gate SJ-MOSFET structure

[29]. The primary feature is that the high doping drift region comprises several alternating n- and p-type stripes. If these stripe layers are reasonably narrow and the net doping concentration in both stripes is roughly equal, the stripes can be completely depleted at relatively low biases; at which point, the stripe layers act as an intrinsic layer and a uniform electric field distribution is attained, leading to a high breakdown voltage. According to [30], one of the first vertical MOSFET devices to incorporate superjunction physics was introduced in early 1980, and commercial devices were presented as CoolMOS [31] and MDMESH [32], in the late 1990s.

Figure 13.19 shows a cross sectional view of the superjunction MOSFET structure, which is similar to the CoolMOS structure. Two basic approaches to fabricating the superjunction MOSFET have been proposed. The first is based on the utilization of p-type and n-type multiple ion implantations process, followed by n-type epitaxial growth one [33]. The second is based on the application of etching process to make deep trenches into an n-drift region, followed by refilling of the trenches with the p-type epitaxial layer [34]. Numerous other structures of the superjunction MOSFET have also been introduced and demonstrated [30]. After forming the alternating n- and p-type columns vertically, the wafer surface is smoothed by CMP (chemical mechanical polishing), then the planar gate structure is formed. Trench and UMOSFET structure can be formed to minimize the channel resistance. The superjunction structure could, for example, be designed three dimensionally, as stripes in parallel with, or orthogonal to the trench gates.

The charge-coupling concept has enabled augmentation of the breakdown capability in power MOSFETs. In designing the superjunction MOSFET, it is critical to properly spec-

ify the doping density and thickness of the n- and p-type columns. The doping Q_{opt} and width are optimized and given by [6]

$$Q_{opt} = 2qN_D w = \varepsilon_s E_c, \tag{13.33}$$

where q is the electron charge, N_D is the doping concentration in the n- column region, w is half the width of the n- column region, ε_s is the dielectric constant of the semiconductor materials, and E_c is the critical electric field.

The physics of superjunction MOSFET operation in forward blocking is different from that of the VDMOSFET and UMOSFET described above. The theoretical analysis of superjunction devices was presented in [28]. When the positive voltage is applied to the drain, a depletion layer is expanded not only under the planar or trench gate electrode but also the vertical p-n junction of the p and n columns in the drift region. This two-dimensional depletion layer expansion leads to the suitable charge coupling, which makes the electric field distribution rectangular and can utilize the very high doping concentrations in the drift region. The latter results in extremely low on-resistance $R_{ON,\,sp}$, which has been presented [29]. Assuming a principle structure similar to superjunction devices such as JFETs, the on-resistance of vertical devices has been analytically related to the breakdown voltage V_B as follows [30]:

$$R_{ON,sp} = 4w\frac{V_B}{\mu\varepsilon E_C^2}, \tag{13.34}$$

where w, μ, ε, and E_c are the half pitch of columns in the superjunction devices, mobility of electrons, dielectric constant of silicon, and critical electric field, respectively. The remarkable potential of superjunction devices to minimize the on-resistance, in comparison with the trade-off relation in conventional devices as illustrated by

$$R_{ON,sp} = \frac{27}{8} \times \frac{V_B^2}{\mu\varepsilon E_C^3}, \tag{13.35}$$

was theoretically demonstrated in [28].

This is particularly suitable for the realization of high-performance silicon power MOSFET with large blocking voltage in 500–700 V range. To reduce the $R_{ON,sp}$, the lateral pitch must, in principle, be narrowed, in order to maintain a high vertical field even with the increase in the n-column doping concentration. Reflecting this design, $R_{ON,sp}$ improvement with lateral pitch narrowing has been demonstrated [35, 36]; and the $R_{ON,sp}$ has been continuously reduced in 600–650 V class power MOSFET products [30, 37–39]. For example, the latest CoolMOS has successfully lowered the specific on-resistance to 8 mΩ cm^2 for 600 V-rated devices. This extremely low on-resistance has been achieved by extreme shrinkage of the pitch of the underlying superjunction structure. Precise tailoring of the doping profiles is required to yield process windows wide enough for mass production; however, with further improvements in related manufacturing processes, an on-resistance in the range of 5 mΩ cm^2 could be achievable.

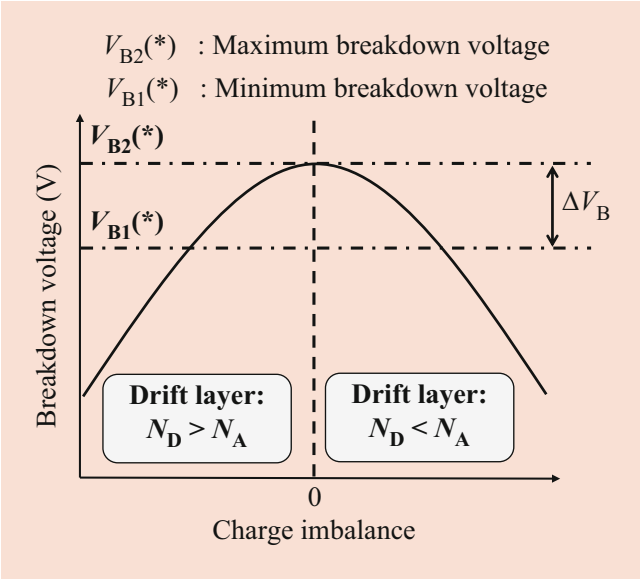


Fig. 13.20 Breakdown voltage degradation due to charge imbalance in superjunction MOSFETs

The breakdown voltage of the superjunction MOSFET degrades through the charge imbalance between the n- and p-columns, because of the intrinsic electric field modulation. Thus, the charge imbalance margin must be designed with an eye to process controllability in mass production. Figure 13.20 is a schematic of such breakdown voltage lowering through charge imbalance. Saito provided an analytical expression for determining the on-resistance limit when taking the influence of charge imbalance in superjunction MOSFETs into account [40]. The breakdown lowering ΔV_B with a flat doping profile in the superjunction is given by

$$\Delta V_B = V_{B2} - V_{B1} = \frac{q\,|N_A - N_D|}{4\varepsilon_s} t_{SJ}^2 = \frac{q\alpha N_{SJ}}{4\varepsilon_s} t_{SJ}^2, \tag{13.36}$$

where q is the electron charge; ε_s is the dielectric constant of the semiconductor materials; N_A is the doping concentration in the p-column; N_D is the doping concentration in the n-column, which is equal to N_{SJ}; and α is the charge imbalance ratio.

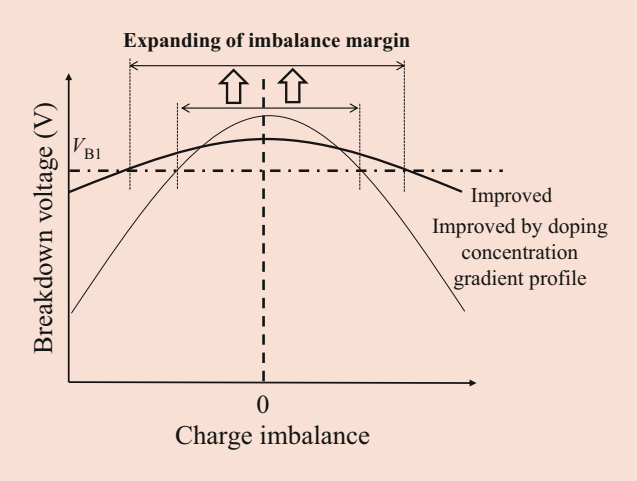


Fig. 13.21 Expanding of charge imbalance margin by doping concentration gradient profile

In order to keep the charge balance margin large, it is necessary to increase the breakdown voltage in the balanced state; but then the on-resistance increases because the pillar is deep and the concentration is reduced. Therefore, it is highly important to improve the trade-off characteristics between the on-resistance and charge imbalance margin. To suppress the decrease in breakdown voltage when the charge balance collapses (Fig. 13.21), it is effective to add a concentration gradient to the pillar. As shown in Fig. 13.22b, the maximum breakdown voltage V_{B2} in the balanced state decreases due to the electric field modulation, but the electric field distribution when the charge balance collapses can be improved, resulting in suppression of the breakdown voltage lowering. Therefore, a graded doping profile expands the charge imbalance margin.

The V_B lowering with a graded doping profile in the superjunction is given by

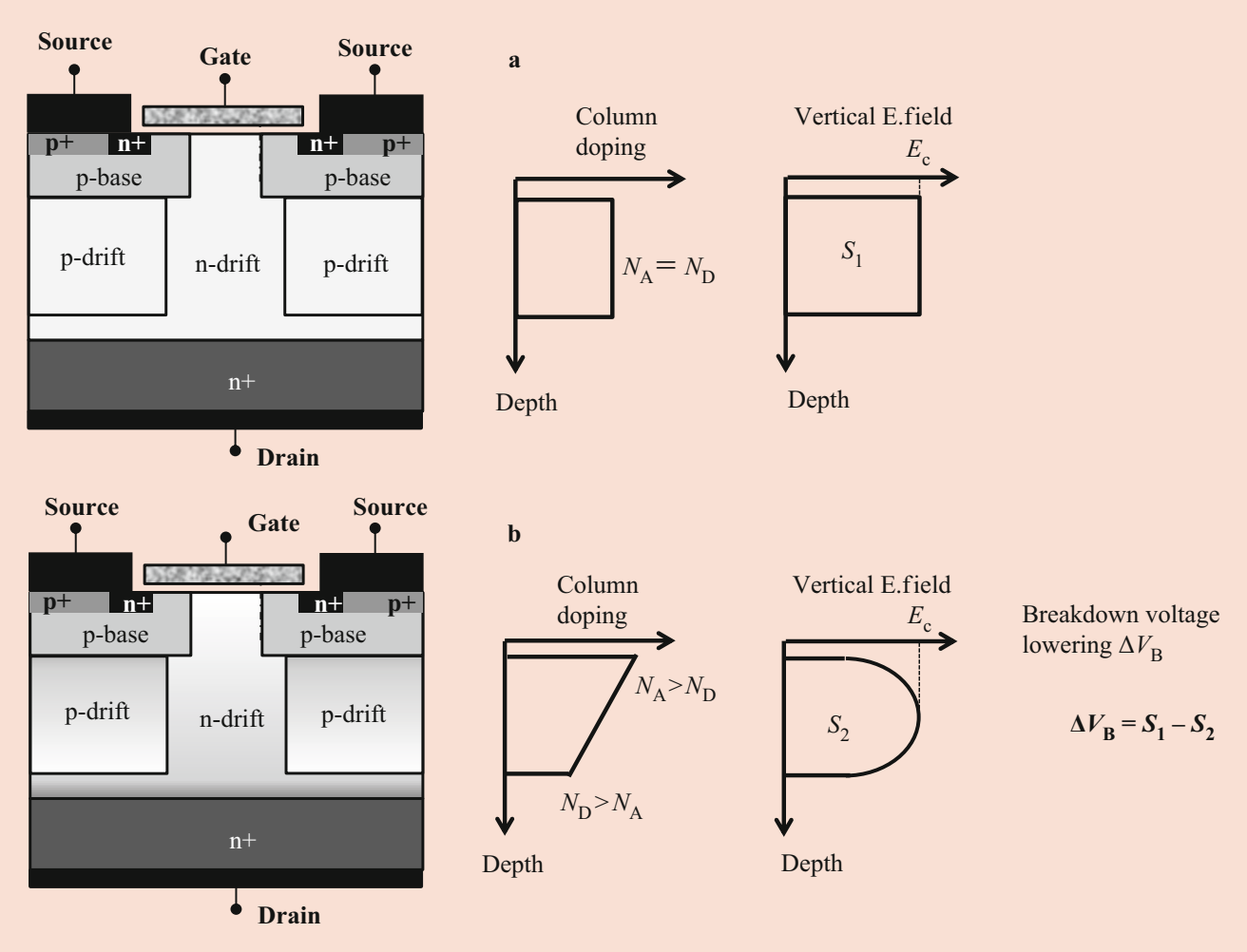


Fig. 13.22 Doping profile and vertical field distribution in columns (**a**) w/o concentration gradient and (**b**) with concentration gradient

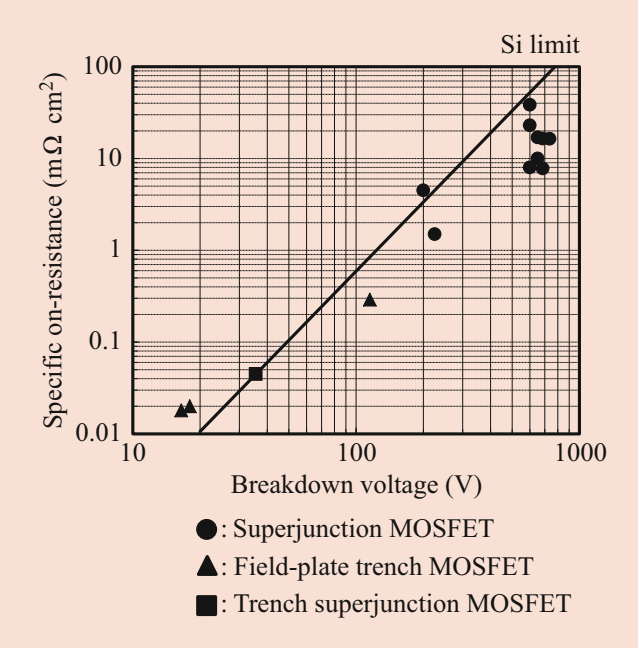


Fig. 13.23 Specific on-resistance versus breakdown voltage of trench and superjunction MOSFETs. This graph was drawn using data in [7] and [30]

$$\Delta V_B = \frac{qN_{SJ}}{24\varepsilon_s} t_{SJ}^2 \left(\gamma + 3\frac{\alpha^2}{\gamma}\right); \tag{13.37}$$

and to minimize ΔV_B, the optimum γ is given by $\gamma = \sqrt{3}\alpha$ from Eq. 13.37, so that ΔV_B is expressed by

$$\Delta V_B = \frac{q\alpha N_{SJ}}{4\sqrt{3}\varepsilon_s} t_{SJ.}^2 \tag{13.38}$$

Graded doping can reduce ΔV_B by $1/\sqrt{3}$ compared to the value with a flat doping profile, as shown in Eq. 13.36; and as a result, the amount of charge in the drift region can be increased and low on-resistance can be achieved. In [40], the theoretical limit of on-resistance in 600 V devices was estimated to be 7 mΩ cm^2 with a charge balance margin of ±3%.

Figure 13.23 shows a recent achievement of $R_{ON,sp}$ versus breakdown voltage of trench (including field-plate trench) and superjunction MOSFETs [7, 30].

13.2.5 MOSFET Body Diode

When applying a negative voltage to the drain electrode of VDMOSFET and UMOSFET structures, the junction of the p-base and n-drift region is in a forward-biased state, and the current starts to flow. This is the pn diode operation, and the current flows when the drain voltage exceeds roughly 0.7 V in the negative direction. This is referred to as the current flow through the MOSFET body diode . A cross section of the UMOSFET structure with the body diode is illustrated in Fig. 13.24, along with the equivalent circuit. The MOSFET body diode can be used as a free-wheeling diode in voltage source converters, so its forward voltage drop and reverse recovery power dissipation must be kept at a low value. When the negative voltage is applied to the drain electrode of MOSFET, the body diode is driven into forward conduction, resulting in the hole injection from the p-base region into the n-drift layer. A large number of holes and electrons flow in the n-drift region, leading to low on-state voltage drop. When the drain voltage of the MOSFET changes from negative to positive, the stored holes and electrons in the n-drift region must be swept out, and then the p-n junction between the p-base and n-drift regions is reverse recovered. The swept-out charge generates a large current flow in the reverse direction, resulting in power loss in the MOSFET. The reverse recovery characteristics of the body diode in power MOSFETs can, however, be controlled by some lifetime control techniques, such as electron irradiation [41, 42].

It has been recognized that power MOSFETs can fail in certain situations involving the body diode operation. Such failure sometimes occurs as the drain voltage rises sharply at the reverse recovery of the p-n junction (p-base and n-drift regions). This sharp increase in drain voltage (i.e., surge voltage) is caused by a rapid decrease in the current (dI/dt) associated with a higher level of recovery current and stray inductance L_{stray} in the circuit ($L_{stray} \times dI/dt$). Therefore, optimal design of the forward voltage drop, reverse recovery loss characteristics, and surge voltage reduction in the body diode is highly important for achieving superior circuit efficiency in the voltage source converter. A suitable method for improving the body diode characteristics involves the integration of a Schottky barrier diode in the power MOSFET device [43]. The reverse leakage current from the integrated Schottky barrier diode can be reduced by using a junction barrier Schottky (JBS) diode [44]. In low-voltage power MOSFETs, such configurations are highly effective; however, in high voltage power MOSFETs (500 V and more), this approach can be ineffective due to the higher on-resistance.

In superjunction MOSFETs, the reverse recovery current flowing through the body diode becomes very strong, resulting in large reverse recovery loss; thus, such devices are not often utilized in voltage source converters with a free-wheeling mode. In order to alleviate this difficulty, a new type of circuit technology, utilizing the synchronous reverse blocking method was proposed [45]; the basic circuit topology is shown in Fig. 13.25. In this configuration, a second low-voltage MOSFET is added in series with the main switch, to block the reverse current in the associated body diode. This second switch must be synchronized with

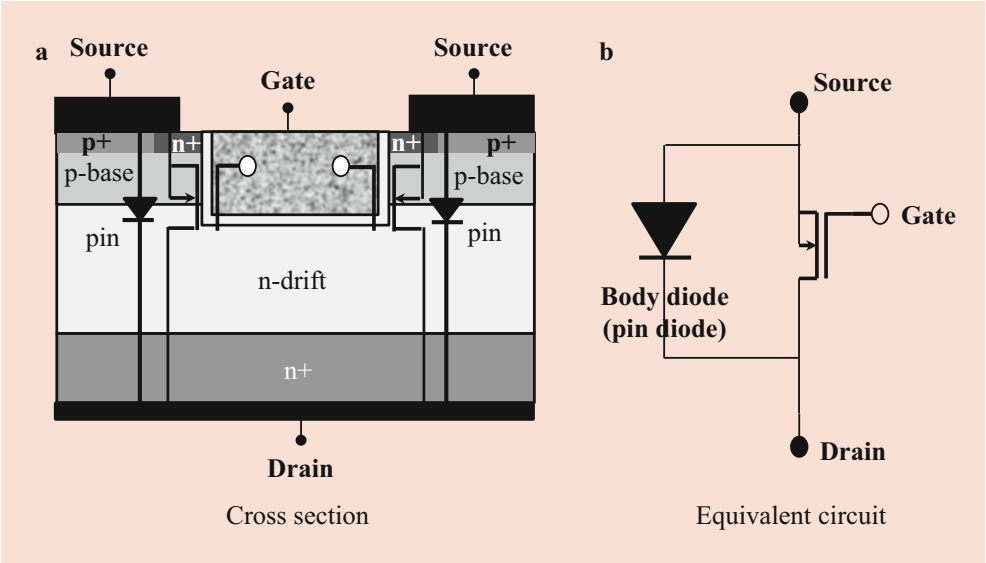


Fig. 13.24 Body diode within the UMOSFET structure. (a) Cross section. (b) Equivalent circuit

the main switch (superjunction MOSFET) so that the reverse current flows through a parallel SiC Schottky diode. In this way, the reverse recovery characteristics of superjunction MOSFET body diodes can be improved.

13.2.6 Edge Terminations for Silicon Power Devices

Figure 13.26a shows a top view of an actual power MOSFET. As can be seen from the figure, on its top surface a power MOSFET has a source electrode and a gate electrode for applying a control signal; and the current flows between the source electrode and a drain electrode on the rear surface, which does not appear in this figure. There is a ring-shaped band around the element, to enclose the gate electrode and the active region (see Fig. 13.26b) where the drain current flows. This band called edge termination region, in which no drain current flows, simply provides a region for supporting high drain voltages (see Fig. 13.26c) and is incorporated not only in power MOSFETs but in IGBTs and diodes.

Figure 13.27 shows a cross section of the end of a power MOSFET with no edge termination regions. Power MOSFETs are fabricated in silicon wafers, and when the wafer process is completed, many square chips are cut out by sawing through the wafer. This process called dicing is performed by diamond-coated blades and results in severe damage to the silicon crystals. In the case of power MOSFETs with no edge terminations (as shown in Fig. 13.27), when the dicing cuts through pn junctions, a large amount of leakage current can be generated and flow in the forward blocking state, because the depletion layer intersects with the crystal damage regions, resulting in degradation of the breakdown voltage and its stability with respect to time. This problem can be addressed, however, by incorporating an edge termination region around the power MOSFET, so that the depletion layer of the pn junction, which must support the high drain voltage, does not intersect with the cutting lines of the dicing saw, where there is severe crystal damage.

A planar junction edge termination has a number of guard rings (or floating rings), and is generally utilized in silicon power MOSFETs, IGBTs, and diodes. Figure 13.28 shows a cross-sectional view of the edge structure. Notably, the guard rings can be fabricated with the pn junction in active regions (or main junction) with no additional process steps at the same time. The breakdown characteristic of the edge termination region depends on the distance of the leftmost guard ring from the main junction (W_{G1}) and the distance of each ring (W_{Gn}). If the distance W_{G1} is too wide, the electric field at the edge of the main junction becomes high ("A" in Fig. 13.28), leading to a breakdown voltage close to a planar junction with no edge termination. If the distance W_{G1} is too narrow, a high electric field is concentrated on the next-outermost ring, resulting in the breakdown voltage worsening. Hence, optimum distance is necessary to show a high breakdown voltage. The breakdown voltage of a planar junction with one single guard ring can be analyzed by calculations [46]; however, at present, to achieve much more reliable characteristic in the edge structure, a number of guard ring structures is utilized in power MOSFET devices. More sophisticated design optimization can be achieved using TCAD simulations of the structure.

Another approach to junction edge termination involves junction termination extension (JTE) structures, which have been shown to dramatically improve the breakdown voltage. As illustrated in Fig. 13.29, these structures contain a p-type

region formed at the peripheral region of the p-n junction [6]. This p-type region, which is very lightly doped, is commonly formed by ion implantation in order to control the dopant charge precisely. If the doping density in the p-type region is too heavy, breakdown at lower voltage takes place at the edge ('C' in Fig. 13.29), because of the smaller radius of p-n junction curvature at this edge. When the doping density in the p-type region is too light, the region is fully depleted at a low reverse voltage, leading to breakdown at the main junction ("B" in Fig. 13.29) at the similar voltage as a structure without termination region.

According to [6], the charge in the p-type region is optimized by

$$Q = \varepsilon_s \times E_c, \tag{13.39}$$

where E_c is a critical electric field for silicon and ε_s is the dielectric constant of silicon. So, the optimum dopant dose in the JTE region (see Fig. 13.29) can be calculated as roughly 1.3×10^{12} cm^{-2} in silicon. A sophisticated optimization of the p-type region can be achieved using TCAD simulations. Although the breakdown voltage of the JTE structure depends on the p-type region, the total dose in this region can be precisely controlled by the ion implantation process, and the breakdown voltage is not likely to vary significantly, even with uneven doping in the p-type regions.

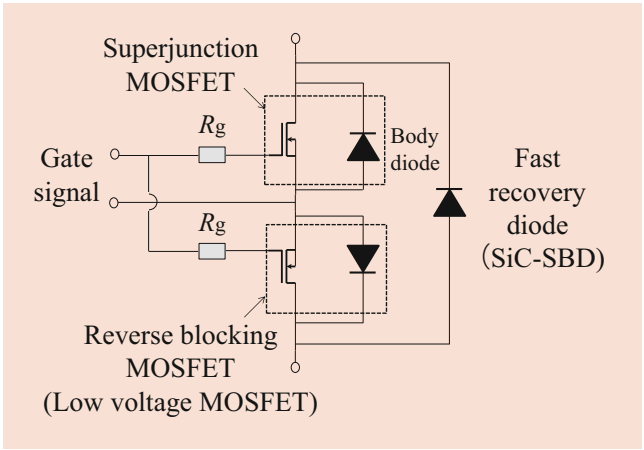


Fig. 13.25 Circuit configuration of synchronous reverse blocking method

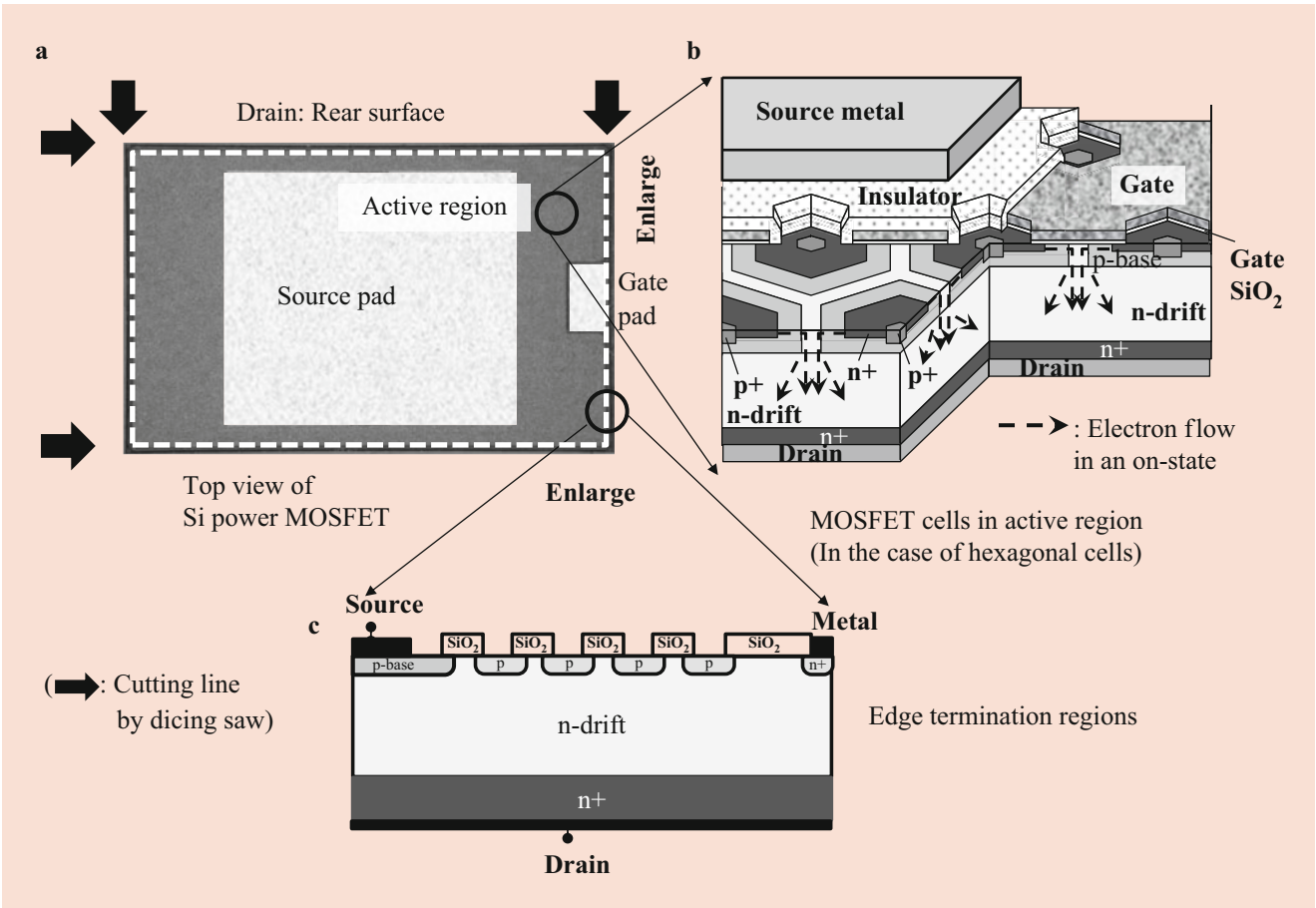


Fig. 13.26 (**a**) Top view of silicon power MOSFET. (**b**) Layout of MOSFET cells in active region. (**c**) Edge termination region

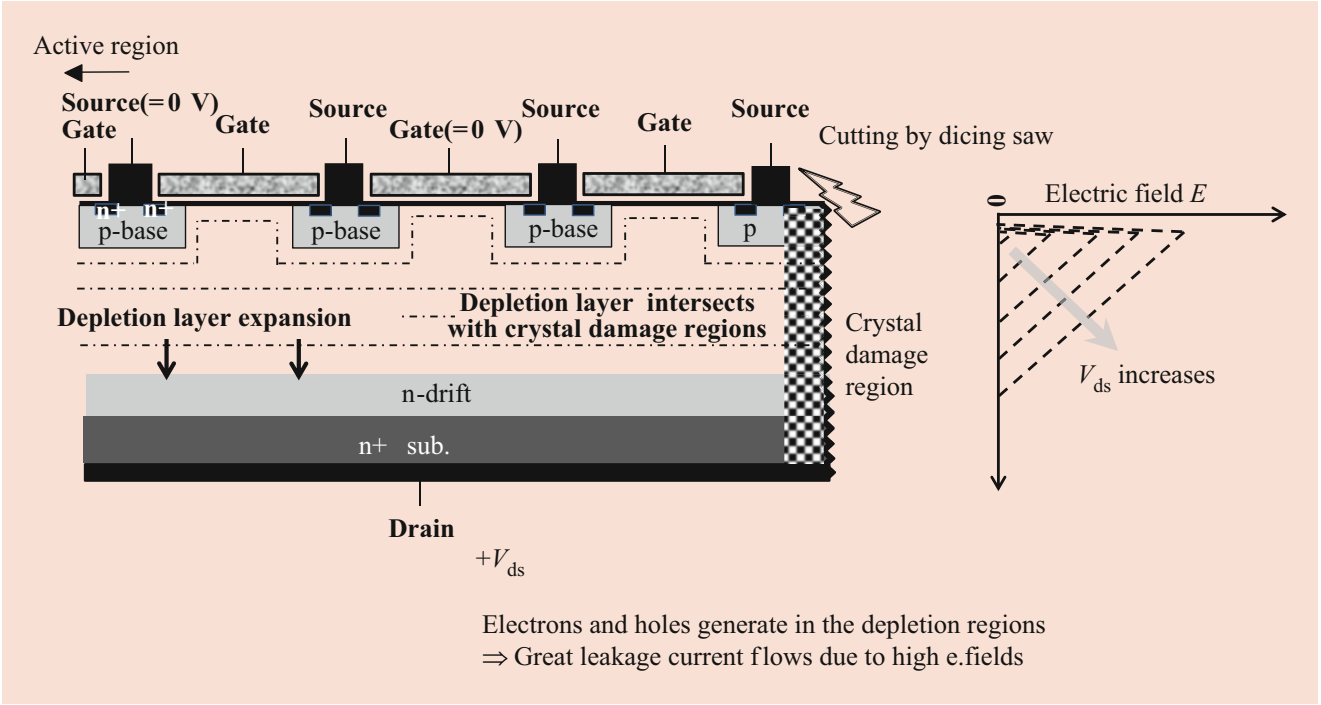


Fig. 13.27 Cross section of power MOSFET end region with no edge termination region. In a forward blocking state, depletion layer expands and intersects with the crystal damage regions

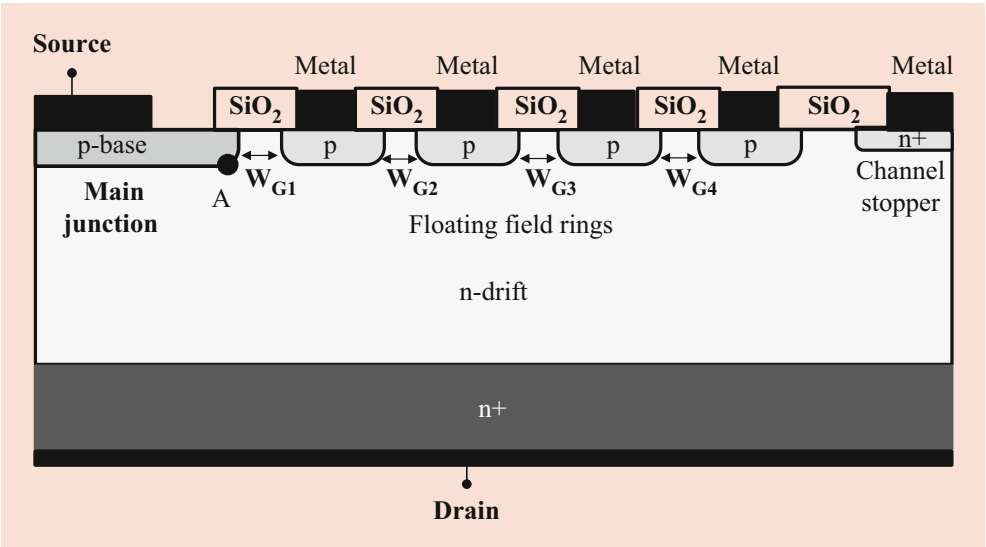


Fig. 13.28 Schematic cross section of multiple floating field ring terminations

Field-plate structures are also popular for use as edge structures. Figure 13.30 shows the effect of the field plate, which expands the depletion region at the edge. In this case, the metal layer is formed on the p+ region and extended over the silicon dioxide layer (SiO_2) at the edge of the power device. Notably, combining the field plate with guard rings means that less rings are needed, thus reducing the area requirement. It is important to minimize the edge termination area as possible to reduce device cost, because this edge termination area cannot be utilized for main current flow in the device. This approach obviates the need for additional photomasks and photolithography processes; however, the edge region can be a weak point for power semiconductor devices, and optimum design and reliable fabrication are highly important for stable and rugged power device development in this case.

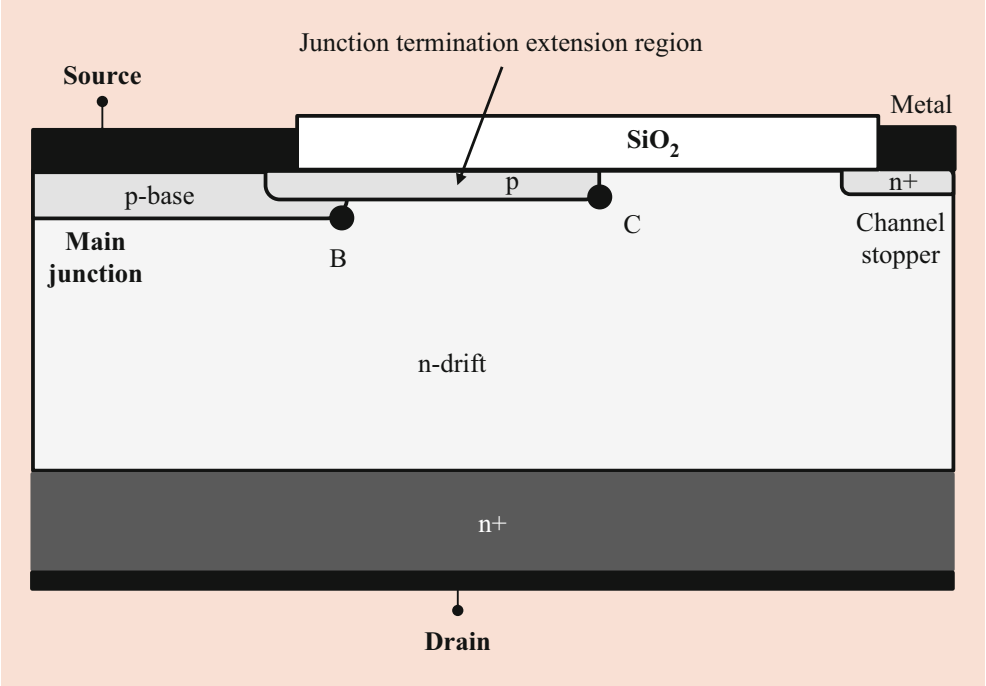


Fig. 13.29 Schematic cross section of junction termination extension

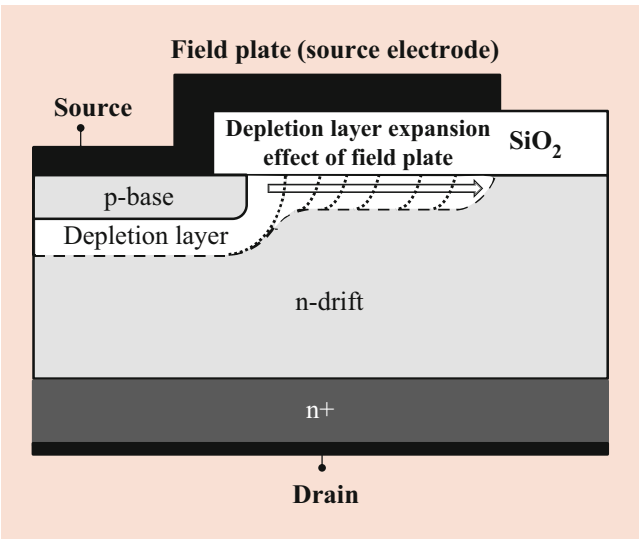


Fig. 13.30 Schematic cross section of field plate at the edge structure

13.2.7 Epitaxial Layers and Substrate Wafers

In vertical MOSFETs such as VDMOSFETs, UMOSFETs, and superjunction MOSFETs, when the electrons reach the lower side of n-drift region, they are distributed throughout the n+ substrate, enabling them to flow evenly through the substrate. The resistance in the n+ substrate is obtained by

$$R_{SUB} = \rho_{SUB} \times t_{SUB}, \tag{13.40}$$

where ρ_{SUB} is the resistivity and t_{SUB} is the thickness of the substrate. Therefore, the resistance in the n+ substrate is strongly dependent on its thickness and resistivity, necessitating the use of available technologies for minimizing its thickness and resistivity while keeping manufacturability well. The base silicon wafer has the function of providing mechanical support; therefore, vertical power MOSFETs for low-voltage application especially require substrates heavily doped with arsenic, phosphorus, or antimony, as well as a post-fabrication wafer thinning process, to achieve the low on-resistance. Power MOSFET device fabrication utilizes epitaxial wafers, which are already pre-deposited in specific epitaxial layers on the n+ substrate. VDMOSFETs and UMOSFETs usually utilize epitaxially grown layers on the substrates, with the base wafer enhanced with specially designed epitaxial layers grown to a precise thickness and doping concentration. Since power MOSFETs utilize heavily doped substrates, special attention must also be paid to substrate polishing, in order to prevent stacking faults and Frenkel defects in the epitaxial layers [7].

In recent UMOSFETs, the unit cell width has become very small, so that special wafers, with features such as exceptional smoothness, are strongly required to insure alignment between the trench mask and specific crystallographic planes. The depth of the trench in gate electrode fabrication must not exceed the n-drift layer thickness during the trench etching process; and as a final fabrication stage, UMOSFET wafers are mechanically thinned and a backside metal is deposited. This backside metal consists of multiple layers

such as titanium, nickel, and silver or gold, in order to obtain an ohmic contact; to provide a solderable low-resistance layer to attach to a lead frame; and to prevent diffusion of the deposited metals into the wafer contact interface. In a recently developed three-step process, the first step involves rough-grit grinding to adjust the wafer to a specific thickness; followed by chemical etching to remove the stress and wafer bow, and complete the thinning; and finally roughening the backside of the wafer surface to improve metal adhesion [7].

13.3 Insulated Gate Bipolar Transistors (IGBTs)

Insulated gate bipolar transistors (IGBTs) were developed in the 1980s as a superior substitute for bipolar power transistors. Though the latter had been utilized for many applications, they had a variety of drawbacks as described in Sect. 13.2.1. The IGBT combines the operational physics of MOSFET and bipolar transistor, as shown in Fig. 13.31. The gate drive signal for the IGBT is applied to the power MOSFET structure, providing the advantages of small size, inexpensive gate circuits that enable high input impedance and voltage-controlled operation. In an operation of the IGBT, the power MOSFET structure supplies electrons to the built-in pnp bipolar power transistor as a base current ($-I_B$), which is in conductivity modulation of the n-drift region, thereby enabling a high collector current (I_c) with low on-state voltage drop. Recently, IGBTs have been utilized in a variety of power electronic apparatus, especially medium and high voltage/current range, such as motor drive application for xEVs (electric vehicles, plug-in hybrid cars, etc.), and uninterruptible power supply (UPS). They continue to play the major role in operating power electronics apparatus, with continual advancement in the devices themselves and in the related packaging technologies.

13.3.1 Background of IGBT Development

In the 1970s, there was a strong need for "self-turn-off" devices, which featured fast switching characteristics with high withstand capability, along with the innovation of control technology such as a pulse width modulation (PWM). To satisfy this need, gate turn-off (GTO) thyristors, which can operate high power, and the Darlington bipolar power transistor with planar type structure and multi-diffusion layers, emerged. The devices show low on-state voltage drop and high current capability, with little base-current control. Moreover, because of the wide reverse biased safe operating area (SOA) and high withstand capability in short-circuit state enabled by optimal design, bipolar power transistors can be highly effective in reducing the power dissipation

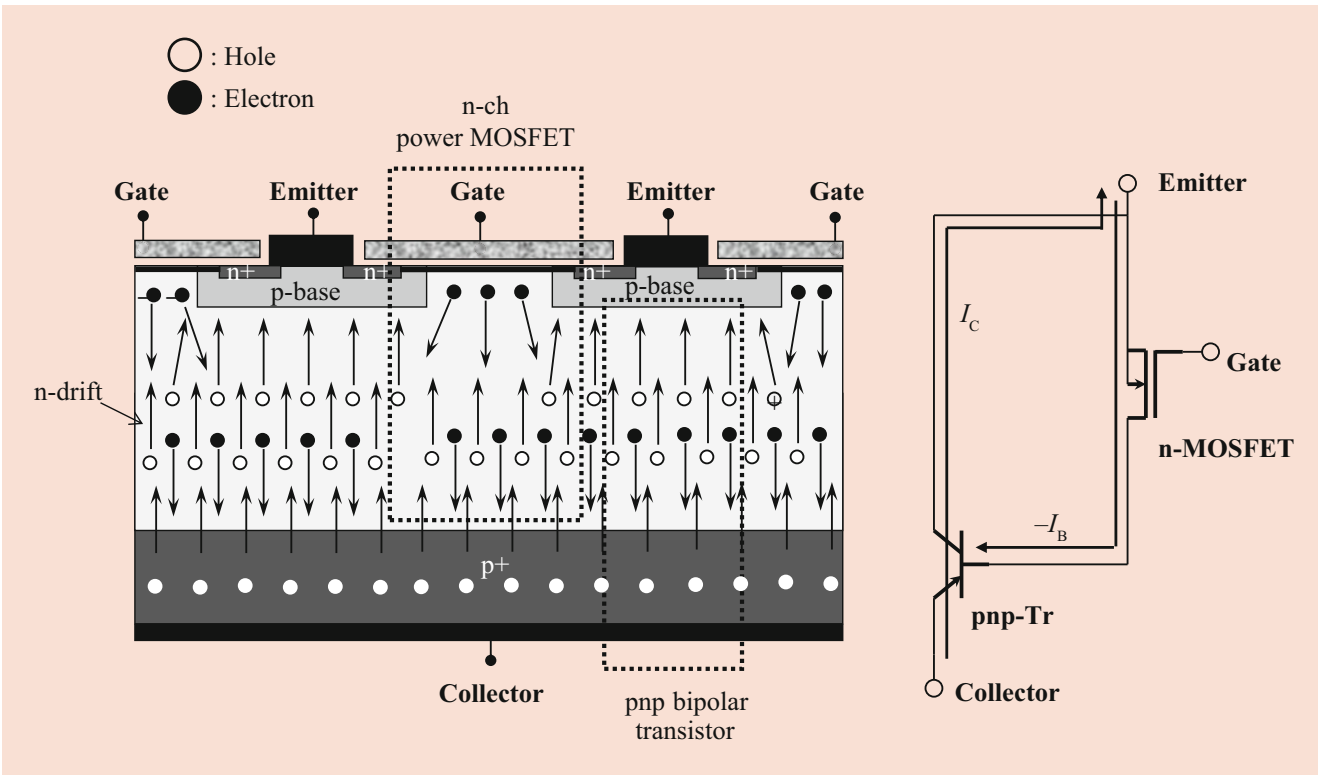


Fig. 13.31 Operational physics of IGBT in the on-state and its equivalent circuit

in voltage source converters, even in high-speed switching operation. Along with these device developments, the package technology advancement, which makes several transistor devices possible to be assembled and connected to each other in a specific circuit configuration, such as three-phase bridge and an H-bridge, in one module, has succeeded in the bipolar transistor power modules development, which have become widely utilized in many power electronics applications.

Power MOSFETs became commercially available in the 1970s, for lower voltage applications such as switching mode power supply, mainly because they require little power for gate control owing to the MOS gate structure, and exhibit very fast switching speeds. In the early 1990s, GTO thyristor and bipolar power transistors still played the major roles for medium- and high-voltage/current applications. However, MOS-gated devices with the fast switching speed were also needed in the case, because carrier frequency in the PWM control increased. Power MOSFETs shows the features of low control power and fast switching, but the on-resistance increases very sharply with the breakdown voltage; as a result, the MOSFET exhibits less power handling capability than bipolar power transistors. For higher power systems, new types of power devices, combining bipolar transistor and MOSFET physics, were presented. Against this background, the IGBT emerged [47, 48]. K. Yamagami et al. presented the principle concept of the IGBT: a wide-base pnp transistor controlled by an n-MOSFET (see Fig. 13.32) [49]; and from the late 1970s to the early 1980s, a number of research groups produced several papers and patents exploring this approach. Scharf and Plummer [50] revealed the first measured results for a lateral type MOS gate thyristor, which operated as a bipolar transistor at relatively low current levels. Baliga showed a MOS gate thyristor in vertical structure, which exhibited high-voltage current saturation at low gate voltage level, with the MOS gate thyristor operating as the wide-base pnp transistor [51]. Plummer developed a MOS gate thyristor with a similar operational mechanism [52]. In 1982, Becke et al. introduced a novel power MOSFET structure with a p anode layer [53]. In the related patent, Becke claimed that the device did not latch up under any operating conditions, meaning that it operated as a pnp transistor at all times. Based upon this patent, in 1983, Russell et al. published measurement results for another novel power MOSFET, the COMFET (conductivity-modulated FET) [54]. In 1982, Baliga et al. presented fabrication and measurement results for an insulated gate rectifier (IGR), as shown in Fig. 13.33 [55]. In this paper, Baliga et al. noted that the parasitic thyristor action should not be activated in normal current range of its operation. Although the device was presented as a rectifier, it was clearly designed as a bipolar transistor with MOS gate. In 1983, GE (General Electric) released the first IGBT product: a power MOS IGBT D94FQ4, R4 with ratings of 400, 500 V, and 18 amperes [56, 57]. However, there was still a problem involved in the practical use of the devices at that time, namely, their poor latch-up withstand capability [58, 59]. Nakagawa et al. [60, 61] overcame this critical obstacle by operating the MOS channel current with a 'non-latch-up' IGBT structure characterized by a surface cell concept of an n+ source and shallow p+ regions with heavy doping (Fig. 13.34); at the same time, solving the SOA problems by means of this structure.

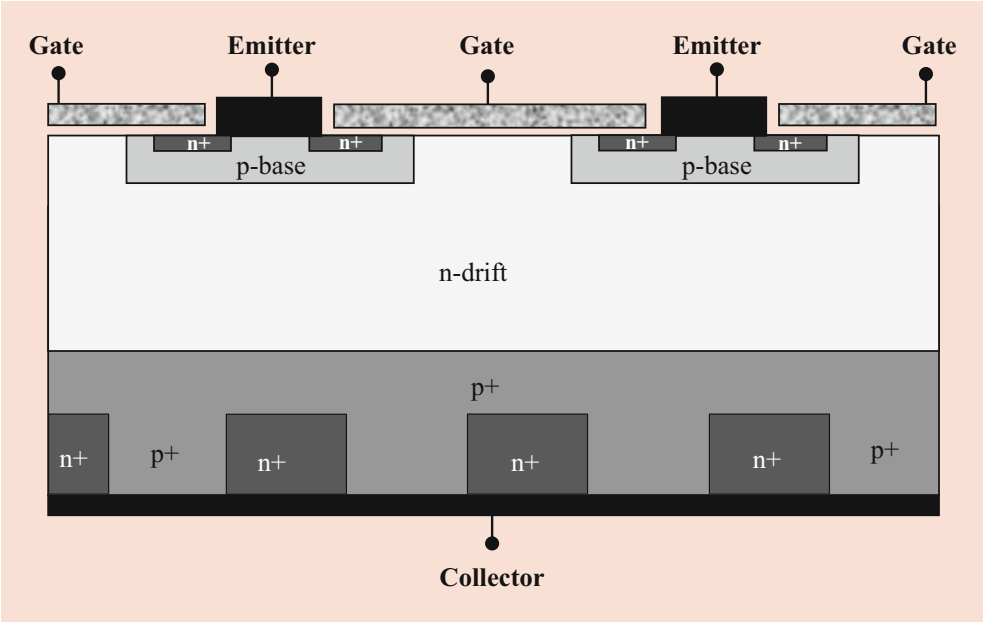


Fig. 13.32 Cross section of a wide base pnp transistor driven by n-ch MOSFET

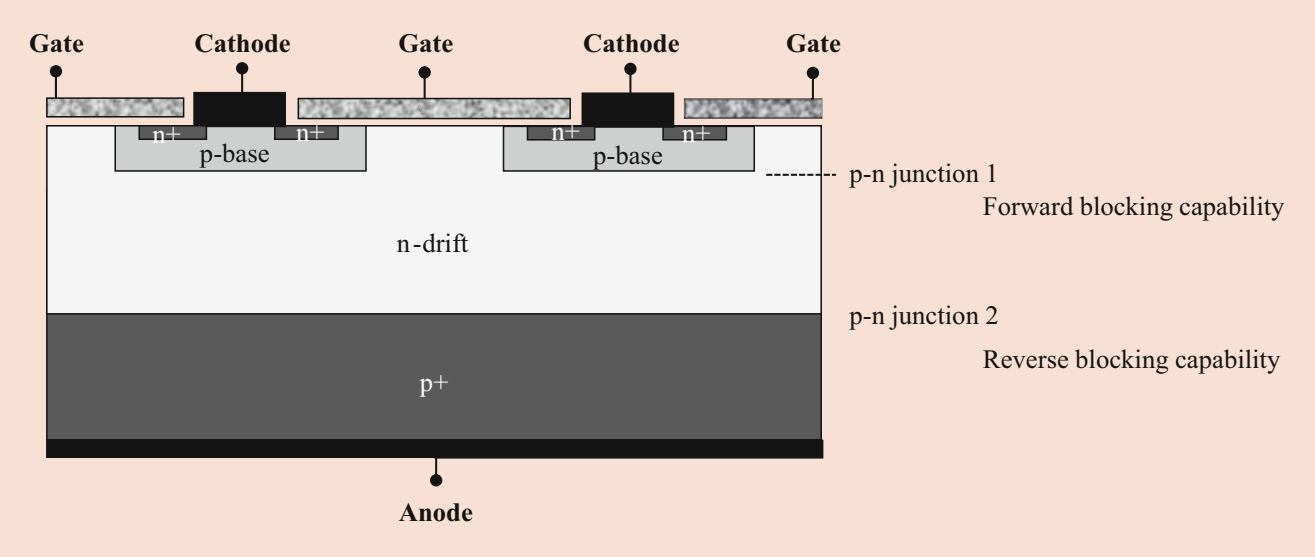


Fig. 13.33 Cross section of the insulated gate rectifier (IGR)

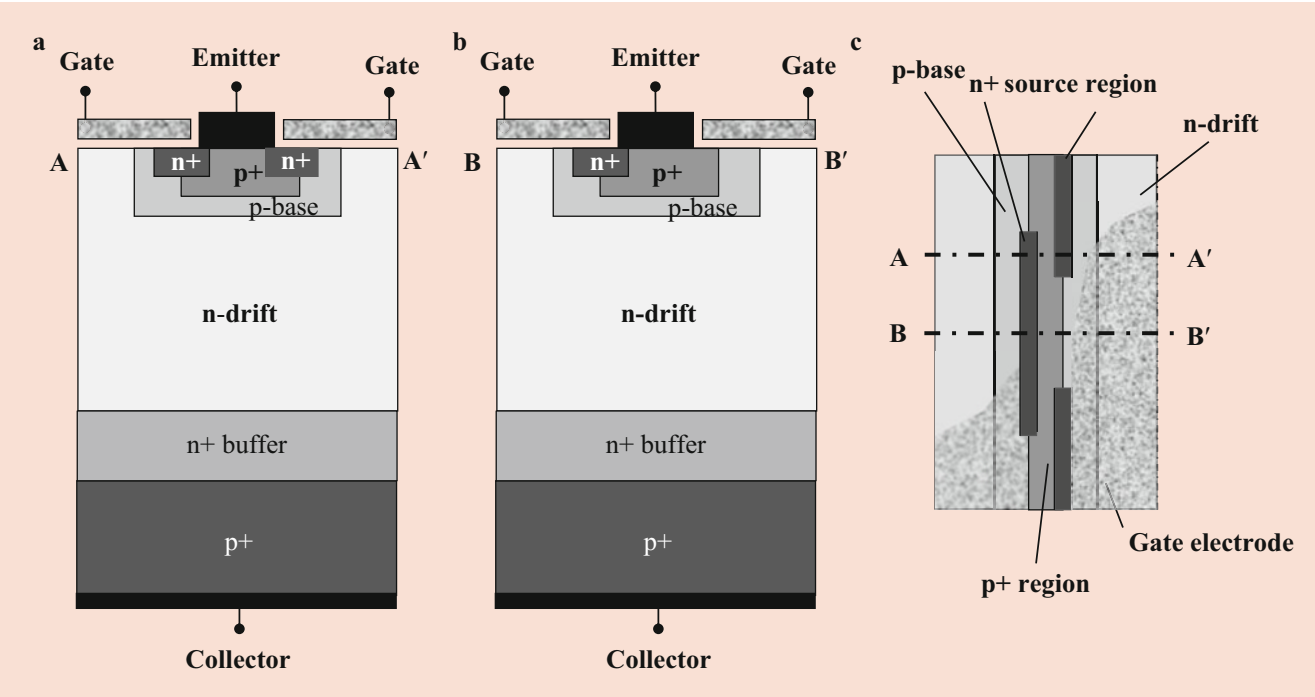


Fig. 13.34 (**a**, **b**) Cross section and (**c**) top view of the non-latch-up IGBT structure. In addition to the application of high impurity p+ region, part of n+ source regions is periodically eliminated in the non-latch-up IGBT structure.

13.3.2 IGBT Structure and Operation

A cross-sectional view of the IGBT structure is illustrated in Fig. 13.35, along with its equivalent circuit. The structure is almost the same with that of the power MOSFET, but with a p+ substrate instead of n+ one; and this structural similarity has enabled quick commercialization of the device, because the IGBT fabrication process is nearly identical to that of the power MOSFET, though the operational physics is absolutely different.

IGBTs have blocking capability both in forward and reverse direction, because the forward voltage can be sustained by the reverse biased p-n junction of the p-base and n-drift regions, and the reverse voltage can be supported by the junction of p+ substrate and n-drift region. However, real commercial devices do not have reverse blocking capability

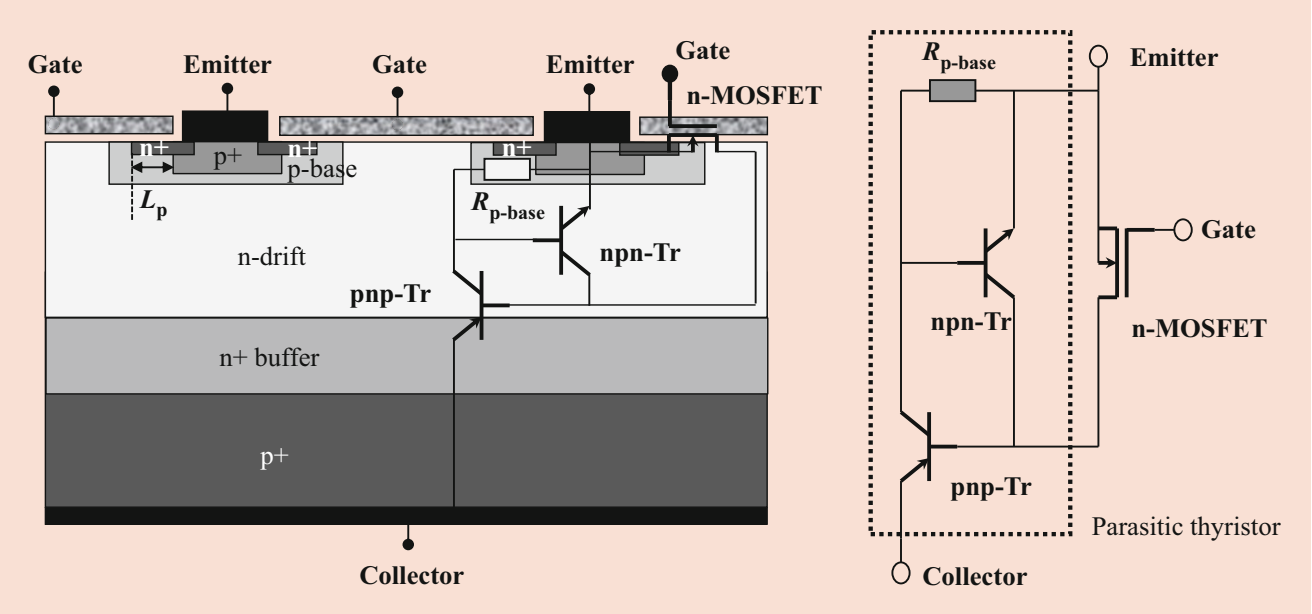


Fig. 13.35 Cross section of the punch-through (PT) type IGBT and its equivalent circuit

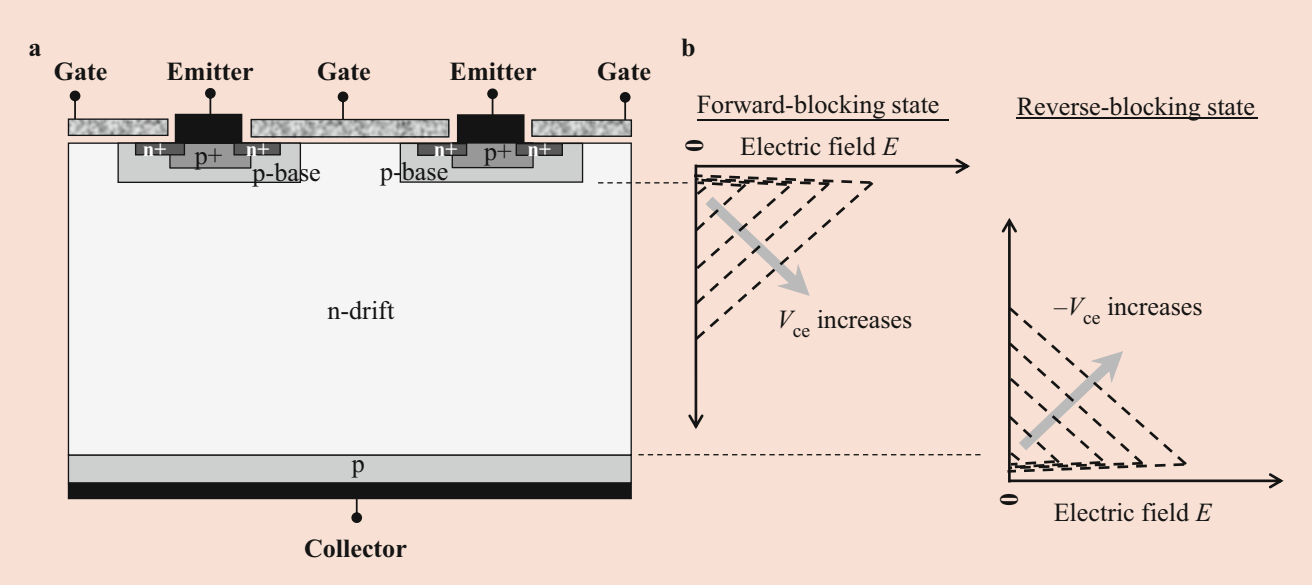


Fig. 13.36 (**a**) Cross section of the non-punch-through (NPT) type IGBT. (**b**) Electric field distribution in forward- and reverse-blocking state in NPT type IGBT

because they have a highly doped n+ buffer layer between the n-drift substrate. This is referred to as a punch-through (PT) structure shown in Fig. 13.35 [62]. In addition, some manufacturers have been developing devices with no n+ buffer layer, named as a non-punch-through (NPT) structure shown in Fig. 13.36 [63].

The current and voltage characteristics of a typical IGBT are shown in Fig. 13.37. With the application of a positive gate voltage over the threshold voltage to form the inversion layer on the surface of p-base region, the device turns on and to its forward conduction state. Electrons can then flow from the n+ emitter region, and after flowing through the inversion layer, the electrons reach the n-drift region. In this state, the backside of the p-n junction is forward biased and holes will be injected from the p+ collector to the n-drift region. Therefore, unlike in a power MOSFET, the collector current starts to increase when the collector voltage exceeds a built-in p-n junction potential of approximately 0.7 V. With the increase of collector forward voltage, the injected hole concentration increases until it exceeds the background

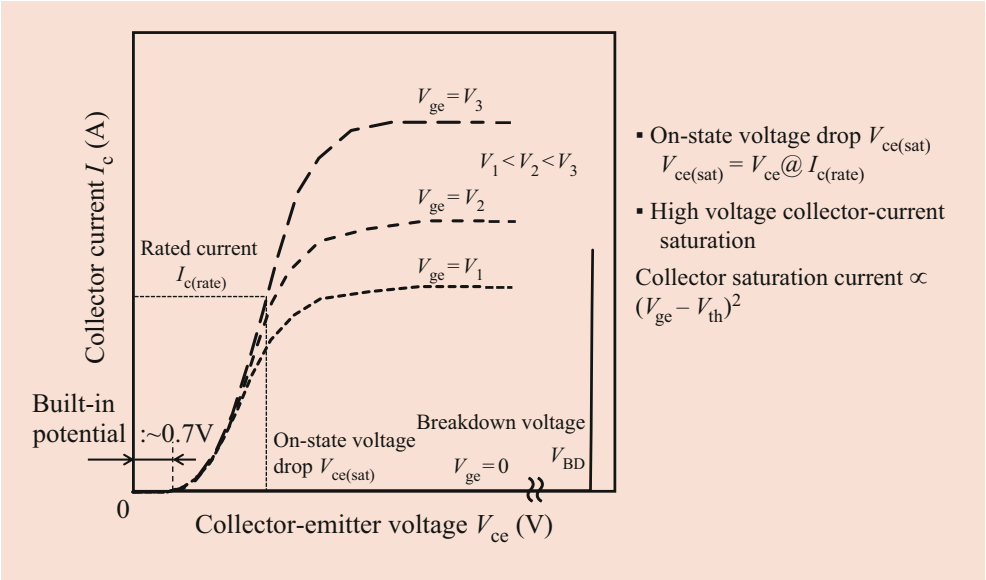


Fig. 13.37 Current and voltage characteristics of typical IGBT

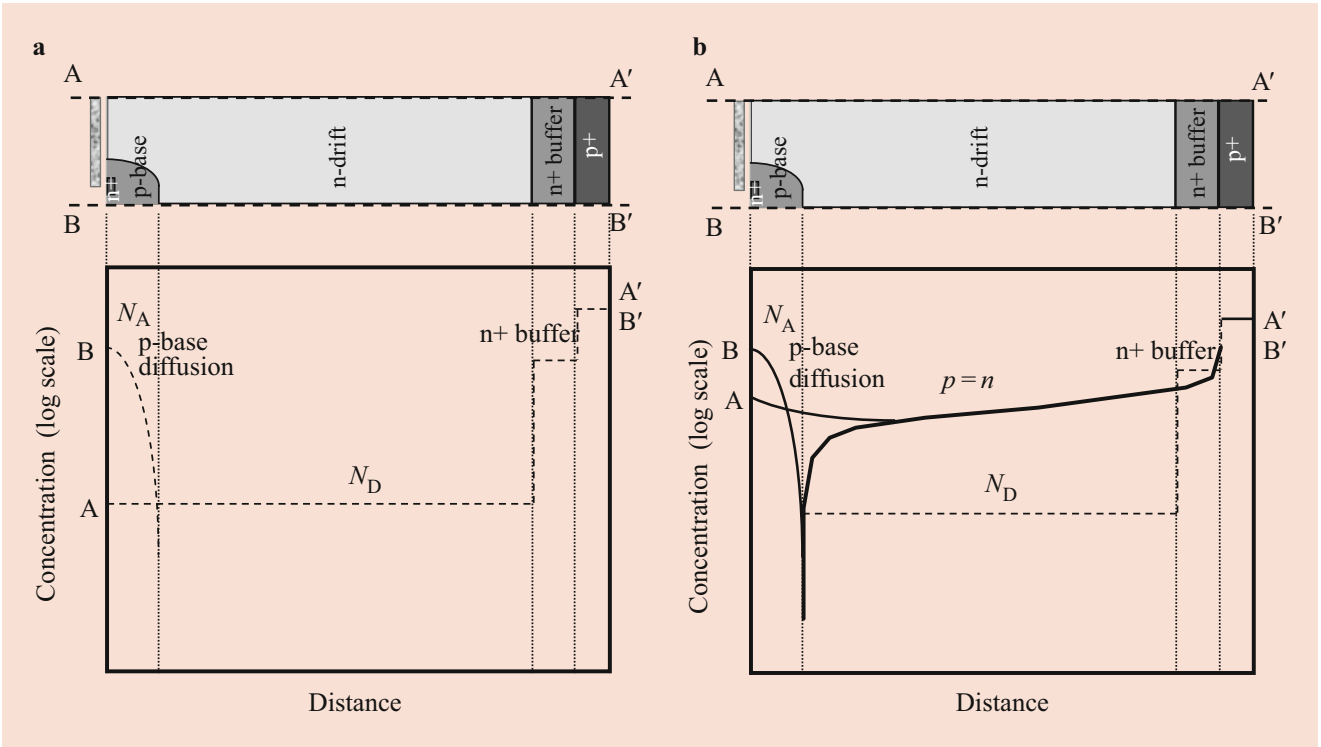


Fig. 13.38 (**a**) Doping profile and (**b**) carrier distribution in the on state within the pnp transistor portion of the PT-IGBT structure

doping level of the n-drift region. The equivalent circuit for the IGBT comprises a wide-base pnp transistor controlled by an n-ch MOSFET in the cascade configuration. In this operational regime, the device behaves like a forward biased wide-base pnp transistor, resulting in high current density operation, with the gate-controlled and high-voltage current saturation characteristics of a power MOSFET. Thus, when the gate voltage is set slightly higher than the threshold voltage, the MOSFET operates in current saturation state, and the IGBT collector current saturates as well (Fig. 13.37).

Figure 13.38 shows the electron and hole plasma distribution in the on-state of PT-IGBT structure, together with the doping profile. As described above, the hole injection from the p+ collector substrate gives rise to great increase in elec-

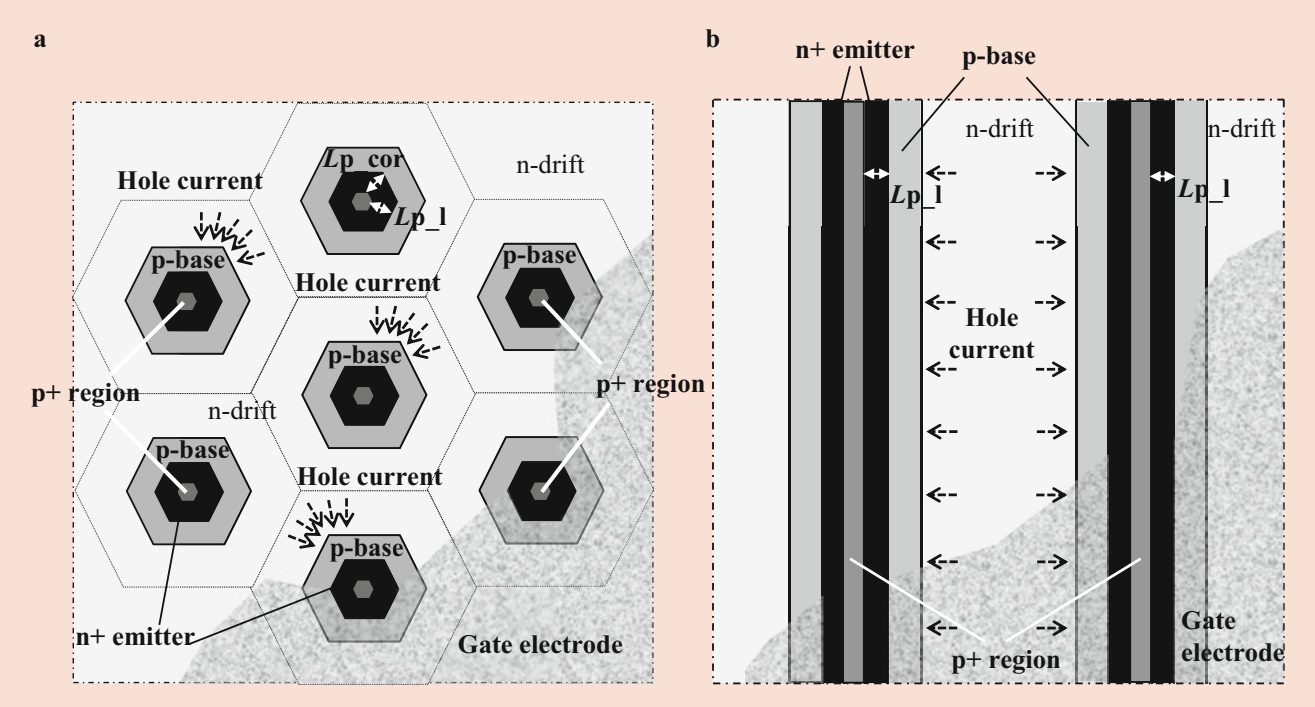


Fig. 13.39 Cell layout and hole current distribution in IGBT structure with (**a**) hexagonal form arranged in hexagonal pattern and (**b**) stripe cell layout

tron and hole concentrations in the n-drift layer, becoming several hundred times higher than the doping density.

In order to switch off the IGBT, it is required to switch the gate voltage off by short-circuiting the gate to the emitter. The operation removes the inversion layer at the surface of the p-base and thus restricts the electron flows to the n-drift layer, initiating the turn-off process. With this, the abundance of electron and hole plasma in the n-drift layer begins to decrease through recombination. The switching behavior is characterized by the rate of this recombination process during turn-off. For low-frequency applications, devices with a relatively long minority carrier lifetime of roughly 10 μs are satisfactory. However, for motor control or high power supply applications, where a turn-off time of less than 0.2–0.3 μs is desired, it is required to minimize the minority carrier lifetime by a lifetime control process like electron irradiation [64]. Unfortunately, IGBTs with a shorter turn-off time exhibit higher on-state voltage drop. Generally, there is a trade-off relation between the on-state voltage drop and the turn-off speed in IGBT structures; however, careful optimization, by controlling the lifetime in the n-drift region and the thickness and doping density of n+ buffer layer in PT-IGBT structures, has resulted in the production of effective commercial devices.

The equivalent circuit shown in Fig. 13.35 has a parasitic thyristor between the collector and emitter electrodes, a structural element characteristic of IGBT structures. Latch-up of this thyristor leads to the loss of gate control and IGBT failure. In the VDMOSFET cell design, square or hexagonal cells arranged in a square or hexagonal pattern have been utilized in order to achieve a larger channel width, resulting in lower on-resistance, as described in Sect. 13.2.2. However, in the IGBT cell design, these VDMOSFET configurations can lead to degradation of the IGBT latch-up capability. The length of the p-base region beneath the n+ emitter (L_p in Fig. 13.35) increases at the corner because the p+ region is formed by a hexagonal window with smaller area, as illustrated in Fig. 13.39 ($L_{p_cor} > L_{p_l}$). In addition, the hole current injected from the backside p+ collector is concentrated at the corner (see Fig. 13.39), so the latch-up current in the hexagonal cells is degraded more than in stripe cells; a characteristic experimentally confirmed in [65]. Therefore, in most IGBT devices, latch-up is suppressed by utilizing a variety of technologies to reduce the resistance $R_{p\text{-}base}$ in the stripe cell structure, as shown in Fig. 13.39. This is aimed at deactivating the npn transistor, so that the IGBT operates as a wide-base pnp transistor controlled by the n-ch MOSFET.

Switching Characteristics

IGBTs are utilized in many power electronics systems, such as motor drive for consumer and industrial applications, to control the power delivered to the inductive load. The typical circuit configuration and switching waveforms of collector current, and collector and gate voltages are illustrated in

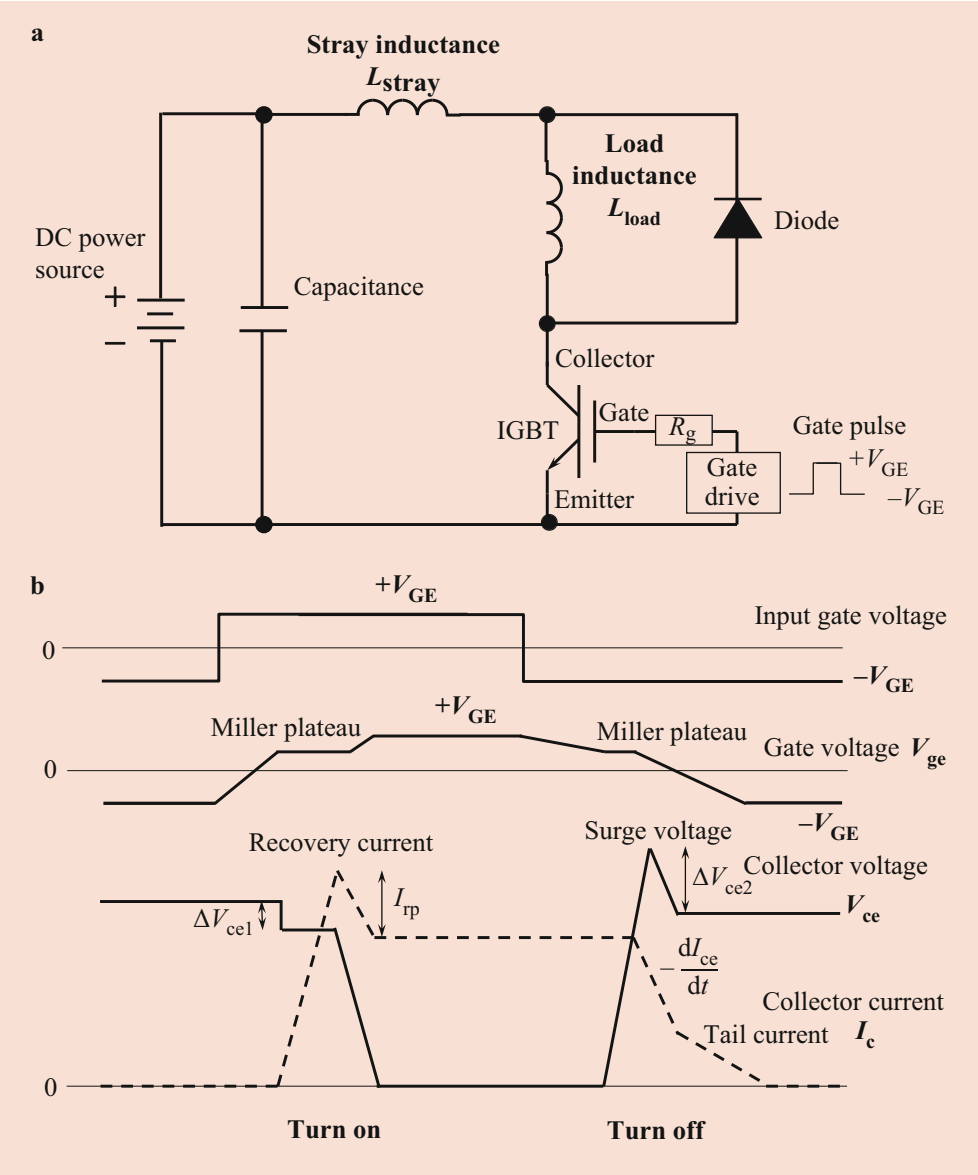


Fig. 13.40 (**a**) Inductive load circuit configuration. (**b**) Schematic of IGBT Inductive load switching waveforms

Fig. 13.40. After turn-on, the IGBT current increases rapidly and gets to an apex point defined by the total amount of the load current and peak reverse recovery current of the diode. After this, the IGBT operates in its forward conduction state, with almost constant collector current flow. When turned off, its collector current decreases by sweeping the stored electron-hole plasma in the n-drift region out and electron-hole recombination. The switching behavior of IGBTs is more complicated than that of power MOSFETs, because of the holes injected from the p+ collector; thus, in this section, the relevant processes will be discussed through investigation of the turn-on and turn-off physics of the IGBT structure.

The turn-on current and voltage waveforms for an inductive load are shown in Fig. 13.41, and details of the stored-carrier dynamics, and electric field and voltage distribution for the turn-on in the PT IGBT with trench gate are shown in Fig. 13.42. These results were derived using two-dimensional TCAD mixed-mode device simulations. The circuit comprises the IGBT and an inductive load, connected in series with the power source by a free-wheeling diode. With IGBT turn-on, the free-wheeling current still flows through the diode. When the gate bias is switched on ("A" in Fig. 13.41), the gate voltage begins to slowly increase due to the capacitance components of the IGBT and the connected gate resistance R_g. The collector current increases while the load is clamped to the source voltage by the conducting free-wheeling diode. When the V_{gs} reaches the threshold voltage V_{th}, the IGBT operates in the active region and the collector current starts to flow. This is a similar mechanism to that of the power MOSFET described in Sect. 13.2.2, but with the addition of backside hole injection from the p+ collector. The collector current flows, due to IGBT operation,

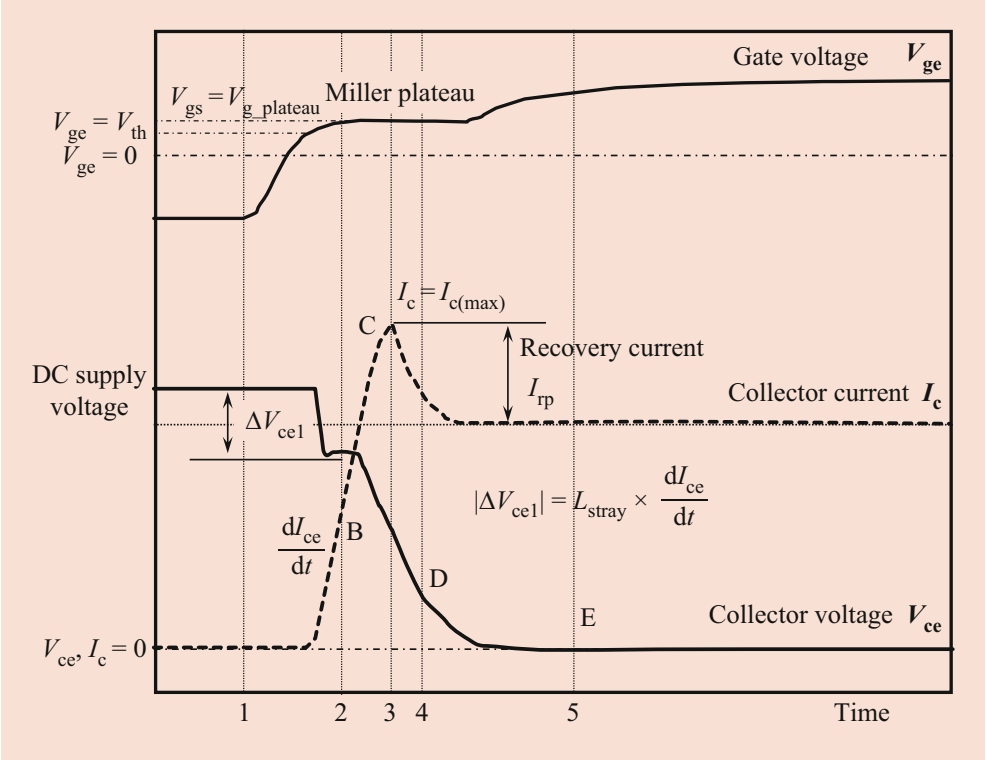
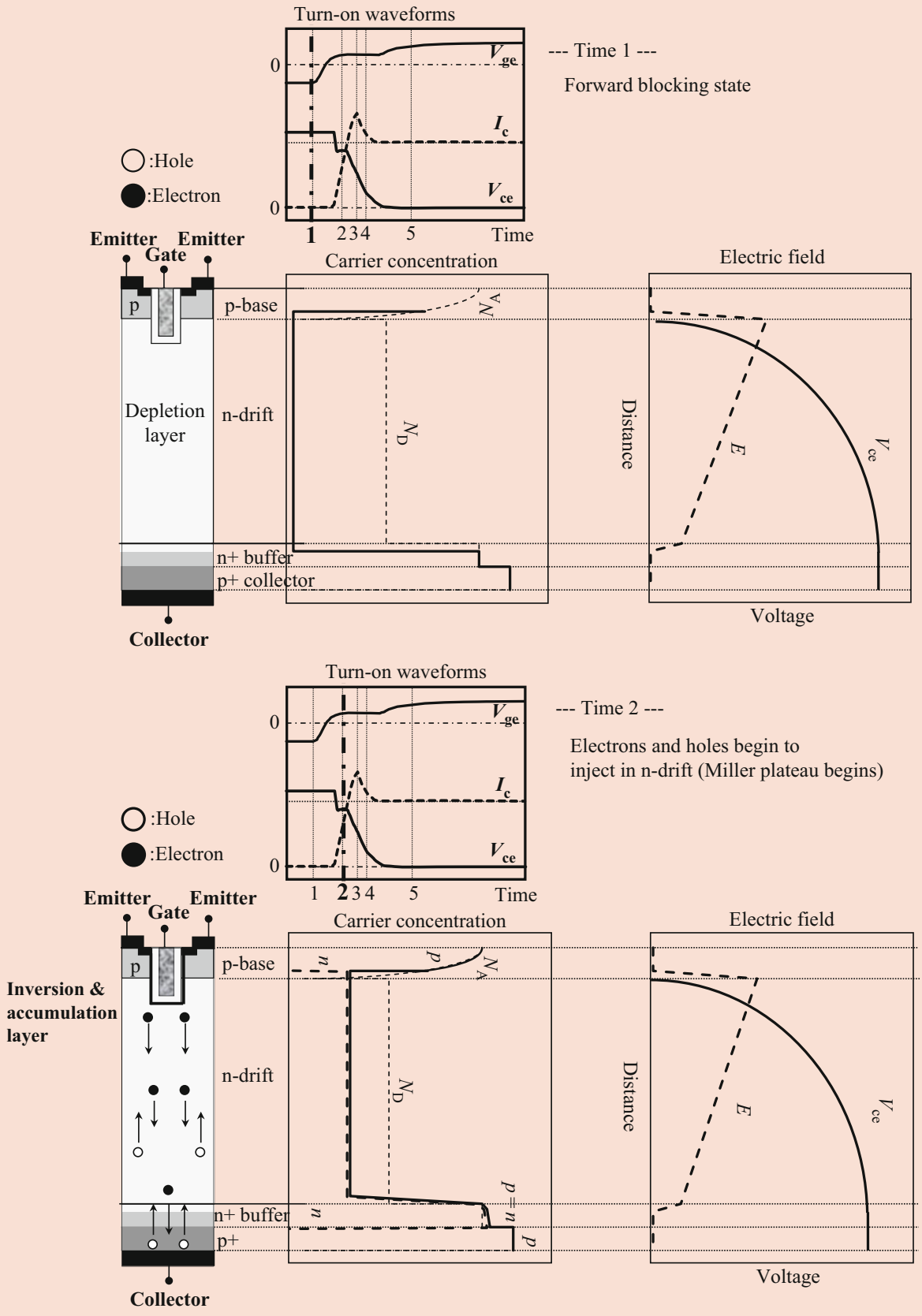


Fig. 13.41 IGBT turn-on waveforms with an inductive load

after the gate voltage increases above the gate threshold voltage. In this regime, the IGBT supports a high collector voltage by expanding the depletion layer in the n- layer ("B" in Fig. 13.41; Time 2 in Fig. 13.42); therefore, there is no conductivity modulation region in the n-drift layer. In Fig. 13.41, the collector voltage drop ΔV_{ce} can be seen in this period. The voltage drop is caused by a constant increase in the IGBT collector current (dI/dt), multiplied with stray inductance L_{stray} in the circuit ($L_{stray} \times dI/dt$). The IGBT current increases and gets to an apex $I_{c(max)}$ defined by the total amount of the load current and the peak reverse recovery current in the free-wheeling diode ("C" in Fig. 13.41; Time 3 in Fig. 13.42), and then the collector current is reduced to a load current. At the same time, the collector voltage V_{ce} starts to fall ("D" in Fig. 13.41; Time 4 in Fig. 13.42), and the voltage continues to fall until it reaches the on-state value ("E" in Fig. 13.41; Time 5 in Fig. 13.32). Finally, the gate voltage starts to increase and continues to do so as long as the gate current I_g flows.

Figure 13.43 shows the inductive load turn-off current and voltage waveforms, and Fig. 13.44 details the stored-carrier dynamics, and electric field and voltage distribution for in the PT IGBT with trench gate. The circuit is comprised of the IGBT and an inductive load, connected in series with the power source, with a clamping diode across the load to transfer the current when the IGBT is turned off. When the gate bias is switched off ("A" in Fig. 13.43, Time 1 in Fig. 13.44), the gate voltage begins to slowly decrease due to the capacitance components of the IGBT and the connected gate resistance R_g. The collector current keeps flowing at its on-state level because of the inductive load ("B" in Fig. 13.43). This collector current is sustained due to pnp bipolar transistor operation, even after the gate voltage drops below the threshold voltage. In this regime, the base current of the pnp transistor is supplied via electron flow due to depletion layer expansion (Time 2 in Fig. 13.44). When the collector voltage reaches the level of the power supply voltage (Time 3 in Fig. 13.44), the current starts to transfer from the IGBT to the diode. Thus, the current initially decreases abruptly ("C" in Fig. 13.43) and then decreases gradually with an exponential shape, through the electron-hole recombination in n-drift layer near the p+ collector side ("D" in Fig. 13.43; Times 4 and 5 in Fig. 13.44). This simultaneous presence of high voltage and current leads to large power dissipation in the IGBT, so it is required to lower the level of the tail current and to shorten the time duration of the turn-off operation.

It should be noted that the sharp increase in the collector or surge voltage ("E" in Fig. 13.43) is caused by a sudden decrease in the IGBT collector current (dI/dt) associated with stray inductance L_{stray} in the circuit ($L_{stray} \times dI/dt$). Therefore, optimal design of the forward voltage drops, turn-off characteristics, and surge voltage reduction in the IGBT are also strongly required in order to achieve superior circuit



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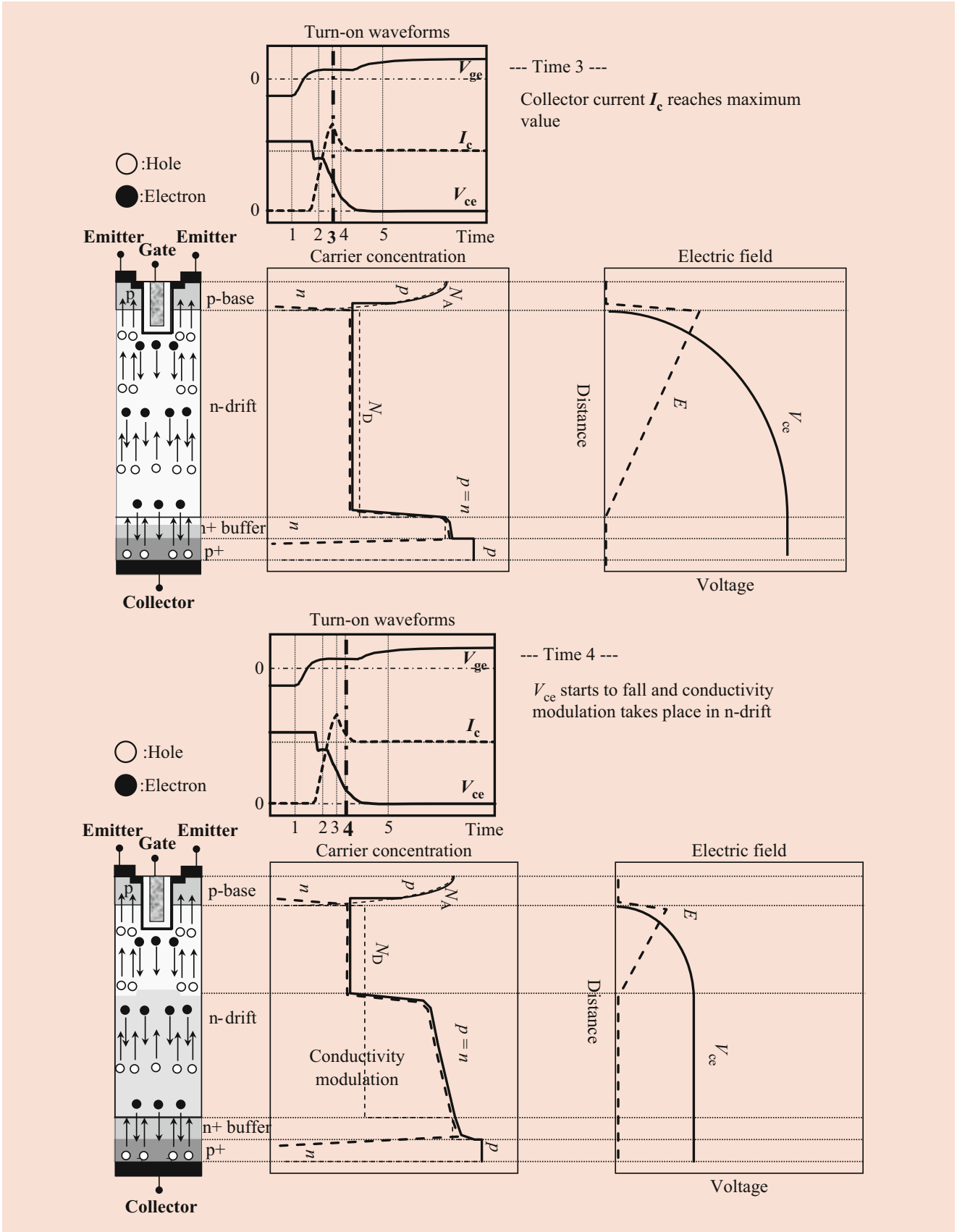

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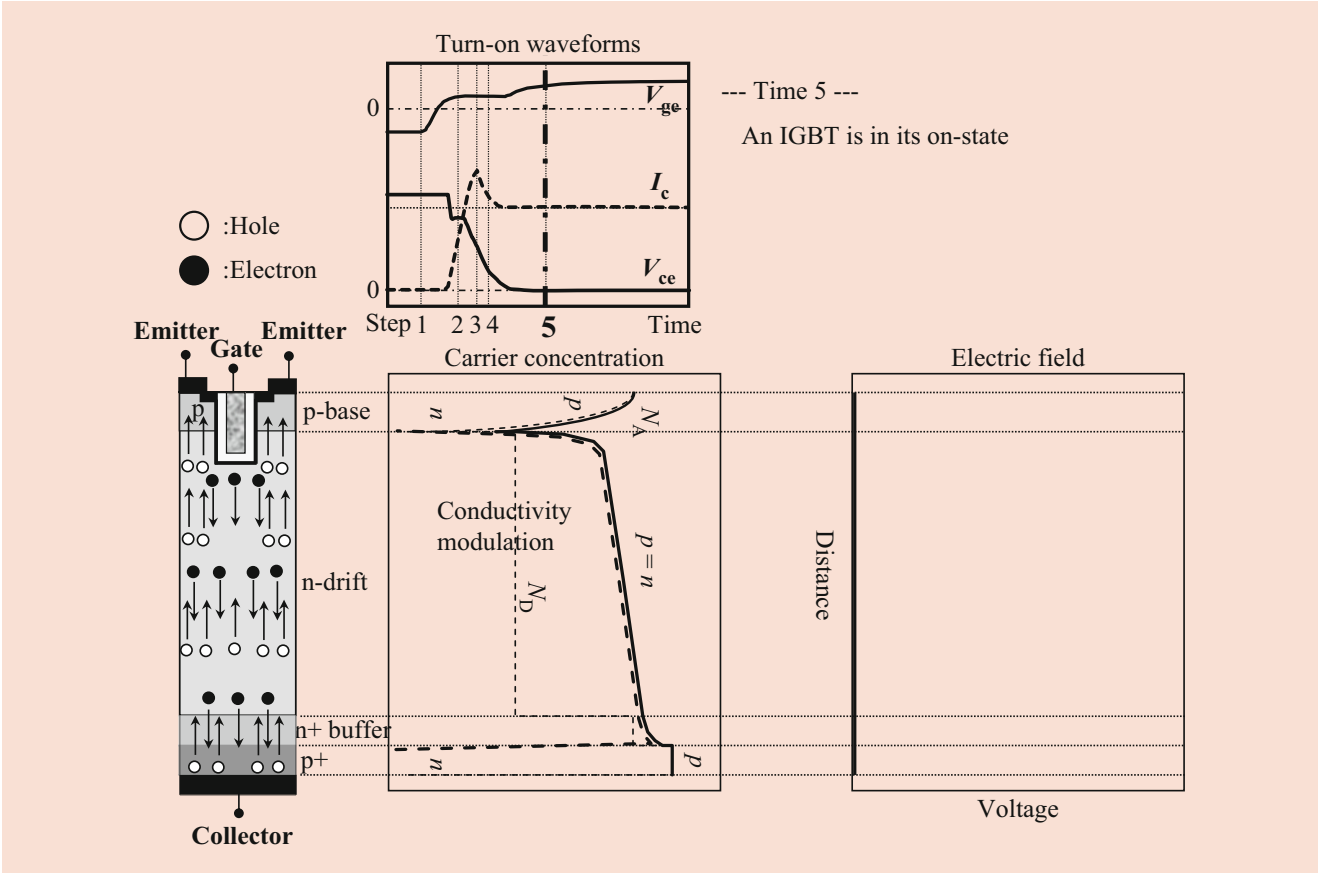


Fig. 13.42 Trench IGBT carrier dynamics, electric field, and voltage distribution during an inductive turn-on operation

efficiency in the voltage source converters. Finally, the collector current falls to zero and the off-state is reached (Time 6 in Fig. 13.44).

13.3.3 IGBT Safe Operating Area

Reverse-Biased SOA

Among the IGBT characteristics, high withstanding capability is extremely important, along with low on-state voltage drop and fast switching speed. With the recent widespread adoption of hybrid and electric vehicles, IGBT destruction during travel represents a serious, even life-threatening danger. As described above, the parasitic thyristor latches up when a large current flows; and avalanche breakdown, which occurs when a large voltage is applied between the collector and emitter, also causes IGBT breakdown. In general-purpose motor drive control applications, for example, there are two operation modes in which the IGBT is most likely to breakdown: IGBT turn-off and load short circuit, in which high voltage and current are applied over the same period.

In an IGBT, the safe operating area (SOA) refers to a voltage/current area that can be safely turned off without breaking. This IGBT turn-off SOA is referred to as a reverse biased SOA (RBSOA). Most of the current IGBTs guarantee that they can be turned off up to twice the rated current within the rated voltage range. The SOA is represented by a rectangle whose horizontal axis is the collector voltage and vertical axis is the collector current (Fig. 13.45). To evaluate an RBSOA, an inductive load circuit, with the assumption of motor load, is generally utilized (Fig. 13.40a). However, the real RBSOA of an actual IGBT is designed to be larger than this rectangle. The maximum turn-off current is determined by the minimum current that will trigger latch-up of the parasitic thyristor, and the maximum applied voltage is determined by the avalanche breakdown voltage at each turn-off current. The minimum current to trigger latch-up of the parasitic thyristor is almost independent of the collector voltage, because it is determined by the parasitic npn transistor structure, as described above. On the other hand, the avalanche breakdown voltage strongly depends on the level of the turn-off collector current. When the turn-off current is zero, the avalanche breakdown voltage is equal to the breakdown voltage between emitter and collector electrodes. However, when the turn-off current starts to increase, mobile holes flow through the depletion layer with the application of high collector voltage (Time 3 in Fig. 13.44); thus, not

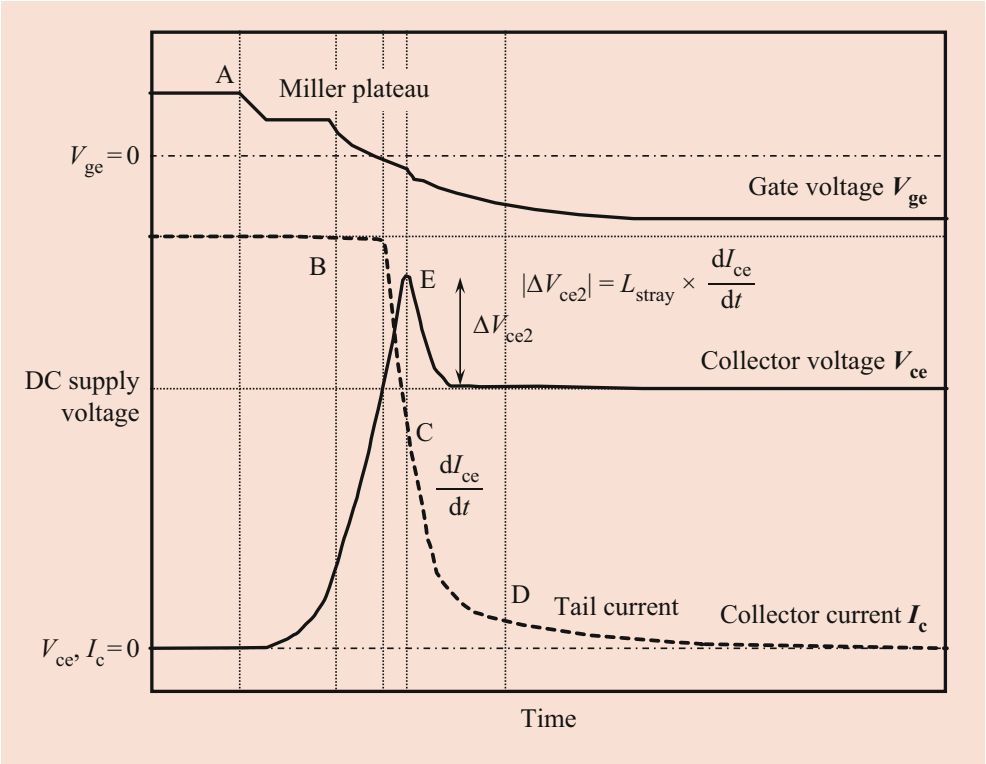


Fig. 13.43 IGBT turn-off waveforms for an inductive load

only the ionized donor density N_D, but also the mobile hole density p, is present in the depletion layer, resulting in increased positive charge there. Therefore, the depletion layer width W_{dep} decreases with the turn-off current, and is expressed as

$$W_{dep} = \sqrt{\frac{2\varepsilon_{Si} V_{ce}}{q\,(N_D + p)}}, \tag{13.41}$$

where N_D is the donor concentration, p is the mobile hole density in the depletion layer, and V_{ce} is the applied collector voltage. We can see that the N_D component in the denominator has changed from that of Eq. 13.7 to $(N_D + p)$; thus, the depletion layer expansion is suppressed by the increased hole concentration at collector current turn-off, resulting in reduction in the avalanche breakdown voltage.

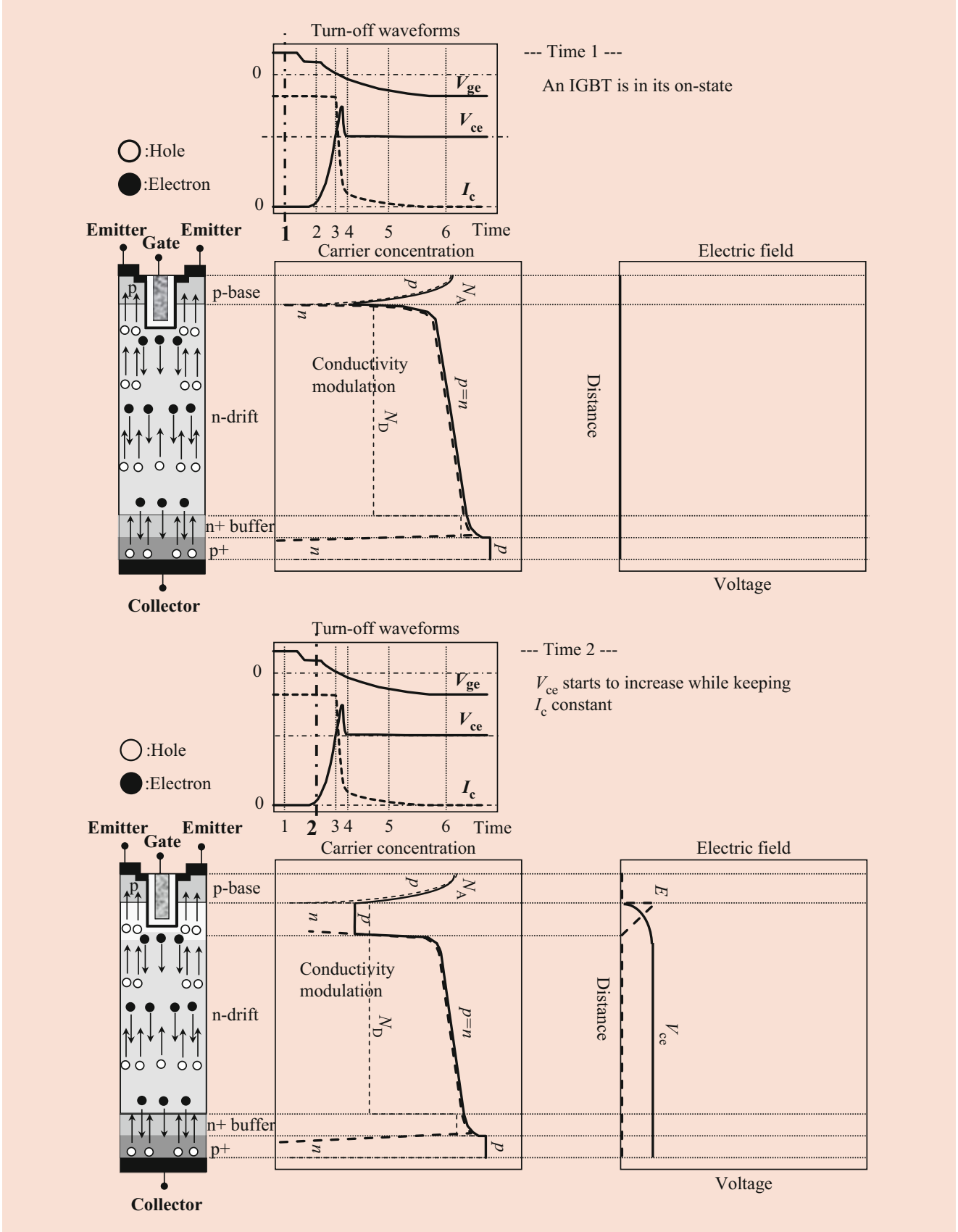
Short-Circuit SOA

If a load connected to an IGBT is shorted for accidental reasons, a high DC voltage is immediately applied directly to the IGBT, and high collector current instantaneously flows because the gate has already been activated. Since an IGBT has high-voltage current saturation characteristics, collector currents are suppressed below a certain specified level. In this situation, the IGBT is subjected to simultaneous high-voltage and high-current duty, and it is necessary to remove the duty as rapidly as possible. The time from the occurrence of the load short circuit to the safe interruption of the current, without destruction of the IGBT, is termed the short circuit SOA (SCSOA), and current IGBTs guarantee roughly 10 μs (at 125 or 150 °C). Figure 13.46 shows a measurement circuit for the SCSOA, as well as typical collector voltage and current waveforms in SCSOA measurement. A number of published studies have analyzed the device failure mechanism, and a detailed analysis has been made in [66]. Here, the IGBT failure mechanism in the short-circuit state is illustrated in Fig. 13.47 and summarized as follows:

(i) The parasitic thyristor latch-up ("A" in Fig. 13.47)
Breakdown due to latch-up of the parasitic thyristor. In the latest IGBTs, the latch-up withstanding capability is sufficiently high, and the device is unlikely to be destroyed by this event.

(ii) Avalanche breakdown ("B" in Fig. 13.47)
Breakdown as a result of an increase in the electric field strength on the p+ collector layer side due to low hole-injection efficiency.

(iii) Dissipated energy destruction ("C" in Fig. 13.47)
Temperature rise in the device due to energy dissipation from high voltage and current flowing at the same time. Finally, destroyed by thermal runaway. A frequently observed cause of failure.



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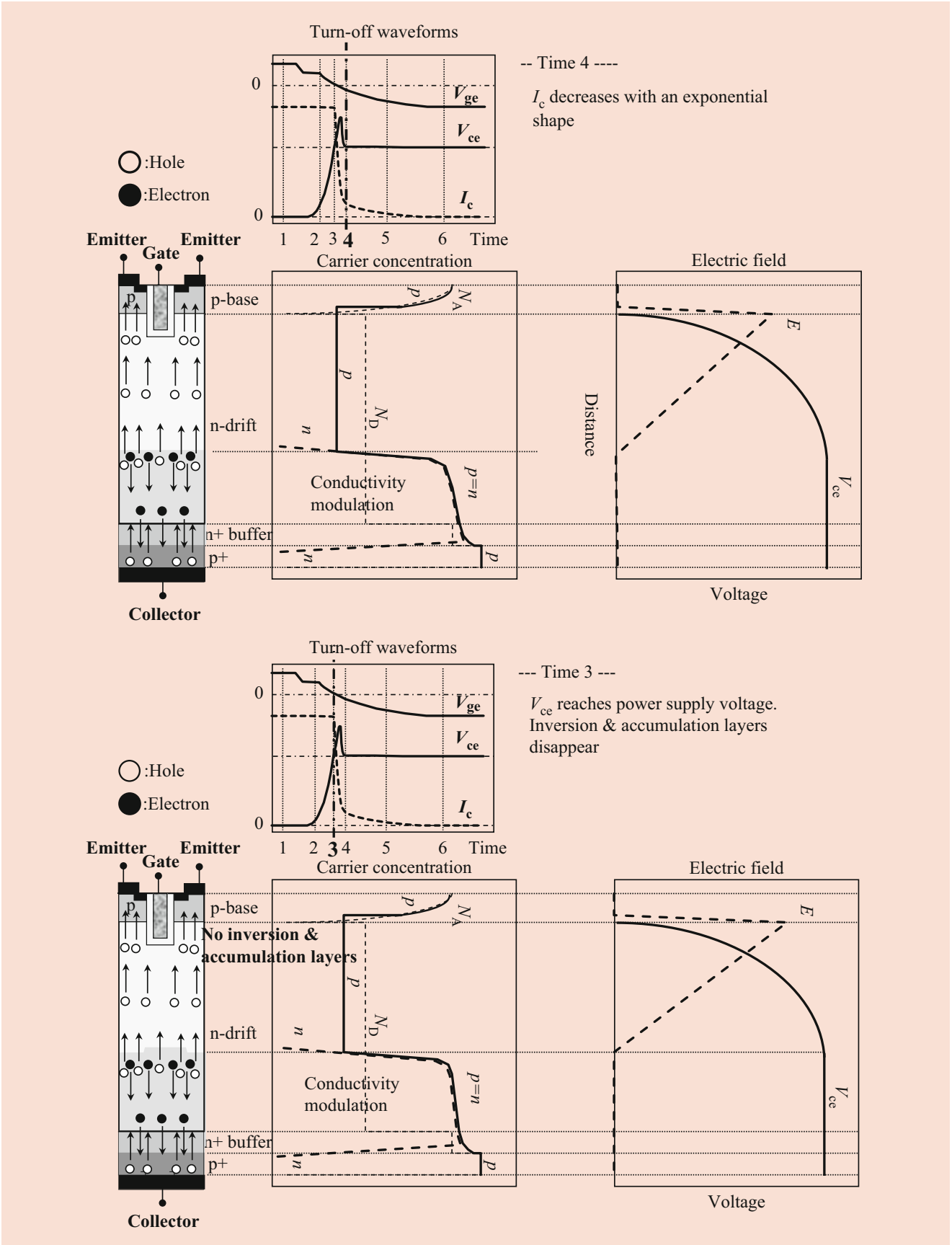

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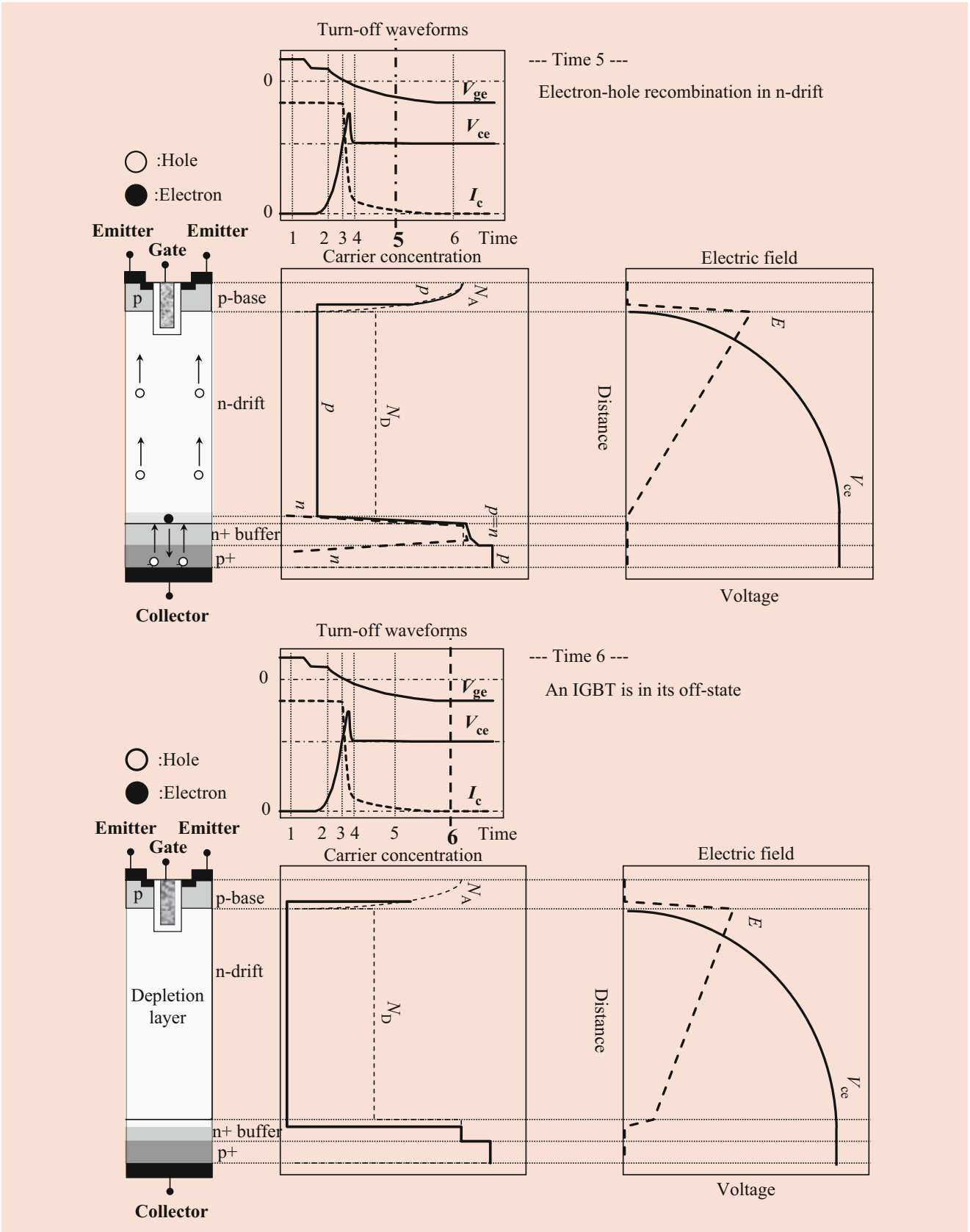


Fig. 13.44 Trench IGBT carrier dynamics, electric field, and voltage distribution during an inductive turn-off operation

(iv) Turn-off breakdown ("D" in Fig. 13.47)
Breakdown by avalanche generation due to collector surge voltage generated by the product of dI_c/dt and the stray inductance (L_{stray}) of the measurement circuit. This can be avoided by increasing the gate resistance to reduce the turn-off dI_c/dt.

(v) Thermal runaway destruction ("E" in Fig. 13.47)
Temperature rise in the device due to energy dissipation, followed by thermal diffusion to the p+ collector layer side after turn-off, resulting in leakage current increase. Finally, destroyed by thermal runaway. This is occasionally found in thin wafer IGBTs.

State-of-the-art IGBTs are rarely broken by (i) latch-up, (ii) avalanche breakdown, or (iv) turn-off breakdown, due to the advanced design technology; instead, (iii) energy dissipation and (v) thermal runaway destruction are the major causes of device failure. These two failure modes are due to the energy dissipated during high voltage and current flows. Therefore, it is required to suppress high current flow in the device, for improving failure tolerance; however, this leads to an increased on-state voltage drop meaning that the IGBT on-state voltage and SCSOA are in a trade-off relation.

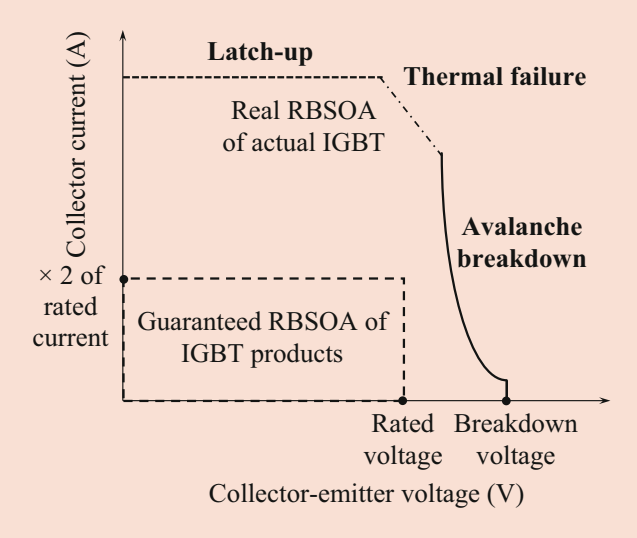


Fig. 13.45 Reverse biased SOA (RBSOA) of IGBT

13.3.4 Evolution of the IGBT Structure and Design Concept

The IGR (insulated gate rectifier) was a serviceable MOS gate bipolar transistor device. However, its turn-off speed was too slow, and its RBSOA [55, 56] and SCSOA were too small, to offer a superior substitute to the power bipolar transistor, though Nakagawa [60, 61] solved the SOA problems with the non-latch-up structure described above. To improve the switching characteristic, Goodman et al. developed a new type of IGBT, with an n^+ buffer layer between the n-drift region and p+ collector [62]. With this modification, the IGBT can achieve fast switching speed by a lifetime control process, with almost no sacrifice of the on-state characteristics. Further innovation is required for the IGBT if a breakthrough is to be achieved in the trade-off relation between low on-state voltage drop, fast switching speed, and high withstand capability. Therefore, as in the case of integrated circuits, a lot of the most sophisticated technological innovations are being utilized to the IGBT structure, with the aim of mitigating, if not overcoming, this trade-off relation. Among them, the technologies for IGBT cell design and fabrication process have been leading to advancement in the device characteristics.

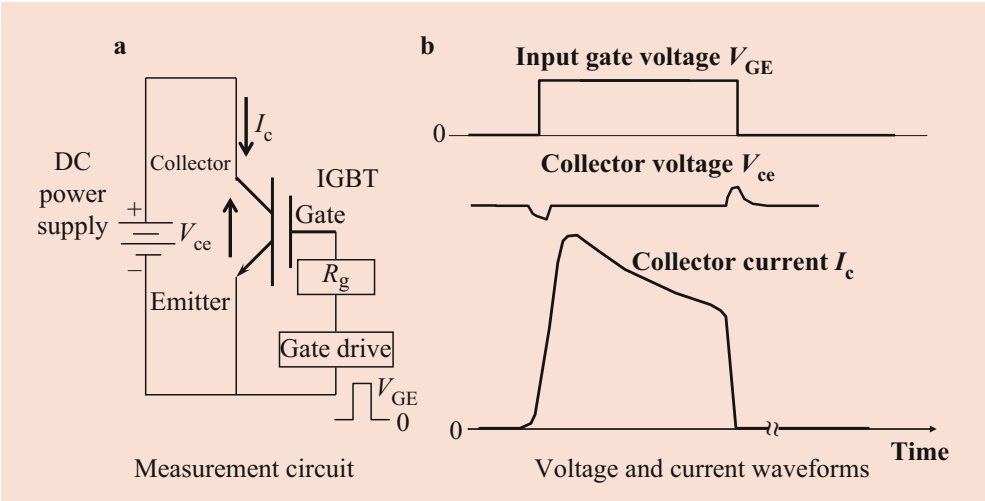


Fig. 13.46 Voltage and current waveforms in IGBT SCSOA measurement. (a) Measurement circuit. (b) Voltage and current waveforms

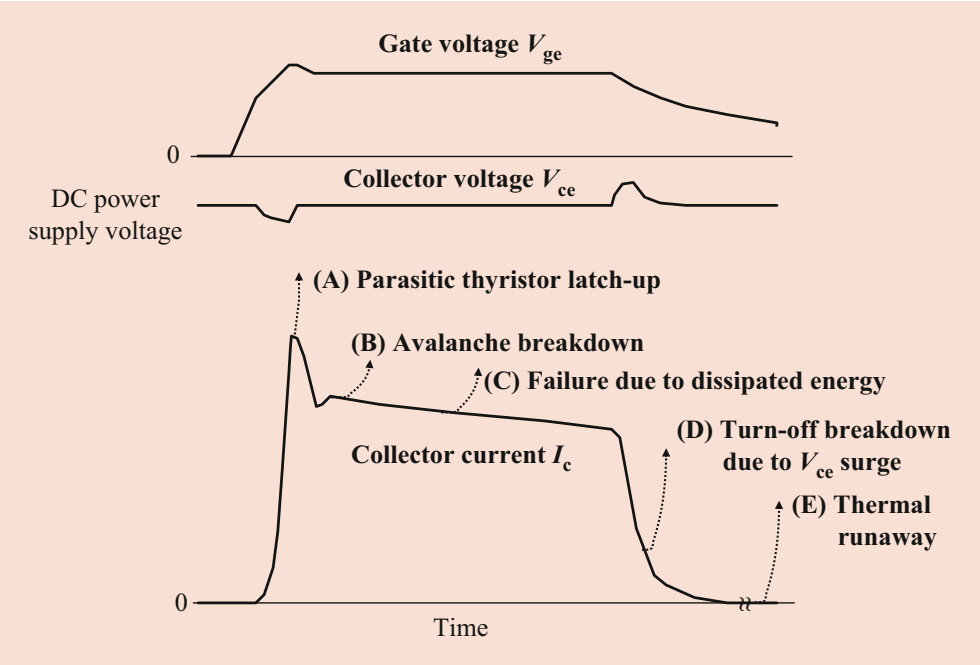


Fig. 13.47 Failure mechanisms in IGBT SCSOA measurement

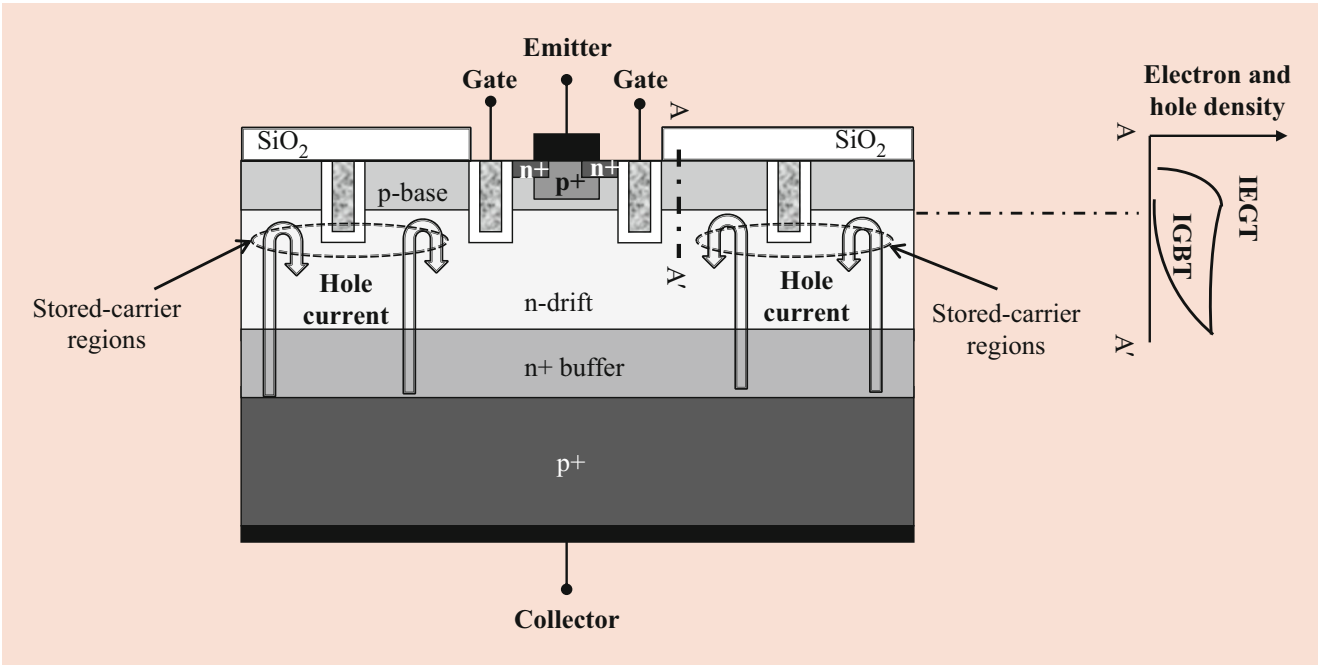


Fig. 13.48 Cross section of IEGT structure and comparison of schematic carrier distribution between IEGT and IGBT

The IGBT has the power MOSFET structure with p^+ collector substrate, so that the design and fabrication process technologies are similar with those of the power MOSFET. Hence, trench-gate technologies have been utilized to improve the on-state voltage drop, and the trench IGBT was ultimately developed by utilizing cutting-edge U-LSI (ultra-large-scale integrated circuit) design and process technologies. After this, several important breakthroughs in design and understanding followed for IGBT improvement. Initially, there had been many works to incorporate trench gate technologies into the IGBT, with a common approach being the creation of a trench structure with a very fine cell pitch [67]. However, in this case, the device has a huge channel width, unable to control short-circuit conditions without the addition

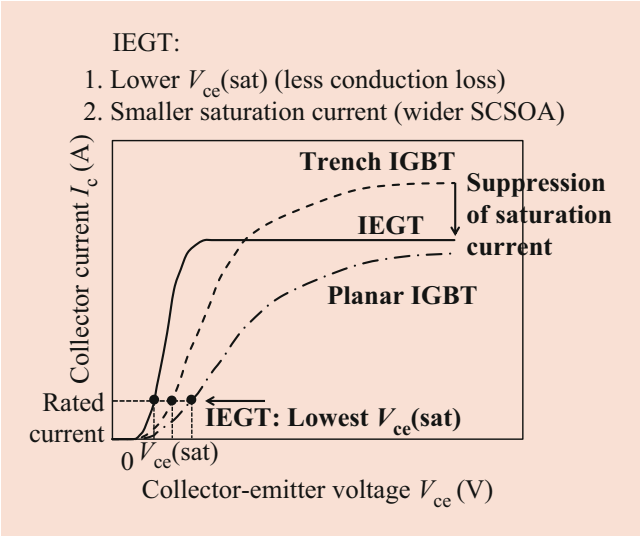


Fig. 13.49 Comparison of I–V characteristics between IEGT, trench IGBT, and planar IGBT

of an internal or external circuit for current limitation, such as was utilized in some IGBTs with planar gate [68]. Moreover, the electron-hole plasma distribution was not suitable for enabling lower on-state voltage drops.

In one important approach to addressing these issues, Kitagawa et al. proposed utilization of the injection enhancement (IE) effect [69] and developed the IEGT (injection enhanced gate transistor) device shown in Fig. 13.48. This configuration achieves an extremely lower forward voltage drop, through an improvement in the gate structure that increases the resistance to hole current flow into the emitter electrode, which results in enhancement of electron-hole plasma around the device surface. The structure became widely used in IGBT development and is still utilized in current IGBT devices.

Figure 13.49 shows another effect of the application of the IEGT structure. By eliminating some of the gate and emitter electrodes from the surface, the total channel width in the IEGT structure is reduced, which in turn reduces the saturated current level in the device. This results in wider SCSOAs, with lower on-state voltage drop; and this means that the device achieves lower on-state voltage drop and higher short-circuit withstanding capability at the same time. Alternative IGBT structures, which included an additional doped n layer underneath the p-base of the trench and/or planar cells, were developed by Takahashi et al. (the CSTBT, or carrier stored trench-gate bipolar transistor) [70] and M. Mori et al. (the HiGT, or high-conductivity IGBT) [71], respectively. Laska et al. developed a 1200 V trench IGBT device which attempted to optimize the cell design in terms of size, distance, and shape for enabling lower on-state voltage drop and wider SCSOA, simultaneously [72].

The IGBT products in early days below 1200 V were fabricated based on a design concept involving an n- epitaxial layer grown on a p^+ substrate. The design concept led to an extremely high hole injection from the p+ collector, requiring strong lifetime control to get fast switching speed and resulting in a relatively poor SCSOA and unsuitability for operating in parallel. Thus, Miller et al. developed a new type of bulk IGBT structure, a non-punch-through (NPT) IGBT [63], with the following characteristics:

(i) Utilizable with inexpensive floating zone (FZ) bulk wafer
(ii) Thinner wafer thickness needed
(iii) Low hole injection from the p collector
(iv) Non-requirement of lifetime control

With its low hole injection and non-requirement of lifetime control, the NPT IGBT attains an almost flat electron-hole plasma distribution, enabling both on-state voltage drop and faster switching speed, and offers the further advantage of a positive temperature coefficient in the forward current. This makes the NPT IGBT suitable for operating in parallel, resulting in easy use in high power applications. Notably, it also exhibits wider RBSOA and SCSOA owing to the thicker n-drift region, leading to minimization of electric field in the device. Consequently, the NPT IGBT development has accelerated the change from conventional power bipolar transistors to IGBTs.

An obvious means of improving the NPT structure lies in utilizing a configuration that involves a field distribution with trapezoidal shape in forward blocking states, as is typical of the PT IGBT. This is enabled by incorporating a relatively low-doped n-type field-stop layer enough to avoid affecting the low-doping p-collector in the NPT IGBT, but high enough to restrict the electrical field in forward blocking state. In this way, it enables to thin the drift-layer in the NPT structure. In a 1200 V device, an IGBT with the field-stop layer can be produced with a drift-layer thickness of roughly 120 μm instead of 180 μm, for example. Figure 13.50 and Table 13.2 compare the unit cell cross sections and design concepts of the NPT IGBT and field-stop IGBT. The field-stop (FS) IGBT was introduced by Matsudai et al. [73, 74] and then by Laska et al. [75]. It was optimized by the NPT IGBT design concept described above. The FS IGBT does not require as thick an n-drift layer as the NPT IGBT, because the former incorporates a field-stop layer to restrict the expansion of depletion layer. Commonly, the field-stop layer has a relatively low doping concentration (roughly below 1.0×10^{16} cm^{-3}), far less than the n+ buffer regions in the PT IGBTs shown in Fig. 13.35. Consequently, almost the flat distribution of electron-hole plasma can be obtained in its forward conduction state, and its on-state voltage drop is lowered. In addition, the FS IGBT can exhibit smaller switching power dissipation,

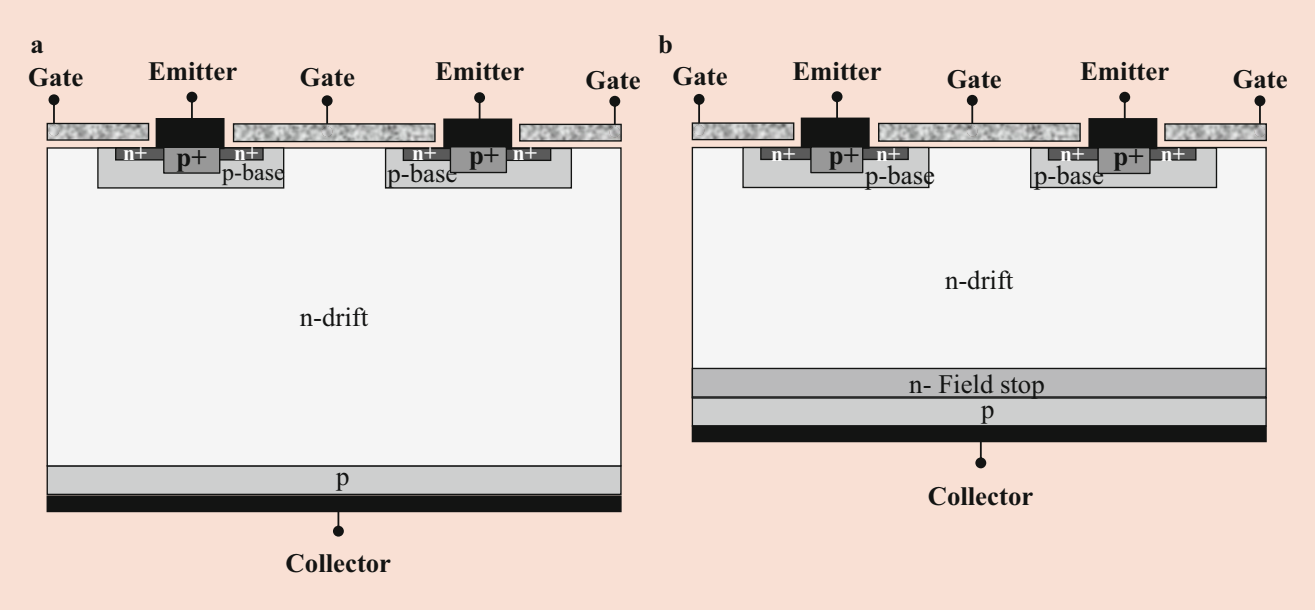


Fig. 13.50 Structural change of IGBT cell design. (**a**) NPT-IGBT; (**b**) FS-IGBT

due to the lesser number of excess carriers as a result of the thinner drift layer. Figure 13.51 shows a comparison of the schematic electron-hole plasma distribution in the FS-IGBT and early PT IGBT, in the on-state. Based on the drift-diffusion theory, the hole current density J_p and electron current density J_n in the IGBT can be expressed, respectively, as follows:

$$J_p = -qD_p\nabla p - q\mu_p p\nabla\varphi \tag{13.42}$$

$$J_n = qD_n\nabla n - q\mu_n n\nabla\varphi, \tag{13.43}$$

where q is the electron charge ($q = 1.6 \times 10^{-19}$ C); D_p and D_n are the hole and electron diffusion constants, respectively; μ_p and μ_n are the hole and electron mobility; p and n are the hole and electron concentrations; and φ is the electrostatic potential. It is clear from these equations that each current density consists of diffusion- and drift-current components.

From Fig. 13.51, it should be noted that in the PT structure the hole drift and diffusion currents are added, while the corresponding electron currents cancel each other, and this makes the hole current predominate over the total current flow in the IGBT on-state. In the FS IGBT, on the other hand, due to the almost flat carrier distribution, the hole and electron diffusion currents are both reduced dramatically, and as a result, the electron current predominates. Therefore, since electron mobility is much greater than hole mobility in silicon material, a higher current with lesser amounts of carriers is achieved, with both lower on-state voltage drop and higher switching speed. By incorporating a trench-gate structure, the increased channel density is achieved and the on-state voltage drop can be significantly lowered. Thus, the FS IGBT with trench gate is the most sophisticated IGBT structure.

Figure 13.52 shows the improvement of IGBT wafer thickness for the 600 V, 1200 V, and 1700 V voltage class [76]. Thin wafer technology is especially critical in the case of the IGBT, not only for the usual benefits of wafer thinness, but also for impurity implantation and diffusion, and for evaporation of the metal electrode on the wafer backside with absolutely no wafer breakage. Thus, the thin wafer technology for FS-IGBT is recognized as one of the most advanced technology in the entire semiconductor field, though advancement in thin wafer technology began to slow down around 2003, and the thickness of recent IGBT dies is roughly comparable to, or only slightly thinner than, those in 2003, mainly due to silicon material limitations. However, 50-μm wafers for 600 V devices, and 90-μm wafers for 1200 V devices, seem feasible in the near future; though with thinner IGBT dies, the soft switching characteristic, cosmic ray robustness, and thermal SCSOA will become more critical. In any case, the thin wafer design based on field-stop vertical cell optimization has contributed vastly to expansion of the IGBT rating limit, especially with respect to blocking voltage, which has attained 6.5 kV at present.

13.3.5 IGBT Module Technologies

The goal of the IGBT technological innovation discussed above was advancement not only in power dissipation but

Table 13.2 Comparison of the different IGBT design concept

	PT-IGBT	NPT-IGBT	FS-IGBT (or SPT-IGBT)
Injection efficiency from p collector	High	Low	
n buffer layer	High dose Functions (a) To stop an electric field	N.A	Moderately low dose Functions (a) To stop an electric field
	(b) To reduce the very high injection efficiency	(b) To optimize injection efficiency	
n-drift layer	Thin	Medium	Thin
Lifetime control	High (lifetime killing)	No lifetime killing	
Wafer	Epi layer on CZ wafer	Bulk wafer (FZ or MCZ)	

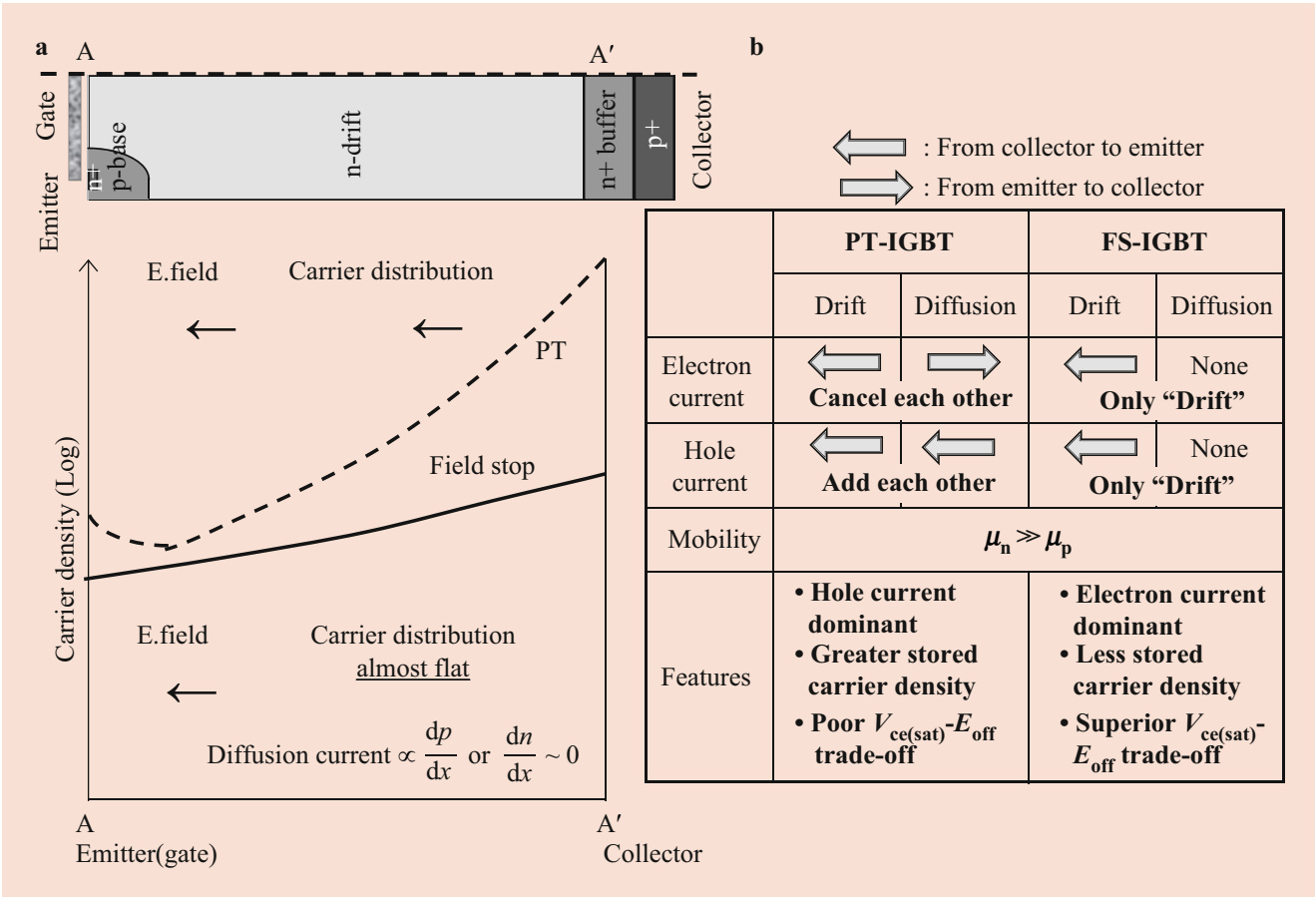


Fig. 13.51 Comparison of (**a**) schematic of electron-hole plasma and (**b**) features between the PT-IGBT and FS-IGBT in the on state

also in cost reduction through improvement in device characteristics that results in shrinkage in die size, as shown in Fig. 13.53. IGBT modules comprise multiple IGBT devices assembled on a substrate with ceramic isolation, which is itself set up on a thick-copper (Cu) base plate. FWDs are also assembled in the module, for simple system assembly and to enable to minimize both inside and outside stray inductances of the module. Several technological innovations related to the FWD are discussed in Sect. 13.5.

In a structure of the IGBT module on a cooling fin shown in Fig. 13.54, the direct copper bond (DCB) substrate is connected through a solder layer to a heat-dissipating thick Cu base, and a cooling fin is attached to the Cu base. In order to minimize the module size, shrinking a die size of the IGBT and FWD chip is required. However, such die-size shrinking results in increased power density, leading to reduced reliability due to increased device temperature. Nonetheless, the advanced IGBT module has been achieved side by side with IGBT and FWD device characteristics. State-of-the-art module packages give higher reliability and improved electrical characteristics, exploiting the new DCB substrate holding both high thermal conductivity and me-

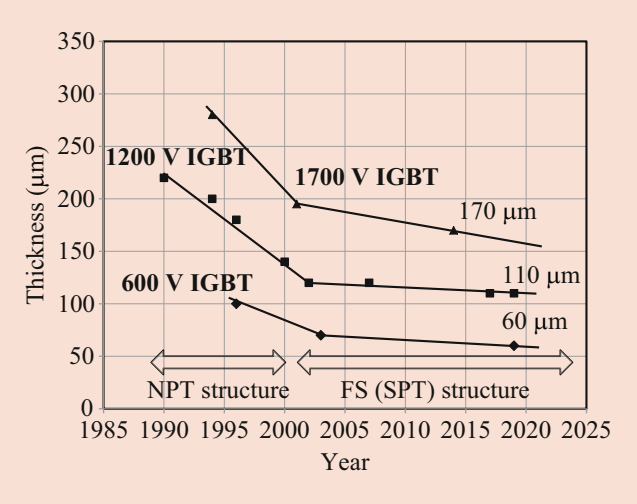


Fig. 13.52 Chronology of the IGBT wafer thickness improvement for 600, 1200, and 1700 V devices

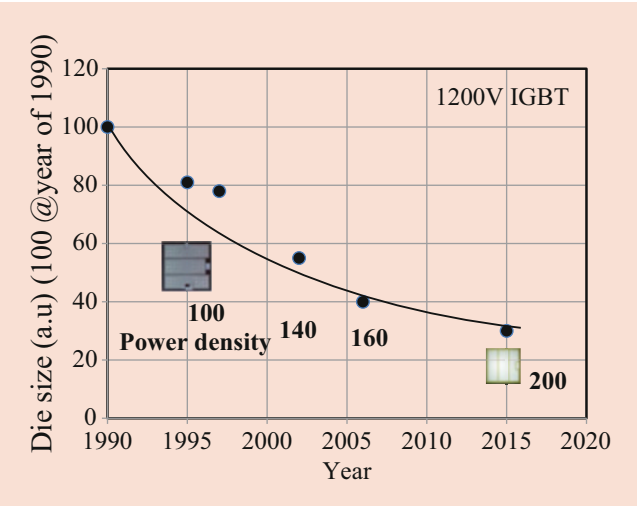


Fig. 13.53 Chronology of 1200 V IGBT chip size shrinkage and its power density

chanical strength, to enhance the operable power density of the module while achieving minimized size with low cost [77]. Thus, improvement in the module technology and shrinkage in the die size have both led to footprint reduction in the IGBT module and thereby to greater IGBT module applicability to smaller-sized power electronics devices. In a whole system of power electronics, higher energy efficiency and smaller-sized output power are of great importance, and IGBT modules are thus in wide use. With this in mind, in 1984, a new design incorporating dedicated drive and protection circuits into IGBTs, to surmount the inherent parasitic limitations of IGBT and enhance its performance as possible, was introduced. This is an intelligent power module, IPM for short [78]. A key feature of the IPM is that the printed circuit board (PCB) containing the gate drive and control circuit is assembled directly above the IGBTs and diodes. Extremely effective over-current sensing and short-circuit protection were achieved by using the advanced current sensing IGBT cells that enabled non-stop monitoring of the IGBT current; and system reliability was enhanced more by the incorporated over-temperature sensing and protection in the IPM. Hence, the IPM has shown improvements in a whole system performance and reliability over conventional IGBT modules and, consequently, has been widely used in a variety of power electronics apparatus, along with uninterrupted improvement in IGBT and diode devices, and packaging and control circuit technologies.

13.3.6 P-ch IGBT Devices

In the 1980s, p-ch IGBT structures were developed as complementary inverters in high-power range. In high-power inverter circuits, complementary topologies of common source types [12, 79] can minimize the dead time as possible between the upper and lower arm in one leg, alleviating the problems caused by dead time, such as harmonics generation as described in Sect. 13.2.2. A leg consisting of complementarily set up n-ch and p-ch devices can reduce the dead time and enable increased switching frequency with no shoot-through of a DC voltage. Traditionally, there has been considerable need for high-power p-ch applications, but no p-ch power devices acceptable for these applications. For example, the area of a p-ch MOSFET requires roughly 2.5 to 3 times larger than that of the corresponding n-ch MOSFET, in order to exhibit the same on-resistance. However, this dramatic size disadvantage is not observed in the case of the IGBT structure, because of the conductivity modulation in the drift region, and this advantage helped launch p-ch IGBT development. Chang et al. reported that the trade-off characteristics between on-state voltage drop and turn-off power dissipation in a p-ch IGBT were marginally worse than in an n-ch counterpart, because of the higher channel resistance in the p-ch IGBT [80]. However, a severe issue for the p-ch IGBT was poor RBSOA and SCSOAs, and this issue is theoretically unsolvable [81, 82]. It has been demonstrated numerically and experimentally that p-ch IGBT structures are easily destroyed, not by latch-up of the parasitic thyristor, but by avalanche multiplication, because the electrons, which have a much higher avalanche ionization rate than holes in silicon material [83], flow across the p-n junction of n-base and p-drift region in the p-ch IGBT structure, where there is a high electric field under turn-off and short-circuit conditions. Carriers flowing through a high electric field gain sufficient energy to excite electron-hole pairs. The carrier generation rate G is expressed as

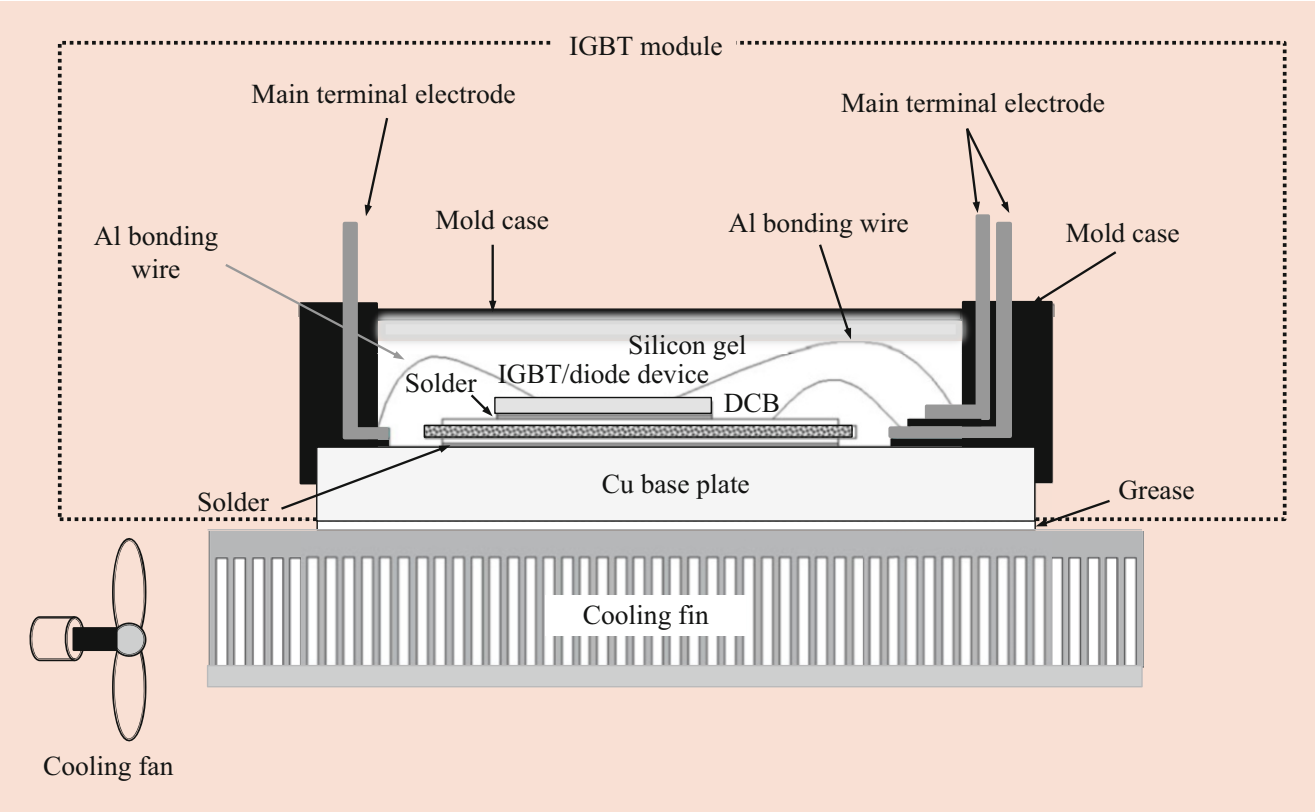


Fig. 13.54 Cross section of IGBT module on a cooling fin

$$G = \frac{1}{q}\left(\alpha_{\mathrm{p}}\left|J_{\mathrm{p}}\right| + \alpha_{\mathrm{n}}\left|J_{\mathrm{n}}\right|\right), \tag{13.44}$$

where q is the electron charge ($q = 1.6 \times 10^{-19}$ C), α_{p} and α_{n} are the hole and electron impact ionization rate respectively, and J_{p} and J_{n} are the hole and electron current density.

As a result, avalanche generation takes place near the junction, so that many generated holes flow toward the n+ collector region as additional base current in the wide-base npn transistor, resulting in huge current flows when the positive feedback between the avalanche generation and electron injection from the n+ collector takes place. Finally, this huge current flows through the p-ch IGBT, causing destructive failure of the device.

Figure 13.55 compares the SCSOA of p-ch and n-ch IGBTs. The n-ch IGBT exhibits poor latch-up capability in this figure; however, this characteristics can be improved through utilization of the non-latch-up structure mentioned in Sect. 13.3.3. However, the poor p-ch IGBT avalanche capability cannot be similarly improved through the application of device design technologies. For this reason, most IGBTs have been developed by n-ch structures, and consequently, there are hardly high-power complementary inverter circuits incorporating both n-ch and p-ch IGBTs.

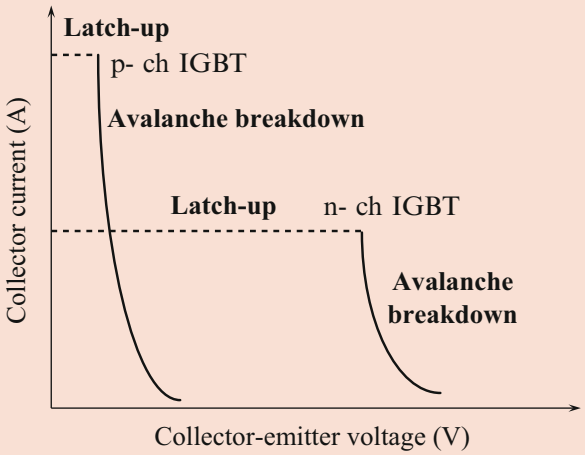


Fig. 13.55 Comparison of the short-circuit SOAs between p-ch and n-ch IGBT

13.3.7 State-of-the-Art IGBTs

The most critical components of an IGBT are its wide-base pnp transistor design in the upper region of the device, and the vertical cell structure comprising an n-drift layer, a field-stop layer, and back-side p+ collector, as shown in Fig. 13.50b.

Design Concepts for the IGBT Transistor Cell and Vertical Structure

Trench cell technology has been widely introduced and incorporated over the entire voltage class range, from 400 V to 6.5 kV cell designs; from the trench cell-based IEGT [84] with its wide distances between the cells [72], to structures with narrower or otherwise different gate and/or source trenches; and in designs that do or do not include an additional doped n layer underneath the p body [67, 70]. However, all the designs share the basic principle of enhancing the amounts of electrons and holes in the upper part of the device during the on state, through hole confinement or the injection enhancement effect [69]. Consequently, the on-state voltage drop in such trench cell-based IGBTs with increased carriers is greatly lowered compared to earlier, planar cell-based IGBTs.

The latest efforts to further enhance the carrier concentration on the upper part tend to focus on reducing the cell size and pitch to the micro or even sub-micron level [85–87], as shown in Fig. 13.56. However, if the increase in electron and hole plasma in the upper part is overemphasized, the result can be excessive turn-off power dissipation as the excess plasma is not swept out rapidly enough. Thus, carrier engineering with respect to the electrons and holes in the surface side of the IGBT must be carefully balanced, to enable low on-state voltage drop and fast turn-off characteristics at the same time.

An equally critical IGBT design element is the vertical structure. The current vertical design is a punch-through configuration with a low-doped field-stop layer interposed between the n-drift region and the back-side p collector with low hole injection, without lifetime control process (see Fig. 13.50b), which is often referred to as a field-stop [73, 75] or soft punch-through structure [88]. This self-evident development from the earlier NPT [63] and PT [89] design concept seeks to optimize both the cost and performance of industrial IGBTs. It has traditionally been utilized in 1200 V voltage class devices, and then stepwise up to 6.5 kV devices, but has also been incorporated in lower voltage classes, from 600 V to even less than 400 V, and in devices ranging in thickness from roughly 45 μm (400 V) to roughly 700 μm (6.5 kV).

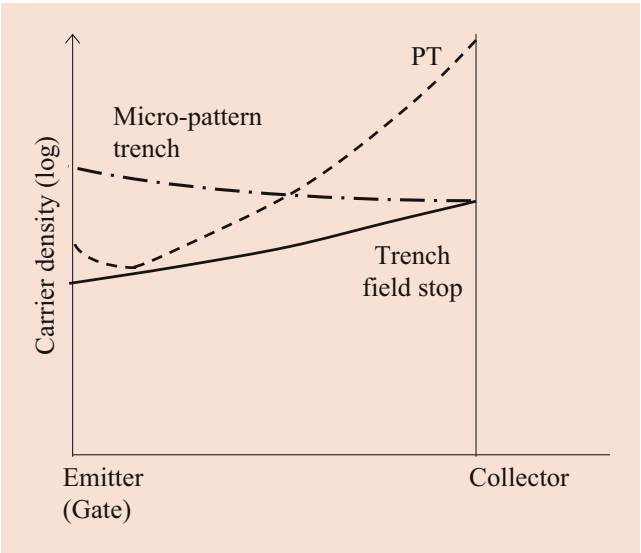


Fig. 13.56 Schematic electron-hole plasma distribution in the on state among the different cell concept of IGBT (PT, trench FS, and micro-pattern trench)

Reverse Blocking IGBT and Reverse Conducting IGBT

Among the recent developments in current-art IGBT technology is integrating additional functions in the device. One example is the reverse blocking IGBT (RB IGBT) [90], which offers advantages for particular applications such as matrix converters for AC to AC direct conversion, but drawbacks for process difficulty and vertical optimization restrictions compared to field-stop IGBTs (see Fig. 13.57). The main feature of RB IGBT is the reverse blocking capability. The RB IGBT structure is a type of NPT configuration and has been improved by the addition of a junction isolation region (Fig. 13.57), which is absent in conventional IGBTs. A lateral or dicing face is generated during the manufacturing of a cut-out from the wafer, and crystal deformations and high-density crystal defects typically occur. At this lateral face, carriers continuously generated from these crystal defects are transported by the electric field of the applied negative voltage, leading to large leakage current. Thus, without the junction isolation region, conventional IGBTs do not have enough reverse blocking capability, because there is leakage current flow through the IGBT device when reverse voltage is applied between the collector and emitter electrodes. In the RB IGBT, on the other hand, the junction isolation region prevents leakage current from flowing through the RB IGBT and enhances the reverse blocking capability. An example of the measured forward and reverse blocking characteristics of a 1.2 kV RB IGBT is provided in Figs. 13.58 and 13.59. The reverse breakdown voltage of about 1270 V is similar to the forward breakdown voltage. In spite of their distinct differences, RB IGBTs and NPT IGBTs are similarly structured in the active regions, and their turn-off characteristics are therefore similar. In terms of the trade-off characteristics between forward voltage drop and turn-off loss in the RB IGBT and NPT IGBT with diode in series, a clear benefit is shown in Fig. 13.59. The turn-off of the RB IGBT is similar to that of an IGBT with a diode; however, the former has a much lower forward voltage drop than the latter, due to the absence of an additional diode. This improvement contributes to a reduction of power dissipation when utilizing an RB IGBT as a bi-directional switch.

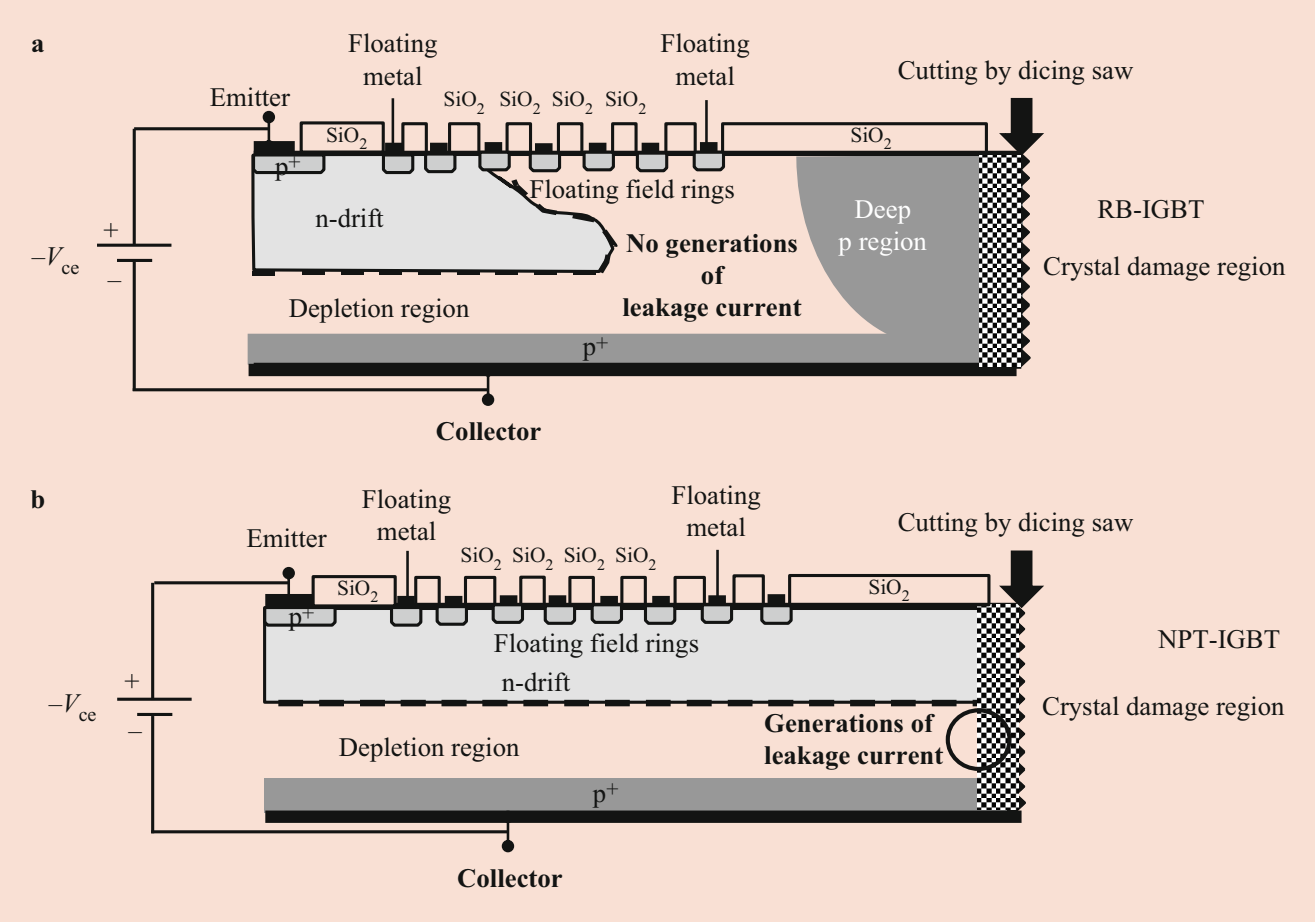


Fig. 13.57 Comparison of cross section between RB-IGBT and NPT-IGBT. Depletion expansions by a reverse bias are drawn in these figures

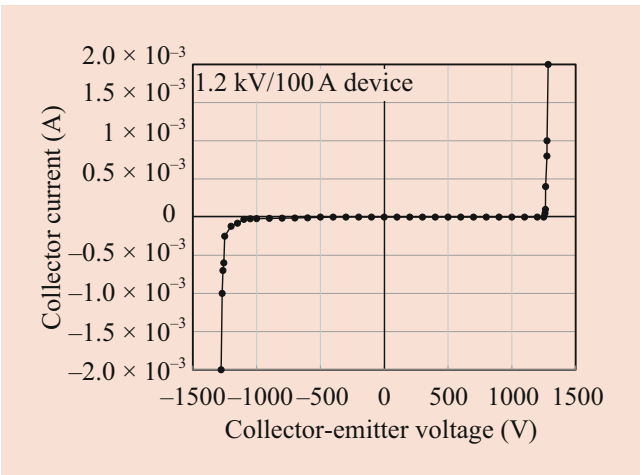


Fig. 13.58 An example of measured forward and reverse blocking capability of 1.2 kV RB-IGBT(@R.T)

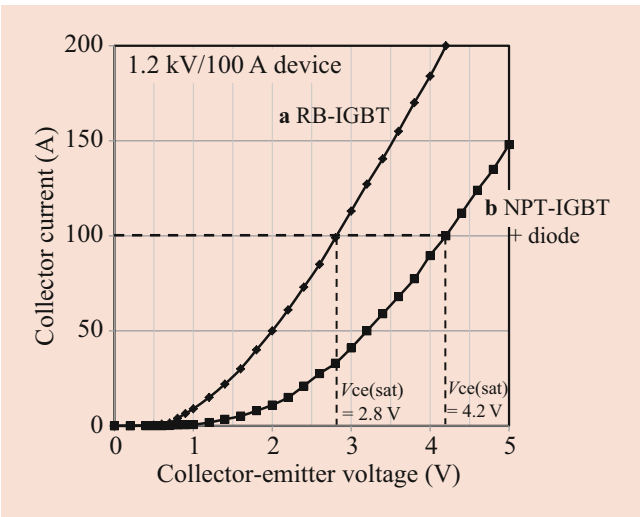


Fig. 13.59 An example of measured forward I-V characteristics (@125 °C). **a** RB-IGBT, **b** NPT-IGBT + diode in series

Another promising focus for integration is the incorporation of free-wheeling diode functionality in the IGBT, resulting in a so-called reverse conducting or RC IGBT (Fig. 13.60). In these devices, the IGBT and free-wheeling diode (FWD) are integrated into a single device, resulting in significant reduction in the RC-IGBT module size. The RC IGBT structure was proposed as part of the p-ch IGBT

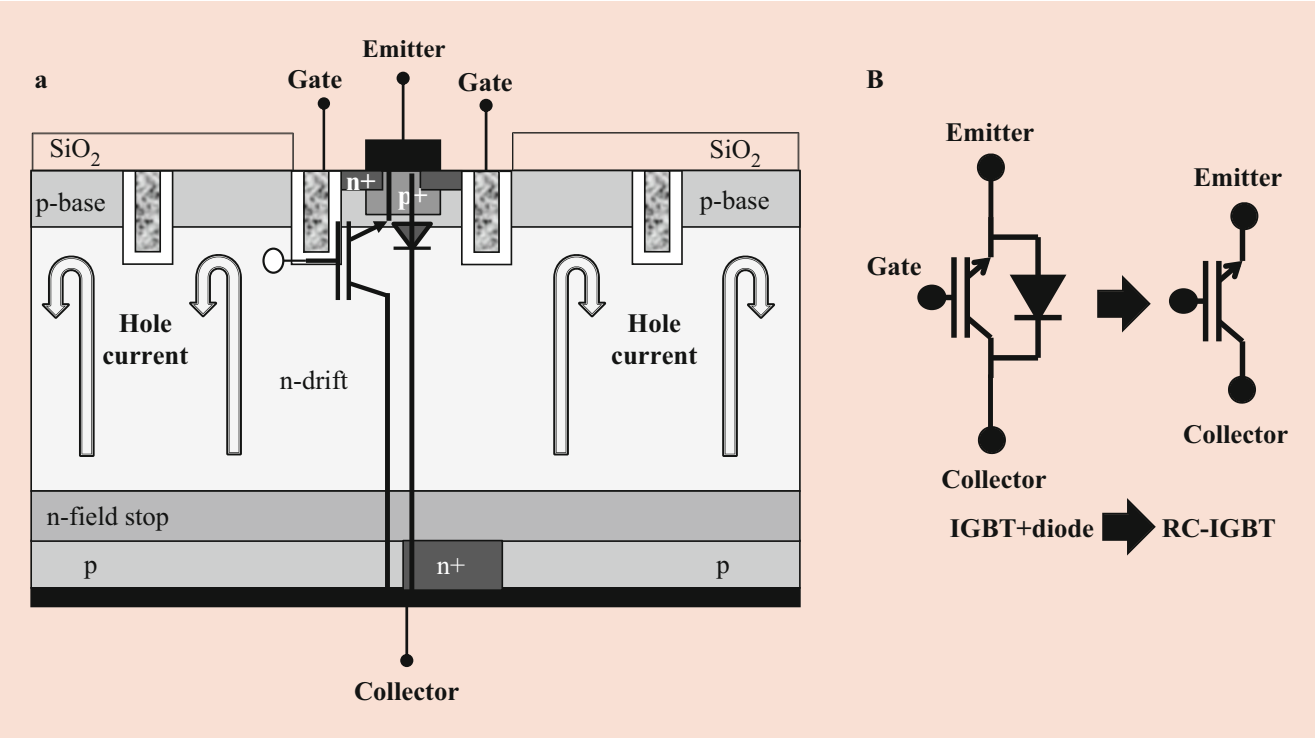


Fig. 13.60 RC IGBT as an integration of IGBT and FWD within one die. (a) Cross section. (b) Equivalent circuit

with collector short [91], based on the design concept in [92]; and in 2004, the structure was presented in the context of NPT technology [93]. FS-IGBT technology was initially applied and well-suited only to particular applications such as induction heating [94]; however, it could also be optimally designed, in terms of the integrated diode function, for typical applications for industry and consumer electronics in the 600 V and 1200 V voltage ranges, with its requirement for hard diode commutation [95, 96]. The particular challenge here is to integrate highly disparate optimized features, such as low lifetime in diode and highly doped p-base in IGBT cell, in a single die. A current RC-IGBT module was recently developed for automotive and industrial applications, and trench FS-IGBT technology with finer cell pitch and thinner wafers has been developed. Consequently, the forward voltage drop in IGBT plus diode operation has been reduced in comparison with previous-generation devices [97]. In addition, IGBT and FWD components are alternately located on the RC-IGBT die, resulting in better thermal resistance than in conventional IGBTs, because the dissipation from individual components is radiated from the entire die surface. This is especially useful in so-called rotor locks, step-up converters, and active short-circuit systems. In the case of rotor locks, the RC IGBT can dramatically suppress temperature increase, because of the large heat radiation area; and even traction applications in the high voltage region of 3.3 kV have been discussed [98, 99]. The structure is generally highly useful for high voltage applications, because the IGBT and FWD share edge termination regions, leading to a significant reduction in the silicon wafer area.

The future of this competition between the standard combination of independent IGBTs and diodes, and integrated solutions such as RB IGBTs and RC IGBTs, is unclear, but may at least partly depend on development in inverter topologies and applications for cooling and gate drive design.

Increase of the Maximum Junction Temperature and Power Density

The evolution from the earliest IGBTs to the current state-of-the-art structure can also be considered in terms of the maximum junction temperatures (T_j) of the dies in the package. From 125 to 150 °C appears to be the standard maximum junction temperature for IGBTs in conventional modules. Further, state-of-the-art IGBT modules are also specified for a T_j of 175 °C, both as a continuous condition [100, 101] and for overload cases [102, 103]. Improvements to support these enhanced junction temperatures come from both the semiconductor device side (reduced leakage current at high temperature, high intrinsic over-current and short-circuit robustness) and the module side, as well as from interconnected die technologies in the package.

Increased junction temperature enables dramatic shrinkage in die size for a given nominal current, with shrinkage correlated to the increased in T_j. This enhanced current rating per device die size can be utilized either for minimizing the module footprint for a given power level or enhancing the output power for a given module footprint. Both designs lead to higher power density and enable the module users to either reduce the size and weight of the given inverter or significantly increase its power. The increase in nominal current and output power in a standard industrial IGBT module over several generations, enabled by shrinkage of device die size, is shown in Fig. 13.53. Thus, power density enhancement has been a crucial trend in, and remains the primary driver behind, IGBT innovation and has been enabled not only by improvements in transistor cell and vertical technology but also by successful approaches to increasing the junction temperature.

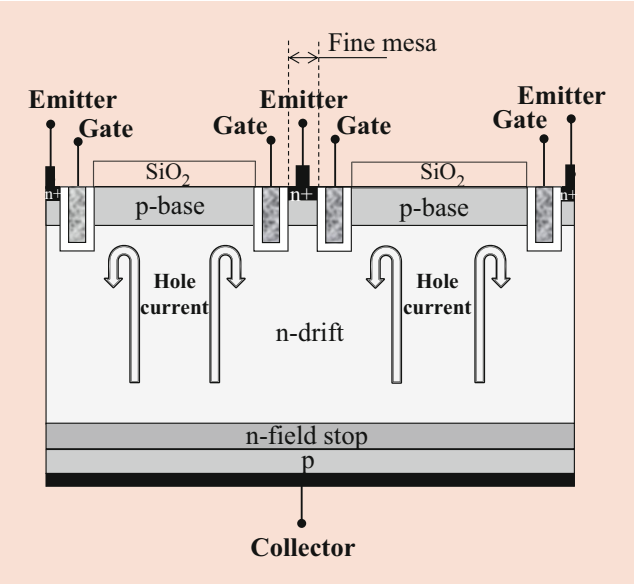


Fig. 13.61 An example of IGBT structure with fine mesa

13.3.8 Future Prospects of IGBT Devices

There are numerous questions concerning the nature and significance of further development in IGBT technology, especially given the new wide bandgap power devices that mainly utilize silicon carbide (SiC) (≥1200 V) or gallium nitride (GaN) (<1200 V). As silicon IGBTs approach their theoretical limits, it becomes even more important to determine which properties are critically necessary from an application point of view.

Typical examples include voltage slope (dV/dt) limitation at turning on and turning off of IGBT and short-circuit withstanding capability. These properties define the direction of silicon IGBT development and must be reconceptualized in the context of wide bandgap power devices. For example, the advantages provided by the latter devices, due to their very low switching losses, are only in effect when they are allowed to switch very quickly; and this may not suit the requirements of many power current electronics users seeking a dV/dt value of less than 10 kV/μs, owing to concerns about electromagnetic interference (EMI) and a desire to minimize motor deterioration. Allowing higher dV/dt would enable switching loss reduction than for silicon IGBTs. However, the actual correlation between dV/dt values and the EMI spectrum in current applications is often unclear.

Reducing the usual short-circuit requirements from 10 μs to 5 μs, or even less, would raise the possibility of increasing of ratio of channel width W to length L (W/L), enabling on-state loss reductions in both SiC MOSFETs and silicon IGBTs [104]. Even if the current requirements for dV/dt and short-circuit withstanding are adopted, there are ways to further improve silicon IGBT technology; however, the more these requirements are eased, the more likely it will be that improvements will take place. In order to envisage possible future developments, it will be useful to briefly reconsider single-cell and vertical-structure IGBT devices.

Next-Generation Transistor Cell and Vertical Structures

In light of the theoretical limits of IGBT on-state characteristic [105], much current research is focusing on sub-micron (down to 0.5-μm) mesas between adjacent deep trenches [84, 106, 107], as shown, for example, in Fig. 13.61. In addition, there are indications that the on-state voltage drop can be lowered nearly 1 V devices rated for a 1200 V blocking; however, excessively high turn-off switching losses due to excessive amounts of electron-hole plasma, as well as problems related to short-circuit robustness, remain to be addressed. If such difficulties are overcome, next-generation IGBTs may benefit from significant loss reduction in the on-state and device shrinkage by incorporating mesa structures in the deep submicron region or even below.

There is also room for improvement in IGBT vertical structure design. As is the case in every vertical bipolar power device, the thinner the n-drift layer, the greater the opportunity for reduction in both forward conduction and switching power dissipations. Recently, 1200 V IGBTs with a device thickness of roughly 110-μm, and 600 V IGBTs of roughly 70-μm thickness, have become common. Based on the theoretical limits for blocking capability, 1200 V devices of roughly 90-μm thickness, and 600 V devices of roughly 50-μm thickness, seem feasible, with recent ultrathin wafer technology seemingly able to satisfy these requirements [108]. However, the thinner the IGBT device, the more critical will be the softness in switching waveforms, cosmic ray robustness, and SCSOA determined by thermal reasons. About the softness in switching waveforms, module and

inverter systems with low stray inductance will play an important role, along with optimized engineering of field-stop and refinement in the specification of injection efficiency in p collector. The last, in particular, must be considered, especially given the recent elucidation of the three-dimensional trade-off between on-state and switching losses and overvoltage at turn-off [86]. It is becoming clear that unfavorable high injection efficiency in the back-side collector could be in the best compromise about overall losses and overvoltage, at least as long as high stray inductances take place. To maintain the robustness for cosmic ray at a sufficiently high level, the doping concentration in the n-drift region can be increased; and a sufficiently high level of thermal SCSOA can be achieved, even with reduced device thickness, by incorporating a thick metal layer on the device surface.

Intelligent Gate Drive Control

As one means to address the trade-off between short-circuit withstand capability and forward voltage drop, IGBT devices have been designed with increased ratio of channel width W to length L (W/L), over-current sensing, and reduced gate-voltage capability. This is because, in the case of short circuiting, the current still flows at a manageable level within the first few micro seconds. As this approach is common in intelligent power modules (IPMs) [109], in the future it may also be utilized in standard IGBT modules, as it ensures at least one significant improvement in IGBT performance compared to standard short-circuit rated IGBTs [110].

Another important improvement, based on sophisticated gate drive operation, is available for RC IGBTs. By also utilizing trench cells for the diode function in the IGBT, a dedicated gate drive operation can be achieved, to vary the electron and hole carrier distribution from a higher concentration level during free-wheeling mode to a lower concentration level shortly before commutation [110]. Using this operational scheme, a reverse conducting diode controlled IGBT (RCDC IGBT) can increase its potential to high-voltage, such as 3.3 and 6.5 kV, traction and HVDC applications. A similar approach is evident in the design of the BIGT (bimode insulated gate transistor) [111], which illustrates a means of power density enhancement for 3.3, 4.5, and 6.5 kV power modules. If these more sophisticated gate drive technologies also become standard in the medium voltage range (600–1700 V), the RCDC IGBT design can enhance power density compared to the conventional approach involving independent optimized IGBT and diode devices [112]. And in the future, the electron-hole plasma concentration at a high level during on-state, and then varying it to a lower level before the switching, may become more popular also in IGBTs .

Advanced Thermal Management

The trend of improving the maximum junction temperature (T_j) will likely continue, up to at least 200 °C. It has already been demonstrated that silicon IGBTs can operate at high temperature levels up to 200 °C, making overload operations of RBSOA and SCSOA at 200 °C seem feasible [113, 114]. The peripheral region around the power device, such as the package with its plastic components, and the terminals and peripheral components outside the package, must have capability to withstand such high temperature levels. More specifically, the mold compound in discrete IGBTs, and the silicone gel in standard IGBT modules, presents challenges at increased temperatures, but there already exist solutions for gels up to 200 °C [115].

Two other important issues in this context are the increased temperature swings that result in baseplates and lead frame connections stressing power devices, and inadequate wire bonding on the surface of the IGBT, resulting in fewer power and temperature cycles until failure. For these innovations, sophisticated solutions already in place may also be feasible even up to 200 °C, whether in the form of sintering interconnection technology on the back and surface side of the semiconductor device [116–118], or alternatively, through surface side copper wire bonding [100]. Using the recently developed technique involving thick copper metallization on the surface side, to facilitate the copper bonding process, also improves the thermal SCSOA, which can enable reduction in die size and device thickness [119].

It is strongly expected that the such combined solution of semiconductor device and module will encourage the use of higher T_j up to 200 °C in the future, and that these will lead to innovations in not only single cell and vertical structures but also gate driving with higher-power density.

13.4 MOS Gate Thyristors

In a range of high blocking voltage, the IGBT shows much lower forward conduction loss than the power MOSFET, and it is commonly known that thyristor structures show lower conduction loss than bipolar transistors. The thyristor family consists of several structures from the simple silicon-controlled rectifier (SCR) [120] to the complex triac [121]. A basic thyristor structure comprises four semiconductor layers (p_1, n_1, p_2, n_2) and three pn junctions (J_1, J_2, and J_3) in series, as shown in Fig. 13.62. Thyristor operation can be understood in terms of a two-transistor model, with transistor T_1 being an npn bipolar junction transistor (BJT) comprised of n_1-p_1-n_2, and transistor T_2 being a pnp BJT comprised of p_2-n_2-p_1. A positive voltage is applied between the anode and cathode electrodes, and current conduction does not take place because the central pn junction J_2 is reverse-biased. When a gate current I_g is supplied as the base current, the collector current of the npn BJT T_1 begins to flow, providing the base current drive for the pnp BJT T_2. Thus, a regenerative

situation will occur when the sum of the current gain in the two BJTs exceeds unity ($\alpha_1 + \alpha_2 > 1$).

There has been much greater interest in developing thyristor devices with MOS control capability, for achieving a much lower forward conduction loss. Although the turn-on of a vertical thyristor structure through MOS gate has been demonstrated [51], the turn-off of the thyristor current using the MOS gate is very hard because of the regenerative activity occurring in the thyristor. Some promising ideas to achieve this capability have been introduced and presented experimentally; and several promising structures have been developed. In this section, the some promising MOS gate thyristor structures and their operation are introduced.

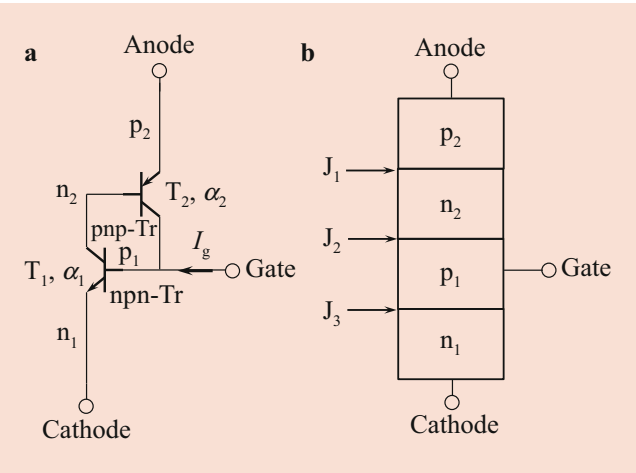


Fig. 13.62 Thyristor: (**a**) npn-pnp transistor model; (**b**) basic structure. α_1: current gain of npn bipolar transistor; α_2: current gain of pnp bipolar transistor

13.4.1 The MOS-Controlled Thyristor (MCT)

Figure 13.63 shows a cross section and an equivalent circuit of the MCT structure [122]. The thyristor structure is formed by coupled n+/p-base/n-drift (npn-Tr as shown in Fig. 13.63) and p+/n-drift/p-base (pnp-Tr as shown in Fig. 13.63) transistors, and the on-state current flows through the thyristor. When the positive anode voltage is applied, the device can be switched on by a positive gate voltage to form the inversion layer at the surface of the p-base region in the n-ch MOSFET (n-MOSFET). Electrons from the cathode begin to flow through the inversion layer into the n-drift region, and these electrons act as the base current for the pnp transistor (pnp-Tr) in the thyristor structure. Holes are injected from the p+ anode into the n-drift region and collected by the p-base region. Eventually, the hole current flow triggers the activation of npn transistor (npn-Tr) and latch-up of the thyristor, at which point, the positive gate voltage can be removed, and the on-state current keeps flowing in the thyristor region while showing a low on-state voltage drop. The MCT can be turned on by using the n-ch MOSFET and has an extremely low on-state voltage drop of roughly 1.0 V and more. The thyristor operation can be halted by turning on the p-ch MOSFET (p-MOSFET) incorporated into the p-base region. Also, it has been made clear that the MCT must be operated with a snubber circuit because of the limited RBSOA [123, 124]. As the MCT does not possess high-voltage current saturation characteristics, it has no short circuit SOA. Another drawback of the MCT is that its triple-diffusion junction structure makes its manufacture more difficult. Despite these problems, however, MCT devices have become commercially available.

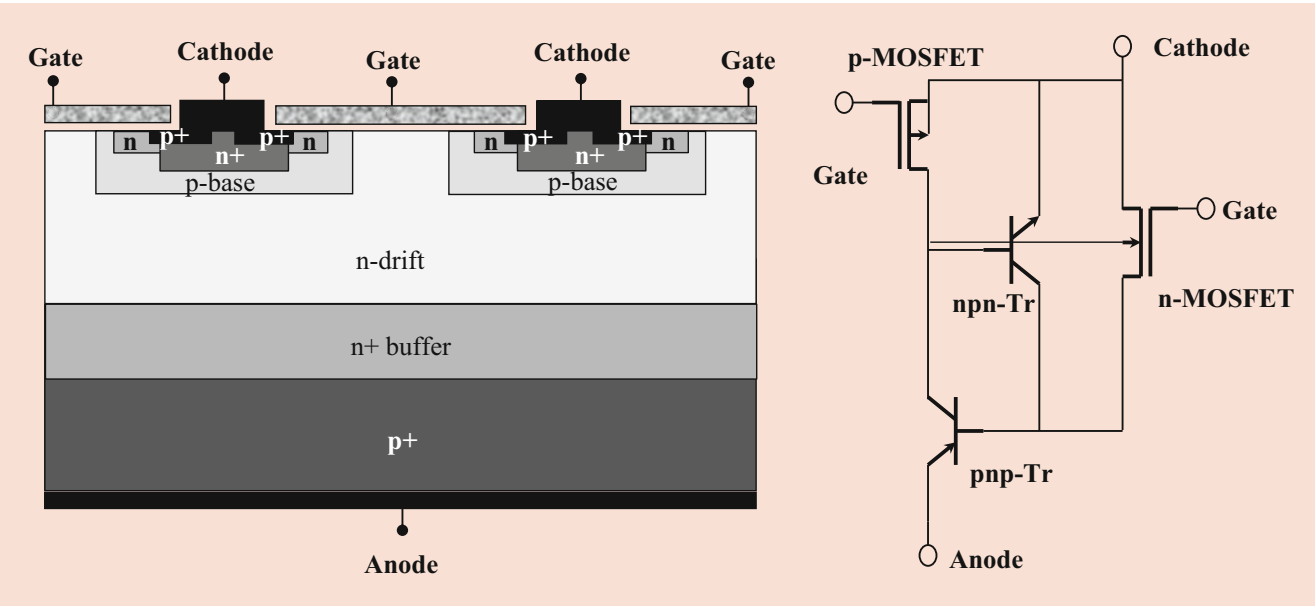


Fig. 13.63 Cross section of the MOS-controlled thyristor (MCT) and its equivalent circuit

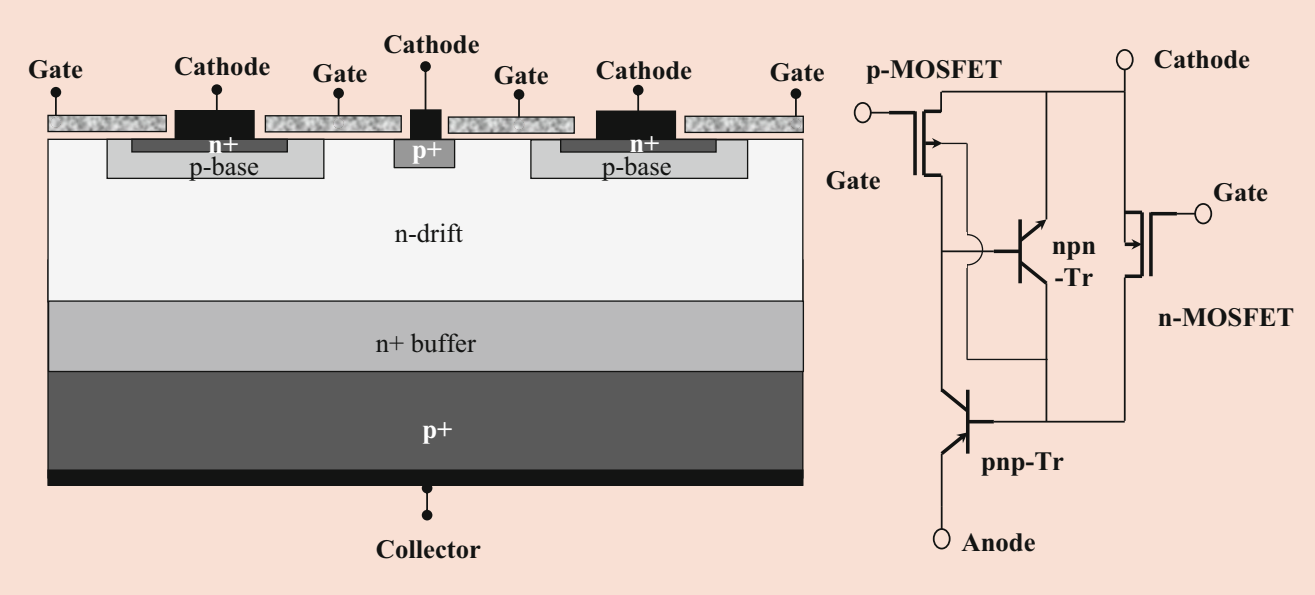


Fig. 13.64 Cross section of the base resistance-controlled thyristor (BRT) and its equivalent circuit

13.4.2 The Base Resistance-Controlled Thyristor (BRT)

A cross section of the BRT device is shown in Fig. 13.64, along with its equivalent circuit [125]. This device has a thyristor region with adjacent n-ch and p-ch MOSFETs. Notably, the p-ch MOSFET is fabricated in the n-drift region in the device. The thyristor region can be activated by a positive gate voltage, creating an inversion layer through which electrons flow into the n-drift region in the IGBT operation. Holes are injected from a p+ substrate in the anode side into the drift region and collected by the p-base, where they flow laterally underneath the n+ cathode region to the p+ region. The device shows IGBT mode operation at low current levels, and the hole current flow in the p-base generates a voltage drop that forward biases the n+ cathode/p-base junction. This forward-biased potential is sufficient to inject electrons from the n+ cathode, leading to latch-up of the thyristor. Once this thyristor is latched up, the current keeps flowing in the thyristor region with an extremely low on-state voltage drop. When a negative gate bias is applied, the BRT can be turned off to form a p-ch MOSFET at the surface of the n-drift region. Through the action of the p-ch lateral MOSFET, the thyristor's regenerative activity can be halted by diverting the hole current flowing into the p-base region to the cathode electrode. This device has exhibited excellent on-state characteristics, with a forward voltage drop of roughly 1.0 V and more and high current turn-off capability owing to diverting the hole current into the p-base. In addition, the process for BRT fabrication is compatible with that for the IGBT fabrication. However, the device does not possess high voltage current saturation characteristics and thus has the same drawbacks as the MCT without any short-circuit SOA.

13.4.3 The Emitter-Switched Thyristor (EST)

The EST structure (dual channel EST) is shown in Fig. 13.65, along with its equivalent circuit [126]. It differs from the EST structure originally reported [127]. The lateral n-ch MOSFET is formed using a standard DMOS process. This leads to the formation of a dual-channel MOSFET connecting n+ floating in thyristor region with the cathode electrode. Applying a positive anode voltage, the device can be switched on by a positive gate voltage to form an inversion layer at the surface of the p-base region. Electrons from the cathode flow through the inversion layer then enter the n-drift region. These electrons act as the base current for the pnp transistor in the main thyristor; then, holes are injected from the p+ anode into the n-drift region, and collected by the p-base region. Before latch-up of the main thyristor, these holes flow laterally in the p-base beneath the n+ floating region to the emitter short formed along the cathode finger orthogonal to the cross section. In this operation mode, the device works as an IGBT. As the current increases, the n+ floating and p-base junction in the npn transistor is forward biased and the main thyristor latches up. The device is turned off by lowering the gate voltage below the threshold voltage of the n-ch MOSFET, which leads to the elimination of inversion layer for electron flow, so that the n+ floating emitter is disconnected from the cathode, halting the thyristor action. In the EST, MOS-gated control makes the thyristor current flow through inversion layer in the MOSFET channel, which not only shows capability of MOS gated turn-off but also enables high voltage current saturation. These are features unique to the EST. The physics of the high-voltage current saturation derives from pinch-off of the n-ch MOSFET. When a high anode voltage is applied with low gate bias, the n+ floating

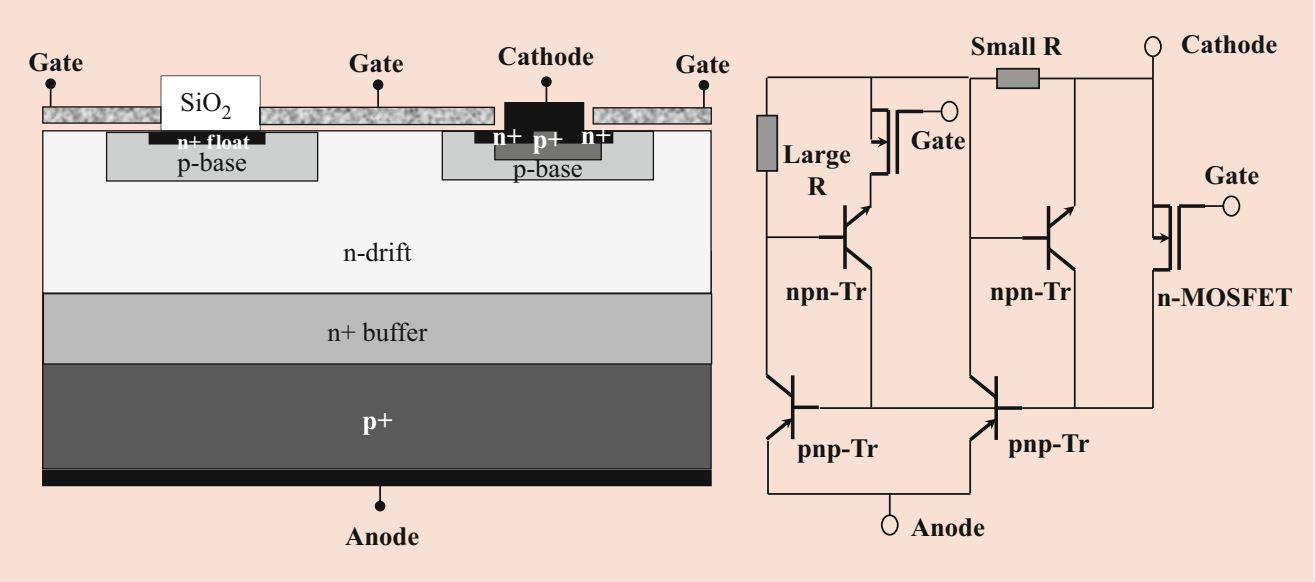


Fig. 13.65 Cross section of the dual channel emitter switched thyristor (EST) and its equivalent circuit

region is in isolation state by the channel pinch-off between the p-base diffusion regions, and as a result, the injection of electrons from the n+ floating region ceases. Consequently, the EST operates as an IGBT, with high voltage current saturation capability [128]. However, the device has a somewhat higher forward voltage drop across the MOSFET, and this adds to the voltage drop across the thyristor, as shown in Fig. 13.66.

The MOS-controlled cascode thyristor (MCCT) structure and operation are very similar to the dual channel EST, with the main structural feature being the absence of electrode connection to the deep n+ emitter and p-base region in the main thyristor [129]; and like the EST devices, the MCCT possesses the twin capabilities of MOS gate controlled turn-off and high voltage current saturation.

13.4.4 MOS Gate Thyristors and IGBT Competition

The IGBT is distinguished by its simple gate drive and high-voltage current saturation, and numerous works have investigated its suitability for high power applications. At the same time, MOS gate thyristors such as MCTs and BRTs have been similarly studied, as potentially superior alternatives, because of their equally simple gate characteristics and lower forward voltage drops. However, since the latter do not have high voltage current saturation, resulting in much more limited short-circuit SOAs, the market has not accepted them as feasible alternatives to the IGBT. The dual channel EST and MCCT are the only reported MOS gate thyristors with gate controlled current saturation capability, which makes them suitable for applications requiring short-circuit protection, because they can limit the anode current to a specific value even in the short-circuit state, by reducing the gate voltage using an integrated protection circuit. However, since the EST and MCCT have dual channel MOSFETs connecting the n^+ floating region and cathode electrode in series, they exhibit higher on-state voltage drop than other thyristors. Therefore, with the advent of recent sophisticated IGBT designs such as the IEGT [69] and CSTBT [70], which show extremely lower on-state voltage drop through electron-hole plasma enhancement around the surface of the device (see Sect. 13.3.4), the improvement in forward voltage drop provided by the dual channel EST and MCCT is not significant enough to make them superior alternatives to IGBTs. Finally, MOS gate thyristor research and development has been gradually declining, resulting in very few such devices being in the market at this time .

13.5 Power Rectifiers

13.5.1 Unipolar Devices

A Schottky barrier diode (SBD) with rectification capability can be simply fabricated by forming a metal layer on the silicon surface. SBD products are commonly designed for relatively low breakdown (<200 V). The features of SBDs over pin diodes is the very fast reverse recovery due to the absence of minority carriers; and silicon SBDs are now utilized in a variety of high frequency applications. When reverse voltage is applied to an SBD, a very small leakage current flows; and when forward voltage is applied, a large forward current flows and its on-resistance is low. It is well known that the on-state voltage drop in the

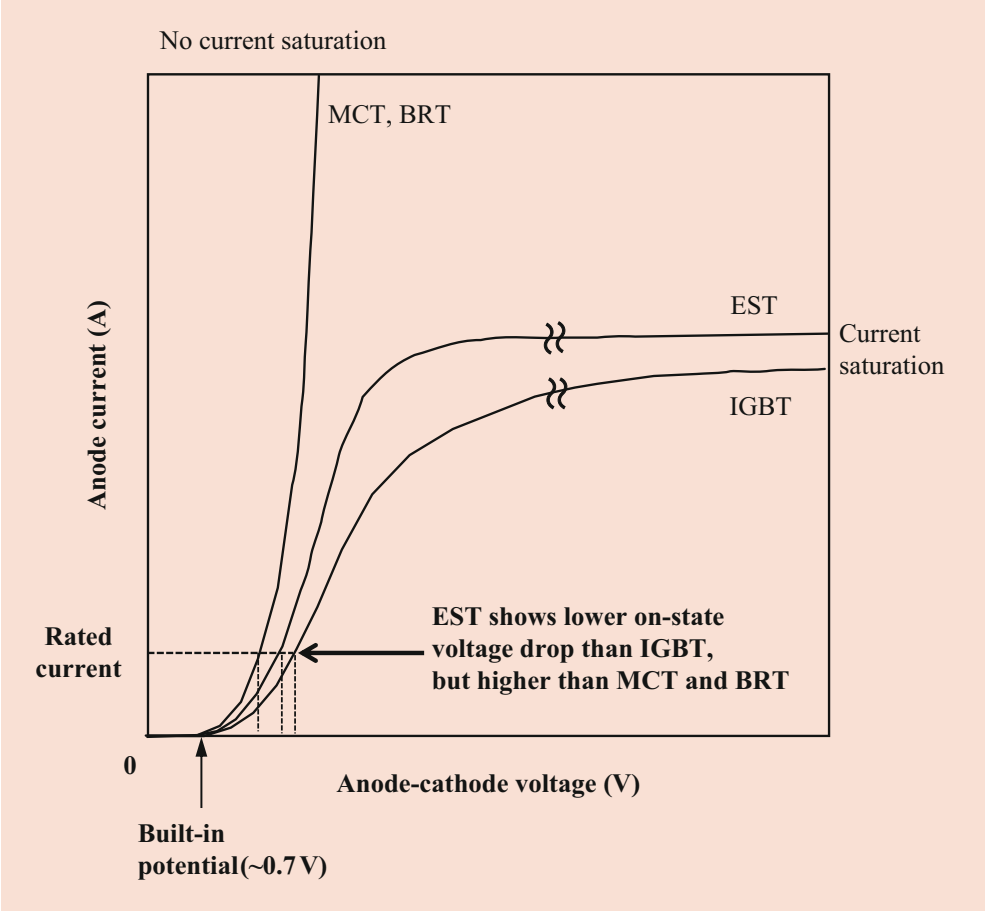


Fig. 13.66 Comparison of current-voltage curves of MCT, BRT, EST, and IGBT

forward current mode and the leakage current in the reverse blocking state are in a trade-off relation. For this reason, the metal formation should be optimized carefully to meet the specific target and application for which the SBD is designed.

Figure 13.67 shows cross sections of a junction barrier controlled Schottky (JBS) diode, along with a Schottky barrier and pin diodes. The JBS diode was presented first in [44] and has a Schottky contacts with p-n junctions consisting of a p+ region and n-drift layer incorporated into the n-drift region. The Schottky contacts are formed with the n-drift region and the ohmic contacts are with the p+ regions, so the JBS diode comprises SBDs and pin diodes connected in parallel. The JBS diodes show low-power dissipations in reverse recovery, and thus the important point to design the JBS diodes is to reduce the on-state voltage drop for the target breakdown voltage. The total on-state voltage drops are mainly the sum of the voltage drops over the Schottky junction and the n-drift layer. The important design parameters are Schottky barrier height and current ideality factor as the Schottky properties, and the dimensions (depth and width) of p+ region, and the doping concentration and thickness of the n-drift layer. The n-drift layer immediately beneath the Schottky contact is placed between p+ regions, to deplete the layer in the Schottky interface region in order to limit the leakage current, with the level of restraint correlated to the thickness of the depletion layer. When reverse voltage is applied, the depletion layers expand into the channel between the p+ regions and pinch off the Schottky barrier. With this, a potential barrier is formed, which restricts the high electric field at the Schottky interface while a further increase in reverse voltage is supported by the n-drift region. The distance between the p+ regions must be so designed that the pinch-off is completed before a high electric field at the Schottky interface exceeds the point where inordinate leakage current takes place.

When a forward voltage is applied, the unipolar current flows through the channels. The channel regions should be placed with a sufficient distance that their depletion regions do not contact each other in a forward voltage or even zero voltage application; thus, a conductive current path is kept enough through the n-drift region between Schottky interface and the n+ substrate. Since forward voltage drop results in on-state power dissipation, the thickness and doping

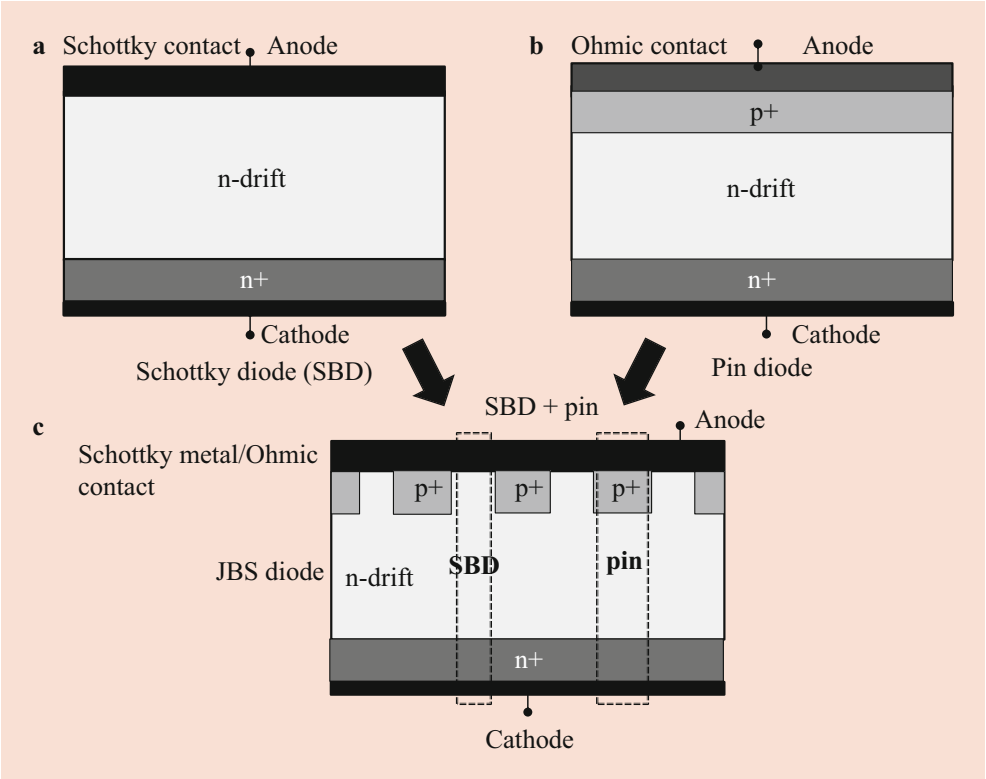


Fig. 13.67 Schematic cross section of the (a) Schottky, (b) Pin, and (c) JBS diodes

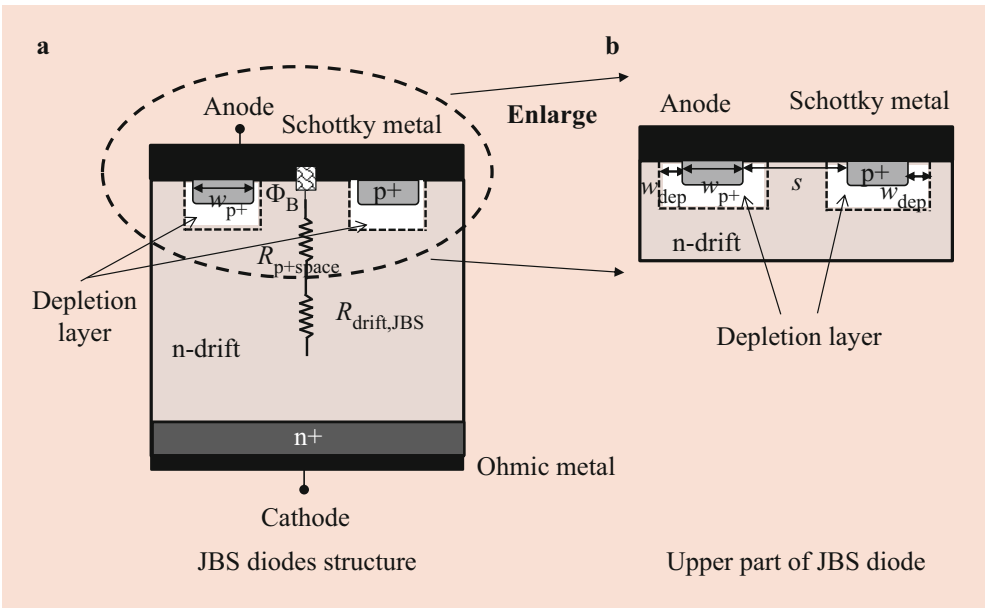


Fig. 13.68 Unit cell of JBS rectifier with geometrical parameters defined. (a) Cross section of JBS rectifier. (b) Upper part of JBS diode

concentration of the n-drift layer should be optimized in the diodes, to simultaneously attain lower on-resistance and higher blocking voltage. Figure 13.68 shows a unit cell and an enlarged view of a JBS diode. According to [130], the current density through the Schottky barrier for a stripe p+ region is given by

$$J_{\mathrm{F,JBS}} = \frac{s + w_{\mathrm{p+}}}{s - 2w_{\mathrm{dep}}} J_{\mathrm{F}}, \tag{13.45}$$

where s is the spacing in between the p+ regions, $w_{\mathrm{p+}}$ is the width of the p+ regions, and w_{dep} is the junction depletion width from the p+ regions. Based on the thermionic emission model, the total forward voltage drop of a JBS diode at a given current density is expressed by

$$V_{\mathrm{F,JBS}} = \frac{kT}{q} \ln\left(\frac{J_{\mathrm{F,JBS}}}{A^{**}T^2}\right) + \Phi_{\mathrm{B}} + R_{\mathrm{p+space}} \times J_{\mathrm{F}} + R_{\mathrm{drift,JBS}} \times J_{\mathrm{F}}, \tag{13.46}$$

where k is Boltzmann's constant, q is the charge on electron, T is the absolute temperature, J_{F} is the forward current density at $V_{\mathrm{F,JBS}}$, A^{**} is Richardson's constant, $R_{\mathrm{drift,\,JBS}}$ is the resistance of n-drift region, and $R_{\mathrm{p+\,space}}$ is the total amount of the resistance from the p+ regions and current flowing and distributing below the region. According to this equation, it is found that the main parameters to optimize are Schottky barrier height, the dimension of the p+ region (width and depth), and the resistance in n-drift region, thereby controlling the trade-off between on-state voltage drop and reverse leakage current. So, the improvement of the reverse leakage characteristics without an increase in on-resistance is achieved when the spacing and width/depth of the p+ region are optimally designed.

13.5.2 Bipolar Devices

In medium- and high-voltage applications (600–3300 V), it has become highly important to design the power bipolar rectifier, typically a pin diode with a low on-state voltage drop and good switching performances. Since IGBT modules comprise several IGBT devices and free-wheeling diodes (FWDs) mounted on an isolated substrate in the module for ease of system assembly, the superior characteristics of IGBT modules strongly depend on improvement not only in IGBT but also FWD technology. The crucial characteristics for FWDs are (i) low forward voltage drop, (ii) short reverse recovery time, (iii) small peak reverse recovery current, and (iv) soft reverse recovery characteristic. As described above (Sect. 13.3.2), IGBT modules are utilized in many power electronics applications, to control the power transmitted to the inductive load (see Fig. 13.40). After IGBT turn-on, the IGBT current increases rapidly and gets to an apex defined by the total amount of the load current and the peak reverse recovery current in the diode. In this operation, the diode current decreases at a constant rate until the diode can support voltage; and as a result, a large reverse-recovery current flows because of the stored charge. As in the case of IGBTs, pin diode reverse recovery is discussed through analysis of the reverse recovery physics of the pin diode structure. Figure 13.69 shows the current and voltage waveforms of pin diode reverse recovery for an inductive load, and Fig. 13.70

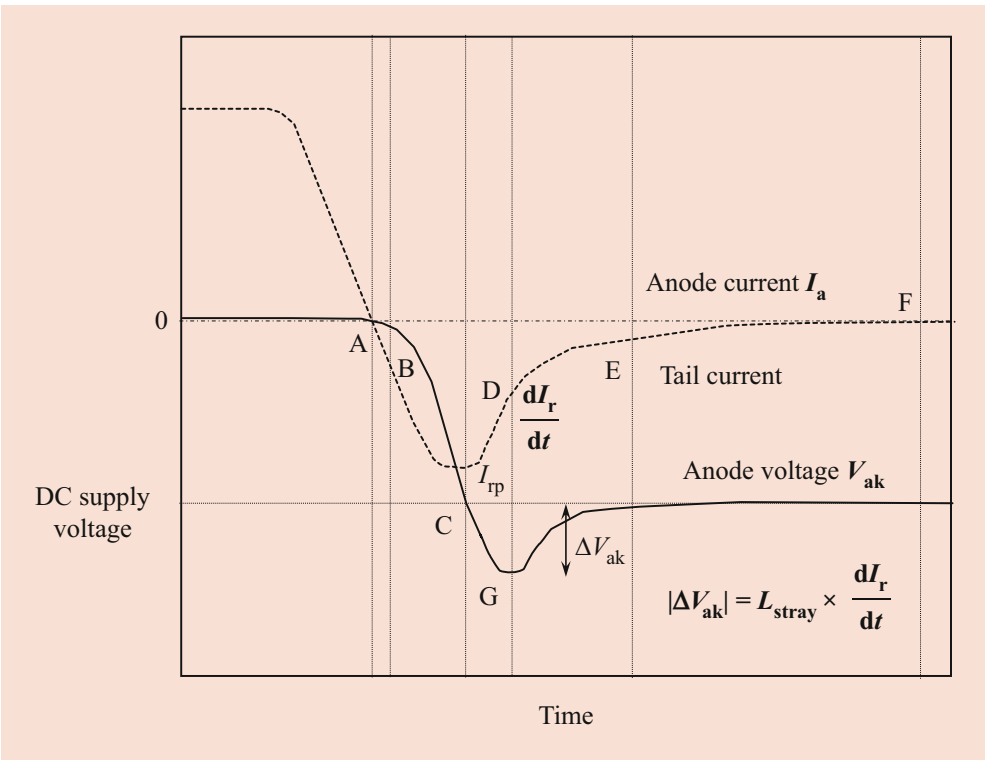
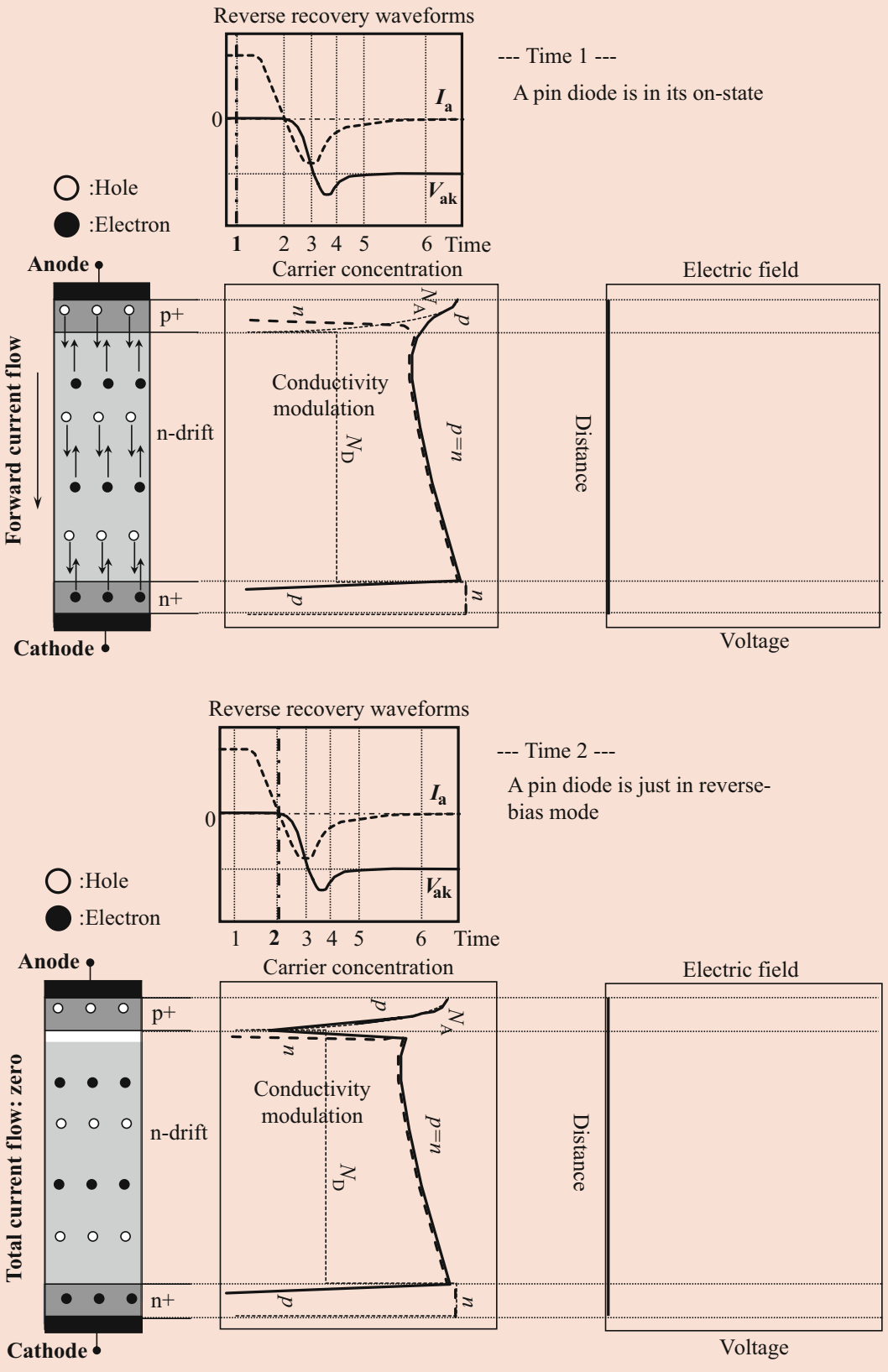


Fig. 13.69 Pin diode reverse recovery waveforms for an inductive load



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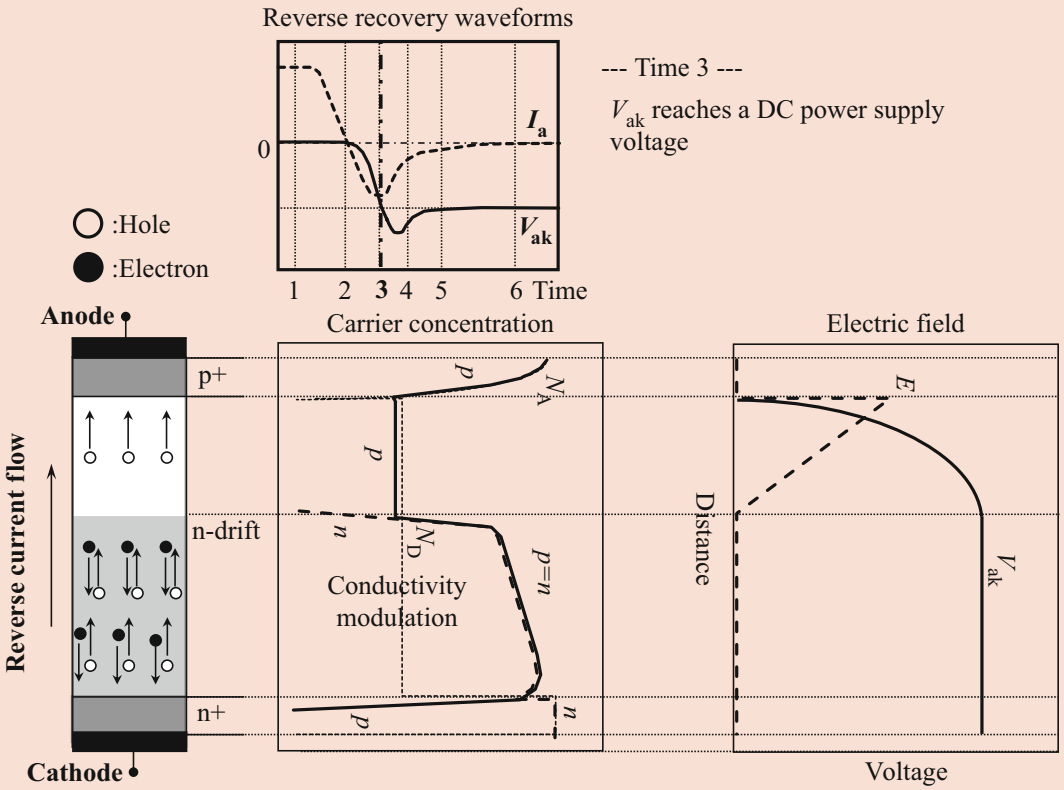

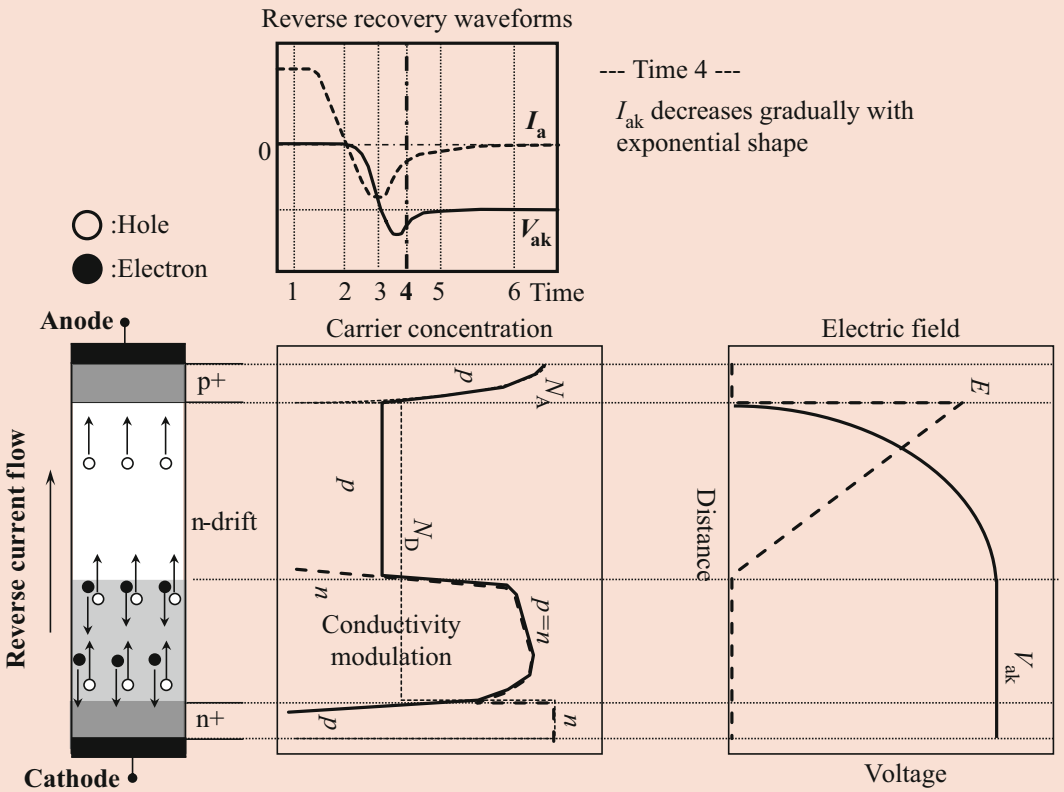

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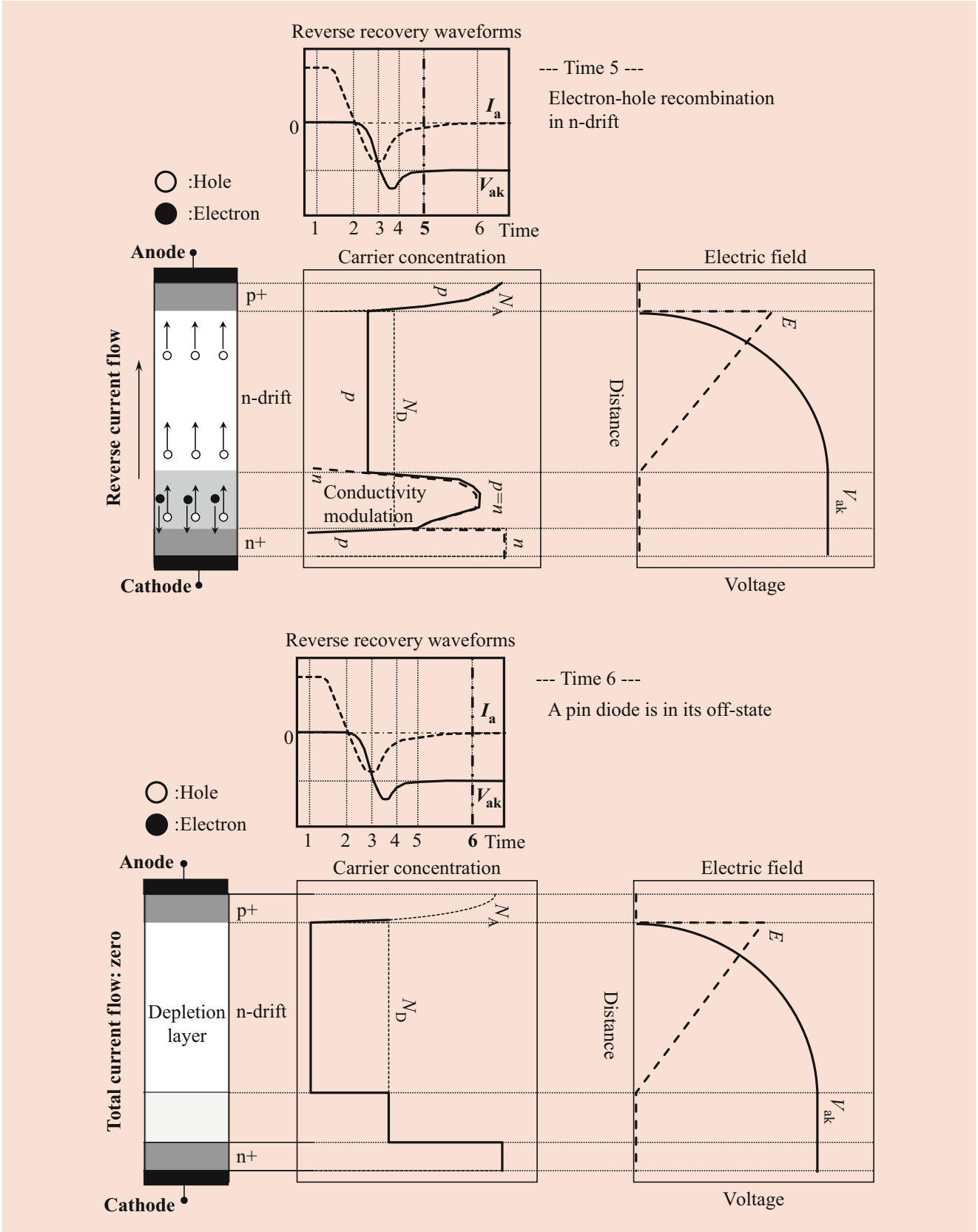

Fig. 13.70 A pin diode carrier dynamics, electric field, and voltage distribution during reverse recovery process

details the stored-carrier dynamics and electric field and voltage distribution in the reverse recovery.

When a forward current flows through pin diodes, the n-drift layer is strongly conductivity-modulated, and electron and hole concentrations become much larger than the donor density in the n-drift layer, resulting in low forward voltage drop of the diode (Time 1 in Fig. 13.70). First, the anode current in the diode decreases at a constant rate and remains in its forward-biased mode until Point A in Fig. 13.69. After the direction of current flow is changed from forward to reverse, the voltage across the diode starts to increase in the module, with the diode in reverse-bias mode, until it reaches the power source voltage ("B" in Fig. 13.69; Time 2 in Fig. 13.70). In this regime, the stored electrons and holes are swept away by depletion layer expansion. When the reverse voltage equals the voltage in the DC power source, the current flowing through the diode in reverse direction reaches its peak level, I_{rp} ("C" in Fig. 13.69; Time 3 in Fig. 13.70). Then, the current starts to transfer from the diode to the IGBT; thus, the current initially decreases relatively sharply ("D" in Fig. 13.69), and then more gradually with an exponential shape, due to the recombination of large amounts of stored electrons and holes in the n-drift layer near the n+ cathode side ("E" in Fig. 13.69; Times 4 and 5 in Fig. 13.70). As in the case of IGBT turn-off waveforms, the simultaneous presence of high voltage and current leads to large power dissipation in the pin diode, so it is necessary to lower the level of the tail current and shorten the time duration of the turn-off operation.

It should be noted that the sharp increase in the anode or surge voltage ("G" in Fig. 13.69) is caused by a sudden decrease in the diode anode current ($\mathrm{d}I/\mathrm{d}t$) associated with stray inductance L_{stray} in the circuit ($L_{stray} \times \mathrm{d}I/\mathrm{d}t$). This is referred to as a "hard recovery characteristic" and could cause noise emission and device failure. Therefore, optimal design of the forward voltage drop, reverse-recovery characteristics, and surge voltage reduction in the pin diode are also strongly required in order to achieve superior circuit efficiency in voltage source converters. Finally, the anode current falls to zero and the off state is reached ("F" in Fig. 13.69; Time 6 in Fig. 13.70).

As in the IGBT switching operation, the high voltage and current present at the same time, resulting in large power loss in the diode. Since the peak reverse recovery current flows through the IGBT, which controls this switching operation, it is highly important to minimize the peak level of the reverse recovery current and reverse recovery time of the diode (i.e., the duration of the reverse recovery operation).

It should be noted that the sharp increase in the anode voltage in reverse direction (i.e., the surge voltage) is caused by a sudden decrease in the diode current ($\mathrm{d}I/\mathrm{d}t$) associated with stray inductance L_{stray} in the circuit ($L_{stray} \times \mathrm{d}I/\mathrm{d}t$). Therefore, optimal design for forward voltage drop, reverse recovery, and surge voltage reduction in the diode is also strongly required in order to achieve superior circuit efficiency in the voltage source converter. The requirement for soft reverse recovery behavior derives from the high-voltage spikes that can occur if the reverse recovery $\mathrm{d}I/\mathrm{d}t$ is large. The pin diode technological innovation presented a breakthrough in removal of the surge and spike voltage and current and voltage oscillation under any severe conditions as well as in power dissipation and cost reduction. The tendency for oscillation enhances during reverse recovery of the lower current, especially around one-tenth of the nominal current, so the softness characteristic can be improved by an enhanced holes and electrons injection in the device; however, this results in higher recovery power dissipations at the pin diode. The device was designed and developed to show the maximized softness with a minimum of injected holes and electrons; consequently, the latest pin diodes must exhibit both softness characteristic and the minimized recovery loss with a very smooth switching waveform in high output power applications. A variety of high-voltage diodes have been proposed and investigated in the attempt to achieve these goals [131–133]. Figure 13.71 shows the structures of the static shielding diode (SSD) and merged pin and Schottky (MPS) diode. In these diodes, the goal is to minimize the amount of stored charge within the n-drift region during a forward conduction operation, by reducing the hole injection of the p+/n- surface junction.

SSD and MPS Diodes

In the SSD (Fig. 13.71a), a shallow lightly doped p-layer and a part of the n-layer are surrounded by a heavily doped p+ region. The width of the p-n junction surrounded by the p+ region is defined as the channel width W_{ch} . The p-layer is thin and has a low doping concentration. In the SSD, the main forward current path is the p-n-n+ diode region. It has been shown that the on-state voltage drops and reverse recovery time in a p-n-n + diode decreases with decreasing doping concentration in the p-layer [44], and this provides the SSD with low-loss, high-speed capability. The channel region is narrowed such that the electrical field near the p-n junction is lowered in the reverse blocking mode, resulting in higher blocking voltage. And as the p-n junction is shielded by applying a reverse voltage, the diode is designated as a static shielding diode or SSD.

The MPS diode design concept is based on the integration of a Schottky contact region and p-n junction of p+ region and n-drift region grid structure, as shown in Fig. 13.71b. In terms of reverse blocking capability, pure Schottky rectifiers fabricated for high breakdown voltage have been shown to often exhibit extremely soft breakdown waveforms, which has been associated with the Schottky barrier lowering effect. However, the barrier lowering effect can be reduced in the MPS diode, through the use of p-n junctions surrounding

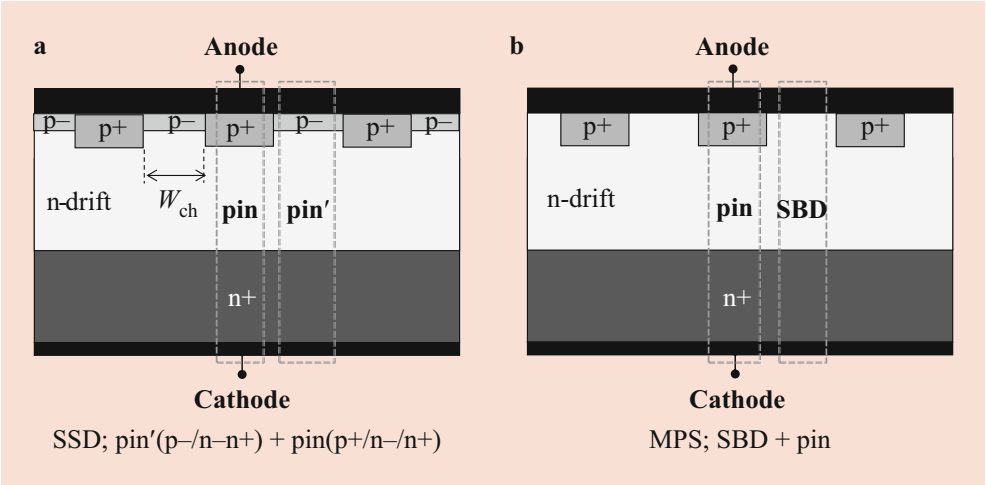

Fig. 13.71 Cross section of the power rectifier structure. (**a**) SSD; (**b**) MPS

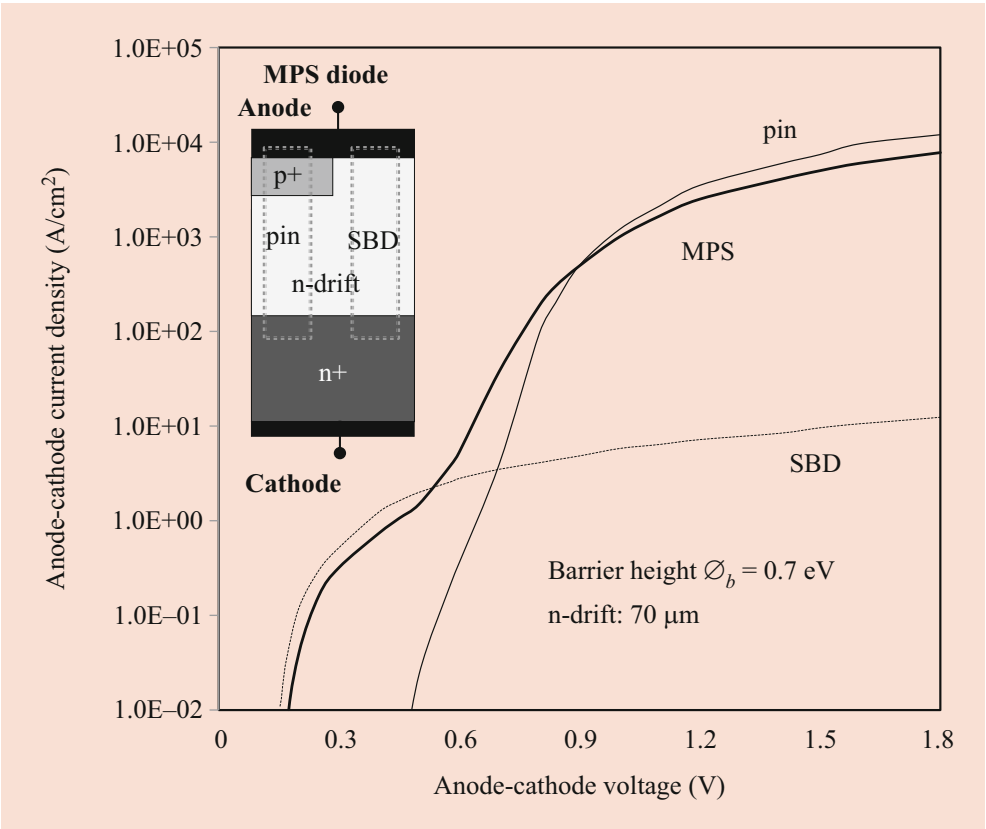

Fig. 13.72 An example of calculated forward characteristics of an MPS diode with 50% Schottky area (breakdown voltage = 700 V)

the Schottky interface. The depletion layers related to these junctions produce a potential barrier below the Schottky interface, preventing the electric field from increasing at the interface. In this way, the MPS diode can be designed to show a breakdown voltage equal to that of the pin diode. Figure 13.72 shows examples of calculated forward characteristics. The MPS diode operates at current densities intermediate to the Schottky and pin diodes at forward voltage drops of less than roughly 0.6 V. However, at higher forward voltage drops, the diode operates at a higher current density than these diodes. In terms of reverse recovery, the MPS diode exhibits a lower peak recovery current, shorter recovery time, and smaller dI/dt. This improvement in performance is because of the decrease in stored electrons and holes in the n-drift region. Consequently, an MPS diode trade-off curve between forward voltage drop and stored electrons and holes

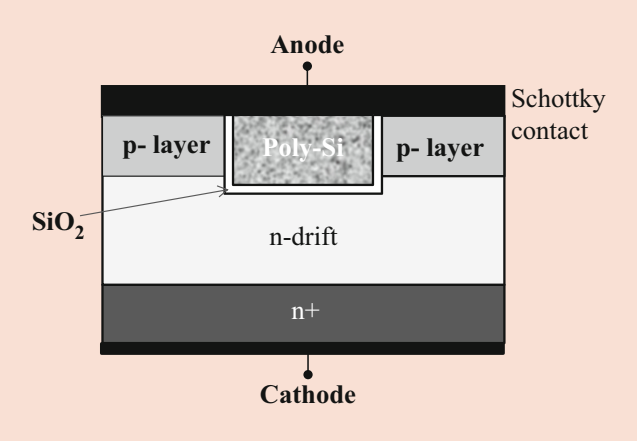

Fig. 13.73 Cross section of the trench MOS barrier Schottky diode structure

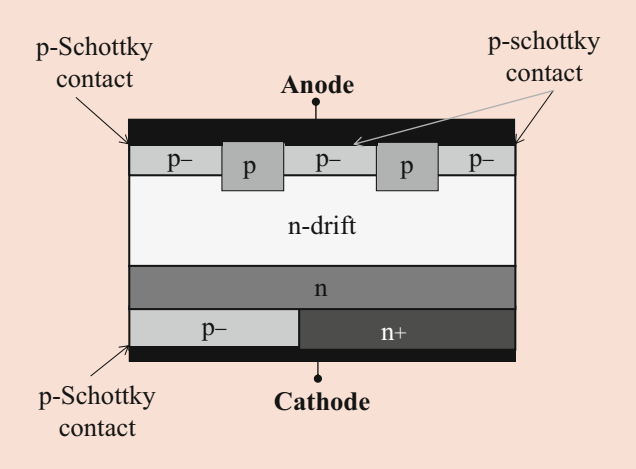

Fig. 13.74 Cross section of the Schottky controlled injection diode structure

has been obtained by changing the areal percentage of the Schottky region while maintaining a constant lifetime [134]. The results clearly indicate that a much superior trade-off is achieved by optimizing the width and depth of each region in the device in the MPS diode. Notably, this method of MPS diode optimization has the advantage that it can be performed during device layout and design, without the additional processing costs associated with the lifetime control processes used in pin diode design.

State-of-the-Art Diode Structure

Diode improvement is steadily undergoing structural optimization of the anode and cathode regions, including advancements in lifetime distribution design. Given the comparative simplicity of the basic diode structure, there remains room for further improvement in characteristics such as forward voltage drop and recovery loss, through optimization of the anode structure and lifetime control is still available at this time [134–137]. Hsu et al., for example, reported improvement in the on-resistance of 300 V and 600 V diodes, with the use of so-called trench MOS barrier Schottky (TMBS) (Fig. 13.73) or tandem PiN Schottky (TPS) structures [135, 136], in which the anode layer is composed of a combination of a thin p-layer and a Schottky barrier junction. Since the Schottky characteristics can be maintained, the forward voltage drop can be dramatically reduced; and since the minority carriers in the n-drift region can be minimized in the on-state, the trade-off characteristic between the forward voltage drop and reverse recovery loss is dramatically improved. Kameyama et al. [137] reported that by controlling the hole and electron trap density, it is possible to fabricate diodes with low loss dissipation and spike voltage suppression in reverse recovery transient. In their study, the energy level and hole and electron trap concentration were adjusted by varying the helium irradiation and annealing process parameters. Matsudai et al. proposed the so-called Schottky controlled injection diode structure [138] (Fig. 13.74), in which a flat and linear carrier profile is achieved during the on-state by controlling the electron flow in the p-Schottky region, low hole injection from the p-anode region, and electron injection from the cathode and by ensuring a high lifetime effect in the drift region; with the result that low forward voltage drop, short reverse recovery time, and small leakage current can be simultaneously attained even at high temperatures.

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Silicon Carbide Power Devices

14

B. Jayant Baliga

Contents

14.1 Introduction 491
14.2 Ideal Specific on-Resistance for Silicon Carbide 493
14.3 Silicon Carbide Power Rectifiers 494
14.4 Silicon Power MOSFETs 496
14.5 SiC Power DI-MOSFET Structure 498
14.5.1 Blocking Characteristics 498
14.5.2 On-Resistance 500
14.5.3 Threshold Voltage 503
14.5.4 Reliability 503
14.6 Shielded SiC Planar Power MOSFET Structure 505
14.6.1 Device Structures 505
14.6.2 Gate Oxide Screening 505
14.6.3 Threshold Voltage 505
14.6.4 Channel Mobility 507
14.6.5 On-Resistance 507
14.6.6 Experimental Results 508
14.7 Silicon Carbide Power MOSFETs with Improved High-Frequency Performance 510
14.8 SiC Power MOSFET Body-Diode 510
14.9 Silicon Carbide Power JBSFETs 511
14.10 Unclamped Inductive Switching Stress 512
14.11 Short-Circuit Capability 512
14.12 Shielded Trench-Gate Power MOSFET Structure 512
14.12.1 Device Structure 513
14.12.2 On-Resistance 513
14.12.3 Experimental Results 514
14.13 SiC Trench-Gate MOSFET with Thick Trench Bottom Oxide 515
14.14 SiC Trench-Gate MOSFET with Deep P+ Trench Regions 516
14.15 SiC V-Groove Trench-Gate MOSFET 516
14.16 Silicon Carbide Bi-Directional Field Effect Transistor 517
14.17 Commercial Devices 518
14.18 Silicon Carbide Power Device Applications 519
14.19 Conclusions 520
References 521

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Abstract

Power and energy in all sectors of the economy are controlled using power semiconductor devices. Power electronics has relied up on silicon power devices for over half a century. Improvement in performance by replacing silicon devices with silicon carbide devices was recognized in the early 1980s. Subsequent progress with the growth of high-quality large diameters SiC wafers and innovations in SiC device structures have enabled their commercialization since 2005. This chapter discusses the physics and design of SiC unipolar devices, as well as their applications.

Keywords

ACCUFET · Baliga's Figure of Merit · BiDFET · Electric vehicles · IGBT · JBS diode · JBSFET · Motor drives · Specific on-resistance · Power MOSFET · Silicon carbide

14.1 Introduction

The efficient generation, distribution, and management of power is essential in modern society to mitigate environmental impact and global warming. This was accomplished using bipolar silicon power devices in the 1950s. Silicon bipolar transistor and thyristor ratings were enlarged rapidly to serve

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more applications. The cumbersome control and protection circuitry for these devices led to high cost and unwieldy solutions. The advent of MOS technology for digital circuits created a new class of devices in the 1970s for power switching applications. Silicon power MOSFETs are now extensively used in high-frequency applications with relatively low operating voltages (under 100 V). Another class of silicon devices evolved in the 1980s with the merger of MOS and bipolar physics. The Insulated Gate Bipolar Transistor (IGBT) [1] has been the most successful innovation among these types of devices. It has become the technology of choice for all medium- and high-power applications due to high power density, simple interface, and ruggedness.

The concept of two-dimensional charge coupling was created in the 1990s to significantly reduce the on-state resistance of silicon power devices [2, 3]. An electrode embedded inside a deep vertical trench formed the basis for the first approach. A new generation of silicon power MOSFETs and diodes has been commercialized with voltage ratings of 30–200 V with this method. A second approach relies up on alternating vertical columns of P and N type silicon regions. Power MOSFETs with blocking voltages around 600 V have been commercialized using this method. All wide bandgap semiconductor power devices must compete with these advanced silicon power devices that are now available in the market.

Applications for power devices range over a broad spectrum of power levels and frequencies as shown in Fig. 14.1. On one extreme, HVDC power distribution and electric trains require control of megawatts of power at low frequencies. On the other extreme, very high frequency applications require only 100 watts of power. Device power ratings decrease when the operating frequency increases. These applications are primarily utilize silicon devices today.

The current and voltage requirements for some applications are shown in Fig. 14.2. In telecommunications and display drives, multiple high-voltage devices are required. Silicon devices can be integrated on a single monolithic chip when the current falls below 1 ampere for these applications. Discrete power MOSFETs are needed for automotive

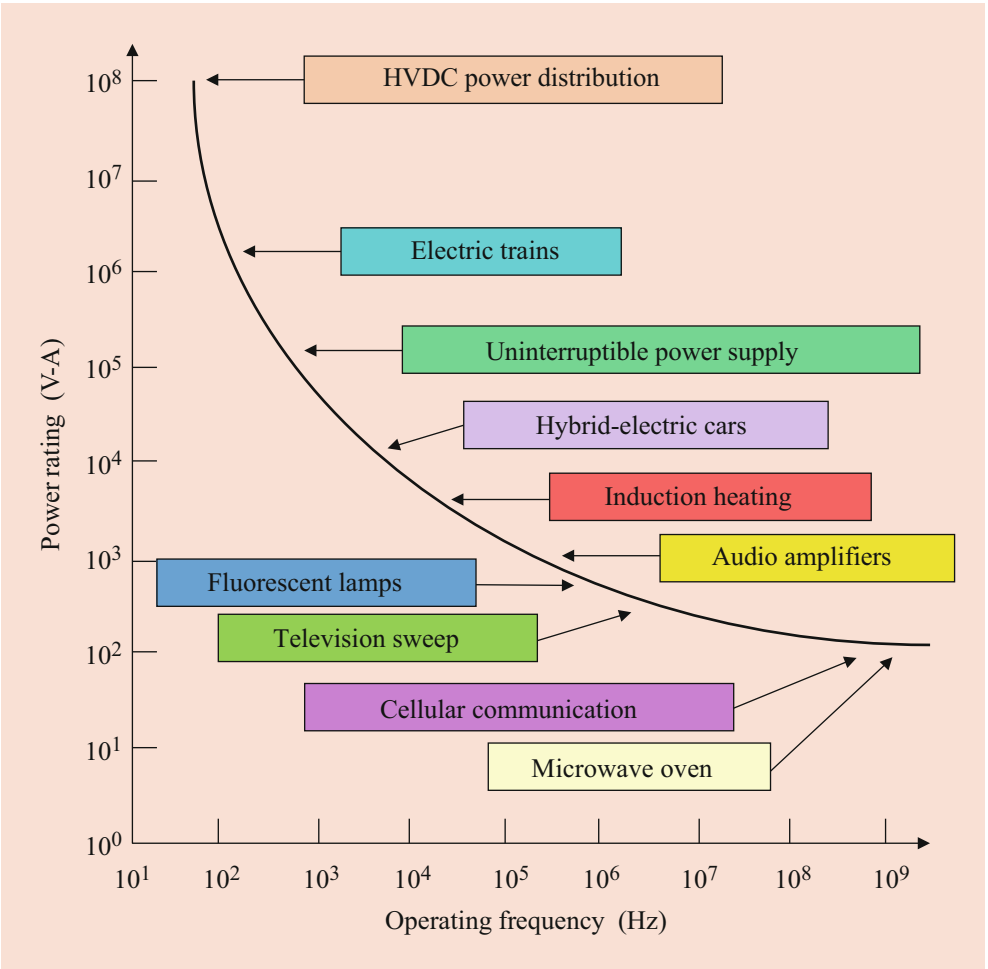

Fig. 14.1 Power semiconductor device applications

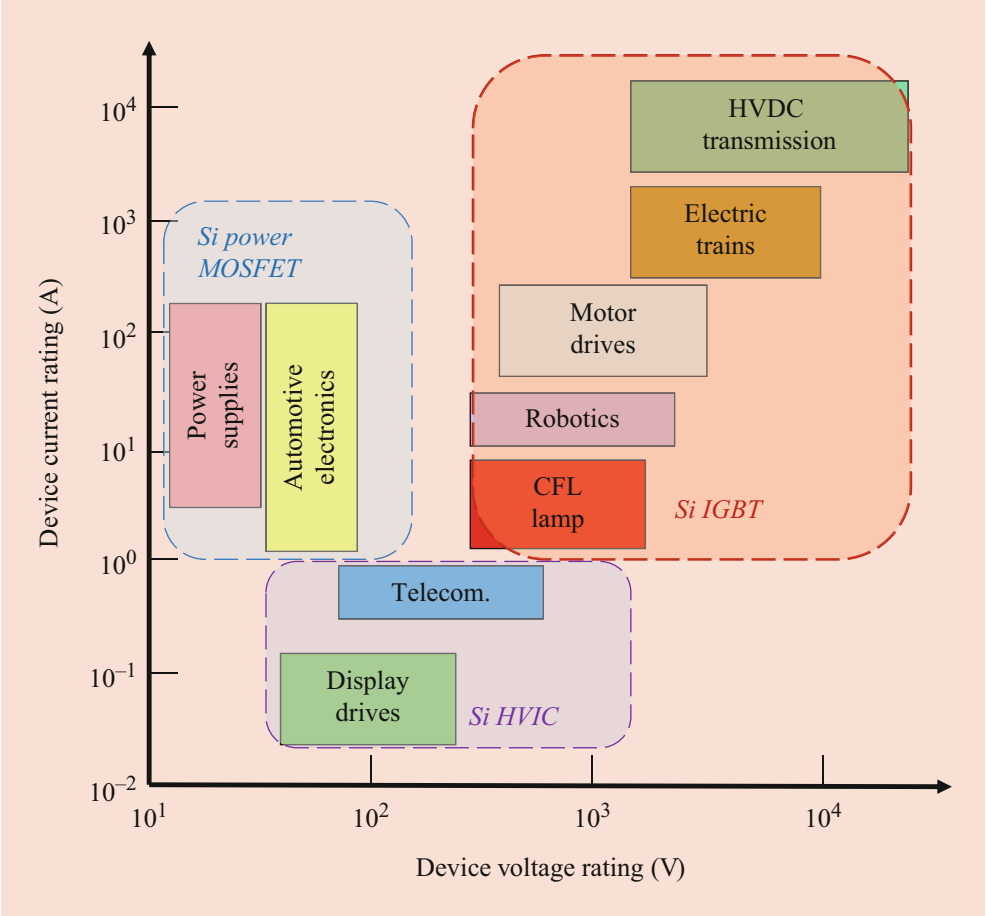

Fig. 14.2 Silicon power device ratings for various applications

electronics and switch mode power supplies where high currents must be delivered. Silicon IGBT modules have been developed during the last decade with blocking voltages of 6500 V and current handling capability of 1000 A. They have enabled voltage source converters for HVDC power distribution. For applications with operating voltages over 300 V and high current handling capability, the IGBT has been proven to be the best technology. All sectors of the economy, including consumer, industrial, transportation, lighting, medical, defense, and renewable energy generation, rely up on this device today [1].

Despite huge strides in improving the performance of silicon power MOSFETs and IGBTs during the past 25 years, it has become apparent that the performance of power electronic applications can be enhanced in terms of efficiency, size, and weight by replacement of silicon devices with devices made from wide band gap semiconductors. This has motived the development of power devices from silicon carbide material due to its large band gap of 3.3 eV compared with 1.1 eV for silicon. This chapter discusses the merits of silicon carbide and the performance of power rectifiers and MOSFETs that can be made using this material.

14.2 Ideal Specific on-Resistance for Silicon Carbide

The performance of vertical unipolar power devices is constrained by the ideal specific on-resistance for the drift region given by [4]

$$R_{\text{on-ideal}} = \frac{4\ \text{BV}^2}{\varepsilon_S\ \mu_n\ E_C^3} \tag{14.1}$$

where BV is the device breakdown voltage, ε_S is the semiconductor dielectric constant, μ_n is the electron mobility, and E_C is the critical electric field for breakdown. The denominator is now commonly referred to as Baliga's Figure-of-Merit (BFOM) [5, 6] for semiconductors:

$$\text{BFOM} = \varepsilon_S\ \mu_n\ E_C^3 = \frac{4\ \text{BV}^2}{R_{\text{on-ideal}}} \tag{14.2}$$

It allows assessment of the maximum power handling capability (W/cm^2) of unipolar power devices made from var-

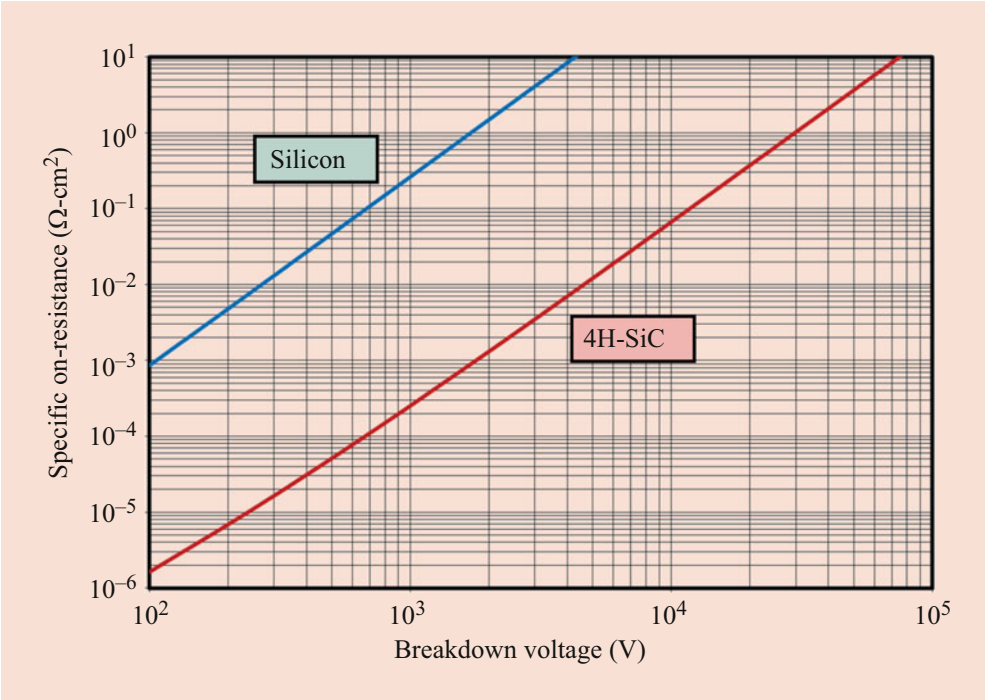

Fig. 14.3 Ideal specific on-resistance for silicon carbide power devices

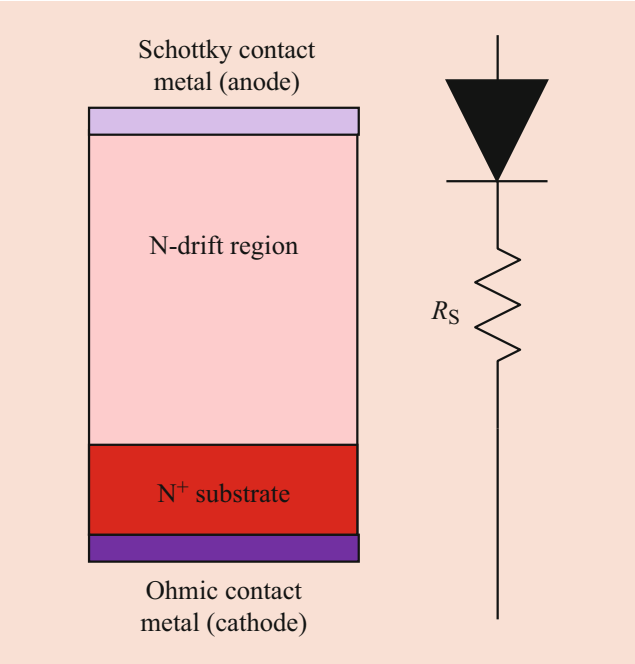

Fig. 14.4 Basic power Schottky rectifier structure

ious materials. The BFOM for silicon carbide is 1000 times superior to that for silicon mainly due to the approximately tenfold increase in the critical electric field for breakdown. Silicon carbide unipolar high-voltage power devices with low on-state voltage drop can be created due to the large BFOM for this material.

The 4H-SiC ideal specific on-resistance is shown in Fig. 14.3 for devices with breakdown voltages ranging from 100 to 100,000 V. The values for the ideal specific on-resistance of silicon devices are shown in the figure for comparison. The ratio of the specific on-resistance for these materials increases from about 500 at 100 V to 1300 at 40,000 V. Unipolar SiC power devices such as Schottky rectifiers and power MOSFETs have been created with low on-state voltage drop and excellent switching speed. They have begun to replace silicon bipolar power devices such as P-i-N rectifiers and IGBTs.

14.3 Silicon Carbide Power Rectifiers

Power P-i-N diodes made from silicon rely up on the injection of minority carriers during on-state current flow [4] to achieve low on-state power losses. The reverse recovery process produces a large reverse current during turn-off for removal of these minority carriers. Significant power losses occur in the diode and the power switches in circuits due to the reverse recovery current. The unipolar Schottky rectifier operates without minority carrier injection eliminating the reverse recovery current. The power Schottky rectifier structure is illustrated in Fig. 14.4. It has an n-drift region designed to support the reverse blocking voltage. The drift region resistance increases drastically with increasing blocking voltage. Commercially available silicon Schottky rectifiers are limited to blocking voltage rating up to 150 V because the

on-state voltage drop becomes unacceptably large. Silicon P-i-N rectifiers are required circuits with larger operating voltages in spite of their high switching losses.

The low drift region resistance of silicon carbide Schottky rectifiers, as shown in Fig. 14.3, allows creating low on-state voltage drop devices with very high blocking voltage capability. The on-state characteristics of SiC Schottky rectifiers with various voltage ratings are shown in Fig. 14.5 for the case of a typical metal-semiconductor barrier height of 1.1 eV. The current flow is limited by the Schottky barrier at low on-state current levels. The series resistance of the drift region begins to contribute to the on-state voltage drop when the current density exceeds 100 A/cm^2. This contribution is small for devices with blocking voltages of up to 3000 V. The on-state voltage drop has an acceptable value even for devices with a blocking voltage of 5000 V. SiC Schottky rectifiers can therefore be expected to replace silicon P-i-N rectifiers with blocking voltages as high as 5000 V.

A large increase in the reverse leakage current with increasing reverse bias voltage is observed in SiC Schottky rectifiers. The reverse leakage current goes up by five orders of magnitude due to the Schottky barrier lowering and tunneling phenomena as demonstrated in Fig. 14.6. The resulting larger power loss during the blocking mode of operation becomes a serious thermal runaway problem for these rectifiers.

The Junction-Barrier controlled Schottky (JBS) structure [7, 8], shown in Fig. 14.7, was proposed to prevent the rapid increase in leakage current for Schottky rectifiers with increasing reverse bias voltage. In this structure, P^+ regions are selectively introduced below the Schottky contacts. The depletion region developed at the junction forms a potential barrier under the Schottky contact suppressing the electric field at the Schottky contact. The Schottky barrier lowering and tunneling phenomena are mitigated by the lower electric field at the Schottky contact [2].

The reduction in leakage current achievable with the JBS structure is demonstrated in Fig. 14.8. Here, the width of the P^+ region was kept fixed at 1 μm while changing the cell pitch. The increase in leakage current is only 10 times for a cell pitch of 2 μm (i.e. a Schottky contact width in the cell of 1 μm) compared with 100,000 times for the Schottky diode.

The P^+ region reduces the area of the Schottky contact and increases the drift region resistance by constriction of current flow between the junctions. The on-state voltage drop increases when compared with the Schottky rectifier as shown in Fig. 14.9. The increase in on-state voltage drop is small (~100 mV) if the cell pitch of 2 μm is used. This cell pitch is adequate to suppress the increase in leakage current as shown in Fig. 14.8.

All commercially available SiC power rectifiers utilize the JBS structure. Devices with voltage ratings of 1.2 kV have been used as anti-parallel diodes for silicon IGBTs since 2005. Devices with voltage ratings of 1.7 kV have recently been commercialized. Eventually, SiC JBS rectifiers are expected to become commercially available with voltage ratings extending from 600 V to 5 kV.

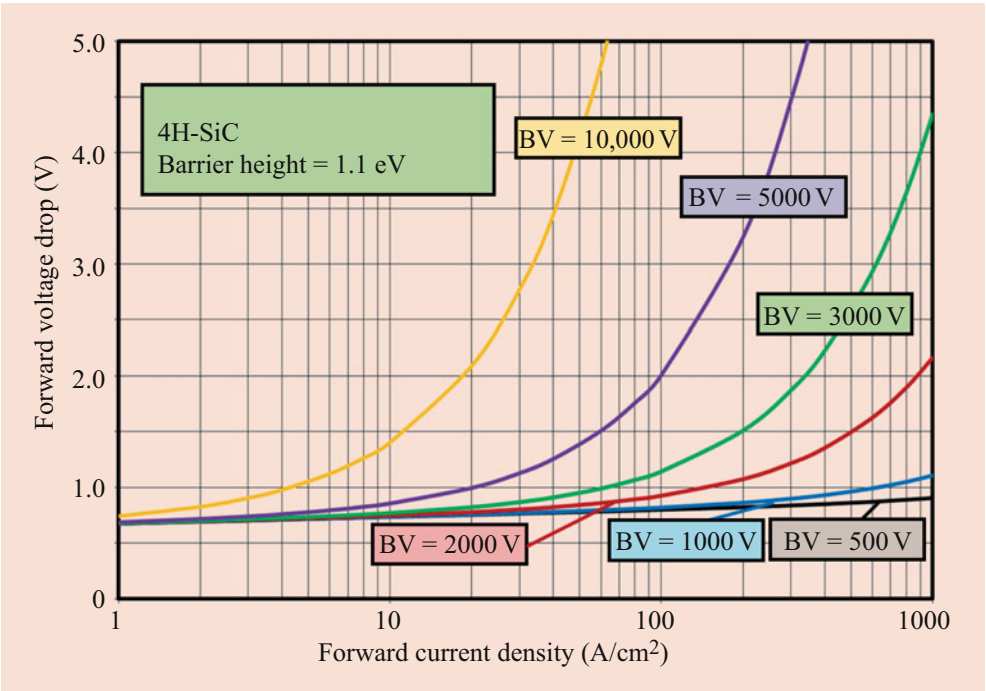

Fig. 14.5 On-state characteristics of SiC Schottky rectifier structures

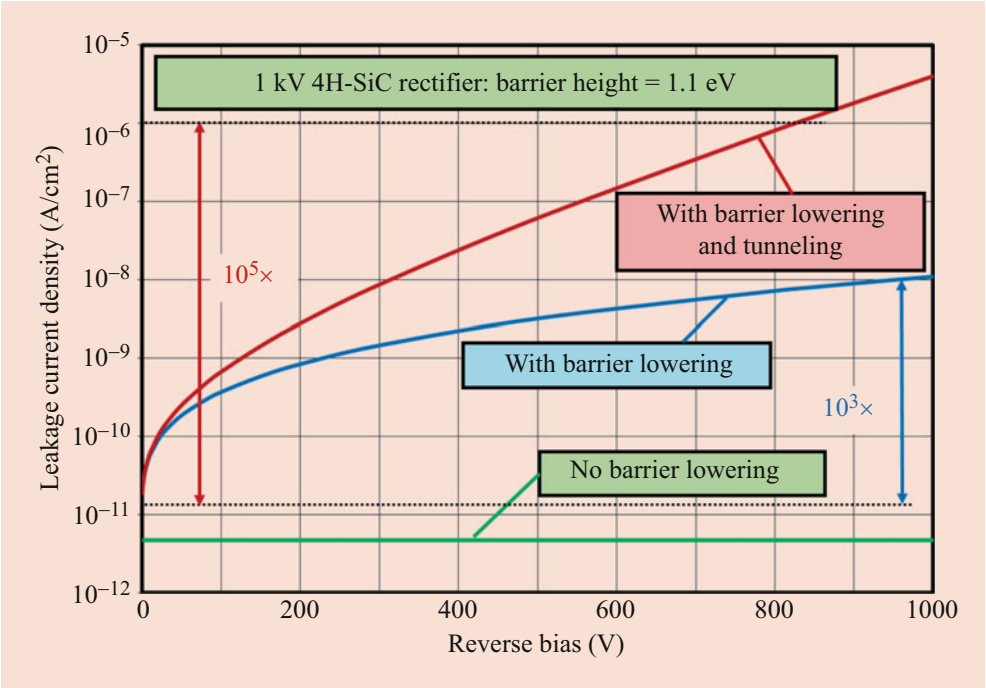

Fig. 14.6 Reverse leakage current for SiC Schottky rectifiers

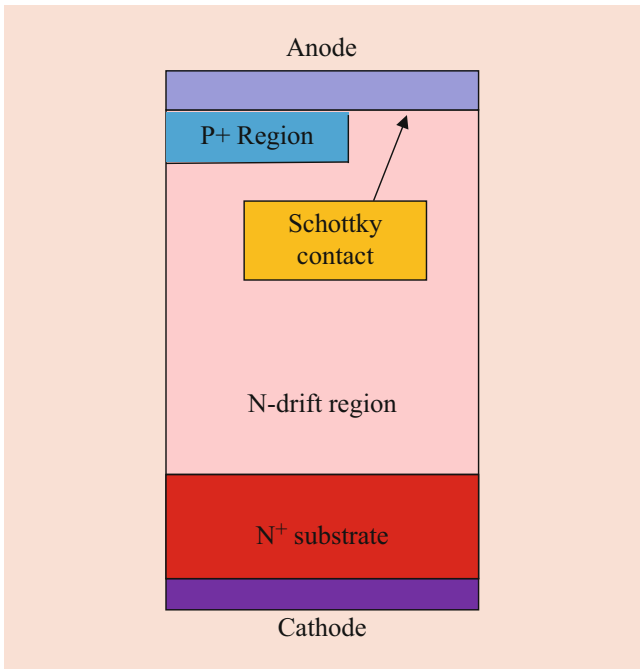

Fig. 14.7 Junction Barrier controlled Schottky (JBS) rectifier

14.4 Silicon Power MOSFETs

Silicon power MOSFET with blocking voltages below 150 V is available from many companies. Their structures are shown in Fig. 14.10. The P-base and N$^+$ source regions are self-aligned to the edge of the polysilicon gate electrode in the D-MOSFET structure. This is achieved by ion-implantation of boron flowed by its drive-in cycle to create the P-base region and then ion-implantation of phosphorus with its drive-in cycles to create the N$^+$ source regions. The difference in the lateral diffusion of the impurities under the gate electrode defines the channel length. A positive drain bias is supported across the P-base/N-drift region junction. The doping concentration and thickness of the drift region decides the voltage blocking capability. A rapid increase in the drift region resistance with increasing blocking voltage limits silicon power MOSFETs to below 150 V [4].

The gate electrode is embedded within a trench etched into the silicon surface for the silicon U-MOSFET structure shown in Fig. 14.10. The vertical extension of the P-base and N$^+$ source regions, as determined by the ion-implant energies and drive times for the dopants, determine the channel length. The channel is formed on the side-wall of the trench at the surface of the P-base region. The on-state resistance of the silicon U-MOSFET structure is less than that of the D-MOSFET structure because of elimination of the JFET region [2].

An important advancement in silicon power MOSFET technology was achieved by the introduction of the charge coupling concept. It allowed supporting high drain voltages with large drift region doping concentrations [3]. The silicon charge coupled graded-doped GD-MOSFET structure is illustrated in Fig. 14.11a [9, 10]. A deep trench region with a source connected electrode is added to the drift

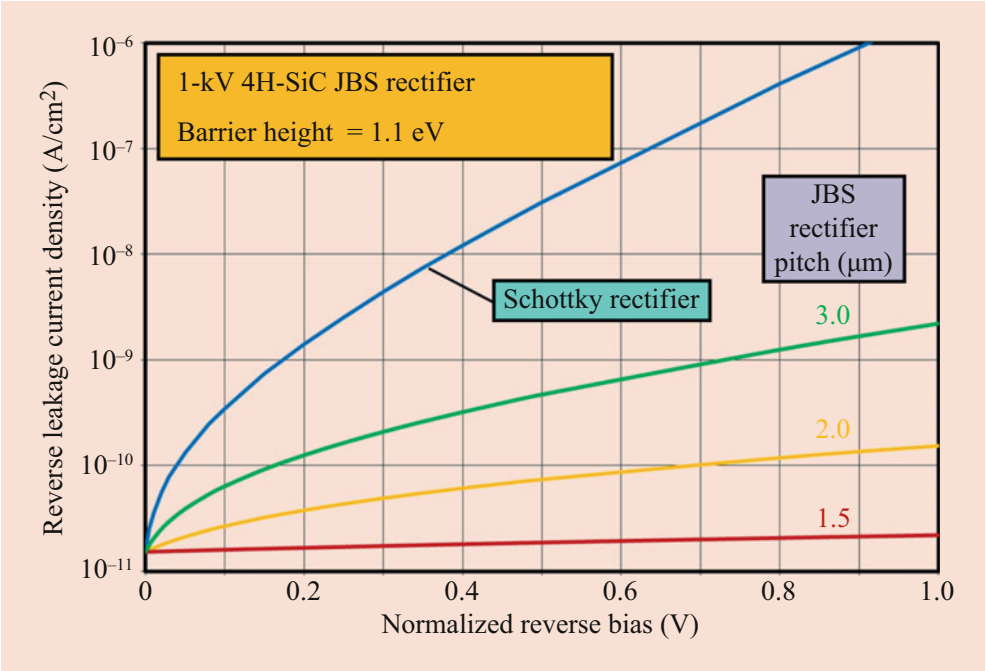

Fig. 14.8 Reduction of leakage current with the JBS structure

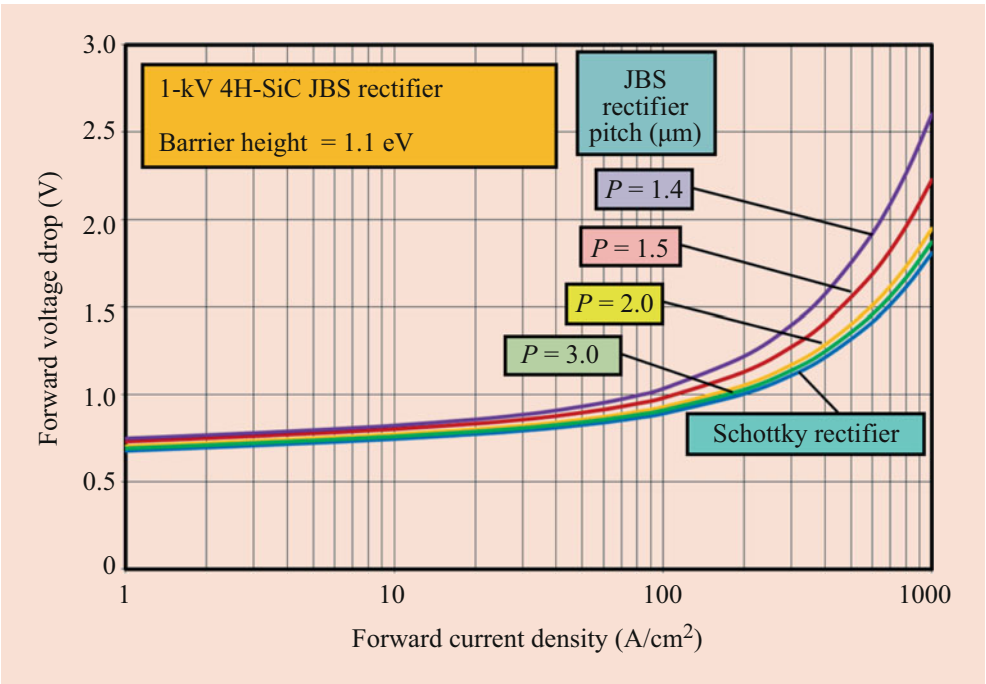

Fig. 14.9 Increase in on-state voltage drop for the JBS rectifier structure

region. A graded doping profile in the drift region with high doping concentrations [11] can be used to achieve blocking voltages greater than the parallel-plane breakdown voltage. The specific on-resistance of these devices is much (5–25 times) smaller than that of conventional silicon devices with blocking voltages ranging from 50 to 1000 V [3]. These devices have also been called split-gate devices.

A charge-coupled silicon power MOSFET with the superjunction structure is shown in Fig. 14.11b. The vertical P-N junction formed between columns of P and N drift regions [12] produces the charge coupling effect. This device has been optimized for blocking voltages between 600 and 900 V [3]. It has 3–10 times lower specific on-resistance compared with the conventional silicon power MOSFETs for

a breakdown voltage of 600 V. The specific on-resistance of 600 V rated superjunction devices is about 10 mΩ-cm^2.

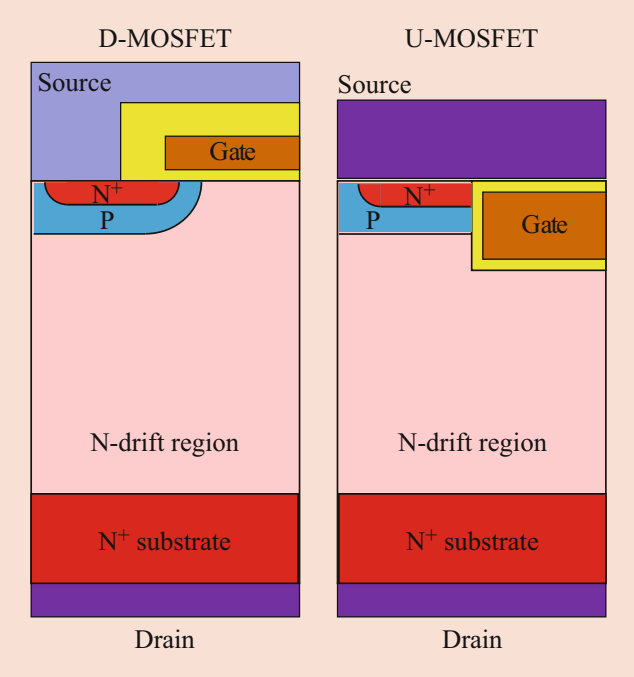

Fig. 14.10 Silicon power MOSFET structures

Products have been released by many companies using the above approaches. SiC power switches must compete with these new charge coupled silicon power MOSFET products. The charge coupled silicon devices require a more expensive fabrication process. This reduces the cost differential with SiC power MOSFETs.

14.5 SiC Power DI-MOSFET Structure

Due to the low diffusion coefficients for dopants in silicon carbide, it was proposed [13] that photoresist masks be used to stagger the P-base and N^+ source ion implantations as illustrated in Fig. 14.12. High-voltage power MOSFETs, called DI-MOSFETs because of the Double-Implant process, were subsequently made using the approach [14].

14.5.1 Blocking Characteristics

The voltage is supported by a depletion region formed on both sides of the P-base/N-drift junction in the forward blocking mode of the SiC planar power MOSFET structure. The maximum blocking voltage occurs when the electric field at the junction becoming equal to the critical electric field for breakdown. The parasitic N^+/P/N bipolar transistor is suppressed by short-circuiting the N^+ source and P-base

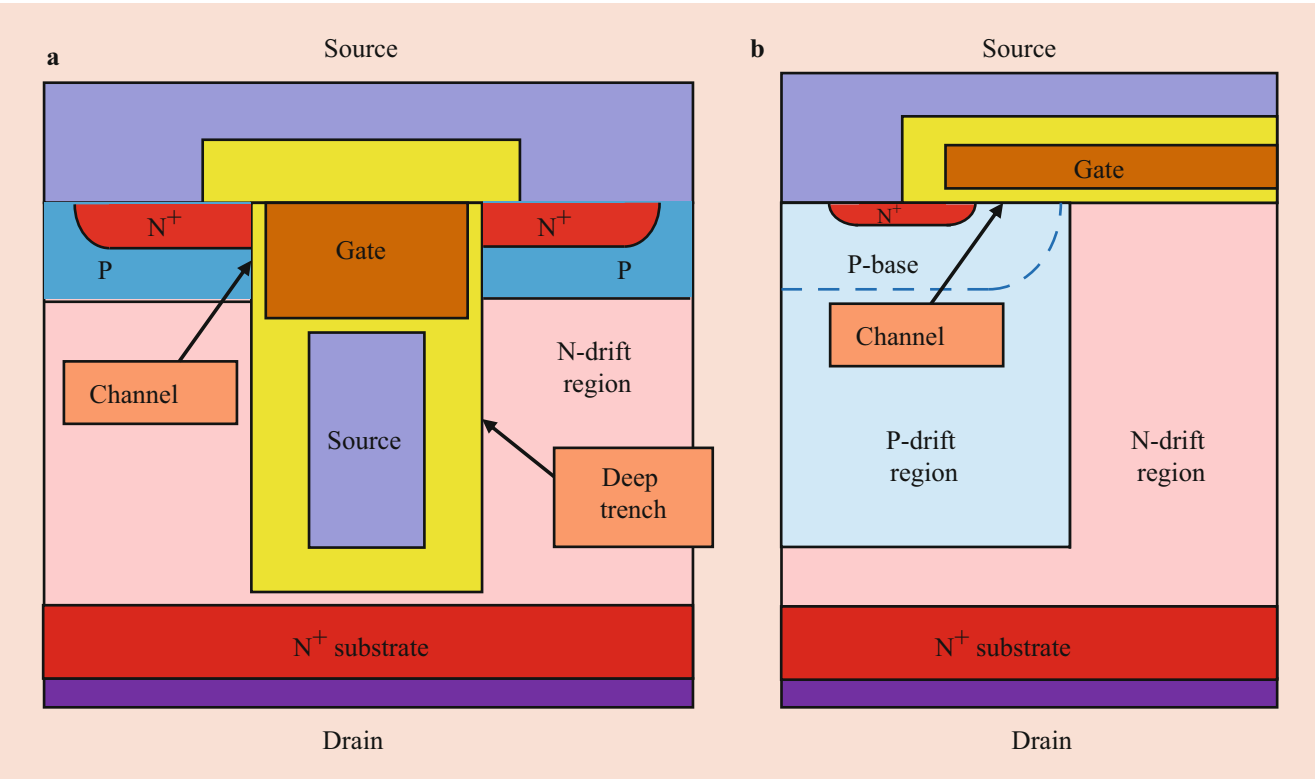

Fig. 14.11 Charge-coupled silicon power MOSFET structures. (**a**) GD-MOSFET structure. (**b**) Superjunction MOSFET structure

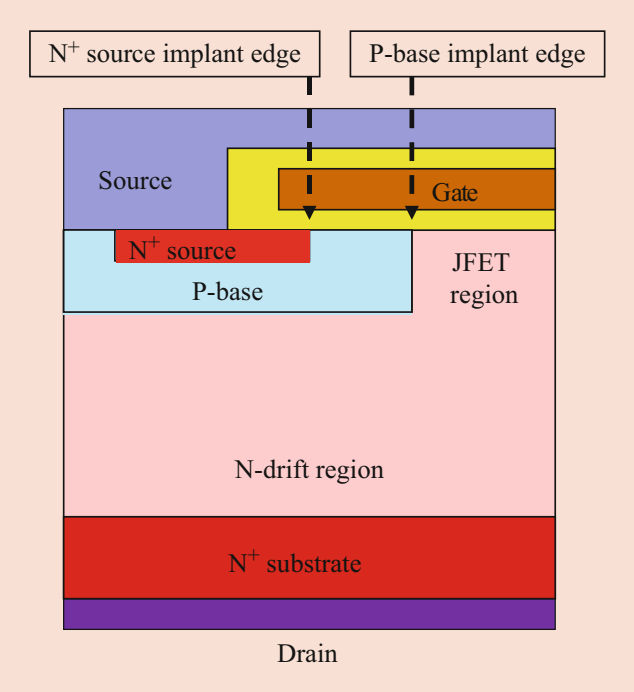

Fig. 14.12 The SiC planar power DI-MOSFET structure

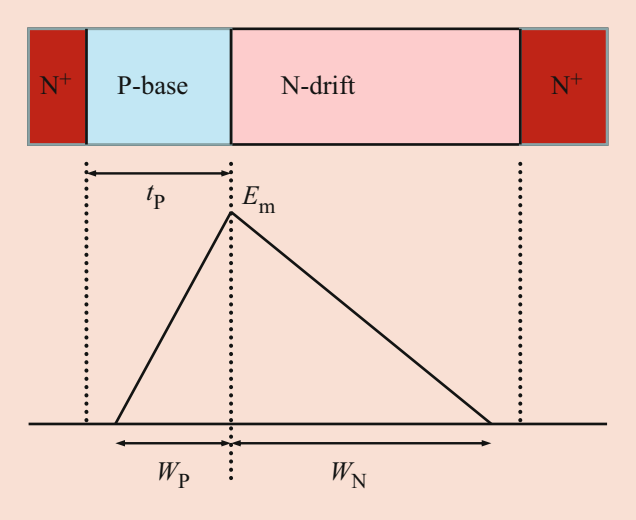

Fig. 14.13 Reach-through problem in a SiC power MOSFET structure

regions using the source metal as shown in Fig. 14.12. In spite of this, the blocking voltage can be compromised by reach-through of the depletion region in the P-base region. The doping concentration and thickness of the P-base region must be sufficient to prevent this problem.

The reach-through problem is worse for SiC devices when compared with silicon devices due to the high doping concentration of their N-type drift region and the higher electric field at the P-N junction [4]. A triangular electric field distribution is shown in Fig. 14.13 for the case of uniform doping on both sides of the junction with the maximum electric field at the P-base/N-drift junction. The depletion width in the P-base is given by

$$W_P = \frac{\varepsilon_S E_m}{qN_A} \tag{14.3}$$

where N_A is the doping concentration of the P-base region. The minimum P-base thickness required to prevent reach-though limited breakdown is obtained when the P-base region is completely depleted with the critical electric field for breakdown at the junction:

$$t_P = \frac{\varepsilon_S E_C}{qN_A} \tag{14.4}$$

where E_C is the critical electric field for breakdown.

The minimum P-base thickness for 4H-SiC power MOSFETs can be compared with that for silicon devices in Fig. 14.14. The thickness for 4H-SiC devices is about six times larger than for silicon for the same P-base doping concentration [4]. This limits the minimum channel length for silicon carbide devices to much larger values than for silicon devices making the channel resistance high. The 10 times lower channel inversion layer mobility observed for silicon carbide makes this problem worse.

A threshold voltage between 1 and 5 V can be achieved in silicon power MOSFETs with typical P-base doping concentration of 1×10^{17} cm^{-3} and gate oxide thickness of 500–1000 angstroms. This allows reducing the channel length to 0.5 μm without reach-through. The P-base doping concentration must be increased to above 4×10^{17} cm^{-3} for 4H-SiC to prevent reach-through with a 0.5 μm P-base thickness resulting in a threshold voltage above 10 V.

In the silicon carbide power MOSFET structure, a very high electric field also develops in the gate oxide under forward blocking conditions. Gausses Law determines the electric field developed in the oxide based up on the electric field at the semiconductor interface:

$$E_{Oxide} = \left(\frac{\varepsilon_{Semi}}{\varepsilon_{Oxide}}\right) \cdot E_{Semi} \tag{14.5}$$

where ε_{Semi} and ε_{Oxide} are the dielectric constants of the semiconductor and oxide and E_{Semi} is the electric field at the semiconductor interface. The electric field in the oxide ($\varepsilon_{Oxide} = 3.85$) is approximately 3-times larger than in the semiconductor for both silicon ($\varepsilon_{Semi} = 11.7$) and silicon carbide ($\varepsilon_{Semi} = 9.7$). The electric field in the oxide does not exceed the reliability limit of about 4×10^6 V/cm because the maximum electric field in the silicon cannot exceed 3×10^5 V/cm due to avalanche breakdown. In contrast, the electric field in the oxide approaches 9×10^6 V/cm when

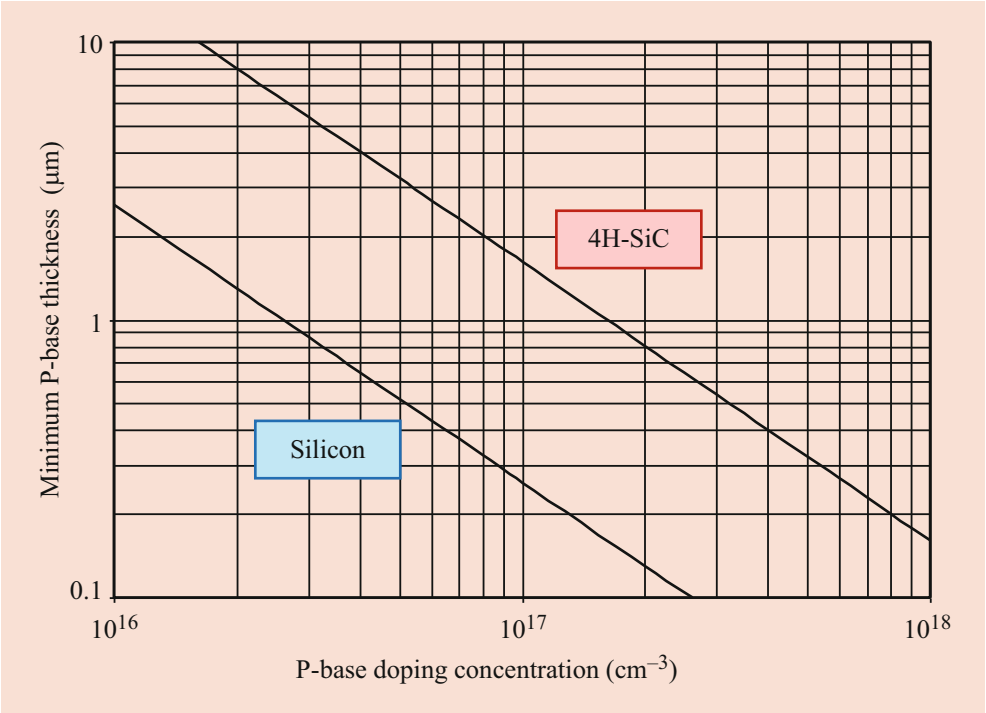

Fig. 14.14 Minimum P-base thickness required to prevent reach-through breakdown in 4H-SiC and Silicon devices

the electric field in 4H-SiC reaches its breakdown strength of 3×10^6 V/cm. This exceeds not only the reliability limit but produces rupture of the oxide leading to catastrophic failure. The electric field in the gate oxide must be carefully examined during the design of silicon carbide MOSFET structures. Innovative SiC power MOSFET structures were proposed [15] that shield the gate oxide from high electric field in the drift region to address this problem.

14.5.2 On-Resistance

On-state current flow occurs in the power MOSFET by forming an inversion layer channel at the surface of the P-base region due to a positive gate bias above the threshold voltage. The shaded area current path in Fig. 14.15 indicates the path for current flow [4]. The current flows from the channel into the JFET region. An accumulation layer above the JFET region distributes electrons into the JFET region. The current then flows uniformly through the JFET region. From the JFET region, the current spreads at a 45 degree angle into the N-drift region. It becomes uniform after a certain depth which depends on the width of the P-base region (s in the figure). The total on-resistance for the planar power MOSFET structure can be calculated by adding all the resistances shown in the figure:

$$R_{on,sp} = R_{CH} + R_A + R_{JFET} + R_D + R_{subs} \qquad (14.6)$$

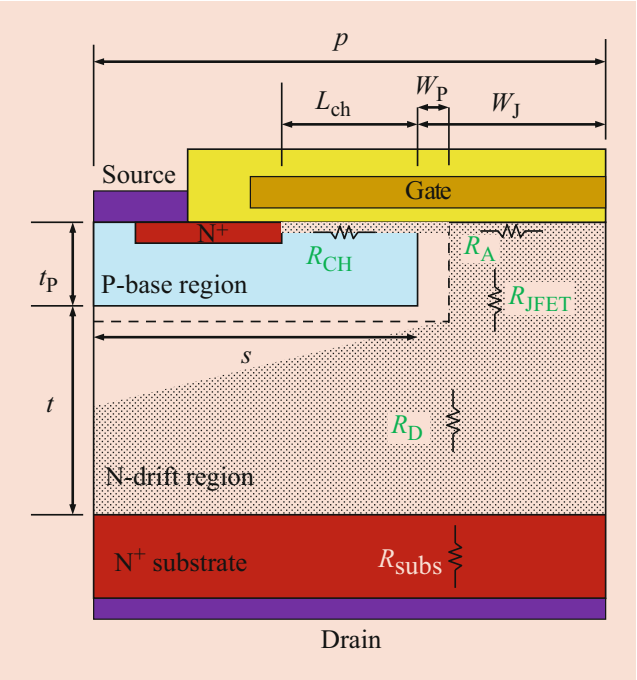

Fig. 14.15 Internal resistances for the planar 4H-SiC power MOSFET

where R_{CH} is the channel resistance, R_A is the accumulation region resistance, R_{JFET} is the resistance of the JFET region, R_D is the resistance of the drift region, and R_{subs} is the resistance of the N^+ substrate. These resistances can be analytically calculated:

(a) The specific channel resistance

$$R_{CH} = \frac{(L_{CH}.p)}{\mu_{inv} C_{ox} (V_G - V_T)} \tag{14.7}$$

where L_{CH} is the channel length as defined in Fig. 14.15, μ_{inv} is the electron inversion layer mobility, C_{ox} is the specific capacitance of the gate oxide, V_G is the applied gate bias, and V_T is the threshold voltage. The specific capacitance is given by

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{14.8}$$

where ε_{ox} is the dielectric constant for the gate oxide and t_{ox} is its thickness.

(b) The specific accumulation layer resistance

$$R_A = \frac{K (W_J - W_P) p}{\mu_a C_{ox} (V_G - V_{TA})} \tag{14.9}$$

where W_P is the P-base/N-JFET junction zero-bias depletion width, μ_a is the electron accumulation layer mobility and V_{TA} is the accumulation threshold voltage. The factor K is 0.1–0.3 for SiC power devices because of the low accumulation layer mobility and the low JFET region resistance. The JFET region doping concentration ($N_{D,JFET}$) is increased above the drift region doping concentration. The depletion width is

$$W_P = \sqrt{\frac{2\varepsilon_S V_{biP}}{qN_{D,JFET}}} \tag{14.10}$$

where V_{biP} is the built-in potential (typically 3.3 V) for 4H-SiC.

(c) The specific JFET region resistance

$$R_{JFET} = \rho_D \cdot t_P \left(\frac{p}{W_J - W_P} \right) \tag{14.11}$$

where t_p is the depth of the P-base region.

(d) The drift region spreading resistance

$$R_D = \rho_D \cdot p \cdot \ln \left(\frac{p}{W_J - W_P} \right) + \rho_D \cdot (t - s - W_P) \tag{14.12}$$

where t is the thickness of the drift region below the P-base region and s is the width of the P-base region.

(e) The N^+ substrate resistance

$$R_{subs} = \rho_{subs} \cdot t_{subs} \tag{14.13}$$

where ρ_{subs} and t_{subs} are the resistivity and thickness of the substrate. A typical value for the N^+ substrate resistivity for 4H-SiC is 0.020 Ω-cm and its thickness if typically 350 μm leading to a contribution of 7×10^{-4} Ω-cm^2.

The various components of the specific on-resistances for a 1.2 kV rated 4H-SiC planar MOSFET with a drift region doping concentration of 1×10^{16} cm^{-3} and thickness of 10 μm were modeled using the above equations with a gate oxide thickness of 0.1 μm. An accumulation channel mobility of twice the inversion layer mobility was assumed. The P-base had a depth of 1 μm. The gate drive voltage (V_G) was assumed to be 20 V above the threshold voltage.

The on-resistance components are shown in Fig. 14.16 for the case of a channel mobility of 100 cm^2/V-s. An inversion layer mobility above 100 cm^2/V-s was first experimentally observed [16] in 1998. The drift region resistance is dominant for this large channel mobility even for a channel length of 2 μm. A total specific on-resistance of 2.7 mΩ-cm^2 is obtained for a channel length of 1 μm. This value is ten times the ideal specific on-resistance. A channel mobility of 15–20 cm^2/Vs has been reported for modern commercially available 4H-SiC planar power MOSFETs. They have a specific on-resistance of 3.5–4.0 mΩ-cm^2 by reducing the channel length to 0.5 μm and using a gate oxide thickness of 500 angstroms.

The JFET width in SiC planar power MOSFETs must be optimized to achieve a low specific on-resistance while reducing the electric field in the gate oxide. The optimization of the JFET width is illustrated in Fig. 14.17. The specific on-resistance is very large when the JFET width is below 0.8 μm because the zero bias depletion width is 0.6 μm. When the JFET width is increased, its resistance decreases rapidly while the increase in cell pitch produces an increase in the channel specific resistance. The minimum specific on-resistance is observed at a JFET width of 1 μm. The electric field in the gate oxide under forward blocking mode must be monitored when optimizing the JFET width [3]. The electric field in the gate oxide is sufficiently low at the JFET width of 1 μm for reliable operation of the devices.

The channel mobility has a large impact on the specific on-resistance of lower breakdown voltage SiC planar MOSFETs. This is demonstrated in Fig. 14.18 by modelling devices with a JFET doping concentration of 1×10^{16} cm^{-3}. The other cell parameters are P-base depth of 1 μm, gate oxide thickness of 0.05 μm, accumulation layer mobility of 200 cm^2/V-s, and channel length of 1 μm. A gate bias voltage of 10 V above the threshold voltage was assumed here. For the case of a channel mobility of 100 cm^2/Vs, the specific on-resistance becomes nearly equal to the ideal value when the breakdown voltage exceeds 5000 V. However, the channel

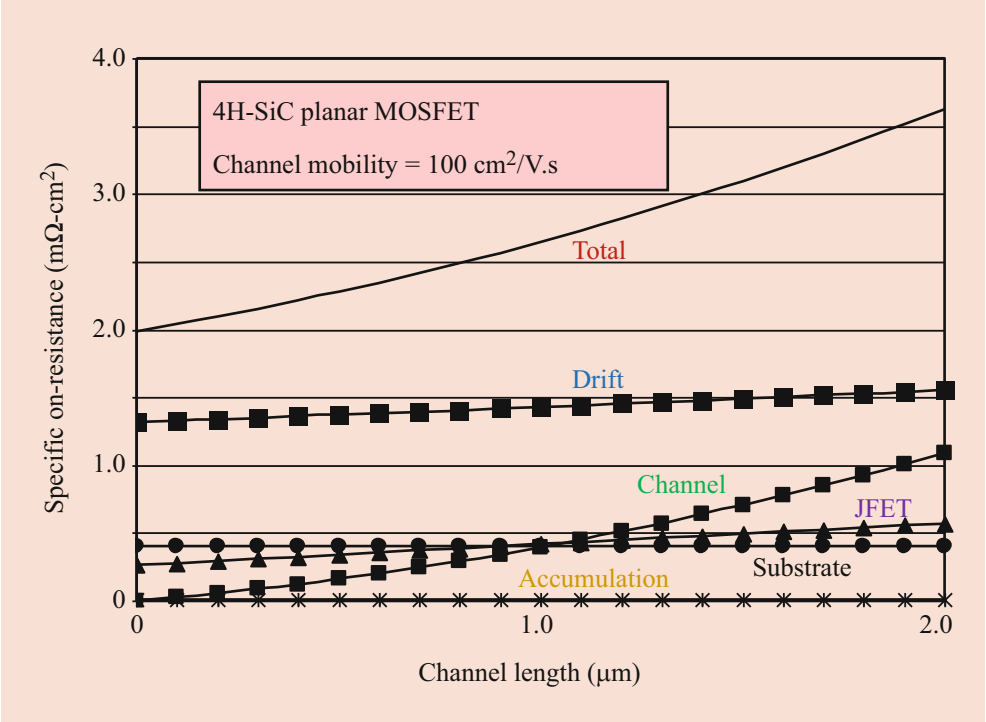

Fig. 14.16 Components of On-Resistance for 1.2 kV rated 4H-SiC Planar MOSFETs inversion layer mobility = 100 cm^2/v-s

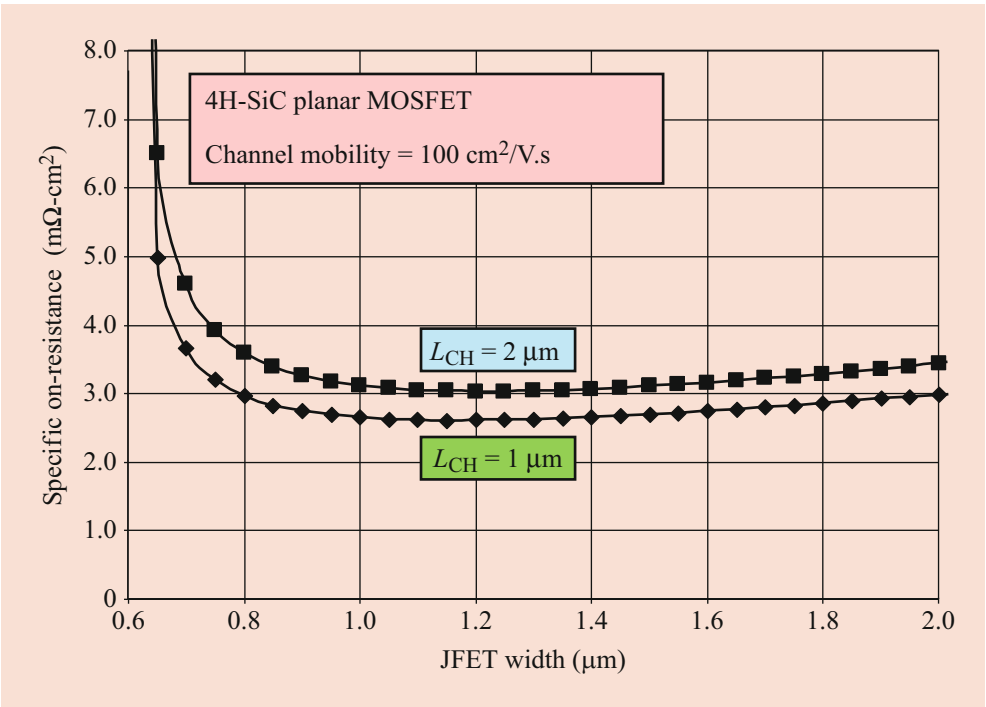

Fig. 14.17 Specific on-resistance for 1.2 kV 4H-SiC planar MOSFET as a function of JFET width: inversion layer mobility = 100 cm^2/v-s

resistance limits the performance of SiC planar MOSFETs when the breakdown voltage is less than 1000 V. The performance is degraded even at large breakdown voltages if the channel mobility is reduced to 10 cm^2/V-s. 4H-SiC planar MOSFETs can surpass the performance of silicon devices by several orders of magnitude at breakdown voltages above 1000 V if a channel mobility of at least 10 cm^2/V-s is achieved.

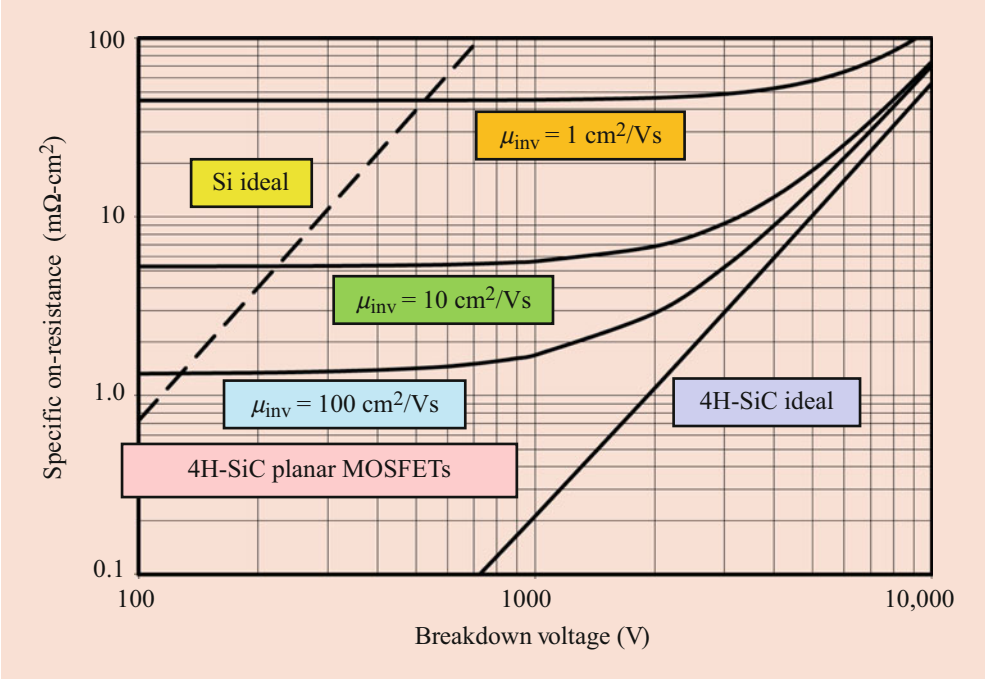

Fig. 14.18 Specific on-resistance for 4H-SiC planar MOSFETs with three cases of channel mobility

14.5.3 Threshold Voltage

A minimum threshold voltage above 1 V is required for power MOSFETs for most applications to prevent inadvertent turn-on during voltage spikes in the circuit. However, a high threshold voltage increases the channel resistance. Most high voltage power electronic circuits use a gate drive voltage of 15 V. The threshold voltage should therefore be kept at 2–3 V. The threshold voltage is defined as the gate bias for the on-set of *strong inversion* [17]:

$$V_{TH} = \frac{\sqrt{4\varepsilon_S kTN_A \ln(N_A/n_i)}}{C_{ox}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) \quad (14.14)$$

where N_A is the doping concentration of the P-base region, k is Boltzmann's constant, and T is the absolute temperature. Positive fixed oxide charge shifts the threshold voltage in the negative direction:

$$\Delta V_{TH} = \frac{Q_F}{C_{ox}} \quad (14.15)$$

Heavily doped N-type polysilicon gate electrode produces a negative shift of the threshold voltage by 1 V [3].

The threshold voltage for 4H-SiC planar MOSFETs calculated using Eq. (14.15) is provided in Fig. 14.19 for a gate oxide thickness of 0.1 μm. The values for a silicon device with the same gate oxide thickness are shown in this figure for comparison. A threshold voltage of 3 V is obtained for a P-base doping concentration of 1×10^{17} cm^{-3} for silicon devices. Silicon power MOSFETs with channel lengths of 0.5 μm operate without reach-through problems. However, a P-base doping concentration of 3×10^{17} cm^{-3} must be used for 4H-SiC (see Fig. 14.14) to prevent reach-through breakdown. The threshold voltage for the 4H-SiC MOSFET approaches 20 V for this doping concentration. The conventional power MOSFET structure shown in Fig. 14.12 cannot be used silicon carbide power MOSFETs.

14.5.4 Reliability

Power MOSFETs are prone to shift in the threshold voltage due to the injection of electrons into the gate oxide if they gain sufficient energy to overcome the potential barrier between the semiconductor and the oxide. The energy band offsets with silicon dioxide for the case of silicon and SiC are shown in Fig. 14.20. The band offset between the conduction band edges is much smaller for SiC than for silicon.

The band diagram in the on-state for the 4H-SiC MOS structure with polysilicon gate is shown in Fig. 14.21 for a positive bias applied to the gate. A narrow barrier is formed at the SiC-SiO_2 interface allowing the tunneling of electrons from SiC into the oxide. Current flow due to Fowler-Nordheim tunneling injects electrons into the oxide. This has been in measurements reported on 6H-SiC [18] and 4H-SiC [19] MOS-capacitors. The trapping of electrons in the gate oxide causes threshold voltage shifts violating reliability requirements [20]. Based up on time-dependent

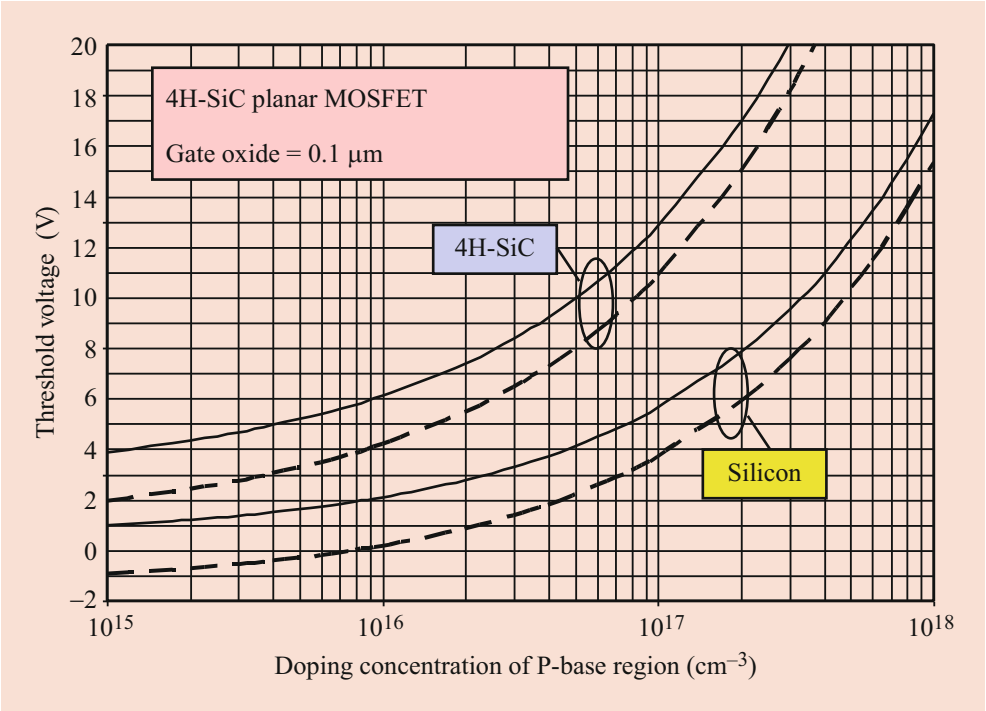

Fig. 14.19 Threshold voltages for 4H-SiC planar MOSFETs (solid lines). Contribution of N^+ polysilicon gate and 2×10^{11} cm^{-2} oxide fixed charge is shown by dashed lines

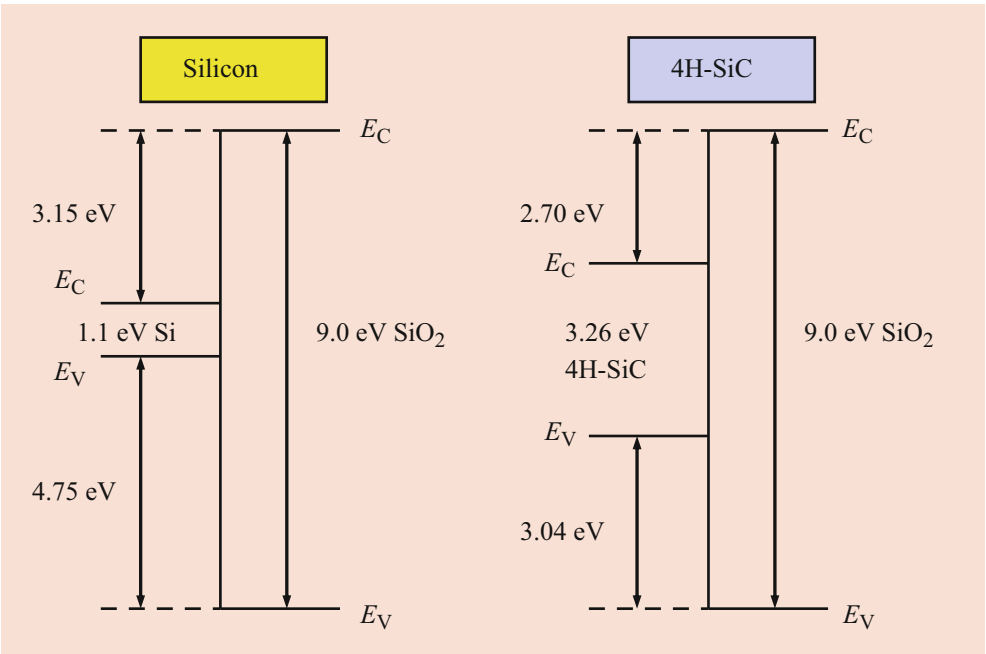

Fig. 14.20 Band offsets for Si and SiC with SiO_2

dielectric breakdown studies [21], a 100-year mean-time-to-failure (MTTF) was projected at 175 °C assuming a gate oxide electric field of below 3 MV/cm. Low gate oxide electric field under blocking conditions can be achieved by using the shielded planar power MOSFET structure discussed in the next section.

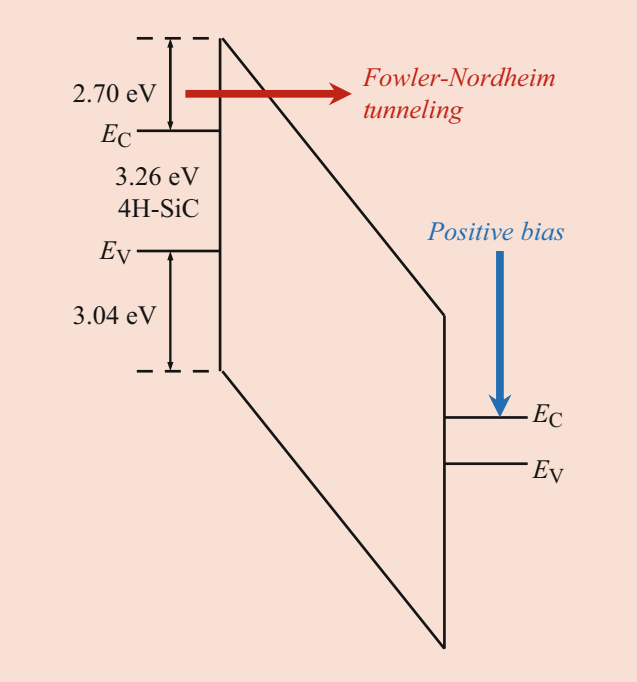

Fig. 14.21 Polysilicon/oxide/4H-SiC band diagram under on-state gate bias

14.6 Shielded SiC Planar Power MOSFET Structure

The conventional silicon planar power DMOSFET structure cannot be used to make SiC devices because of (a) a reach-through problem, (b) a high threshold voltage, (c) a high gate oxide electric field, and (d) a low channel mobility. These problems were solved with the shielded planar-gate structure proposed [15] at NCSU in 1995.

14.6.1 Device Structures

The shielded SiC planar-gate power MOSFET structure with inversion and accumulation channels are shown in Fig. 14.22. The P^+ shielding region extends under both the N^+ source region and the base region. The JFET region formed between the P^+ shielding regions is optimized to minimize the specific on-resistance. The electric field in the gate oxide is reduced by the potential barrier formed in the JFET region by the P^+ shielding regions. The reduced electric field near the surface also prevents lateral reach-through of the base region. This allows reducing the base doping levels to achieve a good threshold voltage of 2–3 V.

Enhancement-mode operation is achieved in the accumulation mode structure by choosing the doping and thickness of the N-base region so that it is completely depleted by the built-in potential of the P+/N junction at zero gate bias [22]. This is fundamentally different than in buried channel MOS devices [23] where an un-depleted N-type channel region allows current flow at zero gate bias resulting in a depletion-mode device which is unacceptable for power electronics applications. On-state state current flow occurs in both structures when a positive bias is applied to the gate with either an inversion or accumulation layer channel. The accumulation-mode structure has a smaller specific on-resistance because of a larger accumulation layer electron mobility.

14.6.2 Gate Oxide Screening

The width of the JFET region determines the highest electric field developed in the gate oxide for both of the shielded structures. The results of numerical simulations [22] to extract the electric field in SiC below the gate oxide are shown in Fig. 14.23 for a drift region doping concentration of 1×10^{16} cm^{-3}. A JFET width of 1.5 μm reduces the SiC electric field to 1.5 MV/cm which keeps the oxide electric field within reliability requirements. A JFET width of 1.5 μm leads to a low specific on-resistance because the zero-bias depletion width is 0.6 μm.

14.6.3 Threshold Voltage

A model for the threshold voltage of accumulation-mode MOSFETs can be developed [24] using the electric field profile shown in Fig. 14.24. The electric field in the SiC and oxide are.

$$E_1 = \frac{V_{bi}}{W_N} - \frac{qN_D W_N}{2\varepsilon_S} \tag{14.16}$$

$$E_2 = \frac{V_{bi}}{W_N} + \frac{qN_D W_N}{2\varepsilon_S} \tag{14.17}$$

$$E_{ox} = \frac{\varepsilon_S}{\varepsilon_{ox}} E_1 \tag{14.18}$$

The threshold voltage is obtained by calculating the area under the electric field profile:

$$V_{TH} = \varphi_{MS} + \left(\frac{\varepsilon_S V_{bi}}{\varepsilon_{ox} W_N} - \frac{qN_D W_N}{2\varepsilon_{ox}} \right) \cdot t_{ox} \tag{14.19}$$

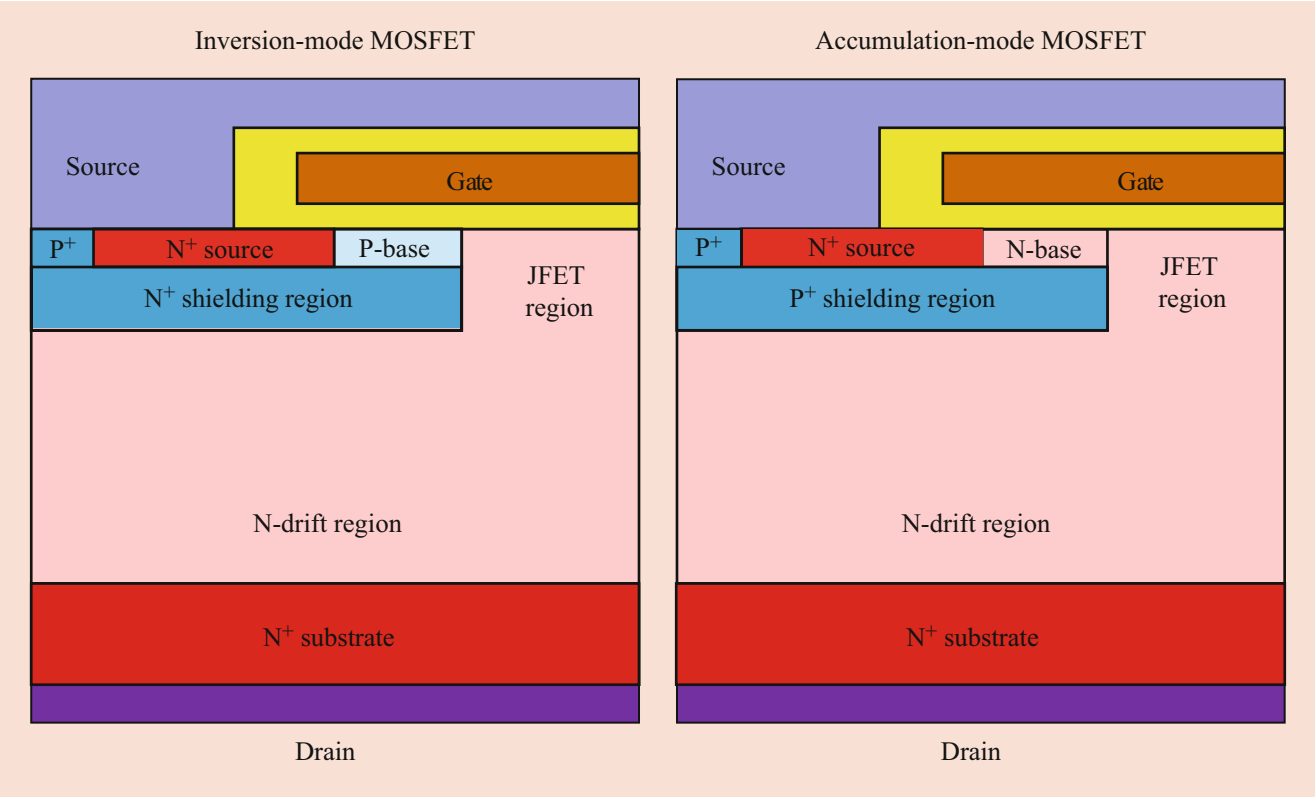

Fig. 14.22 SiC power MOSFET structures with shielding regions

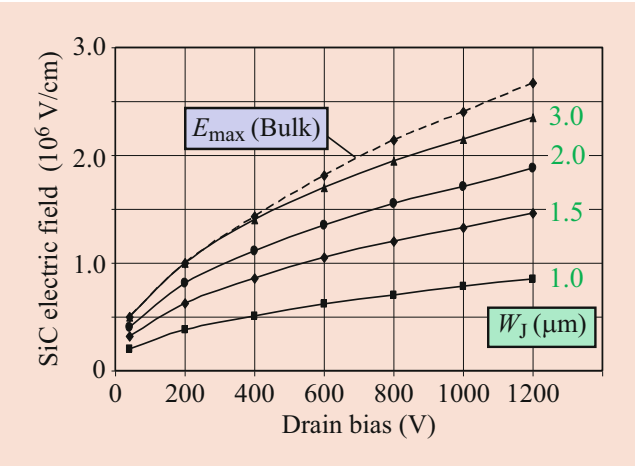

Fig. 14.23 Electric field in the SiC at the gate oxide interface for the planar 4H-SiC shielded accumulation-mode MOSFET structure

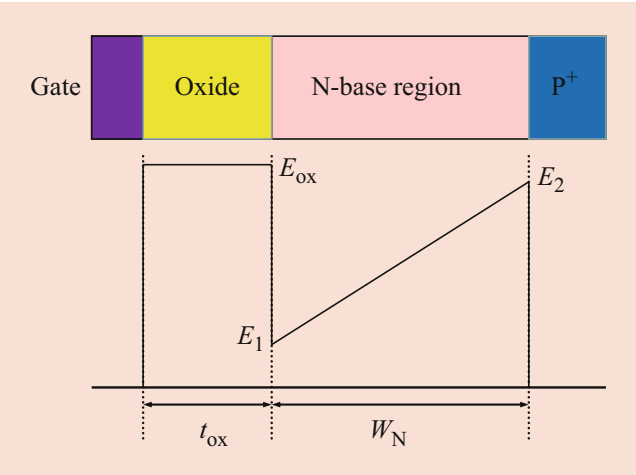

Fig. 14.24 Accumulation-mode MOSFET structure electric field distribution in the gate region

and taking into account the work function difference between the gate material and the lightly doped N-Base region.

The threshold voltages calculated for 4H-SiC accumulation-channel MOSFETs are shown in Fig. 14.25 for a gate oxide thickness of 0.05 μm, N-base thickness of 0.2 μm, and a gate-semiconductor work-function difference of 1 V [22]. The threshold voltages for the conventional inversion-channel 4H-SiC MOSFET are included in the figure for comparison. The threshold voltage for the accumulation-channel case decreases with increasing N-base doping concentration. Lower threshold voltages can be achieved with the accumulation channel than in the inversion-channel structures. A threshold voltage of 2.8 V is obtained for the accumulation-channel device with a N-base doping

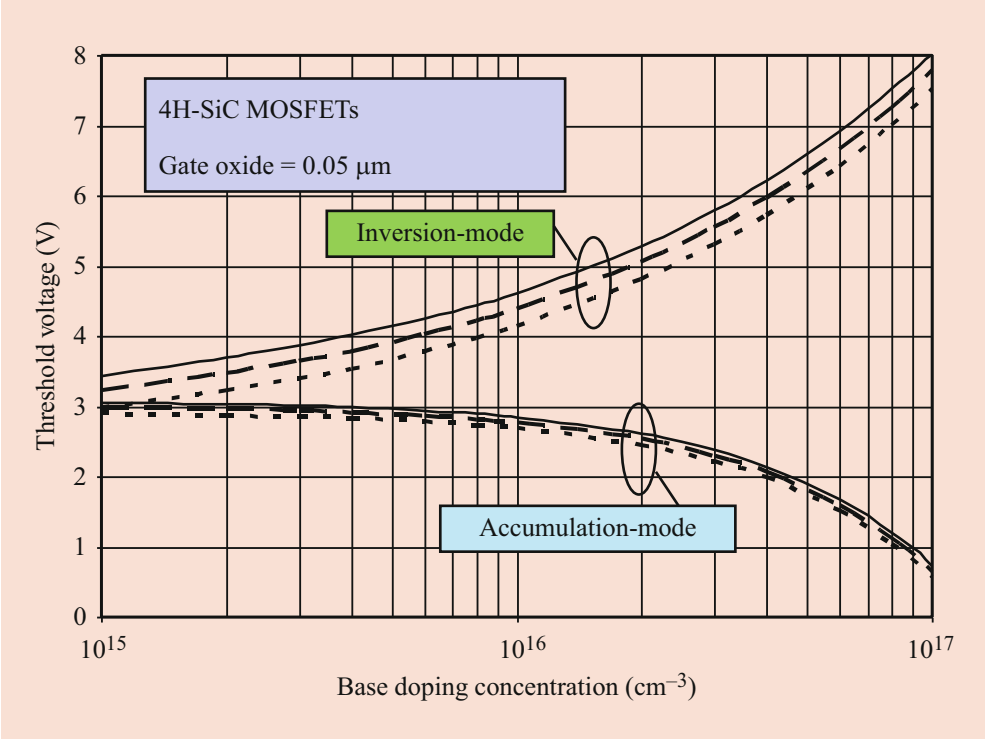

Fig. 14.25 4H-SiC accumulation-mode MOSFETs threshold voltage (Solid line: 300°K; Dash line: 400°K; Dotted line: 500°K)

concentration of 1×10^{16} cm^{-3}. The threshold voltage will be reduced to 2 V due to typical fixed oxide charge of 10^{11} cm^{-2}. This model has been verified by numerical simulations [25].

14.6.4 Channel Mobility

Obtaining a high channel mobility in SiC power MOSFETs was identified as an important goal during the development of these devices [26]. The interface quality was significantly improved for 6H-SiC by anneal thermally grown oxide in a NO ambient [27] producing a peak inversion layer mobility of 70 cm^2/Vs. In contrast, the inversion layer mobility for 4H-SiC was found [28, 29] to be less than 1 cm^2/Vs due to trapping of electrons [30]. In 1998, NCSU reported [31] record high inversion layer mobility of 165 cm^2/Vs using deposited oxides on 4H-SiC. The key process step required for obtaining a high inversion layer mobility was found to be a wet oxide anneal [32]. The first evidence of phonon scattering limited inversion layer mobility was obtained in this work. The results were reproduced by the NCSU sponsors [33] and other research groups [34]. It has been reported that the channel mobility is inversely proportional to the interface state density. A significant reduction in the interface state density has been accomplished by performing annealing at 1175 °C in a nitric oxide (NO) ambient for 2 h [24, 35–37].

4H-SiC power MOSFETs are manufactured with ion-implanted P-base regions. Damage caused by the ion implantation could reduce the channel mobility. N-channel lateral MOSFETs have been fabricated on aluminum implanted layers in 4H-SiC [38] with a doping concentration of 1×10^{17} cm^{-3}. A peak inversion layer mobility of 100 cm^2/V-s was observed.

In 1998, a high accumulation layer mobility of 120 cm^2/Vs was observed by NCSU [39] for 4H-SiC using deposited oxides. A peak accumulation mobility of 140 cm^2/V-s was reported in 2001 with thermally grown oxide on nitrogen implanted regions [40]. The accumulation layer mobility was measured in 2001 using the Hall bar structure [41] to eliminate the impact of charge trapping. The accumulation mobility decreased from 350 cm^2/V-s in weak accumulation to 200 cm^2/V-s in strong accumulation compared with an effective mobility of only 3–5 cm^2/V-s due to trapping of electrons.

14.6.5 On-Resistance

The current path in the on-state for the shielded accumulation-channel planar SiC power MOSFET is similar to that shown in Fig. 14.15. The resistance components for the shielded planar MOSFET structures can be calculated by using the equations in Sect. 14.5.2.

The specific channel resistance for the shielded inversion-channel structure is

$$R_{CH} = \frac{(L_{CH} \cdot p)}{\mu_{inv} C_{ox} (V_G - V_T)} \tag{14.20}$$

where p is the cell pitch, L_{CH} is the channel length, μ_{inv} is the inversion layer mobility for electrons, C_{ox} is the specific capacitance of the gate oxide, V_G is the gate bias, and V_T is the threshold voltage. The specific channel resistance for the shielded accumulation-channel structure is.

$$R_{CH} = \frac{(L_{CH} \cdot p)}{\mu_a C_{ox} (V_G - V_T)} \tag{14.21}$$

where μ_a is the accumulation layer mobility for electrons. Larger accumulation layer mobility than inversion layer mobility has been experimentally observed in silicon carbide. The threshold voltage for creating an accumulation layer is smaller than for creating an inversion layer. These factors reduce the channel resistance contribution in the accumulation channel device.

A comparison between the inversion and accumulation channel devices can be made while keeping all other parameters the same. The specific on-resistance for the shielded planar 4H-SiC MOSFETs with various breakdown voltages is shown in Fig. 14.26 based up on (a) gate oxide thickness of 0.05 μm; (b) "a" value of 1 μm; (c) P^+ region depth of 1 μm; (d) gate drive voltage (V_G – V_T) of 10 V; (e) channel length of 1 μm; (f) JFET width (W_J) of 1 μm; (g) cell pitch of 3 μm; and (h) N^+ substrate resistance of 0.04 mΩ-cm^2. It can be seen in Fig. 14.26 that device specific on-resistance approaches the ideal value when the breakdown voltage exceeds 5000 V for both structures because the drift region resistance becomes dominant. The channel contribution becomes dominant when the breakdown voltage falls below 1000 V. The accumulation-channel device has a specific on-resistance of 1.5 mΩ-cm^2 compared with 4 mΩ-cm^2 for the inversion channel device at a breakdown voltage of 1000-V. These values can be reduced by decreasing the channel length to 0.5 μm.

14.6.6 Experimental Results

Experimental results for 4H-SiC inversion-channel DI-MOSFETs were reported [42] in 2001 using 25 μm thick epitaxial layers with doping concentration of 3×10^{15} cm^{-3}. The 2000 V devices had a large-specific on-resistance (55 mΩ-cm^2) due to an inversion layer mobility of only 14 cm^2/Vs. 10 kV inversion-channel DI-MOSFET devices with specific on-resistance of 236 mΩ-cm^2 were reported [43] in 2003. Significantly better 10-kV 4H-SiC planar inversion-channel power MOSFETs with a specific on-resistance of 123 mΩ-cm^2 were then reported in 2004 by using a drift region with doping concentration of 8×10^{14} cm^{-3} and thickness of 85 μm [44].

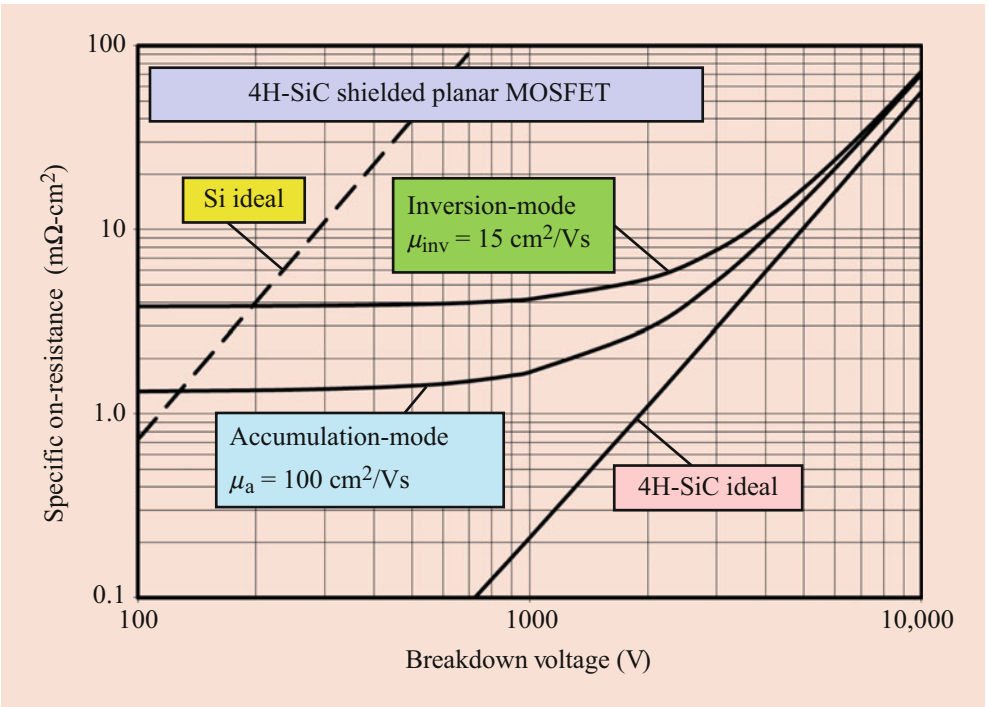

Fig. 14.26 Specific on-resistance for the shielded planar-gate 4H-SiC MOSFETs

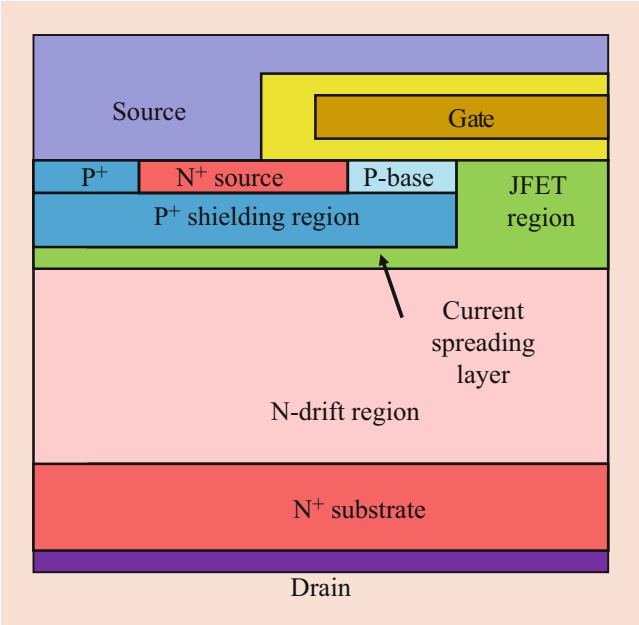

Fig. 14.27 4H-SiC MOSFET with current spreading layer

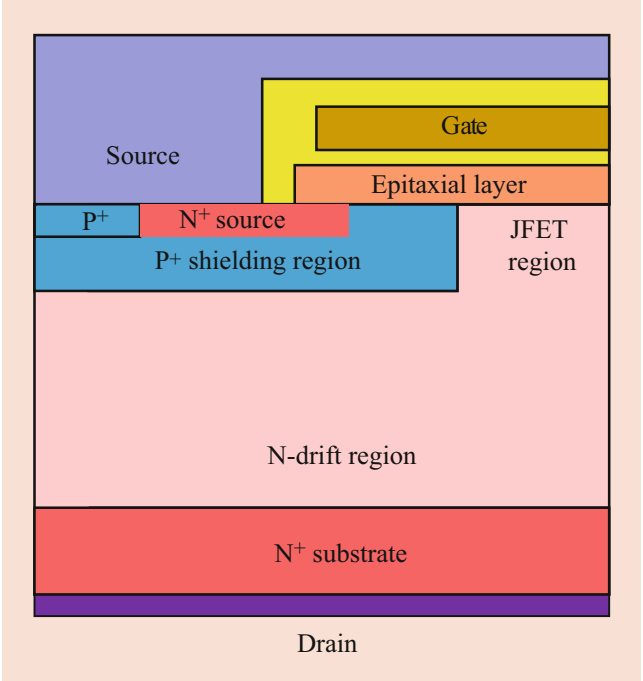

Fig. 14.28 4H-SiC planar-gate ACCUFET structure using an epitaxial N-base region

A self-aligned implant process for planar 4H-SiC MOSFETs was demonstrated in 2004 [45, 46]. A sidewall spacer that serves as an implant mask was formed by the oxidation of a sacrificial polysilicon layer to achieve a channel length of less than 0.5 μm. 2 kV planar 4H-SiC inversion-mode MOSFETs were reported with a specific on-resistance of 27 mΩ-cm^2.

A 1-kV inversion-channel DI-MOSFET structure with current spreading layer (CSL) as shown in Fig. 14.27 was reported in 2007 [47]. The CSL with optimum doping concentration of 1×10^{17} cm^{-3} can be epitaxially grown on top of the n-type drift layer. A catastrophic drop in breakdown voltage occurs when the CSL doping concentration exceeds 2×10^{17} cm^{-3}. Devices with specific on-resistance of 6.95 mΩ-cm^2 were achieved using a self-aligned process to reduce the channel length to 0.3 μm.

Large-area (0.45 cm × 0.45 cm chips with 0.15 cm^2 active area) planar SiC inversion-channel power MOSFETs could be fabricated in 2010 on 3 inch diameter wafers with blocking voltage of 1200 V [48]. The devices can handle 40 A in the on-state with a specific on-resistance of 7.1 mΩ-cm^2. Their performance is limited by the channel resistance.

1.5 kV 4H-SiC planar inversion-channel power MOSFETs were reported [49] in 2011 with a specific on-resistance of 3.7 mΩ-cm^2. A self-aligned implant process was used to achieve a channel length of 0.5 μm. Improved high-current devices with blocking voltage of 1600 V had a specific on-resistance of 7 mΩ-cm^2. 1.6 kV devices with a chip area of 0.56 cm^2 (active area of 0.40 cm^2) were reported [50] in 2013 to allow handling a drain current of 150 A. Much smaller high temperature switching losses were confirmed when compared with silicon IGBTs. In 2014, 1.7 kV 4H-SiC planar inversion-channel power MOSFETs were reported [51] with specific on-resistance of 5.5 mΩ-cm^2.

The first planar shielded accumulation-mode MOSFET structure were fabricated [52] at PSRC in 1997 using 6H-SiC using a drift region with 1×10^{16} cm^{-3} doping concentration and 10 μm thickness. The un-terminated devices had a breakdown voltage of 350 V although the epi-layer was designed to support 1500 V. A specific on-resistance of 18 mΩ-cm^2 was measured at a gate bias of only 5 V for a structure with cell width of 21 μm, channel length of 2.5 μm, and JFET width of 4 μm. The design of the 6H-SiC ACCUFET was analyzed [53] in 1999. The optimization of the JFET width to minimize the specific on-resistance while reducing the gate oxide electric field was explained in this work.

A 4H-SiC ACCUFET structure, shown in Fig. 14.28, was reported [54] in 2006 with the N-base region created by an N-type epitaxially layer. The threshold voltage was near zero volts. A specific on-resistance of 5 mΩ-cm^2 was reported at a gate bias of 20 V.

A 10 kV 4H-SiC ACCUFETs was reported in 2008 with drift layer doping concentration of 5×10^{14} cm^{-3} and 100 μm thickness and the N-base region formed with a 0.1 μm thick epitaxial layer [55, 56]. The 10 kV breakdown voltage was achieved with a three-zone, 750 μm wide, JTE edge termination. The measured specific on-resistance (170 mΩ-cm^2) was within 3-times the ideal case.

The 1 kV, 40 A 4H-SiC ACCUFET devices with the structure shown in Fig. 14.28 were reported in 2010 [57]. A specific on-resistance of 3.5 mΩ-cm^2 was achieved. The devices were evaluated at 30 kHz for induction cook-top applications. Their switching loss was only 5 W compared with 19 W for the silicon IGBT.

14.7 Silicon Carbide Power MOSFETs with Improved High-Frequency Performance

In order to maximize the benefits of replacing silicon IGBTs with SiC power MOSFETs, it is necessary to increase the circuit operating frequency to reduce the size and cost of passive elements. SiC power MOSFETs must be optimized to reduce their switching losses to obtain good higher frequency performance. This can be achieved by reducing the reverse transfer capacitance (C_{GD}) with innovations in the gate structure. Several device structures that produce a significantly improved (smaller) high-frequency figures-of-merit (HFFOM), defined by [R_{on}*C_{GD}] and [R_{on}*Q_{GD}], are discussed in this section.

A P^+ diverter region connected to the source electrode was incorporated in the 4H-SiC planar power MOSFET structure (called the Central Implant or CI-MOSFET), as shown in Fig. 14.29, in 2015 [58]. Additional process steps are required to add the P^+ diverter region. The P^+ diverter increases the specific on-resistance due to a JFET formed between it and the P-base region. Its impact can be mitigated by increasing the doping concentration in the JFET region. The gate-drain capacitance and reverse transfer gate charge were reduced by a factor of 3 times with this approach.

Two alternate SiC planar-gate power MOSFET structures with improved high-frequency performance are shown in Fig. 14.30. The polysilicon gate has an opening in the middle of the gate electrode in the Split-Gate (SG) MOSFET structure. The fabrication process for this structure is identical to conventional SiC planar-gate power MOSFET. Its measured HFFOM [R_{on}*C_{GD}] was experimentally verified to be 1.3-times smaller, while its HFFOM [R_{on}*Q_{GD}] was 2.4-times smaller than for the conventional MOSFET structure [59].

The P^+ shielding region is extended beyond the edge of the gate electrode in the Buffered-Gate (BG) MOSFET structure, as illustrated in Fig. 14.30. A second JFET region (JFET2) with higher doping concentration must be included to prevent complete depletion of the N-type region above the P^+ shielding region. The experimentally measured HFFOM [R_{on}*C_{GD}] for the 1.2 kV rated BG-MOSFET was 3.6-times smaller, and its HFFOM [R_{on}*Q_{GD}] was 4.0-times smaller than the conventional MOSFET structure [60].

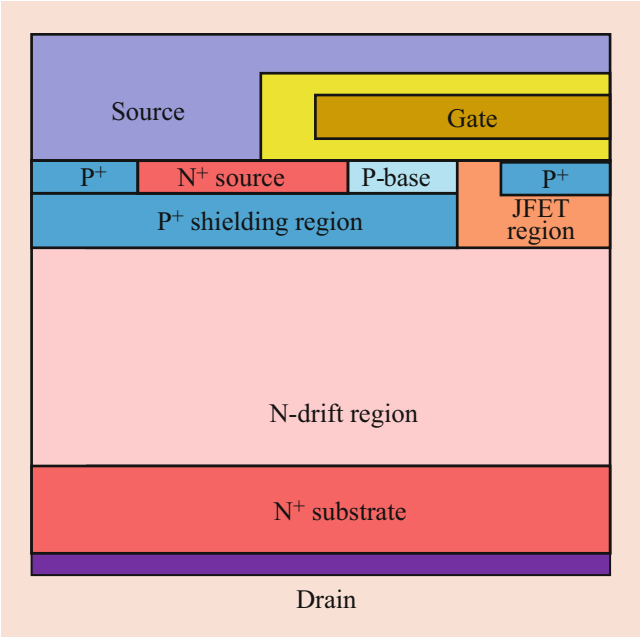

Fig. 14.29 4H-SiC planar-gate MOSFET structure with P^+ diverter region

14.8 SiC Power MOSFET Body-Diode

The body diode in the power MOSFET structure can be used as an anti-parallel diode in power circuits [4]. The body diode is a P-i-N rectifier operating under high-level injection in the on-state. The on-state voltage drop increased [61] after the body diode was turned-on for 1 h for the 10-kV SiC power MOSFET devices. The generation of stacking faults at basal-plane-dislocations (BPDs) due to the release of recombination energy of electrons and holes in the epitaxial layer was discovered as the reason. The on-resistance of the MOSFET was also observed to increase due to mobility degradation by the additional scattering at the stacking faults.

This body diode stability problem is reduced for lower breakdown voltage devices. This has been demonstrated [62] by performing tests on 1200-V 4H-SiC power MOSFETs. An increase by 0.8% for the body diode on-state voltage drop and a 5.4% increase in the on-resistance were observed for 1.2 kV devices after the conduction of the body diode for 1000 hours.

Although stable operation of the body diode in the SiC power MOSFETs may be possible with improved epitaxial layer quality, it has a large on-state voltage drop of 4–5 V. In addition, the injection of minority carriers during current conduction through the body diode generates a stored charge in the drift layer. This stored charge produces a reverse recovery current during operation in typical hard switched inverter circuits used for motor drives or solar PV converters. It has been found that a significant (~50%) increase in turn-on losses is observed in the companion power MOSFETs in

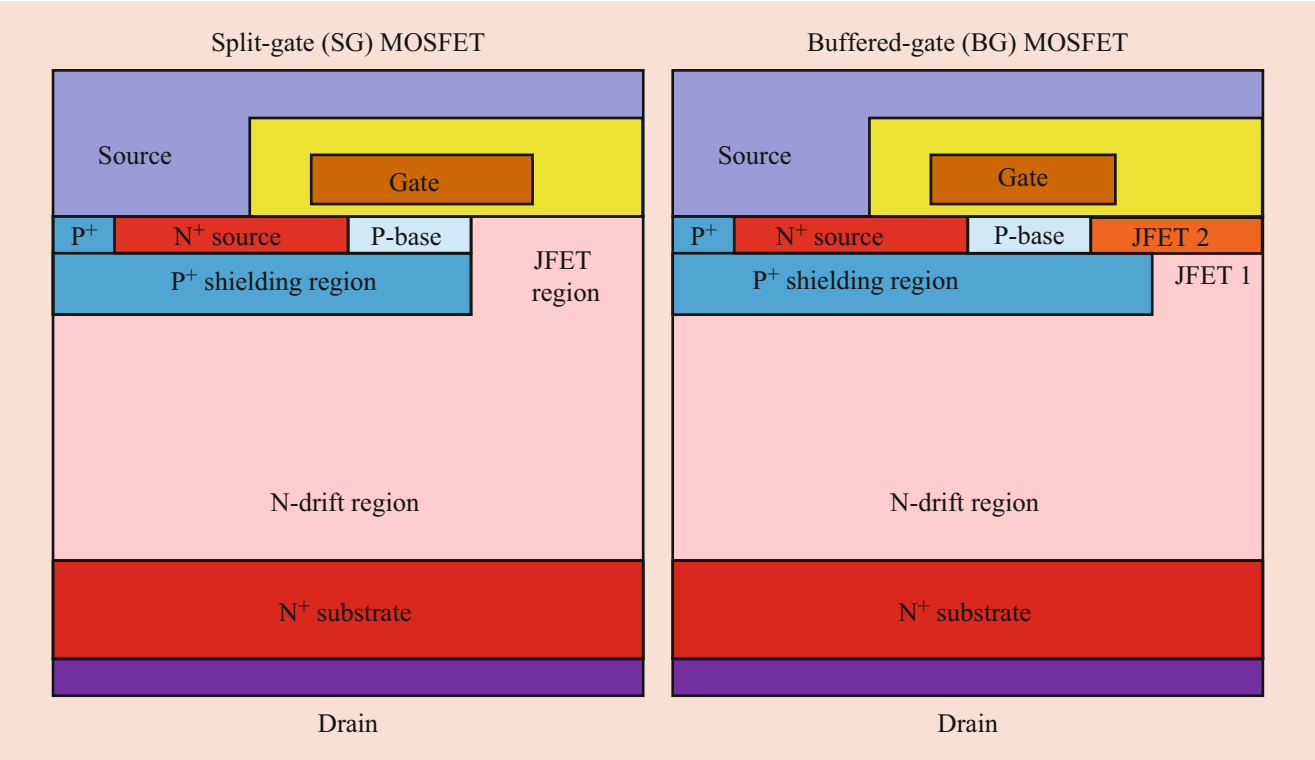

Fig. 14.30 SiC power MOSFETs with improved high frequency operation

the H-bridge inverter at elevated (150 °C) temperatures due to the reverse recovery current in the body diode [63]. The turn-on switching losses can be reduced by using the JBSFET structure discussed in the next section.

14.9 Silicon Carbide Power JBSFETs

Power transistors used in applications, such as the motor drive H-bridge circuit, must allow current flow in the first and third quadrant. The third-quadrant current flow can be conveniently achieved by using the body diode in the power MOSFET structure. The on-state voltage drop of the body diode in SiC power MOSFETs exceeds 4 V resulting in large conduction losses. The removal of the stored charge in the drift region produces a large reverse recovery current which increases the turn-on switching losses in the MOSFETs. This problem becomes worse at elevated junction temperatures.

The SiC JBSFET structure, with a JBS diode integrated into the power MOSFET structure [64, 65] as illustrated in Fig. 14.31, was developed to solve the above problems. The JBS diode can be fabricated using a single metal (Nickel) to simultaneously make a Schottky contact to the N-drift region and ohmic contacts to the N^+ source and P-base regions. The JBS diode has a low on-state voltage drop of 2 V preventing current flow via the body diode.

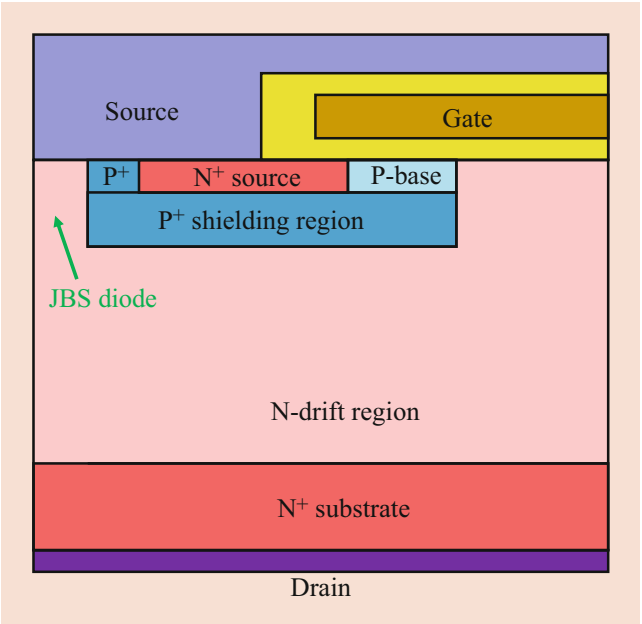

Fig. 14.31 The SiC JBSFET structure with JBS diode integrated into the power MOSFET structure

Measurements performed using 1.2 kV SiC JBSFETs in a typical hard-switched H-bridge inverter circuit have demonstrated that the peak reverse recovery current at elevated

temperature (150 °C) is reduced by 20% when compared with a 1.2 kV SiC power MOSFET's body diode [62]. The turn-on losses were found to be 50% smaller when using the JBSFET when compared with the SiC power MOSFET .

14.10 Unclamped Inductive Switching Stress

Power MOSFETs must be capable of absorbing high stress in circuits with unclamped inductive loads (UIL). The energy stored in the inductor must be absorbed by the device under high current avalanche breakdown. 1.2-kV 4H-SiC power MOSFETs has been studied under UIL stress [66]. A large (∼1000×) increase in leakage current was reported with 4% reduction in on-resistance. The greatest impact ionization was observed in the JFET region adjacent to the channel in numerical simulations. Hot holes are believed to be injected into the gate oxide producing the observed instability. The structure shown in Fig. 14.32 with a thick gate oxide over the JFET region was proposed to alleviate the problem. The thick gate oxide produced a reduction in the impact ionization rate due to smaller electric field near the channel.

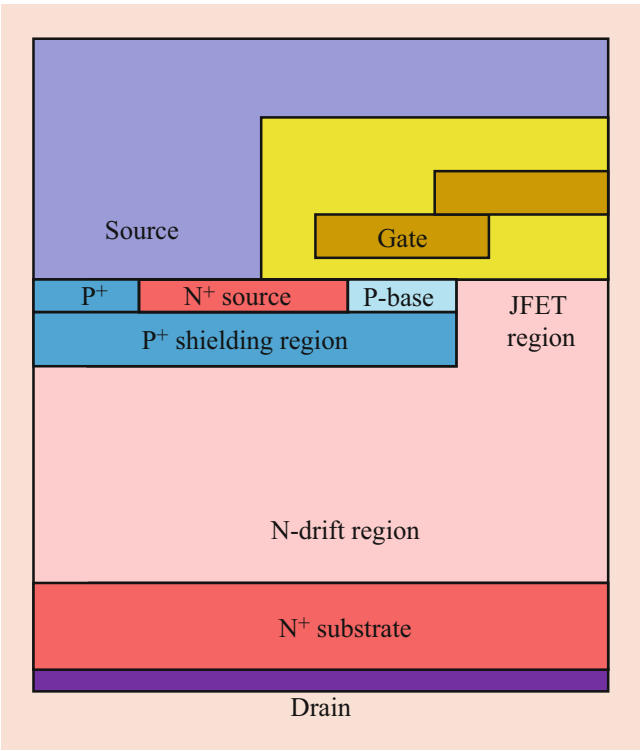

Fig. 14.32 Thick gate oxide planar 4H-SiC MOSFET structure with improved UIS capability

14.11 Short-Circuit Capability

Silicon IGBTs have excellent short-circuit withstand capability that is now commonly utilized in power electronic applications [1]. A similar capability is required for 4H-SiC power MOSFETs. Short-circuit tests on 1.2 kV 4H-SiC power MOSFETs tested with a DC bus voltage of 400 V [67] demonstrated 50 μs short-circuit time at a gate bias of 15 V. Planar-shielded 4H-SiC power MOSFET structures were reported [68] with improved performance due to shielding of the gate oxide. The devices were not evaluated at the typical circuit operating conditions of 800 V drain bias and 20 V gate bias.

1.2 kV Si IGBTs are available with the capability to survive a short circuit event in typical motor-drive applications for a duration of 15 μs with a collector bias of 800 V and on-state gate bias of 15 V. In contrast, typical 1.2 kV SiC power MOSFETs can survive a short circuit duration of only 4 μs with a collector bias of 800 V and on-state gate bias of 20 V [69]. An increase in short-circuit time can be achieved by reducing the saturated drain current at the on-state gate bias by increasing the channel length, reducing the channel width, or increasing the gate oxide thickness. All of these approaches produce an increase in the on-state resistance. Consequently, the short circuit capability must be traded-off against the specific on-resistance.

A recent study has demonstrated that the 1.2 kV SiC JBSFET structure provides a superior trade-off between specific on-resistance and short-circuit withstand capability (time) [70]. The JBSFET has a larger cell width compared with the MOSFET because of integration of the JBS diode. This reduces the channel density leading to a smaller saturation current for the same gate drive voltage. The 1.2 kV JBSFET were found to have a short-circuit time of 7 μs for a gate bias of 20 V and 11 μs for a gate bias of 15 V. As discussed in the previous section, the power SiC MOSFET must be paired with a JBS anti-parallel diode to reduce reverse recovery losses. The specific on-resistance for the JBSFET was found to be 24% smaller than that for a MOSFET with antiparallel diode when the area of the JBS diode is taken into account.

14.12 Shielded Trench-Gate Power MOSFET Structure

The silicon UMOSFET structure shown in Fig. 14.10 cannot be replicated in SiC because a high electric field develops across the oxide at the bottom of the trench leading to destructive failure. This problem occurs because the trench penetrates the P-base region exposing the gate oxide at the bottom of the trench to the high electric field in the silicon carbide drift region. The electric field in the gate oxide

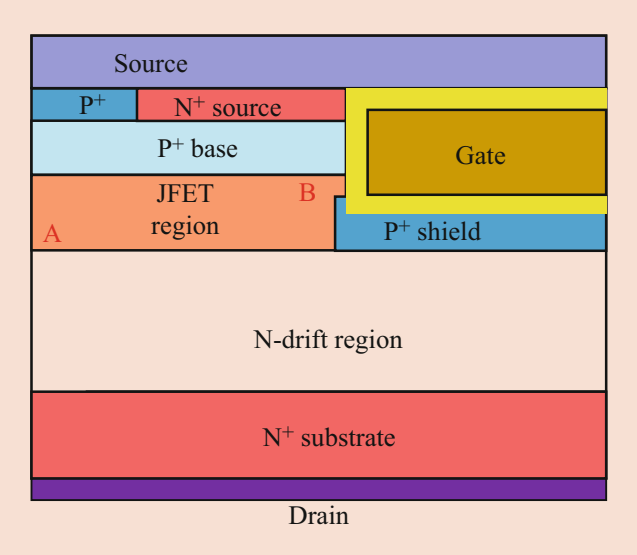

Fig. 14.33 Trench-gate SiC power MOSFET structure with P+ shielding region at trench bottom

reaches its rupture strength well before the electric field in the semiconductor approaches its breakdown field strength [22]. Consequently, in order to operate at any given blocking voltage, the drift region doping concentration has to be reduced and its thickness increased until the specific on-resistance becomes 25 times larger than that for the ideal drift region. This problem inhibited the performance of the first trench-gate 4H-SiC power MOSFETs. The trench-gate SiC power MOSFET structure with a P^+ shielding region at the trench bottom was proposed [71] to solve the problem.

14.12.1 Device Structure

The shielded trench-gate SiC power MOSFET structure is shown in Fig. 14.33. A P^+ region, connected to the source electrode at a location orthogonal to the device cross section, is placed at the bottom of the trench. The P^+ shielding region can be formed by ion implantation after etching the trenches.

The shielded trench-gate power MOSFET blocks current flow at low drain bias voltages with the voltage supported by the P-base/N-drift junction. A positive potential occurs at location "A" in Fig. 14.33 reverse biasing the junction between the P^+ shielding region and the N-drift region. The JFET formed by the P^+ shielding region produces a potential barrier at location "A" shielding the P-base region. This suppresses reach-through in the P-base region allowing shortening the channel length to reduce the on-resistance. It also reduces the electric field at location "B" which prevents high gate oxide electric fields.

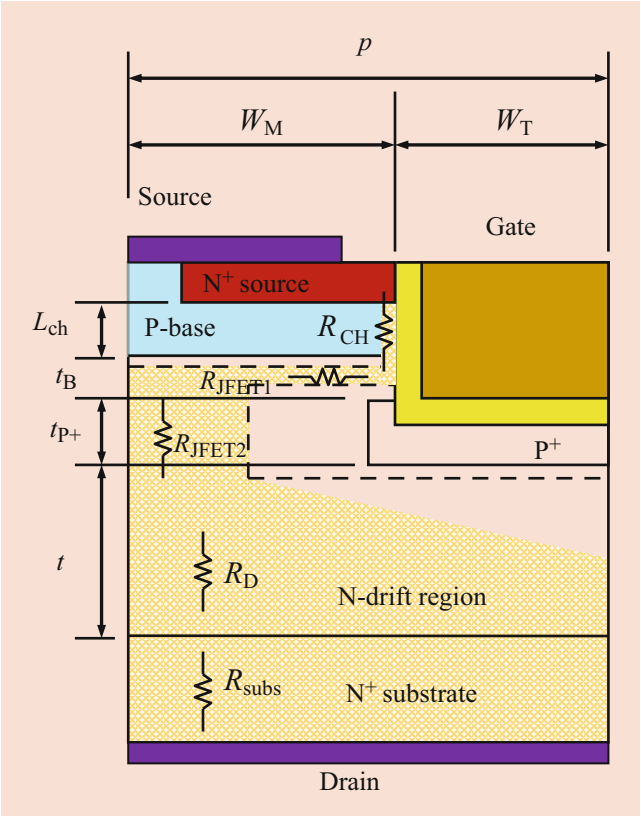

Fig. 14.34 Resistances in the shielded trench-gate SiC power MOSFET

14.12.2 On-Resistance

Current flow between the drain and source occurs in the shielded trench-gate MOSFET structure by creating an inversion layer channel at the trench sidewalls on the surface of the P-base region. Current flows from the source region into the drift region through the channel. The current flow at point "B" in Fig. 14.33 occurs via the first JFET (JFET1) region. It is then constricted by a second JFET (JFET2) region at point A before spreading into the N-drift region at a 45 degree angle. The current flow path is shown by the shaded regions in Fig. 14.34.

The spacing t_B in the figure must be sufficient to prevent it from becoming completely depleted. A smaller spacing can be used by increasing the doping concentration in the JFET1 region. The resistance of the second JFET region (R_{JFET2} in the figure) can also be reduced with this enhanced doping.

The specific on-resistance for the shielded trench-gate power MOSFET structure is

$$R_{on,sp} = R_{CH} + R_{JFET1} + R_{JFET2} + R_D + R_{subs} \quad (14.22)$$

where R_{CH} is the channel resistance, R_{JFET1} and R_{JFET2} are the resistances of the two JFET regions, R_D is the resistance of

the drift region, and R_{subs} is the resistance of the N^+ substrate. The specific channel resistance is.

$$R_{CH} = \frac{(L_{CH} \cdot p)}{\mu_{inv} C_{ox} (V_G - V_T)} \tag{14.23}$$

where L_{CH} is the channel length, μ_{inv} is the inversion layer mobility, C_{ox} is the specific gate oxide capacitance, V_G is the applied gate bias, and V_T is the threshold voltage. The specific gate oxide capacitance is

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{14.24}$$

where ε_{ox} is the dielectric constant for the gate oxide and t_{ox} is its thickness.

The specific resistance of the first JFET region is

$$R_{JFET1} = \rho_{JFET} \cdot p \cdot \left(\frac{x_{P+} + W_P}{t_B - 2W_P} \right) \tag{14.25}$$

where ρ_{JFET} is the resistivity of the JFET region, x_{P+} is the junction depth of the P^+ shielding region, and W_P is the zero-bias JFET region depletion width. The specific resistance of the second JFET region is

$$R_{JFET2} = \rho_{JFET} \cdot p \cdot \left(\frac{t_{P+} + 2W_P}{W_M - x_{P+} - W_P} \right) \tag{14.26}$$

The drift region spreading resistance is

$$R_D = \rho_D \cdot p \cdot \ln \left(\frac{p}{W_M - x_{P+} - W_P} \right) + \rho_D \cdot (t - W_T - x_{P+} - W_P) \tag{14.27}$$

where t is the thickness of the drift region below the P^+ shielding region and W_T, W_M are the widths of the trench and mesa regions, respectively, as shown in the figure. The N^+ substrate resistance is

$$R_{subs} = \rho_{subs} \cdot t_{subs} \tag{14.28}$$

where ρ_{subs} and t_{subs} are the resistivity and thickness of the substrate, respectively. The typical value is 4×10^{-4} Ω-cm^2.

The specific on-resistances obtained by using the above analytical models are shown in Fig. 14.35 for the 1.2 kV rated 4H-SiC shielded trench MOSFETs modeled using the above analytical expressions. Device parameters were (a) drift region thickness (t) of 12 μm; (b) drift doping concentration of 1×10^{16} cm^{-3}; (c) gate oxide thickness of 0.05 μm; (d) mesa width (W_M) of 1.0 μm; (e) trench width (W_T) of 0.25 μm; (f) P^+ shielding region junction depth of 0.2 μm; (g) space between P^+ shielding region and the P-base region (t_B) of 0.8 μm; and (h) JFET region doping concentration of 5×10^{16} cm^{-3}. A gate bias voltage (V_G) of 15 V was assumed with threshold voltage (V_T) of 5 V.

The on-resistance components are plotted in Fig. 14.35 for the case of channel inversion layer mobility of 25 cm^2/Vs. The channel resistance increases with increasing channel length as expected with no change in the other components. The drift region resistance is dominant for channel lengths below 1 μm. A total specific on-resistance of 1.8 mΩ-cm^2 can be achieved with a channel length of 0.4 μm, This is only five times the ideal specific on-resistance of the drift region.

14.12.3 Experimental Results

The trench-gate 4H-SiC power MOSFETs with a P^+ shielding region were experimentally demonstrated [72] in 2002 using a 50 μm thick N-type drift region with doping concentration of 8.5×10^{14} cm^{-3}. The doping concentration in the JFET region was increased by growth of an N-type layer with doping concentration of 2×10^{17} cm^{-3}. The 1 μm thick P-type base region was epitaxially grown with doping concentration of 2×10^{17} cm^{-3}. The N^+ source region with doping concentration of 1×10^{19} cm^{-}3 was also epitaxially grown. After etching the trench regions, the 0.8 μm deep P^+ shielding regions were created by aluminum ion implantation using a dose of 4×10^{13} cm^{-2}. A 0.275 μm thick gate oxide was formed by oxidation of polysilicon deposited into the trench resulting in a high threshold voltage of 40 V. A breakdown voltage of 3000 V was achieved by using a JTE edge termination. The low inversion layer channel mobility of 2 cm^2/V-s resulted in a high-specific on-resistance of 120 mΩ-cm^2 at a gate bias of 100 V. 5 kV devices were subsequently reported using 115 μm thick N-type drift regions with doping concentration of 7.5×10^{14} cm^{-3} [73]. A specific on-resistance of 228 mΩ-cm^2 was observed at a gate bias of 40 V.

An accumulation-channel trench-gate MOSFET structure, shown in Fig. 14.36, was reported with an epitaxially grown N-base region on the trench sidewalls [74] to achieve an accumulation channel mobility of 9–30 cm^2/V-s. A breakdown voltage of 1400 V was obtained by using a 10 μm thick N-type drift region with doping concentration of 2.5×10^{15} cm^{-3}. The 0.13 μm thick gate oxide was created by thermal oxidation of polysilicon deposited into the trenches. 16 mΩ-cm^2 specific on-resistance of was reported at a gate bias of 40 V.

The specific on-resistance of the shielded trench-gate 4H-SiC power MOSFET was improved by using two JFET layers [75] as shown in Fig. 14.37. A JFET layer 1 with doping concentration of 0.5–1 $\times 10^{17}$ cm^{-3} with a thickness of 0.5 μm was used to reduce R_{JFET1} and a JFET layer 2 with doping concentration of 1–2 $\times 10^{16}$ cm^{-3} with a thickness of 3 μm was used to reduce R_{JFET2}. A drift layer doping

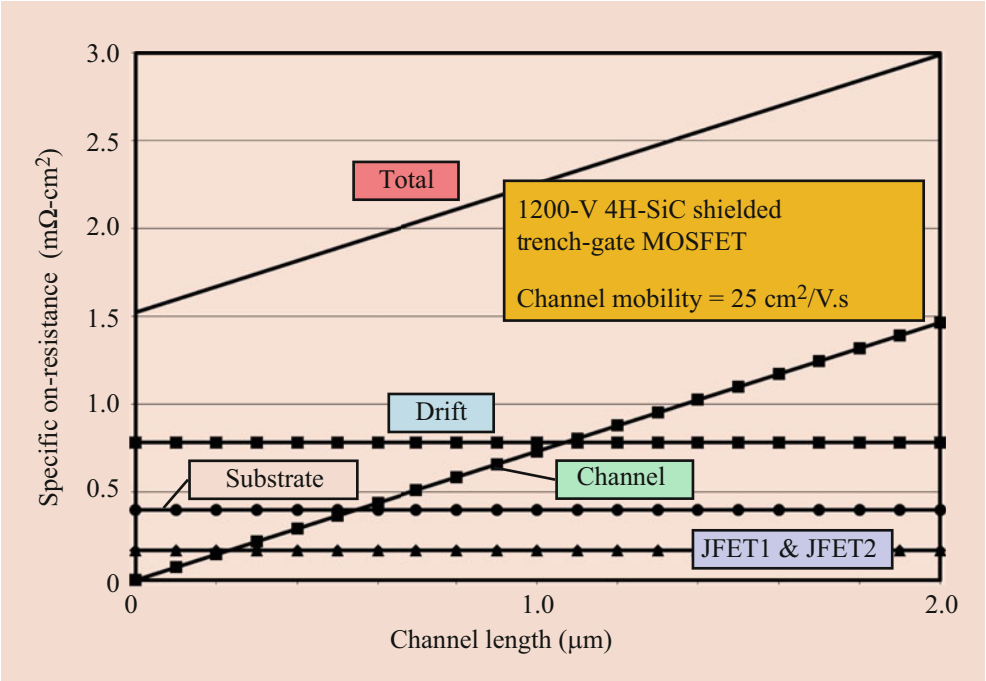

Fig. 14.35 On-resistances within 1.2 kV 4H-SiC shielded trench-gate MOSFET

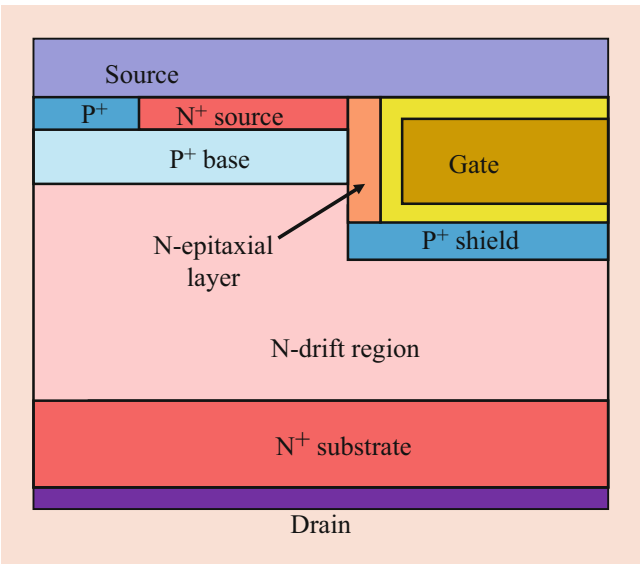

Fig. 14.36 Accumulation-channel trench-gate power MOSFET with epitaxial N-base region

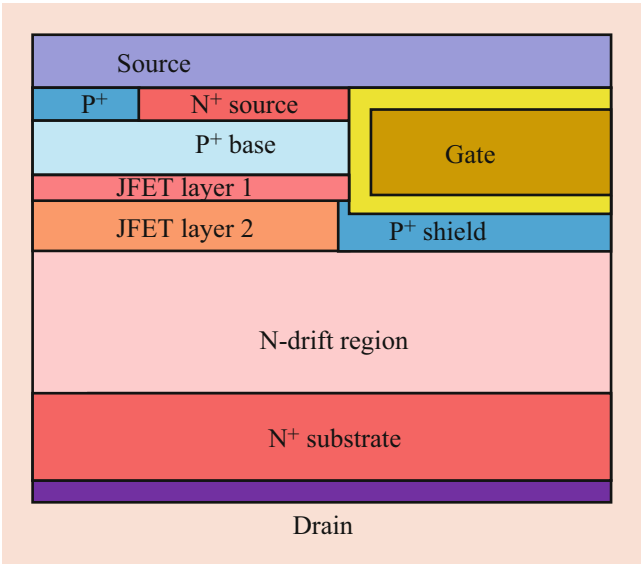

Fig. 14.37 Shielded trench-gate power MOSFET structure containing two JFET layers

concentration of 3–5 × 10^{15} cm^{-3} and thickness of 25 μm produced a blocking voltage of 1600 V. In spite of using a high gate bias of 60 V due to the large gate oxide thickness of 0.16 μm, a high specific on-resistance of 50 mΩ-cm^2 was observed. Various layout designs for connecting the P^+ shielding region to the source electrode have been explored [76]. At least one ground for every 9 cells was found to be necessary to get good short-circuit capability.

14.13 SiC Trench-Gate MOSFET with Thick Trench Bottom Oxide

The 4H-SiC trench-gate power MOSFET with thick trench bottom oxide is illustrated in Fig. 14.38. The electric field in the oxide at the bottom of the trench is reduced due to the larger thickness [77]. The electric field in the thick bottom

oxide was reduced to 5.0 MV/cm compared with 7.8 MV/cm for case with thin bottom oxide at a drain voltage of 1400 V for a drift region doping concentration of 6×10^{15} cm^{-3} and thickness of 13 μm. A specific on-resistance of 4.6 mΩ-cm^2 was reported for a gate bias of 20-V with 0.075 μm thick gate oxide.

Numerical simulations comparing the electrical performance of 1.2 kV rated SiC trench-gate power MOSFETs have been reported [78]. A summary of the findings are shown in Table 14.1. The trench bottom oxide thickness is the same as the gate oxide thickness in the basic structure. The trench-gate structure with thick bottom oxide (0.7 μm) has the lowest specific on-resistance. Its high-frequency-figure-of-merit (HF-FOM = [$R_{ON,SP}$*$C_{GD,SP}$]) is better than the basic trench-gate MOSFET structure. The trench-gate structure with P$^+$ shielding region at the trench bottom (see Fig. 14.33) has a higher specific on-resistance but similar HFFOM. The commercially available trench-gate MOSFETs from Rohm and Infineon have larger specific on-resistance. The Rohm and Infineon devices are discussed in the next section.

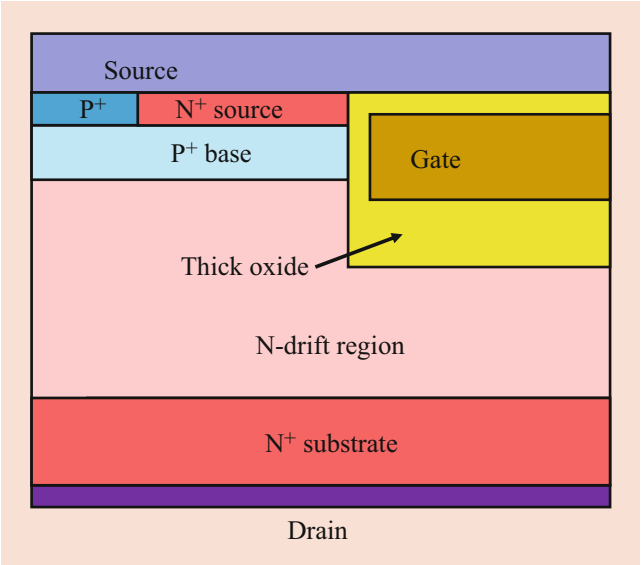

Fig. 14.38 Trench-gate power MOSFET structure with thick trench bottom oxide

14.14 SiC Trench-Gate MOSFET with Deep P+ Trench Regions

An approach taken by Rohm for shielding the gate oxide from high electric fields generated in the silicon carbide drift region is incorporation of a P$^+$ region in the mesa region by etching a second deep trench [79] as illustrated in Fig. 14.39. The deep P$^+$ regions shield the oxide at the bottom of the gate trenches. The electric field in the oxide was found to be less than 3 MV/cm if the P$^+$ region is 1.2 μm deeper than the bottom of the gate trench. 600 V devices were reported [80] with specific on-resistance of 0.79 mΩ-cm^2. Subsequently, 1200 V devices were reported [81] with specific on-resistance of 4 mΩ-cm^2 at a gate bias of 18 V.

The trench-gate SiC power MOSFET structure, shown in Fig. 14.40, with two deep P$^+$ regions has been reported by Infineon [82]. Both P$^+$ regions are used to form the JFET that reduces the electric field in the gate oxide. It is worth pointing out that the channel in this structure is formed along only one sidewall of the trench. This reduces the channel density resulting in the highest specific on-resistance among the trench-gate devices as shown in Table 14.1. However, it has a very low gate-drain capacitance resulting in excellent HFFOM.

14.15 SiC V-Groove Trench-Gate MOSFET

V-groove formation by thermochemical etching in a chlorine ambient [83] was used to make the trench 4H-SiC power MOSFET structure shown in Fig. 14.41. An inversion layer mobility of 80 cm^2/V-s was reported [84] along the sloping trench sidewalls. After growth of the N-type drift layer with doping concentration of 4.5×10^{15} cm^{-3} with a thickness of 12 μm, buried P$^+$ regions were formed by Aluminum ion implantation. A second epitaxial layer was then grown with doping concentration of 7×10^{15} cm^{-3} and thickness of

Table 14.1 Simulation results for trench-gate SiC MOSFET structures

MOSFET structure	Cell pitch (μm)	$R_{ON,SP}$ (mΩ-cm^2)	BV (V)	$C_{GD,SP}$ (pF/cm^2)	HF-FOM (mΩ-pF)
Basic structure	1.3	1.8	1645	734	1321
NCSU thick trench bottom oxide structure	1.3	1.89	1610	417	788
NCSU structure with dual P$^+$ shielding regions	1.3	2.68	1672	289	775
Rohm structure with deep P$^+$ trench regions	3.0	2.44	756 (reach-through limited)	366	893
Infineon with deep P$^+$ trench regions	2.8	3.77	1538	10	37

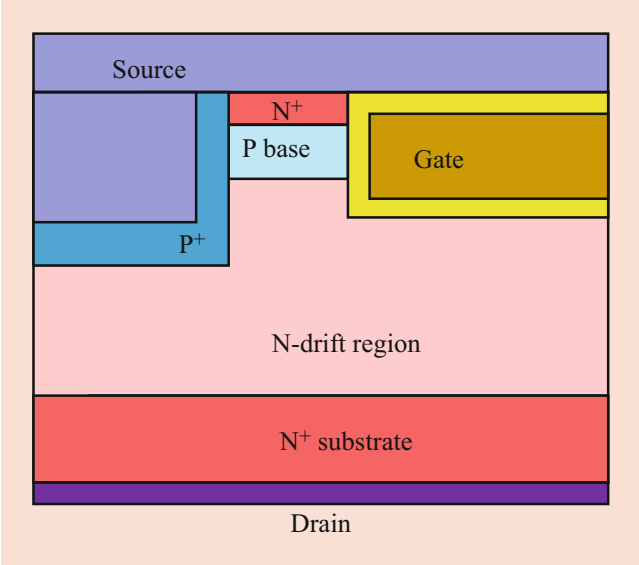

Fig. 14.39 Trench-gate power MOSFET structure with deep P^+ shielding region formed in a second trench

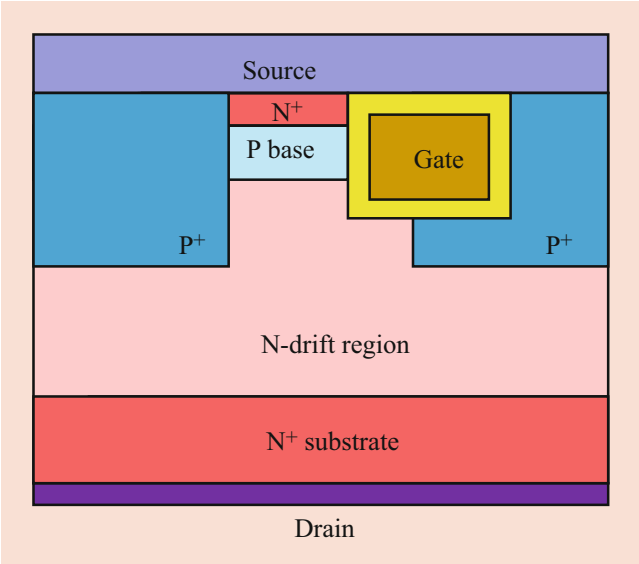

Fig. 14.40 Trench-gate power MOSFET structure with two deep P^+ shielding regions

3 μm. A channel length of 0.6 μm is achieved on the sloping trench sidewalls by controlling the P-base and N^+ source region depths. The buried P^+ regions shield the gate oxide. Devices with breakdown voltage of 1700-V had a specific on-resistance of 3.6 mΩ-cm^2 at a gate bias of 18 V. A hexagonal cell topology was optimized [85] demonstrating that the P^+ regions should occupy 30% of the active area to produce the best trade-off between low specific on-resistance and high breakdown voltage.

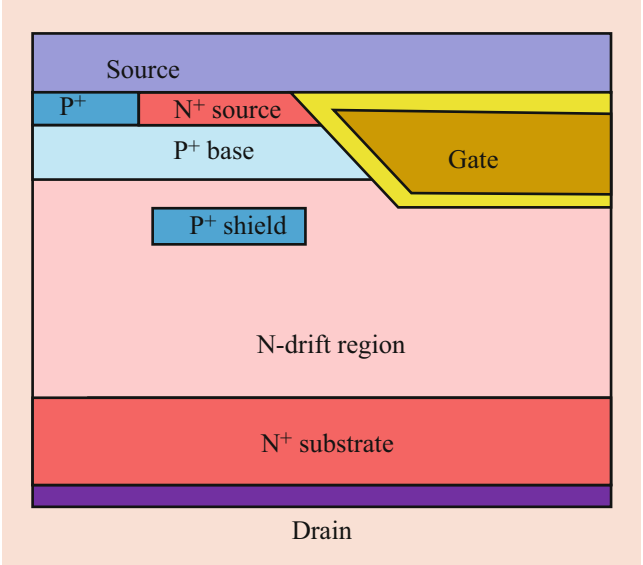

Fig. 14.41 Trench-gate power MOSFET structure with buried P^+ shielding region and V-groove trench shape

14.16 Silicon Carbide Bi-Directional Field Effect Transistor

Power devices that can block high voltage in the first and third quadrants and carry gate controlled current in both quadrants are required to create matrix converters [86]. Bidirectional switches have been proposed using either silicon IGBTs or SiC power MOSFETs with multiple independently packaged devices. These approaches are expensive, consume space, and exhibit high on-state voltage drop. The SiC-based Bi-directional Field Effect Transistor (BiDFET) solves these issues [87, 88]. In the BiDFET, two SiC JBSFETs are connected in series as shown in Fig. 14.42 with a common drain. The JBSFETs can be monolithically integrated on the same SiC wafer to create a four-terminal device. High AC voltages can be applied to terminal T2 of the BiDFET with Terminal T1 as the reference terminal. Gates G1 and G2 can be biased to control current flow in the first and third quadrant.

With zero bias applied to gate G1 with respect to terminal T1, a high positive voltage applied to terminal T2 can be supported across power JBSFET-1 and its edge termination, while the JBS diode in JBSFET 2 is forward biased. With zero bias applied to gate G2 with respect to terminal T2, a high negative voltage applied to terminal T2 can be supported across power JBSFET-2, and its edge termination while the JBS diode in JBSFET 1 is forward biased. This provides the BiDFET with symmetric high blocking voltage capability in both quadrants.

Application of a positive gate drive voltage to both gates G1 and G2 with reference to the corresponding terminals T1 and T2 allows current conduction in the first and third quadrants via the channel for both SiC power JBSFETs. The

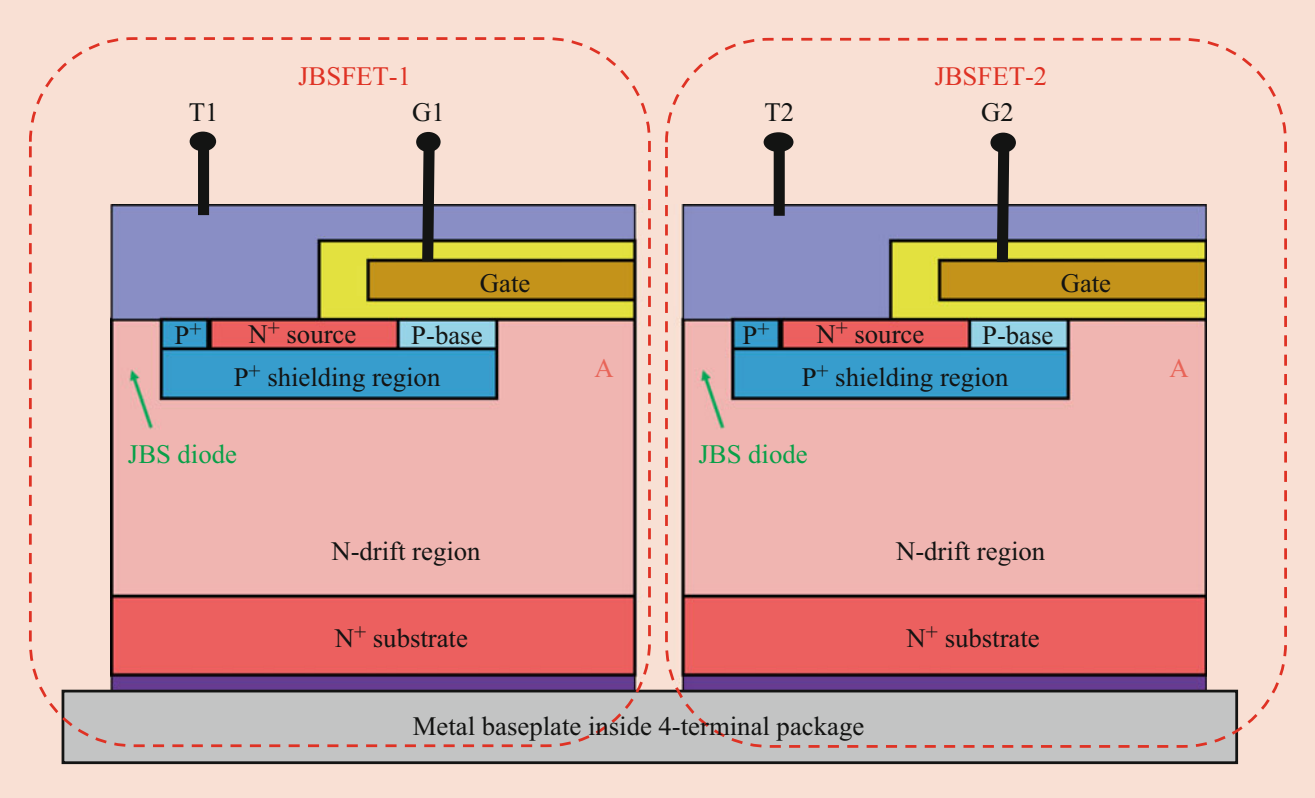

Fig. 14.42 The SiC Bi-Directional Field Effect Transistor (BiDFET) structure

on-resistance of the BiDFET is the sum of the on-resistance of JBSFET 1 and 2.

Excellent output characteristics with gate voltage controlled current saturation are achieved in the BiDFET due to the internal SiC power JBSFETs. Fast switching capability is also ensured in the BiDFET due to the internal SiC power JBSFETs. These features allow matrix converters with BiDFETs to operate at high frequencies to achieve high-power density.

BiDFET were first experimentally demonstrated by using 1.2 kV rated JBSFETs [88]. The devices exhibited gate voltage controlled output characteristics with blocking voltages of up to 1650 V in the first and third quadrant. The on-resistance of the BiDFET in both quadrants was found to be the sum of the resistance of each of the JBSFETs as expected. A low on-state voltage drop can be achieved by increasing the active area of both JBSFETs. A 1.2 kV rated SiC BiDFET with on-resistance of 50 mΩ was achieved by packaging two commercially available SiC power MOSFET dies in a 4-terminal module [89]. In addition, a monolithic 1.2 kV SiC BiDFET was successfully manufactured in a 6-inch foundry and the single die packaged in a 4-terminal module [90]. In comparison with previous bi-directional switches that required 4–6 separately packaged devices, the BiDFET requires only a single four-terminal package.

14.17 Commercial Devices

The commercialization of silicon carbide power devices became feasible with the ability to grow 4H-SiC wafers with diameters of 100 mm. Wafers with diameters of 150 mm are now available from multiple sources. In addition, the ability to grow thick epitaxial layers with doping concentration approaching 1×10^{14} cm^{-3} have made the manufacturing of the very high voltage (>10-kV) silicon carbide products a possibility. However, companies have targeted the 1200-V and 1700-V markets for their initial products. At this voltage range, the 4H-SiC unipolar devices offer much better switching characteristics than silicon IGBTs while providing a lower on-state voltage drop as well.

The first 4H-SiC products were JBS rectifiers. Two kinds of silicon carbide switches have been developed as products: JFETs and MOSFETs. The JFETs were introduced earlier because of problems with poor channel mobility in MOSFETs. Recent progress with improving MOS-channels – with advanced gate oxide and interface preparation, and by utilizing the accumulation-mode concept – has made high performance 4H-SiC power MOSFET products feasible. The momentum for power switch product commercialization has now shifted from JFETs to MOSFETs.

14.18 Silicon Carbide Power Device Applications

Silicon carbide power MOSFETs are excellent candidates to replace silicon IGBTs in all applications because of their low on-resistance and reduced switching losses. However, the cost of the SiC power MOSFETs is substantially larger than that of silicon IGBTs. As a consequence, SiC power MOSFETs have been successfully used only in selected applications as shown in Fig. 14.43. One of these applications is inverters for solar power generation. The replacement of silicon IGBTs with SiC power MOSFETs has been shown to increase the efficiency by 1–2%. This modest gain in energy generation offsets the larger initial cost of the SiC devices.

Another promising application for SiC power MOSFETs is in inverters for electric and hybrid-electric vehicles. The improved inverter efficiency allows extending the range of the vehicles. In addition, the SiC inverters can be operated at higher frequencies than those based on silicon IGBTs. This allows reduction of passive component size and weight, an important benefit for electric vehicles.

As the cost of SiC power MOSFET is reduced in the future, it is anticipated that their applications will expand as indicated by the arrows in Fig. 14.43. The penetration of SiC power MOSFETs into applications served by the Si IGBT will be accelerated by making products with superior HF-FOMs, such as the SG-MOSFET and BG-MOSFET.

Due to the low switching losses for silicon carbide power MOSFETs, they are good competitors to silicon IGBTs in circuits operating at higher frequencies. One example is a 1 MVA solid-state power substation (SSPS) designed using 10-kV SiC modules [91] soft-switching at 20 kHz. Twenty-four MOSFETs and twelve Schottky diodes were used per module to achieve a current handling capability of 120 A per switch. Low voltage silicon Schottky diodes were placed in series with the SiC power MOSFETs to prevent conduction of the body diode. This can be avoided in the future by using the SiC JBSFET structure. The SSPS converted 13.8-kV to 300-V with 97% efficiency resulting in 75% reduction in weight and 50% reduction in size over the conventional 60-Hz transformer.

4H-SiC power MOSFETs have also been used to create a solid-state transformer (SST) to convert the 3.6-kV distribution grid voltage to 400-V DC and 240/120-V AC voltage [92]. By using 13-kV SiC power MOSFETs on the primary side, the topology of the SST is simplified to a single H-bridge AC/DC rectifier, an isolated dual half-bridge (DHB) DC/DC converter, and a DC/AC inverter. The DC link operates at 6-kV inside the SST. The DHB is

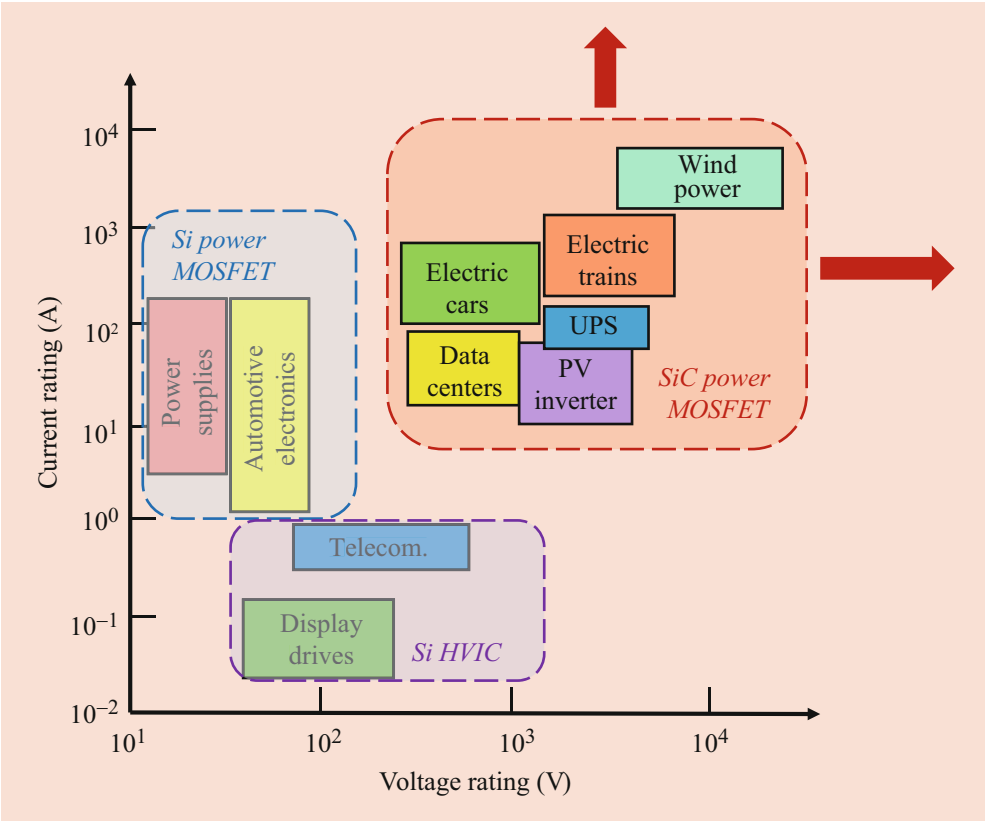

Fig. 14.43 SiC power device application opportunities

operated at 15 kHz to reduce the size and weight of the high-frequency transformer. The switching losses in the SiC power MOSFETs are reduced by soft-switching. 1.2 kV SiC power MOSFETs are used on the secondary side to produce the 400-V DC and 220/120 V AC outputs. The rectifier stage and the DHB were found to have an efficiency of over 98%, while the peak efficiency for the inverter stage was 97%.

14.19 Conclusions

In this chapter, the inclusion of a P-N junction to shield the Schottky contact was shown to be essential to create SiC JBS rectifiers that became successful products. These devices are now commercially available for use as anti-parallel diodes with IGBTs in inverter circuits.

In the case of SiC planar-gate power MOSFETs, the incorporation of a sub-surface P^+ shielding region was found to be essential to prevent P-base reach-through limited breakdown and for preventing high electric fields from developing across the gate oxide during the blocking mode. Since relatively low inversion layer mobility has been reported for 4H-SiC MOSFETs, an accumulation-mode structure was proposed with an N-base region that is completely depleted by the built-in potential of the underlying P^+/N junction. This structure takes advantage of the much larger accumulation mobility observed in semiconductors.

The operating principle of the planar shielded MOSFET structures has been reviewed in the chapter providing guidelines for the design of the structures. It has been demonstrated that the JFET width is a critical parameter that controls the electric field at the gate oxide interface as well as the specific on-resistance. Its optimization is important for obtaining high performance devices. In the case of the accumulation-mode structure, the appropriate combination of the doping concentration and thickness of the N-base region must be chosen to ensure that it is completely depleted by the built-in potential of the underlying P^+/N junction. With adequate shielding of the base region, it is found that short channel devices will support high blocking voltages limited only by the properties of the drift region. These devices have excellent safe-operating-area and fast switching speed. This technology has potential for use in systems operating at and perhaps above 10,000 V.

The specific on-resistance for SiC power MOSFETs calculated using two values for the channel resistance are shown in Fig. 14.44 as a function of the blocking voltage. The ideal specific on-resistance for silicon and silicon carbide is included in the figure. It is apparent that the planar-gate devices can approach the ideal limit of performance for blocking voltages above 5 kV. However, devices with blocking voltages below 2 kV become limited by the channel resistance. State-of-the-art devices planar-gate devices have performance consistent with this analysis as shown by the triangular points [93].

In conclusion, silicon carbide power MOSFETs have reached a sufficient degree of maturity to find applications at higher frequencies. They can replace silicon IGBTs in

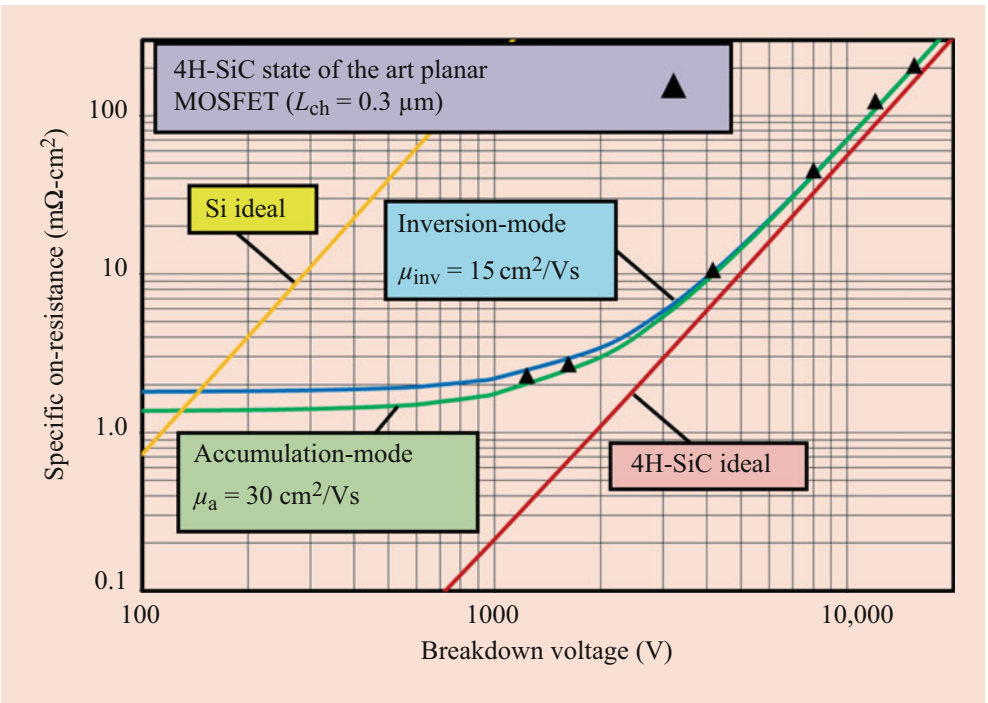

Fig. 14.44 Specific on-resistance for SiC power MOSFETs of various blocking voltages

applications where the switching losses are dominant to achieve significant reduction of size and weight due to improved efficiency. The development of silicon carbide power devices has been motivated by the opportunity to create unipolar devices with high blocking voltage capability. Silicon carbide JBS rectifiers and power MOSFETs with excellent on-state voltage drop have been demonstrated with blocking voltages up to 5000 V. These devices offer low switching losses when compared with the silicon P-i-N rectifiers and IGBTs enabling increasing the circuit operating frequency which reduces the size of passive components and filters in applications. The applications of the SiC devices is constrained by their higher cost when compared with silicon devices. The lower switching losses of these devices can to utilized to increase the circuit operating frequency leading to smaller, less expensive passive elements to offset the higher device cost.

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GaN-Based Lateral and Vertical Devices

15

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Contents

15.1 GaN Material and Epitaxy 526
15.1.1 Typical Layer Stacks for Lateral GaN Power Transistors 527
15.1.2 Substrates, Nucleation, and Strain Management 527
15.1.3 Growth on SiC Substrates 527
15.1.4 Growth on Si Substrates 527
15.1.5 Back-Barrier Selection 529
15.1.6 HEMT Heterostructures 530

15.2 Lateral Devices Architectures 531
15.2.1 Applications 533
15.2.2 State-of-the-Art 533
15.2.3 Limitations of GaN Lateral Devices 534
15.2.4 Pushing the Limits of Lateral GaN Devices: Enhancement of the Blocking Voltage 537
15.2.5 Normally-Off GaN Lateral Devices 538

15.3 Vertical Devices Architectures 541
15.3.1 Device/Circuit Hybrid Modeling 543
15.3.2 Physics Models for GaN 543
15.3.3 A Review of CAVET 549
15.3.4 Operation Principle of the CAVET 549
15.3.5 Trench CAVET 550
15.3.6 Vertical MOSFETs 551
15.3.7 Regrowth-Based Vertical MOSFET (OGFET) 552
15.3.8 Static Induction Transistor 553
15.3.9 Conclusions on GaN Vertical Transistors 555

15.4 Parasitics and Reliability 556
15.4.1 Charge-Trapping in GaN-Based Power HEMTs 556
15.4.2 Methods to Investigate Charge-Trapping Phenomena 557
15.4.3 Performance and Characteristics of GaN Devices and Challenges 560
15.4.4 Reliability Issues of GaN-Based Power HEMTs 564
15.4.5 Gate-Stack Reliability 565
15.4.6 Off-State Reliability 568
15.4.7 Stability in Semi-on Conditions 572

15.5 Conclusions 573

References 573

Abstract

In the last decade, GaN has emerged as an excellent material for application in power electronics. The wide energy gap of gallium nitride (3.4 eV) enables high-temperature operation, while the large breakdown field (3.3 MV/cm, 11 times higher than silicon) allows to reach kV-range operation while maintaining a low on-resistance. Thanks to the high mobility of the two-dimensional electron gas at the AlGaN/GaN interface, lateral GaN transistors have a very low on-resistance; commercial products are already on the market, and new technologies are being developed, targeting the 650 V/900 V ranges. Recently, the attention toward vertical GaN transistors has constantly increased: a vertical layout allows to substantially increase current density while taking advantage of the wide bandgap and high breakdown field of GaN. Vertical transistors based on GaN are expected to find application in converters with medium high power levels (>5 to 10 kW), once the technology reaches maturity.

This chapter reviews the main properties of GaN-based materials and devices. The first part focuses on the main challenges related to the growth of high-quality GaN epitaxial stacks. The second and the third parts focus on GaN lateral and vertical devices, respectively. Finally, the fourth section describes the trapping and degradation

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processes that limit the performance and the reliability of GaN transistors, and the related physical mechanisms. This chapter represents an ideal guide for a reader willing to enter the world of GaN devices.

Keywords

GaN · Technology · Gallium nitride · Reliability · Transistor · III-V

15.1 GaN Material and Epitaxy

When GaN-based white LED's became the technology to beat for lighting applications after some major technological hurdles were overcome, such as the development of a workable epitaxy regime [1], scientific interest was aroused to use this material system also for purely electronic applications. By taking advantage of the strong polarization fields in the III-nitrides, which limit the performance of quantum well-based light emitters because of the quantum confined Stark effect [2], a unique structure for transistor channels was devised: the GaN/AlGaN high electron mobility transistor (HEMT) [3]. These lateral transistor devices can handle very large power densities due to the combination of the good transport properties on the one hand and of the excellent voltage handling capabilities on the other hand, courtesy of the material's high bandgap and critical electrical field. From epitaxy point of view, these two types of applications are characterized by a number of distinct differences.

For opto-electronics, the substrate of choice is sapphire, as it is optically transparent, relatively easy to perform hetero-epitaxy on and can be reused several times by taking advantage of the laser lift-off technique [4]. For electronic applications, sapphire has a major shortcoming in terms of its low thermal conductivity which causes trouble with thermal dissipation in high power density devices. Instead, the traditional choice for substrates for electronic applications is SiC, while in the recent years Si has become a very popular choice as well.

A second major difference between the two types of application is the range of alloys that is typically used. For the bulk of lighting applications, LEDs need to cover the visible range of the optical spectrum which is done by using InGaN alloys in combination with n- and p-doped GaN layers. Because of the volatility of Indium and the miscibility issues in InGaN alloys [5], epitaxy of such layers is performed at relatively low temperatures, roughly between 700 °C and 900 °C for MOCVD processes. For electronic applications, the critical electric field of the materials is an important parameter, which scales directly with the bandgap of the semiconductor materials. As a result, layers stacks for electronic applications typically consist of AlGaN alloys that require a rather different epitaxial regime, e.g., characterized by the higher growth temperatures (above 1000 °C when grown by MOCVD) to obtain the best material quality.

Obviously, the layer stack designs differ significantly as well: p-i-n diodes for LEDs as opposed to the undoped HEMT hetero-structures for lateral transistors.

15.1.1 Typical Layer Stacks for Lateral GaN Power Transistors

The lack of availability of native GaN substrates in large wafer diameters and at reasonable cost forces the GaN community to use hetero-epitaxy to grow III-nitride materials on foreign substrates, such as sapphire, silicon, or silicon carbide. The intrinsic mismatches between substrate and epitaxial materials, for instance, in terms of lattice constant or thermal expansion coefficient, prevent the direct growth of the active HEMT layers on top of the substrate. Instead, a relatively complex buffer stack needs to be inserted in between. Figure 15.1 shows the typical construction of the epitaxial layer stack, together with the most commonly used implementations. We will discuss the different variations below.

15.1.2 Substrates, Nucleation, and Strain Management

For electronic applications, typically two substrate types are used: silicon carbide (SiC) and silicon (see Table 15.1). Sapphire, which is the substrate of choice for the LED business, is not used because of its low thermal conductivity that becomes a reliability issue for transistors that operate at and dissipate high power densities.

15.1.3 Growth on SiC Substrates

For most RF applications, SiC is used as a substrate, first because of its relatively low lattice mismatch with GaN that allows a very simple nucleation and buffer structure and secondly because of its high thermal conductivity. In practice, the layer stack as depicted in Fig. 15.1 is simplified to consist of a thin AlN nucleation layer, a GaN-based confinement layer (typically unintentionally doped or Fe-doped) with a thickness of roughly 1 μm and the active channel/barrier layer combination.

Most SiC substrates are wafered from SiC bulk crystals that are grown using the Physical Vapor Transport (PVT) method [6]. The latter operates at temperatures exceeding 2000 °C, provides low growth velocities, and is thus very energy intensive. The typical crystals that can be obtained by PVT are typically only 20–30 cm long and yield only a limited number of wafers. As a result, SiC wafers are 20–50 times more expensive than their Silicon counterparts.

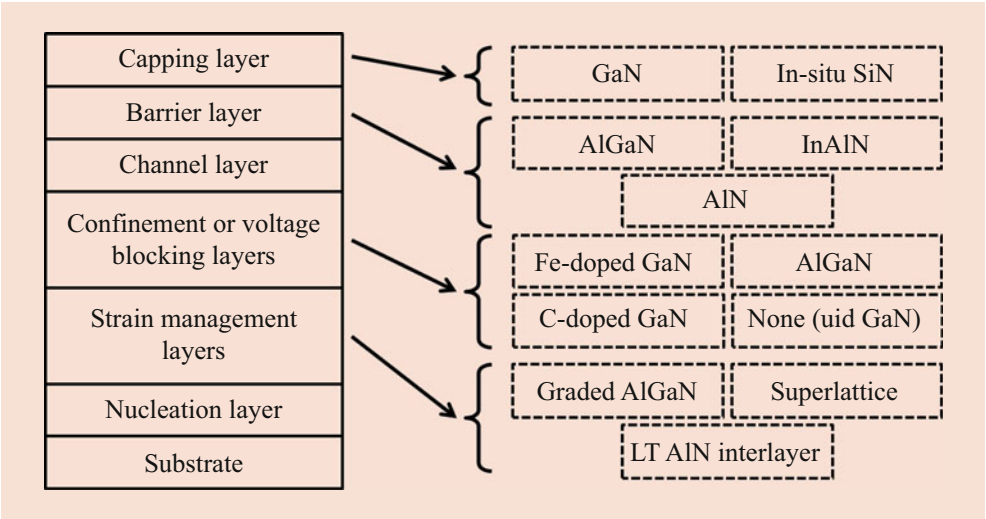

Fig. 15.1 Layer stack variations for GaN electronics

Table 15.1 Properties of commonly used substrate materials

Substrate materials	GaN	SiC	Sapphire	Si
Lattice constant (å)	3.19	3.08	4.76	5.43
Mismatch to GaN	*0*	*−3.6%*	*33.0%*	*41.3%*
Thermal expansion coefficient (10^{-6} K)	5.59	4.3	7.3	3.59
Mismatch to GaN	*0*	*30.0%*	*−23.4%*	*55.7%*
Thermal conductivity (W/cmK)	1.3	4.9	0.23	1.4

Moreover, scaling the diameter of the crystal boule has been proven difficult. Only recently has the industry made the step from 4″ to 6″ diameters, with however still some quality issues remaining to be solved for the outer ring of the 6″ substrates. 200 mm SiC has been demonstrated but is currently not commercially available in large quantities.

15.1.4 Growth on Si Substrates

Over the last 15 years, a lot of effort has been spent to develop an epitaxy process to grow GaN directly on Si substrates (Krost). Being able to work on Si is very appealing: it is obviously the material of choice on which the bulk of the semiconductor industry is built (e.g., for logic and memory applications). Si manufacturing technology is extremely mature (yields well above 95%), very cost effective and capable of mass production (hundreds of thousands of wafers per month). Besides the cost advantage compared to SiC, one of the main drivers to select Si substrates is that it allows for much more easy integration of GaN-based devices with circuitry manufactured in Silicon-based CMOS. This is due to ease of back-side processing (e.g., wafer thinning or through-Si-via processing using the Bosch process) as well as due to the fact that there is no mismatch in material properties (thermal expansion coefficient being a good example).

Unfortunately, the hetero-epitaxy of GaN on Si comes with a plethora of challenges. For starters, the electronically most suitable type of GaN comes in a hexagonal close packed crystal structure (also called Wurtzite), which doesn't match the crystal structure of Si: the face-centered cubic crystal structure. The typical technical work-around is to use the triangular symmetry of the <111> plane of the Si.

Although many epitaxial techniques exist such as molecular beam epitaxy (MBE), hydride vapor phase epitaxy (HVPE), or liquid phase epitaxy (LPE), almost all production of GaN epitaxial layers is performed by a technique called metal-organic chemical vapor deposition (MOCVD) or metal-organic vapor phase epitaxy (MOVPE). In this technique, the growth temperature for high-quality GaN or AlGaN layers is above 1000 °C. At these temperatures, Ga attacks the Si substrate because of the eutectic lowering of the melting point of the materials; a phenomenon called Ga melt-ba ck of Si [7]. As a result, one cannot directly grow GaN on Si, but one needs to insert a layer of a different material. As on SiC, the solution is to grow an AlN nucleation layer that not only constitutes a good starting crystal for consecutive epitaxial growth but that also protects the Si from Ga-containing molecules in the vapor phase. Different solutions with other intermediary layers exist such as the use of 3C-SiC or rare earth oxides, but these lack the elegance and simplicity of using an in situ grown layer.

The nucleation process is an important one, because the extended defects that originate in this layer tend to propagate as threading dislocations through the entire layer stack that is built on top. Because of the reactivity of both species and the strong bond strength between aluminum and nitrogen, the growing AlN has low surface mobility and as a result,

the growth occurs by the formation of many separate AlN islands that laterally expand and coalesce. The locations where the islands meet are a source for many kinds of 1D and 2D extended defects. For the same reasons as mentioned above, AlN easily reverts to a three-dimensional growth mode (Volmer-Weber or Stanski-Krastanov) thus forming pyramids, rather than the preferred two-dimensional layer-by-layer growth mode (Frank-van der Merwe). This easily leads to surface roughening.

It has been shown that the properties of the interface between the Si and the AlN is of major importance both for high-voltage power switching as well as for RF power applications. In the former case, lateral conductivity along this interface causes the premature breakdown of lateral devices (as will be explained in Sect. 15.2 of this chapter), whereas for the latter case, the conductive interface causes RF losses for propagating signals and efficiency degradation in amplifiers.

There are more issues with GaN-on-Si epitaxy. As indicated in Table 15.1, GaN and Si have rather different thermal expansion coefficients. Even when one manages to employ the nucleation techniques as described above to grow high-quality GaN material, the cool-down step of over 1000 °C after epitaxy induces a substantial amount of tensile stress in the GaN epilayers, proportional to the thickness thereof. This is especially critical for high-voltage applications where the vertical voltage rating scales linearly with the thickness of the epilayer stack, requiring for instance a more than 5 μm thick layer stack for a 650 V rated device. Without controlling this issue, GaN-on-Si wafers tend to have significant bow and warp and are prone to the formation of cracks or even wafer breakage [8].

Over the years, several solutions where proposed to compensate for this tensile strain formation. They are all based on the principle of designing a buffer that generates an equal amount of compressive stress. In this way, it is possible to manufacture GaN-on-Si wafers that are perfectly flat; yet it is important to understand that such flat wafers are never stress-free but merely well stress-compensated. There is a second implication as well: the total amount of compressive stress that may be generated by the buffer is limited by the onset of plastical deformation of the Silicon substrate. This means that, depending on the thickness of the Silicon substrate, there is an upper limit to the total thickness of the III-nitride epilayer that can be grown on top.

The first type of strain management buffer is based on graded AlGaN layers. On top of the AlN nucleation layer, AlGaN layers are deposited where the Al composition is reduced, either continuously or in discrete steps, from 100% (AlN) down to 0% (GaN). In this configuration, AlGaN layers with lower Al content have a larger lattice constant that the AlGaN material beneath, and the pseudomorphic growth of the former forces them to be compressed. Because of the finite composition range of the AlGaN and the presence of strain relaxation effects, the maximum layer thickness that can be deposited in this way is limited to 6–7 μm.

An alternative approach consists of the use of the so-called low-temperature AlN interlayers. Here the GaN layer growth is repeatedly interrupted to introduce a thin AlN layer that is grown at very low temperatures (e.g., 700 °C). In these conditions, the AlN will not build up strain internally because of the even further reduced surface mobility, and it very quickly relaxes to its native in-plane lattice constant (3.11 Å) which is lower than the one of the GaN (3.19 Å). Then, in a next step under "normal" growth conditions, the growth of the GaN is continued and generates compressive strain in a similar way as described above. This process can be repeated several times. The main drawback of this approach is the poor quality of the AlN interlayers themselves (due to the low growth temperature) which can impact the electrical behavior of the layer stack, for instance, in terms of leakage current or trapping effects.

The second alternative approach which is today widely employed for high voltage power switching applications is the use of strained superlattice (SSL) buffers. These consist of a large number of repetitions (e.g., 100–150 times) of a bilayer made up out of 5–20 nm thin AlN and (Al)GaN layers. By keeping the thicknesses of the individual layers below their critical thickness, the total strain of the superlattice can be controlled by varying the ratio between the thicknesses of the two constituent layers.

15.1.5 Back-Barrier Selection

Besides the chemical and mechanical considerations, the layers below the HEMT heterostructure also play an important electrical role. This is obviously the case in the devices' off-state, where the electric field extends into and causes a depletion of the buffer layers where it induces electrical stress that may lead to leakage and time-dependent breakdown effects. However, the presence of traps in the buffer layers can also lead to a degradation of the devices' on-state behavior: the so-called current collapse (see further, e.g., Figs. 15.8 and 15.9). The electrical requirements for the buffer layers directly under the GaN channel layer also depend on the application.

GaN-on-Si is attracting a lot of interest for power switching applications especially for devices rated at 600 V or 650 V. One of the requirements of the circuit designers is that there are no floating potential nodes, which implies that also the substrate is grounded. As a result the GaN-on-Si stack has to be capable of handling about twice the rated voltage to be able to cope with inductive voltage spikes and to guarantee a reasonable lifetime. The total voltage is split over the strain

management layers (that are typically designed with only the strain aspect in mind) and over the voltage blocking layers.

One attractive implementation for the voltage blocking layers is to use impurity-doped GaN. One can for instance increase the resistivity of GaN by incorporating deep acceptor levels in the form of Carbon-doping. In an MOCVD process, carbon is available from the source molecules for the group III elements (e.g., from methyl groups), so by modifying the thermodynamic growth conditions, the amount of Carbon that is incorporated in the epilayers can be tuned. Alternatively, one can opt for a dedicated dopant source gas for carbon, such as ethylene or methane, to allow a wider parameter space for the epitaxial conditions. Substantial amounts of work have been performed by various groups to understand and control the effect of such Carbon doping. Moens et al. showed that a layer stack as described above can be modelled as a leaky dielectric [9], with two regimes of current conduction below and above a certain critical voltage. One concern with deep acceptor levels is that they may serve as a trapping state causing current collapse. Also in this respect, different models have been proposed. Uren et al. showed the importance of charge redistribution between the 2DEG and the carbon-doped layer [10], while Verzellesi et al. [11] described the effect of how the carbon is incorporated into the crystal lattice on its trapping behavior.

For RF applications, one of the main device features is the use of short gate lengths which create very high electric field peaks at the drain edge of the gate that can cause punch-through [12]. When using a thick (i.e., more than 200–300 nm) unintentionally doped GaN channel layer with the gate pinched off, the 2DEG carriers may be pushed out of the quantum well and still travel from drain to source through the lower part of the GaN channel layer. This induces a bias-dependent off-state leakage current and a degradation of the sub-threshold slope. To prevent this effect, the carriers need to be better confined into the 2DEG quantum well by modifying the layer stack directly under the (thinned) GaN channel.

The most effective method, inspired by similar approaches in AlGaAs/GaAs HEMT technology, is the use of an AlGaN back-barrier just below the GaN channel layer. Even the use of AlGaN layers with Al content as low as 5% creates a very high-energy barrier for 2DEG electrons, based partly on the bandgap discontinuity but mostly on the polarization charge at the AlGaN/GaN back interface [13]. This makes the AlGaN back-barrier the most suitable configuration for very high frequency operation (e.g., W-band) where very short sub-100 nm gate lengths are used [14]. There is also a major drawback: the thermal conductivity of ternary AlGaN alloys is significantly lower than that of either GaN or AlN [15], so for a given power dissipation, the peak channel temperature will be significantly higher than in the case of using GaN-based confinement layers.

To limit the punch-through effect in thick GaN channel layers, one method is to use Fe-doping to compensate for the intrinsic n-type background of GaN material. Fe is a deep acceptor in GaN that makes the layer highly resistive. Fe-doped GaN buffers are the de facto standard for GaN on SiC epiwafers used for RF applications. However, iron is not allowed in Si CMOS processing foundries where Fe contamination levels should be below $5 \times 10^{10}/\text{cm}^2$, which severely limits its usefulness for GaN-on-Si wafers. Fe also has a long diffusion tail in GaN, making it impossible to make abrupt interfaces between the Fe-doped buffer and the UID GaN channel layer. Finally, there are some reports that link Fe-doping with a trap with activation energy of approximately 0.6 eV [16].

Triggered by the promising results and understanding obtained for power switching, the use of carbon-doped buffers is also being introduced for RF applications. On a device level, the impact of the buffer is evaluated mainly in terms of off-state leakage and subthreshold behavior, the absence of current collapse and the capability to dissipate large power densities. Carbon-doped GaN confinement layers have been compared directly to AlGaN back-barrier designs with favorable outcome [17].

15.1.6 HEMT Heterostructures

Even though the above explains the importance of the nucleation and buffer layers, it is obvious that in GaN epiwafers for electronics an important role is reserved for the channel and barrier layers of the HEMT heterostructure. The underlying physics behind the formation of the 2DEG in such structures are reviewed in Sect. 15.2 of this chapter and have also been described in an excellent way elsewhere [3].

The work-horse heterostructure both for power switching and RF applications is still the combination of a thin AlGaN barrier layer on top of a GaN channel layer. The thickness of the barrier layer typically ranges from 10 to 30 nm, with Aluminum content between 15% and 30%. This yields a two-dimensional electron gas with an electron density of between $6 \times 10^{12}/\text{cm}^2$ and $1.5 \times 10^{13}/\text{cm}^2$ and associated electron mobility above 1800 cm^2/Vs. The fine-tuning of the structural parameters depends on a wide range of criteria and applications such as maximized electron mobility, improved reliability [18], or reduced electron density to allow e-mode operation through the local depletion of the channel by a p-type (Al)GaN layer under the gate [19].

The AlGaN/GaN heterostructure benefits from a piezoelectric polarization component that adds up to the spontaneous polarization field of the AlGaN layer. As a result, adding more strain to the AlGaN layer by increasing the Aluminum content is beneficial for the number of carriers that are contained in the 2DEG. However during epitaxy,

a growing strained layer only remains pseudomorphic to the underlying lattice until a so-called critical thickness is reached [20, 21] after which the strained layer starts to relax, e.g., by the creation of misfit dislocations [22]. It was shown that for AlGaN/GaN heterostructures, strain relaxation can also occur by the formation of V-grooves in the AlGaN layer, caused by the preferential out-diffusion of Gallium from the ternary material [23]. By adding a thin layer of SiN during the epitaxy, this mechanism can be suppressed and the relaxation temporarily postponed [24] until another relaxation mechanism sets in. Thus, not only does in-situ SiN provide a rather effective surface passivation [25], it also allows for the epitaxial growth of aluminum-rich AlGaN barriers.

The most extreme case of this barrier configuration consists of a pure AlN barrier layer grown on top of the GaN channel layer, as AlN has the widest bandgap and the highest polarization coefficients of the InAlGaN alloys, making it theoretically the best choice for the HEMT heterostructure. As an example, an AlN barrier layer with a thickness of only 4 nm capped with 10 nm of in situ SiN yields a 2DEG density of $2.15 \times 10^{13}/\text{cm}^2$ with an associated electron mobility of about 1000 cm^2/Vs. These data points make this structure very interesting for RF purposes because it allows bringing the gate electrode very close to a densely populated 2DEG, which results in a much improved transconductance of the transistor [26].

One drawback of using AlGaN barrier layers is that the use of strained barrier layers may have a detrimental effect on device reliability [27]. Fortunately, it is also possible to create strain-free HEMT heterostructures, by combining the GaN channel with a lattice-matched InAlN barrier layer [28]. For an indium composition of about 17%, InAlN has the same lattice constant as GaN but a significantly higher bandgap energy of 4.4 eV. Because both InN and AlN have higher polarization fields than GaN, a 2DEG is still induced at the interface between InAlN barrier and GaN channel due to spontaneous polarization only. For example, for a lattice-matched InAlN barrier layer with a thickness of 6 nm with thin cap of SiN, the authors have obtained a 2DEG density of $1.65 \times 10^{13}/\text{cm}^2$, which is about 50% higher than for a standard 20 nm $Al_{25}Ga_{75}N$ barrier layer. One remarkable property is that the electron mobility in this InAlN/GaN heterostructure is as high with a value of 1800 cm^2/Vs, much higher than what can be obtained with the AlN barriers with values around 1000 cm^2/Vs. As a result, InAlN have the lowest sheet resistance of any HEMT configuration, in this case around 220 Ω/sq. compared to typical values of 350 Ω/sq. or above for AlGaN-based heterostructures. Values as low as 170 Ω/sq. have been reported for thicker InAlN barriers [29].

Recently, a new nitride alloy ScAlN was proposed as an alternative barrier material [30]. Even though results are still scarce, an 2DEG electron density of $3 \times 10^{13}/\text{cm}^2$ was reported for layer structures grown by MBE [31].

15.2 Lateral Devices Architectures

The first lateral gallium nitride device was reported for microwave applications in the late 1990s [32]. Subsequently, RF architectures expertize has been basically adapted for power and switching applications because of their high off-state breakdown strength combined with an excellent channel conductivity. These GaN-based switches would offer greater efficiency, power handling, and other performance attributes compared to the well-established, widely available silicon MOSFET power devices. The superior electron mobility means that a GaN transistor will have a smaller size for a given on-resistance and breakdown voltage than a silicon (Si) semiconductor. Thus, GaN also offers extremely fast switching speed and excellent reverse-recovery performance, critical for low-loss, high-efficiency performance. Furthermore, despite their large lattice mismatch (about 14%), high-quality GaN growth can be achieved on cost-effective Si substrate using advanced techniques to accommodate the strain issues. Although GaN on SiC substrates are generally advantageous for high power devices because of the high thermal conductivity and lower lattice mismatch, the growth on Si substrates is more promising for power applications because of the scalability of wafer diameters to 200 mm and more and due to the comparably low price level. The ability of power semiconductor devices to enhance the power electronics performance/cost figure of merit can be simplified by its own price/performance figure of merit, namely, dependent on the switching power loss, ohmic power loss, and the cost, where the switching power loss reflects the thermal limitation, most often achieved through increasing switching frequency and subsequent reduction in output filter components. Therefore, in addition to efficiency improvements, the use of GaN semiconductors instead of state of the art silicon-based devices for power electronic systems allows the reduction of size/weight of the conversion subsystems, due to significant reduction in cooling system requirements.

The structure of a common AlGaN/GaN high electron mobility transistor (HEMT) appears in Fig. 15.2 along with the band diagram. At the heterojunction between the AlGaN barrier and the GaN channel, the two materials discontinuity in polarization leads to carrier diffusion. The AlGaN free electrons are attracted to the GaN channel and create an accumulation of charges at the interface of both layers. At the thermodynamic equilibrium, a discontinuity of the conduction band at the AlGaN/GaN interface is observed. This discontinuity forms triangular potential well. Confine in a very small area, those electrons create a two-dimensional electron gas (2DEG) enabling a high charge density conduction between

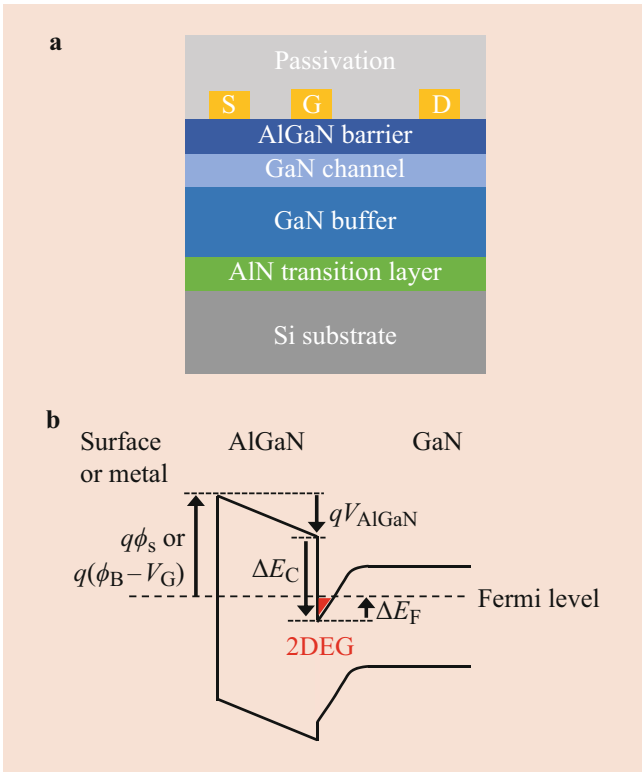

Fig. 15.2 (**a**) Cross section of an AlGaN/GaN HEMT associated with (**b**) his band diagram

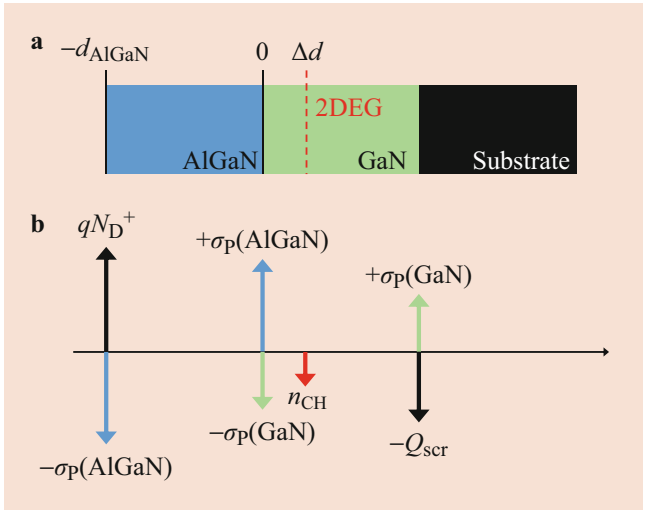

Fig. 15.3 (**a**) Schematic structure of a GaN HEMT for the calculation of the channel charge density and (**b**) charge distribution in the device. The AlN transition layer is not considered for easier understanding

the drain and the source. Unlike GaAs HEMTs, GaN HEMTs do not require any electron doping to create the 2DEG at the interface between the barrier and the channel. Indeed, the creation of the 2DEG is the result of the piezoelectric and spontaneous polarizations inherent of the AlGaN/GaN heterostructure. The electron density in the 2DEG is directly dependent on the nature and the thickness of the material used as barrier layer [33, 34]. The high electron confinement at the interface allows reducing the electron scattering, which leads to an electron mobility typically ranging from 900 and 2200 cm^2/Vs [35, 36].

In more detail, all the contributions leading to the formation of the channel can be computed as follows, referring to Fig. 15.3a for the device structure and dimensions, to Fig. 15.3b for the charge distribution and to Fig. 15.2b for the band diagram, and assuming Ga-face polarity. For thick AlGaN layers, the surface potential $q\phi_s$ is pinned by the surface donor levels located at the upper barrier surface and is almost equivalent to the donor energy depth E_D. Due to the lattice mismatch between AlGaN, and GaN, the thinner AlGaN barrier is submitted to tensile strain; therefore the total polarization charge $-\sigma_P$(AlGaN) at the AlGaN surface is the sum of the spontaneous polarization $-\sigma_{SP}$(AlGaN) and piezoelectric polarization $-\sigma_{PE}$(AlGaN) contribution

$$-\sigma_P\,(\text{AlGaN}) = -\sigma_{SP}\,(\text{AlGaN}) - \sigma_{PE}\,(\text{AlGaN}) \qquad (15.1)$$

An additional positive charge contribution N_D^+ is present at the surface, caused by the unscreened fixed positive charge left by the ionized donors. If the AlGaN layer is thick enough, the Fermi level will reach the donor state level, and the electrons will be stimulated into the conductive band and swiped toward the other side by the force of the polarization-induced electric field. Once contacting with a GaN layer, electrons will flow into the GaN side because of the drop of the Fermi level. The electrons will accumulate at the interface and contribute to the formation of the 2DEG. At the interface between the barrier and the channel region, the net polarization charge $-\sigma_{P,}$(net) is the sum of the contribution by the AlGaN and the GaN layers, σ_P(AlGaN) and $-\sigma_P$(GaN), respectively,

$$\sigma_P\,(\text{net}) = \sigma_P\,(\text{AlGaN}) - \sigma_P\,(\text{GaN}) \qquad (15.2)$$

Given the stronger spontaneous polarization field in AlGaN with respect to GaN, the net charge is a positive number. This positive net charge leads to the presence of an electron distribution in the channel region close to the hetero-interface. We assume that this charge density qn_{CH} is distributed as a two-dimensional charge layer at a distance Δd from the AlGaN/GaN interface, where Δd is the center of the charge distribution. Starting from the AlGaN surface, we can follow the profile of the lower edge of the conduction band from the Fermi level in the metal to the Fermi level in the GaN buffer and write

$$\phi_s - V_{AlGaN} - \frac{\Delta E_C}{q} + \frac{\Delta E_F}{q} = 0 \tag{15.3}$$

where ΔE_C is the conduction band energy discontinuity at the hetero-interface, ΔE_F the distance between the Fermi level and the lower edge of the conduction band at the interface, and V_{AlGaN} the potential across the AlGaN region

$$V_{AlGaN} = \frac{\left|\sigma_P\,(\text{net}) - qn_{CH}\right| \cdot d_{AlGaN}}{\varepsilon} \tag{15.4}$$

ΔE_F can be expressed as

$$\Delta E_F = \frac{qn_{CH}}{\varepsilon} \cdot \Delta d \tag{15.5}$$

The electron channel density n_{CH} is then

$$n_{CH} = \frac{\sigma_P\,(\text{net}) \cdot d_{AlGaN} - \varepsilon(\phi_s - \Delta E_C/q)}{qD} \tag{15.6}$$

where

$$D = d_{AlGaN} + \Delta d \tag{15.7}$$

is the distance between the AlGaN surface and the channel location. In a complete HEMT structure, a gate metal is deposed on top of the AlGaN barrier, which can be used to vary the AlGaN surface potential. When a bias V_G is applied to the gate contact, the surface potential ϕ_s equals $\phi_B - V_G$, where ϕ_B is the barrier height of the metal-semiconductor junction, and therefore we obtain

$$n_{CH}\,(V_G) = \frac{\sigma_P\,(\text{net}) \cdot d_{AlGaN} - \varepsilon\,(\phi_B - V_G - \Delta E_C/q)}{qD} \tag{15.8}$$

Concluding, at the interface between the gallium nitride buffer and the substrate, we have the positive polarization charge of the gallium nitride $+\sigma_P$(GaN) and an additional screening charge $-Q_{scr}$ to ensure charge neutrality in the full structure.

The high electron mobility combined to the high density of charges in the 2DEG enable very low on-state resistances (R_{ON}). Up to 650 V voltage range, GaN devices can thus be foreseen as the best choice as compared its counterparts considering a proven high level of reliability. At higher-voltage operation, this technology is basically limited by the Si substrate. This limitation will be detailed later in this chapter. However, increasing the blocking voltage of GaN lateral devices would pave the way for more efficient devices beyond 1 kV applications [37, 38].

15.2.1 Applications

Silicon-based devices such as MOSFETs (Metal-Oxide-Semiconductor Field Effect Transistor) or IGBTs (Insulated-Gate Bipolar Transistor) have been extremely successful and represent the present standard for power switches in power applications – AC/DC supplies, DC/DC supplies, and motor controls – ranging from just tens of watts up to hundreds and even thousands of watts. They have seen continual improvements in key parameters such as on-resistance $R_{DS(ON)}$, voltage ratings, switching speed, packaging, and other attributes. However, the rate of improvements in these MOSFETs has leveled off, as their performance is now close to the theoretical limit as determined by the underlying fundamental physics of these materials and processes. In this frame, GaN lateral devices have a growing impact on the current power market. Indeed, due to its impressive intrinsic characteristics (shown Fig. 15.4), GaN material has a truly predisposition for high-voltage and high-speed switching applications as confirmed by many market reports for low and mid-voltage range (<600 V) in a short term.

GaN could impact a wide range of applications using various operating voltage. For instance, GaN presents a unique palette of viable solutions for both high power and medium power applications that can power the next generation cars efficiently and economically. Hybrid vehicles represent today a growing market where companies are significantly investing. The emergence of wireless power is another key application enabled by GaN. Eventually, the entire home can be equipped with transmitters and repeaters that will power the lights, TV, and other household appliances wirelessly. GaN transistors will support this rapidly emerging application. Another good example is the use of GaN components in an extremely small x-ray machine that fits in the size of a pill. In this case, GaN's superior performance to obtain 10–100 times higher resolution so diseases can be detected earlier, more accurately and less expensively. Also, in addition to its ability to survive in a harsh environment, the small size, and high efficiency of GaN device make them very attractive for use in space application. GaN is inherently radiation tolerant. Unlike silicon, where special fabrication techniques and special packaging is needed to shield semiconductors from the effects of radiation, GaN's natural properties make it relatively immune to these harmful rays.

15.2.2 State-of-the-Art

The specific on-state resistance of any semiconductor devices used for power electronic applications is one of the key performance parameters. An ideal power switching device should have a high breakdown voltage to cope for the off-state condition with a sufficient margin while its on-state

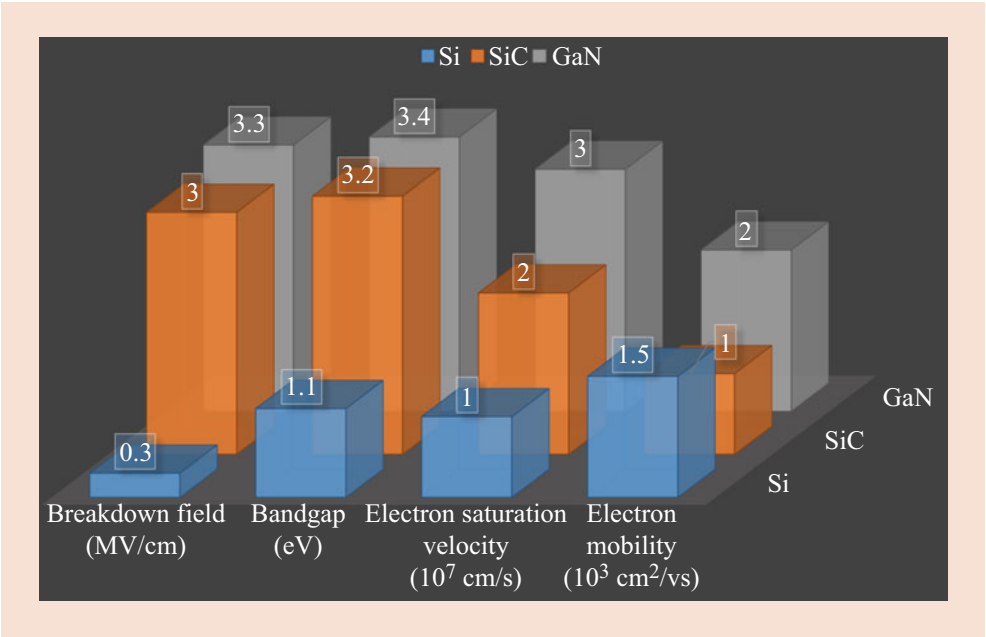

Fig. 15.4 Comparison of intrinsic characteristics of GaN, Si, and SiC material

resistance should be as small as possible. This request translates into the trade-off situation depicted in Fig. 15.4. High breakdown devices require extended drift regions, e.g., the distance between gate and drain needs to be sufficiently large. This means that the increase of the breakdown voltage induces resistive elements that are added to the device thus increasing the on-state resistance. As shown in Fig. 15.5, the optimum on-state resistance for each types of devices follows specific theoretical limits, which have been calculated for unipolar devices. In fact, as power switching devices are operated in the linear (mobility controlled) region at on-state, the on-state resistance increases with breakdown voltage practically in a quadratic dependency. Accordingly, GaN devices have an advantage over Si devices by theoretically at least three orders of magnitude. They even outperform SiC devices.

It can be noticed that many large companies are devoted to the development of GaN power devices. A wide range of commercial GaN power devices are already commercialized. This reflects the potential short-term market penetration of these emerging devices. Nevertheless, several hurdles still need to be overcome such as the cost that needs to be reduced in order to be competitive with Si-based devices while delivering superior performance; the reliability of normally-off GaN devices and in particular the control of the dynamic on-resistance up to high temperature; the integration and associated packaging that needs to be implemented without sacrificing the performances; and the sourcing that needs to be increased to allow high acceptance of this technology from the industry. Furthermore, higher voltage range (>1.2 kV), limited currently to below 1 kV would extend the impact of GaN lateral devices for power applications.

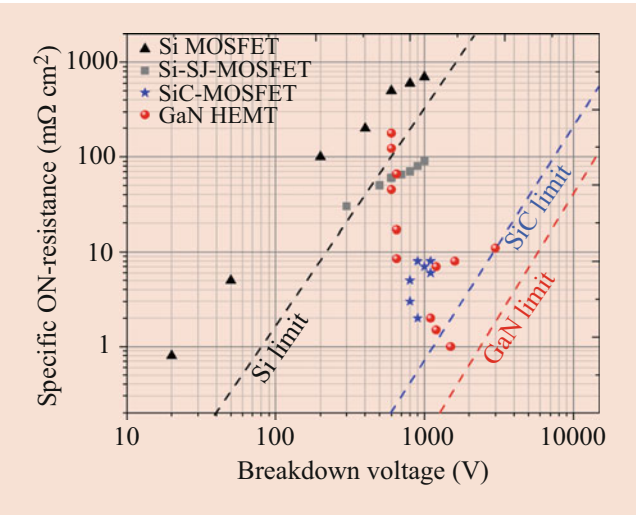

Fig. 15.5 Specific on-resistance as a function of the breakdown voltage of various materials

15.2.3 Limitations of GaN Lateral Devices

As discussed previously, GaN lateral devices are already showing attractive performances as compared to silicon technology [39–41]. However, the operating voltage of GaN devices is limited to below 1 kV, which is significantly lower

than the full potential of this technology. One of the main technological bottlenecks include:

- The parasitic conduction at the buffer/Si substrate interface under high voltage
- The dynamic R_{ON} issues
- The normally-on behavior

Parasitic Conduction Under High Voltage

Many different physical effects are limiting the high voltage performance of GaN devices. They all have to be taken into account when developing high voltage GaN devices. The breakdown voltage is often defined as the voltage level at which the drain current of the pinched-off transistors is exceeding a normalized value of 1 μA per mm device width. The main sources of leakage for an AlGaN/GaN HEMT device are represented in Fig. 15.6. Device breakdown mainly depends on the specific epitaxial design of the buffer layer, its material quality, the lateral geometrical design of the devices, and their passivation technique. The latter issues are mainly dependent on processing technology, whereas the former parameters are due to the GaN/AlGaN epitaxial design, the material properties and the interfacing between GaN/AlGaN material technologies and processing. Some mechanisms, for example, surface arcing between adjacent conductive structures with a large potential difference are known from standard power electronic device technologies.

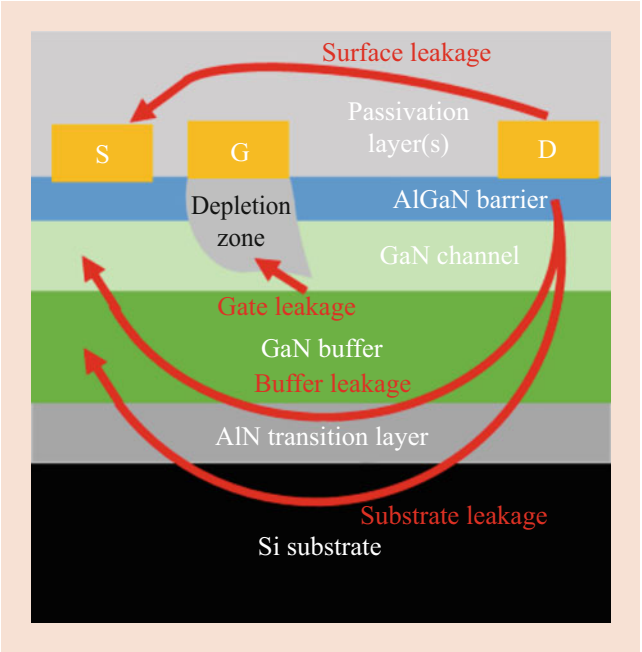

Fig. 15.6 Representation of the main sources of leakage for a HEMT AlGaN/GaN device on Si substrate

These mechanisms can be harnessed by applying adapted passivation and encapsulation schemes.

Buffer leakage current is due to the injection of charge carriers into the buffer under high bias. This phenomenon is commonly called punch-through effects [42]. In this case, if the channel is closed by a sufficiently negative gate bias, electrons are bypassing the gate control region via the buffer. Several solutions have been developed to overcome this issue by the use for instance of carbon or Fe-doped buffer [44–45] or an AlGaN back barrier [46].

In off-state condition, the gate polarization creates a large depletion region, and the electrons can flow from the gate to the drain, most probably due to electron injection across the gate barrier. As these effects are triggered by high electric field strength, particularly at the drain side edge of the gate or close to the drain electrode, field plates can suppress this effect and thus shift the breakdown voltage to higher values.

A strong limitation of GaN lateral devices grown on silicon substrate is the parasitic conduction at the buffer/Si substrate interface under high voltage. Figure 15.7 shows the breakdown voltage (BV) defined for a leakage current of 1 μA/mm, for various epitaxial thicknesses as a function of the gate-drain voltage distance (L_{GD}). If the leakage currents are suppressed by suitable technological means, GaN HEMTs BV scales with increasing L_{GD}. Thus, L_{GD} determines the maximum allowable operation voltage. For small L_{GD} (typically <15 μm), the breakdown voltage monotonically increases, generally indicating a breakdown mechanism that is triggered by properties directly influenced by L_{GD} scaling. In this case, breakdown occurs between the drain side edge of the gate and the channel region with a simultaneous increase of gate and drain current. On the other hand, for higher L_{GD}, BV saturates with respect to the epitaxial total thickness. Detailed investigations have shown that the dominating current flow at breakdown condition is now originating from the source, flowing vertically through the buffer to the conductive substrate and back to the drain terminal.

Therefore, increasing the epitaxial thickness allows improving BV. However, buffer thickness typically above 6–7 μm with low bow is extremely difficult to achieve on large wafer diameters and often leads to higher defect density and eventually cracks. Another way to reduce the parasitic conduction at the buffer/Si substrate interface [48–50] is to locally remove the substrate and subsequently replace by a wider bandgap material. This approach will be described later in this chapter.

Dynamic R_{ON} Issues

GaN-based power transistors can only gain market acceptance if they demonstrate switching properties superior to

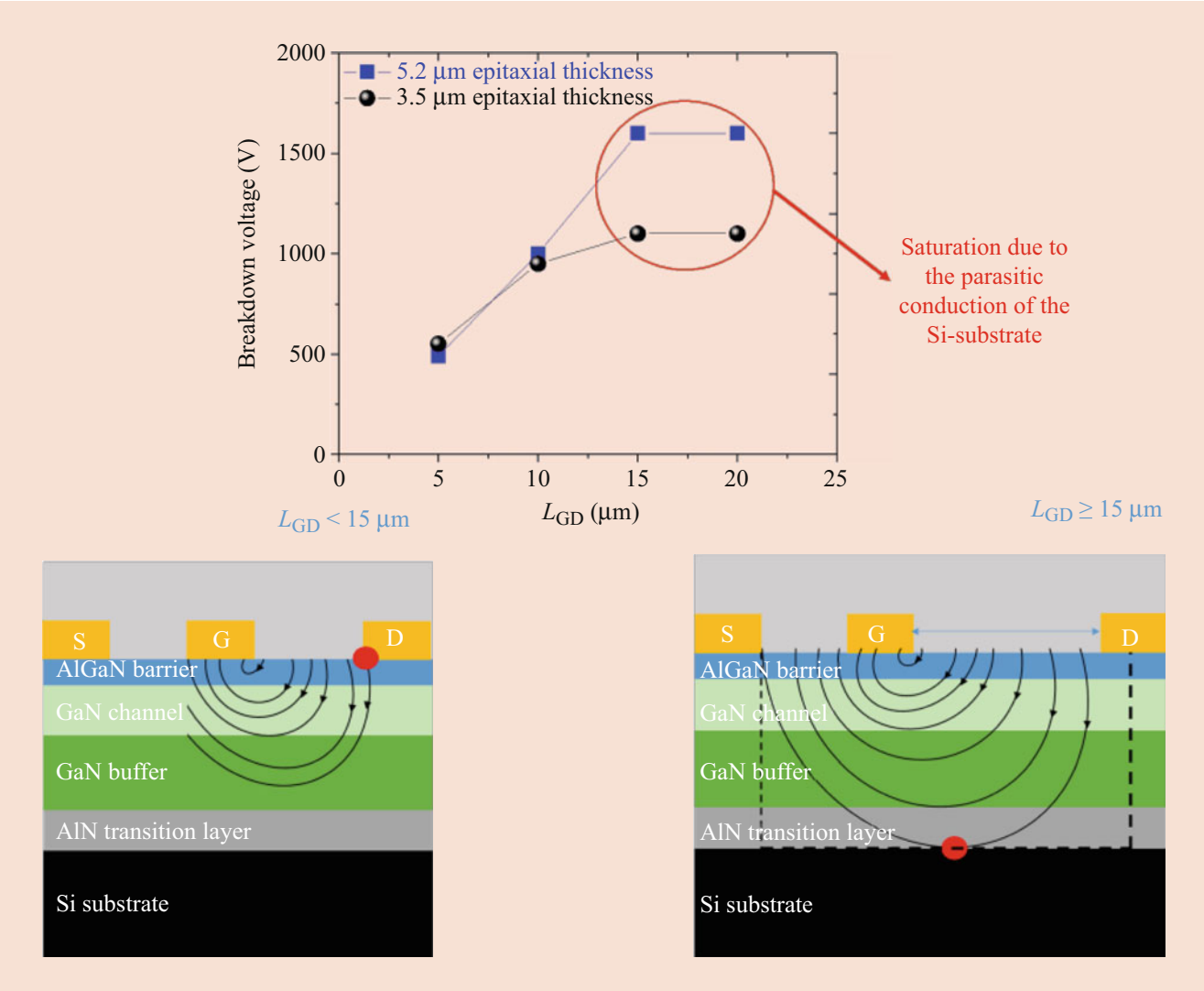

Fig. 15.7 Breakdown voltage comparison of AlGaN/GaN HEMTs with various epitaxial thicknesses as a function of the gate-drain distance [47]

competing technologies. Due to trapping effects the static on-state resistance R_{on_stat} may increase upon dynamic switching of the device leading to a degraded dynamic on-state resistance (R_{on_dyn}). This effect is also known from GaN microwave transistors. As power switching devices are never driven into saturation for most of the switching sequence (only dynamically during a switching event), the dynamic change of the on-state resistance is taken as a criterion to quantify the dynamic trapping effects. As shown in Fig. 15.8, this parasitic effect can cause a strong degradation of the dynamic on-state resistance, which often scales with device switching voltage and thus significantly challenges high voltage GaN switching applications.

The trapping effects in the device structure responsible of the degradation of the dynamic R_{ON} are commonly represented by negative electric charges located in different areas: near the surface (usually process induced) and into the buffer layers (poor interface quality, doping compensation, etc.) [52–53]. Figure 15.9 depicts the mechanism of the traps and the degradation of the dynamic R_{ON} during switching. Trapping can take place at various places, in the epitaxial layers, at passivation semiconductor interfaces or even at interfaces between different passivation layers. In consequence, electron transport in the channel region immediately after switching from one condition to another is impeded by negatively charged traps until they are emptied. This leads to increased switching losses, reduced system efficiency, and explains time dependence of R_{on_dyn}. An optimized buffer design avoiding deep trapping with a proper surface passivation and the use of field plates to spread the peak electric field are some essential countermeasures towards optimized power switching.

15.2.4 Pushing the Limits of Lateral GaN Devices: Enhancement of the Blocking Voltage

One of the main challenges with GaN-on-Si lateral devices is the enhancement of the blocking voltage. Several parameters still limit today the device operation for higher voltage (silicon substrate, epitaxial structure thickness). One way to increase the breakdown is the use of thicker buffer layers. Advanced architectures based on AlN/GaN superlattices or thick (up to 7 μm) quasi-carbon-free buffer combined with strain-management interlayers have been developed successfully. A key point is that regardless of the chosen approach, buffer trapping should be avoided.

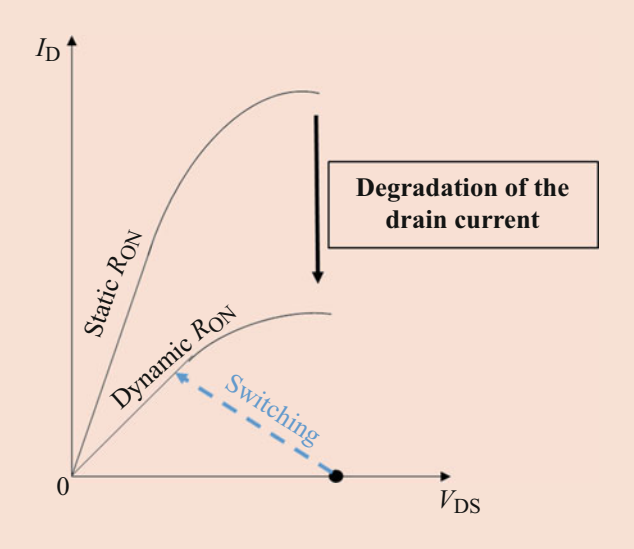

Fig. 15.8 Degradation of the dynamic R_{ON} during switching of a GaN HEMT

An example of electrical characteristics from a thick and excellent buffer crystal quality showing low leakage current and state-of-the-art vertical breakdown voltage above 1400 V (~2 MV/cm) appears in Fig. 15.10 [54]. Furthermore, substrate ramp measurements reveal very low trapping effects up to 1.2 kV (Fig. 15.10b. It has been indeed shown that ramping the substrate to a high (negative) potential allows to reproduce the off-state operation under the drain contact in a transistor. In this case, any buffer charge trapping or storage will be visible in the substrate ramp characteristics.

Another promising solution to increase the blocking voltage of GaN-on-Si lateral devices is the local substrate removal (LSR). This method consists in a selective silicon substrate removal around the device and subsequent replacement by an ultra-wide bandgap followed by a backside metallization [49] as described in Fig. 15.11.

Aluminum nitride (AlN) deposited by PVD is a promising dielectric in this frame since it has a low mismatch with the nucleation layers, a significant breakdown field above 4 MV/cm and offers a cost effective manufacturing technology scalable to large wafer diameter [55]. The LSR

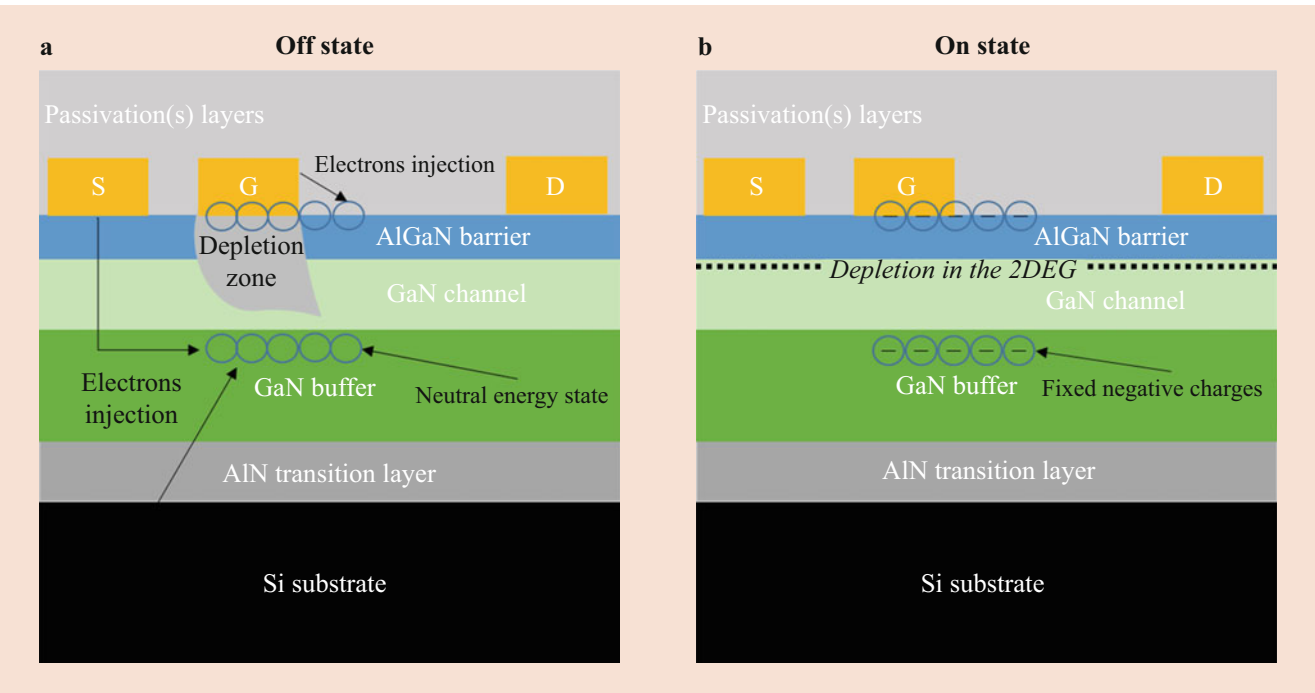

Fig. 15.9 Illustration of the influence of the trapping effect on the R_{ON} of a GaN HEMT during switching (**a**) off state (**b**) on state

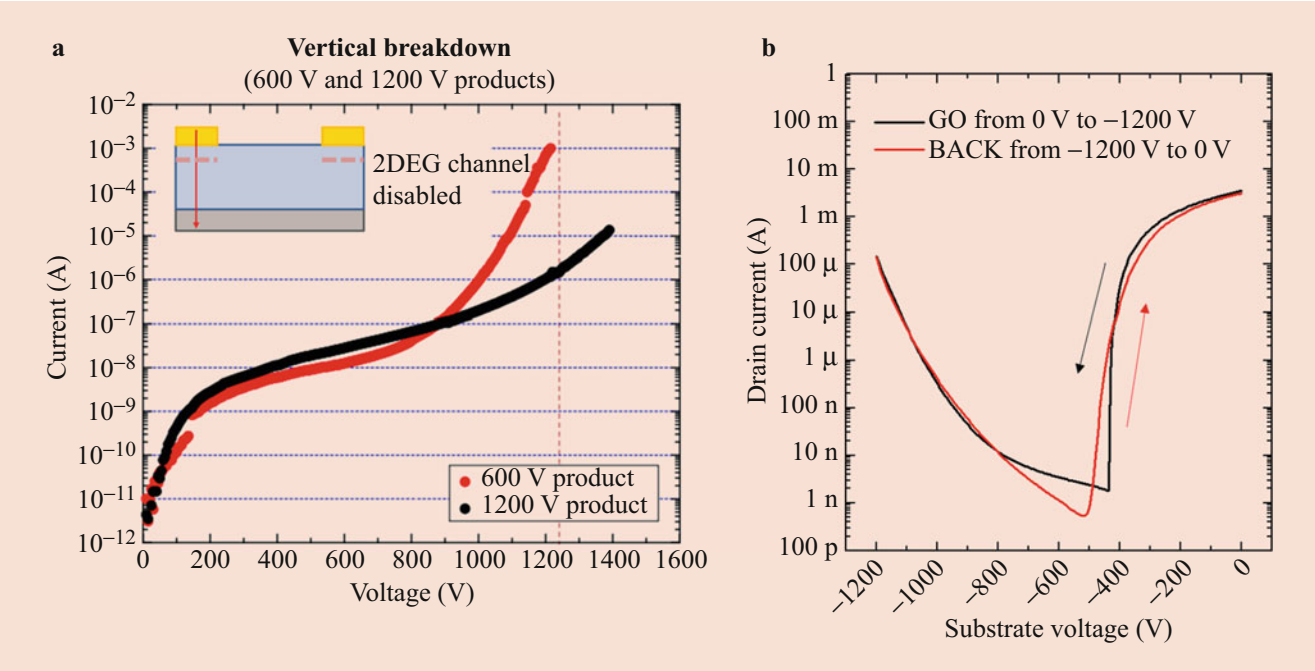

Fig. 15.10 (**a**) Vertical breakdown voltage and (**b**) substrate ramp measurement up to 1.2 kV of GaN-based heterostructure

technique combined with 15 µm thick AlN layer resulted in state-of-the-art GaN-based HEMTs with remarkably low off-state leakage current (<1 µA/mm) beyond 3 kV while maintaining a low specific on-resistance about 10 mΩ.cm^2 (Fig. 15.12). The comparison of these devices without LSR confirms that the drain leakage current flows essentially at the AlN nucleation layer/Si substrate interface. Furthermore, significant recovery of the maximum current density after the backside metallization enabled to reduce the self-heating. It can also be pointed out that this approach do not induce additional charge trapping. The integrity of a trap-free buffer is thus not affected by the substrate removal while extending significantly the bias operation capability.

15.2.5 Normally-Off GaN Lateral Devices

Normally-off configuration is an essential prerequisite for power applications in order to reduce the power consumption and keep a simple gate drive configuration. Many approaches have been demonstrated toward normally-off GaN lateral transistors. The general approach is to shift the conduction band of the channel region controlled by the gate above the Fermi level at zero gate bias and thus to obtain a positive threshold voltage. For power applications threshold voltage (V_{TH}) ranges above +1 V are desirable to ensure safe operation conditions, while the on-state resistance should be kept as low as possible.

MISHEMTs

The main advantage of the MISHEMT (*Metal Insulator Semiconductor HEMT*) structure is that a high threshold voltage levels can be obtained. A gate recessing is combined with gate dielectric isolator techniques to avoid gate leakage increase (Fig. 15.13). However, interface charges subsequent to the gate recess etching and dielectric deposition still plague this type of devices. The choice of the insulator has a strong impact on the interface traps. For instance, some studies showed that the use Al_2O_3 induces negative charges, while HfO_2 gives rise to positive charges [56].

F$^-$ Ion Implant under the Gate

Another possibility to achieve normally-off operation on a GaN HEMT is the use of ion implantation by plasma Fig. 15.14. This method was first demonstrated in 2006 [57] showing positive V_{TH}. The fluorine F$^-$ ion implantation into the AlGaN barrier layer localized under the gate makes use of the natural strong electronegativity of the F$^-$ ion to deplete the DEG as charge neutrality is ensured. A trade-off between the mobility/R_{ON} degradation and higher V_{TH} positive shift exists depending on the plasma condition such as time and power used. Furthermore, the device reliability under high voltage still needs to be demonstrated for this approach. For instance, several groups have shown a strong dependence of the amount of fluorine ion implantation on the increase of the current collapse and the annealing temperature [58] leading to a threshold voltage instability.

Fig. 15.11 Cross section describing the fabrication of the local substrate removal approach

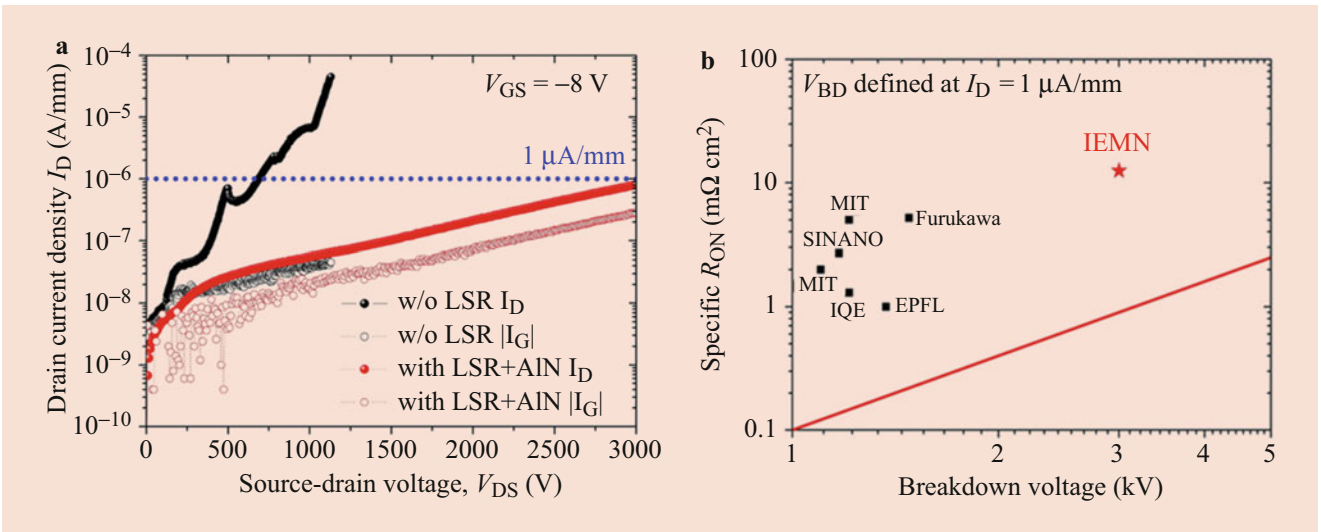

Fig. 15.12 (**a**) Off-state leakage current characteristics of AlGaN/GaN MISHEMTs with and without LSR/thick AlN deposition. (**b**) Benchmark of GaN-on-Si HEMTs with blocking voltage defined at an off-state leakage current of 1 µA/mm. (Reprinted from E. Dogmus et al. [55] under the terms of the Creative Commons Attribution 4.0 license (CC-BY) http://creativecommons.org/licenses/by/4.0/)

The Cascode Circuit

Normally-off behavior can also be obtained by connecting a standard normally-off Si MOSFET optimized for low-voltage operation and a high-voltage GaN normally-on transistor in cascode configuration (Fig. 15.15). In this hybrid configuration, the Si MOSFET is used to control the GaN HEMT gate with only positive gate voltage through the Si MOSFET resulting in a normally-off overall behavior. On-state and off-state properties should be determined by the GaN device, whereas the normally-off property is due to the Si device. The packaged cascode configuration looks like a high-voltage normally-off transistor. It combines the advantages of a large gate threshold voltage and gate voltage swing (feature of the Si normally-off transistor), a high breakdown voltage and a comparably low on-state resistance related to the normally-on GaN HEMT. Combining these two devices brings several drawbacks: the input capacitance is determined by the Si-MOSFET and therefore comparably high slowing down the switching speed [59]. Furthermore, the Si MOSFET limits strongly the overall temperature operation offered by the GaN technology. Nevertheless, several manufacturers are pursuing the commercialization of the cascode design.

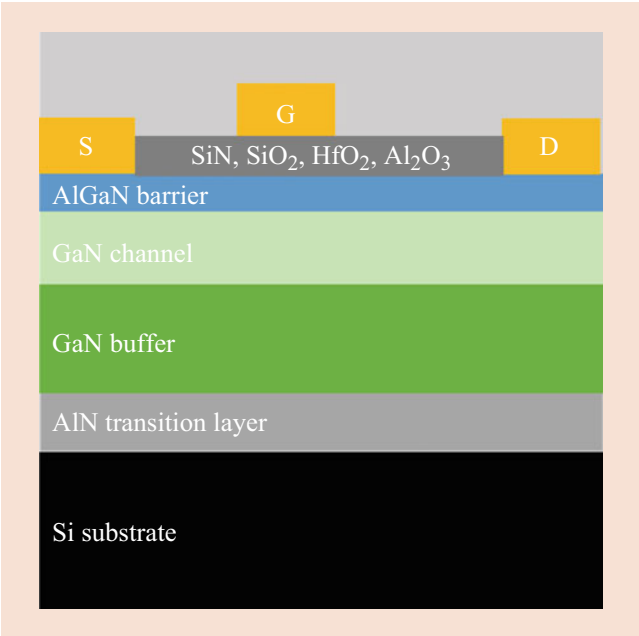

Fig. 15.13 Cross-session of a MISHEMT

P-GaN

The first demonstration of p-AlGaN or p-GaN under the gate in order to achieve normally-off operation has been realized by Panasonic in 2007 [60] despite the challenge of p-doping (Magnesium) of GaN material. Figure 15.16 describes the band diagrams with and without a p-GaN cap layer. At zero gate bias, the p-GaN layer is depleted leaving back a fixed negative charge which in turn depletes the channel. When the positive gate bias increases further, holes are injected into the pn heterojunction, which results in a higher drain current of the device.

In practice, a careful epilayer design needs to be used in order to achieve a positive threshold voltage. One of the key parameter is the concentration of Mg in the p-GaN layer. Some studies have shown that a concentration in the range of 2×10^{19} cm^{-3} is necessary [62] with a trade-off with defect density increase in the case of higher Mg concentration. A second important parameter to be considered is the Al content into the $Al_xGa_{1-x}N$ barrier layer. A lower electron density into the 2DEG resulting from a reduced Al content favors a stronger depletion and thus higher pinch-off voltage.

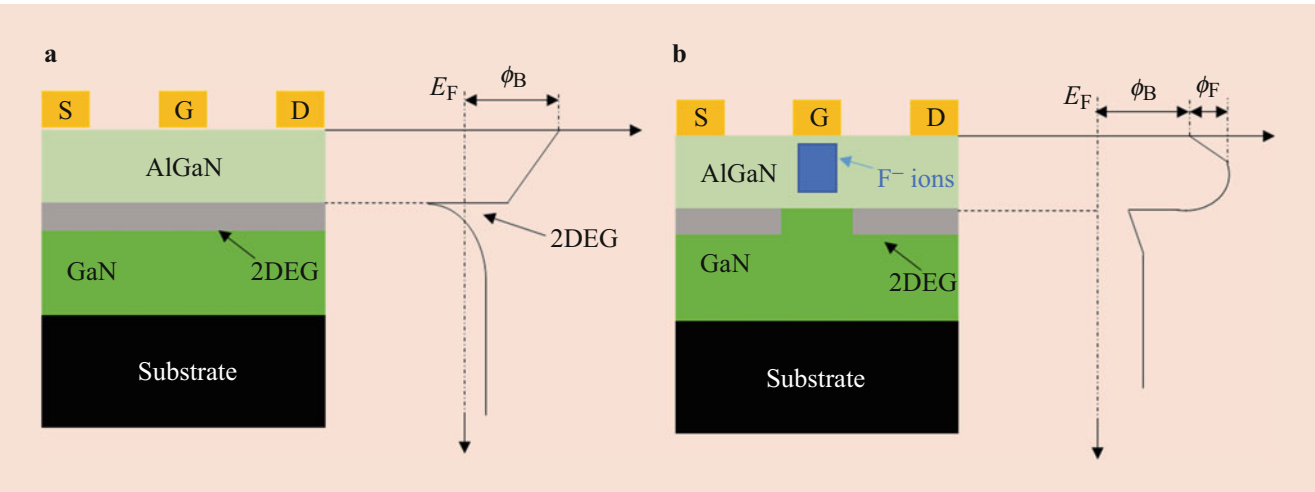

Fig. 15.14 Cross section of a conventional AlGaN/GaN HEMT and an AlGaN/GaN HEMT with F^- ion implant under the gate associated to their conduction band profiles

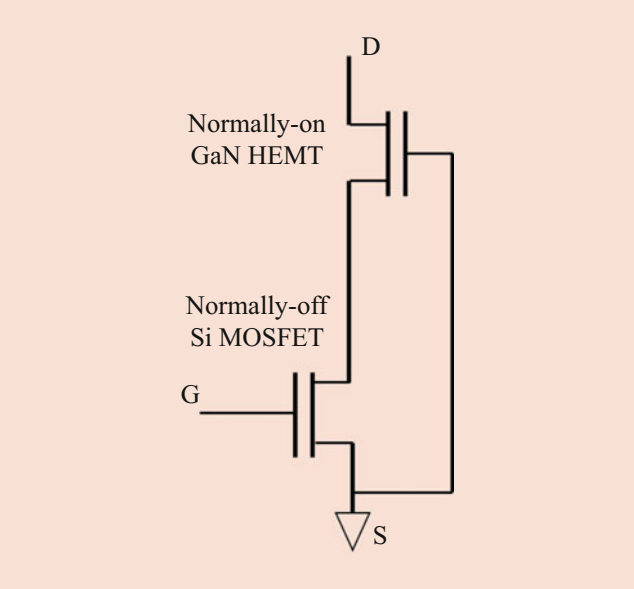

Fig. 15.15 Cascode type hybrid integration of GaN normally-on and Si normally-off device

Processing of GaN Lateral Devices

A conventional Schottky gate D-mode and p-GaN E-mode GaN HEMT device structures are schematically shown in Fig. 15.17. The process modules for the GaN HEMT device fabrication include the ohmic contact formation for source and drain, device isolation, p-GaN gate contact or MIS gate, surface passivation, and interconnects. The source and drain metal stacks facilitate the ohmic contacts. In order to avoid cross-contamination with Si processes in production lines, Au-free metallizations have to be used. The gate contact is deposited on top of a high-quality dielectric for the D-mode GaN HEMTs. In the case of E-mode, the p-GaN layer should be removed except under the gate area. The dry etching is widely used for this step. One of the key factors to achieve high performance device and high yield is the etching selectivity of GaN over AlGaN. The commonly used Cl_2/BCl_3 plasma results in a poor selectivity. Fluorine-based chemistry etching technique has been reported to provide better selectivity. The etching of compound semiconductor films containing Al can be optimized in Cl-based plasmas by adding F-containing gases. For instance, the BCl_3/SF_6 selective dry etching on AlGaN/GaN allows decreasing the AlGaN etching rate resulting from the formation of non-volatile AlF_3 residues on AlGaN surface. Actually, the AlF_3 reduces the etching efficiency of chlorine enabling a selective etching of GaN over AlGaN. To further enhance the etching selectivity, a thin AlN etch stop layer can be inserted between the p-GaN and AlGaN layers improving the V_{TH} uniformity. Finally, the surface passivation (especially of the sidewalls) plays a crucial role for proper device operation in order to prevent the current collapse and related large dynamic on-resistances.

Future Prospects

GaN power switching devices will play an important role in future power electronic applications due to their outstanding properties. With the continuous progress of manufacture technology, GaN power devices with high breakdown voltage, high temperature resistance, low conduction losses, and high output power should penetrate large markets soon. In particular, the increasing need of higher efficiency will make GaN devices extremely attractive. The collection of data shows that the newest generations of the emerging GaN power switching definitely outperform their Si competitors. It is now the time to convert prototype devices to highly mature industrial devices. Nevertheless, the better performance/cost ratio than available devices needs to be realized by proving their reliability to a large extend. Furthermore, higher switching frequency and higher operating temperatures translate indeed in smaller passive components and cooling systems, which would benefit any power applications. However, the main challenge will be the lack of passive components, advanced packaging technologies, and circuit designs for handling such small dies with their fast-switching characteristics at the converter level. This may postpone the introduction of GaN devices for some applications in a short term. On the other hand, in several applications (e.g., mobile applications in transportation systems, power supplies for notebooks, and communication units), there is a high pressure to reduce the power converter's size and weight while increasing the efficiency.

15.3 Vertical Devices Architectures

Power electronics is a highly discussed topic of our century. As we prepare ourselves to address the next-generation power requirements, we make a note of the changing landscape of power generation and delivery. With the rollout of renewables as sources for electricity, more and more electronics are getting connected to the source side and load side of our grid. The trend will only continue upwards. This suggests higher power device integration to the grid which to a device engineer translates to finding solutions that are power dense. Besides grid, there are several applications, extending from automotive to robotics and touching our daily lives, which require a more efficient power conversion unit. Every power conversion unit requires a solid-state switch to perform their job.

Silicon-based power electronics have served us well. However, it is time for wide bandgap semiconductors to address the issues of high-power electronics, where higher power density is a key driver. Vertical GaN technology is one of the pillars that would prove its worth in the coming years in delivering the appropriate performance over cost benefit that the market is looking for. In this chapter,

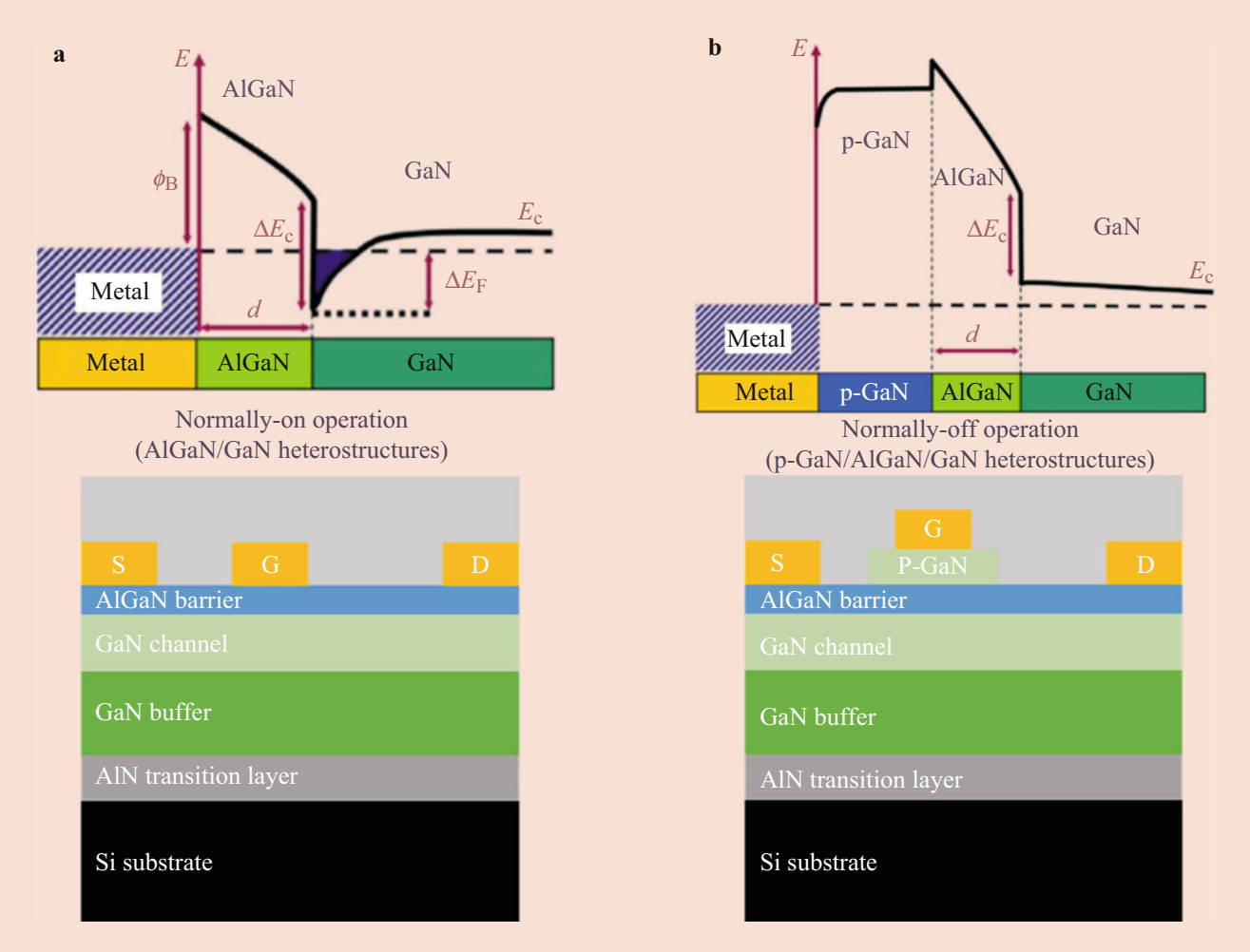

Fig. 15.16 (**a**) Band diagram of an AlGaN/GaN normally-on HEMT and (**b**) a p-GaN/AlGaN/GaN HEMT [61]. (Reprinted from G. Greco et al. [61], 2018, Copyright (2018), with permission from Elsevier)

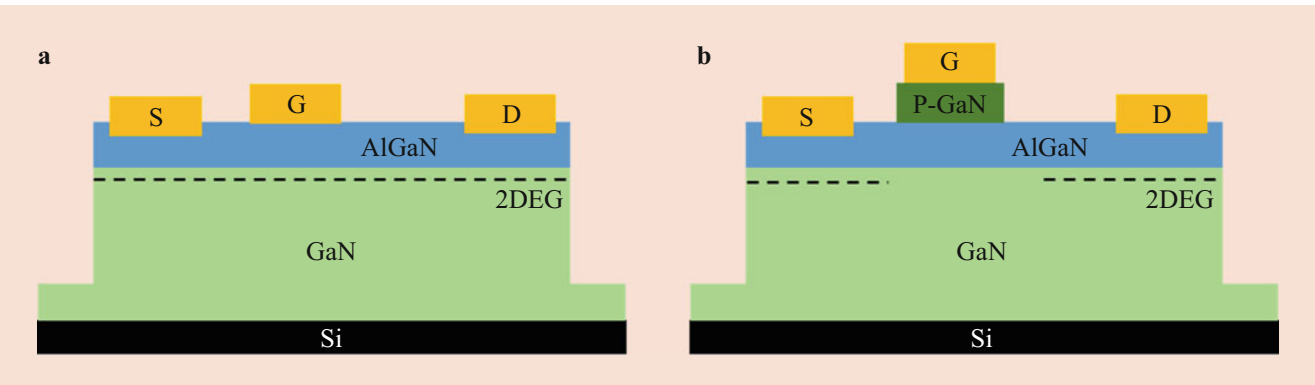

Fig. 15.17 D-mode GaN device structure (**a**) and p-GaN E-mode device structure (**b**)

we go over vertical devices in GaN like Current aperture vertical electron transistor (CAVET), vertical Metal Oxide Field Effect transistor (v-MOSFET), and Static Induction transistor (SIT) [63]. But before we go over the devices, we will discuss about TCAD models that we found extremely valuable to predict device performance during our research.

15.3.1 Device/Circuit Hybrid Modeling

For power semiconductor devices, technology computer-aided design (TCAD) simulation is a vital tool to accurately predict the behavior and optimize the design of devices. For the well-proven practice of Si-based devices, there are reliable simulation platforms that include process, device, and circuit (system) models. However, due to the maturing nature of the GaN technology, there are very few available device simulation tools. Due to the expensive manufacturing of GaN devices, it becomes even more important to develop an accurate and reliable TCAD modeling for GaN devices to predict device behaviors.

A flowchart of the device/circuit hybrid modeling approach is shown in Fig. 15.18 [64]. Before the development of the model, a 700 V AlGaN/GaN HEMT was fabricated. Based on the extracted data from the fabricated HEMT, we developed a physics-based device model for it, and then integrated it with a circuit model to study the dynamic characteristics and power losses of the HEMT. Using this device-circuit-integrated model, we can start with 2D drift-diffusion modeling of the device and build all the way up to its circuit implementation to evaluate its switching performance. The method of using a hybrid model should give us an inexpensive and accurate way to project and benchmark the performance that can be extended to any GaN-based power transistors.

15.3.2 Physics Models for GaN

Drift-Diffusion Model

The TCAD device simulation uses the drift-diffusion model, which solves the Poisson and current continuity equations. The equations are shown as

$$\nabla^2 \varphi = \frac{q\,(n - p + N_{\mathrm{A}} - N_{\mathrm{D}})}{\varepsilon_{\mathrm{s}}}, \tag{15.9}$$

$$\frac{\partial n}{\partial t} = G_{\mathrm{n}} - U_{\mathrm{n}} + \frac{1}{q}\nabla \cdot \vec{J}_{\mathrm{n}}, \tag{15.10}$$

where φ is the electrostatic potential, q is the electron charge, n is the free electron density, p is the free hole density, N_{A} is the ionized acceptor density, N_{D} is the ionized donor density, G_{n} is the regeneration rate for electron, U_{n} is the recombination rate of electron, and $\boldsymbol{J}_{\mathrm{n}}$ is the electron current density.

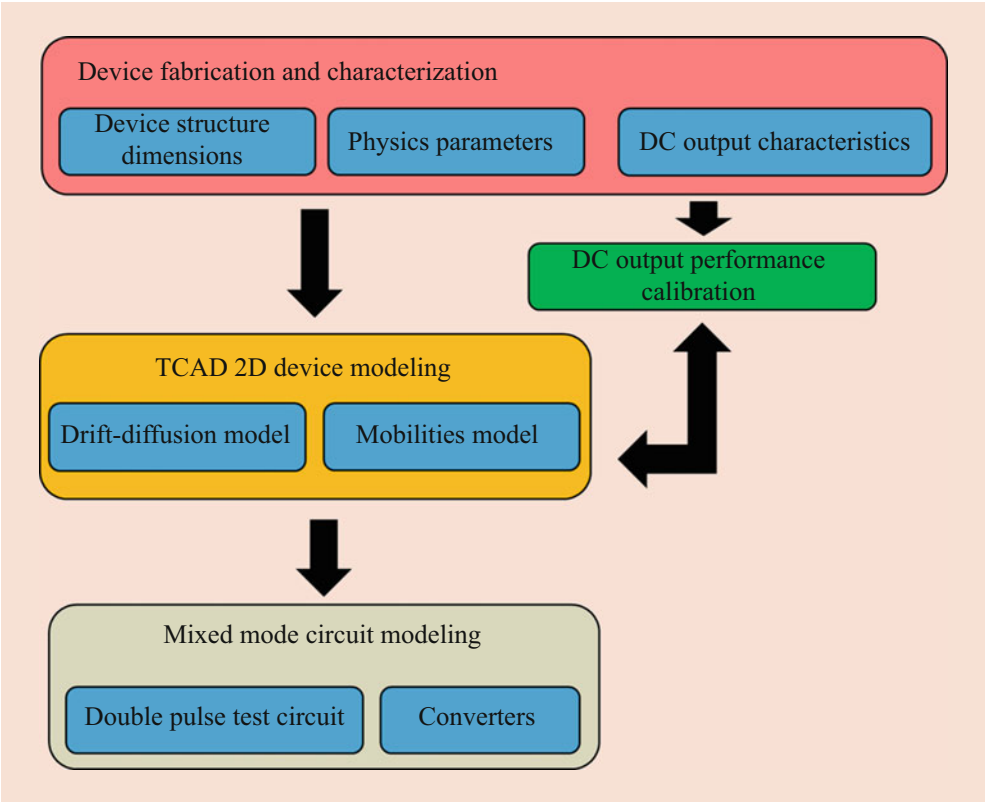

Fig. 15.18 The flowchart of simulation methodology

B. Polarization

The non-centrosymmetric compound crystals exhibit polarity along the axes of (0001) of GaN. Two types of polarization existence in the AlGaN/GaN heterostructure: the strain-induced piezoelectric polarization P_{PE} and the spontaneous polarization P_{SP}. The amount of the polarization induced sheet charge density can be written as [65]

$$|\sigma(x)| = \left|2\frac{a(0)-a(x)}{a(x)}\left\{e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)}\right\} + P_{SP}(x) - P_{SP}(0)\right|, \tag{15.11}$$

where the x is Al mole fraction in AlGaN, the lattice constant $a(x)$ is given by $a(x) = (-0.0077x + 0.3189)$ nm; a$(t) = (-0.0077t + 0.3189)$nm elastic constants $c_{13}(x)$ and $c_{33}(x)$ can be written as $c_{13}(x) = (5x + 103)$ GPa and $c_{33}(x) = (-32x + 405)$ GPa, respectively; piezoelectric constants $e_{33}(x)$ and $e_{31}(x)$ can be expressed as $e_{33}(x) = (0.73x + 0.73)$ C/m^2 and $e_{31}(x) = (-0.11x - 0.49)$ C/m^2, respectively; and the spontaneous polarization $P_{sp}(x)$ is given by $P_{sp}(x) = (-0.052x - 0.029)$ C/m^2.

Electron Mobility

Electron mobility is a key parameter to determine the conductivity of a given semiconductor. A number of theoretical and experimental studies have been performed to understand the electron mobility in GaN. In a recent report, a dual model, one for low-field and the other for high field, was observed to well fit to the reported theoretical and experimental data [66]. The low field electron mobility is given according to the doping and temperature-dependent Arora model [66]:

$$\mu_0(T,N) = \mu_{min}\left(\frac{T}{300}\right)^{\beta_1} + \frac{(\mu_{max}-\mu_{min})\left(\frac{T}{300}\right)^{\beta_2}}{1+\left[\frac{N}{N_{ref}\left(\frac{T}{300}\right)^{\beta_3}}\right]^{\alpha(T/300)^{\beta_4}}}, \tag{15.12}$$

T is temperature, μ_{min}, μ_{max}, β_1, β_2, β_3, β_4, and α are parameters that can be determined by experiment.

Due to the unique energy band diagram, GaN shows a negative differential region in the field-velocity curve for electrons at very high fields. This is caused by the movement of high-energy electrons from lower Γ valley to the higher M and L valleys, where electrons have higher effective mass, reducing the velocity. The transferred electron effect model was found to have a reasonable fit to the tendencies observed for the experimental and theoretical data [66].

Table 15.2 Mobility model parameters used in GaN device simulation [66–68]

Parameters	Values
μ_{min}	115 cm^2/Vs
μ_{max}	1800 cm^2/Vs
β_1	−1.5
β_2	−1.5
β_3	3.02
β_4	0.81
A	0.8
N_{ref}	7×10^{16} cm^{-3}
$v_{n,sat}$	1.9064×10^7 cm/s
E_C	1.7×10^5 V/cm
n_1	4.19
n_2	0.885
A	5.64

$$\mu(T,N) = \frac{\mu_{n0}(T,N) + v_{n,sat}\frac{E^{n1-1}}{E_C{}^{n1}}}{1 + a\left[\frac{E}{E_C}\right]^{n_2} + \left[\frac{E}{E_C}\right]^{n_1}}, \tag{15.13}$$

The parameters used in GaN simulation are listed in Table 15.2.

Device Modeling Calibration

The TCAD simulated device was identical in design with the fabricated device, the structure of which is shown in Fig. 15.19. An excellent agreement between the experimental and the simulated data was obtained by optimizing the physical parameters to replicate GaN's physical parameters. We repeated the optimization until a satisfactory fit of the experimental and simulated data was obtained as illustrated in Fig. 15.20.

Figure 15.21 shows the capacitances in a single E-mode device, the output capacitance (C_{oss}), input capacitance (C_{iss}), and reverse capacitance (C_{rss}) can be written as

$$C_{oss} = C_{GD} + C_{DS} \tag{15.14}$$

$$C_{iss} = C_{GS} + C_{DS} \tag{15.15}$$

$$C_{rss} = C_{GD} \tag{15.16}$$

In a cascoded configuration, the D-mode GaN device is cascoded with an E-mode Si MOSFET to render the combination into a normally-off device. The capacitance distribution is shown in Fig. 15.22. Capacitances labeled

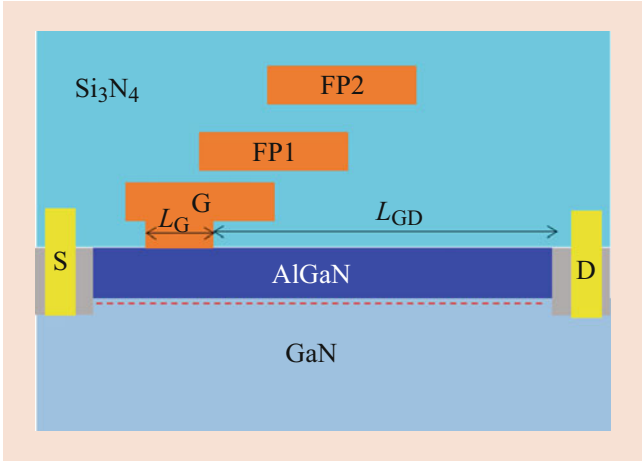

Fig. 15.19 HEMT structure used in the simulation. The HEMT has three field plates (FP) with a gate to drain distance $L_{GD} = 10\ \mu m$, gate length $L_G = 2\ \mu m$. (© 2016 IEEE. Reprinted, with permission, from D. Ji et al. [64])

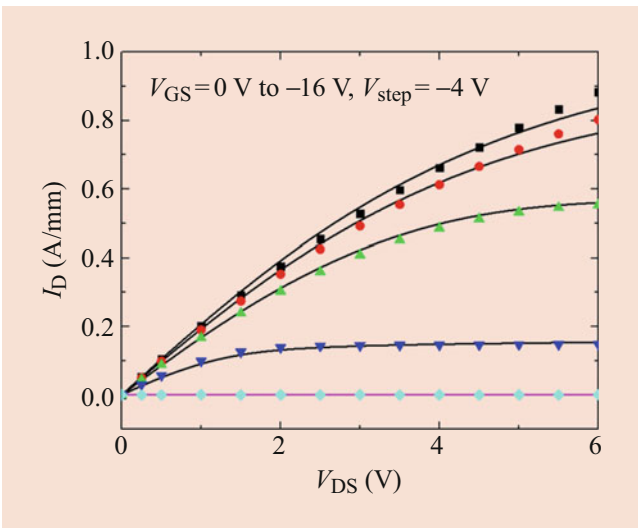

Fig. 15.20 A comparison of HEMT IV characteristics between simulation (dot curves) and experiment (solid curves). (© 2016 IEEE. Reprinted, with permission, from D. Ji et al. [64])

with a subscript "1" and "2" represent for Si MOSFET and AlGaN/GaN HEMT, respectively.

In this cascoded configuration, the output capacitance (C_{oss}), input capacitance (C_{iss}), and reverse capacitance (C_{rss}) can be written as [64]

$$C_{iss} = C_{GS1} + \frac{C_{GD1}\,(C_{GS2} + C_{DS1} + C_{DS2})}{C_{GD1} + C_{GS2} + C_{DS1} + C_{DS2}}, \qquad (15.17)$$

$$C_{oss} = C_{GD2} + \frac{C_{DS2}\,(C_{GD1} + C_{DS1} + C_{GS2})}{C_{GD1} + C_{DS1} + C_{GS2} + C_{DS2}}, \qquad (15.18)$$

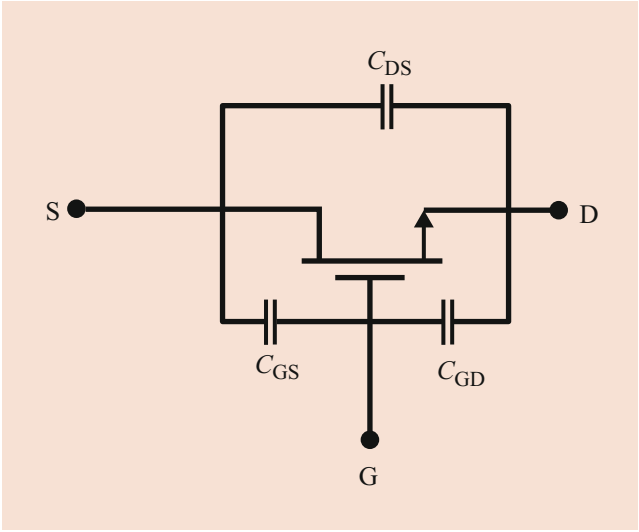

Fig. 15.21 Capacitance distribution in a single power MOSFET

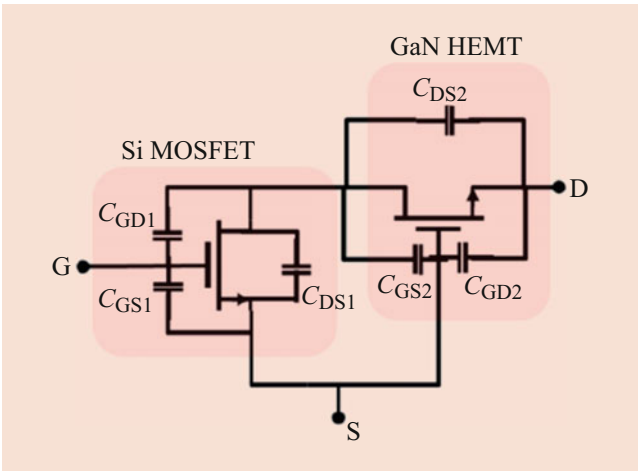

Fig. 15.22 Capacitance distribution in a cascoded HEMT. (© 2016 IEEE. Reprinted, with permission, from D. Ji et al. [64])

$$C_{rss} = \frac{C_{DS2}C_{GD1}}{C_{GD1} + C_{DS2}}, \qquad (15.19)$$

The *C-V* characteristics, which determine the switching performance of a power transistor, was obtained from the simulation and is shown in Fig. 15.23.

Figure 15.24 shows a double pulse test circuit with an inductive load that is widely used in the evaluation of power devices. The free-wheeling diode was assumed to be ideal, and a current source was adopted instead of the inductor to simplify the simulation. The Si MOSFET has a voltage rating of 30 V and R_{ON} of 20 mΩ. One of the highlights of this work is the successful incorporation of the parasitic inductance in the cascoded device. The parasitic inductances in our model were $L_G = 2$ nH, $L_S = 10$ nH, and $L_D = 1.9$ nH [64].

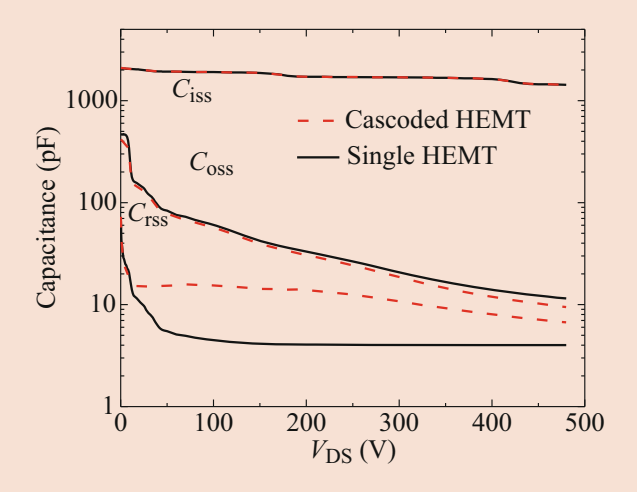

Fig. 15.23 *C-V* characteristics in the cascoded HEMT and single E-mode HEMT

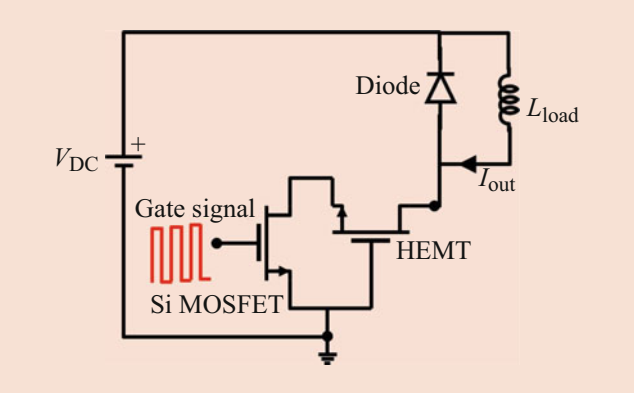

Fig. 15.24 Test circuit used in the simulation. (© 2016 IEEE. Reprinted, with permission, from D. Ji et al. [64])

Figure 15.25a shows the turn-on switching characteristics of a 600 V cascoded HEMT, with a total on-state resistance R_{ON} of 290 mΩ. The resistance and the capacitance characteristics discussed in the previous section applies to the particular device discussed in this section. A V_{DS} of 480 V, I_D of 5.5 A and external gate resistance R_G of 2 Ω were used in this simulation.

From the waveforms shown in Fig. 15.8a, the turn-on delay time $t_{d(on)}$ is 5 ns, and rise time t_r is 3 ns, showing a turn-on $\Delta v/\Delta t$ of ~120 kV/μs. Figure 15.25b shows the power loss during the turn-on transient, the total energy loss is 37 μJ.

From the waveforms of Fig. 15.26a, the turn-off delay time $t_{d(off)}$ is 12.5 ns, and fall time t_f is 4 ns, giving a turn-off $\Delta v/\Delta t = \sim 95$ kV/μs. The power loss shown in Fig. 15.26b indicates a turn-off switching loss of 3 μJ.

For the validation of the device-circuit integrated model, we chose a commercially available HEMT (Transphorm TPH3002LD) to perform the simulation. We first simulated

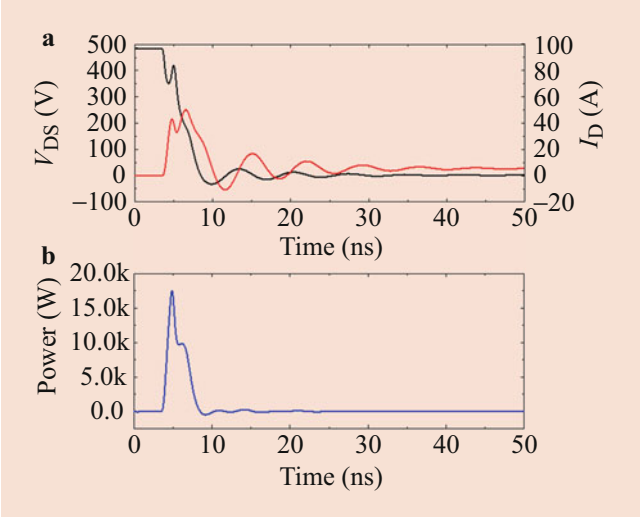

Fig. 15.25 (**a**) Simulated turn-on switching waveforms of the cascoded HEMT; (**b**) power loss during the turn-on switching

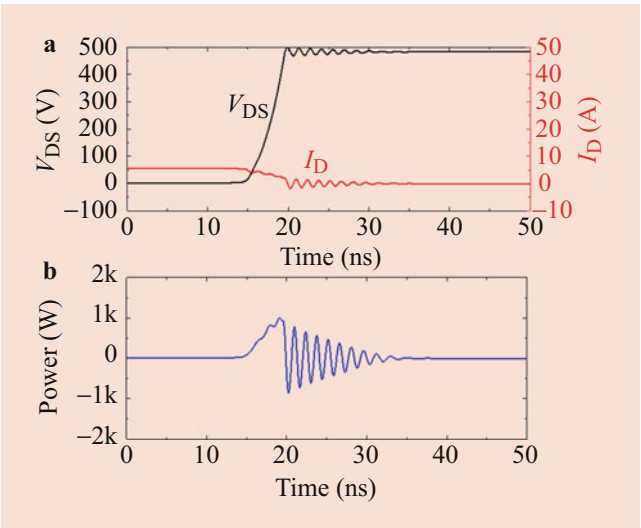

Fig. 15.26 (**a**) Simulated turn-off switching waveforms of the cascoded HEMT; (**b**) power loss during the turn-off switching

the HEMT and then tested it in a cascode configuration to replicate TPH3002LD, using the same circuit as shown in Fig. 15.24. A comparison between TPH3002LD and our simulated device is shown in Table 15.3. A reasonable agreement was obtained as evident from Table 15.3, now confirming both drift-diffusion and circuit model, and hence our hybrid modeling technique. The reasonable agreement of the TPH3002LD with our simulated data built and reassured a reliable platform to now apply for any GaN power device and project its switching performance.

Modeling of Vertical GaN Devices

Using the device-circuit-integrated model built in the Silvaco's MixedMode platform and calibrated using GaN

Table 15.3 Comparison of the simulated and commercial GaN cascoded HEMT

Parameters	Transphorm TPH3002LD	Simulated GaN cascoded HEMT	Test conditions
V_{BR} (V)	600	700	
V_{TH} (V)	1.8	2	
R_{ON} (Ω)	0.29	0.29	
Q_G (nC)	9.3	13	$V_{DS} = 100$ V, $V_{GS} = 0$–4.5 V, $I_D = 5.5$ A
$t_{d(on)}$ (ns)	7	5	$V_{DS} = 480$ V, $V_{GS} = 0$–10 V, $I_D = 5.5$ A, $R_G = 2$ Ω
t_r (ns)	3	3	
$t_{d(off)}$ (ns)	11	12.5	
t_f (ns)	4.5	4	
$C_{oss(tr)}$ (pF)	63	50.9	$V_{GS} = 0$ V, $V_{DS} = 480$ V
$C_{oss(er)}$ (pF)	36	28	
C_{oss} (pF)	26	18	$V_{GS} = 0$ V, $V_{DS} = 400$ V, $f = 1$ MHz
C_{iss} (pF)	785	1631	
C_{rss} (pF)	3.5	3	

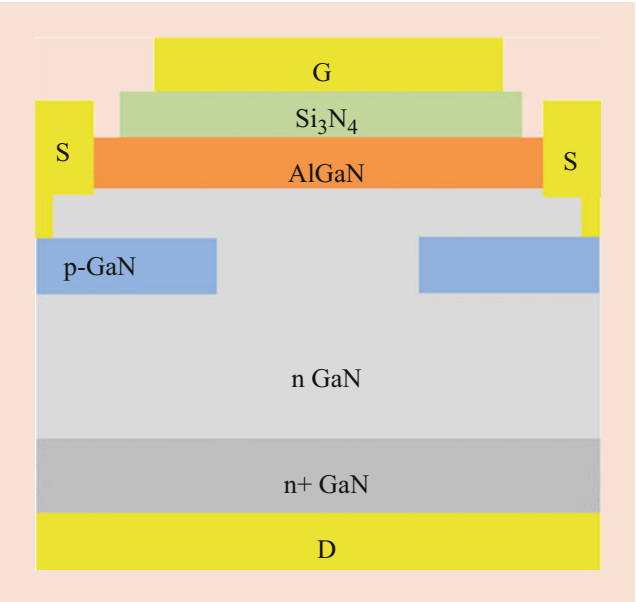

Fig. 15.27 Schematic of a normally-on CAVET

HEMTs [64], the switching performance of the vertical GaN transistor was analyzed. In this section, a current aperture vertical electron transistor (CAVET) was used, since this device was one of the most developed vertical GaN devices. The structure of the CAVET is shown in Fig. 15.27.

Figure 15.27 shows the schematic of a normally-on CAVET. A thick n-GaN with 10^{16} cm^{-3} doping was designed to form the drift region on a conductive GaN (10^{18} cm^{-3}) substrate. 0.4 μm-thick p-type current blocking layers (CBLs) were implemented with a doping density of 3×10^{17} cm^{-3} to block current from flowing through any other path other than the designed aperture ($N_D = 3 \times 10^{17}$ cm^{-3}). AlGaN/GaN channel was defined on top of the CBL and the aperture to conduct electrons from the source through a high mobility 2D channel obtained at the hetero-interface. Sources contacting the 2D electron gas were designed on either side of the gate at a distance of 2 μm. The p-GaN CBLs were connected to the source to provide a discharge path for any electrons trapped in the p-type layer.

CAVETs are normally-on devices similar to GaN HEMTs. Techniques that are typically applied to HEMTs can be applied to CAVETs to render it normally-off. We adopted a cascoded CAVET approach in this work to achieve normally-off operation, where the cascode was designed with a low-voltage Si MOSFET. The cascoded CAVET was subjected to switching operation, and detailed performance matrix was generated.

Figure 15.28 shows the cascode configuration designed with a low-voltage normally-off Si MOSFET as the input and a high-voltage normally-on CAVET as the output. The current paths of the forward conduction are labeled with the arrows in Fig. 15.28a. In the forward conduction, the total on-state resistance (R_{on}) is the sum of the MOSFET R_{on} and the CAVET R_{on}. In the reverse conduction cycle (shown in Fig. 15.28b), the current flows through the body diode of the Si MOSFET and the CAVET channel. It is important to note that the body diode of the CAVET does not conduct current at any time of the operation.

Figure 15.29 shows the turn-on switching characteristics of a 1.2 kV cascoded CAVET, with a total on-state resistance R_{ON} of 80 mΩ. A V_{DS} of 800 V, I_D of 20 A and external gate resistance R_G of 2.5 Ω were used in this simulation. Before we discuss the results a close-up look at the turn-on event in a switching cycle will be befitting. The turn-on event can be divided into three stages [64].

In the first stage, when a V_{GS} is applied to the gate electrode, the gate current I_G starts charging the Si MOSFET gate to source capacitor C_{GS_MOS}. As a result, Si MOSFET gate to source voltage V_{GS_MOS} increases.

Once the V_{GS_MOS} reaches the threshold voltage of Si MOSFET, in the second stage, the MOSFET channel is turned on, and channel current increases. The Si MOSFET channel current discharges three capacitors: Si MOSFET gate to drain capacitor C_{GD_MOS}, Si MOSFET drain to source capacitor C_{DS_MOS}, and GaN CAVET gate to source capacitor C_{GS_CAVET}, as a result of which, MOSFET drain to source voltage V_{DS_MOS} decreases, and the CAVET source to gate voltage V_{SG_CAVET} decreases as well.

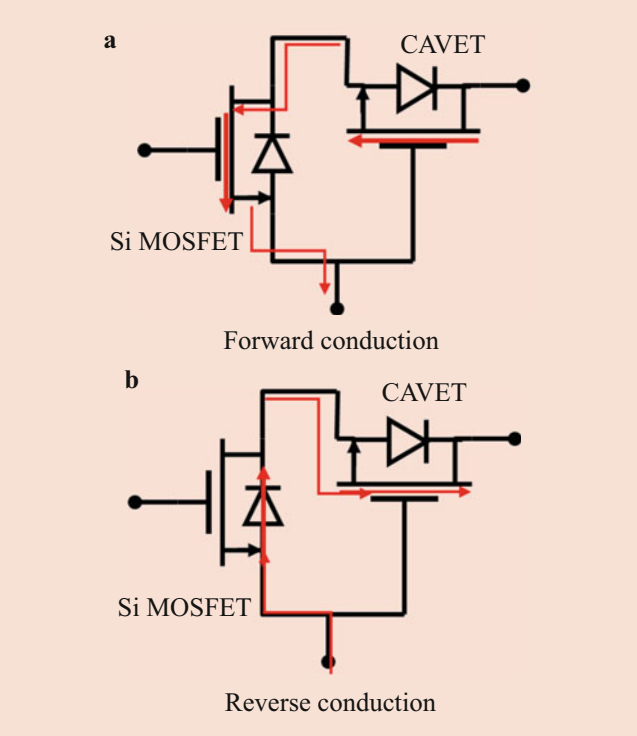

Fig. 15.28 (**a**) Forward conduction of the cascoded CAVET; (**b**) reverse conduction of the cascoded CAVET

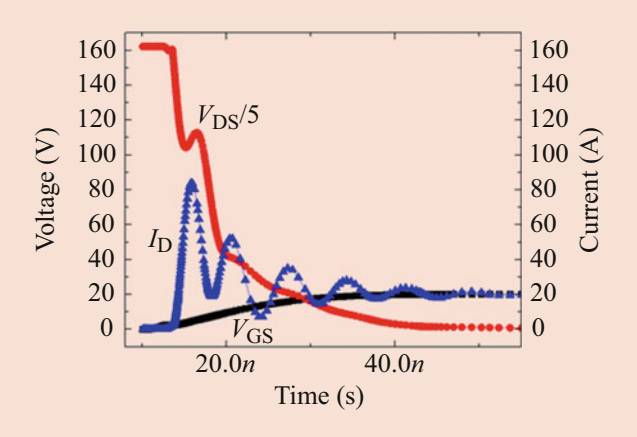

Fig. 15.29 Simulated turn-on switching waveforms of the cascoded CAVET. (© 2016 IEEE. Reprinted, with permission, from D. Ji et al. [64])

Third, when V_{SG_CAVET} reaches the threshold voltage of GaN CAVET, CAVET channel current increases, and this current start discharging the GaN CAVET drain to source capacitor C_{DS_CAVET} and GaN CAVET gate to drain capacitor C_{GD_CAVET}, reducing V_{DS_CAVET} further.

From the waveforms shown in Fig. 15.29, the turn-on delay time $T_{on\text{-}delay}$ is 2 ns, and rise time T_r is 16 ns, showing

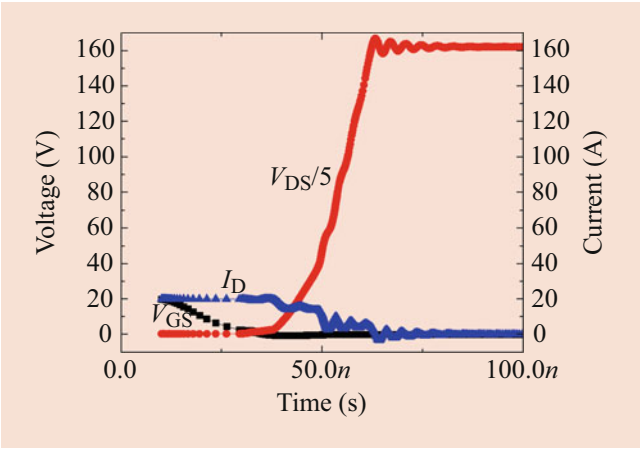

Fig. 15.30 Simulated turn-off switching waveforms of the cascoded CAVET. (© 2016 IEEE. Reprinted, with permission, from D. Ji et al. [64])

a turn-on $\Delta v/\Delta t$ of 40 kV/μs. The total gate charge of the CAVET is 88 nC.

The turn-off switching waveforms are shown in Fig. 15.30. Similar to the turn-on transient, the turn-off phenomenon can be subdivided into three stages.

First, when the applied MOSFET V_{GS} changes from on to off state (from 10 V to 0 V), the Si MOSFET gate to source capacitor C_{GS_MOS} is discharged and as a consequence, Si MOSFET channel current decreases, which is smaller than the operation current (output current in current source), and the excess current charges the MOSFET drain to source capacitor C_{DS_MOS}, increasing V_{DS_MOS}. Since the GaN CAVET source to gate capacitor C_{SG_CAVET} is in parallel with C_{DS_MOS}, the voltage V_{SG_CAVET} also increases.

Next, when V_{SG_CAVET} increases, the channel current in CAVET decreases, as a result, the channel current is smaller than the output current. The excess current starts charging CAVET drain to source capacitor C_{DS_CAVET} and gate to drain capacitor C_{GD_CAVET}, as a result, V_{DS_CAVET} increases.

When V_{SG_CAVET} reaches a value smaller than the threshold voltage of CAVET, the channel is completely pinched off, and the remaining gate current continues to charge the capacitors: C_{GD_MOS}, C_{DS_MOS}, C_{GD_CAVET}, and C_{DS_CAVET}, further raising the V_{DS_MOS} and V_{DS_CAVET}.

From the waveforms of Fig. 15.30, the turn-off delay time $T_{off\text{-}delay}$ is 29.5 ns, and fall time T_f is 18 ns, giving a turn-off $\Delta v/\Delta t = 35.6$ kV/μs.

Table 15.4 shows the comparison of CREE SiC MOSFET (CREE Inc.), simulated SiC MOSFET, and simulated cascoded CAVET with the same voltage and current rating. The switching performance agreement between CREE and simulated SiC MOSFETs provides the competency of the model. When compared to standard SiC MOSFET, cascoded CAVET has faster switching time, and lower switching loss, hence enabling higher frequency operation.

Table 15.4 Switching performance comparison of SiC MOSFET and GaN CAVET

Parameters	Cree SiC MOSFET (CREE Inc.)	Simulated SiC MOSFET [64]	Simulated GaN CAVET [64]
V_{BR} (kV)	1.2	1.2	1.2
R_{on} (mΩ)	80	80	80
$t_{off\text{-}delay}$ (ns)	40	55	29.5
t_f (ns)	38	25	18
$t_{on\text{-}delay}$ (ns)	13	10	2
t_r (ns)	24	27	16
Q_G (nC)	90.8	157	88
E_{off} (μJ)	305	312	57
E_{on} (μJ)	305	304	152
E_{ts} (μJ)	610	616	209

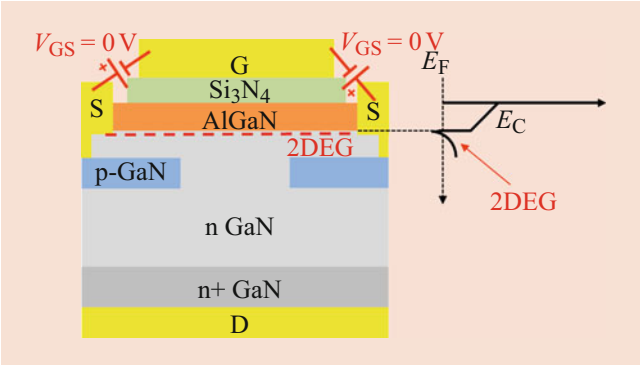

Fig. 15.31 Cross section of an on-state GaN CAVET and the conduction band diagram

15.3.3 A Review of CAVET

CAVETs are vertical GaN vertical devices that take full advantage of the polarization-based two-dimensional electron gas (2DEG) in its design. Comprised of a 2DEG induced channel to carry the current, a CAVET needs a thick homoepitaxially grown drift region to hold the blocking voltage. There have been two types of approach in fabricating CAVETs: (1) planar CAVET and (2) trench CAVET. The planar CAVET has an AlGaN/GaN 2DEG channel in the c-plane, which has high electron density and high mobility. The trench CAVET adopts the semi-polar plane as the channel, the density of the electrons depends on the slope of trench sidewalls.

The first GaN CAVET based on a sapphire substrate was developed in 2004 [69]. The device structure began with a p-GaN/n-GaN/*n*+GaN epilayers. An aperture region was etched and an AlGaN/GaN HEMT structure was regrown by MOCVD to refill the aperture region and served as the channel as well. The design of the first GaN CAVET was for radio frequency (RF) applications. Several years later in 2008, the first power GaN CAVET based on bulk GaN substrate was reported with the CBL formed by Mg-ion implantation [70]. The device process began with the MOCVD grown *n*-GaN on conductive bulk GaN substrate; then, the selective area Mg-ion-implantation was implemented to form the CBL to block current from the aperture region other than any other paths. The top AlGaN/GaN structure was regrown by MBE. The first high-voltage CAVET with switching characteristics was demonstrated by Chowdhury et al. with a 300 V breakdown voltage and a $R_{on,sp}$ of 2.2 mΩ•cm^2 [71]. A significant progress in the device development was realized with the demonstration of 1.5 kV JFET (a variant of CAVET) on bulk substrate by H. Nie et al. in 2014 from Avogy Inc. [72].

15.3.4 Operation Principle of the CAVET

A CAVET is a unique design where the best properties that GaN offers are best utilized. Polarization doping is one of these properties which is leveraged in a CAVET design. Due to the positive polarization charge locates at the AlGaN/GaN interface, a triangular quantum well is formed, and electrons are attracted (shown in Fig. 15.31). The high-density electrons are confined in the triangular quantum well, forming the 2DEG. Under a zero-gate bias, the channel is conductive due to the 2DEG, the device is in the on-state. During on-state of the CAVET, the electrons from the source go through the 2DEG channel, the aperture and the drift region and are finally collected by the drain electrode. The overlap between the gate electrode and the CBL is the effective gate length that offers channel modulation.

Like in a HEMT, in order to pinch off the 2DEG channel in a CAVET, a negative gate bias is required. At the off-state, the electrons in the channel are depleted by the gate potential. The p-n junction formed by p-type (or Mg-implanted) CBL and drift region blocks the off-state voltages. Figure 15.29 shows the schematic of a planar CAVET where the CBL (shown as p-GaN) is formed using an ion implantation process of GaN with Mg ions. During the on-state, the voltage applied between the source and the drain drops across the channel. The design must ensure that the aperture is more conductive than the channel. Under the off-state, the depletion region is extended into the drift layer to sustain the drain to source voltage. Besides forcing the current flow through the aperture and blocking any parasitic current flow from drain to source, the CBL also needs to be conductive enough to prevent charge trapping which may lead to current collapse. From our experiments [73, 74], we found that CAVETs with Al-implanted CBL was dispersive, whereas CAVETs with Mg-implanted CBL were dispersionless. CAVETs with ion-implanted CBL require regrowth of AlGaN/GaN channel. The regrown channel and the aperture

are grown on the planar surface where CBL is formed by ion implantation. One significant challenge in the ion-implanted process was the out-diffusion of Mg from the CBL to the regrown layers causing the channel to get totally wiped off. Although several tactics were employed, one of those being using a thin AlN diffusion-stopper layer [73, 74], the most successful technique was achieved through the regrowth of the channel through a lower temperature MBE regrowth that led to the successful CAVETs. In an alternative approach MOCVD grown p-type layers were used to form the CBL. This is the basic building block for a Trench CAVET which is discussed next.

15.3.5 Trench CAVET

The conventional GaN CAVET typically uses Mg-implanted p-GaN for the CBL. A major fabrication challenge is posed by Mg out-diffusion during the regrowth process. First, the channel resistance can go very high due to the diffusion of Mg species into the channel, thereby depleting 2DEG. To prevent the diffusion of Mg into the regrown channel the regrowth temperature of the channel in a CAVET is restricted, making it rely on low-temperature growth processes. Low-temperature MOCVD regrowth process does not typically result into a high-quality material. MBE regrowth although has proven to be successful in arresting Mg diffusion, there are concerns on the formation of vertical highly conductive paths under metal-rich growth conduction, causing shorts in the device. An MBE-regrown channel requires exposure of the sample to the atmosphere for prolonged interval, and process limitations make it challenging to remove environmental contaminants from the regrowth interface. Low-temperature flow modulation epitaxy by MOCVD may be considered an alternative, but it is not yet understood whether the material quality produced in such a fashion that can support high-current and high-voltage devices.

A solution to the aforementioned problem was proposed by introducing a trench gate structure into the conventional CAVET, as shown in Fig. 15.32 [75, 76]. Instead of using Mg-implanted p-GaN for the CBL, the trench CAVET adopts MOCVD-grown Mg-doped p-GaN as the CBL material. The trench CAVET utilizes the regrown AlGaN/GaN on the trench sidewall as the channel. The trench sidewall angle determines the polarization scale of the channel: a 90-degree angle indicates a non-polar plane, and a 45-degree angle indicates a semi-polar plane. The threshold voltage in a trench CAVET can be adjusted by the trench sidewall angle. The functioning of a trench CAVET is similar to a trench MOSFET, except for the AlGaN/GaN channel. In a conventional trench MOSFET, the channel is formed by inversion layer between the oxide and the p-type semiconductor. The electron mobility in the inversion layer is typically below

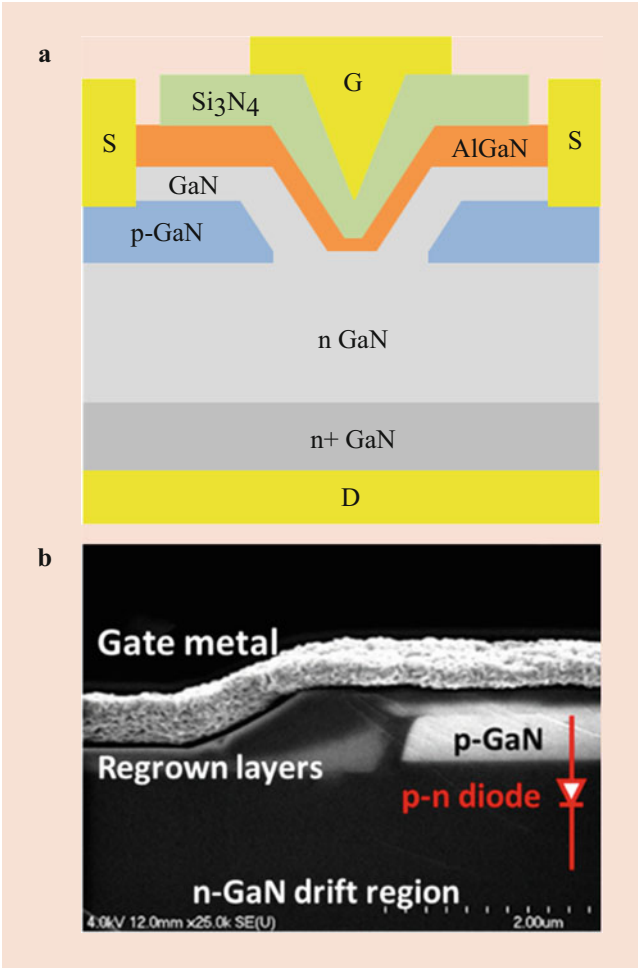

Fig. 15.32 (**a**) Schematic illustrations of the trench CAVET. (**b**) SEM image showing a buried p-n junction which blocking voltage in the off-state. (© 2017 IEEE. Reprinted, with permission, from D. Ji et al. [75])

50 cm^2/Vs, limited by the interface roughness scattering. However, in a trench CAVET, the channel is formed by the 2DEG, which takes the advantage of the high mobility in the HEMT structure. Ideally, the channel mobility in a trench CAVET can be as high as 1690 cm^2/Vs [77].

In GaN, a robust oxide technology is not available yet. However, thanks to the development of GaN HEMT in the last decade, the in situ grown Si_3N_4 on AlGaN/GaN structure has low interface traps, which is essential to the device reliability. A trench CAVET takes the advantage of the matured HEMT gate dielectric technology to suppress gate leakage.

The first metal-insulator-semiconductor (MIS) gate trench CAVET was reported by Ji et al. in 2016 on bulk GaN substrates [75]. The device had a breakdown voltage of 225 V limited by the gate-to-drain breakdown. By using a thicker gate dielectric layer and a low damage RIE trench etch, a high breakdown voltage of 880 V was obtained in 2018 [76]. A low hysteresis of ~0.1 V was achieved by using high-quality in situ Si_3N_4 gate dielectric (Figs. 15.33, 15.34, and 15.35).

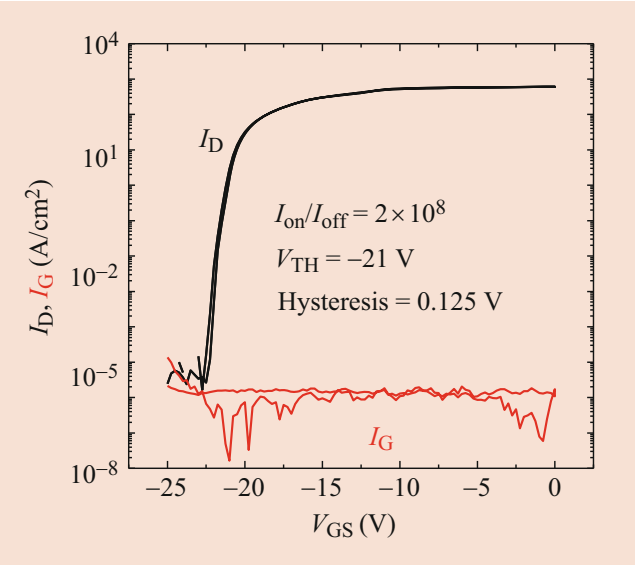

Fig. 15.33 Double-swept I_D-V_{GS} transfer characteristics of the fabricated trench CAVET [76]. (© 2018 IEEE. Reprinted, with permission, from D. Ji et al. [76])

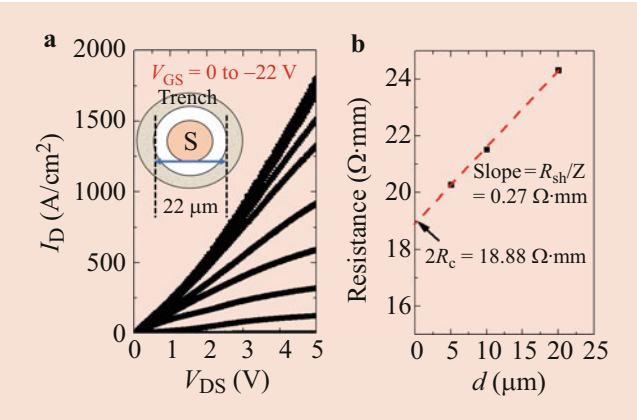

Fig. 15.34 (**a**) I_D-V_{DS} characteristics of the fabricated trench CAVET. (**b**) Analysis of contact resistance [76]. (© 2018 IEEE. Reprinted, with permission, from D. Ji et al. [76])

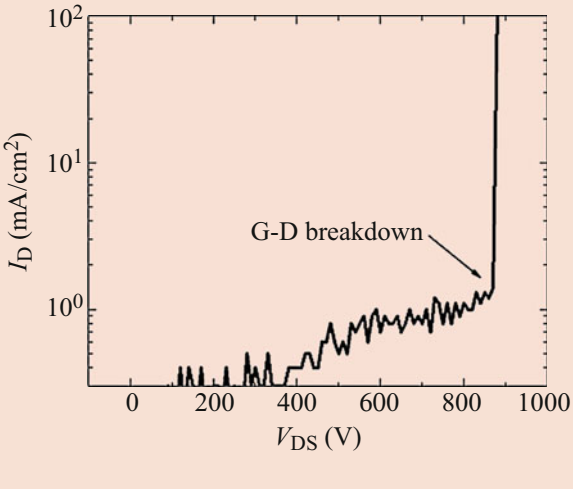

Fig. 15.35 Off-state characteristics of the fabricated trench CAVET [76]. (© 2018 IEEE. Reprinted, with permission, from D. Ji et al. [76])

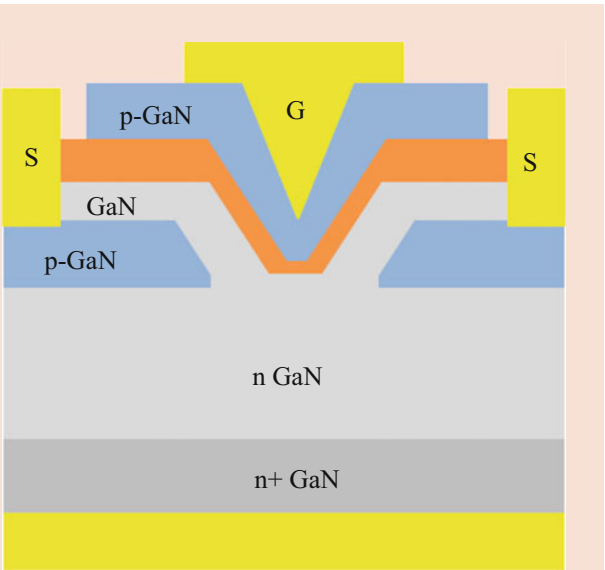

Fig. 15.36 Trench CAVET with a p-GaN gate layer [77]

The p-GaN gate structure is widely used in normally-off lateral GaN HEMTs. Due to the high electron density of 2DEG induced by the polarization charge, the threshold voltage of p-GaN gated HEMT is typically less than 2 V. However, a more positive threshold voltage can be realized in a p-GaN gated trench CAVET with the channel formed at the semi-polar plane. This was first demonstrated by Shibata et al. in 2016 [77]. Based on a p-n epitaxial structure on bulk GaN substrate, a "V"-shaped trench was formed using inductively coupled plasma (ICP) etching, the p-GaN/AlGaN/GaN triple layers were regrown over the trench by MOCVD. Because the channel locates at the semi-polar plane instead of the c-plane, the threshold voltage shifted toward the positive side by 1.5 V. A high positive threshold voltage of 2.5 V was demonstrated with 1700 V blocking capability on a 13 μm-thick drift region offering a low specific on-resistance of 1 mΩ·cm^2 (Fig. 15.36).

15.3.6 Vertical MOSFETs

Vertical GaN MOSFETs are the other branch of devices, showing a promising performance by offering a normally-off solution, thereby overcoming a significant drawback of any GaN HEMT-based design.

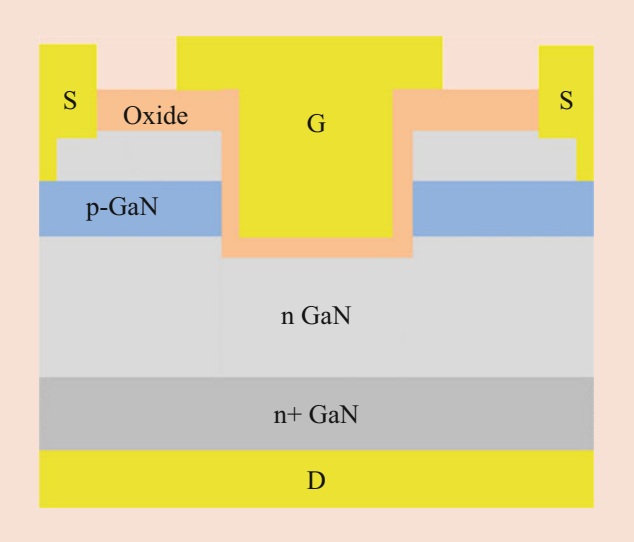

Fig. 15.37 Structure of GaN MOSFET

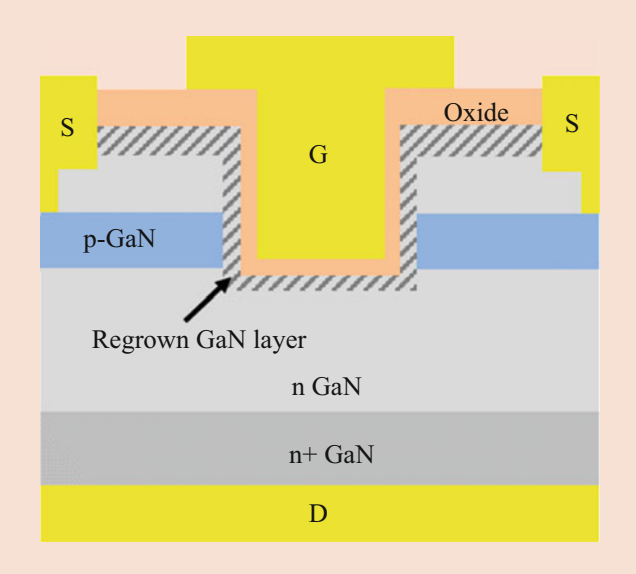

Fig. 15.38 Structure of GaN OGFET. (© 2018 IEEE. Reprinted, with permission, from D. Ji et al. [168])

There are two types of MOSFET reported so far (1) non-regrowth-based MOSFET and (2) regrowth-based MOSFET (OGFET). In this section, both devices will be introduced.

Since the development of dry etch technology in the early 1990s, the trench MOSFET has been a dominant device structure for power electronics. To date, both Si- and SiC-based trench MOSFET have been commercialized and shown excellent performance. However, because of the absence of bulk GaN substrate, the GaN-based trench MOSFET was not available until 2004–2005. In 2007, the first GaN MOSFET was reported by Otake et al. [78], the device has a high threshold voltage of 5.1 V. After 7 years of intense research, a 1.6 kV device was developed by Oka et al. in 2014 [79].

Figure 15.37 shows the structure of a vertical GaN MOSFET. A key feature of these devices, the p-n junction between source and drain is formed by p-base and n-drift regions. The device breakdown voltage is determined by the reverse characteristics of the main p-n junction. A n+ source region is created partially on top of the p-base region, while the junction between the n+ source region and the p-base region is connected to the source contact to improve the breakdown voltage by eliminating the n-p-n open base effect. The channel located at the etched sidewall is formed by the inversion layer of the MOS structure.

Compared to the CAVET structure, there are two basic advantages of the MOSFET: (1) the MOSFET is a reliable normally-off device with a high threshold voltage over 2 V; (2) regrowth can be avoided which makes the process less challenging, reducing the cost and turnaround time. Such advantages of the MOSFET make it an attractive design for vertical GaN transistors. However, for GaN MOSFET, the biggest challenge lies in the channel electron mobility of the device. During on-state, the electrons flow through the inversion layer of the sidewall MOS structure, the channel electron mobility is limited by the surface roughness and impurity scattering. Another issue along with the poor channel property is the device reliability. The GaN MOSFET cannot be widely recognized without a strong reliability.

15.3.7 Regrowth-Based Vertical MOSFET (OGFET)

GaN OGFET is a modified structure based on the conventional trench MOSFET. Compared to the conventional trench MOSFET, the OGFET has two features: (1) an unintentional doped (UID) GaN interlayer is used as the channel region, which enhances the channel electron mobility to reduce the Coulomb scattering by the dopants; (2) the oxide is in situ grown by MOCVD, which reduces the interface states and improves the gate oxide reliability. The novelty of the OGFET is enhancing the channel electron mobility without scarifying the normally-off behavior.

The working principle of the OGFET is similar to the MOSFET. Under a zero V_{GS}, the electrons in the GaN interlayer (shaded region in Fig. 15.38) are depleted by the p-GaN base region making the OGFET go to its off-state. The energy band diagram and the simulated electron contour are shown in Fig. 15.39. The p-n diode formed by the p-GaN base region and the n-GaN drift region is used to hold the high off-state blocking voltage. The electric field distribution along the p-GaN base region and the n-GaN drift region is shown in Fig. 15.40.

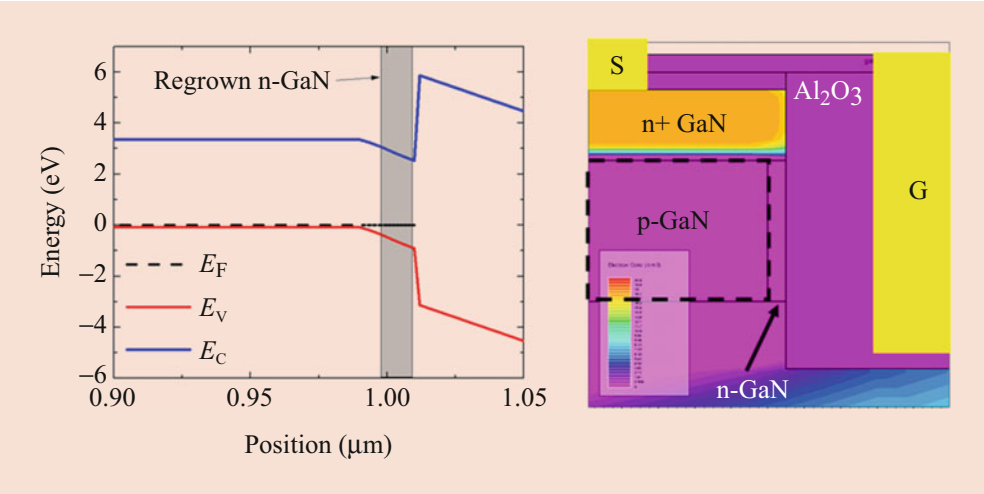

Fig. 15.39 Energy band diagram and the electron distribution of the OGFET in off-state

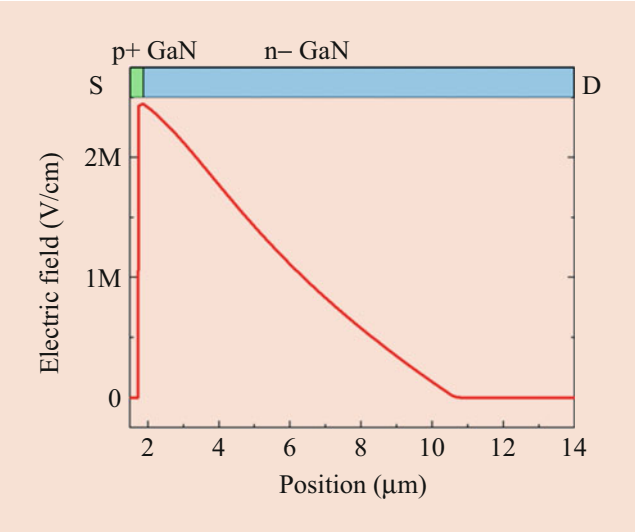

Fig. 15.40 Electric field distribution along the drift region

Under a positive V_{GS} > threshold, electrons are accumulated in the UID GaN insert layer, and the transistor is in its on-state. The energy band diagram and the electron concentration is shown in Fig. 15.41. Because of the enhanced channel electron mobility, the OGFET has smaller $R_{on,sp}$ compared to the conventional trench MOSFET.

In 2016, Gupta et al. reported the first OGFET results based on the sapphire substrates, the device showed a 60% $R_{on,sp}$ reduction while maintaining the threshold voltage >2 V [80]. In 2017, Gupta et al. demonstrated an OGFET on bulk GaN substrates with a breakdown voltage of 990 V and a low $R_{on,sp}$ of 2.6 mΩ·cm^2 [81]. In the same year, *Ji* et al. demonstrated a high-performance OGFET with a breakdown voltage over 1.43 kV with a low $R_{on,sp}$ of 2.2 mΩ·cm^2 [82]. The *I-V* characteristics of the fabricated OGFET are shown in Fig. 15.26. Figure 15.27 shows the transfer I_D-V_{GS} characteristics and the gate leakage. The threshold voltage, V_{TH}, defined at a current level of 10^{-4} A/cm^2 ($I_{on}/I_{off} = 10^6$), obtained was 4.7 V (when V_{GS} sweeps up). A clockwise hysteresis of ΔV_{TH} of 0.3 V was observed. Low sub-threshold slope of 283 mV/decade was measured from $I_D = 10^{-5}$ A/cm^2 to 10^{-2} A/cm^2. The off-state characteristics of the fabricated devices are shown in Fig. 15.42 (Figs. 15.43 and 15.44).

15.3.8 Static Induction Transistor

Static induction transistor is another form of vertical devices, in which current flows vertically through a short channel as shown in Fig. 15.45 [83, 84]. From the equivalent circuit, the overall transconductance, G'_m, is described by intrinsic transconductance, G_m, and series channel resistance, r_s, to be $G'_m = G_m/(1 + r_s \cdot G_m)$. The small distance between gate and source induces $r_s \rightarrow 0$, so that $G'_m \rightarrow G_m$. Consequently, SIT shows a triode-like non-saturating output property, not following square-law behavior shown in the pentode-like FET, which has $r_s \cdot G_m \gg 1$, leading to $G'_m \rightarrow 1/r_s$. The drain current is controlled by electrostatically induced potential energy barrier, that is why the transistor is named, depending on the gate and drain bias. With no gate bias, the drain current is simply defined by the effective cross-sessional area of the channel (A_{eff}), which is related to the depletion width formed at the junctions, so that $I_d = qA_{eff}\, v_d\, N_d$, where q is electron charge, v_d is electron velocity, and N_d is electron density. As applying more negative gate bias, the depletion width increases further and merges at pinch-off, developing the electrostatic barrier in the channel. The minimum barrier height (Φ_0), saddle point, now depends on the drain bias through the drain induced barrier lowering (DIBL) as shown

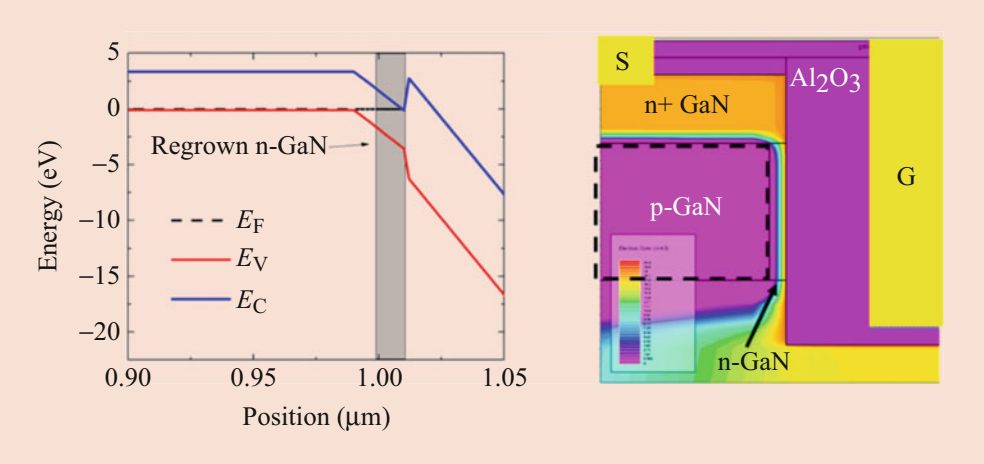

Fig. 15.41 Energy band diagram and the electron distribution of the OGFET in on-state

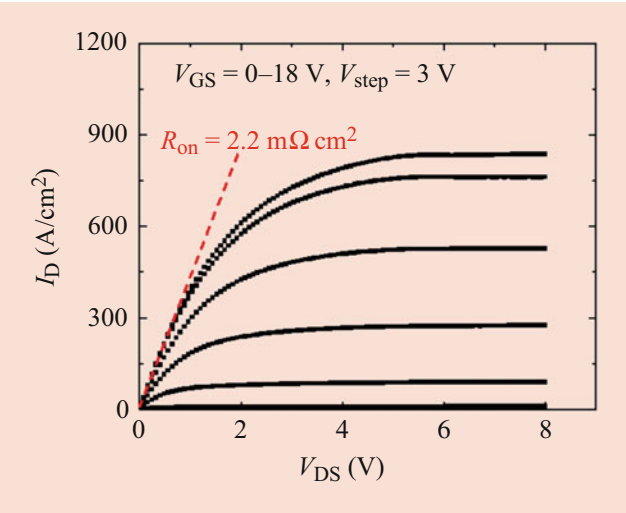

Fig. 15.42 I-V characteristics of fabricated OGFET with saturation current density of 850 A/cm^2 and $R_{on,sp}$ of 2.2 mΩ·cm^2. (© 2017 IEEE. Reprinted, with permission, from D. Ji et al. [82])

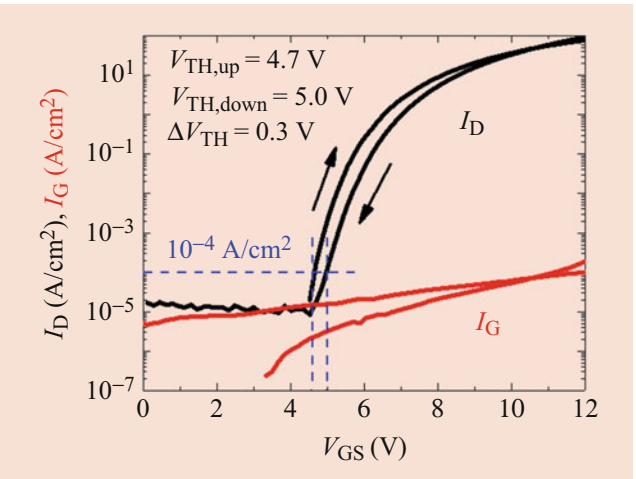

Fig. 15.43 Transfer characteristics of the fabricated OGFET (black curves) and gate leakage (red curves). The threshold voltages of sweep up and down were 4.7 V and 5 V (defined at a current level of 10^{-4} A/cm^2). The sub-threshold slope was 283 mV/decade measured from 10^{-5} A/cm^2 to 10^{-2} A/cm^2. (© 2017 IEEE. Reprinted, with permission, from D. Ji et al. [82])

in Fig. 15.46, governing the electron flow in a manner of thermionic emission, so I_d can be described as,

$$I_d = I_0 \exp\left\{\frac{q}{kT}(\Phi_0 - \alpha V_d)\right\}, \tag{15.20}$$

where α is DIBL coefficient. As increasing drain bias, space charge limited conduction is dominant in the current flow, and the electron velocity becomes saturated. Under high gate and drain bias, the current can be modified as

$$I_d = 2A_{eff}\varepsilon_s v_{sat}\frac{V_d}{L^2}, \tag{15.21}$$

where ε_s is permittivity, v_{sat} is saturation velocity, and L is channel length. This linear relationship between I_d and V_d together with small channel resistance provide benefits to power devices.

The SIT design has been developed from buried-gate to recessed-gate structures using various materials such as SiC and GaN [85–88]. Figure 15.47 presents the output and transfer characteristic of the GaN SIT. By using a Schottky junction, the SIT was fabricated without any p-type GaN or gate dielectrics, which involve difficulty in the activation and reliability. The current density and on-resistance are estimated to be 0.65 kA cm^{-2} and 1.48 mΩcm^2. It is also shown the off current increase as applying larger V_d because

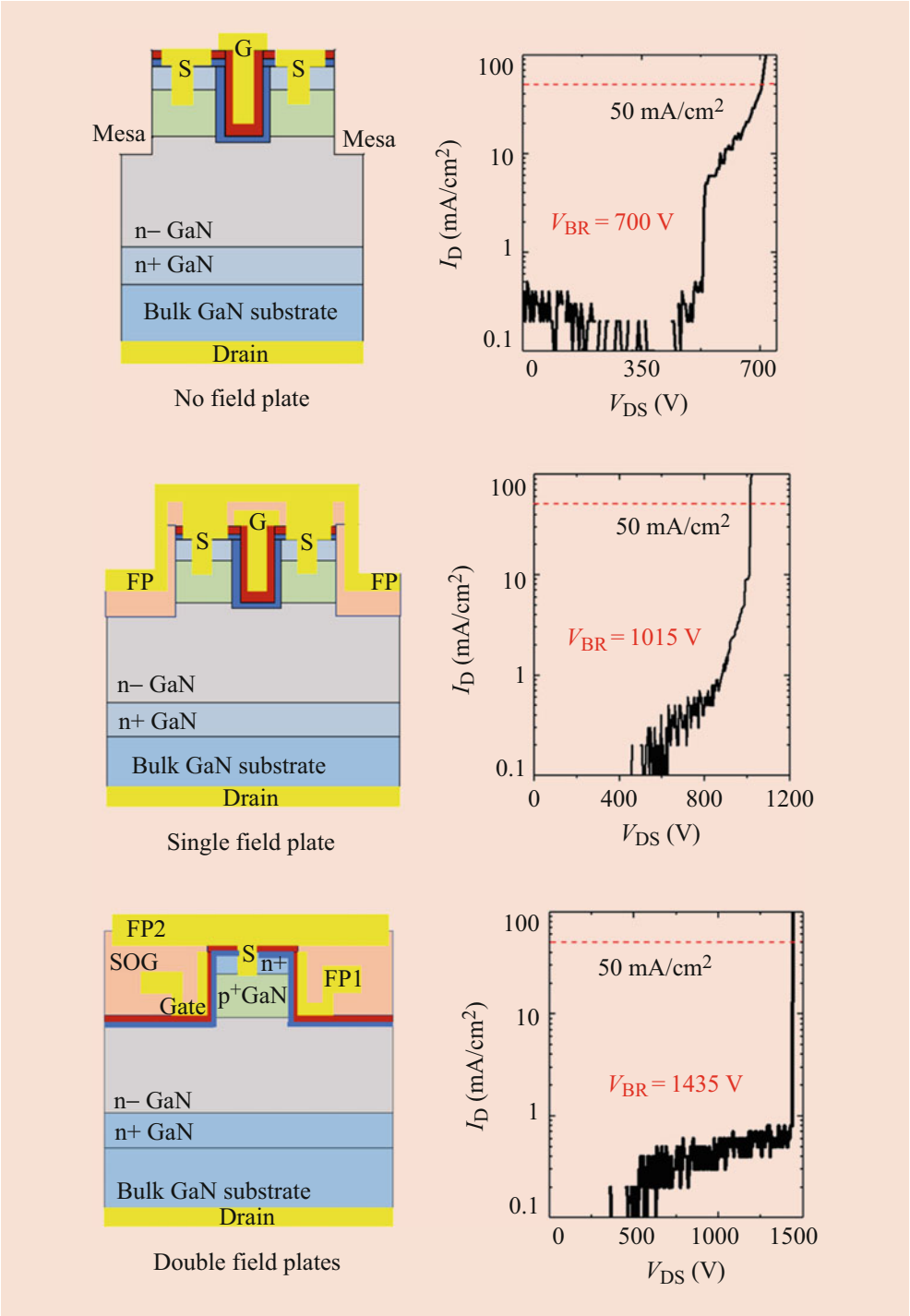

Fig. 15.44 Off-state characteristics of the fabricated OGFETs with no field plate (mesa etch only), single field plate, and double field plates. With the help of the double-field-plate structure, a 1.4 kV breakdown voltage was achieved [82]. (© 2017 IEEE. Reprinted, with permission, from D. Ji et al. [82])

the potential barrier height becomes lower, allowing the thermionic electrons to pass through the barrier.

SITs in GaN form a useful set of devices where without any p-type layers or any gate oxide, one can realize a transistor.

15.3.9 Conclusions on GaN Vertical Transistors

In this chapter, we have discussed the importance of TCAD models in GaN. We went through the details of setting up a model that gives us a scope to study devices inside a

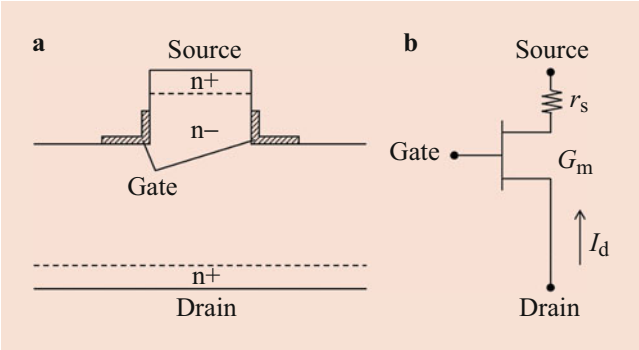

Fig. 15.45 (**a**) Schematic cross-section of static induction transistor and (**b**) its equivalent circuit

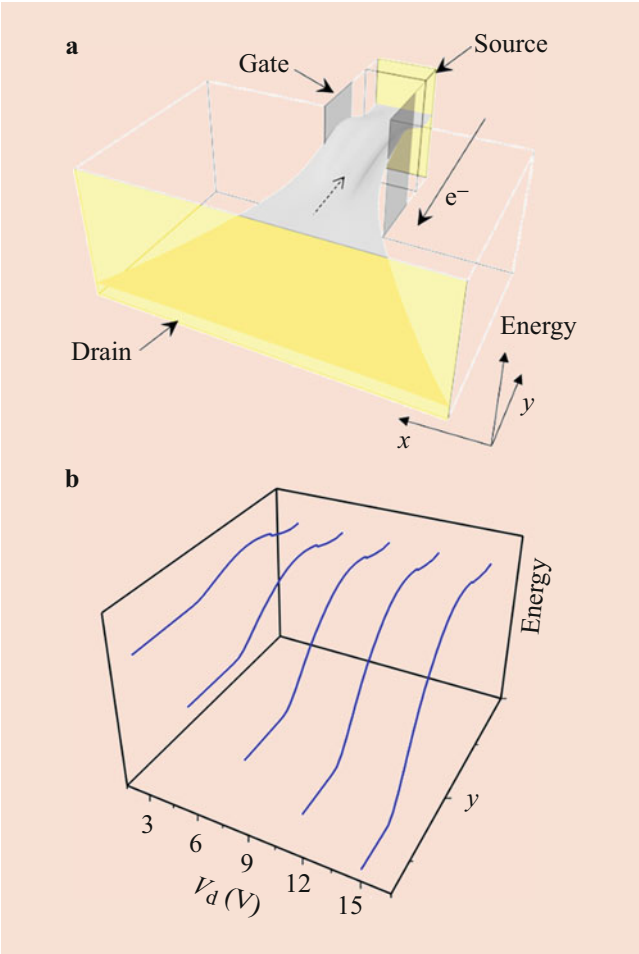

Fig. 15.46 (**a**) Schematic diagram of potential distribution in SIT. (**b**) Dependence of the minimum barrier height, which is pointed by a dashed arrow in (**a**), on the drain bias

power converter application. We went through the operation principles of three important variations of vertical devices possible in GaN. CAVET, MOSFET, and SITs, discussed in this chapter, come with their unique advantages and limitations. In terms of their applications, all three flavors of vertical device would play a significant role. In our view, a SIT is suited for 200–600 V application, a CAVET is best suited for operations up to 900 V and above 900 V, v-MOSFETs are the best candidates. Besides playing a role as a potential power electronic switch, SITs can be used for RF amplification application, making it quite versatile.

15.4 Parasitics and Reliability

In this section, we discuss the main parasitic mechanisms that limit the performance of GaN-based devices, with a specific focus on charge trapping. In addition, we describe the most relevant degradation processes and their impact on device characteristics and lifetime.

15.4.1 Charge-Trapping in GaN-Based Power HEMTs

GaN power devices have unique properties compared to conventional silicon transistors. Specifically, GaN transistors take advantage of the high mobility of the 2-dimensional electron gas and have a very low on-resistance. As an example, commercially available devices can have an on-resistance of 25 mΩ for a 60 A transistors, see [89]. In addition, the breakdown field of GaN (3.3 MV/cm) is more than 10 times higher than that of silicon, and this enables high voltage operation [90]; kV-range devices have already been demonstrated, thus clearing the way for 1200 V GaN-based technology [91]. Finally, GaN is a wide-bandgap semiconductor ($E_g = 3.4$ eV), and for this reason devices based on GaN can be operated at high temperatures (functional operation was demonstrated up to 900 °C, see [92] for details). The fact that GaN can operate at such high temperatures and electric fields may pose significant limitations in terms of trapping and reliability. In this section, we will focus mostly on charge trapping processes, which may limit the dynamic performance of the devices.

In absence of defects, the two-dimensional electron gas of a HEMT should always have a high mobility; unfortunately, when GaN devices are fabricated, point and extended defects are inevitably incorporated in the material.

Defects in GaN may be intrinsic or extrinsic: intrinsic defects include vacancies, self-interstitials and antisites, and their presence is strongly influenced by the growth conditions. Extrinsic defects originate from impurities introduced by growth (such as carbon, hydrogen, oxygen), dopants (such as magnesium, silicon, carbon), or external contaminants. Surface defects can also play a role, especially at interfaces, in presence of a non-optimized passivation.

Several papers have been published on defects in GaN: a comprehensive list of relevant references in this field can be

found in [93]. Here we list the most common defects, along with some key publications on the topic.

- Nitrogen vacancies have been identified and studied in several GaN-based devices, with relatively shallow activation energy, in the upper half of the bandgap (E_C – 0.09 eV/E_C – 0.27 eV) [94–97].
- Mg-related acceptors are typically located 0.16–0.20 eV above the valence band and may be present both in GaN-based optoelectronic devices and in normally-off transistors with p-GaN gate [98].
- Nitrogen antisite defects have been detected in GaN samples and devices in the energy range between E_C – 0.5 eV and E_C – 0.62 eV [96, 99–103].
- Iron and iron-related defects have been investigated by Silvestri et al. and detected at E_C – 0.72 eV [104, 105].
- Gallium vacancies (that have been correlated to the presence of yellow luminescence in GaN, see [106] and references therein) typically have activation energies in the range E_V + 0.85/E_V + 0.94 eV (see [107, 108]).
- Substitutional carbon (or carbon at nitrogen site, C_N) has been also indicated as a source for yellow luminescence in GaN [109]. C_N is typically located at E_V + 0.9 eV and plays an important role in determining the electrical properties of GaN-based transistors [110].

Dislocations have been found to significantly impact on the density and concentration of deep levels in GaN-based materials and devices; recent papers have described the activation energy of defects whose concentration increases with dislocation density (see for instance [95, 111, 112]).

In a GaN power HEMT, traps may be present at several locations within the device structure and several mechanisms may lead to charge trapping. With reference to Fig. 15.48, we discuss briefly the following processes:

1. The trapping of charge in the gate stack (mechanism 1 in Fig. 15.48); this process results in a shift of threshold voltage, whose sign depends on the type of trapped carrier. Trapping of electrons induces a positive threshold voltage shift and may be particularly severe for metal-insulator-semiconductor (MIS) structures, as discussed in several recent reports (see, for instance, [113–117]). In the case of MIS structures, electrons can be trapped at high positive gate bias, being injected at the dielectric/semiconductor interface, or in the dielectric itself [116]. GaN power transistors with a p-GaN gate may also suffer from hole trapping, that leads to a negative threshold voltage shift when the devices are submitted to positive gate stress [90, 118].
2. The trapping of hot-electrons within the AlGaN barrier or in the GaN channel/buffer layers (mechanism 2 in Fig. 15.48). This process can impact the on-resistance of the devices and worsens the performance of the transistors [119, 120].
3. The ionization of buffer traps; this process is prevalent when the devices are in the off-state, and the buffer is significantly depleted (mechanism 3 in Fig. 15.48). Ionization of buffer traps can be promoted by the injection from the silicon-substrate [10, 110, 121].
4. The injection of electrons at surface states located in the access regions (mechanism 4 in Fig. 15.48), with consequent increase in the resistivity of the access regions [122]. This effect can be mitigated through the optimization of the surface treatments and passivation.

15.4.2 Methods to Investigate Charge-Trapping Phenomena

In power devices, the gate-drain spacing is much longer than the gate length and the gate-source spacing. Trapping in the gate-drain access region can significantly lower the on-resistance of the devices, leading to the so-called dynamic-R_{on} issue. Trapping under the gate may lead to positive- or negative-threshold bias instabilities (PBTI or NBTI). The de-trapping time-constants of known traps in GaN are in the range between 1 μs and 100–1000 s, depending on the temperature and activation energy [93]. As a consequence, a careful optimization of the material and interface properties is needed in order to ensure than power GaN HEMTs can reach operating frequencies in the range 100 kHz–10 MHz, needed for the applications [123, 124].

Several techniques have been proposed for the investigation of trap properties in GaN-based transistors. We discuss here one of the most commonly adopted, the drain-current transient (DCT) spectroscopy, which is quite similar to current deep-level transient spectroscopy (I-DLTS). A typical schematic of the measurement setup is reported in Fig. 15.49, as presented by Bisi et al. in [125]. The gate and the drain are driven by two independent pulse generators, whose output is amplified by two power amplifiers. The devices are biased through a resistive load (R_{sense} in Fig. 15.49); the drain-source voltage (V_{DS}) is measured through a voltage probe, while the drain current (I_{DS}) is measured through a high voltage differential probe. Both probes are connected to an oscilloscope, controlled by a computer. Such systems can be used both on device and on wafer level, for the dynamic characterization of the transistors up to 600–1200 V. Typically, transient measurements are carried out after a double-pulsed measurement has been performed, to evaluate the total increase in dynamic R_{on} induced by trapping. The measurement sequence for DCT is as follows: the devices are first kept in a trapping bias point (e.g., in the off-state, point

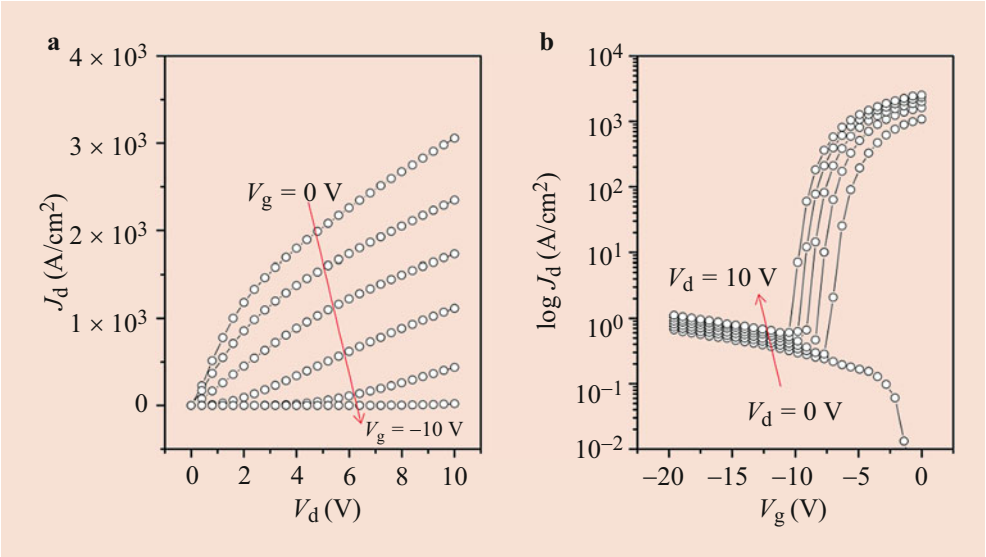

Fig. 15.47 (**a**) Output characteristic of the GaN SIT. The V_g was applied from 0 to −10 V in a step of −2 V. (**b**) Corresponding semilog transfer curve. The V_d biased from 0 to 10 V in 2 V steps

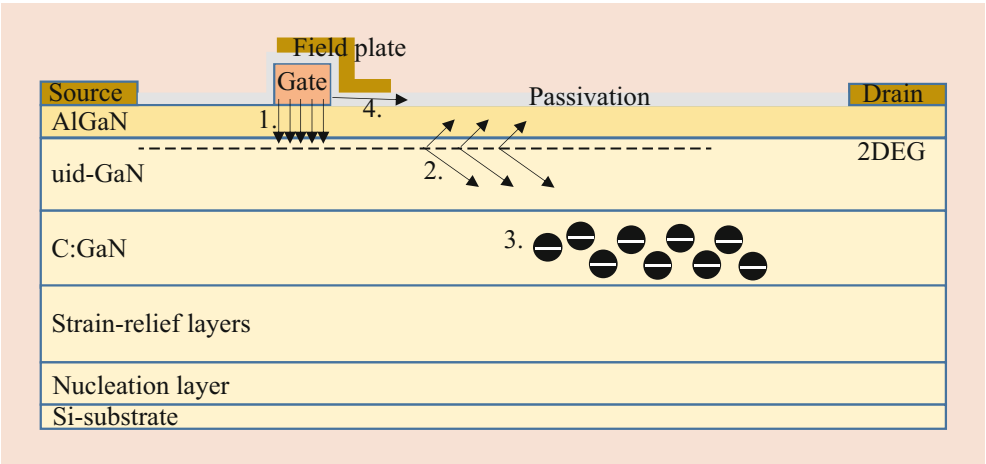

Fig. 15.48 Schematic representation of a GaN-based power HEMT, showing different possible locations for traps and trapping processes. (1) Trapping in the gate stack; (2) injection of hot-electrons in the barrier or in the buffer; (3) ionization of acceptors in the buffer; (4) injection of carriers at surface states

F in Fig. 15.49b), for a relatively long time (10–100 s). This ensures filling of all traps. Then, devices are turned-on, with the aim of reaching a bias point in the linear regime (point M in Fig. 15.49b). The evolution of the current transient during the turn-on phase is measured, and the changes in dynamic on-resistance are probed.

Figure 15.50 reports the results of double-pulsed measurements carried out on a GaN transistor; trapping was induced by exposing this device to off-state conditions. As can be noticed (Fig. 15.50a), increasing stress bias induced a significant increase in on-resistance. The physical properties of the traps responsible for the increase in dynamic-R_{on} were extrapolated by means of R_{on}-transient measurements (Fig. 15.50b). As can be noticed, right after turn-on the value of on-resistance is significantly higher than the reference value (at 100 s), and a gradual recovery transient is observed with increasing times from 1 μs to 100 s. Figure 15.50c reports the derivatives of the drain-current transients with respect to logarithmic time ($dR_{ON}/\log(t)$, DCT spectral plot). The position of the peaks of these curves are related to the time constant of the traps, while the peak height is related to trap density.

Plots like Fig. 15.50c give only a qualitative idea of the trapping and de-trapping processes and provide a visual representation of the mechanisms. A more quantitative investigation can be done by stretched- or multi-exponential

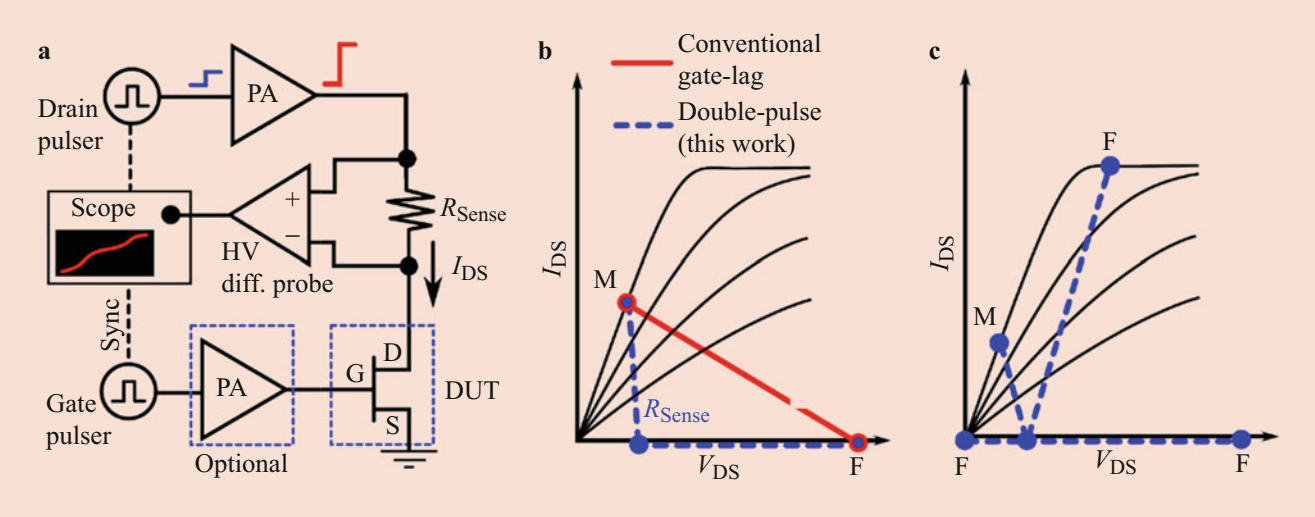

Fig. 15.49 (**a**) Conceptual schematic diagram of the proposed high-voltage double-pulsed system, including the low-voltage pulse generators, the high-speed power amplifiers, the high-voltage differential probe devoted to the current probing, and the oscilloscope. (**b**) Comparison between the conventional fixed-V_{DD} gate-lag technique and the proposed double-pulsed technique. The latter allows the releasing of the load-line constrains and the de-coupling of Filling/Measuring (F/M) bias-pairs. (**c**) Examples of filling and measuring bias-points which would require negative load-resistors, achievable only with the proposed double-pulsed technique. (© 2014 IEEE. Reprinted, with permission, from [125])

fitting of the de-trapping transients, that permit to extrapolate the time-constants of the de-trapping processes [120]. In a recent paper [93], Bisi et al. presented a comprehensive comparison of three different methods for the extrapolation of time-constants from drain-current transients: (i) fitting of transients by polynomial function and subsequent extrapolation of τ from the peaks of the derivative curves $dR_{ON}/\log(t)$; (ii) the fitting of the current transients as the sum of 100 exponentials with fixed time constants and variable amplitudes; and (iii) the fitting by means of a stretched multi-exponential function

$$I_{DS}(t) = I_{DS,final} - \sum_{i}^{N} A_i e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \tag{15.22}$$

where the fitting parameters represent the amplitude of the individual exponentials (A_i) and the related time constant (τ) and stretching factors (β_i) [126]. The stretching factor is introduced to take into account the non-ideality of the de-trapping processes, that can deviate from pure exponential due to (a) the presence of multiple deep levels; (b) a high density of defect states, that leads to the creation of mini-bands [127, 128]; (c) the fact that transients originate from the presence of defect states in alloys, such as AlGaN, which lead to multiple defect signatures [129]; and (d) de-trapping can be governed by non-purely thermal processes, such as hopping or tunneling [130, 131]. All the three techniques described above can provide an estimate of the time constants and be used for the extrapolation of the Arrhenius plot of the traps. However, a recent paper [93] indicated that the time constants extrapolated by polynomial fitting and fixed-time constant exponential can be significantly different from those extrapolated by stretched exponential fitting, since several traps feature a non-purely exponential behavior. Care must be taken to identify, case by case, the most suitable technique for the study of the de-trapping transients and for the identification of the related time constants.

For GaN power devices, the de-trapping kinetics are investigated in the linear regime, i.e., with a low V_{DS} (e.g., 0.5–1 V). For this reason, the activation energy is not strongly influenced by Poole-Frenkel effects, i.e., by a field-assisted change in the de-trapping barrier. However, if de-trapping transients are measured in the saturation region, a higher field may be present, that can modify the de-trapping kinetics. For more information on the role of Poole-Frenkel phenomena one can refer to [132], that shows that in presence of electric field, the de-trapping barrier decreases by an amount $\Delta\phi_{PF}$, proportional to the square root of the electric field F according to

$$\Delta\phi_{PF} = \left(\frac{q^3}{\pi\varepsilon}\right)^{\frac{1}{2}}\sqrt{F} = \beta\sqrt{F} \tag{15.23}$$

As a consequence, the ionization energy (E_i) of a trap is modified with respect to the zero-field value $E_i(0)$ according to

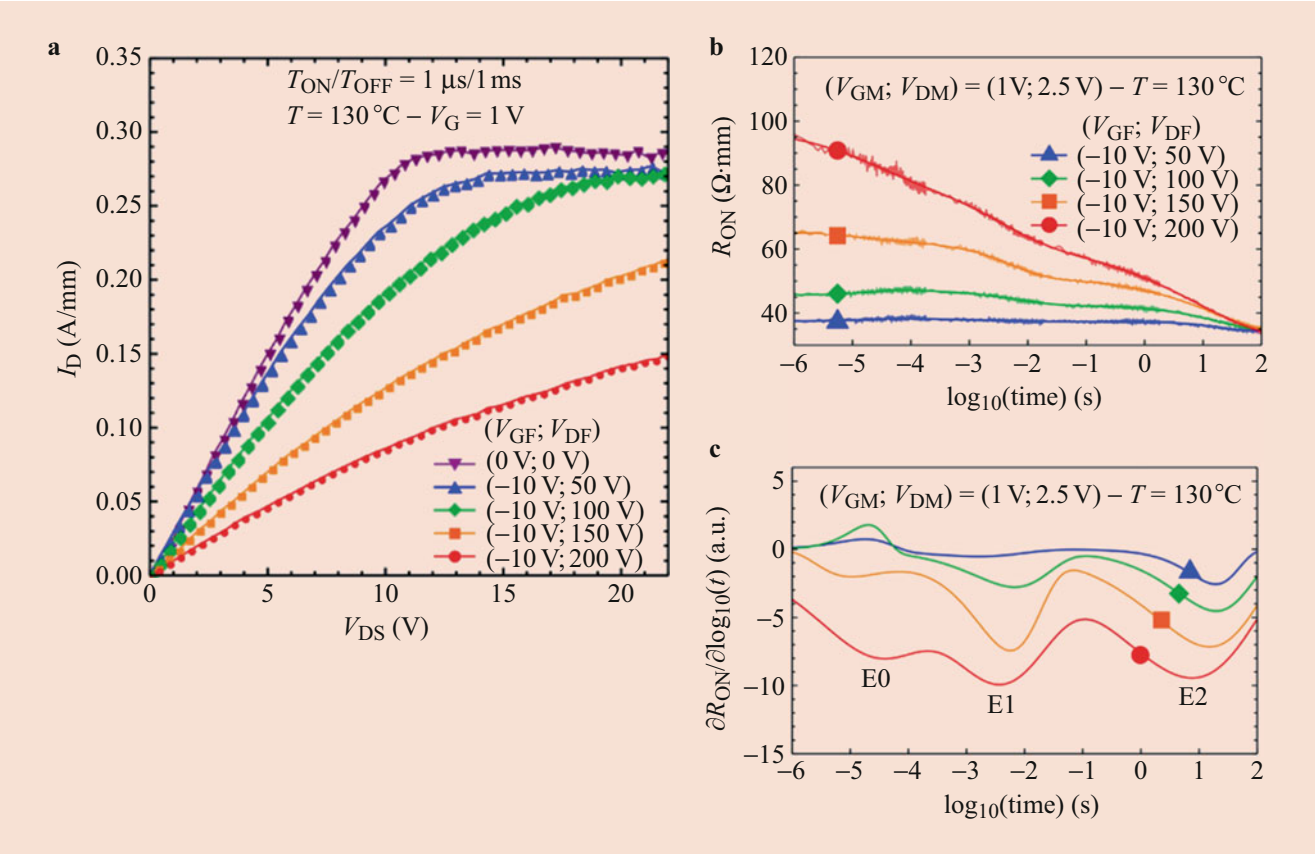

Fig. 15.50 (**a**) Double-pulsed I_D–V_D characterization with high-voltage off-state (V_{GF}; V_{DF}) quiescent-bias-points. As the quiescent drain-voltage is increased from 50 to 200 V, the device experiences a dramatic increase of the dynamic R_{ON}. (**b**) Time-resolved dynamic R_{ON} recovery transients, and (**c**) derivative of the stretched-exponential fit-functions, employed to extrapolate the three distinct deep-levels signatures. Three dominant charge (de)trapping process can be identified. As the filling drain-voltage is increased from 50 to 200 V, the increase of peak-amplitudes, ascribed to charge-trapping magnitude, can be observed. (© 2014 IEEE. Reprinted, with permission, from [125])

$$E_i(F) = E_i(0) - \beta\sqrt{F} \tag{15.24}$$

It is worth noticing that traps located in a 10^6 V/cm field region can have an activation energy 0.2–0.25 eV smaller than the zero-field energy (see [132] for details).

When analyzing the de-trapping transients, one should also consider the impact of self-heating effects on the extracted activation energy: Chini et al. [133] demonstrated that if devices have a significant self-heating during the de-trapping phase, this can lead to a wrong estimation of the activation energy. By calibrating the temperature data taking into account device self-heating, one can correct the Arrhenius plots and obtain a reliable estimation of the activation energy of the traps. This requires a careful estimation of the thermal resistance of the devices, which must be done on the very same wafer prober used for the DCT analysis. A reliable on-wafer technique for such estimation was proposed by Joh et al. in [134].

15.4.3 Performance and Characteristics of GaN Devices and Challenges

So far we have discussed about the typical traps present in AlGaN/GaN power devices, and about the methods to investigate these traps. Now we will focus on the performance and characteristics of GaN devices.

Figure 15.51 reports the dependence of on-resistance on the trapping voltage and temperature for a GaN (lateral) power HEMT. The used measurement conditions range between 0 V and 600 V (voltage) and between 30 °C and 150 °C (temperature), which are consistent with real-life operation. Dynamic R_{on} has a non-monotonic trend with off-state voltage, in the whole measurement range. An explanation for this behavior can be given based on previous papers [10, 126] and on Fig. 15.51b: at low trapping voltages (<200 V), the buffer (carbon-doped) is partly depleted, thus resulting in the accumulation of negative charge. This increases dynamic-

R_{on} with respect to the de-trapped conditions. In the buffer, the carbon acceptors have energy equal to $E_V + 0.9$ eV. At higher voltages, the increase in vertical (drain-substrate) leakage leads to a re-distribution of charge within the stack. Also, band-to-band conduction may lead to the storage of positive charges at the interface with the strain-relief layer (Fig. 15.51b). As a consequence, for voltages higher than 300 V a decrease in dynamic-R_{on} is observed (Fig. 15.51a). Remarkably, the value of dynamic-R_{on} after stress at 600 V is almost equal to the value under rest-condition, indicating that current technologies have a negligible dynamic-R_{on} increase at high voltage. The interplay between the increase and decrease in dynamic R_{on} can be affected by temperature, as shown in Fig. 15.51a.

From the discussion above, it is clear that there are two strategies to reduce the dynamic-R_{on} in high-voltage GaN transistors. A first approach is to minimize the influence of carbon doping on 2DEG concentration; this can be achieved through optimization of the level of C-doping and of the thickness of the undoped GaN. A second approach is the optimization of the leakage through the unintentionally doped GaN layer; this can favor the redistribution of charge through the structure, without increasing the vertical leakage current too much. Thanks to the continuous optimization of the growth and processing parameters, it is now possible to fabricate devices with zero dynamic-R_{on} both at room temperature and high temperature (see an example in Fig. 15.52, up to 600 V, 150 °C). In [126], drain current transient measurements were carried out to identify the properties of the traps responsible for dynamic-R_{on}. The authors commented that activation energies in the range 0.6–0.9 eV are typically ascribed to acceptors in GaN [135, 136]. It is worth noticing that lateral and vertical charge redistribution can take place during R_{on} measurements, thus slightly changing the activation energy of defects with respect to what expected from theoretical calculations (see details in [137]).

So far, we only discussed charge trapping mechanisms induced by the off-state field. During real-life operation, GaN transistor cross also another regime which is relevant in terms of trapping, the semi-on state. Typically, semi-on conditions are reached during the switching transient, e.g., when in a boost power converter the transistor is switched from off- to on-state. During this transition, there is a short interval during which a high drain voltage and a high drain current are simultaneously present. This leads to the presence of hot-electrons, which can favor charge trapping within the structure of the devices. One strategy for investigating the impact of hot-electrons in a hard switching event is to artificially create hard switching conditions by tuning the overlap between the drain and gate waveform. In [138], Rossetto et al. investigated the impact of soft- and hard-switching conditions on the dynamic-R_{on} of AlGaN/GaN power HEMTs. They used a custom setup that permits to modify the overlapping between drain and gate waveforms

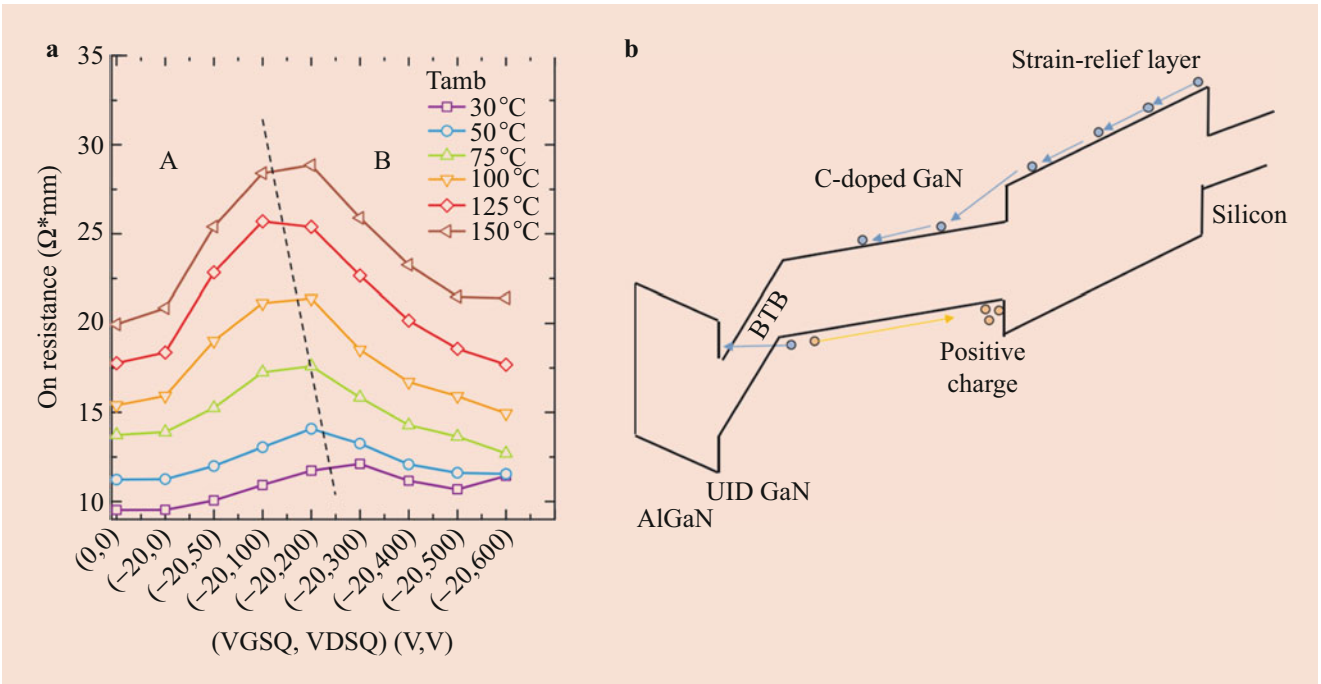

Fig. 15.51 (**a**) Dependence of dynamic-R_{on} (as measured from pulsed I-V measurements) on trapping voltage and temperature. (**b**) Schematic representation of the mechanisms responsible for non-monotonic dynamic-R_{on} as a function of trapping voltage. (Reused from [126], doi: https://doi.org/10.1016/j.mssp.2017.10.009, Creative Commons Attribution License (CC BY) http://creativecommons.org/licenses/by/4.0/)

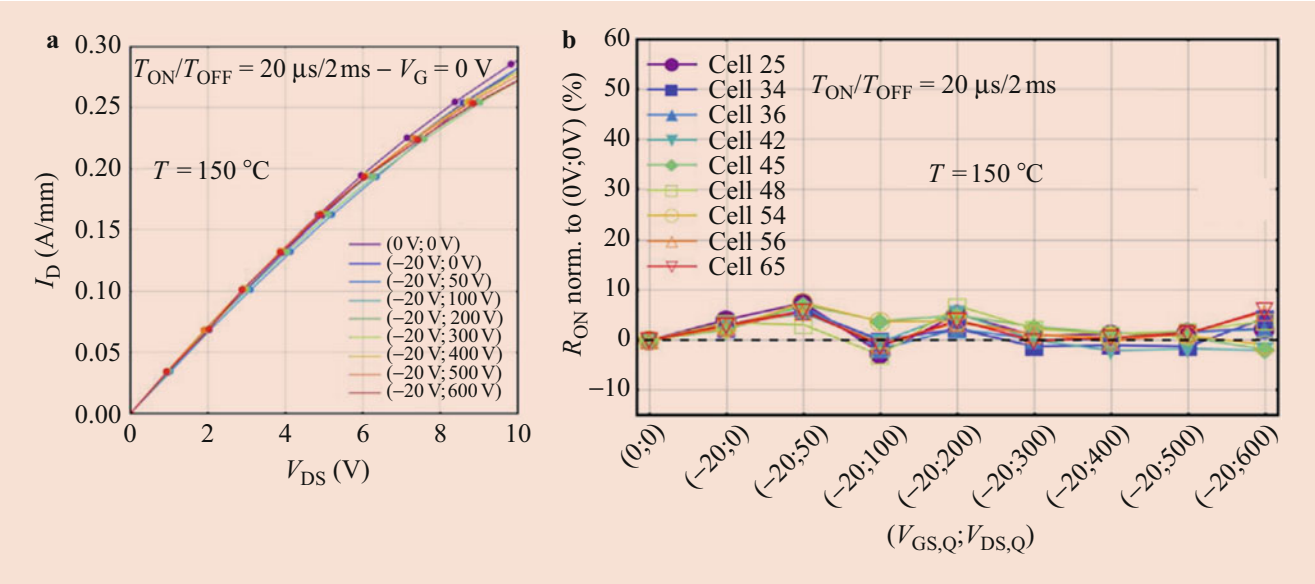

Fig. 15.52 (**a**, **b**) Results of pulsed-IV measurements carried out on an optimized device up to $V_{DS,Q}$ = 600 V, at high temperature. The plot on (**b**) represents the dependence of dynamic-R_{on} (normalized to the value measured with no trapping bias) on trapping voltage. Each line refers to an individual device on the wafer. (Reused from [126], Creative Commons Attribution License (CC BY) http://creativecommons.org/licenses/by/4.0/)

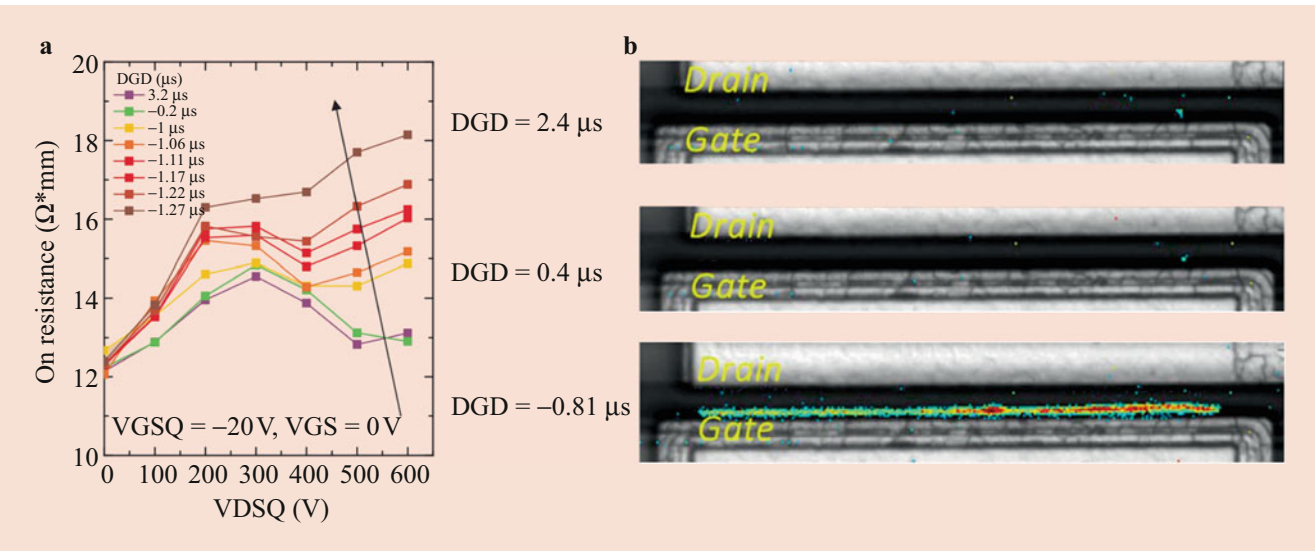

Fig. 15.53 (**a**) Dependence of dynamic-R_{on} on the trapping voltage V_{DSQ} and on the overlapping between the gate and drain waveforms. (**b**) EL patterns measured during soft and hard switching transitions. (Reused from [126], doi: https://doi.org/10.1016/j.mssp.2017.10.009, Creative Commons Attribution License (CC BY) http://creativecommons.org/licenses/by/4.0/)

used to induce charge trapping. The results of their study demonstrated that the investigated samples have a small dynamic-R_{on} up to V_{DS} = 600 V in soft switching. On the other hand, a significant increase in dynamic-R_{on} was observed in hard switching. A representation of this phenomenon is reported in Fig. 15.53a, which shows that the dynamic-R_{on} vs off-state voltage curves change as a function of the parameter DGD (drain-gate delay). This parameter represents the time interval between a drain voltage equal to V_{DSQ}/2 and a gate level equal to the threshold voltage V_{TH}. Therefore DGD is positive for soft-switching transitions and negative for hard-switching transitions. As can be noticed, for DGD < 0 (hard switching) the dynamic-R_{on} is significantly enhanced compared to soft-switching (DGD > 0). The hard switching intervals reached in Fig. 15.53a (µs range) are significantly longer than in real-life operation (where a slew rate of 10–100 V/ns is more realistic), thus corresponding to an extremely stressful scenario.

The increased dynamic-R_{on} measured in hard switching conditions is ascribed to the trapping of hot-electrons within the devices. A confirmation of the presence of hot-electrons was obtained by means of electroluminescence measurements (Fig. 15.53b). No EL signal was measured in soft switching, since no current flows through the devices during the switching transition. On the contrary, under hard switching conditions, EL signal was detected on the whole channel width, with a peak on the drain-side gate edge.

A further mechanism of charge trapping is related to the gate stack; in several cases, V_{th} instabilities have been reported for GaN-based power transistors, causing negative- or positive-threshold bias instability (NBTI or PBTI). The physical origin of such V_{th} shifts are strongly dependent on the gate architectures (e.g., metal-insulator semiconductor, Schottky-gate, p-type gate, etc.).

In MIS-transistors [113–117], threshold voltage instabilities are due to the trapping of electrons at the interface between dielectric and semiconductor or to the injection of charge inside the dielectric [116].

More recent papers indicated that also normally-off GaN power transistors can suffer from threshold voltage instabilities [90, 118, 139, 140]; different mechanisms have been indicated as responsible for the positive and negative threshold voltage instabilities in GaN-based transistors with p-type gate. In [140], the authors suggested that a positive threshold voltage shift may be detected after stressing the devices at $V_{GS} = 1$ V (see Fig. 15.54a, b). This V_{th} variation was ascribed to the injection of electrons from the 2DEG to the AlGaN barrier, which may occur once the 2DEG has been formed (see Fig. 15.54c). For higher voltages, the accumulation of positive charges (holes) in the AlGaN barrier and/or at the passivation/AlGaN interface can induce a negative shift in threshold voltage (Fig. 15.54). Another paper [139] investigated the role of hole accumulation in the p-GaN (causing a negative threshold voltage shift) and hole depletion in the p-GaN (causing a positive threshold voltage shift). This chapter indicated that an unbalance between the hole tunneling current through the Schottky barrier and the thermionic emission on the AlGaN barrier can significantly change the total charge in the p-GaN, thus resulting in V_{th} shift.

Finally, one of the latest trends in GaN technology is the development of vertical transistors. In several cases, an MOS approach is used, in order to ensure a high robustness and a good threshold current. Recently, only few papers on the stability and reliability of GaN-on-GaN vertical devices have been published [141–144]. As an example, we refer here to the results presented in [144]. In this paper, the authors investigated the stability of the threshold voltage of GaN-on-GaN vertical fin field-effect transistors (VFETs). The results of threshold voltage transients indicated the existence of two different trapping processes (Fig. 15.55a). At low voltages, a negative shift in threshold voltage was observed; this effect was ascribed to the de-trapping of electrons from the Al_2O_3 insulator, induced by a low positive bias. At high voltages

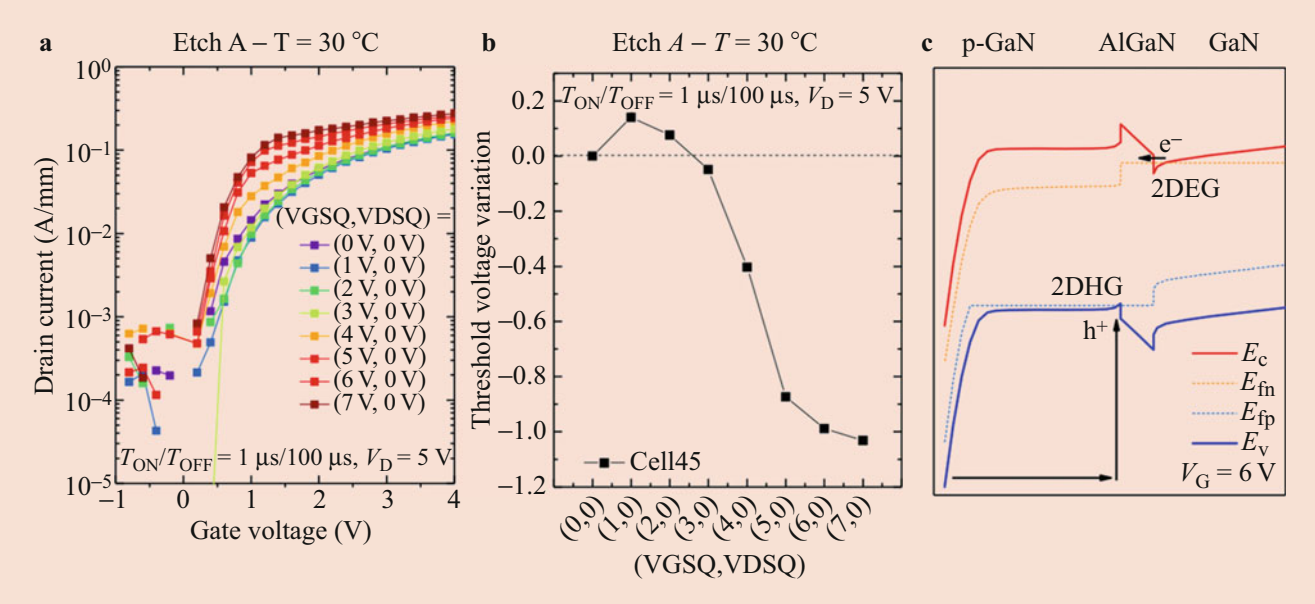

Fig. 15.54 (**a**) drain current versus gate voltage after different forward gate voltage stress; (**b**) pinch-off voltage variation versus forward gate voltage stress; (**c**) band diagram under the region at $V_G = 6$ V (simulated with Sentaurus provided by Synopsis). Two mechanisms are reported: (1) injection of electrons from the 2DEG towards the AlGaN barrier; (2) accumulation of positive charges (holes), injected from the gate. (Reprinted from [140] Copyright 2018, with permission from Elsevier)

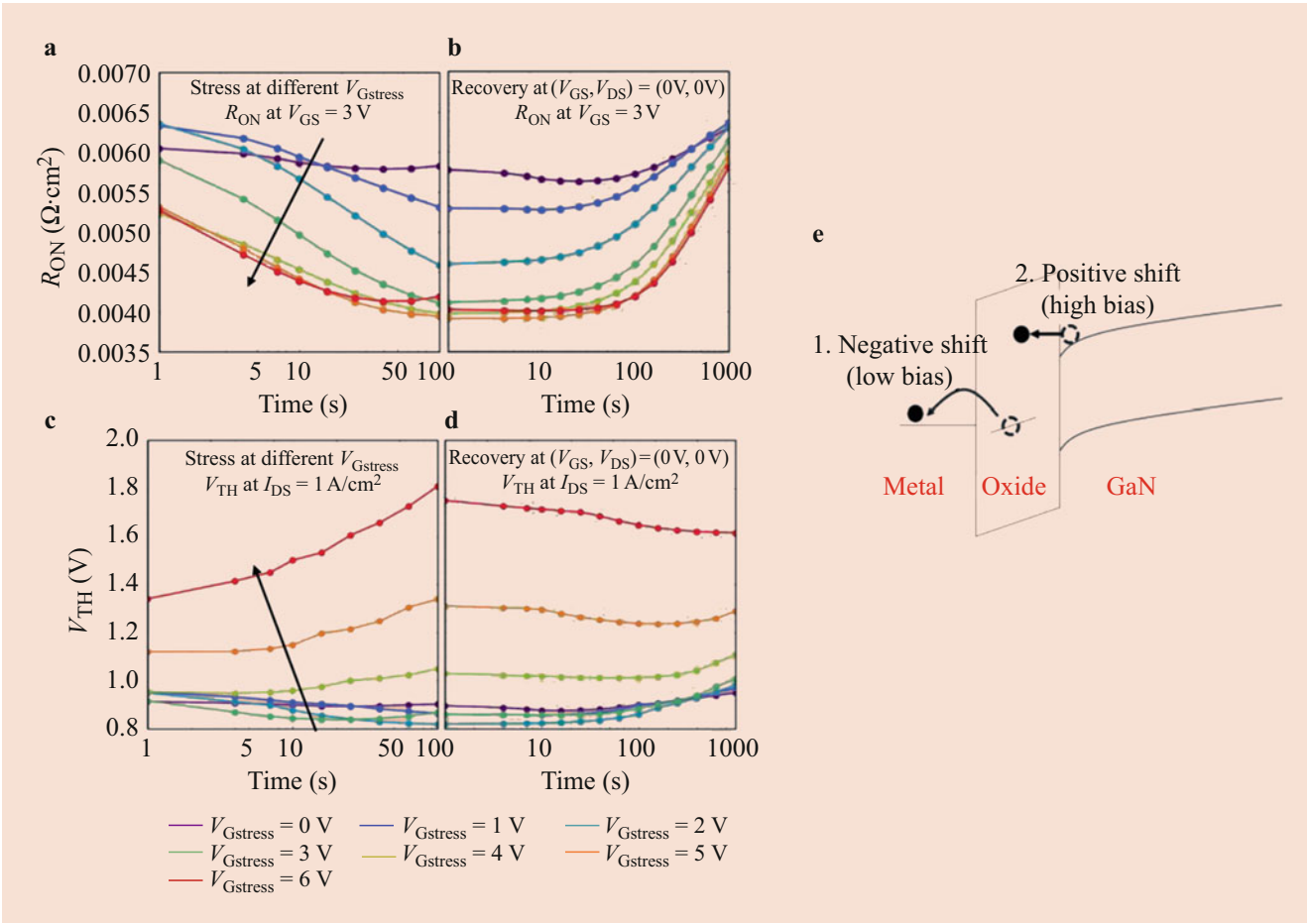

Fig. 15.55 (**a**, **b**) On-resistance and (**c**, **d**) threshold voltage variation during 100 s of (**a**), (**c**) stress at different $V_{Gstress}$ and 1000 s of (**b**), (**d**) recovery (all terminals at zero voltage) at $T_{amb} = 25$ °C. The R_{ON} decrease is a recoverable process. At low stress voltages ($V_{GS} < 2$ V) a negative recoverable ΔV_{TH} is observed; for high stress voltages ($V_{Gstress} > 2$ V) a positive ΔV_{TH} is induced, not recoverable in 1000 s. (**e**) Schematic representation of the two mechanisms responsible for (1) negative and (2) positive threshold voltage shift. The two mechanisms take place at low and high stress voltage, respectively. (© 2017 IEEE. Reprinted, with permission, from [144])

(≥5 V), a substantial positive threshold voltage shift was observed. This process is due to the injection of electrons from the channel to the insulator. The recovery of this second process was found to be slow. A schematic representation of the two processes is given in Fig. 15.55b; see [144] for details.

15.4.4 Reliability Issues of GaN-Based Power HEMTs

Thanks to the unique material properties of GaN, AlGaN/-GaN transistors may be subject to extremely high stress conditions during operation. GaN devices are currently targeting the 600–650 V market segment [89], but research is ongoing to extend to 1200 V and beyond. Current levels can be higher than 50 A on a single component, while – at least for the moment – specifications are quite relaxed for the maximum junction temperature (see, for instance, [89, 145] showing a maximum $T_j = 150$ °C). For E-mode devices, also the maximum gate voltage/current are critical in terms of reliability. In some cases, the maximum gate-to-source voltage is specified in the datasheet (see, for instance, [89], indicating a limit of +7 V), while in some other cases the maximum gate leakage current is defined (see for instance [145], indicating a maximum gate current of 50 mA). Finally, during a switching event GaN power transistors can reach high levels of instantaneous power dissipation; for a representative example, the reader may refer to the results reported by Bahl et al. in [146], showing that in a boost converter, a significant current/voltage overlap is observed during the turn-on phase; peak currents around 15 A were observed when switching from 400 V, resulting in high power densities and hot carrier effects.

Studying the reliability of GaN transistors is a necessary step for the development of this technology. In this section, we describe the most common failure mechanisms that limit

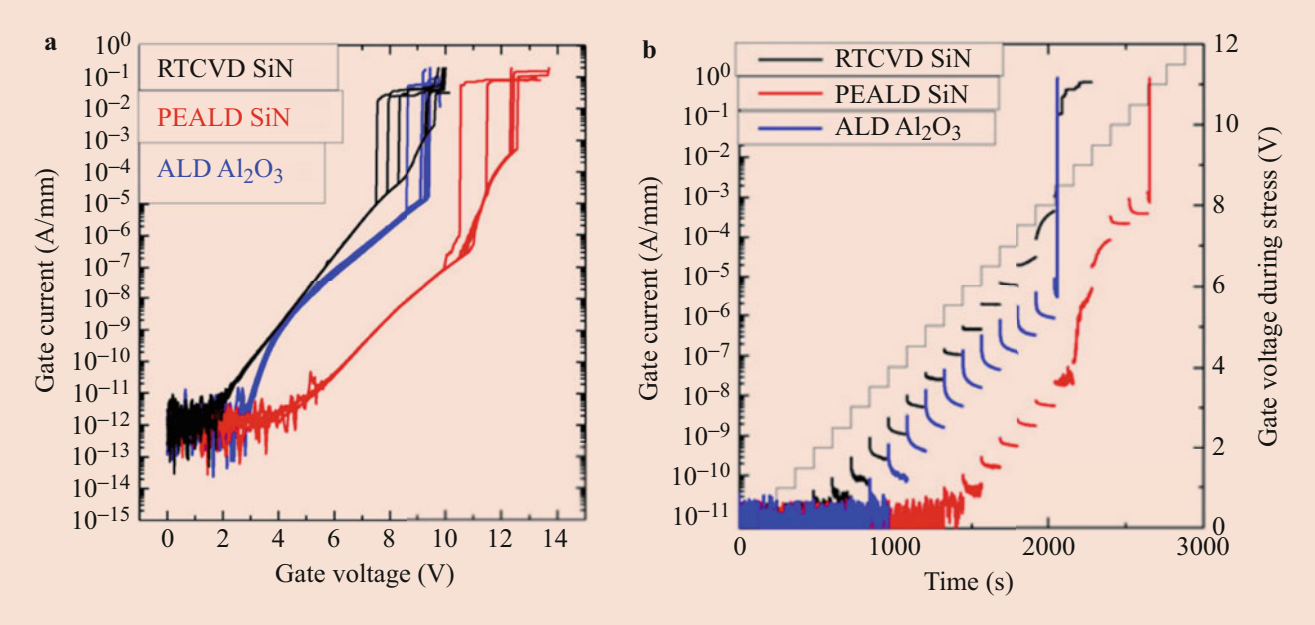

Fig. 15.56 (**a**) Current-voltage breakdown measurements on devices with different gate insulators: RTCVD SiN (black line); PEALD SiN (red line); and ALD Al_2O_3 (blue line). (**b**) Gate current monitored during step stress with drain and source terminals grounded ($V_D = V_S = 0$ V) and increasing V_G in devices with different gate insulators: RTCVD SiN (black solid line), PEALD SiN (red solid line), and ALD Al_2O_3 (blue solid line). Corresponding gate voltage applied during the step stress is reported with a staircase curve. (Reprinted from [147], Copyright 2015, with permission from Elsevier)

the reliability of GaN power devices, along with a description of the related root causes.

15.4.5 Gate-Stack Reliability

As discussed above, the two most studied technologies for the fabrication of the gate are metal-insulator-semiconductor (MIS) and p-GaN gate. The threshold voltages of commercial GaN HEMTs are around 1.1–1.3 V [89, 145], and a certain overdrive is required. For instance, the datasheet of [89] indicates a gate drive range from 0 V to 6 V. For this reason, it is important to evaluate the stability and reliability of GaN transistors at high positive gate voltage and to define proper ways to extrapolate acceleration factors and lifetime.

For insulated-gate devices, the time-dependent failure of the gate dielectric is one of the most relevant degradation process. This mechanism is similar to what has been detected and studied in silicon devices and leads to a catastrophic failure of the gate when a prolonged high-voltage stress is applied to the samples.

As a representative example, we refer here to the case of partially recessed GaN HEMTs with insulated gate. In [147], Meneghesso et al. studied the breakdown voltage of three different wafers of transistors with a residual AlGaN thickness of 3.7 nm, having three different gate insulators: a 15 nm SiN layer deposited by rapid thermal chemical vapor deposition (RTCVD); a 15 nm SiN layer deposited by plasma-enhanced atomic layer deposition (PEALD); and a 15 nm Al_2O_3 layer, deposited by atomic layer deposition (ALD). The results of this study indicated that devices with PEALD-SiN insulator have a leakage more than three orders of magnitude lower than the two other wafers (Fig. 15.56a). In addition, devices with PEALD-deposited SiN were found to have a higher robustness at positive gate voltage (average failure voltage = 11.9 V), compared to RTCVD-SiN and Al_2O_3 (8.65 V and 9.25 V, respectively).

The breakdown voltage evaluated by a simple dc sweep is not fully representative of the real device robustness under long-term stress; typically, step-stress experiments and constant-voltage stress tests are carried out with the aim of analyzing the failure distributions and the related statistics. Figure 15.56b reports the results of a step-stress experiment carried out on one device per wafer; gate voltage was increased by 0.5 V every 120 s, while monitoring the electrical parameters. For positive stress voltages (and above threshold), the 2DEG is fully formed, and a high electric field builds across the residual AlGaN layer and the gate insulator. Such field is rather uniform, since the metal and the 2DEG act as the two plates of a capacitor. As can be noticed, the properties and quality of the dielectric strongly influence the overall reliability of the devices. In addition, the samples with

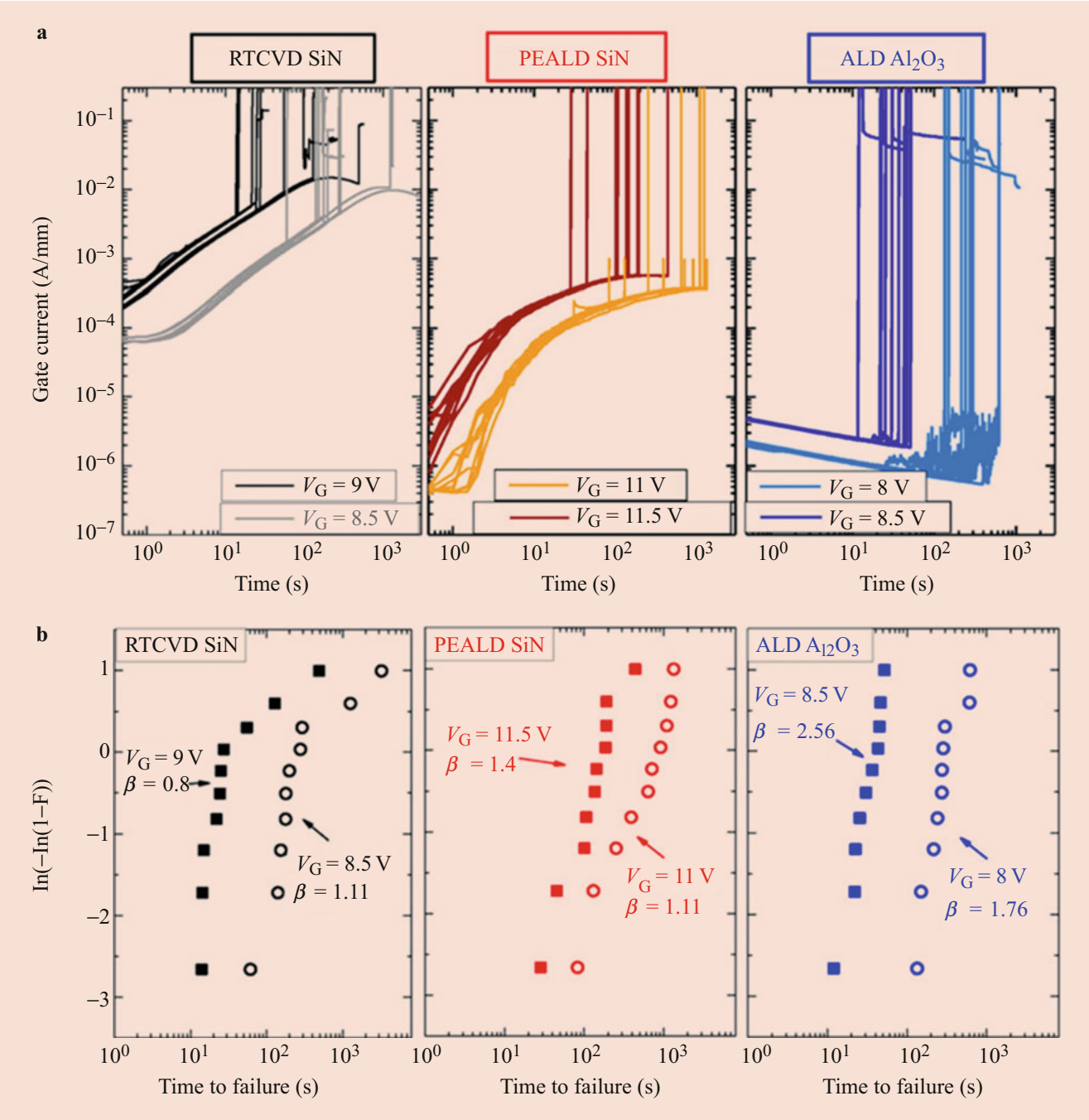

Fig. 15.57 (**a**) TDDB measurements performed on devices with different insulating layers: RTCVD SiN (black line), PEALD SiN (red line), and ALD Al_2O_3 (blue line). (**b**) Weibull plot on devices with different insulating layers: RTCVD SiN (black line), PEALD SiN (red line), and ALD Al_2O_3 (blue line). (Reprinted from [147], Copyright 2015, with permission from Elsevier)

PEALD SiN and RTCVD SiN show a sudden increase in gate leakage at the end of the stress experiment.

Representative results on the effect of constant-voltage stress on the gate leakage of insulated-gate HEMTs are shown in Fig. 15.57. In Fig. 15.57a, we report the variation of gate leakage during a constant voltage stress (ten devices per stress condition, two voltages per insulating material). As expected, by increasing stress voltage a decrease in time-to-failure is observed. Time-to-failure is generally Weibull-distributed (see the Weibull plots in Fig. 15.57). In the example reported in Fig. 15.57b, the shape parameter β does not strongly depend on stress voltage and is around 1.1–1.5, i.e.,

indicative of intrinsic failure. A more detailed analysis of the failure of MIS-HEMTs and related TDDB was given by Wu et al. in [148]. The authors of this chapter demonstrated that the Weibull distribution scales with gate width, confirming the hypothesis on intrinsic failure. In addition, they extrapolated the lifetime to 0.01% of failures at 150 °C, 20 years ($W_g = 36$ mm), giving voltages of 4.9 V (power law) or 7.2 V (exponential law).

In a recent paper [149], Warnock and del Alamo discussed the physical origin of progressive breakdown (PBD) in high-voltage GaN-based MIS-HEMTs. They observed PBD, characterized by a rapid increase in gate leakage noise, taking place before hard breakdown. They indicated that the degradation does not take place at the AlGaN/GaN interface. Their results were found to be consistent with those obtained on silicon MOSFETs [150], supporting the percolation model to explain PBD and hard breakdown.

The time-dependent breakdown of dielectrics can be critical also for vertical GaN devices. Several vertical transistor structures have been recently proposed: the current aperture vertical electron transistor (CAVET) [71], which is based on the use of a current-blocking layer, used to stop vertical current flow through any path other than the aperture to the drain; the V-MOSFET or trench-MOSFET (also modified in the recent OG-FET layout) [81], where a buried p-type GaN layer is used to increase the threshold voltage of the devices; and the vertical fin power-FET [151] and vertical nanowire-FET [152], where current flow is accurately controlled through the use of nanometer-size channels. In most cases, a dielectric is placed under the gate; this dielectric layer can be exposed to high electric fields, especially when the devices are in on-state.

An example of this has been presented by Ruzzarin et al. in [143]. The authors of this paper studied the stability and degradation of vertical fin power-FETs submitted to positive gate stress. The analyzed devices have a vertical metal/insulator/semiconductor layout, where the semiconductor is *n*-type. When submitted to positive gate stress, an accumulation layer is formed in the semiconductor, at the interface with the dielectric. At high gate bias (>7 V), the field in the 15 nm dielectric becomes high and can favor a time-dependent breakdown of the oxide. Specifically, a soft failure was observed at a stress voltage equal to $V_{Gstress} = 7.25$ V (corresponding to an abrupt increase in gate leakage, Fig. 15.58). A catastrophic failure was detected at $V_{Gstress} = 8.75$ V (~6 MV/cm in the gate insulator, Al_2O_3).

Results of simulations (Fig. 15.59) indicated that in vertical fin power-FET at high drain voltage the electric field peaks at the corner of the dielectric. This is supposed to be the region where failure takes place at high drain bias, in the off-state. Strategies for reducing the field in the material

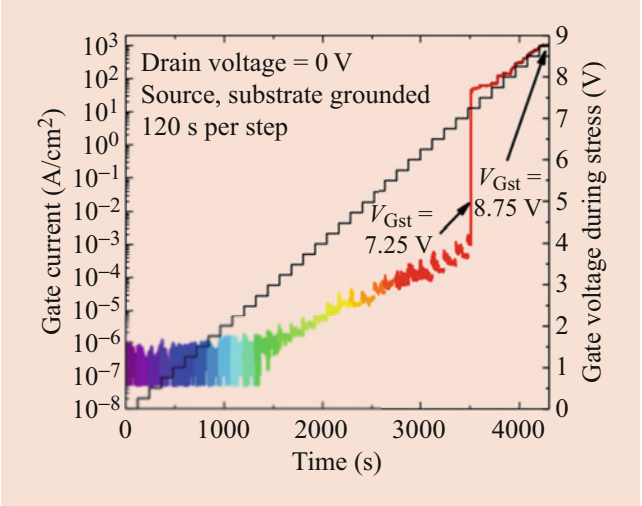

Fig. 15.58 Step stress performed with $V_{Dstress} = 0$ V and by increasing the $V_{Gstress}$ by 0.25 V each 120 s of stress. A positive gate stress induces a permanent increase in gate current, for stress voltages higher than 7.25 V, due to the breakdown of the gate dielectric. The catastrophic failure occurs at $V_{Gstress} = 8.75$ V. (© 2018 IEEE. Reprinted, with permission, from [143])

can be adopted to significantly improve the robustness of the transistors at high drain bias.

For devices with p-GaN gate, different degradation mechanisms have been proposed over the past years. The metal/p-GaN interface can be either Ohmic or Schottky [153]. The second approach allows to substantially reduce the leakage at the gate. When a Schottky junction is created on p-GaN, the resulting stack can be modeled as the back-to-back combination of two diodes. The first results from the metal/p-GaN Schottky junction, and the second is represented by the p-GaN/i-AlGaN interface [154]. Wu et al. [155] analyzed the forward-bias breakdown mechanisms in Schottky metal/p-GaN gate HEMTs. They demonstrated a positive temperature dependency of the gate breakdown voltage, with a coefficient equal to 5×10^{-3} C/V. They demonstrated that – on average – the breakdown voltage at 200 C is 1 V higher than at 25 C. They explained this positive temperature dependence by considering the avalanche multiplication in the space charge region that is present at the metal/p-GaN junction. The electrons can transfer to the p-GaN and be accelerated by the high field in the depleted region. Further, they were able to observe the presence of avalanche luminescence, suggesting that high gate voltages may lead to the generation of electron-hole pairs.

Tapajna et al. [156] analyzed the effect of forward stress on normally-off p-GaN/AlGaN/GaN HEMTs. They indicated that the time-dependence of the gate current increase is consistent with percolation process. By using the Weibull statistics, they estimated the maximum gate voltage

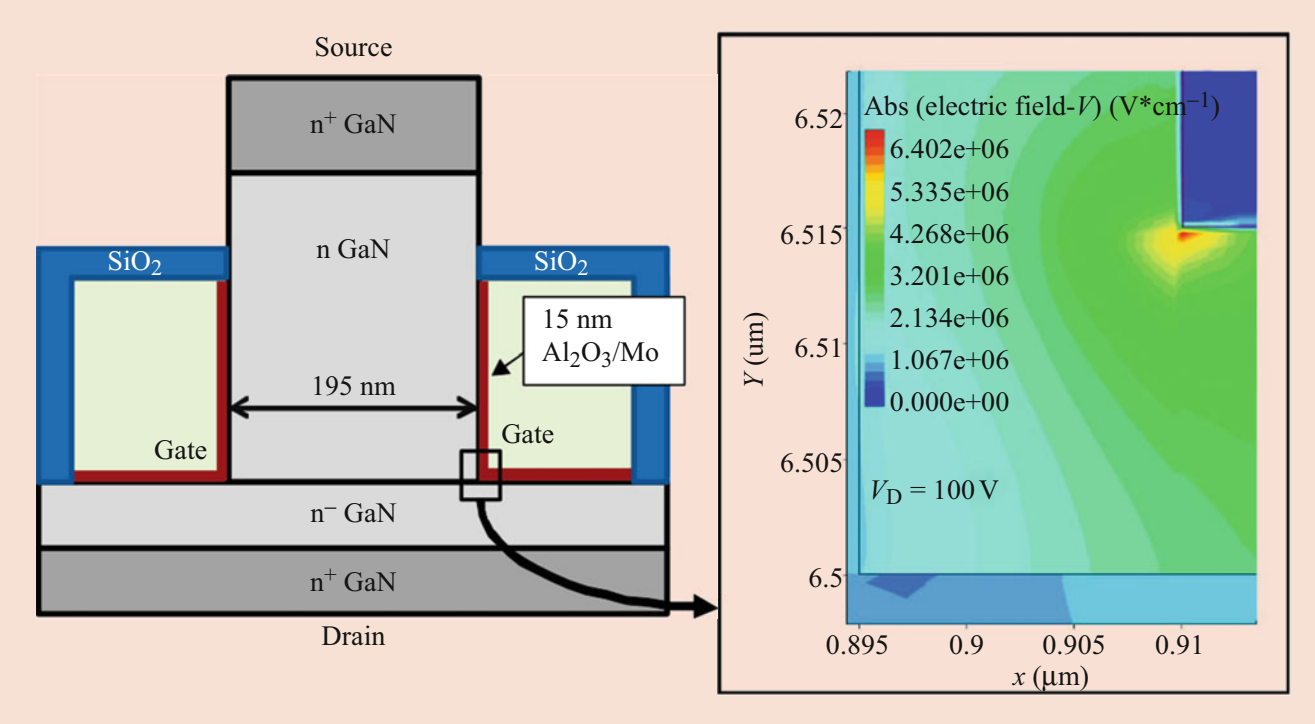

Fig. 15.59 Simulation of the electric field at the dielectric/GaN channel interface at higher drain voltages (in the real device the fin corners are not exactly 90° corners). (© 2018 IEEE. Reprinted, with permission, from [143])

for long-term operation. In addition, they demonstrated that the observed degradation process has a low activation energy.

Tallarico et al. [154] demonstrated that the time-to-failure of GaN-on-Si power HEMTs with p-type gate follows a Weibull distribution. Also, they suggested that the time-to-failure is a function of the initial gate leakage, with higher gate leakage corresponding to a shorter lifetime. They suggested that breakdown is related to the creation of a percolation path in the p-GaN layer.

Rossetto et al. [153] analyzed the influence of the Mg doping concentration on the robustness of AlGaN/GaN HEMTs at positive gate overstress. They proposed a method to separately investigate two different processes, namely, (a) a field-driven breakdown of the metal/p-GaN Schottky junction, induced by TLP test with short pulses. High Mg doping correspond to higher junction fields, thus resulting in lower failure voltages. (b) A current-driven process detected during long-term stress, ascribed to the accumulation of charge at the p-GaN/AlGaN interface [157]. For this process, an increase in Mg doping was found to improve the stability.

In a more recent paper, Masin et al. [158] demonstrated that GaN-HEMTs with p-GaN gate can show a time-to-failure with positive temperature coefficient, when submitted to positive gate stress. They ascribed degradation to the accumulation of holes at the p-GaN/AlGaN interface. This is supposed to increase the injection of electrons from 2DEG to p-GaN, which are then accelerated by the electric field. This eventually leads to defect generation and breakdown.

15.4.6 Off-State Reliability

Another relevant regime where GaN transistors can undergo significant stress is off-state bias, i.e., (for e-mode devices) a null gate voltage and a high (up to 600–650 V) drain voltage. Recent papers have investigated the impact of high off-state bias on the electrical characteristics of GaN transistors (see, e.g., [159–165]). Under off-state conditions, two main factors can promote the degradation of the devices. First, the high lateral field, between gate and drain, can promote a failure of the devices in proximity of the top epitaxial and/or passivation layers. In this case, we refer to "lateral breakdown," since the mechanism originates from the lateral field. Second, in off-state conditions a high bias is present also between drain and substrate. This creates a significant vertical field, which may lead to the "vertical breakdown" of the epitaxial stack.

An example of lateral breakdown was reported in [161–163]. Here the authors demonstrated the existence of time-dependent dielectric breakdown in GaN-based high electron mobility transistors (HEMTs) submitted to stress in off-state bias. Specifically, they demonstrated that under off-state

stress at 600–700 V the devices can show a time-dependent failure, which was ascribed to the failure of the SiN dielectric at the edge of the gate overhang, on the drain side. A representative example of this failure process is shown in Fig. 15.60a: the variation of drain current during stress in off-state with $V_{DS} = 600$ V is reported on ten identical samples. All the analyzed devices reached a catastrophic failure, i.e., a sudden increase in drain current. Time-to-failure (TTF) was found to have an exponential dependence on stress bias. This was explained by considering the existence of a field-dependent degradation process. In addition, TTF was found to be Weibull-distributed (see, for instance, Fig. 15.60b), with a β around 0.5. Such a value is indicative of an extrinsic failure mechanism. Degradation was then ascribed to the time-dependent breakdown of the dielectric under the gate overhang. Numerical simulations were carried out to support this hypothesis. As shown in Fig. 15.61, the electric field in the nitride peaks at the edge of the gate overhang

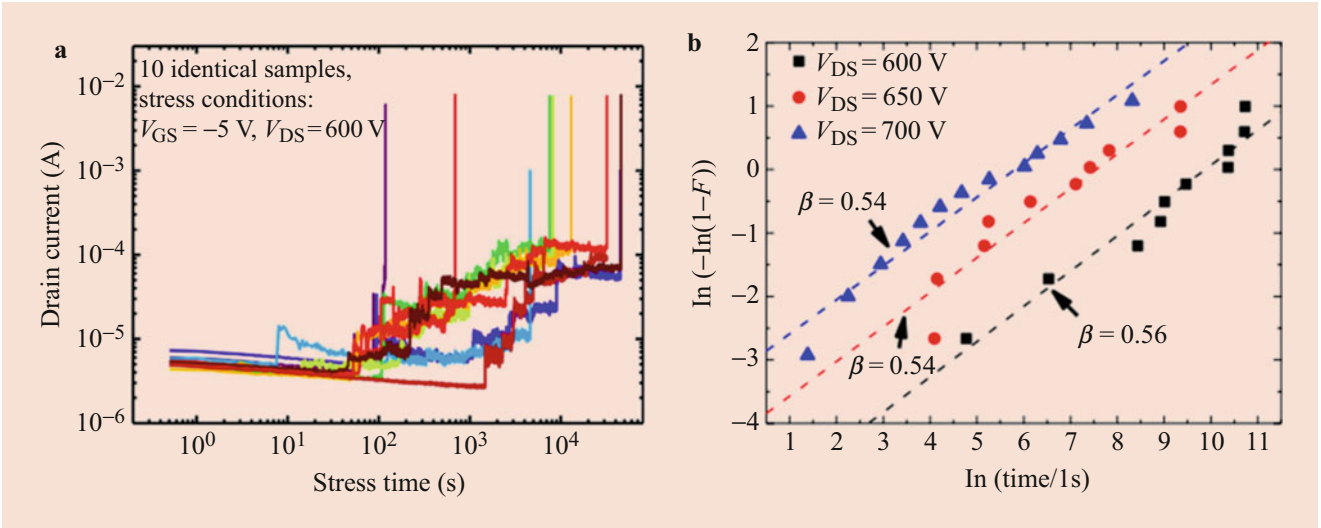

Fig. 15.60 (**a**) Results of constant voltage stress experiments carried out on a set of ten identical devices; the stress conditions are $V_{GS} = -5$ V, $V_{DS} = 600$ V. Only drain current is reported for clarity. (**b**) Weibull-distribution for three sets of devices stressed with VGS = −5 V, and increasing V_{DS} (600, 650, and 700 V). (© 2015 IEEE. Reprinted, with permission, from [163])

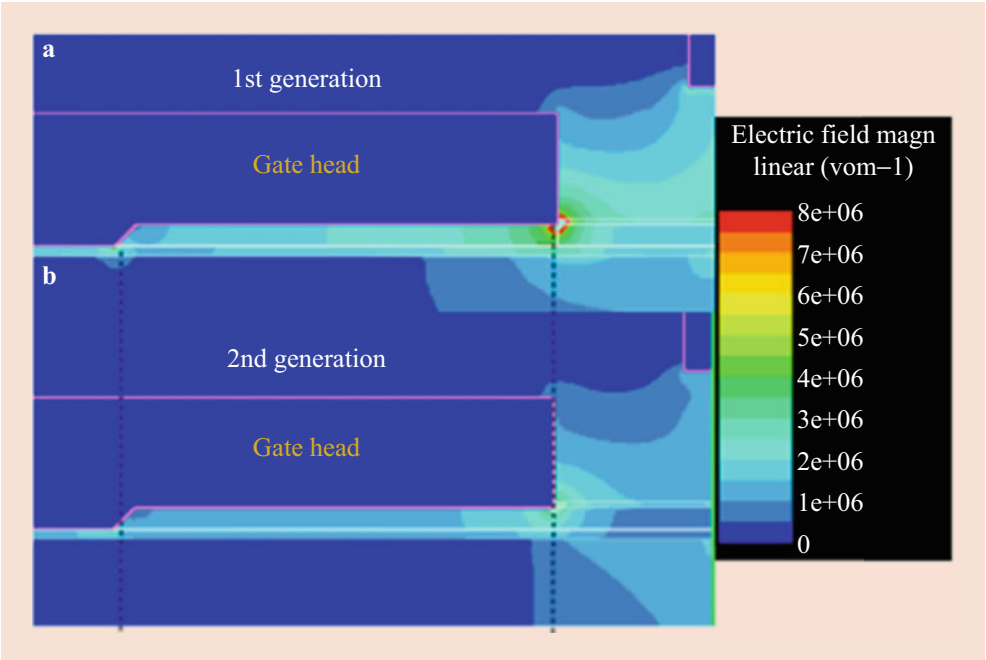

Fig. 15.61 (**a**) Simulated electric field distribution close to the gate edge for a device of Gen-1. (**b**) Simulated electric field distribution close to the gate edge for a device of Gen-2. (© 2015 IEEE. Reprinted, with permission, from [163])

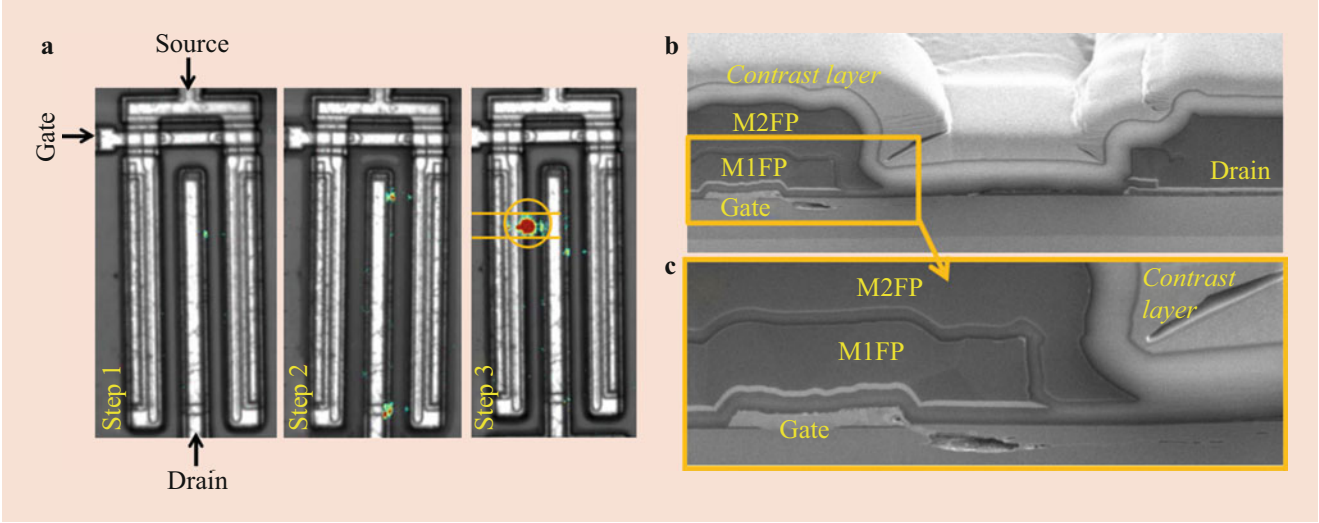

Fig. 15.62 (**a**) Emission microscopy evaluated during stress with $V_{GS} = -5$ V and $V_{DS} = 600$ V. The three frames are referred to increasing stress times. The portion cut for the TEM evaluation in is highlighted in yellow. (**b**) TEM performed on a cross section corresponding to the hot spot indicated in (a), after the constant voltage test, showing a severe degradation in the gate side/edge. (**c**) Enlargement of the damaged portion of the device. (© 2017 IEEE. Reprinted, with permission, from [161])

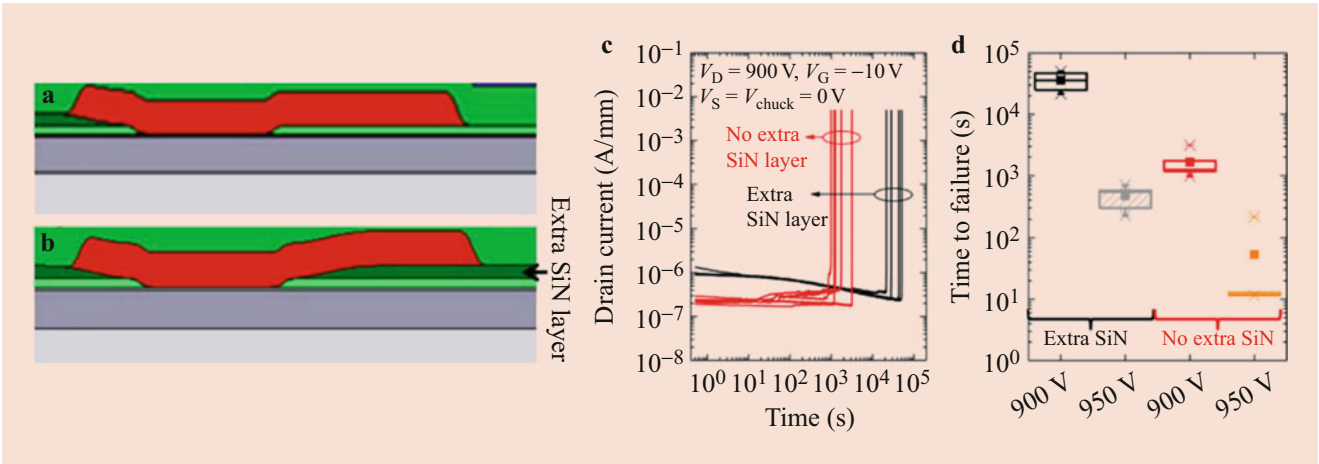

Fig. 15.63 Schematic of the variation in the device geometry, showing a structure (**a**) without and (**b**) with an extra SiN layer. An additional SiN layer is introduced in order to reduce the electric field at the edge of the gate. (**c**) Constant voltage test at $V_D = 900$ V, demonstrating that the extra nitride layer increases time to failure by one order of magnitude. (**d**) Box chart showing the measured time to failure in devices with and without extra SiN layer stressed at $V_D = 900$ V and $V_D = 950$ V. (© 2017 IEEE. Reprinted, with permission, from [161])

and can reach values around 6 MV/cm at $V_{DS} = 600$ V. A physical evidence of this hypothesis was obtained by TEM evaluation [161]. First, emission microscopy was performed in off-state conditions, to identify the presence of hot spots (Fig. 15.62). Then, cross sections were prepared by Focused Ion Beam (FIB) and then observed by Transmission Electron Microscopy (TEM, Fig. 15.62). The results demonstrated that degradation is effectively located at the drain-side gate edge. Stress induced the generation of a shunt-path between the gate head and the 2DEG, across the SiN/AlGaN stack. Such a degradation process is extrinsic (in the sense that it involves a material other than GaN, i.e., SiN). In [161], the authors proposed to add a graded layer of silicon nitride under the head of the gate to improve device reliability (Fig. 15.63). Figure 15.63 reports the results of a constant voltage stress experiment: the presence of the extra SiN layer can increase the TTF by one order of magnitude.

After discussing the extrinsic breakdown mechanisms induced by off-state stress (see above), we discuss here the intrinsic breakdown mechanisms related to the GaN material itself. Recent papers (see, for instance, [160, 165]) studied the robustness of the buffer stack submitted to high off-state conditions. To separately evaluate lateral and vertical breakdown, two-terminal stress experiments are typically carried out. The devices are stressed from drain to substrate, and this results in a significant vertical field. At industrial level,

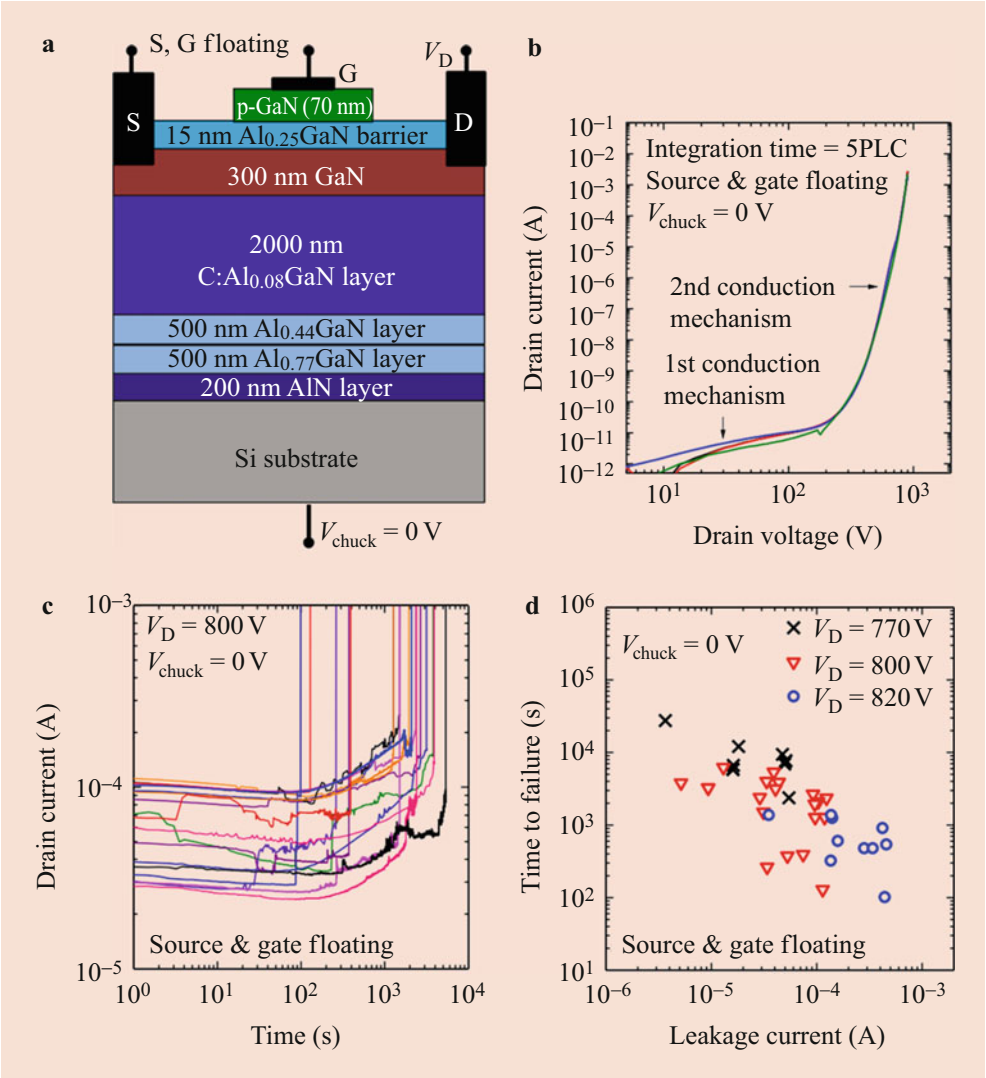

Fig. 15.64 (**a**) Schematic representation of the device under test. (**b**) Drain- controlled vertical leakage current measurement. The measurements were stopped at breakdown. (**c**) Drain current monitored during a constant voltage stress ($V_D = 800$ V). (**d**) TTF dependence on the initial leakage for three drain bias levels applied during the constant voltage stress. (© 2017 IEEE. Reprinted, with permission, from [160])

results on buffer reliability can be obtained also by means of high-oltage off-state stress (HVOS) [165], a condition where a high voltage is applied to the drain, with substrate and source grounded and gate in pinch-off.

Recently, Borga et al. demonstrated that GaN can show a time-dependent vertical breakdown that can result in a sudden increase in vertical leakage current [160]. The study was carried out on devices having the schematic structure reported in Fig. 15.64a, that are designed for 200 V operation. Before the execution of the stress tests experiments, the vertical (2-terminal) leakage current was characterized (see Fig. 15.64b): two conduction mechanisms were identified, with a change in slope around $V_D = 300$ V. Such behavior was explained by considering that for low vertical bias (<200 V) conduction is nearly ohmic and possibly assisted by dislocations. For higher voltages (>300 V) the depletion of the buffer results in the ionization of defects. Poole-Frenkel effects are favored, and an increase in vertical leakage is observed at high bias.

Figure 15.64c reports the results of a constant voltage stress test carried out on 18 identical devices with a vertical voltage of 800 V. After an initial stage where the leakage is stable, devices show first an increase in the noise superimposed to leakage current and then a sudden increase in vertical leakage. This is similar to the behavior of dielectrics under time-dependent breakdown testing, typically explained by the defect-percolation model. Figure 15.64d shows the time-to-failure (TTF) and leakage current measured on three

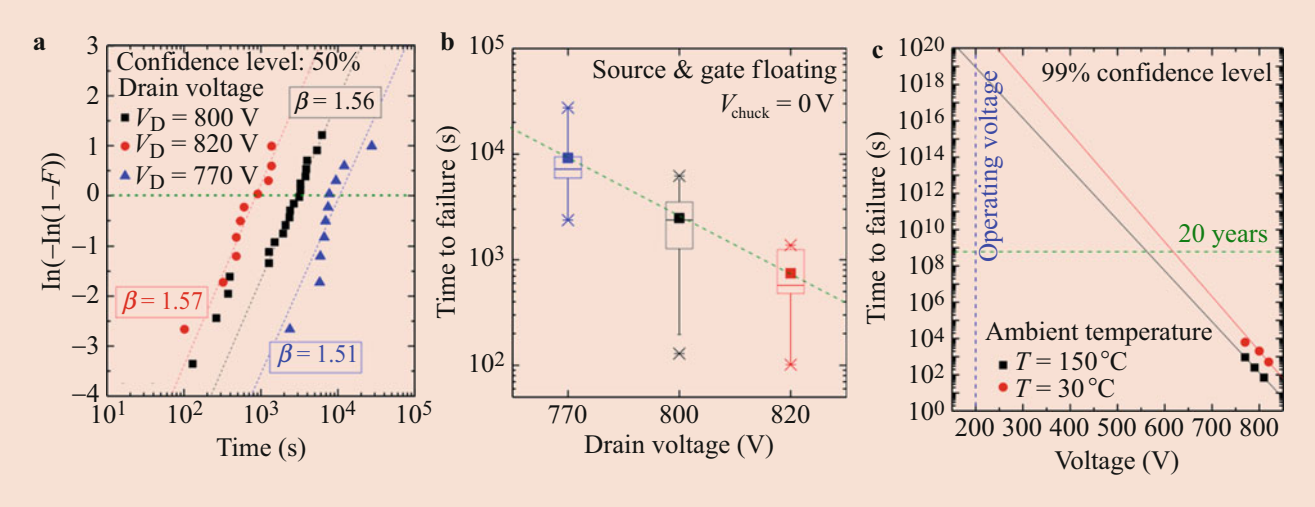

Fig. 15.65 (**a**) Weibull plot of the constant voltage stress. (**b**) TTF dependence on the applied drain voltage (box chart). (**c**) TTF dependence on the drain voltage applied at ambient temperature of 30 °C and 150 °C. Each point represents the Weibull scale factor with a confidence level of 99%. (© 2017 IEEE. Reprinted, with permission, from [160])

sets of samples stressed at different voltages. As expected, by increasing stress bias a decrease in TTF and an increase in leakage current are detected.

A further similarity with dielectric breakdown comes from the fact that TTF is Weibull-distributed. For reference, one can look at Fig. 15.65a, which reports the Weibull plots obtained by stress at three different voltage levels. Figure 15.65b indicates that TTF has an exponential dependence on stress voltage and supports the hypothesis that the degradation mechanism is field-dependent. In addition, a low thermal activation (0.25 eV) was measured.

The time-dependent breakdown of GaN does not represent a major limitation for this material. For the 200 V technology analyzed in [160], the maximum voltage for 20 years lifetime with 1% failure rate is around 560 V.

15.4.7 Stability in Semi-on Conditions

In several real-life application scenarios, GaN-based transistors can be operated under hard switching conditions. A basic example is the case of a boost power converter, where the simultaneous presence of high current and high voltage can take place during the turn-on phase of the devices. It is therefore important to evaluate the stability of the devices not only under soft switching, but also under the more dangerous hard switching regime.

Recently, the interest toward the hard switching behavior of GaN HEMTs has significantly increased. As an example, we mention here three recent papers on the topic, that significantly contributed to the understanding of the trapping/degradation processes under hard switching, i.e., [138, 166, 167].

In [167], Joh et al. investigated the current collapse in GaN-based HEMTs by a novel setup, capable of controlling independently the gate and drain pulses. They suggested that the current collapse can improve under hard switching, due to the generation of holes through impact ionization. The hypothesis in [167] is that in hard switching, if there is a substantial overlap between voltage and current waveforms, hot carriers are produced (in density proportional to $I_D \bullet \exp(-a/V_{DG})$) and can generate holes via impact ionization. Such holes can compensate the electrons trapped at the surface of the devices.

A similar setup was used by Rossetto et al. in [138], see a representative schematic in Fig. 15.66. Here the drain-gate-delay (the time interval between $V_D = V_{DSQ}/2$ and $V_G = V_{TH}$) is changed to generate hard switching events. In this paper, the authors showed that hard switching conditions may lead to an increase in dynamic-on resistance. They ascribed this effect to the fact that during the switching events, channel electrons are accelerated and consequently trapped within the devices.

A comprehensive description of the reliability of GaN-based transistors under hard switching tests was presented by Tanaka et al. in [166]. In this chapter, the authors presented the results of dynamic high-temperature operation life (D-HTOL) tests, carried out on transistors used in half-bridge configuration. They used a frequency of 6.6 kHz, an input voltage of 480 V and a switching current of 10 A. In addition, they compared two different kinds of transistors, the GITs and the HD-GITs, during the D-HTOL test. Here the HD-GIT is the hybrid-drain-embedded gate injection transistor, namely, a GIT where a pdrain is formed over a thick AlGaN barrier to suppress current collapse. The authors of this paper

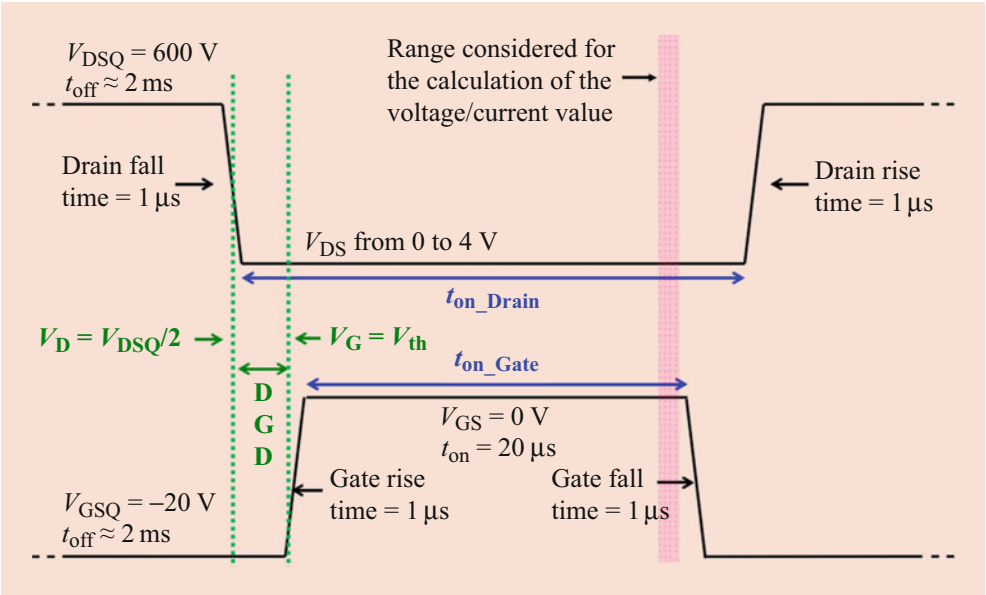

Fig. 15.66 Representative schematic of the drain and gate pulses applied during the analysis of the dynamic ON-resistance. The DGD is defined as the time range between $V_D = V_{DSQ}/2$ and $V_G = V_{TH}$. The range of the pulse considered for the calculation of the current–voltage curve is highlighted in shaded pink. (© 2017 IEEE. Reprinted, with permission, from [138])

demonstrated that in the GIT the maximum switching voltage decreases as the switching current increases; eventually, for high switching currents, the maximum switching voltage becomes lower than the rated voltage. On the other hand, HD-GITs do not fail even under the most severe hard switching conditions (V_{DS} = 640 V, I = 27 A). Thermal runaway is not the primary reason for GIT breakdown. On the contrary, the better reliability of HD-GITs is explained by the injection of holes from pdrain. Such holes can compensate the hole emission from the GaN epilayer under high off-state stress and the capture of hot electrons under semi-on state. Tanaka et al. [166] suggested that the hot electron trapping at the surface of the GIT can trigger the destructive breakdown; a positive-feedback loop is created, that may lead to the sudden shift of the EL position from the gate edge to the drain edge.

15.5 Conclusions

The continuous progress of GaN technology makes gallium nitride an ideal candidate for the development of advanced power semiconductor devices. Exciting challenges in growth and fabrication have already been faced, and GaN transistors are ready to start playing a major role in power conversion.

Within this chapter, we have discussed the main properties of GaN and of GaN-based devices, with focus on four aspects: epitaxial growth, lateral device technology, GaN vertical devices, charge trapping, and reliability issues.

This chapter is a useful reference for the readers willing to approach GaN technology and for experts in the field desiring an up-to-date discussion of the most relevant technological challenges and issues.

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Bipolar Transistors and Silicon Diodes

16

Jean-Michel Sallèse and Farzan Jazaeri

Contents

16.1 The PN Junction . . . 579
16.1.1 Introduction . . . 579
16.1.2 The PN Junction at Equilibrium and in Reverse Bias . . . 579
16.1.3 The pn Junction in Forward Bias . . . 583

16.2 Bipolar Transistors . . . 588
16.2.1 Introduction . . . 588
16.2.2 Structure . . . 589
16.2.3 Principle of Operation . . . 589
16.2.4 DC Operation of the n-p-n BJT Under Forward Active Mode . . . 590
16.2.5 Bipolar-Transistor Configurations . . . 590
16.2.6 Common-Emitter Configuration . . . 590
16.2.7 Common-Collector Configuration . . . 592
16.2.8 Common-Emitter Amplifier . . . 596

16.3 The Metal-Semiconductor Schottky Diode . . . 597
16.3.1 Introduction . . . 597
16.3.2 Additional Factors . . . 601

References . . . 601

Abstract

This chapter addresses the principle of operation of PN junction diodes, bipolar transistors and Schottky diodes. Basics characteristics of diodes are derived by merging electrostatics with semiconductor physics, leading to well know exponential relationships between the current and the applied voltage. Concerning bipolar transistors, they are discussed in a circuit application framework, leaving behind the details of the physics and putting more focus on biasing and the common modes of operation.

Keywords

PN junction · Diode-Bipolar transistor · Schottky diode · Work function · Metal-semiconductor · Amplifier

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16.1 The PN Junction

16.1.1 Introduction

Despite its quite simple architecture, the pn junction is one of the most fundamental semiconductor devices entering in micro- and nano-electronics technology. In addition to be used as a diode, the pn junction is at the root of the bipolar transistor and still plays an essential role in field effect transistors as it defines the source and drain contacts.

In this context, this section aims at recalling the basics in modeling the pn junction in forward and reverse bias under steady-state operation. Initially, the theory was developed by Shockley [3]. To get a simple while predictive analytical model, this section will consider a one-dimensional pn junction and will make use of simplifying assumptions that are common to many textbooks on the topic [1, 2].

In the following, we start analyzing the case of the pn junction in reverse bias. The situation where the pn junction is forward biased will be detailed later.

16.1.2 The PN Junction at Equilibrium and in Reverse Bias

We recall the basics of electrostatics of the pn junction in reverse bias adopting the full depletion approximation viewpoint. This kind of analysis ends with simple relationships that still accurately predict the charge distribution in pn junctions with uniform doping concentrations.

Potentials and Charges: Electrostatics Analysis at Equilibrium

Considering a one dimensional system, the analysis of the pn junction at equilibrium is based on the solution of the Poisson equation:

$$\frac{\mathrm{d}^2V(x)}{\mathrm{d}x^2} = \frac{-\rho(x)}{\varepsilon_{sc}} \tag{16.1}$$

where $V(x)$ and $\rho(x)$ are, respectively, the electrostatic potential and the charge density at abscissa x; see Fig. 16.1.

Assuming full ionization of donors and acceptors, which holds true at working temperatures and for the doping densities of interest, i.e., 10^{14} cm^{-3} – 10^{17} cm^{-3} (note that for higher densities, full ionization and action mass law assumptions may become invalid), the charge density in the semiconductor is

$$\rho(x) = q\left(N_D(x) + p(x)\right) - q\left(N_A(x) + n(x)\right) \tag{16.2}$$

and relation (16.1) becomes

$$\frac{\mathrm{d}^2V(x)}{\mathrm{d}x^2} = \frac{-q\left(N_D(x) + p(x)\right) - q\left(N_A(x) + n(x)\right)}{\varepsilon_{sc}} \tag{16.3}$$

Charge in Neutral Regions

In the neutral regions, i.e., for $x < x_p$ and $x > x_n$ (see Fig. 16.1), we assume that all the dopant atoms are fully ionized, i.e., each dopant releases an electron, meaning that the approximation $n = N_D$ holds true (again, this holds only partly for high doping densities, typically above 10^{18} cm^{-3}). Conversely, in the neutral p-doped region ($x < x_p$), every acceptor will release a hole and we can write $p = N_A$.

In addition, the action mass law $\left(np = n_i^2\right)$ implies that the minority-carrier concentrations in the neutral n-type and p-type doped semiconductors satisfy $p = n_i^2/N_D$ and $n = n_i^2/N_A$, respectively.

Creation of Space Charge Regions

In the vicinity of the interface between the n- and p-type doped layers, free electrons from the n-type semiconductor will diffuse into the opposite p-type region, whereas free holes in the p-type semiconductor will diffuse into the n-type one.

A common and quite justified assumption presumes that there is a deficiency of mobile carriers within some "depletion regions," whose extensions are $W_n = x_n$ and $W_p = -x_p$, while the semiconductor remains neutral otherwise; see Fig. 16.1.

Relation (16.3) must then be solved for these three distinct domains, which writes:

For $0 < x < x_n$, $\rho(x) = qN_D$
For $x_p < x < 0$, $\rho(x) = -qN_A$
Otherwise $\rho(x) = 0$

Note that the continuity of the potential and electric field at $=x_n$, $x = x_p$, and $x = 0$ is also required. Solving relation (16.3) between $x = x_p$ and $x = 0$ and imposing the electric field null at x_p (neutral semiconductor) gives

$$\frac{\mathrm{d}V(x)}{\mathrm{d}x} = -E(x) = \frac{qN_A}{\varepsilon_{sc}}(x - x_P) \tag{16.4}$$

which after integration leads to

$$V(x) = \frac{qN_A}{2\varepsilon_{sc}}(x - x_P)^2 + V_p \tag{16.5}$$

Similarly, imposing the electric field null at x_n, the electrostatic potential in the depleted region between $x = x_n$ and $x = 0$ satisfies

$$\frac{\mathrm{d}V(x)}{\mathrm{d}x} = -E(x) = \frac{-qN_D}{\varepsilon_{sc}}(x - x_n) \tag{16.6}$$

and after integration

$$V(x) = \frac{-qN_D}{2\varepsilon_{sc}}(x - x_N)^2 + V_n \tag{16.7}$$

According to relations (16.5) and (16.7), it comes out that the general solution for the potential distribution in the non-neutral regions follows a quadratic law.

In addition, relations (16.5) and (16.7) still involve unknowns such as the potential in the neutral regions, i.e., V_n and V_p, as well as the extension of the depletion regions, x_n and x_p. Lastly, what is needed is to impose the charge neutrality for the structure as a whole, as well as the limit conditions in terms of potential drop across the pn junction

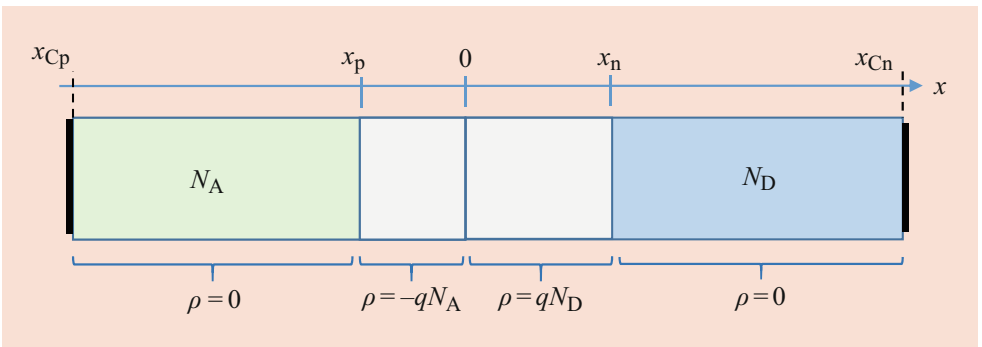

Fig. 16.1 Doping profile and depletion regions in a pn junction at equilibrium

(note that the device is expected to be in reverse bias, a condition that will be made clear later).

The charge neutrality of the diode imposes that the depletion regions are linked to each other:

$$qN_A x_P + qN_D x_N = 0 \tag{16.8}$$

Note that this condition also means that the electric fields at $x = 0$ given by relations (16.4) and (16.6) are equal (in fact, we should say that the displacement vectors $D = \varepsilon_{sc} E$ are equal at the junction interface, i.e., $x = 0$). This condition links the depletion regions (whose extension will then vary inversely with the doping concentration).

Finally, the potential must be continuous at $x = 0$. This last condition links the depletion width to the potential drop $V_n - V_p$:

$$\frac{qN_A}{2\varepsilon_{sc}} {x_P}^2 + V_p = \frac{-qN_D}{2\varepsilon_{sc}} {x_N}^2 + V_n \tag{16.9}$$

$$\begin{aligned} V_n n - V_p &= \frac{qN_A}{2\varepsilon_{sc}} {x_P}^2 + \frac{qN_D}{2\varepsilon_{sc}} {x_N}^2 \\ &= \frac{qN_A\,(-x_P)}{2\varepsilon_{sc}}\,(-x_P) + \frac{qN_D x_N}{2\varepsilon_{sc}} x_N \end{aligned} \tag{16.10}$$

Defining the width of the depleted regions as $W_p = -x_P$ and $W_n = x_n$, and making use of the neutrality condition (relation 16.8), we obtain

$$V_n - V_p = \frac{qN_D W_n}{2\varepsilon_{sc}} \left(W_p + W_n\right) = \frac{qN_D {W_n}^2}{2\varepsilon_{sc}} \left(\frac{W_p}{W_n} + 1\right) \tag{16.11}$$

Or, equivalently,

$$V_n - V_p = \frac{qN_D {W_n}^2}{2\varepsilon_{sc}} \left(\frac{N_D}{N_A} + 1\right) = \frac{qN_D {W_p}^2}{2\varepsilon_{sc}} \left(\frac{N_A}{N_D} + 1\right) \tag{16.12}$$

At this point of the derivation, note that even though the depletion regions are linked to one another, their extension is still not known. Depending on the depletion widths, the electric field will build up a potential that varies quadratically with x according to relations (16.5) and (16.7). However, the potential difference between the p-type neutral and n-type neutral regions *cannot be arbitrary*. This potential should also be consistent with the band bending experienced across the device. Here is the second condition that will fix the depletion width.

The Built-In Potential

The profiles of the charge, electric field and potential satisfying the full depletion approximation are summarized in Fig. 16.2a–d.

Semiconductor statistics link the free-carrier densities to the difference between the Fermi energy and the conduction/-valence bands as follows:

$$n = N_C\, e^{\frac{-(E_C - E_F)}{kT}} \tag{16.13}$$

$$p = N_V\, e^{\frac{(E_V - E_F)}{kT}} \tag{16.14}$$

where N_C and N_V are the effective density of states for the conduction and valence bands

$$N_{C,V} = 2\left(\frac{2\,\pi\, m_{e,h}\, k\, T}{h^2}\right) \tag{16.15}$$

Symbols have their usual meaning (note that $m_{e,h}$ is the *density-of-states effective mass*). Relations (16.13) and (16.14) are valid as far as $n < N_C$ and $p < N_V$ for n- and p-type doped semiconductors, respectively, i.e., they are valid for non-degenerate semiconductors. For instance, in silicon at room temperature, these effective density of states represent quite high concentrations of free carriers, i.e., around 2.8 10^{19} cm^{-3} for electrons and 1.8 10^{19} cm^{-3} for holes. For silicon, when considering regular doping densities used to create p- and n-doped regions, these levels are usually not met, and doping densities are lower than $N_{C,V}$. Only for very high doping levels, like those required for source and drain implants in MOSFETs, relations (16.13) and (16.14) should be revised. Another exception would be small band gap semiconductors, where the density of states is quite low, for instance InAs where $N_C \cong 9\ 10^{16}$ at 300 K.

To calculate the potential difference between the n- and p-type neutral regions, relation (16.13) must be satisfied in each domain.

$$n_n = N_C\, e^{\frac{-\left(E_C^n - E_F\right)}{kT}} \tag{16.16}$$

$$n_p = N_C\, e^{\frac{-\left(E_C^p - E_F\right)}{kT}} \tag{16.17}$$

In addition, we still consider that the free carrier and doping densities are equal (here we use electrons, but the same results would be obtained when considering holes):

$$n_n = N_D \tag{16.18}$$

which implies that minority carriers are known as well:

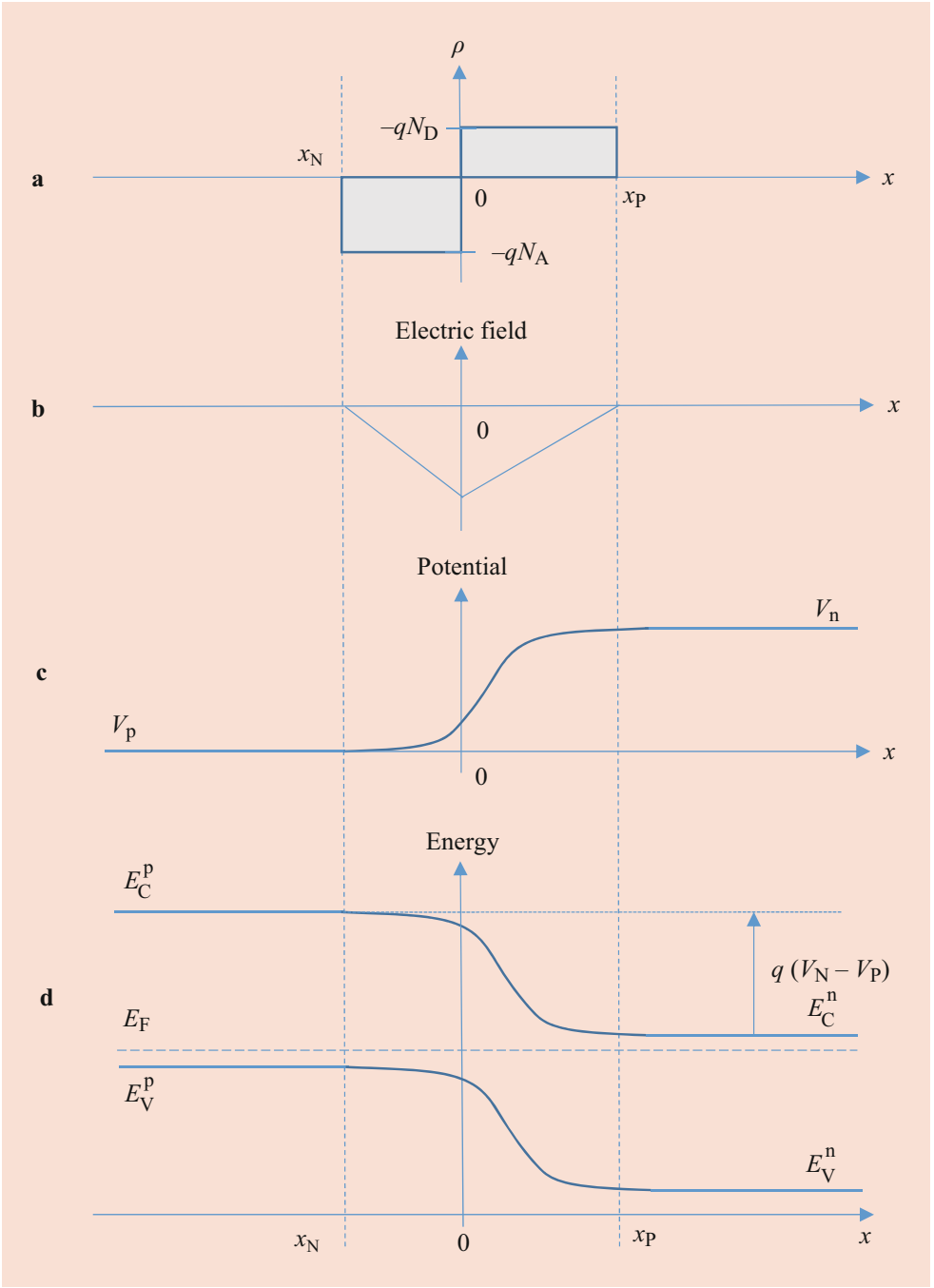

Fig. 16.2 Representation of the charge density (**a**), electric field (**b**), electrostatic potential (**c**) and energy bands bending (**d**) in a pn junction at zero bias

$$n_{\mathrm{p}} = \frac{n_i^2}{N_{\mathrm{A}}} \tag{16.19}$$

Dividing relations (16.16) by (16.17) gives the difference in the conduction (or valence) band energy between the neutral regions of the pn junction:

$$E_{\mathrm{C}}^{\mathrm{p}} - E_{\mathrm{C}}^{\mathrm{n}} = kT\,\mathrm{Ln}\left(\frac{N_{\mathrm{D}}N_{\mathrm{A}}}{n_i^2}\right) \tag{16.20}$$

which in terms of potentials reads

$$V_{\mathrm{n}} - V_{\mathrm{p}} = \frac{kT}{q}\mathrm{Ln}\left(\frac{N_{\mathrm{D}}N_{\mathrm{A}}}{n_i^2}\right) \tag{16.21}$$

This quantity is known as the *built-in potential* of the pn junction, namely, $V_{\mathrm{bi.}}$.

Its value is about 0.7 volt in silicon for doping densities of 10^{16} cm^{-3} (for N_{A} and N_{D}) at 25 °C.

The Depletion Width

So far, we obtained the potential drop in each region depleted from mobile carriers under the full-depletion approxima-

tion; see relation (16.12). Imposing now the condition given by relation (16.21), which is specific to the semiconductor (whereas so far we considered electrostatics only), gives

$$\begin{aligned}\frac{kT}{q}\mathrm{Ln}\left(\frac{N_\mathrm{D}N_\mathrm{A}}{n_i^2}\right) &= \frac{qN_\mathrm{D}{W_n}^2}{2\varepsilon_\mathrm{sc}}\left(\frac{N_\mathrm{D}}{N_\mathrm{A}}+1\right)\\ &= \frac{qN_\mathrm{D}{W_\mathrm{p}}^2}{2\varepsilon_\mathrm{sc}}\left(\frac{N_\mathrm{A}}{N_\mathrm{D}}+1\right)\end{aligned} \tag{16.22}$$

The depletion regions for each doped semiconductor layer are then readily obtained:

$$\begin{aligned}\mathrm{W_n} &= \sqrt{\frac{2\varepsilon_\mathrm{sc}kT}{q^2N_\mathrm{D}}}\sqrt{\frac{N_\mathrm{A}}{N_\mathrm{A}+N_\mathrm{D}}\mathrm{Ln}\left(\frac{N_\mathrm{D}N_\mathrm{A}}{n_i^2}\right)}\\ &= L_{\mathrm{D-n}}\sqrt{\frac{N_\mathrm{A}}{N_\mathrm{A}+N_\mathrm{D}}\mathrm{Ln}\left(\frac{N_\mathrm{D}N_\mathrm{A}}{n_i^2}\right)}\end{aligned} \tag{16.23}$$

Similarly,

$$W_\mathrm{p} = L_{\mathrm{D-p}}\sqrt{\frac{N_\mathrm{D}}{N_\mathrm{A}+N_\mathrm{D}}\mathrm{Ln}\left(\frac{N_\mathrm{D}N_\mathrm{A}}{n_i^2}\right)} \tag{16.24}$$

where $L_{\mathrm{D-n}}$ and $L_{\mathrm{D-p}}$ are the Debye lengths defined as $L_{\mathrm{D-n}} = \sqrt{\frac{2\varepsilon_\mathrm{sc}kT}{q^2N_\mathrm{D}}}$ and $L_{\mathrm{D-p}} = \sqrt{\frac{2\varepsilon_\mathrm{sc}kT}{q^2N_\mathrm{A}}}$.

Finally, the total depletion with W of the pn junction is $W = W_\mathrm{n} + W_\mathrm{p}$.

Note that relation (16.8) indicates that the ratio between the depletion widths scales with the counter ratio of the doping concentrations. Therefore, when a concentration dominates (a quite common situation in real devices), the depletion width of the pn junction can fairly be approximated by the depletion width of the lesser-doped domain:

$$W \cong W_\mathrm{p} = L_{\mathrm{D-p}}\sqrt{\mathrm{Ln}\left(\frac{N_\mathrm{D}N_\mathrm{A}}{n_i^2}\right)} \text{ when } N_\mathrm{D} \gg N_\mathrm{A} \tag{16.25}$$

Analysis of the pn Junction in Reverse Bias

The depletion region can be modulated by applying an external potential V between the n- and p-type doped regions. Here, we consider that we apply a negative voltage to the n side with respect to the p side and define $V = V_\mathrm{N} - V_\mathrm{P}$. This voltage V splits the energy between the Fermi levels on each side of the junction by qV, and therefore it will shift the bands in the neutral regions by the same amount (since the free carrier density is not changed in the neutral regions).

Again, supposing $N_\mathrm{D} \gg N_\mathrm{A}$, relation (16.22) writes

$$V + \frac{kT}{q}\mathrm{Ln}\left(\frac{N_\mathrm{D}N_\mathrm{A}}{n_i^2}\right) \cong \frac{qN_\mathrm{A}{W_\mathrm{p}}^2}{2\varepsilon_\mathrm{sc}} \tag{16.26}$$

and the depletion in the p-type semiconductor is now voltage-dependent

$$W_\mathrm{p}(V) \cong \sqrt{\frac{2\varepsilon_\mathrm{sc}}{qN_\mathrm{A}}}\sqrt{V+V_\mathrm{bi}} \tag{16.27}$$

(the p side is taken as the reference for the potentials).

Depending on the sign of V, the depletion region will either increase ($V > 0$) or decrease ($V < 0$).

Since the charge density can be modulated, the depletion capacitance follows. The charge stored per unit surface in each depletion region (in absolute value) is given by

$$Q_\mathrm{Dep}(V) = q\,N_\mathrm{A}\,W_\mathrm{p}(V) = \sqrt{2\varepsilon_\mathrm{sc}q\,N_\mathrm{A}}\sqrt{V+V_\mathrm{bi}} \tag{16.28}$$

Therefore, the depletion capacitance per unit surface $C_\mathrm{Dep}(V)$ is given by ($N_\mathrm{D} \gg N_\mathrm{A}$):

$$C_\mathrm{Dep}(V) = \frac{\mathrm{d}Q_\mathrm{Dep}(V)}{\mathrm{d}V} = \sqrt{\frac{\varepsilon_\mathrm{sc}q\,N_\mathrm{A}}{2}}\frac{1}{\sqrt{V+V_\mathrm{bi}}} \tag{16.29}$$

This depletion capacitance varies with the applied potential. This characteristic is commonly used to modulate a resonance frequency of a resonant circuit with a DC bias and is known as the junction varactor device [7].

16.1.3 The pn Junction in Forward Bias

When the potential barrier across the pn junction is lowered, the balance between diffusion and drift currents is no longer satisfied and generates a net current flowing across the junction. The common way to model a pn junction in forward bias is to evaluate the excess in minority-carrier concentrations at the limit of each space-charge region. These excess carriers will tend to diffuse inside the neutral region, where a fraction will recombine with the majority carriers introduced by the doping. *Note that this process takes place outside of the depletion region.*

This kind of analysis is formulated with the basics of semiconductor physics (in non-degenerate conditions), ensuring the current continuity condition. Here, we adopt the convention $V = V_\mathrm{P} - V_\mathrm{N}$, where V_P and V_N are the potentials applied to the p- and n-type doped semiconductors, respectively (note that the convention adopted here is different from the reverse bias case in order to consider positive voltages).

Estimation of the Minority Carrier Concentrations

The minority carrier concentration in the neutral regions is known from the intrinsic carrier concentration and the doping densities; see Fig. 16.3.

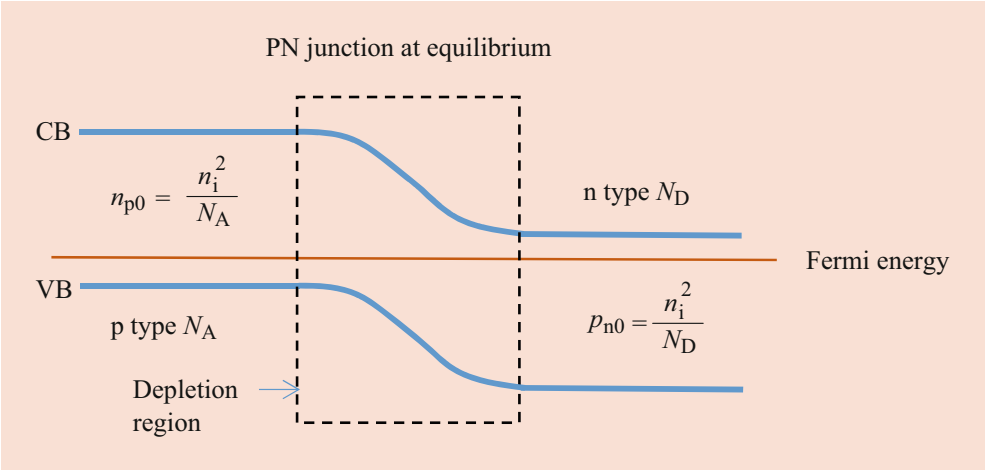

Fig. 16.3 Conduction and valence extrema energies across the pn junction at equilibrium. Minority carrier concentrations are indicated, as well as the limit of the depletion regions

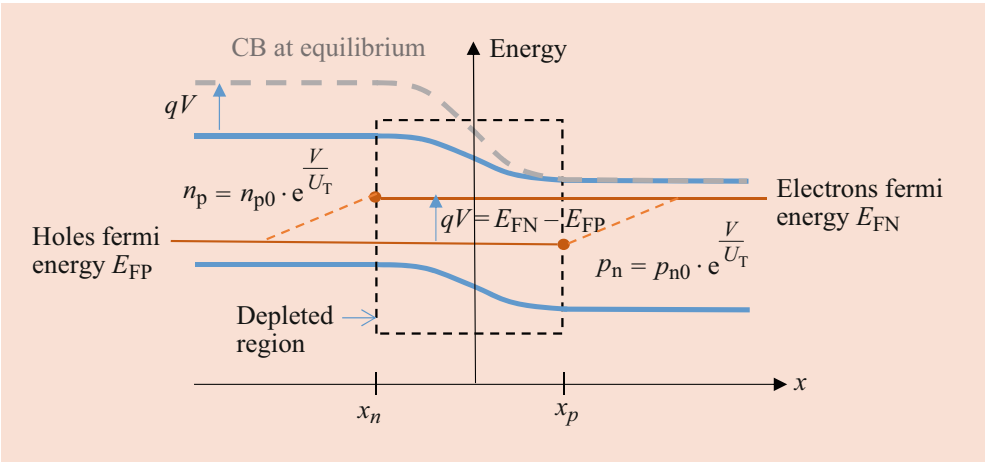

Fig. 16.4 Conduction and valence bands extrema energies across the pn junction under forward bias. Minority-carrier concentrations at the limit of the depletion regions are enhanced with respect to the concentration they have at equilibrium

$$n_{p0} = \frac{n_i^2}{N_A} \tag{16.30}$$

$$p_{n0} = \frac{n_i^2}{N_D} \tag{16.31}$$

As already mentioned, applying a potential V across the pn junction splits the electron and hole Fermi energies by qV and shifts the conduction and valence bands as sketched in Fig. 16.4.

Provided the quasi-Fermi levels for electrons and holes do not vary across the depletion region (but merge in a common Fermi level in the neutral regions at equilibrium, see dotted lines in Fig. 16.4), we obtain the concentrations of minority carriers at the limit of the depletion regions:

$$n_p\left(x_p\right) = n_{p0}\, e^{\frac{qV}{kT}} = \frac{n_i^2}{N_A}\, e^{\frac{V}{U_T}} \tag{16.32}$$

$$p_n\left(x_n\right) = p_{n0}\, e^{\frac{qV}{kT}} = p_{n0}\, e^{\frac{V}{U_T}} = \frac{n_i^2}{N_D}\, e^{\frac{V}{U_T}} \tag{16.33}$$

where $U_T = \frac{kT}{q}$ is the thermal voltage.

When V is positive, the minority carrier concentrations are enhanced at the limit of the depletion regions. The next step is to calculate how these carriers will generate a current.

The Current-Continuity Equation

Assuming that there is no electric field in the neutral regions, under steady state, the continuity equation reverts to a simple second order differential equation:

$$D_p \frac{d^2 p_n}{dx^2} - \frac{p_n - p_{n0}}{\tau_p} = 0 \tag{16.34}$$

where D_p is the diffusion coefficient of holes in the n-type doped semiconductor and τ_p their lifetime.

The same relation can be derived for electrons in the p-type doped layer

$$D_{\mathrm{n}}\frac{\mathrm{d}^2 n_{\mathrm{p}}}{\mathrm{d}x^2}-\frac{n_{\mathrm{p}}-n_{\mathrm{p0}}}{\tau_{\mathrm{n}}}=0 \tag{16.35}$$

Introducing the diffusion length of electrons in the p-type semiconductor, $L_{\mathrm{n}}=\sqrt{D_{\mathrm{n}}\tau_{\mathrm{n}}}$, and for holes in the n-type semiconductor, $L_{\mathrm{p}}=\sqrt{D_{\mathrm{p}}\tau_{\mathrm{p}}}$, we obtain

$$\frac{\mathrm{d}^2 n_{\mathrm{p}}}{\mathrm{d}x^2}-\frac{n_{\mathrm{p}}-n_{\mathrm{p0}}}{{L_{\mathrm{n}}}^2}=0 \tag{16.36}$$

$$\frac{\mathrm{d}^2 p_{\mathrm{n}}}{\mathrm{d}x^2}-\frac{p_{\mathrm{n}}-p_{\mathrm{n0}}}{{L_{\mathrm{p}}}^2}=0 \tag{16.37}$$

Solving these differential equations gives the profile of the minority carrier concentrations in both neutral regions. The last step is to set the limit conditions.

One condition happens at the limit of the space charge region and is rebuilt from relations (16.32) and (16.33). The other one is at the contact itself, i.e., $x=x_{\mathrm{Cn}}$ and $x=x_{\mathrm{Cp}}$, where full recombination in excess minority carriers is imposed:

$$p_{\mathrm{n}}\left(x_{\mathrm{Cn}}\right)=p_{\mathrm{n0}}=\frac{{n_i}^2}{N_{\mathrm{D}}} \tag{16.38}$$

$$n_{\mathrm{p}}\left(x_{\mathrm{Cp}}\right)=n_{\mathrm{p0}}=\frac{n_i^2}{N_{\mathrm{A}}} \tag{16.39}$$

Then, the general solution is

$$p_{\mathrm{n}}(x)-p_{\mathrm{n0}}=p_{\mathrm{n0}}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}}-1\right)\frac{\sinh\left(\left(x_{\mathrm{Cn}}-x\right)/L_{\mathrm{p}}\right)}{\sinh\left(T_{\mathrm{n}}/L_{\mathrm{p}}\right)} \tag{16.40}$$

$$n_{\mathrm{p}}(x)-n_{\mathrm{p0}}=n_{\mathrm{p0}}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}}-1\right)\frac{\sinh\left(\left(x-x_{\mathrm{Cp}}\right)/L_{\mathrm{n}}\right)}{\sinh\left(T_{\mathrm{p}}/L_{\mathrm{n}}\right)} \tag{16.41}$$

where $T_{\mathrm{p}}=W_{\mathrm{p}}-x_{\mathrm{Cp}}$ and $T_{\mathrm{n}}=x_{\mathrm{Cn}}-W_{\mathrm{n}}$ are the extensions of the p- and n-doped neutral regions.

Minority-Carrier Current

The excess of minority carriers in the neutral regions is responsible for diffusion currents:

$$J_{\mathrm{p}}(x)=-qD_{\mathrm{p}}\frac{\mathrm{d}p_{\mathrm{n}}(x)}{\mathrm{d}x} \tag{16.42}$$

$$J_{\mathrm{n}}(x)=qD_{\mathrm{n}}\frac{\mathrm{d}n_{\mathrm{p}}(x)}{\mathrm{d}x} \tag{16.43}$$

Making use of relations (16.40) and (16.41), these currents become explicit functions of the potential and coordinate.

$$\begin{aligned}J_{\mathrm{p}}(x)&=-qD_{\mathrm{p}}\frac{\mathrm{d}p_{\mathrm{n}}(x)}{\mathrm{d}x}\\&=\frac{qD_{\mathrm{p}}n_i^2}{L_{\mathrm{p}}N_{\mathrm{D}}\sinh\left(T_{\mathrm{n}}/L_{\mathrm{p}}\right)}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}}-1\right)\operatorname{csh}\left(\left(x_{\mathrm{Cn}}-x\right)/L_{\mathrm{p}}\right)\end{aligned} \tag{16.44}$$

$$\begin{aligned}J_{\mathrm{n}}(x)&=qD_{\mathrm{n}}\frac{\mathrm{d}n_{\mathrm{p}}(x)}{\mathrm{d}x}\\&=\frac{qD_{\mathrm{n}}n_i^2}{L_{\mathrm{n}}N_{\mathrm{A}}\sinh\left(T_{\mathrm{p}}/L_{\mathrm{n}}\right)}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}}-1\right)\operatorname{csh}\left(\left(x-x_{\mathrm{Cp}}\right)/L_{\mathrm{n}}\right)\end{aligned} \tag{16.45}$$

From relations (16.44) and (16.45), the minority carrier diffusion currents are not constant as they vary with x. However, this does not mean that the *total current* is not constant. Indeed, this condition was already enforced by introducing the current-continuity equation in the steady-state analysis (note that very high-frequency operation requires another approach). In fact, at any coordinate, there is a recombination current that is compensated by a current of majority carriers. This majority carrier current "brings" the majority carriers that will be "used" to enable recombination.

Simplifying Assumptions

Two situations are of practical interest.

The first case is when the neutral regions are wider than the diffusion lengths, i.e., $T_{\mathrm{p}}\gg L_{\mathrm{n}}$ and $T_{\mathrm{n}}\gg L_{\mathrm{p}}$. This case corresponds to "long diodes."

The second case refers to short diodes, i.e., when $T_{\mathrm{p}}\ll L_{\mathrm{n}}$ and $T_{\mathrm{n}}\ll L_{\mathrm{p}}$.

Long Diodes

In a long diode, relations (16.40) and (16.41) can be simplified and excess in minority carrier concentrations are given by

$$\begin{aligned}p_{\mathrm{n}}(x)-p_{\mathrm{n0}}&=p_{\mathrm{n0}}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}}-1\right)\frac{\mathrm{e}^{\left(x_{\mathrm{Cn}}-x\right)/L_{\mathrm{P}}}}{\mathrm{e}^{T_{\mathrm{n}}/L_{\mathrm{p}}}}\\&=p_{\mathrm{n0}}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}}-1\right)\mathrm{e}^{\left(x_{\mathrm{n}}-x\right)/L_{\mathrm{p}}}\end{aligned} \tag{16.46}$$

$$\begin{aligned}n_{\mathrm{p}}(x)-n_{\mathrm{p0}}&=n_{\mathrm{p0}}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}}-1\right)\frac{\mathrm{e}^{\left(x-x_{\mathrm{Cp}}\right)/L_{\mathrm{n}}}}{\mathrm{e}^{T_{\mathrm{p}}/L_{\mathrm{n}}}}\\&=n_{\mathrm{p0}}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}}-1\right)\mathrm{e}^{\left(x-x_{\mathrm{p}}\right)/L_{\mathrm{n}}}\end{aligned} \tag{16.47}$$

Applying relations (16.42) and (16.43), the current density for each type of carrier is (the long diode approximation can also be directly obtained from relations (16.44) and (16.45)):

$$J_{\mathrm{p}}(x) = \frac{qD_{\mathrm{p}}n_i^2}{L_{\mathrm{p}}N_{\mathrm{D}}}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}} - 1\right)\mathrm{e}^{(x_{\mathrm{Cn}}-x)/L_{\mathrm{p}}} \tag{16.48}$$

$$J_{\mathrm{n}}(x) = \frac{qD_{\mathrm{n}}n_i^2}{L_{\mathrm{n}}N_{\mathrm{A}}}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}} - 1\right)\mathrm{e}^{(x-x_{\mathrm{Cp}})/L_{\mathrm{n}}} \tag{16.49}$$

In long diodes, minority carrier currents are not constant along the neutral regions (see comment above).

Short Diodes

In short diodes the hyperbolic sine and cosine function can be replaced by the first order term of a Taylor series, $\sinh(T_{\mathrm{n}}/L_{\mathrm{p}}) \cong T_{\mathrm{n}}/L_{\mathrm{p}}$ ($\sinh(T_{\mathrm{p}}/L_{\mathrm{n}}) \cong T_{\mathrm{p}}/L_{\mathrm{n}}$) and $\mathrm{csh}((x_{\mathrm{Cn}} - x)/L_{\mathrm{p}}) \cong 1$, ($\mathrm{csh}((x - x_{\mathrm{Cp}})/L_{\mathrm{n}}) \cong 1$) leading to

$$p_{\mathrm{n}}(x) - p_{\mathrm{n0}} = p_{\mathrm{n0}}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}} - 1\right)\frac{(x_{\mathrm{Cn}} - x)}{T_{\mathrm{n}}} \tag{16.50}$$

$$n_{\mathrm{p}}(x) - n_{\mathrm{p0}} = n_{\mathrm{p0}}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}} - 1\right)\frac{(x - x_{\mathrm{Cp}})}{T_p} \tag{16.51}$$

These expressions lead to current densities that are now independent of the coordinate:

$$J_{\mathrm{p}} = \frac{qD_{\mathrm{p}}n_i^2}{T_{\mathrm{n}}N_{\mathrm{D}}}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}} - 1\right) \tag{16.52}$$

$$J_{\mathrm{n}} = \frac{qD_{\mathrm{n}}n_i^2}{T_{\mathrm{p}}N_{\mathrm{A}}}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}} - 1\right) \tag{16.53}$$

Where we assumed for simplicity $p_{\mathrm{n0}}N_{\mathrm{D}} = n_i^2$ and $n_{\mathrm{p0}}N_{\mathrm{A}} = n_i^2$.

The limit conditions are represented in Figs. 16.5 and 16.6 for the minority carrier concentrations and minority-carrier currents, respectively.

In short diodes, the diffusion current is constant in the neutral regions.

Total Current Densities

In each domain, the sum of the currents generated by the diffusion of minority carriers and the current originating by majority carriers enabling recombination is constant. This condition holds in particular at the edge of the depletion regions, i.e., at x_{p} and x_{n}. At these coordinates, the recombination current is null since recombination did not operate yet (this is where minority carriers are 'freshly' injected). Therefore, only the diffusion current exists, meaning that the current density arising from the transfer of electrons from the n-type into the p-type doped semiconductor layers is given by

$$J_{\mathrm{n}} = J_{\mathrm{n}}\left(x_{\mathrm{Cp}}\right) = qD_{\mathrm{n}}\frac{\mathrm{d}n_{\mathrm{p}}(x)}{\mathrm{d}x} = \frac{qD_{\mathrm{n}}n_i^2}{L_{\mathrm{n}}N_{\mathrm{A}}\tanh\left(T_{\mathrm{p}}/L_{\mathrm{n}}\right)}\left(\mathrm{e}^{\frac{V}{U_{\mathrm{T}}}} - 1\right) \tag{16.54}$$

The same reasoning applies for the current generated by injection of holes in the n-type region:

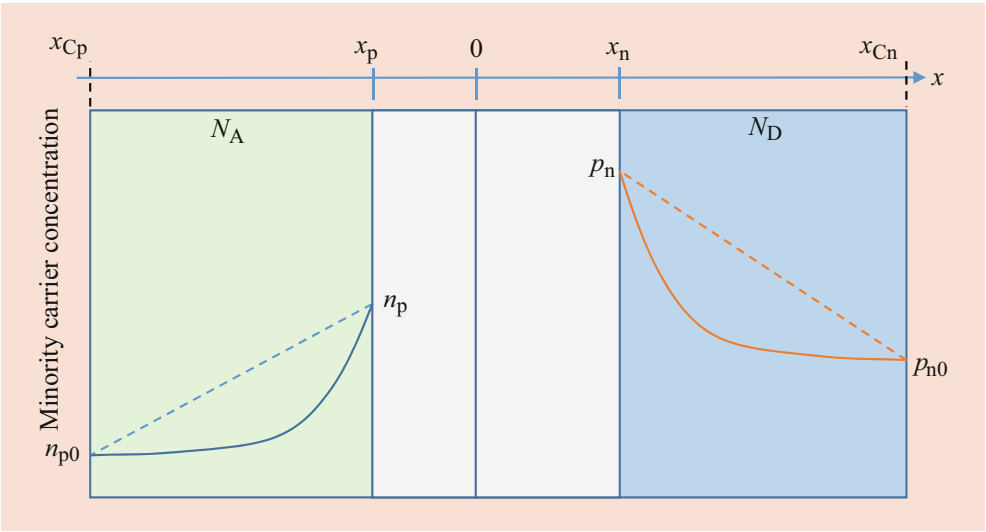

Fig. 16.5 Sketch of the minority-carrier concentration profiles in the neutral regions. Dotted lines are for short diodes. Continuous lines for long diodes. Note that the limit conditions are identical in both cases

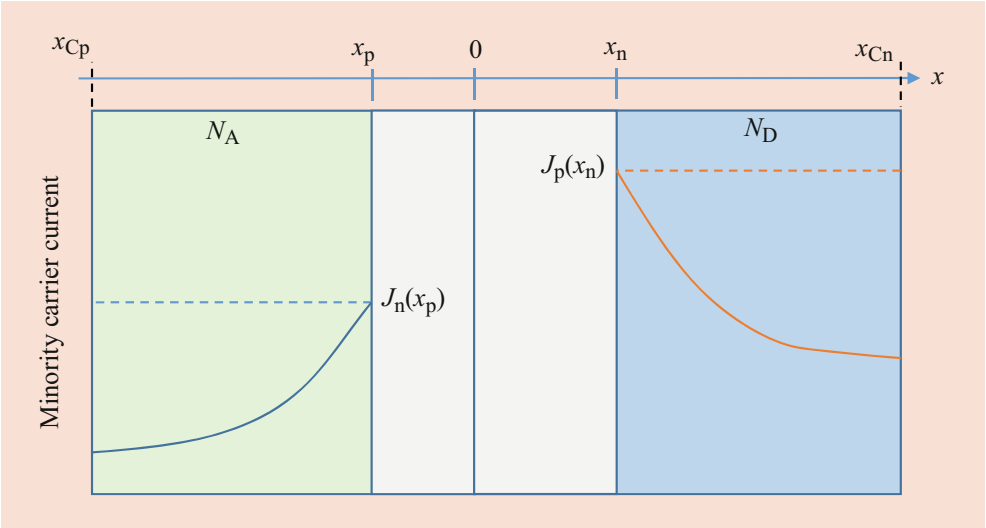

Fig. 16.6 Sketch of the minority-carrier current (diffusion current) profiles in the neutral regions. Dotted lines are for short diodes. Continuous lines for long diodes. Note that only for short diodes the diffusion current is constant in the neutral regions

$$J_p = J_p\,(x_{Cn}) = -qD_p \frac{dp_n(x)}{dx} = \frac{qD_p n_i^2}{L_p N_D \tanh\left(T_n/L_p\right)} \left(e^{\frac{V}{U_T}} - 1\right) \tag{16.55}$$

Finally, the total current flowing in the diode is the sum of electron and hole currents:

$$J_T = J_n + J_p = qn_i^2 \left(e^{\frac{V}{U_T}} - 1\right) \left(\frac{D_n}{L_n N_A \tanh\left(T_p/L_n\right)} + \frac{D_p}{L_p N_D \tanh\left(T_n/L_p\right)}\right) \tag{16.56}$$

Defining the saturation current density J_s as

$$J_s = qn_i^2 \left(\frac{D_n}{L_n N_A \tanh\left(T_p/L_n\right)} + \frac{D_p}{L_p N_D \tanh\left(T_n/L_p\right)}\right) \tag{16.57}$$

The total current in the diode becomes

$$J_T = J_s \left(e^{\frac{V}{U_T}} - 1\right) \tag{16.58}$$

Additional Generation and Recombination Currents from the Space-Charge Region

Depending on the polarization of the pn junction, kinetics of capture and release of mobile carriers by traps in the depletion region are responsible for what is called generation and recombination currents; see [4, 5].

The cases of forward and reverse polarizations are discussed briefly.

Forward Polarization: Recombination-Current Contribution

When the forward bias V exceeds a few U_T, it can be shown that the recombination rate in the space charge region greatly simplifies and can be approximated with [1]:

$$r = \frac{n_i}{2\,\tau}\, e^{\frac{V}{2U_T}} \tag{16.59}$$

This approximation is valid for a limited extension of the depletion region, W_{rec}. This value, as well as the recombination rate, is only meant to give the overall voltage dependence of those additional currents, but is not an exact expression.

Adopting relation (16.59) for the recombination rate, the space charge recombination current is

$$J_{rec} = q\,r\,W_{rec} = W_{rec}\,\frac{q\,n_i}{2\,\tau}\, e^{\frac{V}{2U_T}} \tag{16.60}$$

This current adds to the diffusion currents of the diode in forward bias, and therefore it is dominant only at low forward voltage biases. In practical cases, the recombination current is a parameter which is extracted from measurements.

Reverse Polarization: Generation-Current Contribution

When the diode is reverse biased, traps in the depletion region will be responsible for enhanced thermal emission of carriers. The induced generation current can be approximated by

$$J_{\text{gen}} = -\frac{q\, n_i}{2\, \tau}\, W \tag{16.61}$$

This current adds to the reverse current of the diode; see Fig. 16.7. Note that since the depletion width slightly varies with the reverse bias, this generation current may have some weak dependence on bias too.

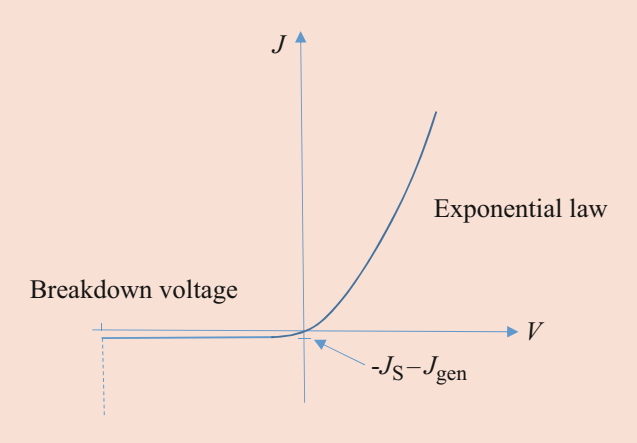

Fig. 16.7 Typical characteristics of a pn junction in forward and reverse bias. Note that the reverse bias cannot exceed a breakdown voltage beyond which the device will be damaged

16.2 Bipolar Transistors

16.2.1 Introduction

In 1947, the first bipolar junction transistor (BJT) was invented by a research team at Bell Laboratories using a germanium substrate. The bipolar junction transistor is one of the most important semiconductor devices. In this chapter we will learn about the bipolar junction transistors. The invention of the transistor led to the invention of many other semiconductor devices, including the integrated circuits, and enabled modern computers and complex electronic systems [6].

The bipolar junction transistor (BJT) is a three-terminal semiconductor device (see Fig. 16.8) which can act as a conductor or insulator based on the applied input signal; due to this property, the transistor can be used as a switch in the digital electronics or can be used as an amplifier in the analog electronics. Nowadays, the bipolar junction transistors are widely used in the electronic industry, and, therefore, anyone who is interested in electronics should have some basic knowledge of BJT [6].

A bipolar junction transistor (BJT) is a solid-state device used for high-speed circuits, analog circuits and power applications. It uses two types of carriers, electrons and holes, whence its name. In this chapter, we focus on the static

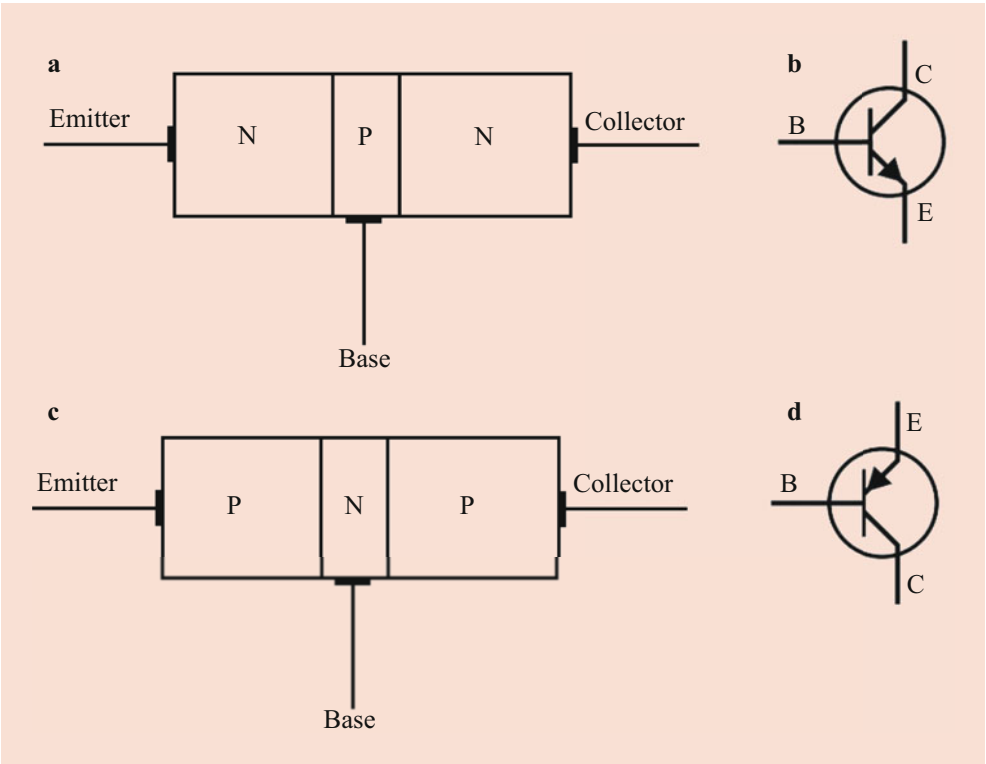

Fig. 16.8 The bipolar junction transistor (BJT) is a three terminal semiconductor device consisting of two semiconductor types, i.e., n-type and p-type. It involves two types of carrier, electrons and holes

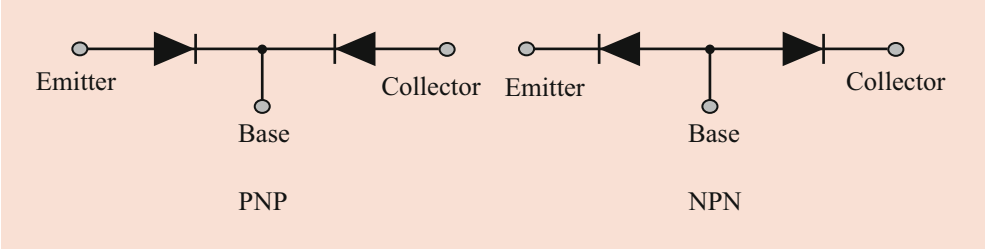

Fig. 16.9 Bipolar junction transistor (BJT) appears as if two back-to-back diodes were connected in series

characteristics obtained from the minority-carrier distributions in coupled p-n junctions. In the final section, we will end up with current gain and modes of operation of bipolar transistors.

16.2.2 Structure

As shown in Fig. 16.8, two types of bipolar transistor are available for BJTs, known as n-p-n (a, b) and p-n-p (c, d) [6]. The n-p-n bipolar transistor is the complementary structure to the p-n-p bipolar transistor. An n-p-n transistor shares a thin p-doped region sandwiched between two n-doped layers, while a p-n-p transistor shares a thin n-doped region sandwiched between two p-type layers. A BJT is a three-terminal device with base (B), emitter (E), and collector (C) contacting to three-doped semiconductor regions called emitter, base, and collector regions. The emitter region is heavily doped compared to the other two layers, and the collector dopant concentration is much smaller than the base one.

16.2.3 Principle of Operation

A BJT is made of two p-n junctions: one holds for the emitter-base junction, while the other defines the base-collector junction. These junctions appear as two back-to-back diodes connected in series (see Fig. 16.9). Actually, without additional analysis, such a device would not behave like a bipolar transistor because when connecting two back-to-back diodes, there is no interaction between them, which means that the two diodes are operating independently [6]. The main difference is that n- and p-type diffusions share the same crystal, i.e., there is no "contact" linking the diodes internally at the base level.

A careful analysis demonstrates that there is a strong interaction between the emitter and the collector by means of the intermediate base region. The emitter is heavily doped and its function is to supply the majority carriers, whereas the collector is lightly doped. The doping concentration of

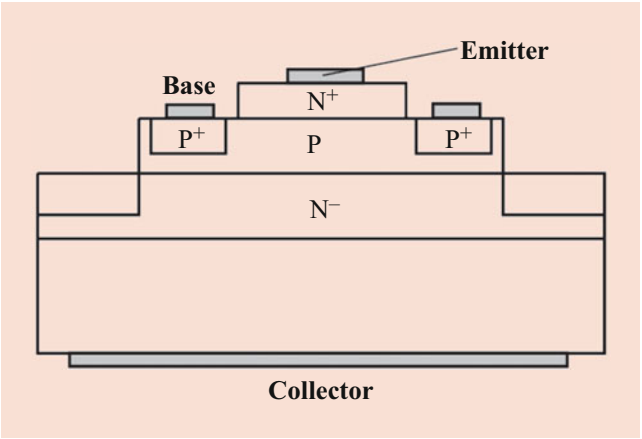

Fig. 16.10 Cross-sectional view of an n-p-n bipolar transistor

the base is between that of the emitter and the collector. In addition, the thickness of the base region is very narrow compared to the others, in order to avoid recombination of minority carriers which should travel across it before being be collected by the collector [6]. A typical cross-section is shown in Fig. 16.10.

From the point of view of applications, bipolar transistors operation is split in three distinct regions:

I. The **Active Region** where the transistor acts as an amplifier and where the base and collector currents are proportional (β is the current transistor gain): $I_C = \beta\, I_B$
II. The **Saturation Region** when the device is "fully-ON" and operates as a switch, $I_C = I_{C\,(Sat)}$
III. The **Cutoff Region** where the transistor is in "OFF-state" and operates as an open switch, $I_C = 0$.

These various modes depend on the biasing of each terminal.

In the active region of operation, the emitter-base junction is forward biased, and the base-collector junction is reverse biased. The voltage at the emitter is V_E, V_B at the base, and V_C at the collector. Considering by way of example the n-p-n transistors, in the active region the base voltage should be larger than that of the emitter, and the collector

voltage should be larger than that of the base (reverse biased collector-base junction).

In the cutoff region, both base-emitter and base-collector junctions are reverse biased. So, to operate the BJT in the cutoff region, both the emitter and collector voltages must be larger than the base voltage.

Lastly, when the BJT operates in saturation, both the base-emitter and base-collector junctions are forward biased, which means that the base voltage V_B must be larger than the emitter and collector voltages. In summary, these are the three regions of operation of the BJT (apart from a fourth one, known as "reverse active region of operation," where the role of the collector and emitter are interchanged [6], but which is not used).

Similarly, when the p-n-p transistor is considered, in the active region of operation the base-emitter junction is still forward biased and the collector-base junction is still reverse biased, but the emitter voltage is larger than the base voltage, and, similarly, the base voltage is larger than the collector voltage.

16.2.4 DC Operation of the n-p-n BJT Under Forward Active Mode

The principle of operation of a bipolar transistor relies on the fact that the base region of the transistor is very thin. The p-n junction between base and emitter is forward biased so that a current made of electrons flows from the emitter into the base, and a hole current flows from the base into the emitter. However, since these forward currents scale with the doping density, (see relations 16.48 and 16.49 for instance), the current injected by the base is negligible with respect to the emitter current (there are about two orders of magnitude between the doping of the base and that of the emitter). On the other hand, the base-collector junction is reverse biased. Most of emitter-injected electrons are swept straight through the very thin base. Once they reach the base-collector depletion layer, they are accelerated by the electric field in the depletion region and are swept across the depletion layer before being collected by the collector. The operating principle of bipolar devices is different from that of unipolar devices, e.g., field-effect transistors (FETs), where the current is controlled either by electrons or holes. BJTs are classified as minority-carrier devices [6].

16.2.5 Bipolar-Transistor Configurations

There are three possible ways to connect the bipolar transistor within a circuit:

- **Common-base configuration** with voltage gain but no current gain
- **Common-emitter configuration** with both current and voltage gain
- **Common-collector configuration** with current gain but no voltage gain
  - Whenever a BJT is used for ***amplification***, it is set in the active region adopting different configurations, i.e., common emitter, common base, common collector.
  - Whenever a BJT is used as a ***switch***, it works either in the saturation or in the cutoff region.

In this section, we discuss in detail these different regions of operation [6].

16.2.6 Common-Emitter Configuration

To use the BJT as an amplifier, the base-emitter junction is forward biased, while the collector-base junction is reverse biased (see Fig. 16.11 [6]).

In case of a common-emitter configuration, the emitter terminal is common to the input and the output ports (see Fig. 16.12). In this configuration, the input signal is applied between the base and the emitter, and the output signal is measured between the collector and the emitter.

More precisely, the base current is the input current while the collector current is the output current (see Fig. 16.13). Voltage V_{BE} is the voltage on the input side, and voltage V_{CE} is the voltage on the output side.

Supposing that DC biasing voltages are already applied, then superimposing a sinusoidal voltage between the base and emitter terminals will modulate the output voltage between the collector and emitter terminals, which can give rise to an amplification. In this configuration, to understand the behavior of the device, we need to understand two types of characteristics, namely, the input and output characteristics.

The input characteristic defines the relationship between the base current I_B and the base-to-emitter voltage V_{BE}.

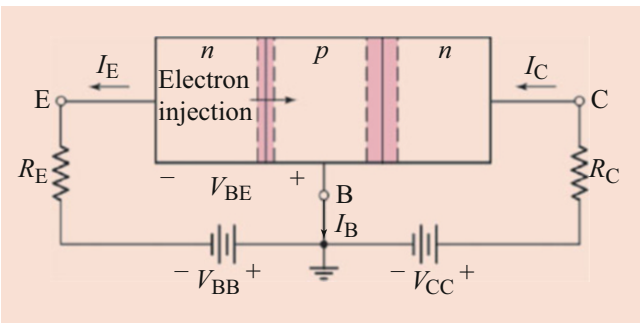

Fig. 16.11 n-p-n transistor biased in forward-active mode. Colored regions sketch the depletion regions of the pn junctions

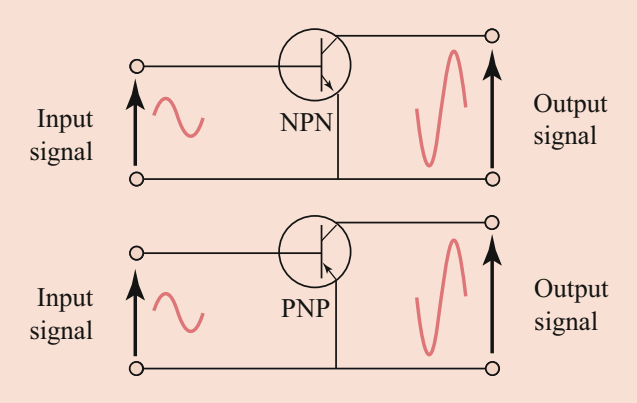

Fig. 16.12 The mostly used amplifier configuration of the bipolar transistor: the common-emitter configuration. Both n-p-n and p-n-p transistors are represented

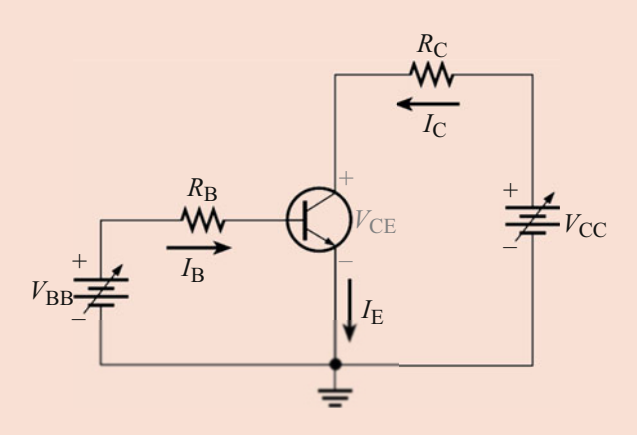

Fig. 16.13 Common-emitter biasing for the n-p-n transistor

Similarly, the output characteristic defines the relationship between the collector current I_C and the collector-to-emitter voltage V_{CE}. Figure 16.14 shows the input characteristics where I_B is plotted versus V_{BE} for different values of V_{CE}.

These curves look very similar to the forward characteristics of a pn junction diode, which is expected since the base-emitter junction on the input side is forward biased. However, note that as the V_{CE} increases, the base current decreases.

The V_{CE} voltage can be written as

$$V_{CE} = V_{CB} + V_{BE} \tag{16.62}$$

Note that for a fixed value of V_{BE}, if V_{CE} is increased, then V_{CB} will also increase, meaning that the reverse bias applied between the collector and the base terminal will increase. This means that the depletion region created at the collector-base junction will get wider (see, for instance, relation (16.27) for the case of a p-type doped semiconductor). Therefore, the effective base width will shrink, and so the probability of recombination for the minority carriers

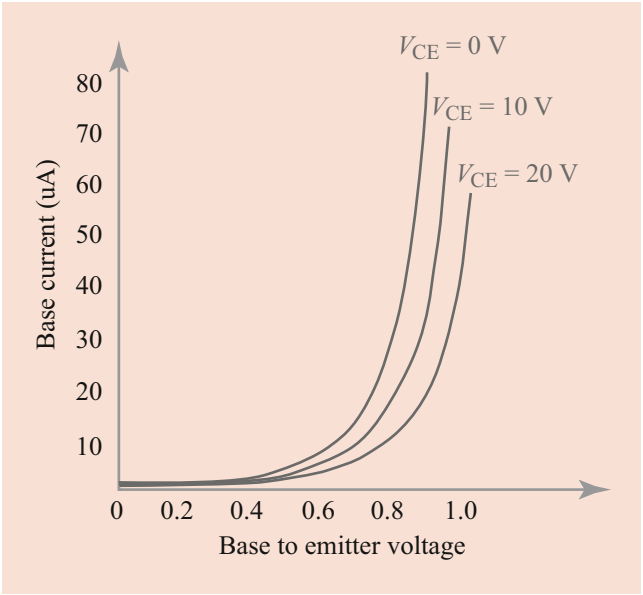

Fig. 16.14 Input characteristics of a BJT in the common-emitter configuration

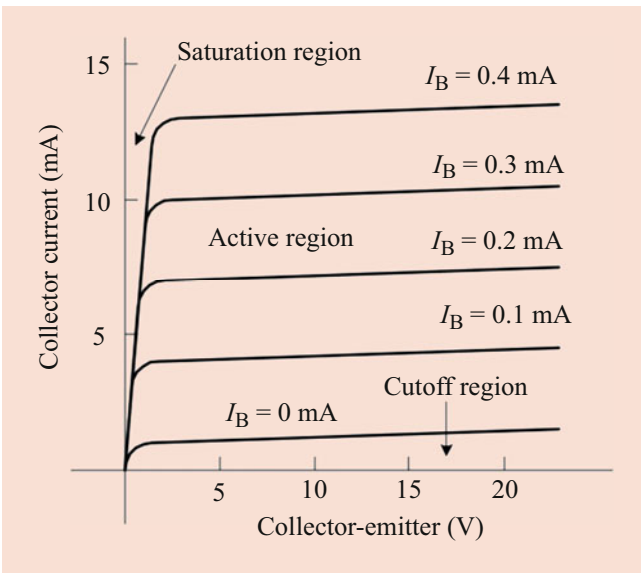

Fig. 16.15 Output characteristics of a BJT in the common-emitter configuration

injected by the emitter into the base will decrease, which will lower the base recombination current I_B. This quite empirical analysis explains the shift in the input characteristics plotted in Fig. 16.14.

In Fig. 16.15, the output characteristics show the relationship between the collector current I_C and V_{CE} for different base currents. Each curve can be divided into the three regions discussed before: one corresponds to the active region, the second to the saturation, and the third to the cutoff region.

In the case of active-region operation, since the base current I_B increases, the collector current increases as well. Here, unlike the common-base configuration, as V_{CE} increases and pushes the transistor in the active region, the collector current I_C also increases, meaning that the collector current characteristics are not strictly "horizontal."

Such a current increase with V_{CE} is attributed to a widening of the depletion region of the collector-emitter, reverse-biased pn junction, resulting in a shorter neutral region for the n-type base. As the effective base width reduces, the probability of recombination in this region will also decrease, and more electrons will be able to cross the base without recombining, meaning that the collector current will increase. Whenever the BJT is used as an amplifier, it is used in the active region. In this region, the base current gets amplified by a factor β, meaning that if I_B is the base input current and I_C is the collector current, then

$$I_C = \beta\, I_B \tag{16.63}$$

Note that under AC operation, this relation still holds, $\Delta I_C = \beta_{AC}\, \Delta I_B$.

Here, β_{AC} is the ratio of the collector- to base-current variations [6]. Usually the values of β_{AC} and β are not the same, but as they are very close to each other, they are often used without discrimination.

In case of operation in the saturation region, the collector-to-base junction and the base-to-emitter junctions are forward biased. This happens when the value of V_{CE} reduces so that the base-collector junction is no longer set in reverse bias. Indeed, as V_{CE} gets close to zero, the collector-to-base junction becomes forward biased. Note that when $V_{CE} = 0$, we obtain $V_{BC} = V_{BE}$, i.e., the base-to-collector junction is also forward biased.

The third region of operation corresponds to the so-called cutoff region.

In the cutoff region, the base current is set to zero, while the collector current is non-zero and can be relatively large. Its expression reads

$$I_C = \alpha\, I_E + I_{CBO} \tag{16.64}$$

where I_{CBO} is the reverse saturation current.

Also, remembering that $I_C = I_E + I_B$, the collector current is equal to

$$I_C = \alpha\ (I_E + I_B) + I_{CBO}. \tag{16.65}$$

Rearranging the above equation, we can write

$$(1-\alpha)\ I_C = \alpha\, I_B + I_{CBO} \text{ or, equivalently}$$

$$\begin{aligned} I_C &= \alpha/(1-\alpha)\ I_B + 1/(1-\alpha)\ I_{CBO} \\ &= \beta\, I_B + 1/(1-\alpha)\ I_{CBO} \end{aligned} \tag{16.66}$$

Whenever the base current I_B is zero, the collector current reduces to $1/(1-\alpha)\, I_{CBO}$.

Typically, the value of α varies from 0.95 to 0.99., meaning that $1/(1-\alpha)$ can be quite large.

On the other hand, the current gain satisfies $1/(1–\alpha) = (\beta + 1)$. Therefore, whenever the base current is set to zero, the "leakage" collector current I_{CEO} is $I_{CEO} = (\beta + 1)\, I_{CBO}$.

It represents the leakage current that flows from the collector to the emitter whenever the base terminal is open.

By way of example, if β is equal to 99 and the value of I_{CBO} is equal to 1 uA, the current I_{CEO} will be equal to 100 uA, which is a quite large leakage current.

As we mentioned already, in the active region of operation the input current gets amplified by the β factor, which is known as the current gain of this configuration. Whenever a load is inserted at the collector or emitter terminals, then we can also obtain a gain in terms of voltage.

So this common-emitter configuration provides the moderate current gain as well as the moderate voltage gain, but it provides very high power gain. This is why this configuration is frequently used for the signal amplification. However, the input and output impedances are in the moderate range. In this configuration, typically the output impedance lies in the range of 50–100 kΩ, which is high, but lower than that of the common-base configuration. Similarly, the input impedance is in range of kΩ, which can be found from the slope of the input characteristics. Here, the input impedance is given by

$$R_{in} = \Delta V_{BE}/\Delta I_B \tag{16.67}$$

16.2.7 Common-Collector Configuration

Similarly, in case of the common-collector configuration, the collector terminal is common between the input and output side (Fig. 16.16).

In this configuration, the input is applied between the base and the collector terminal, and the output is measured between the emitter and the collector terminal (see Fig. 16.16). To use this configuration as an amplifier, it necessary to bias it in a such a way that the base-emitter junction gets forward biased and the collector-base junction gets reverse biased. In fact, in terms of DC biasing, it resembles the common emitter configuration.

From the DC perspective, Fig. 16.17 shows how typical biasing voltages are applied [6].

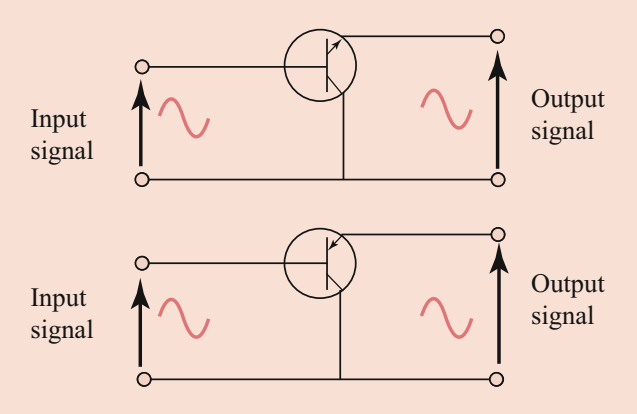

Fig. 16.16 Common-collector configuration

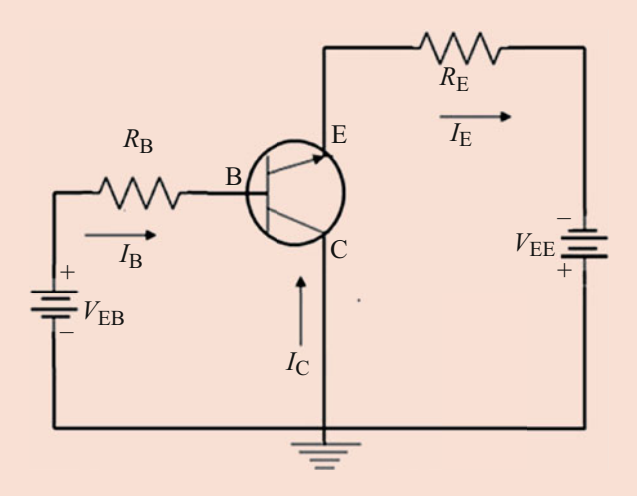

Fig. 16.17 Common-collector configuration

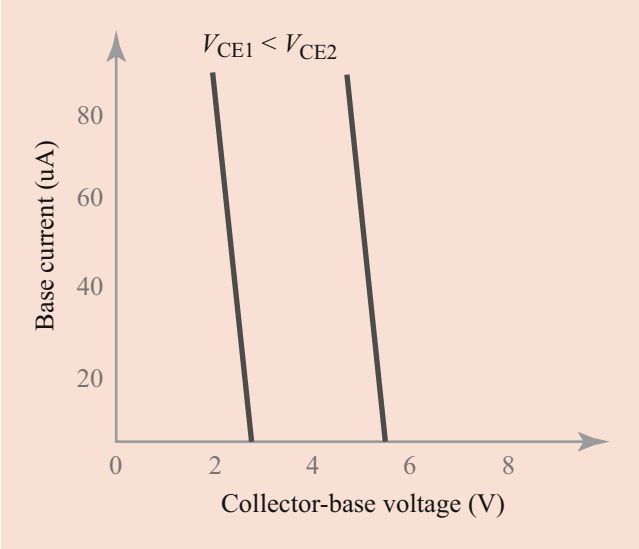

Fig. 16.18 Input characteristic of a common-collector configuration

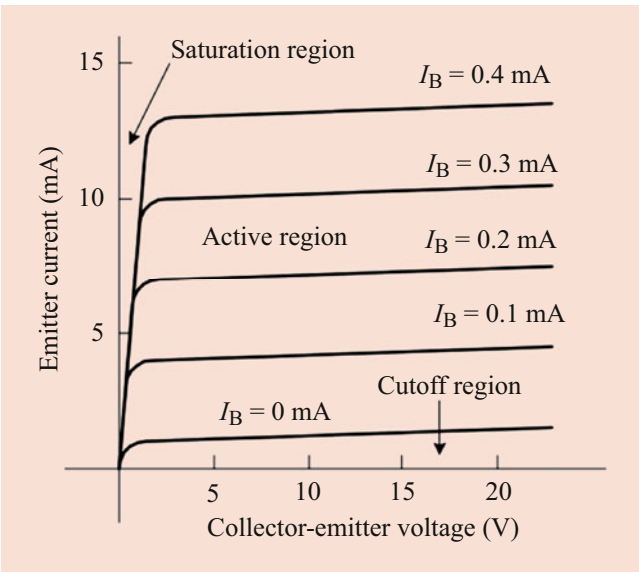

Fig. 16.19 Output characteristics of a BJT in the common-collector configuration

The base current is the current on the input side, while the emitter current is the current on the output side. The emitter current can be expressed as [6, 7]

$$I_E = \alpha\, I_C \tag{16.68}$$

As the value of α is very close to unity, the emitter current is approximately equal to the collector current and that's why the output characteristic in this configuration is very similar to that of the common-emitter configuration.

Similar to other configurations, the behavior of the device can be described by two characteristics, i.e., the input and the output characteristics.

The output characteristics define the relationship between emitter current I_E and V_{CE}, which is very similar to the common-emitter configuration.

The input characteristics show the relationship between the base current I_B and V_{CB}. As shown in Fig. 16.18, for a fixed value of V_{CE}, the base current decreases as the reverse collector-base junction bias V_{CB} increases.

In addition, as seen in the output characteristics (Fig. 16.19), for a fixed value of V_{CB}, the base current I_B increases as V_{CE} increases. This is expected since the base-emitter forward bias V_{BE} will increase ($V_{BE} = V_{BC} + V_{CE}$).

As mentioned already, in the common-collector configuration, the emitter current is the current on the output side, while the base current is the current on the input side; the ratio between this emitter current to the base current is known as the current gain and is denoted by symbol γ:

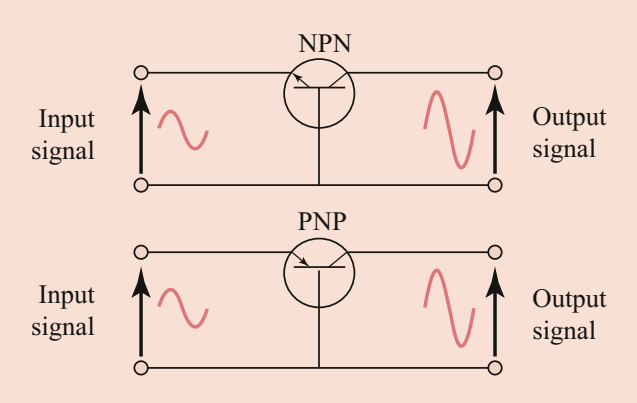

Fig. 16.20 Common-base configuration

$$\gamma = I_E/I_B \tag{16.69}$$

An interesting feature of the common-collector configuration is a very high input impedance and very low output impedance; therefore, it is often used for the impedance matching in circuit amplifiers. Moreover, it provides a very high current gain and a very low voltage gain. In this configuration, the current gain is equal to $\beta + 1$ while the voltage gain is close to unity.

Common-base configuration: Likewise, in the common-base configuration, the base terminal is common between the input and the output side (Fig. 16.20).

Here, the input is applied between the base and the emitter terminal, and the output is measured between the collector and the base terminal. When this configuration is used as an amplifier, the BJT must work in the active region of operation. This means that the base-emitter junction is forward biased and the collector-base junction is reverse biased. For the n-p-n transistor, the applied bias should be set up as shown in Fig. 16.21 [7].

The base-emitter junction is forward biased and the collector base junction is reverse biased. The emitter current will exit the transistor, while the base current and the collector current will enter into the transistor. In case of a p-n-p transistor, the direction of the currents reverses. In all cases, the emitter current is the sum of the base current and the collector current [6].

In this common-base configuration, the behavior of the device can be described by two characteristics, the input and output characteristics. These characteristics are similar to the I-V characteristics which we have seen for the diode. These characteristics show the behavior of the device when the voltage and the current are interchanged. In this case, the emitter current is the input current, and the voltage between the base and the emitter terminal, V_{BE}, is the input voltage.

Therefore, the input characteristics define the relationship between the base-emitter voltage and the emitter current for

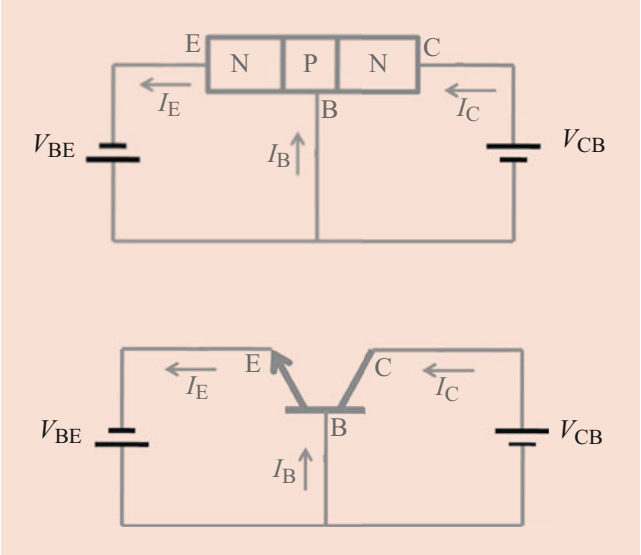

Fig. 16.21 Common-base configuration

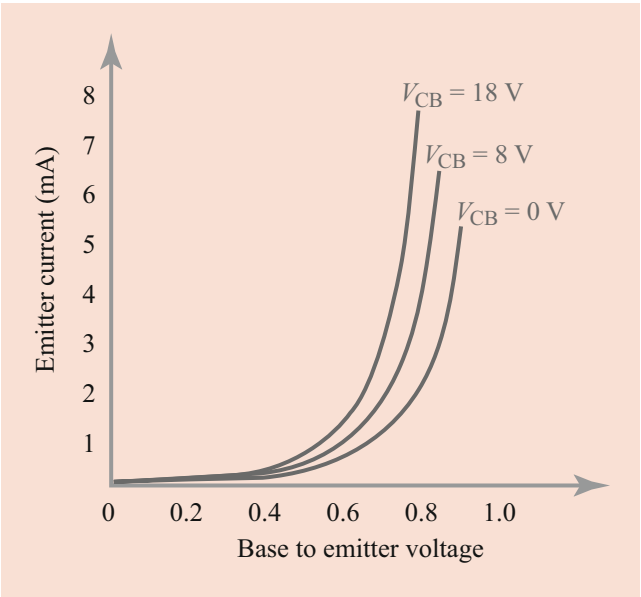

Fig. 16.22 Input characteristics of a BJT in the common-base configuration

a fixed value of V_{CB}. Throughout this discussion, the n-p-n transistor will be considered, whose input characteristics in the common base configuration have the form shown in Fig. 16.22 [6, 7].

As illustrated in Fig. 16.22, there are three curves for the different values of V_{CB}. These curves look similar to the forward characteristics of the pn junction, since the input side corresponds to the forward biasing of the base-emitter diode. As V_{CB} increases, the curve slightly shifts toward the left-hand side and, at the same time, the emitter current also increases. The reason is that when the collector-base junction gets more and more reverse biased, the width of

the depletion region increases. Due to that, the base region will get narrower, and therefore a smaller voltage is sufficient to forward bias the emitter-base junction. From the input characteristic, the input impedance of the device is obtained by considering the slope of the curve. The input resistance is equal to

$$R_i = \Delta V_{BE}/\Delta I_E \tag{16.70}$$

One notes that a small change in V_{BE} produces a large change in the emitter current. This means that in this configuration, the input impedance of the device is very low. This is expected because in the forward-bias conditions, the resistance of the pn junction diode is very small and is typically in the range of ohms, thus a quite low value.

Output characteristics: the collector current is the output current, and the voltage between the collector and the base terminal is the output voltage. The output characteristic defines the relationship between this collector current and the collector-base voltage when the input parameters (among which is the emitter current) are kept constant. If the collector-to-base voltage is changed, then the collector current will change as in Fig. 16.23, where the curves are shown for different values of the emitter current. As the emitter current increases, the collector current increases linearly.

In each curve there are three regions: the active region, the cutoff region, and the saturation region.

In the active region, the relationship between the collector current and the emitter current can be fairly well described by $I_C = \alpha\ I_E$. Here the emitter current is the input current, and the collector current is the output current. The ratio of this collector current to the emitter current gives the current gain α of the BJT in the common-base configuration. In this configuration, even if the reverse collector-base voltage is increased, the increase in the collector current remains marginal [6–8].

Here, the collector behaves like a constant current source, and, for a fixed value of emitter current, it is almost independent of the collector-to-base voltage. Hence, since the collector current only changes proportionally to the input current, this region is used for amplification.

The saturation region. In this region, as V_{CB} is lowered and becomes negative, the collector current starts to decrease. Indeed, without a reverse bias across the collector-base junction, electrons injected from the emitter will hardly be collected by the electric field at the collector junction, thus decreasing the collector current. Therefore, whenever the emitter-base and collector-base junctions are simultaneously forward biased, the BJT operates in the saturation region.

The cutoff region. Whenever the emitter current is zero, the collector current will remain close to zero even if the collector-to-base voltage is increased, since this junction is still reverse biased. To be more precise, the collector current will be very small and will consist in the reverse saturation current of the reverse-biased, collector-base pn junction, which originates from thermal generation of minority carriers. The total collector current I_{CT} is then given by

$$I_{CT} = I_C + I_{CO} \tag{16.71}$$

where I_{CO} is the reverse saturation current.

In the case of a common-base configuration, the emitter terminal is kept open; the reverse saturation current flows between the collector and base terminals and is termed I_{CBO}. This current is similar to the reverse saturation current which was discussed for the diode (note that, as for the diode,

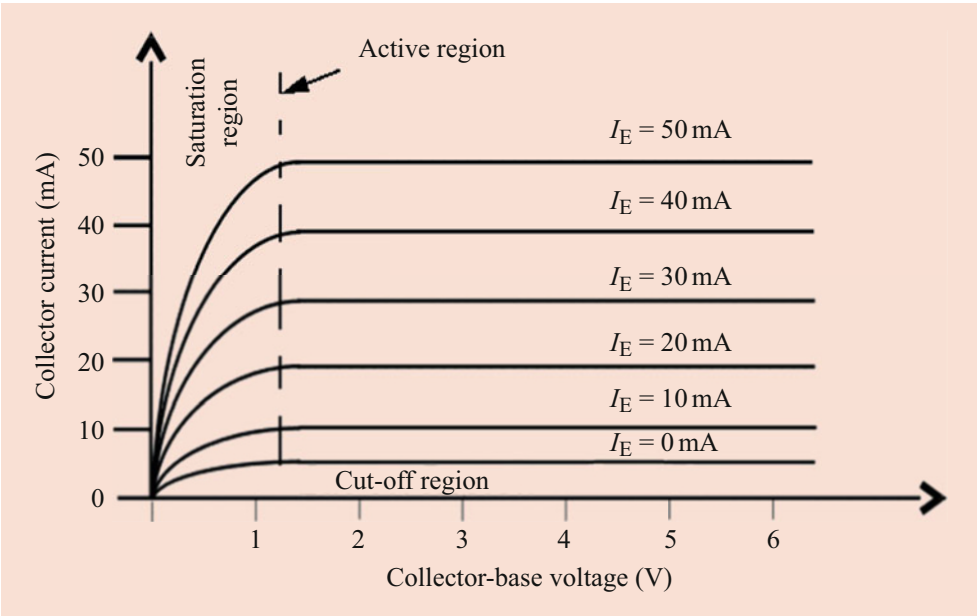

Fig. 16.23 Output characteristics of a BJT in the common-base configuration. The vertical, dashed line indicates the limit of the active region

the reverse saturation current is sensitive to temperature: when temperature increases, the reverse saturation current increases). Due to the improvement in technology, the reverse saturation current is typically in the nA range, meaning that in the cutoff region the collector current is practically negligible (note that for high-power transistors, this current is in the μA range).

In conclusion, the total collector current I_{CT} can be expressed as $I_{CT} = I_C + I_{CBO}$, or in terms of the emitter current

$$I_{CT} = \alpha\, I_E + I_{CBO} \tag{16.72}$$

As already mentioned, in this configuration, the input impedance is very low, typically in the range of ohms. In order to carry on an estimate, assume that the input impedance or the input resistance is equal to 10 Ω and that the input voltage is equal to 5 mV, so that the input current is 0.5 mA. If one assumes that α is equal to 1, then the output current is the same as the input current (since the collector current I_C equals $\alpha\, I_E$). This means that the same current will also flow in the output circuitry. For the common-base configuration, the output impedance R_0 is very high [8].

This is also evident from the output characteristics of Fig. 16.23. In fact, in the active region of operation, when the collector-base voltage increases, the collector current remains almost constant, meaning that the output resistance $\Delta V_{CB}/\Delta I_C$ is very high, typically in the range of hundreds of kΩ. In the example considered here, if the output impedance R_0 is 100 kΩ and R_L is 1 kΩ, V_0 is given by

$$V_0 = I_0 \times R_L = 0.5\,\text{mA} \times 1\,\text{k}\Omega = 500\,\text{mV} \tag{16.73}$$

In this example, the input voltage is 5 mV while the output voltage is 500 mV, namely, the input signal gets amplified by the factor of 100, or, equivalently, the voltage gain is equal to 100.

In conclusion, in the common-base configuration the voltage signal is amplified, whereas the ratio of the collector current to the emitter current is less than unity. This means that whereas the current gain in the common-base configuration is less than 1, it still provides a substantial voltage gain: typically, the voltage gain in this configuration varies from 50 to 300.

It should be noted that the same current is transferred from the input side toward the output side: this means that there is a transfer of current from the low-resistance to the high-resistance circuit; this is why the BJT was named as "transistor" (*transfer resistor*) [6–9].

16.2.8 Common-Emitter Amplifier

With reference to Fig. 16.13, for the base and the collector supplies a double subscription is used, namely, V_{BB} is the source voltage for the base and V_{CC} is the source voltage connected to the collector terminal. The V_{BE} voltage defines the difference between the voltage at the base and emitter terminals, namely, $V_{BE} = V_B - V_E$ and, similarly, $V_{CE} = V_C - V_E$.

Therefore, the base and collector voltages are applied in such a way that the base-emitter junction will be forward biased and the base-collector junction will be reversed bias; in other terms, V_B and V_C are both positive. In addition, whenever the base-emitter pn junction is forward biased, the typical voltage drop across this junction is in range of 0.6 to 0.7 V.

Once the electrons injected from the emitter enter the base region, they become minority carriers; as the base-collector junction is reverse biased, these electrons will be pushed by the electric field toward the collector terminal. It follows that most of the electrons which are injected by the emitter will be collected by the collector region, while a very small amount of electrons will flow into the base terminal. The relations among the currents are established by applying, first, the Kirchhoff law [6, 7, 9],

$$I_B + I_C = I_E \tag{16.74}$$

where the emitter current is the sum of the base and collector currents. As already mentioned, only a fraction of the injected electrons enters the base terminal; thus, the base current will be very small, and, therefore, the collector current is approximately equal to the emitter current:

$$I_C \approx I_E \text{ or } I_C = \alpha\, I_E \tag{16.75}$$

where α defines what fraction of the emitter current is flowing through the collector. Replacing (16.75) in (16.74) yields

$$I_B + \alpha\, I_E = I_E \text{ or } I_B = (1-\alpha)\; I_E = (1-\alpha)\; I_C/\alpha \text{ or } I_C = \alpha/(1-\alpha)\; I_B = \beta\, I_B \tag{16.76}$$

where β is given by [8].

$$\beta = \alpha/(1-\alpha) \tag{16.77}$$

Parameter β is known as the "current gain" of the BJT; its typical values vary from 50 to 400. From these expressions, we can write

$$I_B + I_C = I_E => I_B + \beta\, I_B = I_E => I_E = (\beta + 1)\ I_B. \tag{16.78}$$

Note that the base current is the current on the input side while the collector current is the current on the output side, these two currents being related by (16.76) [7].

That means that controlling the base current on the input side controls the collector current, which is the reason why the bipolar junction transistors are known as the "current-control devices." In contrast, the other type of transistor known as the field-effect transistor is a voltage-controlled device where controlling the input voltage controls the output current. In the configuration of the BJT described above, the output collector current is amplified by the factor β, and, by connecting a resistor between the collector and the emitter terminal, it is also possible to amplify the input signal: in other terms, when the BJT is used in this common emitter configuration, an input AC signal will be amplified.

So far we have not considered the minority carriers in the collector region when the base-collector junction is reverse biased. If the emitter is left open, the current which flows through the collector is only due to minority carriers, and equals I_{CO}. Therefore, this current is similar to the reverse saturation current of the pn junction diode.

In conclusion, the total collector current is given by [6]

$$I_{CT} = I_C + I_{CO}, \tag{16.79}$$

where I_{CO} is the current due to the minority carriers; its typical values are in the range of μA, while those of the collector current I_C are in the range of mA [7, 8].

16.3 The Metal-Semiconductor Schottky Diode

16.3.1 Introduction

In addition to the pn junction, when properly designed, a metal-semiconductor contact may exhibit an asymmetric electrical characteristic that can be used to rectify currents [10]. Initially, the metal-semiconductor rectifier was simply made of a sharp metal pressed on the bare surface of a piece of semiconductor. This kind of device was known well before the physics of semiconductors was understood as was widely used in the early age of radio receivers, the so-called galena-rectifier crystal detector, a metal lead sulfide point-contact device. Later on, Schottky explained this "anomalous" rectifying behavior in terms of space charge in a lightly doped semiconductor, giving its name to this device, i.e., the Schottky diode. The main feature of the Schottky diode with respect to the "usual" pn junction diode is the quite low forward voltage which is about 0.3 volt, compared to 0.7 volt for silicon based pn junctions. Another advantage if the fast recovery time when used in switching applications since only majority carriers are involved, avoiding the recombination time delay inherent to the injection of minority carriers in pn junctions. In addition, Mead [11] proposed to use the property of the Schottky contact as the gate electrode for GaAs field effect transistors, namely, the metal-semiconductor field effect transistor (MESFETs), since, unlike silicon, a reliable oxide is missing in these alloys. The device structure was further refined by Hooper [12]. Today, this Schottky contact is widely used in high-electron mobility transistors (HEMTS) made of III-V semiconductors [13] (see [14] for an overview of applications).

Energy Analysis of Isolated Metal-Semiconductor Systems

The way charges are transferred between a metal and a semiconductor when these come in contact is a fundamental question since it governs the electrical properties of the metal-semiconductor interface [15]. The physics of this hybrid contact can be understood by examining the relative energies of the conduction and valence bands in each material near the interface, in particular the band bending inside the semiconductor. A primary analysis is to consider the amount of energy required to extract an electron, either from the metal or from the semiconductor into vacuum.

From a didactic point of view, it is instructive to consider first the semiconductor and the metal isolated from one another to neglect any interaction between them (see Fig. 16.24). Without loss of generality, we assume an n-type low-doped semiconductor. The Fermi energy as well as the conduction and valence band extrema are drawn, as for the vacuum level.

For each material, a minimum energy is required to extract an electron out of the body into vacuum, i.e., away from the surface. In semiconductors and insulators, this energy is the affinity $q\chi$ which holds for the energy separation between the bottom of the conduction band and the vacuum level.

The electron affinity is an intrinsic energy that depends on the chemical composition and crystalline structure of the material, but not on the doping density of the semiconductor (at least as far as the amount of impurities does not affect the composition, which is assumed).

Concerning metals, since the density of states at the Fermi level is very high (and the Fermi energy is "fixed" due the large amount of electrons), it is the energy separation between the Fermi level and the vacuum level that will be considered as the minimum energy required to extract an electron, that is, the work function. Note that, in semiconductors, the work function will then depend on the doping density (in semiconductors, the Fermi level depends strongly on doping), whereas this quantity can be considered constant in metals.

Energy Distribution Across a Metal-Semiconductor Contact

The relative position of energies in Fig. 16.24 is modified when the metal and the semiconductor come into contact. The energy difference between their electronic states is responsible for a transfer of electrons between the metal and the semiconductor until an equilibrium is reached. The new energy profile of the metal-semiconductor system is sketched in Fig. 16.25.

When no external voltage is applied between the metal and the semiconductor, the Fermi levels in each solid should be equal. Given that the electron affinity and work function are "invariant" quantities for the semiconductor and the metal, respectively, an intrinsic potential drop V_{bi} will build up in the semiconductor (see Fig. 16.25).

For instance, when the work function of the metal is higher than the affinity of the semiconductor, some electrons in the semiconductor are transferred into the metal, leaving ionized donors in a depletion region close to the interface. Since the free-carrier concentration in the metal is very high, the potential drop will mainly take place in the semiconductor.

As for the pn junction, the depletion region generates a built-in voltage V_{bi}. This built-in voltage is the difference between the work function of the metal and the semiconductor

$$V_{bi} = \varnothing_M - \varnothing_{SC} \tag{16.80}$$

On the other hand, the difference between the metal work function and the semiconductor electron affinity is responsible for the energy barrier seen by electrons in the metal at the Fermi level:

$$\varnothing_B = \varnothing_M - \chi_{SC} \tag{16.81}$$

The built-in voltage V_{bi} can also be written in terms of the Fermi energy with respect to the conduction band minima:

$$V_{bi} = \varnothing_B - \varnothing_F \tag{16.82}$$

Whereas $\varnothing_B$ is fixed for a metal-semiconductor system (relation 16.81), relation (16.82) highlights that the built-in voltage depends on the doping density in the semiconductor through the Fermi energy $q\varnothing_F$.

These barrier energies are those that will control the flux of electrons across the interface.

In addition, as for the pn junction, the potential drop inside the semiconductor creates a depletion width W. Under the full depletion approximation, W is given by

$$W = \sqrt{\frac{2\varepsilon_{sc} V_{bi}}{qN_D}} \tag{16.83}$$

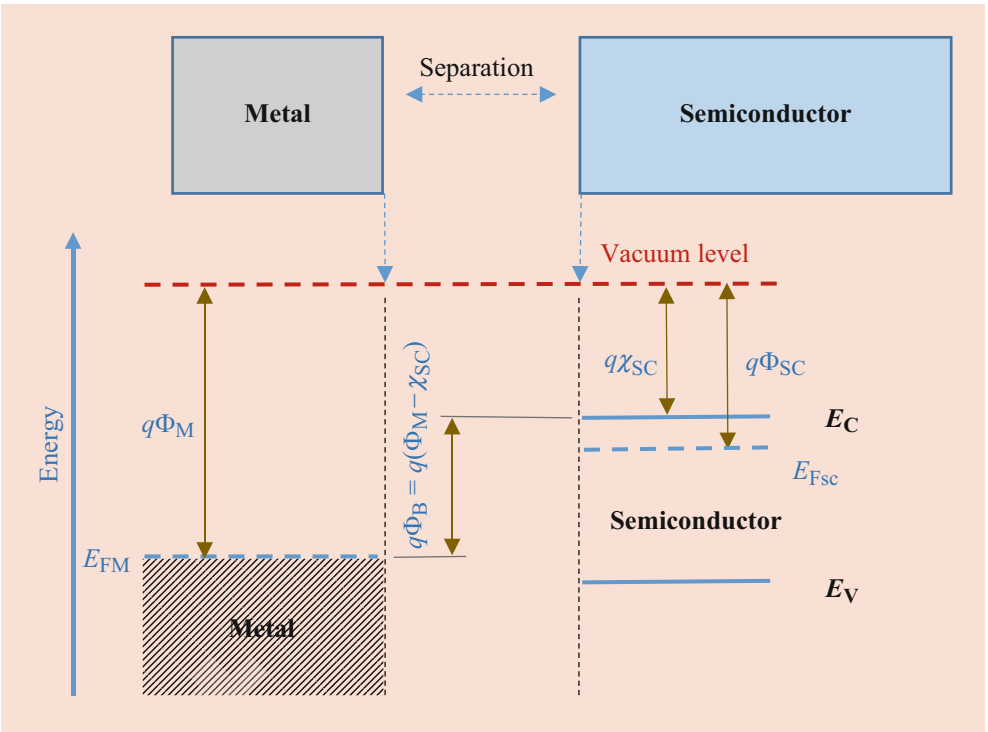

Fig. 16.24 Energy diagram for a metal and a semiconductor when these are separated with negligible interaction. Each material is then characterized by the energy needed to extract an electron into vacuum, i.e., the electron affinity $q\chi$ for semiconductors and the work function $q\Phi_M$ for metals

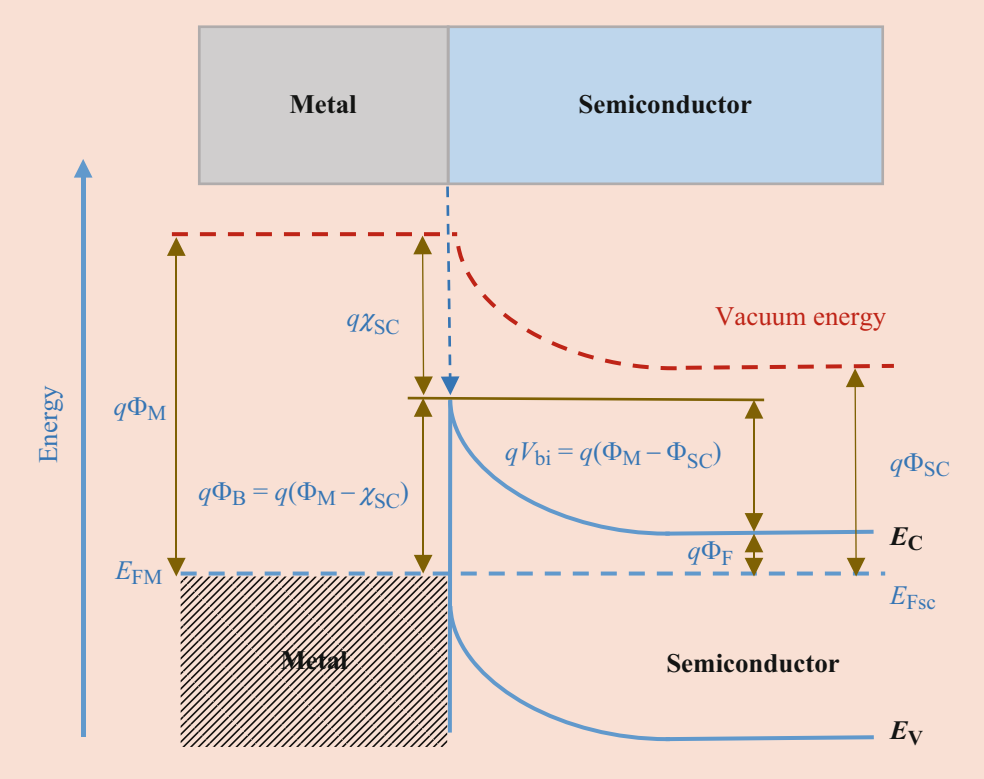

Fig. 16.25 Energy diagram across a metal semiconductor interface at equilibrium. The transfer of electrons from the low n-doped semiconductor into the metal creates a depletion region and an energy barrier qV_{bi} that drops essentially in the semiconductor

The built-in voltage and the depletion depth will then depend on the metal work function, the semiconductor affinity, and the doping.

The Schottky Diode Under Non-equilibrium

When applying a voltage V across the metal-semiconductor junction, the Fermi energies between the metal and the semiconductor split by qV, thus modifying the energy profile at the interface.

There are mainly two approaches to model the voltage-current characteristics of the Schottky diode. Whereas it is quite common to assume that the current is generated by thermionic emission of majority carriers over the barrier energies, another description of charge transport across the interface relies on drift and diffusion currents taking place in the depletion region of the semiconductor, while ensuring the current-continuity condition. Here, we will adopt the thermionic emission viewpoint without necessarily detailing all the steps, which would go beyond the aim of the section. It can be shown that for semiconductors with relatively large mobility and moderate doping densities, the thermionic emission theory is justified.

The thermionic emission at the metal-semiconductor interface is understood in terms of injected fluxes of electrons originating from the metal and the semiconductor at the interface and therefore depends on the electrons concentration at the barrier (see Fig. 16.26).

The current density arising from the transfer of electrons from the semiconductor into the metal (J_{sc-m}) scales linearly with the electron density n_B in the conduction band of the semiconductor evaluated at the barrier peak

$$|J_{sc-m}| = K\, n_B \tag{16.84}$$

where K is a multiplying factor that will not be detailed here.

In the semiconductor, at the barrier interface, the electron density n_B follows the Boltzmann statistics (non-degenerate semiconductor):

$$n_B = N_C e^{-\varnothing_B/U_T} \tag{16.85}$$

where N_c is the effective density of states of the semiconductor and $q\varnothing_B$ is the Fermi level with respect to the conduction band evaluated at the interface.

Then, the current density originating from the transfer of electrons from the semiconductor into the metal can be written as

$$|J_{sc-m}| = K\, N_C e^{-\varnothing_B/U_T} \tag{16.86}$$

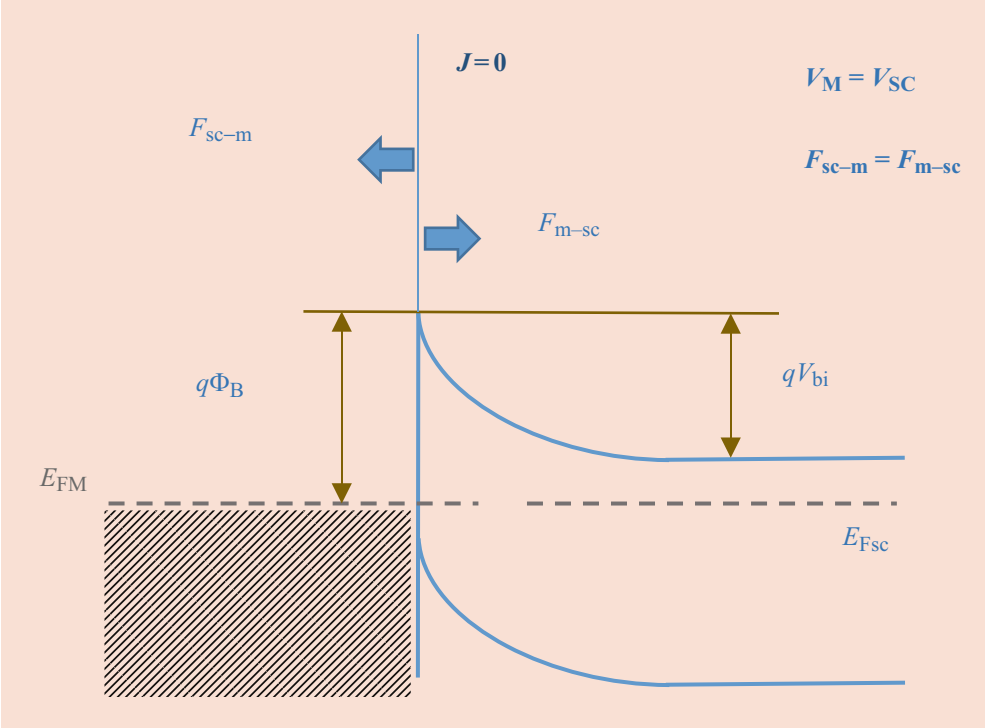

Fig. 16.26 Energy representation of the metal-semiconductor junction under zero bias, i.e., $V_M = V_{SC}$. The fluxes of electron injected by the metal F_{m-sc} and by the semiconductor F_{sc-m} compensate each other

Since under equilibrium, at zero bias, the Fermi levels of the metal and the semiconductor are aligned, no current flows across the structure (see Fig. 16.26). This means that the currents injected between the metal and the semiconductor cancel each other, and therefore the current density injected by the metal into the semiconductor is known at zero bias:

$$|J_{m-sc}| = |J_{sc-m}| = K\, N_C e^{-\varnothing_B/U_T} \tag{16.87}$$

Conversely, when biasing the metal positively by V_f with respect to the n-type semiconductor, the semiconductor-metal built-in potential is decreased, see Fig. 16.27. Since the barrier seen by electrons in the semiconductor is lowered, their transfer rate into the metal F_{sc-m} will increase.

The electron density at the barrier, in the semiconductor, is now

$$n_B = N_C\, e^{-(\varnothing_B - V_F)/U_T} \tag{16.88}$$

and so the current density injected by the semiconductor into the metal becomes

$$|J_{sc-m}| = K\, N_C e^{-(\varnothing_B - V_F)/U_T} \tag{16.89}$$

On the other hand, the energy barrier seen by electrons in the metal is unchanged since the potential drop occurs almost entirely in the semiconductor, implying that the electron transfer flux from the metal into the semiconductor F_{m-sc} will not change.

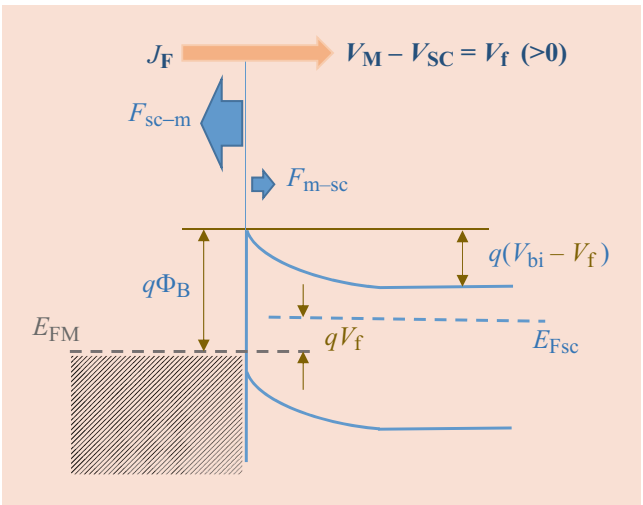

Fig. 16.27 Energy representation of the metal-semiconductor junction under forward bias. The flux of electrons injected by the semiconductor F_{sc-m} dominates with respect to the metal-induced flux F_{m-sc}, giving rise to a net current density J_F across the junction

The current density J_{m-sc} is then still given by relation (16.87).

The case of a negative voltage V_R applied to the metal is illustrated in Fig. 16.28.

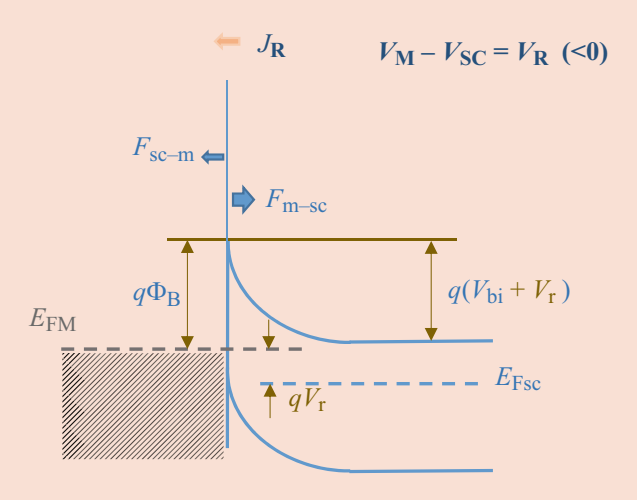

Fig. 16.28 Energy representation of the metal-semiconductor junction under reverse bias. The flux of electrons injected by the semiconductor F_{sc-m} is negligible. The current generated by the flux of electrons F_{m-sc} is the leakage current of the diode

Here the barrier seen by the electrons in the semiconductor is increased by qV_R, meaning that crossing the barrier becomes more unlikely. Conversely, the energy barrier seen by the electrons in the metal, i.e., $q\varnothing_B$, remains unchanged, and so for the flux F_{m-sc}.

The electron current density flowing from the metal into the semiconductor is

$$J = |J_{sc-m}| - |J_{m-sc}| = K N_C e^{-\varnothing_B/U_T} \left(e^{V/U_T} - 1\right) \quad (16.90)$$

Introducing the saturation current density $J_S = A T^2 e^{-\varnothing_B/U_T}$, the current-voltage dependence of the Schottky diode writes

$$J = J_S \left(e^{V/U_T} - 1\right) \quad (16.91)$$

where A is the Richardson constant given by

$$A = \frac{4\pi q m^* k^2}{h^3} \quad (16.92)$$

Relation (16.92) is formally the same as for the pn junction. However, the current in the Schottky diode is made of majority carriers, and therefore no recombination process is involved. This property is beneficial when fast *switching-off* is needed since it gets rid of the time limitation inherent to recombination processes with minority carriers.

16.3.2 Additional Factors

The simplified model derived in this section is an ideal picture of the Schottky diode. In reality, the interface between the semiconductor and the metal is populated with defects that introduce energy levels into the band gap of the semiconductor at that interface. These traps are inherent to dangling bonds, crystal defects, and contaminations at the surface of the semiconductor that are generated during the fabrication process. Their charge state can change dynamically upon bias and modify the electrostatic potential at the metal-semiconductor interface. Traps can also increase leakage current in reverse bias since they intensify electron transfers through forbidden states in the band gap.

In addition, even considering an ideal interface, the barrier potential is still lowered by the presence of electrons in the vicinity of the interface that attract positive charges from the metal. This is known as the image-force lowering concept, whose effect is to reduce the energy of the barrier and hence to increase the current density.

Including these effects goes beyond the scope of this chapter. Interestingly, relation (16.91) remains still valid provided an equivalent Richardson constant A^* is used for the saturation current density.

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Memory Challenges

17

Carlo Cagli and Luca Perniola

Contents

17.1 Overcoming the Concept of Universal Memory 604

17.2 "NVM Candidates" 606
17.2.1 OxRAM 608
17.2.2 Phase Change Memory (PCM) 608
17.2.3 MRAM 610
17.2.4 FeFET 610

17.3 How eNVMs Compare to Each Other 612
17.3.1 eNVMs Comparison 612
17.3.2 Most Relevant eNVM Demonstrators 618
17.3.3 Innovative Applications 618

17.4 eNVM for Neuromorphic Applications 622

17.5 Memory Selectors 626

References 628

Abstract

In the following chapter, we will present a summary of the most interesting emerging nonvolatile memories that have been studied in the last two decades. The particular point of view adopted will focus on the advancements achieved by these competing devices and, most importantly, the challenges that these technologies must face in the next years.

We decided to limit the analysis to four main competing technologies, namely, OxRAM (oxide-based resistive random access memory), PCM (phase change memory), STT-MRAM (spin-transfer torque magnetic RAM), and FeFET (ferroelectric field effect transistor). These four best show the development of the research activity on emerging memory devices, going from the most recent FeFET to one of the most mature PCMs. As each technology is based on a completely different physics, the challenges that each must face on are totally different.

The chapter is composed of four sessions. The first one highlights the need to overcome the concept of "universal memory," a longed-for memory device that could be tuned to substitute any memory currently preset in the PC memory hierarchy by minor adjustments and that could thus impose itself as the only memory really necessary. We will see how this concept, although very attractive and seducing, is unrealistic and must be abandoned to be replaced by an application-centric point of view, where each domain dictates the specifications that a memory has to provide and decide at the end what kind of device suits best.

In the second session, the four memory candidates are presented. A very short history of each is sketched and their working principle is briefly depicted.

Session three is the chapter core. The four memory devices are compared to each other; the advantages of each are analyzed along with their main drawbacks and flaws. Each memory, although at a different maturity level, has many challenges to overcome, and the session provides explication of each. The main research axes and strategies are reviewed trying to give the reader the feeling of the effort that developers are putting into solving the memory puzzle. Many trade-offs must be made, and the apparently endless chase between application requirements and device capability makes the path extremely difficult.

The last part of session three is devoted to some innovative applications that eNVM could actually boost. In these cases researches are trying to exploit the device drawbacks as actual advantages. A review of the main of these applications is provided, showing that even for this case challenges are not missing.

In session four a particular attention is posed on one of the emerging applications treated in session three. Neuromorphic applications are indeed of very high interest at the moment, and eNVMs are regarded with very high interest.

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We will explain why eNVMs are attracting so much interest in the neuromorphic domain, how they can bring some solution to the manufacturing of neural network, and how, at the same time, new challenges emerge for eNVM to meet the constraints of these applications.

Keywords

NVM · Emerging memory · Resistive memory · Phase change · MRAM · OxRAM · FeFET

17.1 Overcoming the Concept of Universal Memory

In the last years, or we may say last decade, a quite impressive amount of new memory candidates were presented to the scientific and industrial public. In this chapter we will focus on some of them, namely, Oxide-based Resistive RAM (OxRAM), PCM (phase change memory), STT-MRAM (spin-transfer torque magnetic RAM), and FeFET (ferroelectric field effect transistor). Many others were also invented and studied, like CBRAM (conductive bridge RAM), or Mott insulators, or Hybrid RAM (sometimes called HDDRAM). What characterizes all these technologies is what is generally referred to as the Gartner expectation, or "hype," cycle (see Fig. 17.1). Each new announcement of a new memory candidate (but this discussion can easily be extended to different technologies and even different industry at all) was always surrounded by an inflated aura of expectations. This is the beginning of such cycle. The "next" generation of memory is born, and it will be the so-much-longed-for "universal" memory. These statements are accompanied by extraordinary results, in terms of endurance or programming window or low power consumption and so on. Very soon however it appears that all these wonderful characteristics cannot be achieved at the same time and on the same wafer. The overestimated expectations quickly leave place to a much more reasonable and realistic set of characteristics that eventually converge to a real product. This is when the trade-offs are made, and it appears that a gain in endurance or in lower consumption is paid by a lower memory margin or a reduced retention.

A good example is described in [1] with PCM technology. PCMs were first announced almost 10 years ago with great emphasis [2], and these announcements were rapidly followed by a first set of products released by Numonyx

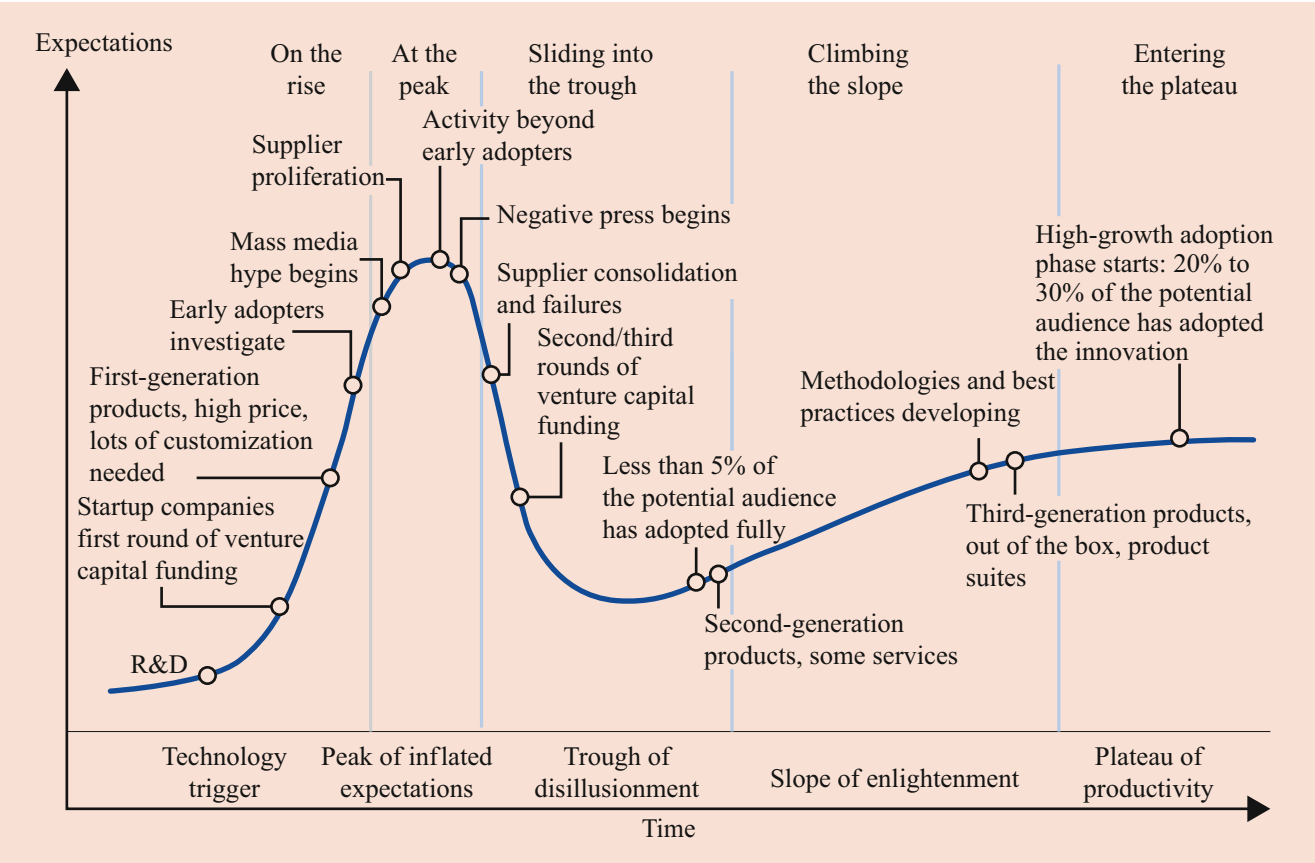


Fig. 17.1 Typical hype curve showing the main phases of appreciation of a new technology. (Figure from [113])

and Samsung. Although the new products guaranteed good sales at the beginning, Flash technology rapidly covered up the distance and reduced drastically PCM market. As a consequence PCMs were withdrawn as quickly as they appeared. Much more recently, and after a long absence of any new announcement, Intel/Micron proposed a completely new product series based on PCM for the storage class memory application [3]. We will come on this very topic later in this chapter.

When a general view is adopted to overview all the existing emerging memories, it appears that the same trade-offs are recurrent even when the physics behind each technology is very different. This kind of analysis was made by both Stanford University (see [4]) and Leti (see [1]). In these studies data coming from different emerging technologies were gathered together and compared in a cross-technology view. The result is that endurance, data retention performance, programming window, and energy consumption are linked by the same rules and appear to obey to a sort of universal law. This law describes the trade-offs that must be made on each technology to find the good compromise between different characteristics to enable a specific application. An explicative example is shown in Fig. 17.2. Here the reader can appreciate the bond that links together the programming window and the endurance performance of technologies that obey to very different switching mechanisms. Endurance always comes at the price of lower programming window. This is particularly true for filament-based memories, like CBRAM and OxRAM [5, 6]. In this case, as a filament is formed and disrupted multiple times, one can imagine that the large memory window that characterizes these devices means the displacement of a relatively large amount of material within the active layer. This is understandably linked to a reduction in endurance characteristic, as the active material is inevitably damaged cycle after cycle. At the opposite end, PCM involves local atom rearrangements in the mushroom region, with much lower net material transfer, and STT-MRAM only relies on spin transfer, with negligible atom rearrangement. Not surprisingly then, PCM features a better endurance with lower resistance window, and STT-MRAM has by far the best endurance at a price of very limited resistance margin. In a similar way, a clear trade-off between write time and endurance can be recognized. In Fig. 17.3 this is elucidated in the case of PCM technology. PCM shows a particularly good example since changing the exact composition of the chalcogenide material has been shown to effectively modify the device characteristics increasing or decreasing different aspects of the cell performance [7]. To improve data retention characteristics generally, materials with higher RESET stability are employed to counter the

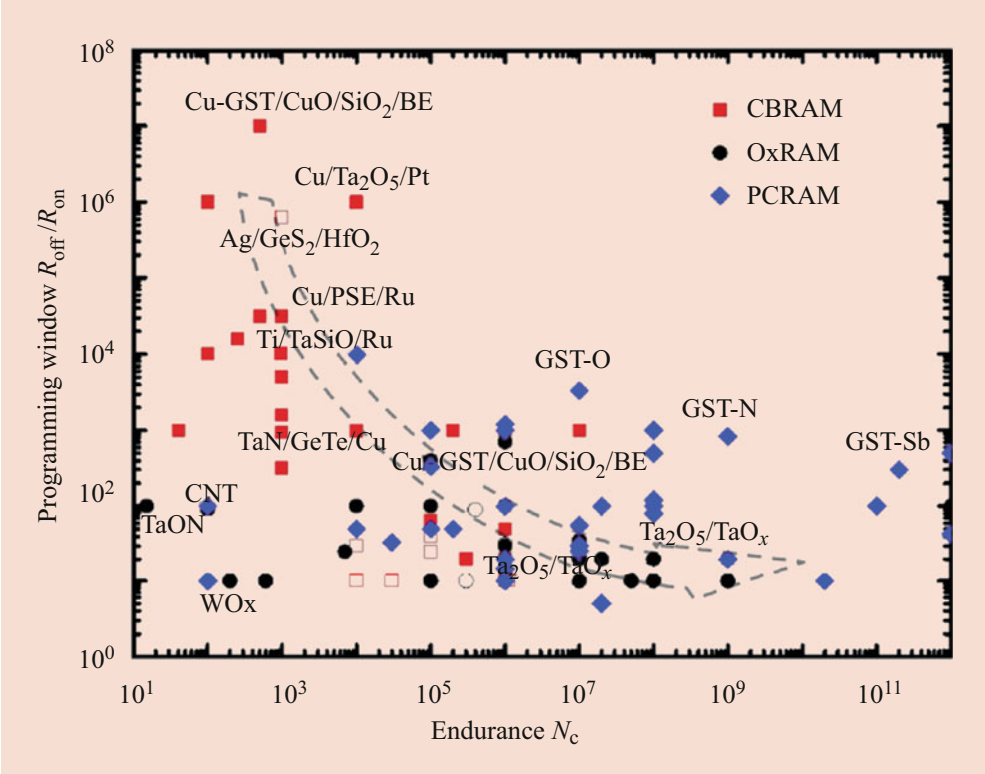


Fig. 17.2 Programming window as a function of endurance for many different emerging memory technologies showing a common cross-technology trend. (From [1])

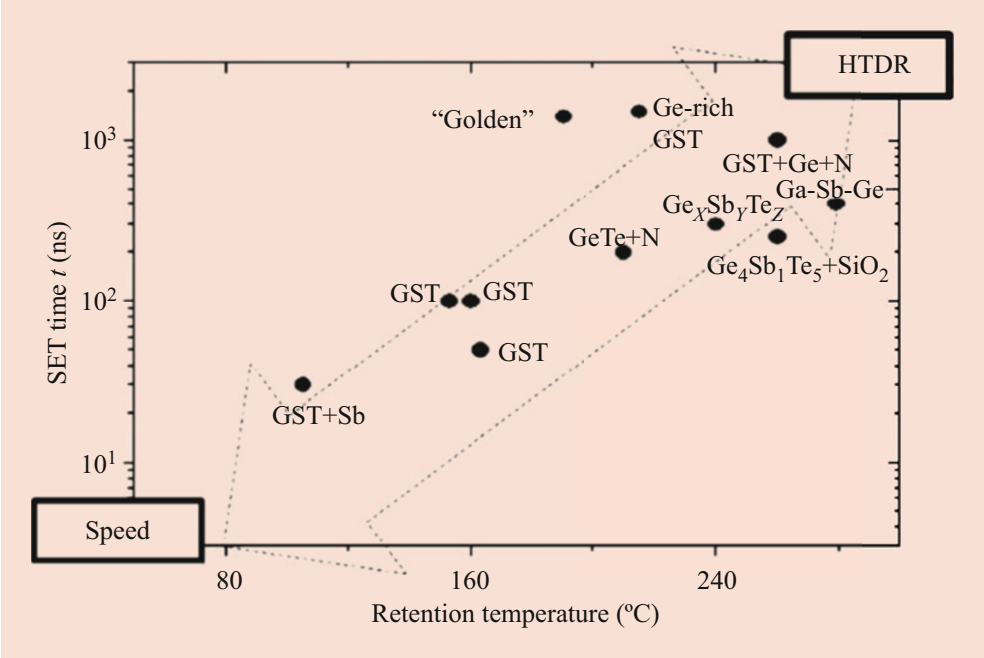


Fig. 17.3 Programming time vs retention temperature for different phase change materials. As speed can be linked to programming energy, the plot suggests that a trade-off between retention and programming energy is obviously to be found. (From [1])

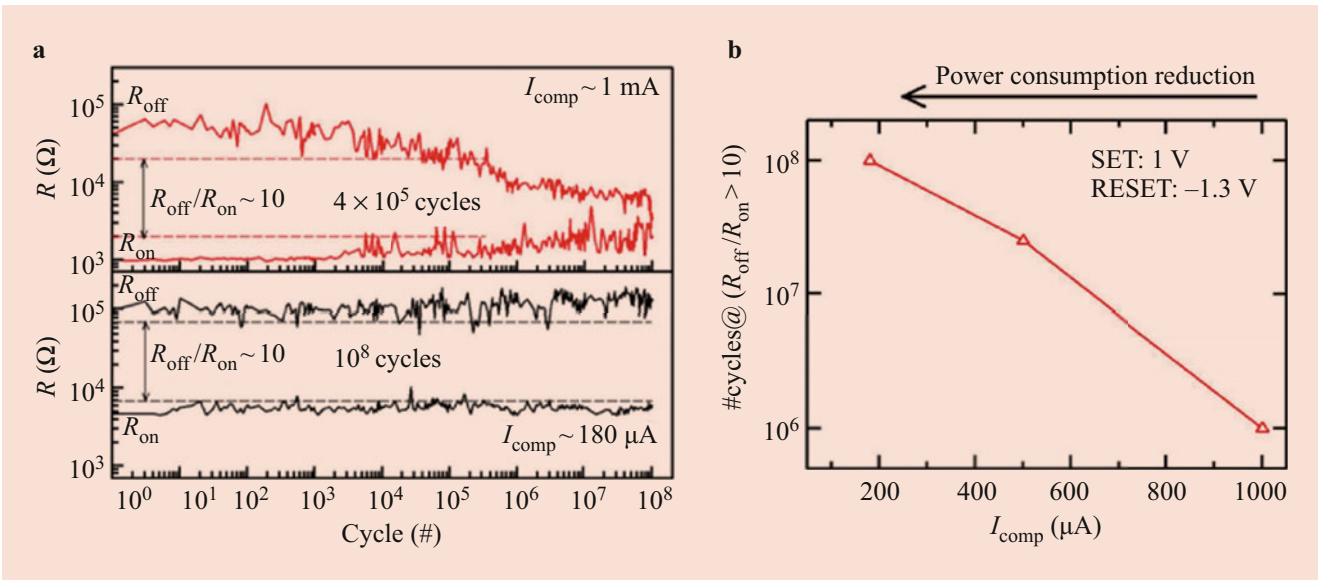


Fig. 17.4 (**a**) Endurance of HfO-based OxRAM; (**b**) endurance vs compliance current used for switching. (Figure from [1])

spontaneous recrystallization of the amorphous phase. This however typically leads to the need of a longer SET time to correctly achieve crystallization. In this sense, Fig. 17.3 shows that a better data retention means a worse endurance. It looks in fact understandable that a more stable RESET, which is necessary to achieve a more robust data retention of the amorphous state, calls for a longer SET pulse to recrystallize the active matrix and that this eventually causes a reduced endurance.

Another trade-off example can be found with HfO_2-based OxRAM where endurance is found to be function of the SET energy [1] as shown in Fig. 17.4a, b. A higher SET energy means a larger SET current (for a fixed program time) which leads to a larger filament and a wider memory window. Quite intuitively, a larger filament means a larger dielectric stress, hence a lower endurance. Understanding these trade-offs leads to the obvious conclusion that each technology must be tailored on the application and that it

looks unrealistic that a single technology would be the good one for very different applications. Some applications will require high endurance (like cache memory) and will need to accept a lower read margin, while others will demand high thermal stability (like embedded memory for code storage, in particular for automotive market) but will probably tolerate a reduced endurance. The main challenge is then to understand which specifications the targeted application requires and tailor the technology to meet these set of constraints.

In the following sections, we will first present the most interesting memory candidates, and we will compare them and analyze the challenge each of them is facing. Next we will focus on applications as the real developing driving force, and we will spend the last section on one of the most recent and demanding ones, the neuromorphic for advanced neural network.

17.2 "NVM Candidates"

In this section we will explore more in detail some of the technology candidates that the actual research is investigating on, among the quite wide NVM panorama. More in particular we will focus on four different flavors of emerging memories, which are by far the most investigated and most promising at the time of writing. We will mention also some other kinds of technologies that are more in an embryonal stage of development and are not quite ready to benchmark themselves on the memory field yet.

As it will be clear very soon, not all the memory technologies under investigation are at the same level of maturity; they are also based on completely different physics and face in general different problems in terms of integration, material, performances, and costs. What is however interesting is that all these technologies turn around the same quest of optimizing many performances at the same time. It should be clear by now that this task is not realistically attainable by any of these candidates, but it will be even clearer that each technology has different degrees of freedom to adapt to different applications. How each technology can adapt to application can make a big deal in which candidate will eventually become a real product, and we will try to show the advantages and weak points of each of them.

Thus in the rest of this section, we will focus on four types of memory candidates, namely, on OxRAM, PCRAM, MRAM, and FeFET which eventually we will shortly describe. First we will briefly recall the working principle of each of these technologies, and then we will show what their potential and weakest point are. We will leave to section three the important task of comparing them, and here we will instead focus on the challenges that each of these emerging technologies is facing with respect to integration, scalability, cost, performance, and readiness. It is almost impossible to cover entirely each aspect of these technologies, each of which could easily be the subject of the entire chapter, not to say of an entire book. However at the end of this section, the reader will have the understanding of the actual status of development for each technology.

17.2.1 OxRAM

OxRAM is a general term to indicate resistive memories that base their working principle on the formation and rupture of a tiny conductive filament shunting an otherwise insulating layer. In other terms, the OxRAM is any capacitor-like device where a dielectric layer is sandwiched between two conductive electrodes. The ability to generate a shunting filament and to restore an insulator layer by proper polarization constitutes the binary behavior that confers the device the memory ability.

OxRAM devices have been studied extensively since the late 1960s and were produced in countless variety and flavors. The number of publications and patents available at the time of writing ranges in the order of tens of thousands (see Fig. 17.5, for instance), and the hype about this promising technology is now starting to fade, as it appears that most of the performances achievable with OxRAM are not, at least not directly, linked to material properties but are rather intrinsic to the structure of the device. This concept will be clarified very soon in the section.

OxRAMs were produced using a large variety of materials. Some of the most studied are NiO_x, HfO_x, TiO_x, Ta_xO_y and perovskite compounds [9, 10]. Other materials were also reported to show resistance switching behaviors like porous Si [11], sulfides [12], chalcogenides [13], and even organic compounds [14]. The main aspects of OxRAM that determined the large research effort we saw are basically the low voltage operation (in the range of a few volts), the ease of integration, the low expected cost adder, and the good data retention performance. As a matter of fact, OxRAM has not yet demonstrated its potential in achieving a real product. This was mainly due to the large intrinsic variability that characterizes in particular the high resistance state (HRS) [15] in addition with other drawbacks that are very specific to OxRAM: the need of a forming process to initiate the resistive switching with a larger potential than the regular operating one, the relatively high current consumption (in the order of 1–100 μA; [16]), and the need of a selector to avoid sneak paths during read and write operations. Another point of attention is the need to reverse the polarity of the programming pulse to restore the HRS, which is a quite common characteristic to many different OxRAMs. This clearly imposes certain constraints on chip design.

Certainly one of the most studied materials for OxRAM has been HfO_2 which has showed good switching behavior

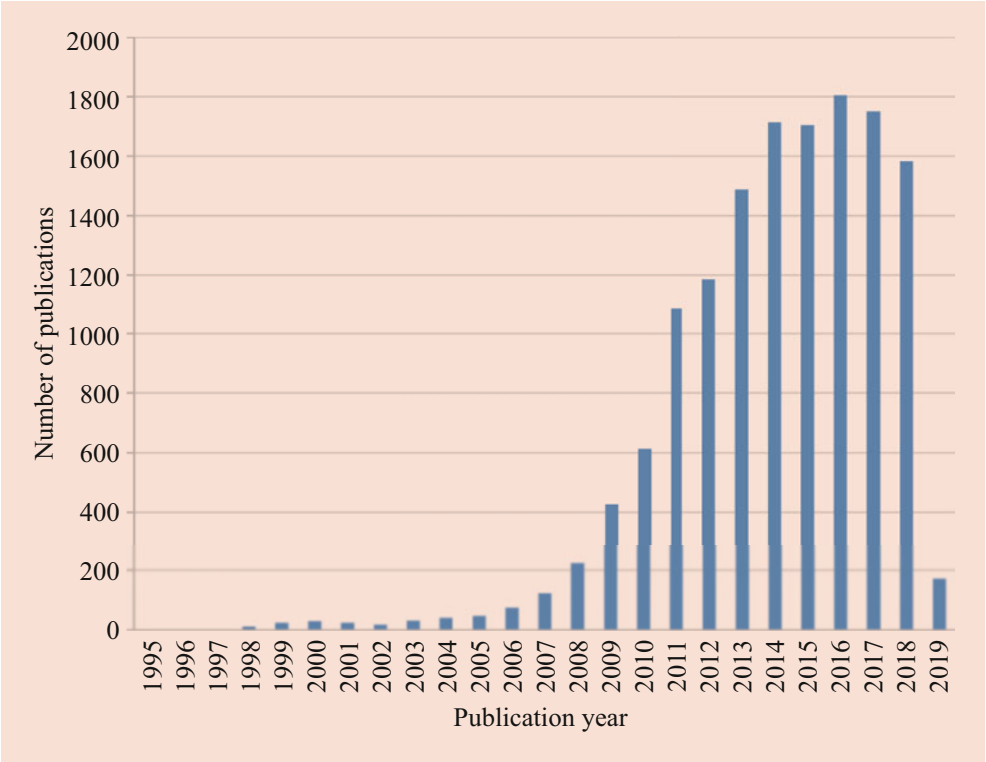


Fig. 17.5 Number of publications for "resistive switching" over the years. (Data from WebofScience [8])

when deposited in a sub-stoichiometric form leading to the presence of oxygen vacancies. HfO_2 deposition was achieved by both ALD and PVD techniques with similar results.

Oxygen vacancies (V_o) are believed to be responsible of the switching mechanism. One of the most accepted theories, even though so far a widely accepted theory is not yet available, proposes that the Vo act as attractive points for O atoms in the surrounding of the active material. O atoms are believed to take the form of negatively charged ions, and thus the electric field promotes the migration of O^- ions and their accumulation in the form of a conductive filament. When a counter polarization is applied, the ions are "pushed" back and forced to recombine at the electrodes causing the dissolution of the conductive path.

More recently, TaO_x [17] and $Ta_\mu O_\mu$ [18] have been investigated more in depth. It is not clear if the switching mechanism still relies on the same O ion migration or more on a local rearrangement of the crystal structure. However Ta-based material shows generally a lower resistance variability but at the same time a lower ration between HRS and LRS.

So far the largest demonstrator chip featuring OxRAM devices had a density of 32 Gb, manufactured in 24 nm technology node [19].

A slightly different flavor of OxRAM is known generally under the name of CBRAM (Conductive Bridge RAM). The main characteristic of CBRAM is the presence of a relatively stable oxide coupled with a reactive electrode. Ions from the electrode can easily migrate within the oxide matrix under the effect of the applied field. The oxide acts as solid electrolyte, while the reactive species are dissolved easily within it. Typical materials for the electrolyte include transition oxides (NiO, TaO, HfO_2), chalcogenides (GST), and silicon [20]. Applying the electric field causes the migration of the reactive species, which are most of the time silver or copper, and the shunting of the dielectric layer when a conductive bridge goes across the entire stack. Reverse polarization causes a back migration of the ions and the dissolution of the conductive bridge. OxRAM and CBRAM are thus extremely similar as both rely on filamentary conductions and obey to similar physics for many reliability aspects. It is noteworthy that while direct observation of the conductive filament in CBRAM was reported multiple times and unmistakably [21], the same is not as obvious for OxRAM, for which a direct observation of an oxygen depleted filament has been extremely difficult and yet de facto unachieved with results as convincing as for CBRAM. So far CBRAM demonstrators feature up to 16 Gb [22].

17.2.2 Phase Change Memory (PCM)

Phase change memories (PCMs) are probably one of the most studied emerging technologies for nonvolatile memories. They were and still are among the most promising

candidates for next-generation memory products. PCMs have in principle the same benefits of OxRAM and CBRAM in terms of low voltage operation, short programming times, and large ON/OFF ratio but are way less affected by intrinsic variability [7, 23, 24]. So far several demonstrators showed the potentials of this technology; in particular it is worth mentioning the results obtained by Numonyx [25] and Hynix [26] which presented a 1 Gb memory array. Samsung [27, 28] also has been very active on developing PCM and reported an 8GB memory array. PCM is seen as a relatively mature technology within the *plethora* of emerging memory devices, and such maturity is demonstrated by the actual presence on the consumer market of PCM products: memory chips in cell phones reported in [29, 30] which use indeed PCM devices.

The very first works on PCM are due to S. Ovshinsky [31] who published back in the 1960s the first results on $Ge_{10}Si_{12}As_{30}Te_{48}$ as a switching material. The physical principle on which PCM relies is the amorphous-crystal transition of a limited volume of phase change material which is thermally achieved. The key PCM features which enable the memory to function are the large difference in electric resistivity between crystal and amorphous phase, the relatively low melting temperature of the alloy, the high crystallization rate, and the good stability of both crystal and amorphous phases. These characteristics allow the PCM to be programmable with short voltage pulses and yet to retain their programmed state long enough to be considered nonvolatile.

The ternary system Ge-Sb-Te (GST) which is now so well-known was introduced later, in the 1980s, along with many different compositions based on the $GeTe/Sb_2Te_3$ group. These new materials allowed faster crystallization which was achievable with rapid pulses in the order of a few tens of nanoseconds [32]. The most known compound is however $Ge_2Sb_2Te_5$ (sometimes called simply 225) [24] which was introduced in the 1990s and had a specific application in optic disks. In that case the property exploited was the high optical contrast between the two stable phases which are achieved by thermal excitation through a laser pulse instead of an electrical stimulation. The step from the optical to the solid-state application was achieved trying to enhance endurance performances and to explore the potential of multilevel programming. [33] demonstrated at the end of the 1990s a very good endurance in the order of 10^{13} program/erase cycles and a relatively good multilevel capability. The main drawback of the 225 compound is however the thermal stability. As a matter of fact, the relatively poor stability at high temperature prevented so far the exploitation of PCM on the actual market. In particular automotive market requires 10 years' data retention at 150 °C which is hardly matched by PCM. Soldering reflow also constituted a problem for PCM, and partly still does, since for security applications data must be pre-coded within the array before reflow of the parts. In this case the thermal budget is 2 minutes at 260 °C. Other than thermal stability, the research focused and yet focuses on current reduction, which aims at cell scaling, and the acceleration of the crystallization phase, again to limit power consumption and cell wear. More recently good results on different GST flavors allowed PCM to gain performances in different directions, and slowly but steadily PCM improved its thermal stability and reduced current consumption. Different stoichiometries in the ternary GST compound as well as dopants were analyzed and proved successful as performance boosters. Still however many trade-offs must be found while choosing the good material. Sb-rich and above all Ge-rich alloys look now as the most promising for applications. Eventually it is worth mentioning the research in progress on different compounds, like GaSb-based materials [34].

17.2.3 MRAM

In the emerging memory panorama, a particular place is reserved to STT-MRAM which improved hugely the conventional MRAM device. In this chapter we will sometime refer to this newer device with the common name MRAM; however the reader must not be confused, as we will only focus on STT-MRAM technology. STT-MRAM implements a spin transfer torque principle which allows to scale the memory cell further and increases the overall device efficiency. The cell structure comes directly from the MRAM precursor, with two magnetic tunnel junctions (MTJ, the active cell part) sandwiched between two electrodes and separated by a 1–2-nm-thick insulation layer. The typical oxide material used as dielectric is MgO. STT-MRAM, just as MRAM, switches between a low and a high resistance state depending on the parallel or antiparallel orientation of the two magnetic layer. Several STT-MRAM products are currently available in various formats [35]. A crucial aspect of STT-MRAM products concerns the magnetic anisotropy [36]. While STT-MRAM with in-plane magnetic anisotropy are already available on market, devices implementing perpendicular anisotropy are still in development with the aim of achieving higher scaling. As we will discuss, scaling is indeed one of the hottest topics for MRAM.

From the performance perspective, MRAM appears as quite mature and really promising [43]. A fast write time (<10 ns) and long endurance (>10^7 cycles) were clearly demonstrated [37, 38], and sufficient data retention has been reported consistently [39]. Bit cell is currently quite large, mainly due to the presence, as for all other resistive devices, of a selector device (most of the times a NMOS). For this reason a possible MRAM application has been seen as SRAM replacement, where the large size of the memory point can be rewarded by the non-volatility of the component.

MRAM still faces difficult challenges. Probably the toughest is being linked to the materials used for MTJ

which are known to be difficult to etch and to clean after etching [40]. This translates in large overhead costs for dedicated machines. In addition, MRAM shows a very small ON/OFF resistance ratio. This means that resistance variability is critically relevant and requires well-designed sensing circuits [41]. This is particularly true in view of scaling the memory point. As density increases and array dimension too, variability is forecast to become a serious threat, and stronger research will be involved to unlock the scaling potential of the technology [41]. Overall, MRAM has various technology challenges to overcome. The manufacturing process is delicate as the device is sensitive to substrate smoothness and encapsulation materials and requires relatively high thermal budget which could have impact of front end. Researchers are spending a considerable effort to improve the technology tolerance and robustness by proper seed layer choice, specific deposition methods, and developing new capping materials. In addition engineers are experimenting with different MTJ recipes, including ferromagnetic multi-layers [42], sometimes interleaved with nonmagnetic metals, and newly developed dielectrics for the tunnel junction.

17.2.4 FeFET

Ferroelectric memories are known and have been studied for at least two decades. Typically the adopted materials are perovskite [44]. Many reasons left ferroelectric memories out of the spotlight, but the main is undoubtedly the excessive active layer thickness and the very difficult, although possible, CMOS compatibility in addition to gate leakage and depolarization [45]. In 2013 however ferroelectricity in Si-doped hafnium oxide was first reported [46], and this was certainly a game changer result. The possibility to exploit Si:HfO_2 gives a path to overcome the integration and scaling limits experienced so far by ferroelectric devices. This is due to the low permittivity along with high coercive field. In addition hafnia is a well-known material for integrators and thus opens the possibility to co-integrate front-end memory along with logic transistors. Different flavors of ferroelectric memory are thus available: a capacitor-like device, 1T1C, and, probably the most promising, 1T. The latter is typically referred to as FeFET. Its working principle, sketched in Fig. 17.6, relies on the polarization change within a ferroelectric Si:HfO_2 gate dielectric obtained by applying a threshold field across the gate stack. This polarization is reversible, by application of a similar field with opposite direction, and modifies the threshold voltage of the Si channel, pretty much as a typical Flash memory but without the need of a floating gate. At the time of writing, a FeFET technology demonstration for 22 nm and 28 nm HKMG was provided [47, 48], which gives interesting outlooks for future developments. The main advantages that FeFET could bring to NVM products would certainly be the a priori high scalability and the low programming voltage, in the range of 1–4 V, along with a very fast programming time (<1 ns) and extremely low programming current, given that during write/erase operations almost no current flows across the device. Moreover it is expected, and to some extent was shown, that FeFET has a remarkable thermal stability, which is one of the main requirements for eNVM. These characteristics would of course make easy for FeFET to find several applications, but as we saw with other eNVM concepts, there are drawbacks. FeFET suffers so far by a limited endurance performance. A typical FeFET leads

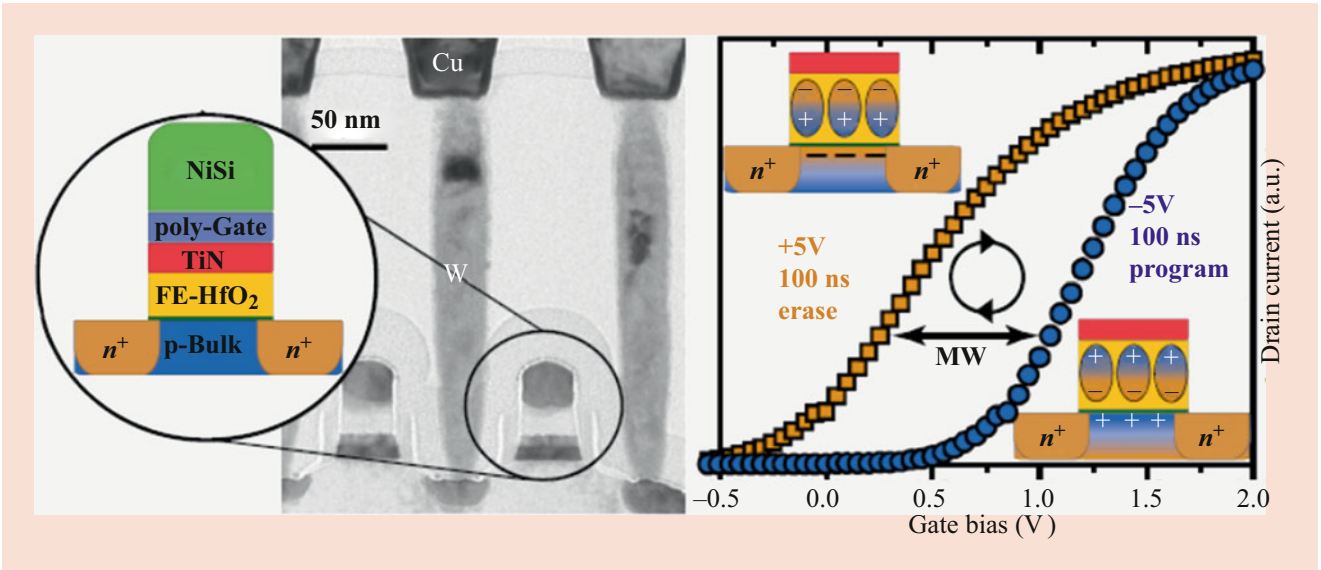


Fig. 17.6 Micrograph of a FeFET device and the typical IdVg curves of erased and programmed states. (From [46])

to 10^4 cycles, even though performances up to 10^7 were reported already in larger 1C (one capacitor) structures. This would still be better or at least comparable to a NAND Flash cell; however FeFET was reported to be read disturb prone, and NOR or AND arrays are therefore preferable for building arrays. Multiple additional metal lines and vias, plus additional access row and column selectors, would then be required, which in turn widely limits the competitiveness of FeFET with respect to NAND devices. Variability has also been shown to be of some issue for FeFET as the Si:HfO_2 ferroelectric crystal features grain sizes of the order of 10 nm. This impacts negatively on the device variability, mainly in terms of remnant polarization, and the problem is further enhanced by the different direction that the internal polarization field can take, leading to a more dispersed channel threshold voltage. Additionally, FeFET show strong trapping phenomena, which require dedicated programming sequence to actively de-trap electrons or holes before the cell can be correctly read [49, 50]. Research is tackling down this issue by specific epitaxial growth of the ferroelectric layer. Eventually, the memory window, defined as the difference between the threshold voltages of the FeFET after write or erase, was shown to be consistently in the order of 1 V, which, given the variability we evoked already, rules out the possibility to store more than 1 bit of information in a single cell.

17.3 How eNVMs Compare to Each Other

17.3.1 eNVMs Comparison

Many review papers compare eNVM together, and the typical table that results out of this quite challenging task is shown as example in Table 17.1 from Yu [51]. It is mandatory to warn the reader that, as the compared technologies are still in development, it is almost impossible to find absolute numbers that clearly explain the actual performance of the device under test. Most of the time, when new data are published, authors tend obviously to highlight the best performance of the DUT, but as we discussed already, many trade-offs are required for an actual memory device to work properly. This means that published tables report performances that are often achieved separately, while the same device is not capable to, for instance, achieve 10^8 cycles while be at the same time soldering reflow compliant and keeping the write potential below 2 V. For this reason, here we preferred to extract performance data consistently from the same chip when possible, but there is no certainty about the actual performance of the DUT. In fact the same device can be operated in different regimes to enhance one feature with respect to one other. For instance, increasing endurance is possible by lowering programming pulse voltage, which however is detrimental for memory margin and hence for array dimension.

Having said that it is undoubtedly possible, and necessary, to compare performances across eNVM data. In Table 17.2 (from [43]), a brief summary of the most important aspects of the eNVM we are focusing on is shown. We must notice that the only eNVM which truly differs in terms of structure is the FeFET, which is the only 1T device. This is of course a key feature for FeFET as it would allow, at least theoretically, to scale the memory device at the same rate of the logic transistor. Most of the other resistive devices are in fact bound to the selector size to be driven at sufficiently large current, while FeFET doesn't require high currents for programming just as a Flash memory. So far some data were provided in literature showing that co-integration of FeFET and 28 HKMG core logic is possible [47], but still quite few data are available to truly estimate the real potentials of FeFET. It is generally agreed that this technology needs research resources to investigate how it can compete with other emerging technologies. At the same time, FeFET is known to be prone to read disturbs and suffers of quite strong

Table 17.1 Table summarizing the main electrical parameters of different memory technologies

	Mainstream memories				Emerging memories		
			FLASH				
	SRAM	DRAM	NOR	NAND	STT-MRAM	PCRAM	RRAM
Cell area	>100 F^2	6 F^2	10 F^2	<4 F^2 (3D)	6 ~ 50 F^2	4 ~ 30 F^2	4 ~ 12 F^2
Multibit	1	1	2	3	1	2	2
Voltage	<1 V	<1 V	>10 V	>10 V	<1.5 V	<3 V	<3 V
Read time	~1 ns	~10 ns	~50 ns	~10 μs	<10 ns	<10 ns	<10 ns
Write time	~1 ns	~10 ns	10 μs–1 ms	100 μs–1 ms	<10 ns	~50 ns	<10 ns
Retention	N/A	~64 ms	>10 y	>10 y	>10 y	>10 y	>10 y
Endurance	>1E16	>1E16	>1E5	>1E4	>1E15	>1E9	>1E6~1E12
Write energy (J/bit)	~fJ	~10 fJ	~100 pJ	~10 fJ	~0.1 pJ	~10 pJ	~0.1 pJ

Data from (Yu 2016)

Notes: F: feature size of the lithography. The energy estimation is on the cell-level (not on the array-level). PCRAM and PRAM can achieve less than 4 qF^2 through 3D integration. The numbers of this table are representative (not the best of the worst cases)

Table 17.2 An over-simplified resume of advantages and challenges on emerging memory technologies

	Main advantages	Key challenges
FeFET	IT cell structure	Material and processing
	Low-power field-driven	FEOL integration
	High performance	Reliability and parasitic effects (e.g., charge trapping)
	Ferroelectric doped HfO_x	
PCM	Maturity	Reliability
	Proven performance	Disturbance
		High switching power
STT-MRAM	High performance	Reducing I_c/Δ (power-stability tradeoff)
	Well-understood physics	
	Novel mechanisms (*e.g.*, SHE, VCMA) to extend capabilities	MTJ patterning and etching
		BEOL thermal budget
RRAM	Simplicity and low cost	Reliability and failures
	High density	Stochastic mechanism and intrinsic variability
	Versatile materials, structures, and behaviors	Forming

From [43]

hole/electron trapping issues. The first problem generally calls for a more robust array structure, which is typically a AND array. This type of array allows each cell to be in parallel along each bitline instead of being in series as in NAND array. There is however a clear drawback in terms of scaling, but it is arguably the bottleneck of the FeFET. It looks in fact natural to compare FeFET with Flash, since both are front-end memories; however as emerging technology, FeFET is actually competing with BEOL memories. With this in mind, AND arrays are quite the obvious solution for resistive memories, since this is the only viable way to prevent sneaking paths during read operations. So the relatively larger AND array that FeFET must be implemented with is not a limiting factor. Still, this will become an issue if this technology was found to be performant enough to pursuit the scaling route. More on the scaling issue comes when dealing with the second problem we evoked: trapping. As a positive programming pulse is applied on the FeFET gate, electron trapping occurs, probably at the interface between the ferroelectric layer and the isolation layer above it [50]. This means that until electrons are actively or passively de-trapped, the device threshold voltage remains unchanged, since the screening effect of the negative charges conceals the internal coercive field. Active de-trap has costs in terms of programming time and energy, but at the moment it is required to allow a fast readout of the memory bit (necessary, for instance, if a program verify must be implemented). Another solution would be enlarging the memory window, which is of course always desirable. This impacts however the vertical scaling quite strongly. The memory window is in fact linked to the dielectric thickness at the first order by $MW = E_c \times t_{ox}$ (where E_c is the coercive field and t_{ox} the ferroelectric layer thickness) [52]. At time of writing, the typical MW is in the order of 1–2 V which looks already quite small if compared to charge trap devices. Vertical reduction of the ferroelectric layer looks thus difficult. In-plane scaling however is not an easier way to go. The ferroelectric HfO_2 has been reported to feature relatively large crystals of about 10 nm size [52]. This granularity immediately impacts the variability of the programmed threshold voltage. This happens in two ways. The first one is linked to the variability in coercive field specific to each grain. As grain size varies, each dielectric gate integrates a different number of grains of different size. This leads to a granularity in threshold voltage that was also reported to be seen in programming. In addition, grains can be oriented differently which means that the polarization field that each grain will apply on the channel is modulated by the cosine of the angle between the remnant field and the vertical z-axis. This causes a further variability in threshold voltage. Another critical aspect of FeFET development is linked to the relatively poor endurance that FeFET demonstrated so far. Typical endurance was reported between 10^4 and 10^6 [49, 53] which depending on the application, as we will further discuss, can be a serious issue. It is believed that the main degradation mechanism consists in the breakdown of the silicon oxide interface between the ferroelectric and the transistor channel. This implies that high endurance requires the silicon interface integrity to be kept during the cell life span. So far however it is not clear how this issue can be tackled while the main research axis points in the direction of decreasing grain size and increasing the coercive field. Another challenge FeFET will have to face is the possibility to be integrated in 3D structure as NAND Flash. This would allow to cope with some of the scaling issues we discussed and to propose a much larger application panel. However to demonstrate the feasibility of going 3D, the most difficult challenge would be the formation of a reliable silicon oxide interface between the ferroelectric hafnium oxide interposed between the two polysilicon structures that constitute the NAND cell series and the gate planes (see Fig. 17.7 [52]). So the 3D route requires major advancements in material development to achieve lower coercive fields and to improve the silicon interfaces. This will only be addressed once that the cell-to-cell disturb and the inhibit schemes required for writing patterns will be proven to be functional.

PCM memory is seen by many as the most mature technology among eNVM. We will show that quite a few demonstrators have been already made available on the market, and this means that most of the technical issues related to PCM have been solved or at least coped with. As we mentioned in the previous section, one of the major challenges that drives the

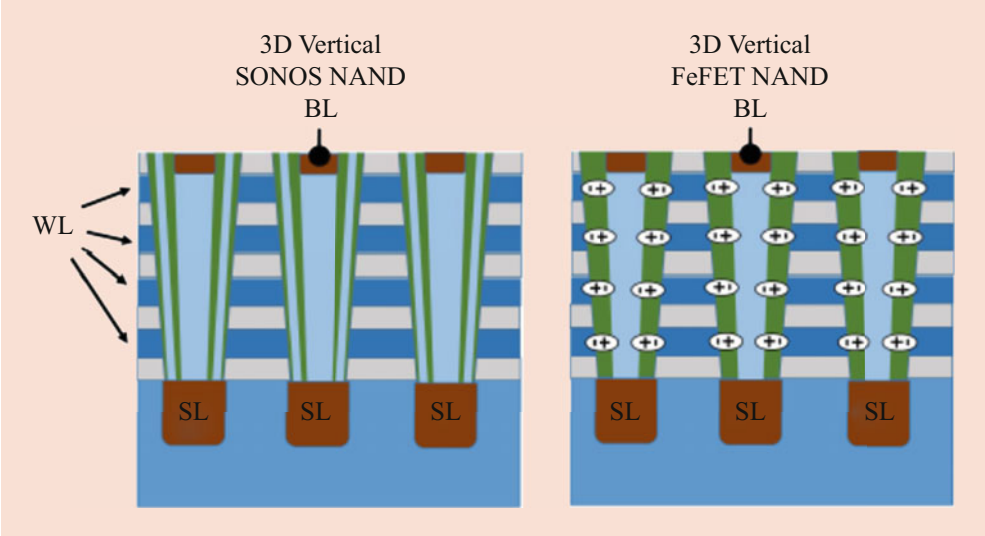


Fig. 17.7 Sketch of SONOS 3D VNAND compared with hypothetical vertical FeFET. (From [52])

development of PCM memories relates to the improvement of the stability of the programmed states. There are two main objectives concerning the thermal stability. The first one is the automotive specification, which is typically 10 years at 150 °C. The second one is probably even more stringent and relates to the pre-encoded data at wafer level. For some applications in fact, it is required that data are encoded on the memory chip before packaging and final board assembly. This is generally due to high security requirements. This however means that the chip will be subjected to additional thermal stress during board soldering reflow. The typical specification is 260 °C and between 2 and 5 minutes.

The stability of the SET and RESET states is very sensitive to the thermal environment of the device. The mechanisms that can compromise the programmed resistances are very well-known and documented and can be summarized in two main points. The first one is the crystallization of the amorphous material. When the amorphous rearranges its atoms, the electrical resistance of the memory bit programmed in RESET state tends to lower as the material becomes more and more crystalline. Eventually this can lead to a fail of the RESET state. A second mechanism of data loss is the structural relaxation of the material (both crystalline and amorphous phases contain imperfections that evolve with time) that causes an increase of electrical resistance. This phenomenon is typically known as resistance drift. RESET is obviously the cell state that is mostly affected by resistance drift as it is inherently disordered and each annealed defect translates into a lower electrical resistance that can be easily spotted in electrical tests. However drift is also observed in SET state, where the material is polycrystalline. Drift is attributed in this case to a structural relaxation of the amorphous residues that are known to exist within the crystalline phase. Grain boundaries are believed to play a role in the dynamics of the relaxation. The inevitable effect of the resistance drift is a fail of the SET state, as the electrical resistance increases gradually until the threshold resistance value is crossed. On the other side, this issue doesn't affect much the RESET state as a higher resistance is desirable but can still cause trouble if the memory is operated in a multilevel way. Research has spent so far a considerable amount of energy and efforts trying to solve both problems, and it is now quite clear that these issues cannot be solved at the same time. Indeed the two mechanisms are deeply linked and appear to be in competition. In [54], for instance, it is shown that materials that improve stability of the RESET state are prone to premature loss of SET state due to higher resistance drift. This eventually means that a trade-off must be found. This is clearly the biggest challenge for PCM.

The second main research axis, key to make PCM successful, is the current reduction during the program pulse. In particular the most current-demanding operating phase of a PCM cell is the RESET. The memory bit being low resistive calls a relatively large amount of current which is required to melt down the crystal material and to sustain the temperature before quenching. To achieve the current reduction task, multiple solutions have been proposed and are under discussion in literature. The first, and probably most obvious, solution would be a bit cell scaling down. A second strategy is the increase of the thermal efficiency of the memory bit by confining the melting heat. This would reduce the power loss allowing reduction of the reset current. A third and probably more difficult path would instead be the modification of the melting material. This approach would mean keep the cell structure and size identical while playing with the material properties. A first way in which the material properties could

be modified would be by lowering the melting temperature Tm of the compound [55]. In [56] instead, the possibility of increasing the electrical resistivity of the crystalline phase is proposed and found to be beneficial while increasing the power generated by the heat source. In [57] another strategy is proposed, consisting in doping the $Ge_2Sb_2Te_5$ matrix with SiO_2, which is found to decrease the reset current by modifying at the same time the thermal and electrical properties of the melting material. It is worth spending a few more words about the microscopic parameters that determine the programming current, in order to allow the reader to better understand the challenge. The main parameter that determines the current necessary for programming is the Joule heating effect that takes place within the phase change material. The power dissipated during the heat up has two contributions as explained, for instance, in [58]. The first one is given by the electrical resistance on the material when it is in the conductive state. This contribution is found to be ohmic. A second contribution is instead non-ohmic and comes from the so-called holding voltage (V_{hold}). These two contributions can be summarized as $P = V_{hold} \cdot I_{prog} + R_{on} \cdot {I_{prog}}^2$.

From this equation it is clear that a lower R_{on} or a higher V_{hold} will cause a higher power dissipation. Both these parameters can be modulated changing the material composition. The second parameter that impacts the current consumption is the heat dissipation during the RESET. This is well described, for instance, in [59] and is shortly summarized in the well-known heat equation (17.1)

$$\rho C_P \cdot \partial T/\partial t + (-k \cdot \mathrm{grad}(T)) = j2/\sigma. \tag{17.1}$$

This equation shows the obvious balance between the heat generation and the heat dissipation. For a RESET to happen, it is necessary that this equilibrium is reached with a temperature above the melting point of the PCM. In [60] it is well explained how modifying the material impacts the melting temperature and how this equilibrium shifts toward higher or lower current demand. Eventually a third effect must be taken into account. It has been reported [61] how the behavior of the material during the cooling phase can impact the programming current. This can indeed happen because if the phase change material features a high growth rate, a dome surrounding the molten mushroom could be recrystallized during the cooling phase. This means that the amorphous material will eventually result as a smaller portion than the actually molten dome. Eventually a larger dome will have to be melted down to achieve the desired amorphous volume, and this is done at the expense of additional programming current. In [61] it is reported how a reduction of Sb/Te ratio in PCM cells based on germanium doped SbTe can lead to a reduction of programming current via a lower growth rate.

MRAM has experienced an impressive progress in the last 5 years, and certainly the development of STT-MRAM devices has further accelerated the research to shorten as much as possible the time to market. We will see in the next session that many chips featuring STT-MRAM technology are currently commercially available. Even so, the magnetic memory still faces quite difficult challenges at the device level and at the circuit level as we already introduced in Sect. 17.2. Here we will focus more on some of these aspects: first the low ON/OFF resistance ratio, which requires extremely accurate and dedicated sensing circuit, and the high write current necessary to accomplish the programming phase of the memory bit. Not only the current is relatively high (typically in the order of a few hundreds of μA) but is also asymmetric between write and erase. Any process variation worsens the situation even further. The low ON/OFF ratio has a clear negative impact on the read latency as longer integration times are generally required. This causes a significant degradation in the memory overhead. In addition any process-induced variation within the reading logic will immediately impact the memory margin which is very small when compared to other emerging resistive RAM. This typically means even longer time for bit reading. As the write sequence is performed with a program/verify sequence, longer latencies on the reading side impact the overall memory latency, given by the sum of read and write latencies. To alleviate the poor ON/OFF ratio problem, various approaches have been proposed. In [62] a self-referencing scheme is proposed to reduce the read errors due to variations in ON and OFF resistances over the array. In a similar direction, in [63] an innovative inverse read is proposed which is proved to reduce read disturb and write power consumption. In [64] the authors investigate the optimization of the sense margin by combining a clamping transistor selector and a reference voltage bias. Eventually it was reported in [65] a reading method based on reference voltage, instead of a current, which proves to increase the sense margin when used to discriminate between ON and OFF states.

The second major challenge concerns the write current. This is a very well-known issue for STT-MRAM, as write current for these devices is high and asymmetric. This is due to the difference in polarization current, which is higher for one of the two logic states, and to the variation of charge current injection. To reduce write current, a new STT-MRAM flavor is under investigation, based on perpendicular magnetic anisotropy (PMA) [66–68]. More than that, a recent discovery of a large change of magnetic anisotropy in a Fe(001)/MgO(001) junction after applying small electric field showed a potential path to reduce current consumption in write procedure. This phenomenon is known as voltage controlled magnetic anisotropy (VCMA) [69]. Eventually we mention a giant spin Hall effect (SHE) reported, for instance, in [70, 71] found in some transition metals which could provide a new source of spin torque less energy demanding. Additionally it could provide a reliable way to separate

writing and reading electrical routes which is expected to positively impact on the device reliability.

OxRAM is still regarded as one of the most promising technologies among the eNVM panorama. We described in Sect. 17.2 some of the advantages of this device. Here we look more into detail to the challenges that this technology must endure before being successful as a real product. An excellent review on this topic can also be found in [9]. As it was already mentioned, the biggest challenge for OxRAM is the poor uniformity of the device electrical characteristics. A very large variation can be found in almost all the electrical parameters that characterize an OxRAM device. Large fluctuations exist in terms of HRS and LRS value and are both temporal (cycle-to-cycle) and spatial (die-to-die or cell-to-cell). Many works deal with the origin of these fluctuations which appear to be clearly intrinsic to the device. It is generally accepted that the stochasticity of the oxygen vacancies or of the ion diffusion is the root cause of the problem. This is discussed, for instance, in [15, 72].

It is quite clear that the variation in the resistance of the LRS (low resistance state) has to be attributed to the existence of conductive filaments of different sizes. Additionally, many report that this can be also caused by the existence of multiple conductive paths. So far, to reduce the variation of LRS distribution, two main routes have been explored: confining the filament in a narrow space and carefully controlling the current during writing process to freeze the formation of CF at a desired resistance value. However the main source of trouble with OxRAM is by far the high resistance state (HRS). In this case in fact, the variability can easily span over two to three decades since the microscopic mechanism that controls HRS is mainly tunneling across the small gap opened within the conductive filament during erase. Since the dependence between the gap dimension and the electrical resistance is exponential, any atomic-level variation within the gap translates into large resistance fluctuations. In addition to that, any defect (for instance, any oxygen vacancy) that remains within the gap can act as a bridge across it; eventually the conductive filament is the sum of many complex percolation paths. As the entropy linked to this situation is extremely high, so is the fluctuation observed. The clear conclusion is that the resistance variation is an intrinsic property of the OxRAM device and little can be done to reduce it. The most investigated approach to palliate this issue deals with the introduction of a capping or an interface layer to better control the interface between the oxide material and its most reactive electrode. In this direction Kim et al. proposed IrO_2 to replace the top electrode of NiO-based OxRAM [73], while several papers published results about TiN electrode buffered with thin Al layer for HfO_x-based OxRAMs [74]. A figure reproducing the remarkable improvement in set voltage distribution is proposed as Fig. 17.7. A second method widely investigated is the concentration of the electric field during set which should focus the conductive filament in a very narrow region. This causes the filament to be forced into the same shape at each cycle, reducing variability. To obtain this result multiple approaches were investigated. Most of them deals with reducing the cell size, as in this work by Lee et al. [75] who scaled the cell size down to 50 nm, or by this work by Fantini et al. where the cell size is as small as 10 nm [76]. This approach shows quite good result with improved set and reset distributions, even if the statistics under test are relatively small (in particular for the 10 nm device). Another research path consists in inserting seeds or extremely sharp edges to enhance the local electric field. In this direction Chang et al., in [77], showed results from TiO_x memory cells with embedded Pt nanocrystals. Similarly Liu et al. in [78] implanted Ti atoms within a ZrO_x matrix. Eventually a cell redesign was also proved to be beneficial at focusing the electric field, thus causing improvement in variability. For instance, Chang et al. in [79] introduced ZnO nanorods across the OxRAM stack in order for them to act as seed and to form filaments protruding out from them. Another example is given by Lee et al. in [75], where a crosspoint architecture is implemented with thin liner used as bottom electrode of a NiO-based device. All the abovementioned approaches showed clear improvements of the device characteristics; still the HRS distribution remains a limiting factor and major challenge for the technology.

Different approaches were also evaluated focusing on the "software" aspects of programmability. Complex program/verify schemes [80], redundancy, differential readings, and a large panel of preconditioning approaches were investigated. Once again, all these efforts although effective were not sufficient to entirely solve the intrinsic stochasticity of OxRAM technology (Fig. 17.8).

In order to summarize what has been described so far, Fig. 17.9 reproduces schematically the most relevant aspects of each technology along with their drawback or issues to be solved. As we saw STT-MRAM are probably the most advanced and promising in terms of performances, and a remarkable effort has been done so far in material and structure optimization. The main axis on which it is necessary to work is related to current reduction, scalability, and cost of manufacturing (see also Table 17.2). Even so, a first commercialization proved the real potential of the technology. A similar situation can be found for PCM, which is again a relatively mature technology with a well-established comprehension of the physical mechanisms of switching and reliability. PCM proved on the market to have a real potential and certainly can find applications. The main issue for PCM relates to thermal stability and power consumption, while good scalability and fast, reliable switching are the main advantages. FeFET is the only 1T device in the emerging NVM panorama. This is certainly its main advantage, since it could conjugate the scalability of a logic transistor with the

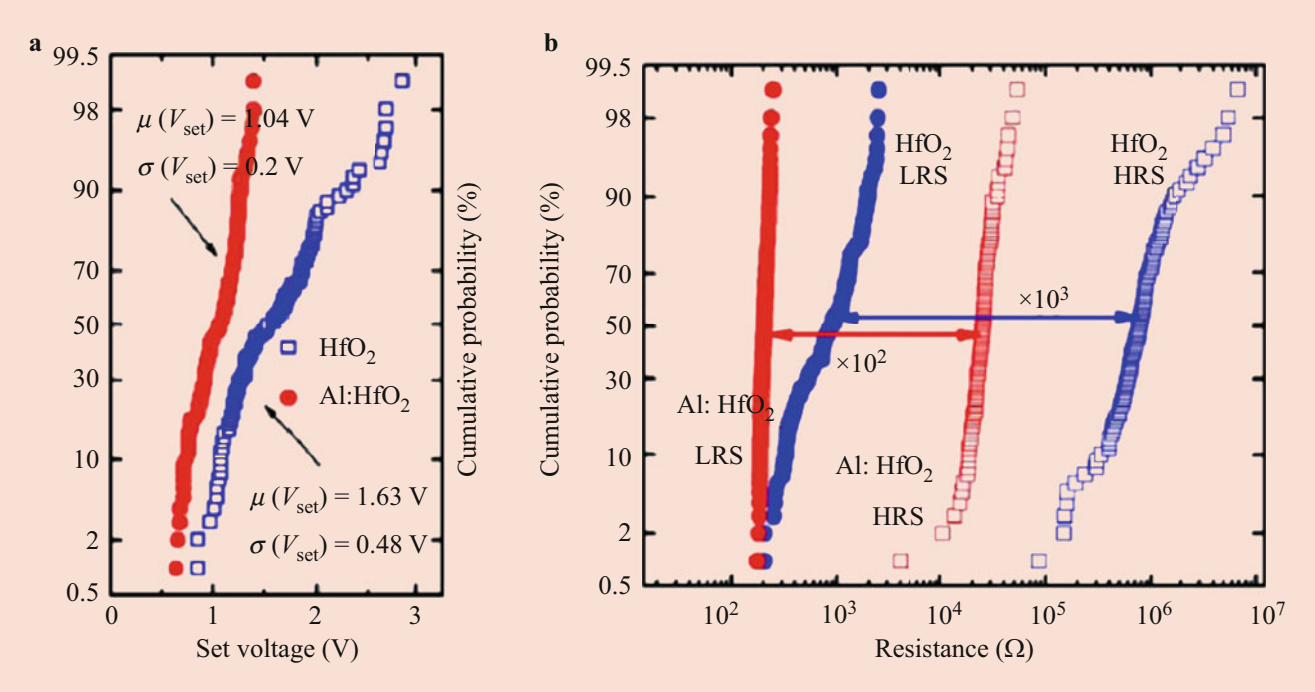


Fig. 17.8 (**a**) Set voltage distributions for HfO_2 and Al-doped HfO_2. (**b**) LRS and HRS resistance distributions. (From [74])

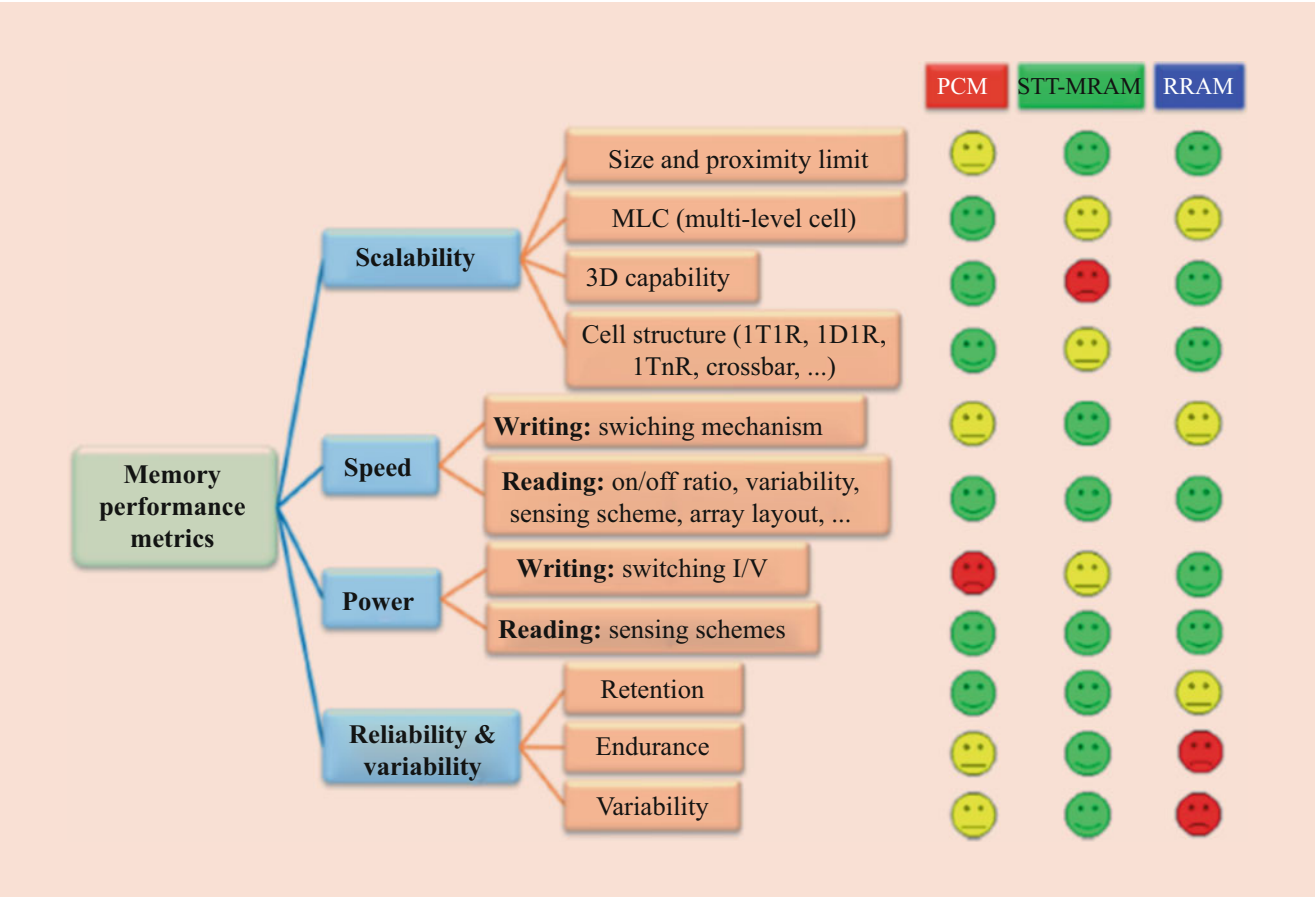


Fig. 17.9 Schematic representation of the main parameters for PCM, STT-MRAM, and RRAM. (From [43])

non-volatility of a resistive RAM. It is, we believe, still too early to understand the true potential of FeFET since much more research is still required. The main other advantages of this technology would be the high speed and a very low energy consumption, in addition to a very high CMOS compatibility. However, high variability, unknown thermal stability, and so far critical endurance are the challenges that FeFET has to face in the next years. It is sure that FeFET is among the emerging NVM the one that needs much more R&D efforts. Eventually OxRAM is probably the simplest device in terms of material and structure. It has been investigated extensively and it is still considered a good candidate for real products. OxRAM has a great advantage in terms of low cost impact, large ON/OFF ratio, and relatively low power consumption but suffers of high variability, which negatively impacts the reliability aspect of the device.

Figure 17.9 effectively summarizes the performance of each NVM described so far. These performances are classed following just four criteria. This is surely reductive as a memory technology must deal with a large number of trade-offs. Process difficulties, additional mask sets, and above all cost are however difficult to evaluate and are so far neglected. The chart classes OxRAM, PCM, and STT-MRAM based on scalability, speed, power consumption, and reliability. Each of these parameters is of course dependent on multiple aspects. Scalability is probably the most difficult aspect to evaluate. How scalable a memory cell is depends on the architecture, on the cell structure, on the selector device, and on the capability to stack 3D array or to use multilevel bits. It must be said however that all emerging NVM, except FeFET, are characterized by similar current consumption and by the need of a selector. This implies that the selector size is probably the most important aspect in determining the scalability of a memory technology. In addition, 3D stack seems to be very premature for any of these technologies and the same goes for the multilevel capability. So far in fact, no strong proof of multilevel programmability was provided on more than a few bits in literature for any of the considered candidates. The speed also depends on multiple factors. The main one is of course the writing mechanism. Although the technologies we considered are very different in terms of physical mechanism, they are relatively close in terms of writing speed. If, in addition, we benchmark these technologies with the typical speed of a Flash memory, it is clear that the memory writing time is not the bottleneck. PCM, FeFET, STT-MRAM, and OxRAM were all demonstrated to be faster than 10 ns on single bit, which is several orders of magnitude lower than a Flash memory (between hundreds of μs and ms). Differences exist however among them. FeFET is supposed to be writable in the ps range, and STT-MRAM can probably match them. OxRAMs were demonstrated writable in 1–10 ns, depending on the voltage applied. PCMs typically require slightly longer time, in particular to set the crystal phase, but newer compound was shown to crystallize in a very short time, in the order of 10 or a few tens of ns. A different situation can however apply for sensing operations. Evaluating the reading speed is quite difficult since it does not only depend on the memory cell itself but on the array architecture also. What is the level or parallelism on the array, how much current it is available for reading, and how large is the array are all parameters that influence the sensing time. Here however we focus on the device itself. The main parameter influencing, at the device level, the read time is the ON/OFF ratio. PCM and OxRAM have a quite large ON/OFF ratio, which makes the reading time possibly very low. STT-MRAM on the contrary are a bit of a challenge on this front, as we discussed previously. Eventually FeFET, since their principle is similar to Flash, have similar characteristics and feature fast reading times. The next parameter reported in the table is the power consumption. It is crucial to underline that power consumption should actually be divided into energy consumption and proper power usage. The first one, the energy, is probably the most important for applications that need to reduce the overall consumption, for instance, portable applications. The second one is instead more important for high performance applications as a high peak power consumption means larger power grids, higher thermal dissipation, and limitations in terms of parallel operations. As last point it must be noted that the energy consumption is the integral of the power absorbed over the time. In these terms, a PCM cell may require more current than a Flash cell but for a much shorter time. Eventually the overall energy required can be similar. Reliability includes many aspects like endurance, data retention, soldering reflow compliance, variability, RTN, read disturb, and others.

17.3.2 Most Relevant eNVM Demonstrators

While most of the research papers available in literature deal with single devices or small arrays, it is necessary to observe what is the actual industry development effort in emerging NVM technology. During the last decade, several demonstrators were proposed by different actors to the scientific and industrial public. Figure 17.10 (adapted from [43]) summarizes some of the most relevant memory chips proposed as technology demonstrators. This plot focuses on PCM, STT-MRAM, and OxRAM. All data reported were published on conferences, and refer to functional arrays which can be considered representative of a real product, although in an early stage of prototyping. In the figure the size of the symbol is meant to be proportional to the technology node used to build the CMOS circuitry of the demonstrator. Each symbol is labelled with the company name, array size, used

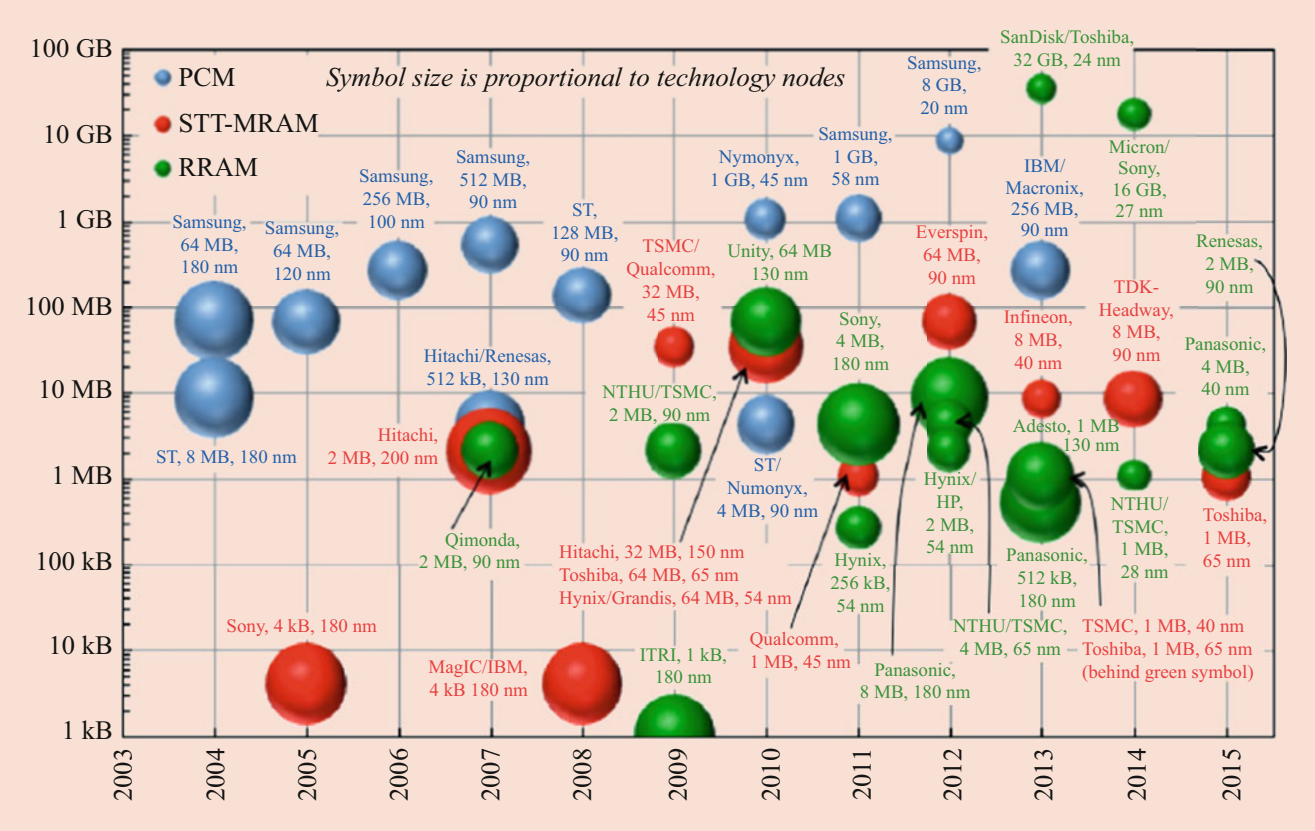


Fig. 17.10 Representation of the fabricated devices over the years based on density and technological node. (From [43])

process, and technology node. Many interesting observations can be made based on these data. The reader will notice that PCM (blue symbols) shows quite a clear trend over the years, with two main actors, Samsung and ST (and its former spin-off Numonyx), proposing increasingly larger memory chips. Also, it appears that PCM technology was the first to achieve a demonstrator stage among the three. The largest PCM array was 8 Gb by Samsung in 20 nm node. Another interesting observation is that STT-MRAM (red symbols) features generally smaller array size compared to PCM. This is due to the different applications STT-MRAM aims at. This device is generally intended for high performance and low size applications (for instance, automotive μC), instead of being oriented to high-density memory. The lowest CMOS technology node used to embed STT-MRAM was in fact 40 nm (by TCMS 1 Mb size). Eventually OxRAM shows very dispersed and inconsistent development path, as different actors aimed at different applications, ranging from μC to neuromorphic to stand-alone. At the same time, it is quite remarkable that so many demonstrators saw the light in a very limited time. Between 2012 and 2015, as many as 11 different test chips were built, showing the high interest that OxRAM attracted in the industry.

17.3.3 Innovative Applications

So far we saw how eNVMs have a wide range of interesting characteristics that drive high interest both in academy and industry. Clearly, new memory devices with innovative aspects with respect to existing technologies open new roads for new applications. In this section we will explore what kind of applications can be envisaged or could be made possible by adopting eNVMs. We discussed the most relevant aspect that characterizes each technology considered so far. For instance, STT-MRAM features a very high speed, while OxRAM is very stable and can sustain high thermal budget. Each eNVM could then ideally be more suited for a specific application based on this description; however as we mentioned in Sect. 17.1, trade-offs are always necessary to enable a specific application, and the success of a technology can only come when several constraints are satisfied at the same time.

The first, quite obvious application that justifies the research of a new memory device is the improvement of the actual products. If we consider, for instance, stand-alone memories (in other words NAND Flash), the typical low voltage operating range of eNVM looks extremely promising since it would remove the requirement of charge pumps

which decrease the array efficiency. At the same time, the high speed typical of eNVM would represent an obvious improvement with respect to Flash. At the end all these aspects represent a cost improvement, which is essentially the driving aspect of NAND Flash. The same reasoning can be applied to SRAM or DRAM, which could in principle be replaced by STT-MRAM or OxRAM, as the first one is characterized by very high speed while the second one is supposed to be very scalable and cheap at production. However the production requirements, the standardization of several products, the needs of the current business, and the justified precaution of customers used since years to a well-established technology represent a high barrier that prevents the adoption of any new device. Two main situations can lead to overcome this barrier. First is a clear and net cost improvement. This scenario is quite unlikely to happen since cost reduction is the result of years of optimizations driven by large demand. Flash technology scales its cost impressively fast and it looks unrealistic that an emerging technology could compete on that. The second situation is related to better performances or entirely new features. The most probable scenario that would lead to the adoption of eNVM is much closer to this one. Emerging memory could compete on performances beyond Flash capabilities – high write speeds, longer endurance, and so on. OxRAM was also demonstrated as a possible solution for flexible and organic electronics. Another sector in which eNVM could penetrate the market is represented by OTP (one time programmable) replacement. OTP, as well as 1T NOR Flash, are often used for code storage in micro-controllers in many different applications. eNVM would bring at lower cost the benefit of re-writability. This is in general true for any embedded application, where standard NVM has difficulties to scale at the most advanced nodes. For instance, Flash technology is hardly achievable below 28 nm, while PCM was demonstrated already at 20 and FeFET at 22 nm. For this purpose however, eNVMs have to show a much improved reliability to become a real solution for embedded applications. In particular automotive market requires very stringent thermal stability and an extremely low defect level. Still many other eNVM characteristics have to be improved before any of the discussed technologies could realistically be embedded.

A second, probably more interesting, domain of applicability of eNVM would be the so-called storage class memory (SCM). The reader may be already familiar with the concept of "memory gap." This term refers to the large difference mainly in terms of speed that can be observed in the current memory hierarchy in computer architecture. The memory close to the CPU is typically SRAM, with access time in the order of ns. DRAM follows with access time in the order of tens of ns, used to catch data and buffer between storage and cache memory. However between DRAM and hard drives, a large gap in speed exists, as the HD works in the ms access time range. Figure 17.11 shows graphically this large gap of

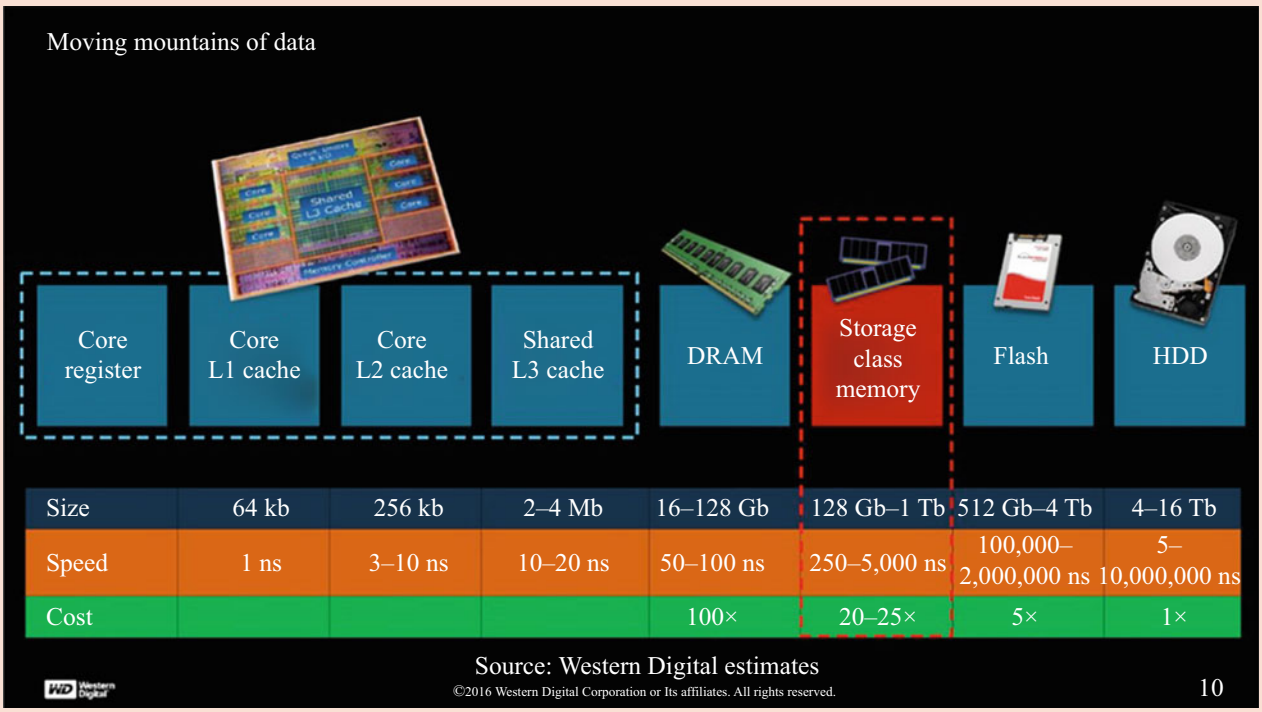


Fig. 17.11 Memory hierarchy. (From [81])

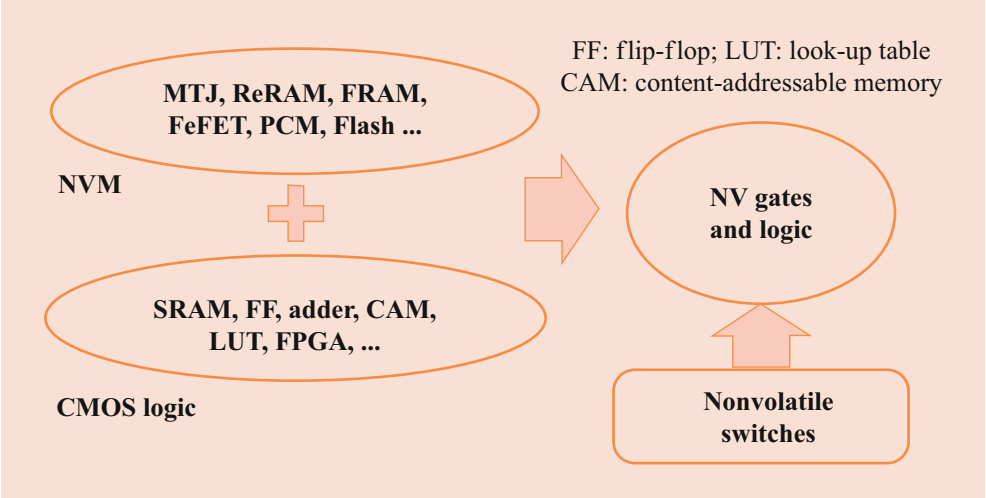


Fig. 17.12 Possible memory implementation for computation. (From [43])

more than three orders of magnitude. The development of NAND Flash as storage memory in SSD drives alleviated this large gap and showed the interest for bridging the leap. A "universal memory" that would have the speed of a DRAM, the non-volatility of a Flash, and the price of a magnetic disk looks extremely attractive but, as we discussed in Sect. 17.1, seems also unrealistic. However, in 2017 the introduction by Intel and Micron of a crossbar resistive memory (with the commercial name of Optane) based on PCM on the consumer market opened and showed the new path. It is still early to assess if commercially this can be considered a success or not, but the electrical behavior of this device indeed boosts the HD performance.

Another potential application that has been scrutinized and could be a market opener for eNVM is the very-low-power application. This class of devices includes those chips that spend most of their lifetime into an off, sleep mode. They only turn on for a short period of time when a trigger event signals the need of an operation. Most devices, while on standby, still consume a relatively high amount of energy, and a significant part of it is used to refresh volatile memory. SRAM cannot be turned off without loss of data, unless, before power down, data are transferred to a nonvolatile support. This has two major disadvantages. First, the data transfer and data writing can take a long time, in the order of tens of ms in the worst cases. In addition, when the trigger is received and the device turns on again, data have to be reverted and SRAM reactivated, causing an additional delay time. Internet of things (IoT) is probably the best example where these devices are required, since power consumption is the main issue. Flash is not a good choice as dumping memory, since its high writing voltage is a big hindrance in low consumption applications and very low-cost devices. For this reason eNVM can be considered as a good candidate as dumping support. Not only eNVM could be used to store SRAM data before standby, but it could also, provided a very good endurance, completely replace SRAM itself. In this case the device could get a high speed, close to actual SRAM but in conjunction with the non-volatility character of eNVM. STT-RAM seems the most appropriate for this scenario, as it can be considered as best performing eNVM currently available in terms of speed and endurance. STT-RAM however has a quite high ON power consumption, and its use can be justifiable only if the saved energy during standby is by far larger than the extra consumption during the ON stage [82].

Many papers also suggest the use of eNVM in the so-called in-memory computing (IMC) approach, where memory bits storing data to be processed are integrated very close to the logic gates that actually process them [83]. By mixing eNVM and logic components, for instance, mixing OxRAM and adders or look-up tables or other logic ports, it is possible to obtain a computational unit with a built-in memory that allows to process data into a nonvolatile environment. This is represented in Fig. 17.12. Some eNVMs look in principle very adapted to this application, for instance, FeFET as it can operate as both a "normal" logic component and as a nonvolatile bit. The use of this kind of architecture, if proved functional, could revolutionize entirely the computing architecture and would benefit of increased speed and reduced power consumption as data transfer would be greatly improved. However the robustness of eNVM has to be quite as high as the logic component, since the memory bits would be used at least as frequently as a classical logic gate, both in reading and in writing mode. Reliability again looks as the biggest constraint.

So far we discussed some applications where eNVM could be preferable with respect to actual technology, and in the last example, we also discussed a potential new application in rupture with the current technology. Some additional ex-

amples must be mentioned where eNVM could have a role as electrical component where the researched characteristic is not its non-volatility but its intrinsic variability or its capability to gradually change its resistance from two or multiple states. The first one is the neuromorphic applications. The interest into this field has been driven by the boost in performance and applications of machine learning (ML). This boost is the result of two main components: on one side the huge amount of data stored in the internet, mainly composed of images, video, music, and text, which can now be used to train artificial intelligence, and, on the other side, the high computational power at our disposal with the advent of parallel computing in conjunction with the ultimate CMOS scaling close to and below 10nm node. At present time, the ability of artificial intelligence in certain tasks, once unique domain of human brain, like image recognition or natural language comprehension has equaled or sometimes surpassed man's ability. The potentials for AI use are endless, from advanced translators to self-driving cars. As we will discuss more in detail in the next section, the limiting factor at developing neuromorphic structure is the difficulties to mimic the actual behavior of a synapse and a neuron. A recent trend in neuromorphic computing is to encode the neuron state into pulses or spikes [84–86], and the information carried over the neural network is represented by the cumulative effect of spikes over time. So far several large-scale neuromorphic systems have been studied and proposed based on the actual silicon technologies. Some examples are Heidelberg's HICANN [87], IMB's TrueNorth [88, 89], or ETH's ROLLS [90] chips. In these examples the neural weight is stored in capacitors or in SRAM cells. Therefore area consumption, energy consumption, and memory volatility are limiting factors. Emerging NVMs are thus considered as very promising candidates to implement synapses thanks to their capabilities to change gradually their resistance, or to switch after a cumulative amount of spikes. This is particularly true for OxRAMs, PCM, and CBRAMs. In addition to this unique feature, the reduced area and power consumption make eNVM ideal for neuromorphic applications. The high variability that characterizes OxRAM could even be considered an advantage in this context as it could promote additional connections in the neural network useful to explore different connection schemes. Even though OxRAM and PCM look so suitable for these applications, actual demonstration of feasibility is limited [91]. The possibility to modulate in a controllable way the resistance of the memory bit has to be improved, and the general asymmetry between write and erase (for instance, SET and RESET in OxRAM are very different) still poses some challenges to easily modulate the reinforcing and depressing learning phases.

In this last section, we discuss some additional explorative applications that are getting more and more attention in recent years. As we saw so far, there are many aspects of eNVM that are unwanted for memory applications. These include resistance variability, switching voltage variability, random telegraph signal noise, and resistance drift, to cite the most important. However for the applications we are about to discuss, these characteristics are actually of interest. These applications in fact profit from the typical stochasticity of most eNVM behavior (mostly OxRAM and CBRAM) to enable some applications in security hardware. In particular we focus on true random number generator (TRNG) and physical unclonable function (PUF).

TRNG are devices that generate a random bit sequence that complies with some requirements that guarantee the actual randomness of the bit stream. The first requirement demands that the bit stream has approximately the same probability to produce "1" as to produce "0." Devices like OxRAM are known to obey to the so-called "time-voltage" dilemma. This means that the probability to switch a cell is a function of both electrical bias and pulse length. If the programming pulses are correctly tuned, the memory cell can work in a range in which the probability to obtain one state or its complementary is equal. This feature enables the generation of true random number streams as demonstrated experimentally in some reports [92–94]. There are two main approaches to exploit eNVM for generating random bit streams. One possibility is to use the variation of write potential, in which the "0" and "1" are produced randomly because the write pulse is close to the switching potential threshold, so that the cycle-to-cycle variation causes the threshold to be higher or lower than the applied potential. The other possibility is to use the variation of the off state which is widely spread in filamentary eNVM. In this case a resistance threshold is carefully placed within the off resistance distribution of the device. As cycle after cycle the off resistance will change, the bit will be read alternatively as a "0" or as a "1." A less explored approach uses instead the signal telegram noise that characterizes the off state of many filament-based eNVM to trigger a random bit sequence [95].

The last application we discuss is PUF. A PUF is a security device that exploits the physical randomness generally linked to uncontrollable process variations to generate a unique, unclonable, stable "fingerprint" of a given chip. PUF must meet stringent specification in order to be implemented as actual source of chip identification. In particular there are three main parameters that quantify the PUF's quality. These parameters are the bias to judge the uniformity of "0" and "1" in the PUF responses, the inter-chip Hamming distance, which tests the uniqueness of the PUF, and the intra-chip Hamming distance which tests the reliability of the device. Using eNVM as PUF means to utilize the intrinsic variation of switching potential as a source of randomness [96–98]. One example is provided in Fig. 17.13a, b. A 1T1R OxRAM array is "challenged" providing two n-bit addresses, and the "response" is given by comparing the bits by pairs,

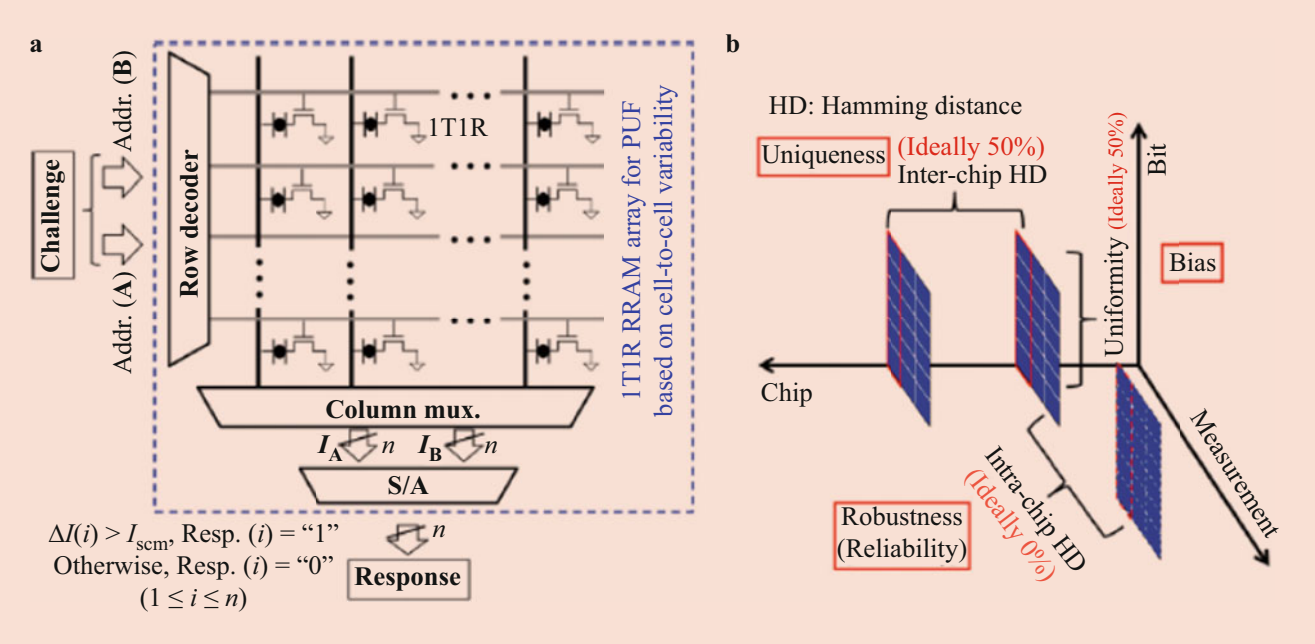


Fig. 17.13 (**a**) Schematic of a PUF based on a 1T1R resistive array. (**b**) Scheme representing how PUF quality is established. (From [96])

which generates an *n*-bit-long word. The randomness and the unclonability are provided here by the intrinsic cell-to-cell variation. OxRAM can present an advantage in PUF design as it allows smaller and less energy-consuming PUFs. Figure 17.13b shows how the PUF quality is established. An equal number of "0" and "1" is to be expected, meaning 50% probability to generate either "0" or "1"; when presented with the same challenge, two distinct PUFs must provide different responses; and when presented multiple times with the same challenge, one PUF must provide always the same response.

For eNVM to function as PUF, some aspects must be considered. The nonideal behavior of filament-based eNVM can be a limiting factor. In particular data retention, thermal instability and read disturb (like RTN, or cell-to-cell cross-talk) can cause the PUF to degrade. PCM and STT-MRAM were also studied as possible PUF devices [99, 100].

17.4 eNVM for Neuromorphic Applications

In this section we describe into more details some aspects of the neuromorphic applications for eNVM. This field is currently one of the strongest drivers of eNVM development, and thus it is relevant for the reader to get some concepts and to understand the main challenges that eNVM must face to enable new neuromorphic features.

As we discussed earlier, quite a few neuromorphic systems have been recently proposed based on silicon technologies. In this case [87–90], SRAM, capacitors, or other standard CMOS components were used to emulate at the same time neurons and synapses. The limitations with this approach are generally the volatility of the neural network and the large area required. Emerging NVM are in this case of great interest for their non-volatility, scaled dimensions, and the possibility to modulate their resistance. In the following part, we propose a short review.

The first example shows the use of eNVM – OxRAM more precisely – for convolutional neural networks (CNN) with supervised learning. CNN are inspired by the structure of the visual systems in mammals [101, 102] and are regarded as very interesting mainly for their relatively small memory footprint. Some significant proof of concepts were provided with software simulations with success in several fields, like the analysis of biological sample images [103], visage detection, optical character recognition (OCR), and human detection in pictures [104–106]. Some on-silicon demonstrators are also available, but, as the computational resources required are extremely high, dedicated SoC are generally used, where FPGAs are optimized to reduce the computational requirements and increase the power efficiency. In [107] an HfO_2-based OxRAM is used as synapses for convolution kernels. This device implements a spike architecture for pattern recognition. The advantage brought by OxRAM is to allow the in-memory computation which is highly time-efficient, leading to lower latency times in pattern analysis when compared to a GPU-based implementation. As can be seen in Fig. 17.14, the CNN architecture is composed of two cascaded convolutional layers (the extraction module) and two fully connected layers (the extraction module). The difference between the two structures is the amount of connections existing between

the layers. In fully connected modules, a large amount of synapses are used to connect every neuron of one layer to every neuron of the next one. Differently, in convolutional networks, a small amount of synapses are shared between the layers reducing the total number of synapses required. The convolutional layer presents several output feature maps. These are connected via the convolutional kernel to some or all the feature maps of the previous layer. The aim of the extraction module is to transform the input image into a feature map, and transferring data from one layer to the next,

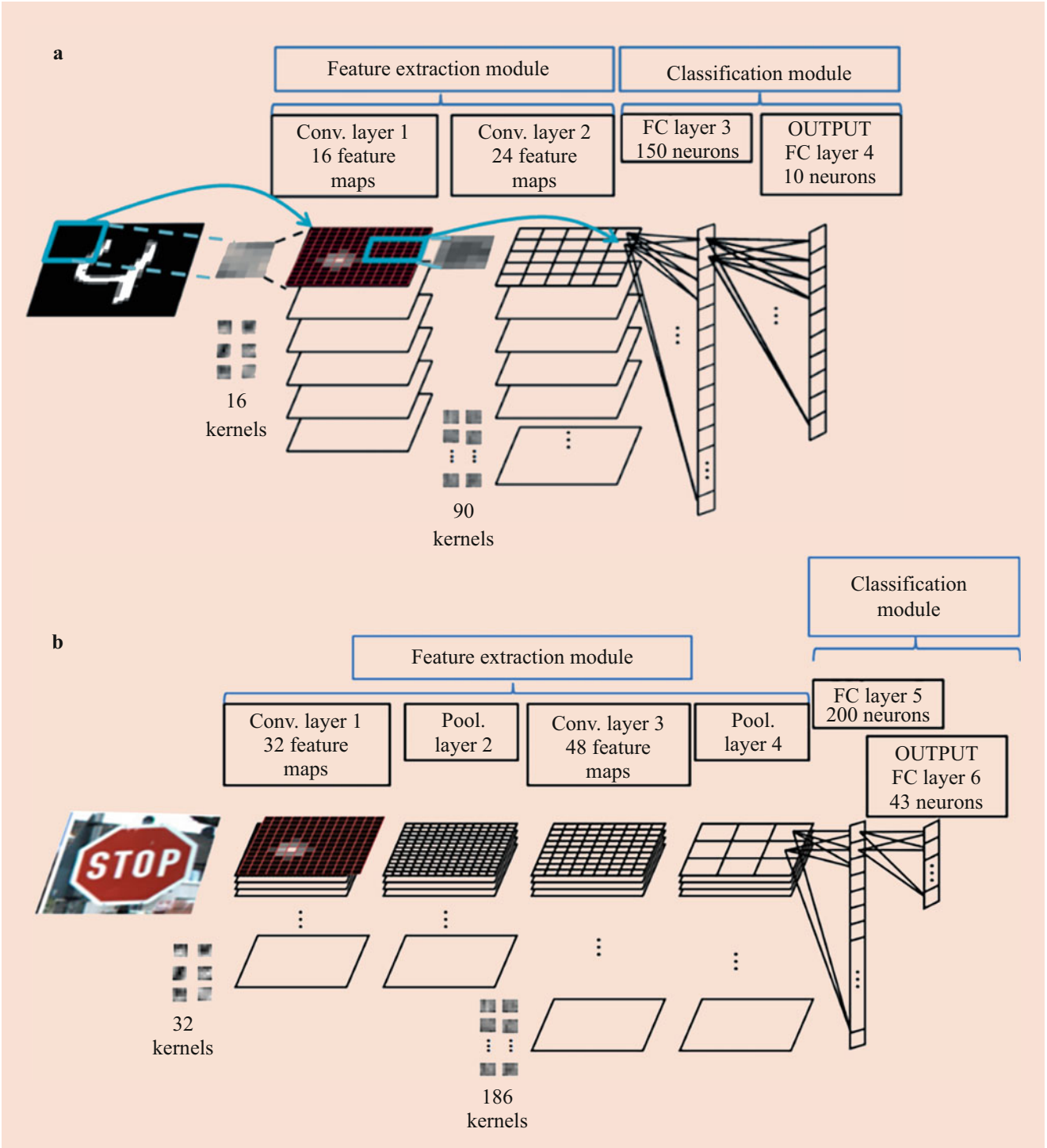


Fig. 17.14 Convolutional neural networks architecture for MNIST database (**a**) and GTSRB database (**b**). The second convolutional layer has each output feature map connected to some only of the input features of the successive maps. (From [107])

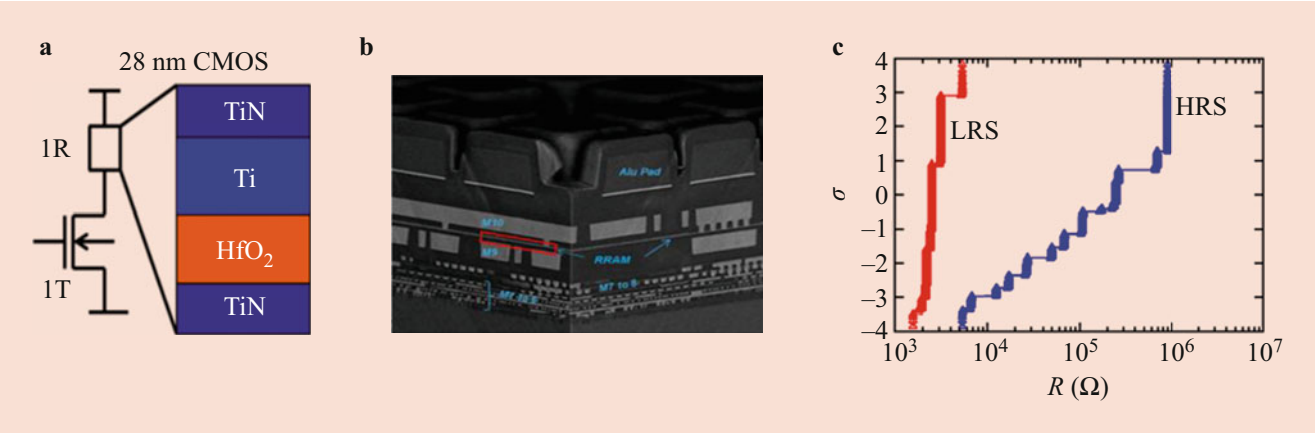


Fig. 17.15 A parallel of 1T1R devices (scheme in (**a**) and SEM image in (**b**)) is taken to build synapses, based on the LRS and HRS distributions of a single device (**c**). (From [108])

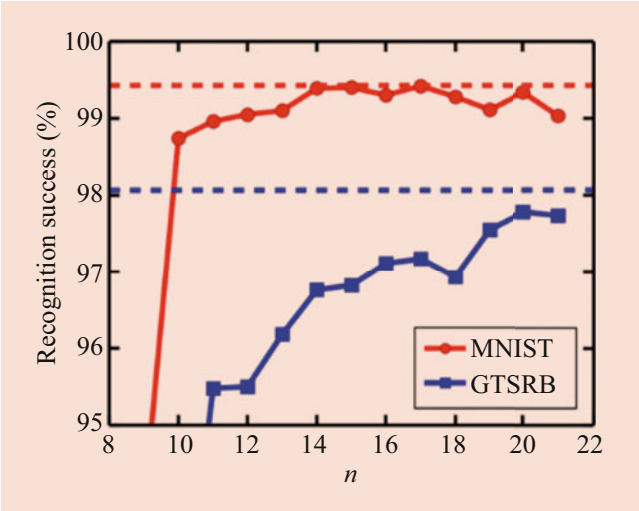


Fig. 17.16 Recognition success rate based on MNIST and GTSRB databases as a function of the number of OxRAM used as synapses building block. (From [107])

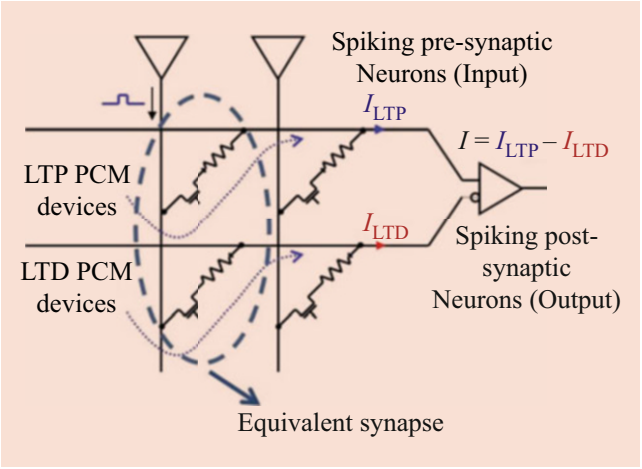


Fig. 17.17 Implementation of a PCM 2 bit cell array used as synaptic device. (From [110])

the set of feature maps gets simplified. Eventually the signal comes to the output neuron layer. The test chip is used to elaborate images from the MNIST (Mixed National Institute of Standards and Technology) database and the GTSRB (German Traffic Sign Benchmark) database containing the 43 German traffic signs. Each output neuron is associated with one category of images. Once an input image is selected belonging to that category, the output neuron is expected to spike out. In Fig. 17.15 the distributions of ON and OFF states of the used OxRAM cells are presented. These cells are connected in parallel in small groups. The amount of cells to be connected in group is computed by simulation and allows to tune the weight of the synapses. The recognition success of this test chip was evaluated by simulation and some results are reported in Fig. 17.16. As the OxRAM groups are enlarged, the recognition success increases since the synapse can be better tuned. With 12 OxRAMs in parallel, 99% pattern recognition of the MNIST database is reached.

Another chance for eNVM applications in neuromorphic chips is given by the unsupervised learning scheme. In the example we saw before in fact, the neural network must be trained and cannot be modified or improved more once the training is complete. If, for instance, a new set of images had to be learned, the training should start over again. Emerging memories as the OxRAM saw in the example can be used to modulate continuously the synaptic weights, de facto implementing the neuron plasticity typical of real brains.

In [109] a PCM device was used to implement a scheme for unsupervised learning in a fully connected neural network. In this case the memory cell can either increase or decrease the synaptic weight to make stronger or weaker connections. This application obviously requires a multilevel capability. Natively PCM shows a strong asymmetry between SET and RESET operations: while SET can be gradually

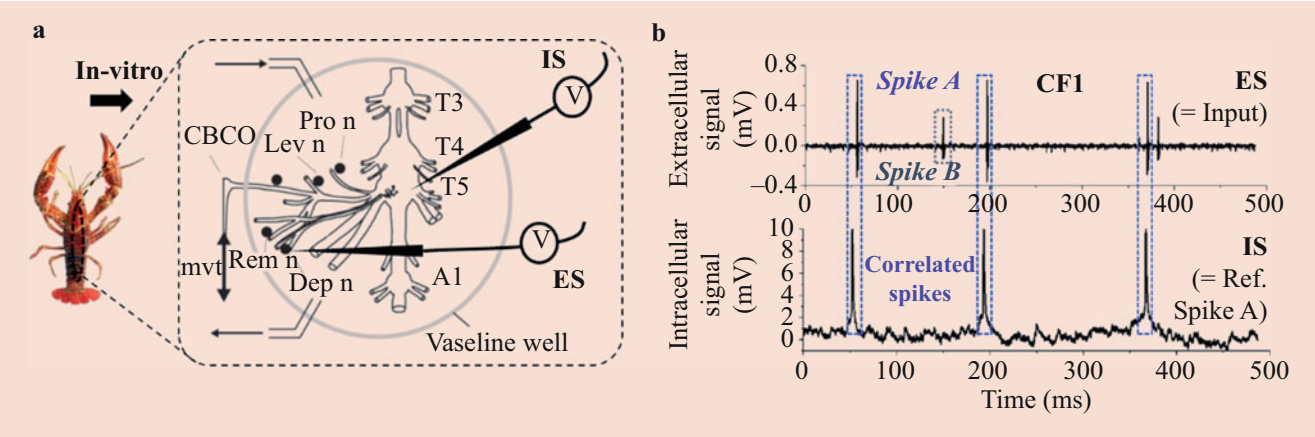


Fig. 17.18 (**a**) Drawing of a ganglion, whose extracellular activity can be recorded in vitro. The recorded signals (**b**) were decoded by a layer of 32 neurons. (From [112])

controlled, as the material crystallizes, RESET is intrinsically abrupt as a quench is generally needed to get the amorphous phase. In Fig. 17.17 a 2 bit synapse is shown, making complementary use of two PCM cells to achieve synapses with the capability of controllable resistance increase and decrease. When actually tested, this system allowed scoring 92% of pattern recognition with a system power consumption during the learning phase of 112 μW. This system was demonstrated for automobile tracking.

Another example of eNVM successfully used in fully connected neural networks is provided by [111]. In this study a CBRAM was exploited to act as synapse in a circuit dedicated to analog signal detection for auditory classification. The exhibited performance was very good along with a reduced power dissipation. The last aspect was indeed the driver advantage of using CBRAM instead of standard CMOS components.

A last example of eNVM for neuromorphic application is given in [112]. In this study low-power neuromorphic computing systems can also be coupled with brain-computer interfaces (BCI). This can allow the development of implants for rehabilitation purposes. The application requires the chip to analyze stream of data for biological sources, make computations, and provide an action in real time based on the input data. OxRAMs were used in a two-layer fully connected neural network able to identify, learn, recognize, and distinguish between different spike shapes of measured biological signals. The device acted without any supervision and was used to decode extracellular activity from in vitro crayfish nerves recorded simultaneously with intracellular data of one motor or sensory neuron of the T5 ganglion (see Fig. 17.18). The biological signal is encoded by 32 frequency band-pass filters. The 32 filtered signals are then full-wave rectified and presented to the input layer of 32 neurons where the analog continuous signals are converted into spikes which are then propagated along the synapses to the 5 output neurons. In this case OxRAM was chosen based on its capability at modulating ON and OFF resistance. This allows the network to keep on training itself by increasing and decreasing continuously the synapses strength in correlation with the input signal.

17.5 Memory Selectors

We have so far discussed about the memory cell; we have seen the different types of emerging concepts, each with their specific performances, challenges, and drawbacks.

In this section we will describe another crucial component of the memory array: the memory selector.

Considering the technology candidates discussed in previous sections in fact, only FeFET can properly work in an array without the need of an additional device that turns ON or OFF depending on which memory cell the system must address. This is possible because FeFET conducts very little current when ground potential is applied on its gate, just as a regular transistor. On the other hand, all resistive devices do not own a gate as they are two terminal devices. This means that in an array, to read a specific word of data, there must be a device that prevents current to be driven by the bits that are not selected, so to access the selected ones only. This task is the role of the memory selector.

Selectors must correspond to a large panel of specifications, the most part of which are summarized in Table 17.3. The most important parameter is the high ON/OFF ratio, but as the reader can easily figure out, the high ON current, the excellent endurance, the correct threshold switching, scalability, and manufacturability are all necessary, and for a selector candidate to fail, only one of these criteria would mean a no go.

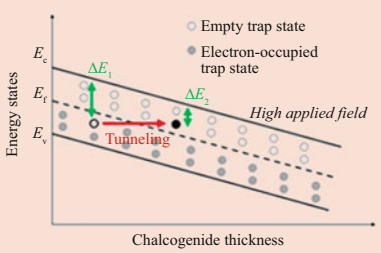
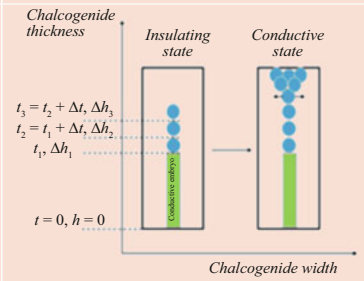
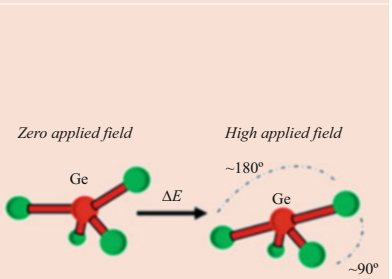
Regular transistors, like logic transistors, would look like good candidates for selectors, as they perform well with almost all requirements listed in Table 17.3, except one, the scalability. For an eNVM to be truly considered as successful embedded memory, its scalability is a key ingredient. This is because emerging eNVMs only make sense in advanced nodes as we discussed in Sect. 17.1. Of course this may come with some exceptions, as we will soon see. Ideally, the selector should not take more Si area than the memory cell, which means that the perfect solution would be a crosspoint array. We discussed already in previous sections about the crosspoint array and its first commercial demonstration by Intel with the Optane product series [3]. It is worth noting that a crosspoint array would of course be very beneficial also for all the innovative applications we discussed in Sect. 17.4 and would boost neuromorphic circuits as well as in-memory computing devices or any other memory-intensive application. Even so, different solution can also be envisaged. For instance, the PCM-based solution by STMicroelectronics adopts a MOSFET as selector, in order to provide enough current density for the demanding reset operation in phase change [125]. This solution implies no crosspoint architecture, but it is still performant in terms of density in 28 nm technology for small arrays.

Table 17.3 A list of key parameters and requirement for memory crossbar selectors

Parameters	General requirement
ON/OFF current ratio	Dictated by the array memory size mainly
Scalability	Ideally selector should not taka additional Si area
Theshold voltage	Compatible with the memory device
Polarity	Compatible with the memory device
ON MAX current	As high as possible, dictated by the energy need of selected cell
Manufacturability	Should not require any modification to the standard process
Endurance	Virtually infinite, at least much larger than memory cell
Reliability	Temperature stability higher than memory cell

In this section we will focus on back-end selectors intended for crosspoint architectures, and we will propose a non-exhaustive review of selectors that appeared in literature so far. A basic categorization of selector types can be cleverly given following [114]. Barrier engineering of single junction or multi-junctions achieves step IV electrical characteristics by tuning the band diagram. Typically a multi-junction can be more performant than a single one but necessitates a more complex process [115–120]. Volatile memory components can also be adopted, in which a filament temporarily shunts the two electrodes and dissolves rapidly after polarization is interrupted [121–124]. The main inconvenience in this case is the time required for the filament to spontaneously dissolve, which can be long with respect to the targeted latency. On the other side, a very steep IV curve is achieved. Eventually threshold switching is among the most promising devices as selector candidates. In most cases chalcogenide materials are adopted as they show a sudden increase of conductivity when a threshold voltage is achieved. Below threshold the resistivity can be very high which guarantees an exceptional selectivity. Although chalcogenide materials have been studied for several decades, the actual physics involved in the threshold switching is still subject to debate. In Table 17.4 three main physical pictures summarize the leading physical explanations that are proposed in literature. The first description (first column of the table) uses the nonequilibrium charge distribution across the material to explain the switching: the

Table 17.4 Principle kind of selector based on their working principle

	Refs. [134 and 136]	Refs. [137 and 138]	Ref. [139]
Mechanism	Field-induced electron energy increase (hopping transport), balanced by energy relaxation (phonon-electron interaction)	Field induced cristal nucleation (phase change) in a host of amorphous resistive MATERIAL	Electric field assisted creation of a metastable metavalent bond
Demonstration	Analytical model combined to electrical measurements Thickness, T^* and material dependence of threshold voltage and current	Analytical model combined to measurements Switching time exponential dependence with voltage and temperature	Ab initio calculations combined to material analyses and electrical measurements
Schematics			

From [114]

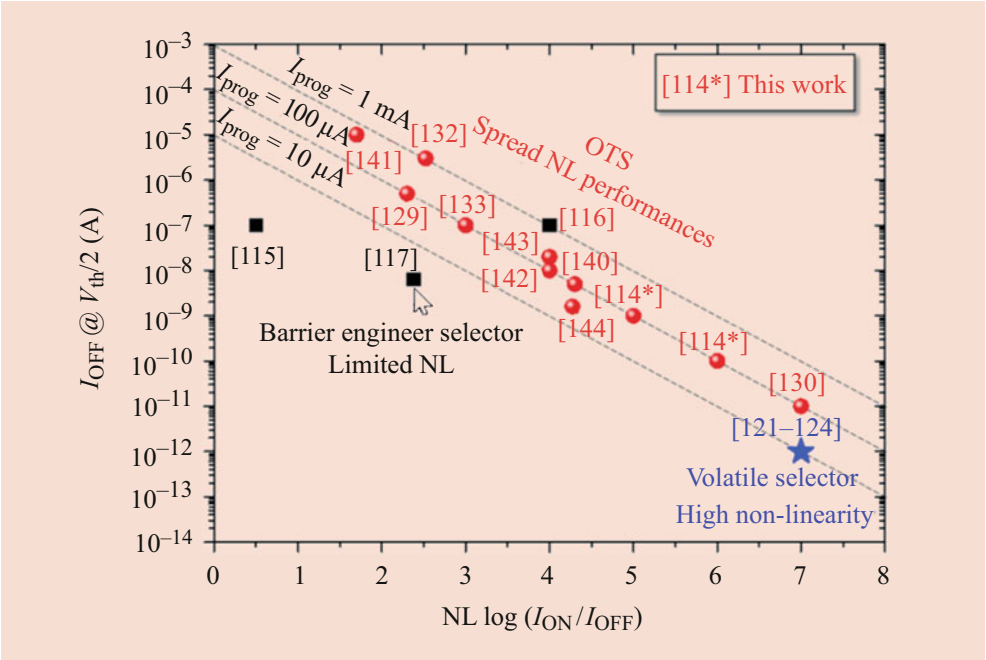


Fig. 17.19 Off current at $V_{th}/2$ vs ON and OFF currents for various selectors in literature. (From [114])

applied field reduces the barrier seen by the electrons in their hopping transport which increases locally the charge's energy. This causes the lowering of electric potential and a further bending of the conduction band near the injection interface, causing a further increase of electron hopping. The system evolves to lower resistivity until the energy relaxation, induced by phonon-electron interaction, saturates the conductivity. A different picture (middle column in Table 17.4) explains the switching as a localized phase change with the growth of a tiny crystalline filament that eventually shunts the electrodes. In this model the growth of the filament is assisted by a locally induced point effect which enhances the field and the temperature at the filament's tip. A third picture (last column in Table 17.4) which applies in particular to Se-based chalcogenide glasses explains the switching as a dipole alignment of metastable bonds.

The principle of a crosspoint selector is very simple. During reading the selector of the selected cell turns on only if the memory bit is in its low resistive state, which causes the reading potential V_{read} to induce switching in the selector. This approach is widely accepted and described, for instance, in [127–134]. Differently, if the memory bit has a high resistance, the read potential V_{read} is insufficient to turn on the selector as most of it drops on the memory bit.

In the next part, we describe the state of the art of OTS selectors mainly in terms of their nonlinearity (ratio between ON and OFF current) and their selectivity (ratio between the ON current in reading condition and the leakage current at $V_{read}/2$), and we focus on some results on read disturb and endurance in the specific case of HfO_2-based OxRAM.

As discussed before probably the most important characteristic of a selector is its ability to prevent sneak paths which would drive current toward unselected cells in a crosspoint array. This means that a selector must feature a very high conductivity in the ON state while also possessing very low leakage current in the OFF state. This is generally referred to as nonlinearity (NL). A good selector shows a very steep IV curve above the threshold potential and a very low parasitic current below it. In Fig. 17.19 the reader can appreciate how different kinds of selectors behave. As it is also clear, a high nonlinearity generally is also accompanied by a lower leakage current, and this general behavior applies for all kinds of selector described in Table 17.3. This is rather obvious as a selector device ON current is upper bound by the application current requirement, and thus its NL is mostly defined by the leakage current amplitude. The OFF current is also critical to determine the tile size of any array, as the leakage current of individual selectors sums up to a total OFF current. As can be seen in Fig. 17.20, multi-MB tiles are possible for OTS selectors.

Furthermore, when a selector in series with a memory cell is considered (1S1R), the programming voltage of the latter is generally dependent on the leakage current of the former. This is true as low leakage OTS is always accompanied by high threshold switching potential. This can be appreciated in Fig. 17.21. In addition, when the selected cell is in its high resistance state, an additional drop of potential appears across it which sums up to the switching voltage of the selector. This leads to a very difficult design of the array, as one must take into account the maximum array size, thus the total

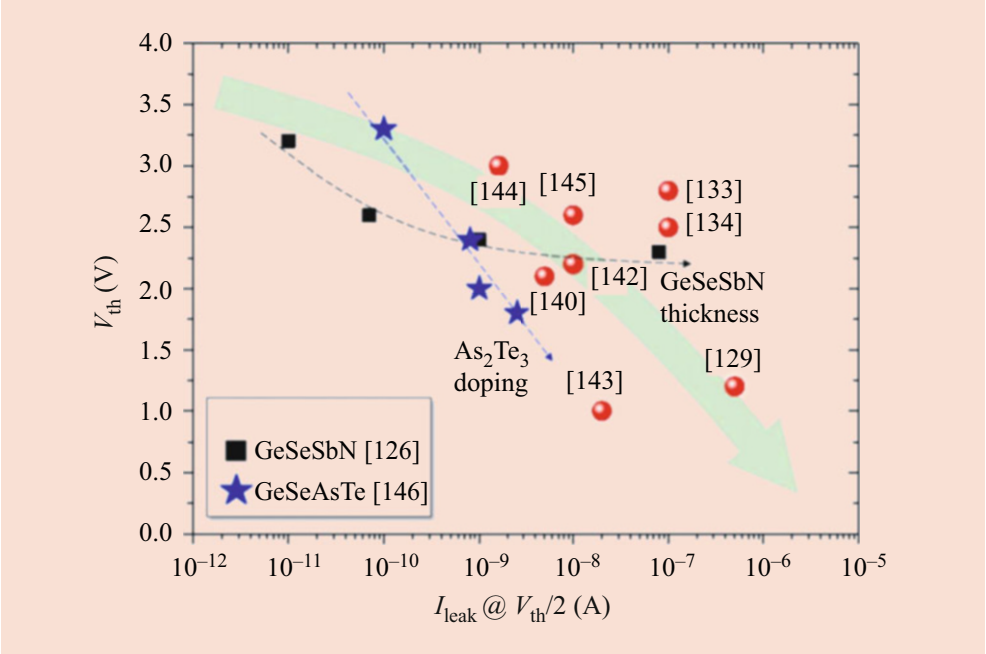


Fig. 17.20 PTS threshold voltage vs current leakage at $V_{read}/2$. Different selector candidates are reported. (From [114])

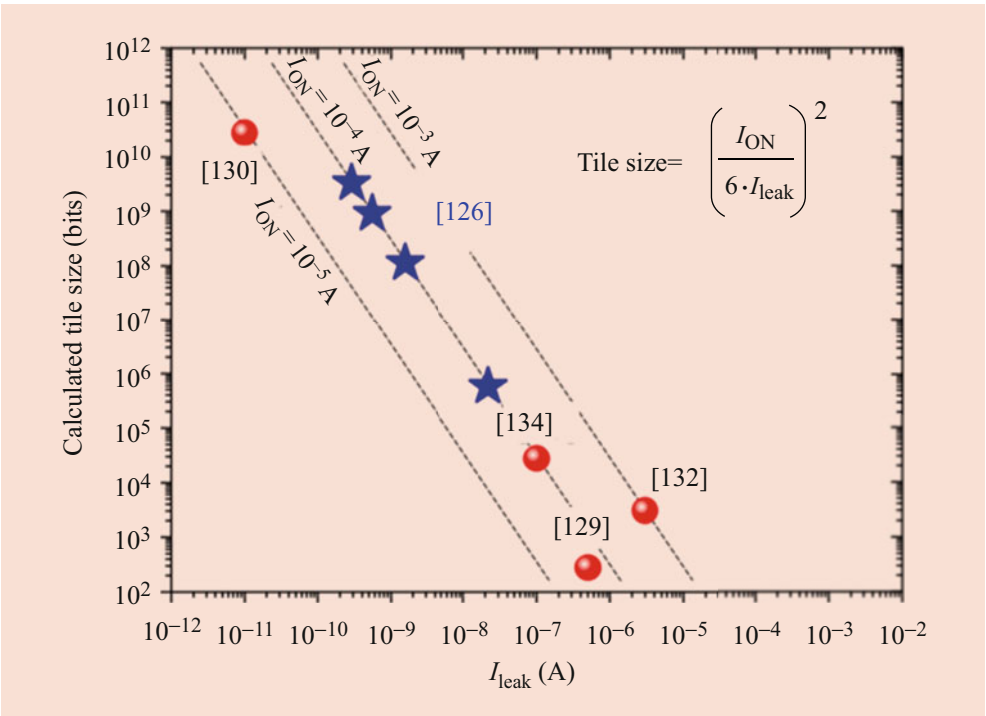


Fig. 17.21 The selector OFF current (and the ON current target) dictates the maximum tile size. (From [114])

leakage current plus the maximum required voltage in the array, which dictates the BL and WL drive transistor type. It seems quite clear that the voltages required in the array are relatively high (in the order of 2–4 V [114]), and this means that thick oxide transistors are likely required. On the other hand, as OTS selectors are built in BEOL, it appears possible to "hide" the driver transistor below the selectors, thus keeping the silicon efficiency to a maximum.

Another figure of merit that surely represents a challenge for OTS is endurance. While for a memory component 10^6 write/erase cycles appear a very reasonable target at array level, a selector must ensure a switch ON/OFF endurance as

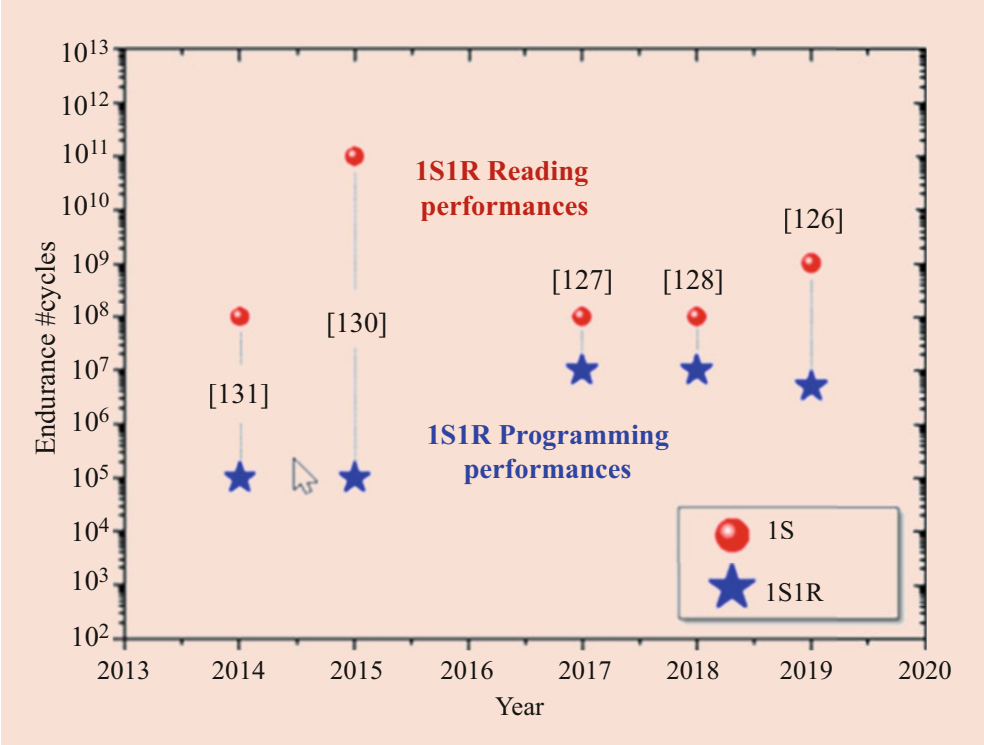


Fig. 17.22 As endurance is one of the most important parameters for selectors, many efforts were spent to improve it. Over the last 5 years, an improvement of X10 was achieved on intrinsic device. (From [114])

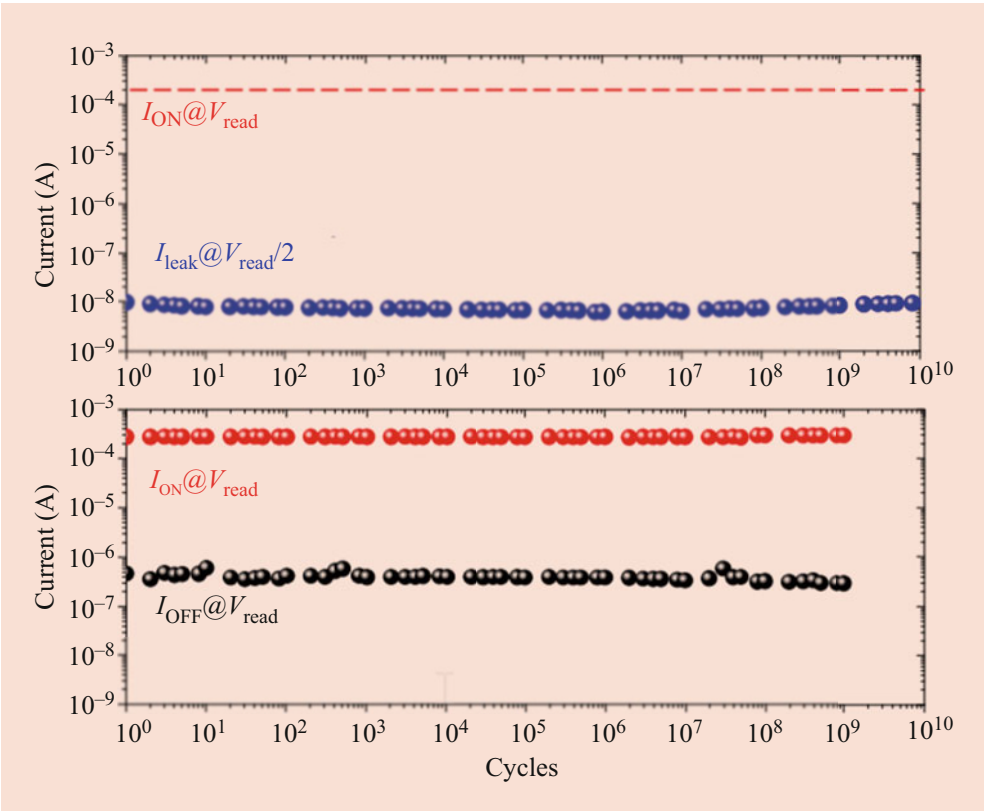


Fig. 17.23 Measured current disturb at $V_{read}/2$ and at V_{read} during endurance test for an HfO_2 OxRAM equipped with a GSSN OTS selector. (From [114])

large as the maximum readings as possible on the memory cell. This means in the order of 10^{10} to 10^{12}. In Fig. 17.22 some results are reported showing the improvement over the years of the read endurance as well as the write endurance of the 1S1R device. More in detail, Fig. 17.23 reports the read disturb at $V_{read}/2$ as well as the readings at V_{read}. These data come from 1S1R device, R being a HfO_2-based OxRAM and the selector being a GSSN OTS device described in [126].

In conclusion, selector development faces as many challenges as the memory devices themselves but has the potential to unlock the ultimate scaling potentials of emerging resistive devices.

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Silicon Sensors

18

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Contents

18.1 Overview . . . 635

18.2 Present and Future Market Applications of Sensors . . . 637
18.2.1 Automotive Micro-sensors . . . 638
18.2.2 The Sensor Consumerization Wave . . . 639
18.2.3 The Internet of Things Era . . . 643

18.3 Micro-sensor Classification and Terminology . . . 645
18.3.1 Classification . . . 645
18.3.2 Terminology . . . 648

18.4 Microfabrication and Micromachining . . . 649

18.5 Microsystem Back End . . . 650
18.5.1 Micro-sensor Assembly and Packaging . . . 651
18.5.2 Micro-sensor Testing and Calibration . . . 653

18.6 Accelerometers . . . 653
18.6.1 Accelerometers Introduction . . . 653
18.6.2 Accelerometer Specifications . . . 654
18.6.3 Accelerometer System . . . 655
18.6.4 Capacitive MEMS Accelerometers: Design Principles . . . 655
18.6.5 Capacitive MEMS Accelerometers: Process Flow . . . 656
18.6.6 Reliability Challenges for MEMS Accelerometers . . . 659
18.6.7 Next-Generation MEMS Accelerometers . . . 660

18.7 Gyroscopes . . . 660
18.7.1 Gyroscopes Introduction . . . 660
18.7.2 Gyroscopes Specifications . . . 660
18.7.3 Gyroscope System . . . 662
18.7.4 Capacitive MEMS Gyroscopes: Design Principles . . . 662
18.7.5 Capacitive MEMS Gyroscopes: Process Flow . . . 664
18.7.6 Reliability Challenges for MEMS Gyroscopes . . . 665
18.7.7 Next-Generation MEMS Gyroscopes . . . 665

18.8 Microphones . . . 666
18.8.1 Microphones Introduction . . . 666
18.8.2 Capacitive MEMS Microphones . . . 668
18.8.3 Piezoelectric MEMS Microphones . . . 669
18.8.4 Reliability Challenges for MEMS Microphones . . . 671

18.9 Pressure Sensors . . . 672
18.9.1 Pressure Sensors Introduction . . . 672
18.9.2 VENSENS™ Pressure Sensor . . . 672
18.9.3 Bastille™ Pressure Sensor . . . 673
18.9.4 Reliability Challenges for MEMS Pressure Sensors . . . 673

18.10 Magnetometers . . . 674
18.10.1 Magnetometers Introduction . . . 675
18.10.2 Hall Sensors . . . 675
18.10.3 Magnetoresistive Sensors . . . 676
18.10.4 Anisotropic Magnetoresistive Sensors . . . 677

18.11 Silicon Image Sensors and Evolutions of CMOS . . . 679
18.11.1 Introduction . . . 679
18.11.2 CCD and CMOS . . . 681
18.11.3 CMOS Image Sensor: A Complete Solution . . . 685

References . . . 696

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Abstract

In the course of human history, the development of high performance low-cost sensors has been fundamental for the progress of Homo sapiens in many fields. In the last 20 years, the pace of sensor development accelerated thanks to microfabrication techniques typical of semiconductor industry. Automotive was the first market to adopt in high-volume silicon sensors; then thanks to the sensor consumerization wave, silicon sensors spread widely in many products of the consumer market (MEMS, Industry group: 2007 industry report, 2007). Entering the internet of things era and with the advent of artificial intelligence, the importance of silicon sensors will continue to grow.

Sensors are all around us: they are in cars, in smartphones, in factories, in pacemakers, in drones, in smart

speakers, and in many other places, with the ultimate goal to sense and to monitor parameters of importance and interest in our daily environment. They play an essential bridge between electronic systems and the user or environment. This chapter is addressing both the technical and business aspects of the commercially most successful silicon sensors, highlighting also the most common wrong prejudices of this industry.

Firstly, this chapter will detail the most relevant market applications of the silicon sensors and their future use in conjunction with the emerging technologies of artificial intelligence and low-power wireless connections, including 5G. Secondly, it will recap the most important features of the sensors, their taxonomy, their sensing fundamentals, their microfabrication technologies, and the great relevance of the package and testing for the sensors. Thirdly, it will discuss detailed examples of the most commercially successful sensors (MEMS, Industry group: 2007 industry report, 2007; MEMS, Trends, 10, pag. 18, 2012) that we can find all around us.

Keywords

MEMS · Inertial sensor · Accelerometer · Gyroscope · Magnetometer · Pressure sensor · Microphone · Silicon image sensor

18.1 Overview

A sensor is a device that detects a change in a physical parameter (i.e., the measurand) and transduces this change into an electronic signal, i.e., a current, voltage, or charge. A sensor is a measurement instrument used to interface with the external world, enabling the sensor user to understand the world more deeply and thus to dominate it. The word sensor comes from the Latin word sensorium, derived from the verb sentire that means perceive with our senses. A man is able to sense the reality with his five senses (hear, see, smell, touch, taste), and since the beginning of his appearance on Earth, humankind, realizing the limits of its natural senses, has been constantly developing better and better sensors. The goal has been always the same: Homo sapiens wanted to become the master of the world.

Time has been the first measurand that humanity has been interested to measure. Two thousand years ago, the Egyptians used large obelisks to track the movements of sun and to measure the passing of time; they developed also water clocks later used by both the Greeks (calling them clepsydrae) and the Chinese, while Japanese were using burning candles to measure time. In the ancient world, time measurement was important for many different purposes, from knowing the exact hour to hold the religious rites for worshipping the gods to the time slot allocated to the defense lawyers in old Rome's courts and to the paid time slot allocated to prostitutes' customers in several brothels [3]. If we exclude few other instruments, like the compass invented in China (used for divination first and later for navigational orienteering around 1050 A.D.), we need to wait for the Scientific Revolution of the seventeenth century, whose foundational Galilean scientific method required the development of many more instruments to challenge the dogmatism of the pre-modern era. Only in the last 40 years a strong boost to sensor massive adoption came from the automotive market (airbags, etc.) and, later, from the consumer and personal electronics market (computers, mobile phones, watches, etc.), thanks to sensors' increased reliability, more affordable cost, optimized power consumption, and miniaturized size.

Sensors are multidisciplinary devices that require the master of many disciplines (physics, engineering, electronics, materials, control theory, etc.) for their design and their production. They are creating new opportunities in many consolidated markets, such as automotive, consumer, and personal electronics, and they are now undergoing a great expansion, owing to the emerging application in industrial internet of things, artificial intelligence, 5G, and future forms of reality (augmented, virtual, and mixed) [4].

The physical dimensions of the different types of sensors span a wide range, from meter scale (i.e., the antennas for space exploration) to microscale (i.e., the ultrasmall silicon-based sensors). The techniques and the materials used to manufacture the different kinds of sensors are also very much different, involving materials such as plastic, ceramics, metals, and semiconductors. The goal of this chapter is to describe commercially successful silicon sensors having two important features:

- They utilize silicon as material, exploiting its excellent semiconductor and thermomechanical properties [5].
- They are realized by means of microfabrication techniques, enabling mass parallelization. When there are 3-D structures in the sensor, realized with micromachining techniques, they are also known with the English acronym of MEMS, i.e., microelectromechanical systems.

These transducers are also known as micro-sensors, since the single smallest dimension is at sub-micrometer scale, though a complete sensor containing both the tracer elements and the electronic ones can be of the order of millimeter. Micro-sensors can be composed of one silicon die containing the transducer standalone (integrated microphone of Akustica) or of multiple dice including also the electronic chip (inertial modules or microphone of STMicroelectronics [6]), all arranged in the same package by means of system in package (SiP) or system-on-chip (SoC) technologies (Table 18.1 and Fig. 18.1).

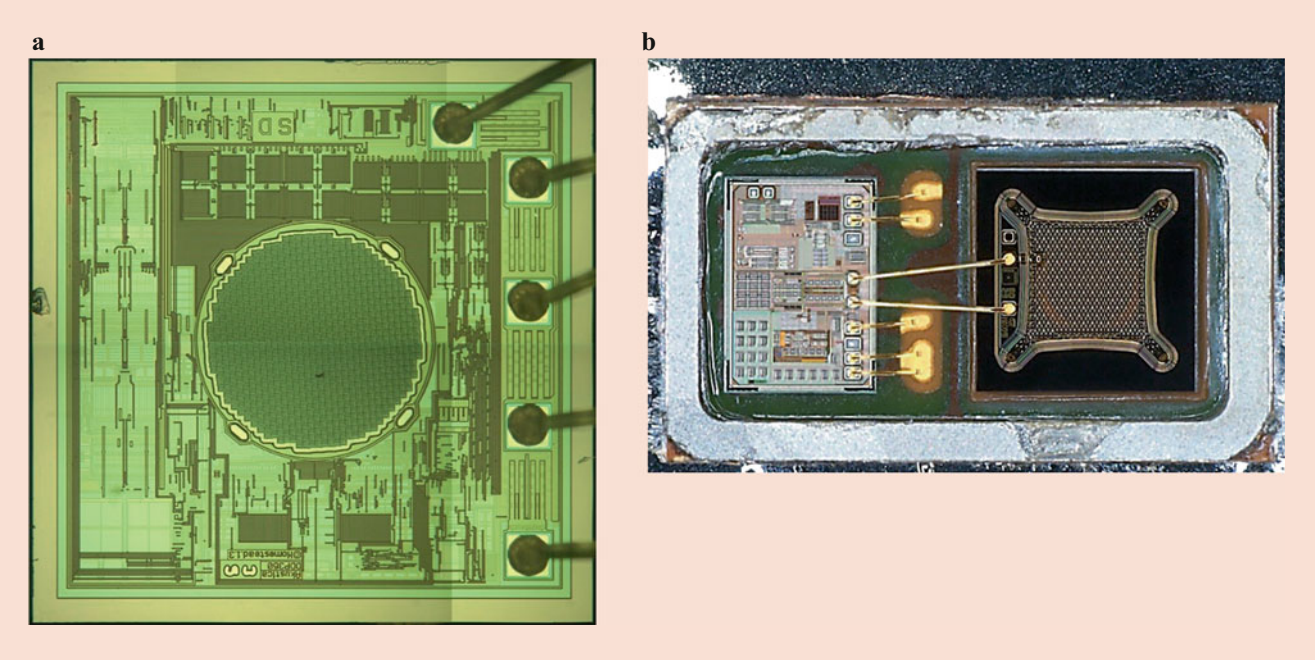

Fig. 18.1 (**a**) Akustica AKU230 integrated microphone is an example of system on chip: membrane is visible in the center, with circuitry all around. (© 2012 MEMS Microphones Technical and Cost Review by System Plus Consulting.) (**b**) STMicroelectronics microphone is an example of system in package: microphone transducer (right) and integrated circuit (left). (© 2018 STMicroelectronics)

Table 18.1 Mechanical and electrical properties of intrinsic silicon

Yield strength (10^{10} dyne/cm^2)	7.0
Knoop hardness (kg/mm^2)	850
Young's modulus (10^{12} dyne/cm^2)	1.9
Density (g/cm^3)	2.3
Thermal conductivity (W/cm °C)	1.57
Thermal expansion (10^{-6}/°C)	2.33
Electron mobility at 300 K (cm^2/V s)	1400
Hole mobility at 300 K (cm^2/V s)	450
Energy gap at 300 K (eV)	1.12

Therefore, this chapter will not address the whole world of sensors. It would be a task too huge to be addressed in a single chapter of a book. We will not talk about non-silicon sensors such as zirconia ceramic oxygen lambda sensors, disposable plastic blood glucose sensors, harsh environment pressure sensors with stainless steel membrane, high performance fiber-optic sensors, piezoelectric quartz resonating gyroscopes, pyroelectric single crystalline lithium-tantalite infrared sensors, II–VI semiconductor cadmium selenide near-infrared detectors, giant magnetoresistive read/write heads for hard disk drive on aluminum titanium carbide ceramic substrates, III–V semiconductor indium antimonide Hall sensors, and nano-sensors based on carbon nanotubes. A complete overview of sensors can be found in specific handbooks such as those in Refs. [7, 8].

The silicon semiconductor sensor era officially starts after the visionary talk given by Feynman on December 1959 [9] and with the realization of the first resonant gate transistor (RGT) of Nathanson et al. in [10].

The RGT allowed the incorporation of high Q frequency selection into silicon integrated circuits. It was batch-fabricated in a manner consistent with silicon technology, and it had a vibrating gold beam operating in the frequency range from 1 to 100 kHz, depending on the geometrical dimensions of the resonant gate, with a gate length in the range of few hundreds of micron and few micron-scale thickness.

Since the beginning, micro-sensors used the same manufacturing techniques of the CMOS (complementary metal-oxide semiconductor) industry, whose evolution was dictated by the famous Moore's law. Since the market for silicon sensors has been much smaller than CMOS industry, micro-sensors have been always classified as part of the so-called more-than-Moore (MtM) world [11]. There are many books, articles, and publications on the MtM subject. But considering both the increasing relevance that micro-sensors continue to acquire in the field of internet of things to boost the wider adoption of artificial intelligence (AI) and the strong contribution given by Feynman, envisioning the possibility to miniaturize the sensors and to stack specialized silicon wafers to realize a complex versatile microsystem, the time has come to see the micro-sensors as part of the Feynman

roadmap instead of more-than-Moore roadmap. The authors of this chapter propose the following transition:

More-than-Moore → Feynman roadmap

This chapter addresses market, technical, and fabrication relevant facts of the micro-sensors, highlighting also some of the prejudices that miserably failed on the market.

18.2 Present and Future Market Applications of Sensors

Today sensors are used almost everywhere to sense and monitor parameters of importance and interest in our daily environment. They play an essential role as interface between electronic systems and the user or environment. Because of the large number and variety of devices required for performing different functionalities, the sensor market is huge.

The most successful silicon sensors include capacitive accelerometers, gyroscopes, microphones and pressure sensors, piezoresistive pressure sensors, temperature sensors, Hall effect and magnetoresistive magnetic sensors, CMOS image sensors, time of flight sensors, ambient light sensors, and humidity and gas sensors. They are used across all the market segments from automotive to personal electronics, from industrial to computers [1]. In the last 40 years, we have also seen many micro-sensors abandoning the CMOS plants because of their inability to meet customer requirements in terms of either cost or performances. These examples include the piezoresistive accelerometers and microphones, the electromagnetic and piezoelectric gyroscopes, and, last but not least, many biosensors for DNA analysis (i.e., lab-on-a-chip).

All modern cars have active (i.e., vehicle dynamic control™) and passive safety systems (airbag) based on micro-machined accelerometers and gyroscopes (inertial sensors). Car tires, equipped with pressure sensors measuring constantly the pressure and alerting the driver in case of danger, are widely spread. Pressure sensors are also used to measure the ambient and the intake manifold pressure to optimize the fuel-to-air ratio with the goal to reduce carbon footprint [12].

Sensors are also used in the industrial market for factory automation, preventive machine diagnostics, and post-sales support.

In the last 30 years, accelerometers spread out also in pacemakers to adapt the pacing signal frequency to the physical activity of the patient and in neurostimulators for different purposes.

It is only in 2005 with Nokia N95™ camera phone and in 2006 with Nintendo Wii™ that the world sees the dawn of the sensor consumerization wave. The Nokia N95™ camera phone was designed, indeed, to achieve in many use cases the same experience as a consumer digital still camera (DSC) product, with exceptional quality at resolution of 5 megapixels so the user could edit the images after capture. In 2006, the three-axis accelerometer of STMicroelectronics together with Wii™, the revolutionary game console of Nintendo [13], changed dramatically the way people were interacting with the digital world of electronic games. Now micro-sensors are everywhere from smartphones to laptops, from tablets to high-end digital cameras, from watches and hearable devices such as the AirPods® to shoes and professional or consumer drones. More intuitive user interfaces, step counter, image stabilization, image and video capture, and depth measurements are just a few of the many applications of sensors in the consumer market. The pictures below show the sensor market revenue by final application category and sensor type (Figs. 18.2, 18.3, and 18.4).

Nowadays, inexpensive, highly reliable, energy-efficient, and tiny sensors enabled by the sensor consumerization wave are ready to be coupled with low-power radios (sub-GHz, Bluetooth, Wi-Fi, Sigfox, LoRa, narrowband IoT, 5G, etc.) in certified wireless modules to enable the large-scale deployment of wireless sensor networks. With the smartphone volume growth slightly decreasing, many technical and business experts believe that we are now leaving the nomadic era, to enter the internet of things era, enabled by wireless sensor networks, autonomous robots, 5G ultrashort latency communication networks, and artificial intelligence [1, 14, 15] (Fig. 18.5).

The following three sections discuss briefly the use of micro-sensors in automotive market, the MEMS consumerization wave, and the dawn of wireless sensor nodes era.

18.2.1 Automotive Micro-sensors

Safety, comfort, and environmental control applications have been the three main drivers of wide micro-sensor adoption in all modern cars from the 1970s till the beginning of our century. Only in the last few years there has been a revamp of micro-sensor adoption in the car industry thanks to autonomous car recent developments. Signals from multiple-axis accelerometers, gyroscopes, and pressure, magnetic, and airflow sensors must be fused together to address the needs of several different applications.

In 1974, the first micro-machined silicon pressure sensors started to be used in electronic fuel injection systems to monitor the manifold absolute pressure (MAP), while mass airflow sensor was used to optimize the air-to-fuel ratio, to reduce gasoline consumption. One decade later, in the 1980s, the pressure sensors started to be used to measure atmospheric pressure, fuel pressure, oil pressure, and others. In particular barometers, measuring the drop of pressure at

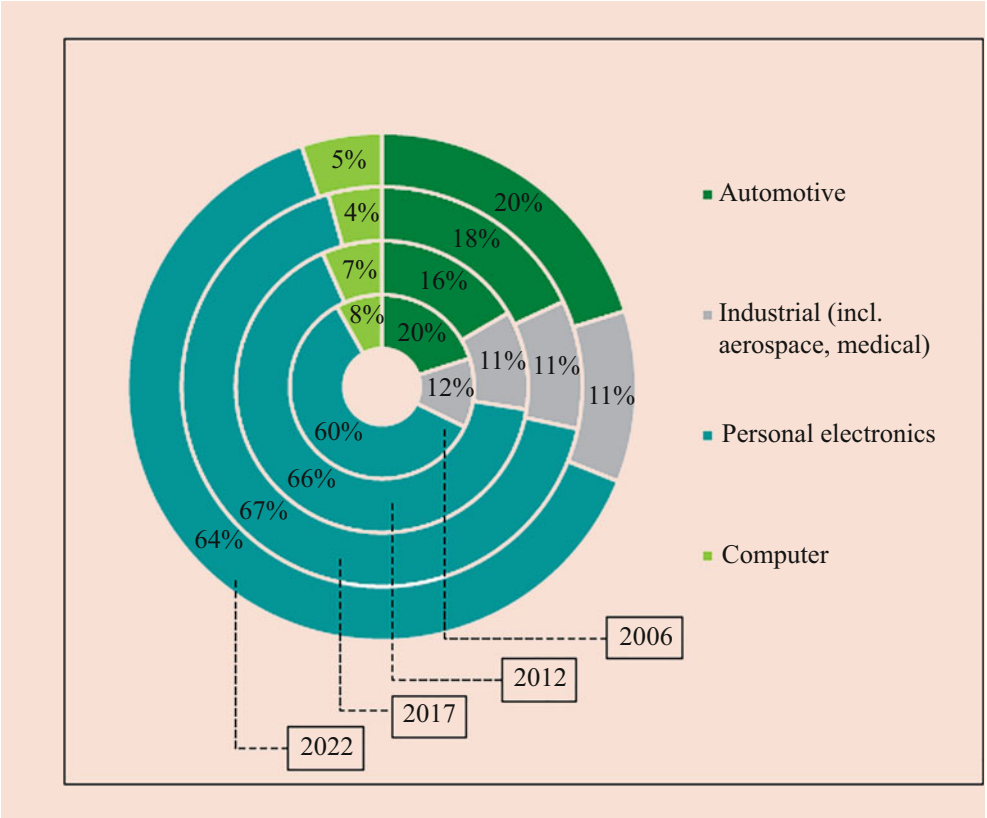

Fig. 18.2 Sensor market revenue by application category (2006–2022). (Source:© 2018 IHS Markit)

different altitude, allowed to increase car engine efficiency, reducing the carbon footprint. Starting April 1, 1989, the US National Highway Traffic Safety Administration (NHTSA) mandated the use of driver-side airbag, and in 1993, dual front airbags in all passenger vehicles were mandated. Few years later, side impact airbags were also required. A microfabricated accelerometer, detecting any sudden change in the vehicle acceleration, in combination with an algorithm, triggers an explosive charge that rapidly deploys the airbag. The airbag accelerometers can be located either in the central part of the car and in this case detect accelerations from 40 to 70 g (g being the acceleration of the Earth's gravity) or in the periphery of the car (satellite accelerometers), with a full scale ranging from 50 to 500 g. After 1996, active safety systems, such as vehicle dynamic control (VDC™) or electronic stability control (ESC®), started to use high-grade low-*g* accelerometers (up to 5 g), yaw rate gyroscopes, and magnetic speed sensors at each wheel. These safety systems help drivers handle a car on icy or rainy roads better, by preventing the dangerous situation of under- or over-steering. After wide adoption of sensors for active safety in European vehicles, in April 2006, the NHTSA mandated the use of ESC active safety systems in all US passenger vehicles, beginning in 2012.

Initial bulky and power-hungry piezoresistive accelerometers, manufactured by Sensonor, and piezoelectric quartz-based yaw rate sensors, mostly manufactured by Panasonic (Japan) or Systron Donner (USA), left the ground to more reliable, lower power, and ultrasmall capacitive inertial sensors (accelerometers and gyroscopes) manufactured by STMicroelectronics, Robert Bosch, and NXP. Micro-machined capacitive sensors, moreover, offered the big advantage to be combined all together on the same package, opening the way to multiple-axes inertial sensors in the automotive safety market, with VTI first, Bosch, and STMicroelectronics later.

After the year 2000, in which the high failure rate of a specific tire brand was implicated in more than 270 deaths and almost 1000 injuries, pressure sensors started to gain momentum for measuring the pressure in the tire and for alerting the driver in case of anomalies. All vehicles manufactured in 2008 or later will have a tire pressure monitoring system. The system consists of a piezoresistive pressure sensor, a simple microcontroller or state machine, and a sub-gigahertz wireless link. It also contains an accelerometer to wake up the systems when the vehicle starts moving.

Last but not least, in car navigation systems based on Global Position System (GPS), receivers also use accelerometers, gyroscopes, and magnetic sensors for dead reckoning

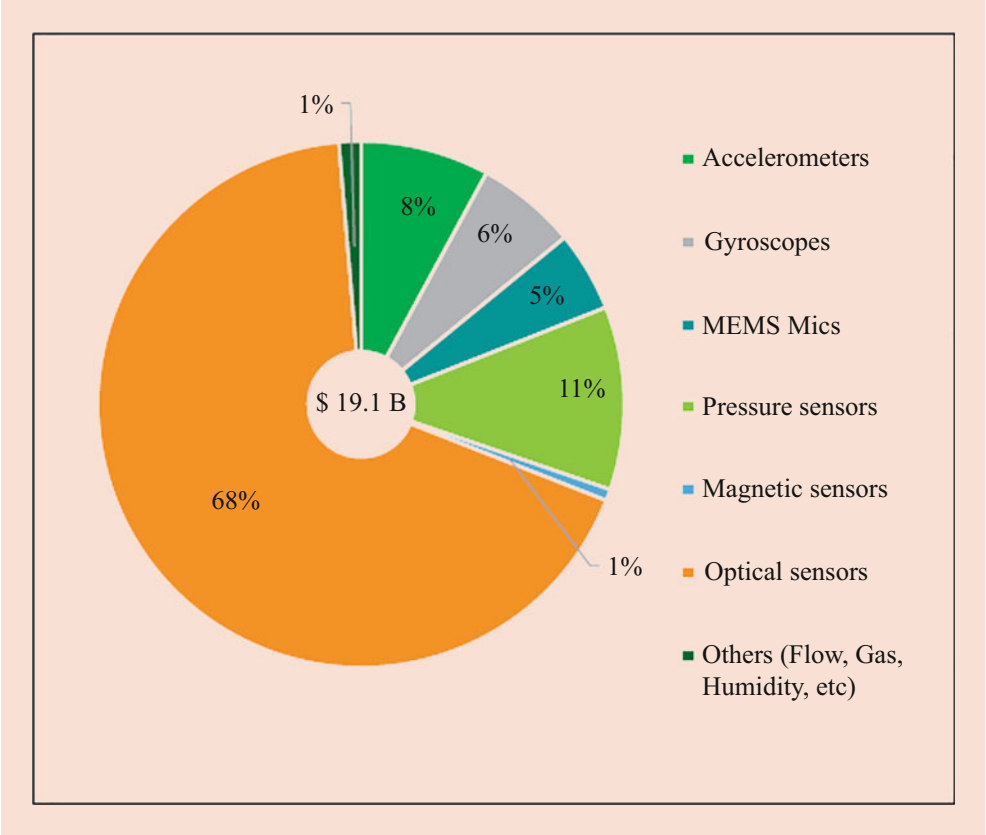

Fig. 18.3 Sensor market revenue by sensor (2017). (Source: © 2018 IHS Markit)

in case urban canyons, tunnels, or blind spots cause a fading of the satellite signals. In year 2012, a big boost to micro-sensor adoption in car navigation systems came from the first available single-package three-axis gyroscope of STMicroelectronics.

18.2.2 The Sensor Consumerization Wave

If the adoption of sensors in the automotive was driven by regulation, vision and imagination triggered the proliferation of micro-fabricated sensors in the consumer market. A few visionary companies, including STMicroelectronics, Knowles Acoustics, and Avago, invested heavily to support the development and manufacturing of sensors, such as accelerometers and microphones, and bulk acoustic wave filters, all suitable for the consumer market [1]. This triggered an extraordinary surge in the number of applications in the consumer market, with user interface applications being the most dominant across several market segments: from remote game controllers to smartphones, from tablets to laptops, from wearable to hearable. Only in the last few years the arrival of artificial intelligence-enabled smart speakers on the market starts to show the full potential of microphones, once seen only as a mere replacement of old electret microphones in the mobile phones. Moreover recently miniaturized motion sensors became a key enablers for a smoother and easier motion control of robots and cobots in industry 4.0 factories.

At the same time, MEMS sensors were spreading all over the consumer market; Nokia N95™ using the 5 megapixel STMicroelectronics CMOS image sensor started to displace the Japanese digital still cameras. And now after 14 years, digital still cameras have been completely replaced by smartphones embedding higher-resolution cameras, up to the recent 48 megapixel cameras of Sony. If at the beginning the CMOS sensors were used for simple video and image capture, now they are used to capture information for application control, multi-shot picture fusion, computational imaging, multi-sensor fusion, and visions applications. Moreover, since the end of 2017, near-infrared CMOS sensors (in iPhone X of Apple) have been used for biometric applications, and just recently some smartphones (like Huawei Mate X) [16] are embedding also time of flight (ToF) sensors for augmented, virtual, and mixed reality applications. Recently announced HoloLens 2 [4] makes also extensive use of indirect time of flight sensors for 3-D mapping of the environment around the user.

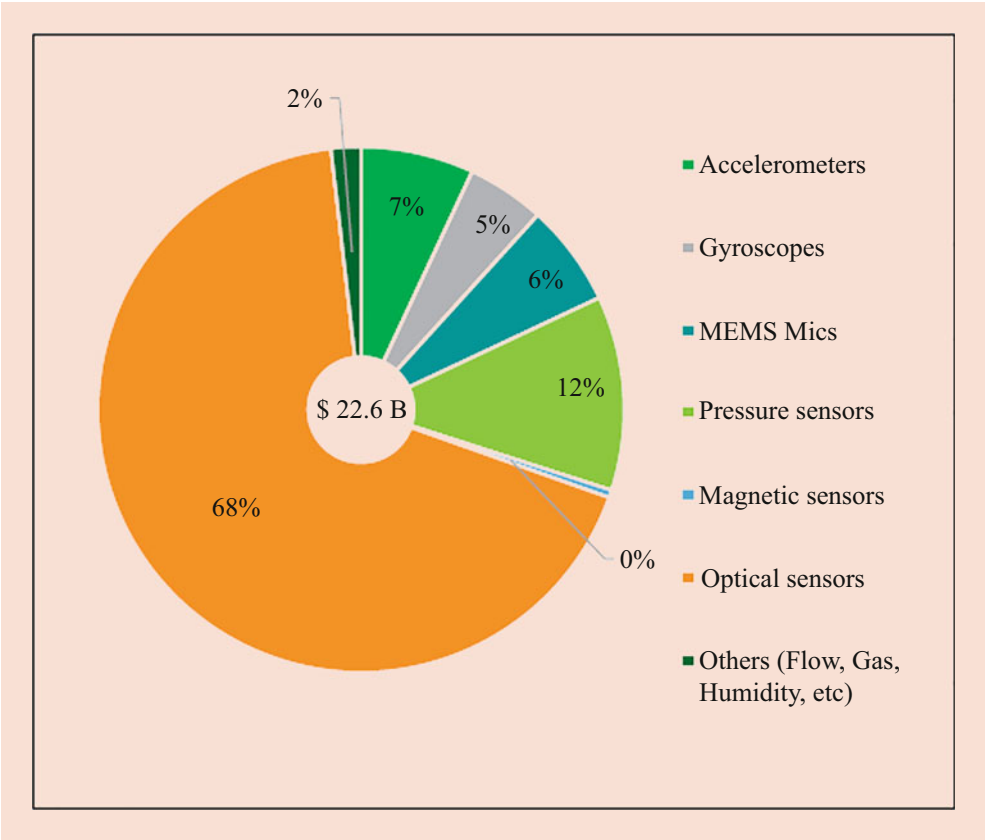

Fig. 18.4 Sensor market revenue by sensor (2022). (Source: © 2018 IHS Markit)

Sensors for User Interface in Game Consoles

May 2006 is definitely a key date for the dawn of the sensor consumerization wave. Before that date accelerometers were used for some medium-volume consumer applications, such as free fall protection in hard disk drives, and gyroscopes were used in digital still cameras and camcorders to improve the quality of recorded video and pictures. The launch of Nintendo Wii™ game console equipped with two single-hand controllers, each with a three-axis accelerometer, represents, without any doubt, the onset of the sensor consumerization wave on a large scale. Some authors of this chapter attended the launch of the Wii™ game console in the Kodak Theater in Los Angeles, and they still remember the thrilling atmosphere in that magic place. Nintendo wanted to leverage an easier user interface to fight against the high processing graphics of Microsoft Xbox and Sony PlayStation. Micromachined accelerometers of STMicroelectronics offered the right solution at the right cost and with the proper performances.

After Nintendo, Sony's PS3™ started to use three-axis accelerometers and one-axis piezoelectric gyroscopes of Murata to realize a more anthropomorphic wireless game controller. Right after, same adoption wave was observed in TV, PC, and set top box remote controllers. In July 2007, Logitech announced a controller called Free Air using a combination of three-axis accelerometer from STMicroelectronics and a two-axis gyroscope from InvenSense to simplify the navigation on a display. This controller was the product that declared once forever the death of piezoelectric gyroscope in the consumer market. Since then all Murata gyroscopes have been replaced by a combination of high performance capacitive gyroscopes and accelerometers (also known as six-axis inertial combo) able to fit in less than 10 mm^3 volume and draining less than 500 μA while enriching the user's experience and device usability (Fig. 18.6).

Sensors for Multiple Functions in Smartphones, Tablets, and Wearables

If sensors are used mostly for user interface in game controllers, they enable multiple applications in personal electronics devices, such as smartphones, tablets, and wearables. The overall smartphone industry owes a lot to Nokia for its wide adoption of STMicroelectronics CMOS 5 megapixel sensor and later micro-machined inertial sensors in their phones. In fact, one of the biggest differences between traditional phones, meant only for phone calls, and smartphones is strictly linked to wide use of multiple types of sensors.

After a pale adoption of smaller and more reliable silicon micro-machined bulk acoustic wave filters from Avago and capacitive silicon microphones by Knowles Acoustics,

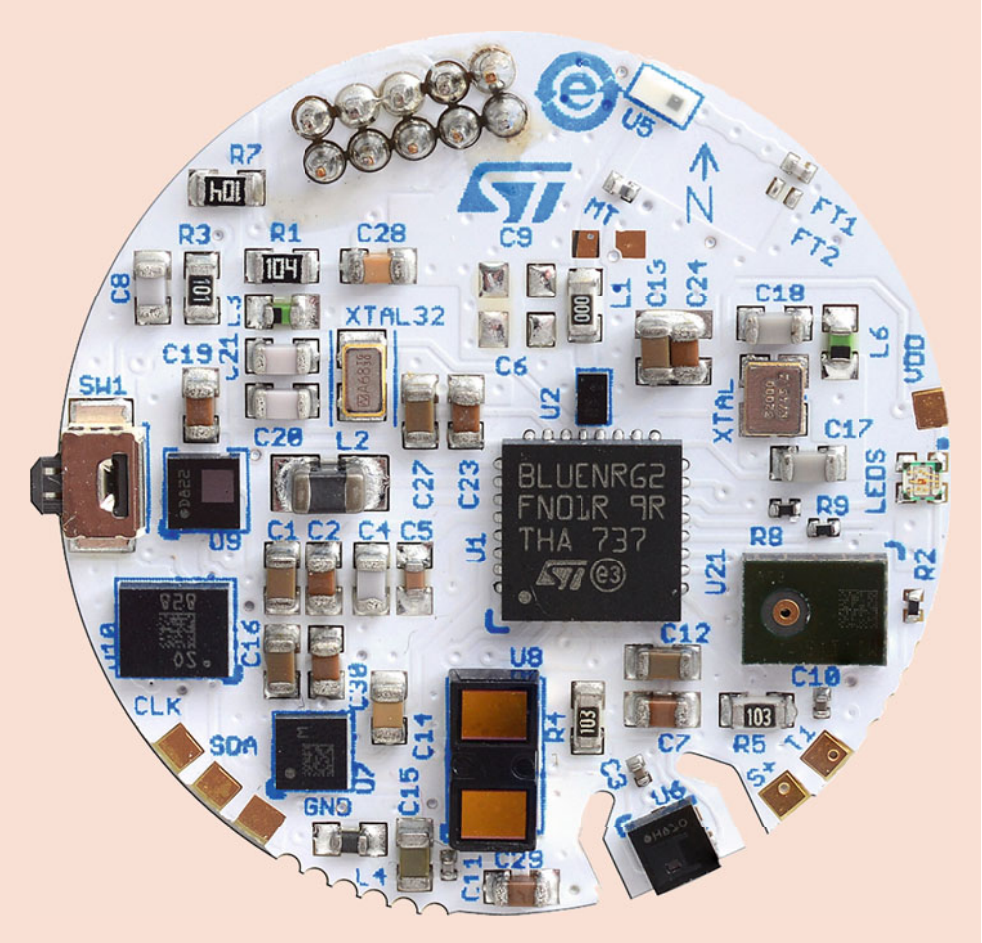

Fig. 18.5 STMicroelectronics BlueNRG-Tile: programmable wireless multi-sensor node. It includes Bluetooth low energy system on chip (center), microphone, humidity and temperature module, time of flight sensor, magnetometer, inertial module, and pressure sensor. (© 2018 by STMicroelectronics)

the big revolution happened in 2006 when three-axis accelerometers were introduced into some mobile phones to simplify the user interface. Initially, this application of sensors was only known to very few people until Apple launched the iPhone™ in June 2007. In this buttonless phone, the accelerometer was key for the new human-machine interface [17]. In fact, the combination of accelerometers, touchscreens, and suitable application software eliminated the need for traditional switches or buttons and thumb wheels for scrolling, zooming, and panning of web pages, e-books, and spreadsheets. The sensors, detecting basic human movements and using them as an input for the mobile phone, allowed passing the limits deriving from the small screens. Nowadays the users can easily navigate through web pages or pan through maps by simply tilting the device in the desired direction. The step from mobile phone to small wearables (like the iPod Nano of Apple of 2009) and big tablets (like the iPad of 2010) was a very easy and obvious one.

However, the pervasion of motion sensors in mobile phones did not stop there, since they started to be used more and more for pedestrian navigation to enable location-based services, so attractive for network operators in constant search of new revenue streams. When navigating

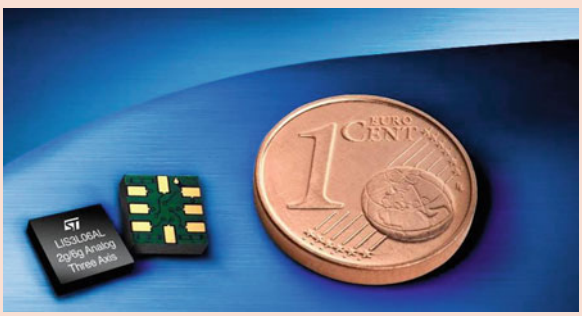

Fig. 18.6 STMicroelectronics LIS3L06AL, first three-axis accelerometer in game consoles, adopted by Nintendo in the Wii. We can also define it as the father of consumer motion MEMS. (© 2018 by STMicroelectronics)

in unknown places, the electromagnetic signals coming from several geostationary satellites and from the cellular network infrastructure can be faded, and thus the GPS function embedded in our phones is not 100% reliable. Tunnels, bridges, and skyscrapers are all obstacles for telecommunications operators who want to sell location-based services such as zone-based advertising and augmented reality experiences. In this context, micro-fabricated low-power and high stability motion sensors can assist and substitute the GPS signal, so that dead reckoning system continues to track people movements. To implement dead reckoning, it is necessary to know the distance and the direction the phone user travelled. An ideal module for personal navigation comprises a three-axis accelerometer plus a three-axis magnetometer plus a three-axis gyroscope and a pressure sensor, everything coupled with the appropriate application software. Often a module like the previous one is also called ten-axis. The accelerometers help to determine the travelled distance and the average speed of the user, the compass picks the heading direction with respect to the magnetic north, the gyroscope measures the change in the direction of user path, and the pressure sensor measures the inclination of travelled path. Emergency services like the E911 in the USA mandate the integration of an altimeter (pressure sensor) in the phone so that in combination with a GPS, it can tell the emergency responders on which floor of the building the caller is. In the last 10 years, many integrated modules have been developed to address this interesting market application, but as of today, we do not have a reliable solution yet. Suppliers are able to deliver highly accurate altimeters and very low-noise magnetic sensors, but we still need a couple of years before we see in the market highly precise and stable six-axis inertial modules suitable to address this long awaited applications. It's also interesting to notice that all the attempts, done by companies such as STMicroelectronics, TDK, and Bosch, to integrate the different sensors in the same modules miserably failed because of the high calibration cost of the final solution. The development of high accuracy six-axis inertial sensors will bring benefits also to future autonomous cars which must rely on digital maps and onboard sensors to navigate in the city jungle.

Before leaving this section, we cannot forget the importance of the sensors in combination with smartphone cameras. If CMOS sensors are used to capture the video and the picture, gyroscopes are used for image stabilization in all medium- and high-end smartphones to avoid blur effects caused by unconscious muscular contractions in the frequency range of few hertz. In the last decade, piezoelectric gyroscopes, mostly manufactured by Japanese suppliers, lost the race against silicon gyroscopes thanks to their smaller dimensions and higher performance in terms of sensitivity and stability. Moreover, silicon gyroscopes can measure angular rates along the pitch and roll axes simultaneously, and, thanks to their reduced dimensions, they can be integrated more easily in the camera module itself (Samsung S8™ smartphone). Last but not least, silicon gyroscopes are sold already calibrated, and thus the final product manufacturer does not have to waste time and money to calibrate the final system, i.e., the full smartphone.

18.2.3 The Internet of Things Era

Micro-fabricated sensors start to be widely utilized in numerous applications both in the industrial and medical market space. Smart factory automation, condition monitoring for preventive machine diagnostics, asset tracking for more efficient logistic services, optimization of water and energy consumption of household appliances, continuous monitoring of people activity, and ambient assisted living are just a few examples of applications in these two markets [18, 19].

Wireless Sensor Networks

Starting from 2013, in the field of wearable electronics , first Fitbit and later other companies like Apple announced products embedding sensors of different types in their watches. The accelerometer was the first sensor used to measure the physical activity; later it was the time of the light sensors to measure the body's function through blood oxygen content measurement. Recently two-lead electrocardiogram (ECG) appeared in the Watch 4 series. Some cardiologists have raised concerns about two-lead ECG: according to them, it is unnecessary for the general population, or it could cause problems, including false positives. At the best, they say, that could result in stress for users and unnecessary visits to doctors, further burdening an increasingly sluggish healthcare system. Even worse, false positives could also lead to unnecessary follow-up tests with the costs and health risks those tests can involve [20]. The next steps are noninvasive glucose monitoring. Several companies are busy in developing and selling add-on devices from blood pressure monitor to a sleep-aiding headband. Last 2019 Consumer Electronics Show in Las Vegas hosted many companies working on digital health. However, mental health has strong impact on blood pressure and ECG readings and thus on a person's overall well-being. Thus, several cardiologists are questioning the usefulness of continuous monitoring in consumer wearable gadgets. The authors share the same concerns.

Global healthcare spending is estimated to reach almost $9 trillion annually by 2020, and this is the field where smart sensors can make a big difference. We will all discover the future of medical wearable devices in the course of next decade; the authors do not have doubts about the successful market adoption of medical-grade wearable devices. It will take time, but it will happen. Figure 18.7 represents an

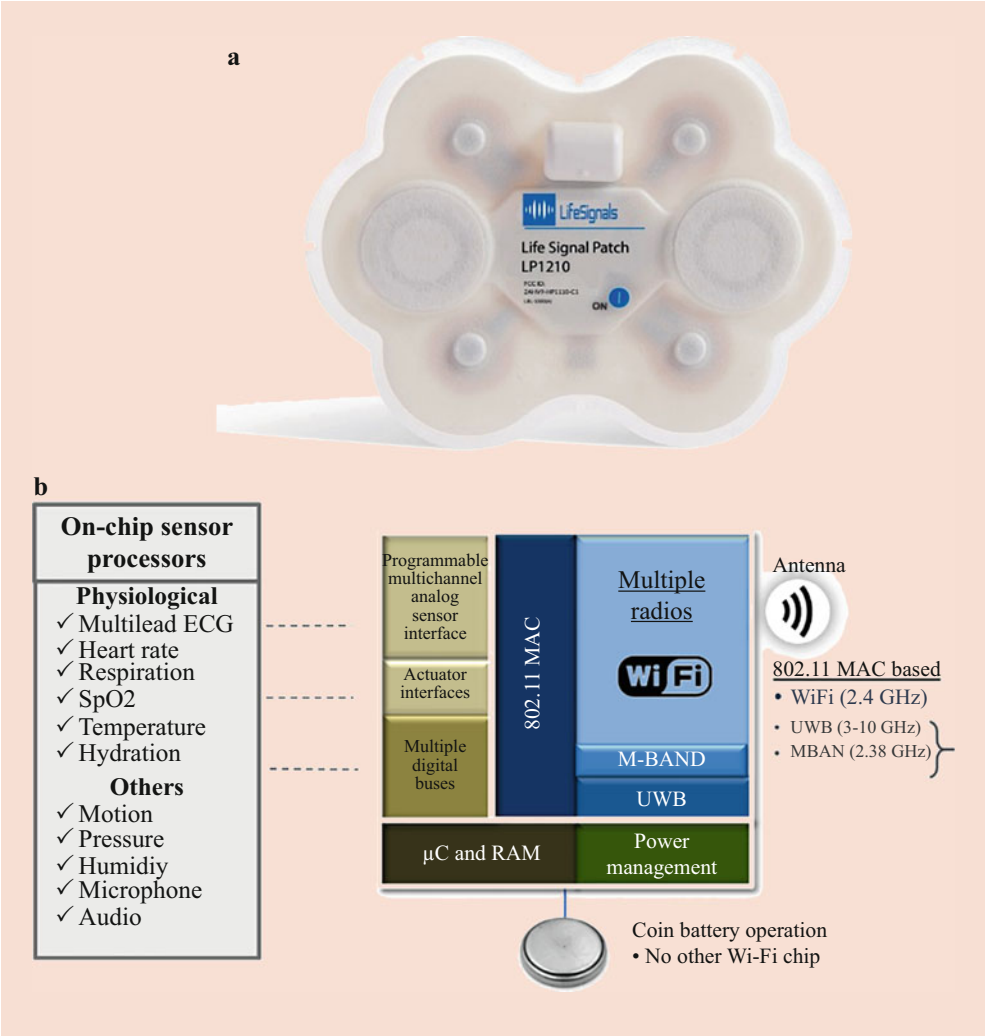

Fig. 18.7 (**a**) LifeSignals ultralow-power wireless patch for professional-grade electrocardiogram (ECG) that can operate with a cheap zinc-air battery at 1.2 V. (**b**) Lifesignal silicon processor chip for patches schematic. (© 2018 by LifeSignals)

ultralow-power wireless patch for professional grade (ECG) developed by Californian start-up LifeSignals in cooperation with STMicroelectronics in the last 5 years [21].

Beyond this growing and essential healthcare market, sensors will leave a sign in the new generation of home and factory robots, including the cobots, and the autonomous cars, enabled by artificial intelligence. The recent market trends in electrification, digitalization, and automation will require more and more the deployment of wireless sensor networks, which today are still in their infancy. A wireless sensor network results from the combination of different wireless sensor nodes (mote), consisting of some combination of a sensor, a microcontroller, a wireless receiver, an antenna and a battery, or even better, an energy scavenger. The potential market for motes is limited only by our imagination, and as soon as overall power consumption of the mote will be lowered (big current technological hurdle), motes will ultimately become a natural part of our lives. Their potential applications range from security and bio-detection to building and home automation, industrial control, pollution monitoring, and agriculture. Moreover, rising concerns for safety, convenience, entertainment, and efficiency factors, coupled with worldwide government regulations in terms of security, could boost sensor usage to unprecedented levels, although not all of them necessarily silicon micro-fabricated. In fact, motes will have to measure real-world variables such as pressure, temperature, heat, flow, force, vibration, acceleration, shock, torque, humidity, and strain as well as capture and record images in the visible and near-IR range. Suppliers must be ready to integrate different technologies in a modular format as well as to achieve high-volume manufacturability of motes. Most of the transducers, with the exceptions of the CMOS image sensors, are coming from advanced 8″ fabs, while the rest of the active silicon components is fabricated in state-of-the-art 12″ fabs. Then, system in package solutions allow a modular and flexible integration of the different

components in a miniaturized and compact module. It is of course not clear which exact application will win in the long run, but it is clear that different new sensors, currently being developed by many companies and research centers, will enable a lot of new applications, driving new revenue streams.

3-D Sensing Solutions

The evolution toward complex stereographic representation or data analysis, for mapping and sensing the surrounding reality using near-infrared (NIR) wavelengths, is now a clear trend in medical, automotive, factory automation, home security, communication, consumer, food, and entertainment markets. 3-D sensing solutions aim to estimate the distance between the object and the sensor. A basic classification of present 3-D sensing solutions (excluding medical diagnostic systems and non-photon-based sensors) are:

- Stereo vision: including active and passive stereo vision, with small volumes in professional industrial applications.
- Structured light (SL): presently widest market adoption through iPhone or professional 3-D scanning systems and originally used by Kinect 1 of Microsoft.
- Time of flight (ToF): including direct (dToF) and indirect time of flight (iToF), with limited volumes in professional industrial applications and growing in automotive for both in-cabin driver monitoring and autonomous driving applications. Kinect 2 of Microsoft represents the highest volume market application of iToF (Fig. 18.8).

Stereo vision and structured light are based on triangulation methodologies and thus they are geometric methods. By triangulation, they estimate indirectly the depth of the scene, calculating the unknown distance knowing the baseline (distance between the two cameras) and focal length. Precise knowledge of the baseline, and therefore precise optical assembly, is key for this methods. Stereo vision is clearly close to human stereographic view, where brain elaborates the signals coming from the two eyes and is able to discriminate 3-D scenarios from pictures and 2-D images. Stereo view works best when the observer is in motion. Geometric systems are on top affected by parallax error (perception of the object depends on the point of view), due to the intrinsic triangulation-based measurement: this issue creates mismatch in object identification. Moreover, depending on the geometry of the object to be measured, there could be mistakes linked to the conic or occlusion shadows, with a consequent misidentification of the shapes and the depth.

Time of flight, instead, is an electronic method that provides a direct measurement of depth without relying on geometrical assumptions. Electrical quantities of the signal, like phase or time delay, are processed to yield a depth value that is independent on the spacing between the components in the system and therefore is compatible with a more relaxed assembly tolerance. Typically, the challenges are signal-to-noise ratio, reaction time, and signal path delays. The advantages are related to the lack of intermediate calculation for geometric systems: electronic methods are simpler, require lower computational power and lower calibration effort, and have lower costs.

All the three 3-D solutions require an application processor. Structured light and time of flight systems require also a light source with related analog drivers. This light source is, in most cases, an IR VCSEL light emitter. In order to avoid the use of visible light, a wavelength of about 950 nm is normally used. Longer wavelength can be chosen to increase the safety for eyes but also to increase the depth of scan, as in the case of LIDAR or RADAR, used in the premium cars.

3-D sensing solutions are bundled with other sensors (inertial sensors, CMOS image sensors, etc.) to move from 3-D to 4-D or synchronous localization and mapping (SLAM): a system that is capable to explore and map an unknown environment while simultaneously keeping track of a subject interacting with and inside that environment. SLAM represents the next step toward virtual reality, autonomous navigation and driving, and next-generation robots and cobots, as showed in Fig. 18.9.

18.3 Micro-sensor Classification and Terminology

Every day we deal with several different types of silicon sensors using several materials (monosilicon, polysilicon, silicon oxide, silicon nitride, etc.) and manufactured with different microfabrication processes. Despite all this variety, sensing the real world always requires dealing with physical variable inputs to be converted in electrical signal variable output. This electrical signal is typically processed in some way, e.g., amplified and/or filtered, and either transmitted, stored, processed further, or converted into a human-readable form, e.g., used to drive an optical display (as shown in Fig. 18.10).

18.3.1 Classification

There are many possible ways to classify the different types of micro-sensors. They can be easily grouped in analog (voltage) or digital (bit stream) sensor families, just looking at the format of their electrical signal output. Moreover, considering that the two key blocks (transducer and electronic processing chip) of a micro-sensor can be realized on the same die or on multiple dice, a classification based on the microfabrication process architecture is also possible. Thus, we can classify sensors in three classes:

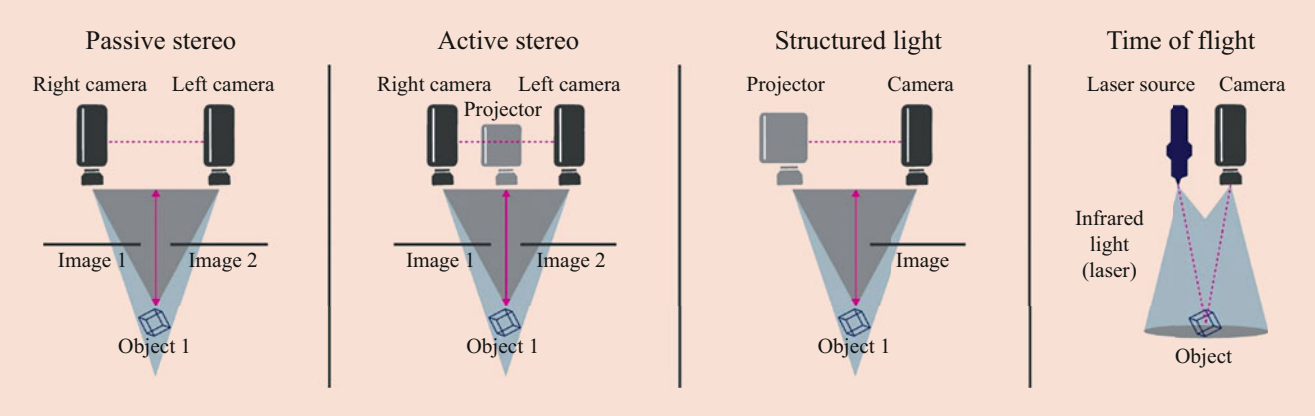

Fig. 18.8 Main 3-D sensing solutions. (© 2018 by STMicroelectronics)

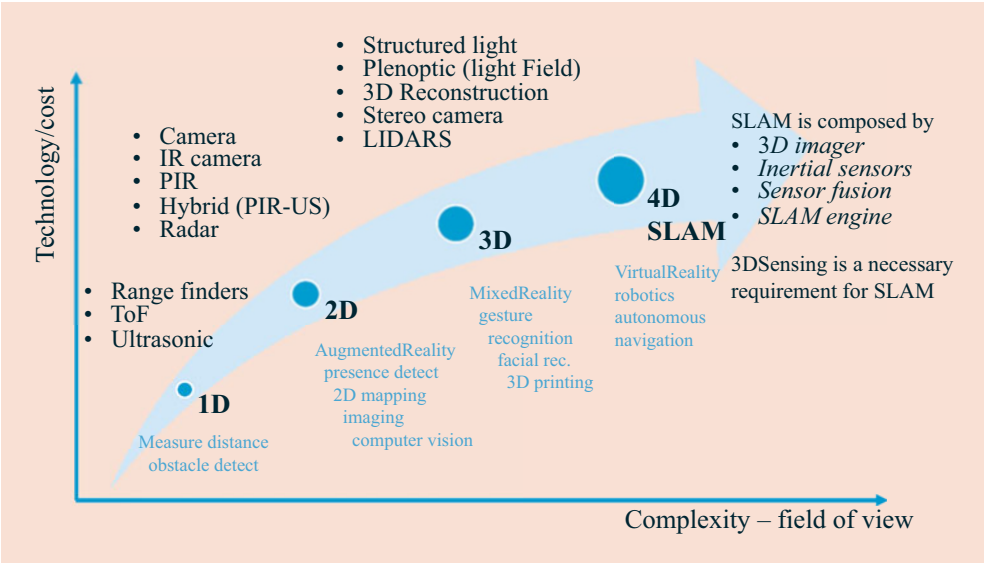

Fig. 18.9 Adoption of 3-D sensing solution across different market applications. (© 2018 STMicroelectronics)

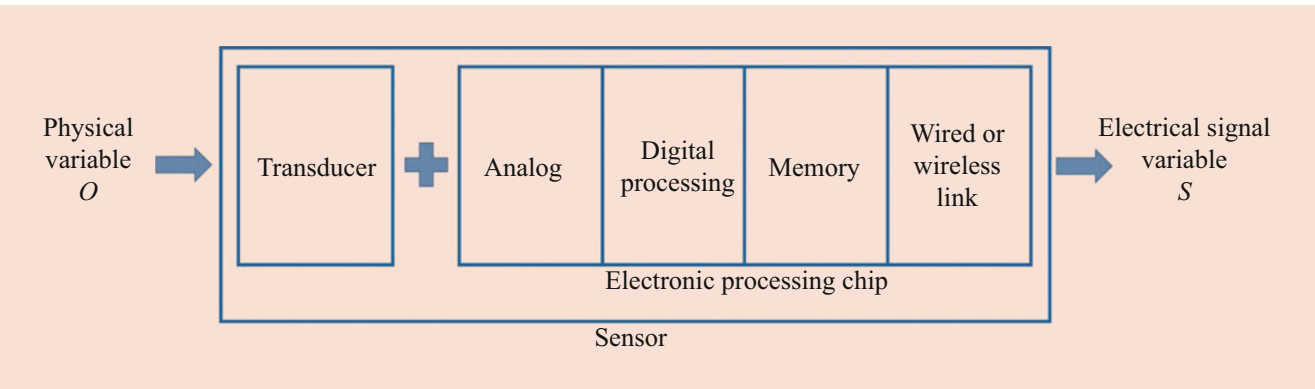

Fig. 18.10 Schematic representation of the transduction and elaboration processes inside a sensor. (© 2018 STMicroelectronics)

1. CMOS monolithic, like the Hall effect sensors of Allegro or the ambient light sensors of AMS or the humidity sensors of Sensirion. The fabrication steps can precede the regular CMOS process (pre-CMOS, like the VENSENS™ process of STMicroelectronics) or follow it (post-CMOS, like the humidity sensors of Sensirion) or can be per-

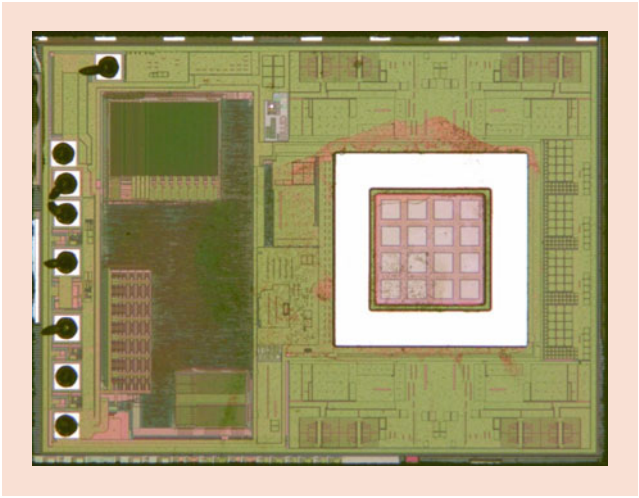

Fig. 18.11 Optical view of AMS color and proximity sensor, realized with CMOS monolithic. (© 2018 ALS and proximity sensor comparison by System Plus Consulting)

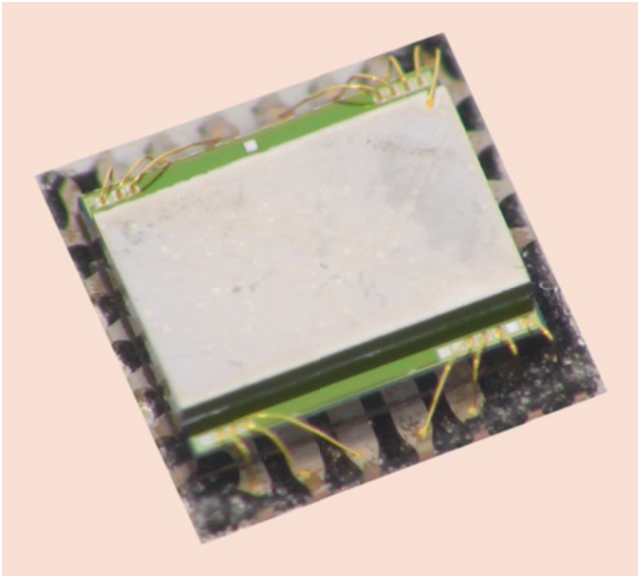

Fig. 18.12 Optical view of InvenSense MPU6500 six-axis inertial measurement unit (IMU): CMOS stacked structure is adopted, with MEMS sensor bonded on top of application-specific integrated circuit (ASIC) with wafer-to-wafer bonding. (©2013 InvenSense MPU6500 six-axis IMU by System Plus Consulting)

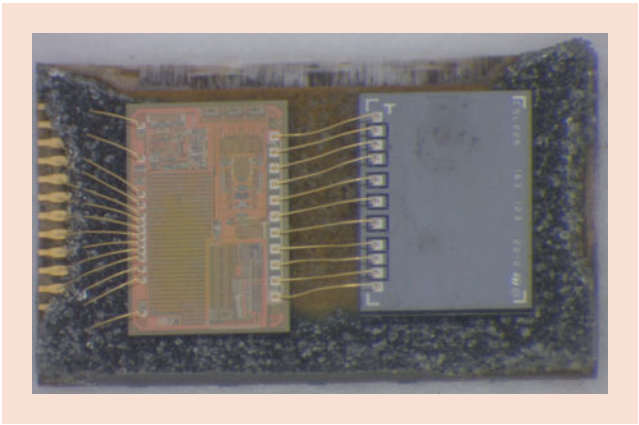

Fig. 18.13 CMOS hybrid: optical view of STMicroelectronics three-axis accelerometer LIS302DL with MEMS and ASIC side-by-side and wire bonded. (© 2017 MEMS Packaging Reverse Technology Review by System Plus Consulting)

formed in between the regular CMOS steps (intermediate CMOS, like the accelerometers of Analog Devices or the Hall effects of Melexis). In the last 20 years, we saw the market failure of many sensors belonging to this class. Akustica microphones are just one example.

2. CMOS stacked, like the gyroscopes of TDK/InvenSense or the backside illuminated CMOS image sensors of Sony. In this case, the wafer containing the different type of transducers is processed separately, and later it is bonded to one or multiple CMOS standard wafers containing the processing electronics by means of wafer-to-wafer metal bonding technologies (aluminum germanium and copper-copper alloys are the most widely used metallurgies).
3. CMOS hybrid or heterogeneous, like the six-axis of STMicroelectronics and Bosch or the microphones of Knowles Acoustics and Goertek. In this case, the transducer itself and the processing electronics reside on two different silicon dice, and later they are connected inside the same package thanks to standard copper or gold wire bonding technologies (Figs. 18.11, 18.12, and 18.13).

Besides the classification criteria suggested above, a convenient way to classify the several types of sensors is in terms of the type of energy they transduce (e.g., mechanical, thermal, and magnetic) into electrical energy. If we exclude nuclear energy and electrical energy (which does not require any transduction), we can distinguish between five basic energy types: mechanical, thermal, radiant, magnetic, and chemical, as detailed in the table below with related example sensors (Table 18.2).

An alternative way to classify electronic sensors is in relation to the conversion process itself. Two categories can be identified: direct/self-generating/active sensors and indirect/modulating/passive sensor. A direct sensor converts one form of energy directly into an electrical signal. For example, a photodetector converts photons (optical energy) into a current and a thermocouple converts radiation into a voltage.

In an indirect sensor, instead, the physical parameter of interest modulates an electrical signal. Time of flight, capacitive, or piezoresistive sensors are a good example. Resistive sensors, for example, are typically biased with a constant voltage, so that the change in resistance due to a change

Table 18.2 Classification of physical parameters and sensors according to the type of energy they convert

Energy	Parameter	Physical effect	Example sensors
Mechanical	Position, velocity, acceleration, force, stress, pressure, strain, torque, stiffness	Piezoelectric, piezoresistive, capacitive, inductive, optical	Accelerometer, strain gauge, load cell, switch, motion sensor, touch sensor, mass flow sensor
Thermal	Temperature, heat flow	Seebeck effect, thermo-resistance, pyroelectricity, thermal noise	Thermal couple, thermal resistance
Radiant (Optical/EM)	Light intensity, wave length, refractive index, polarization, phase	Photoelectric, photovoltaic	Photodiode, photo transistor, photomultiplier tube, position-sensitive detector, CCD
Magnetic	Magnetic field, magnetization	Magnetoresistance, inductance, hall effect	Compass, position, speed sensor
Chemical	pH, humidity, chemical/bioagents, gas	Potentiometry, conductometry, amperometry	pH sensor, gas sensor, humidity sensor

in the parameter of interest (e.g., strain, magnetic field, temperature) results in a modulation of the current flowing through the sensor. In general, modulating sensors are used for the measurement of very weak signals.

Many sensors use displacement sensing to measure a mechanical signal directly, such as acceleration, yaw rate, or sound pressure. Displacement sensing is the most highly developed areas in the field of micro-machined sensors because it can be applied so widely and it is relatively straightforward to implement. All the micro-machined sensor examples provided later in this chapter employ displacement sensing techniques such as capacitive, piezoresistive, and piezoelectric. A detailed explanation of these basic sensing techniques will be provided in Sects. 1.6, 1.7, 1.8, 1.9, and 1.10 in conjunction with the related sensor exploiting it.

Commercially successful micro-machined sensors, also known as MEMS sensor, include accelerometers, gyroscopes, microphones, and pressure sensors. All these micro-machined sensors are passive and detect the physical input signal of interest by means of resistive or capacitive variation induced by a displacement. We do not have yet on the market any commercially successful example of micro-machined sensor measuring an inductive change. Many papers are also published about micro-machined resonant sensors, but authors of this chapter believe that 2 or 3 additional years are needed before having some commercially relevant market examples.

18.3.2 Terminology

There are some key parameters common to all sensors that are specified in their datasheets and have a relevant role in the price of the sensor itself. The reader can find a comprehensive review of sensor terminology in many specialized books like Ref. [7]. The intent of this section is to clarify the meaning of the most critical parameters of any sensor, parameters that often are confused or misused.

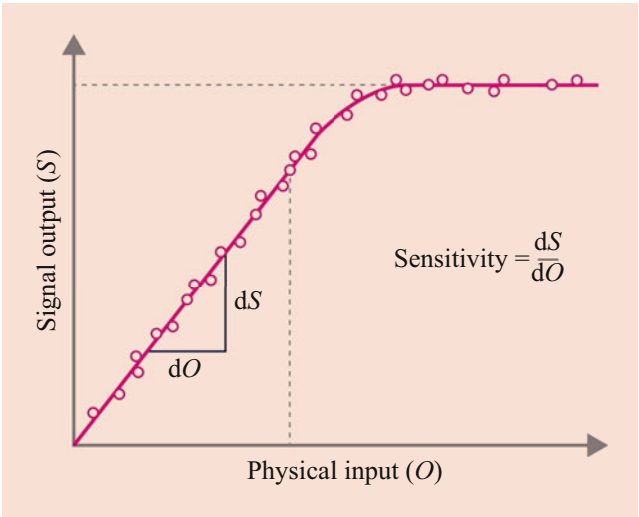

Fig. 18.14 Schematic representation of a calibration curve with illustration of the concept of sensitivity. This example curve has a good linearity in the first part and then deviates from linearity. (© 2018 by STMicroelectronics)

Calibration: Any sensor, before to be used, must be calibrated, so to ensure its correct behavior during its utilization. In fact, the calibration enables to determine the correct relationship between the physical variable input O (observable) and the signal variable output S. The calibration procedure requires the use of a well-known physical input to the sensor and recording the output on a calibration curve accordingly.

Scale factor, most commonly known as *sensitivity,* is the slope of the calibration curve, i.e., dS/dO.

Nonlinearity is the systematic deviation from the straight-line relation between O and S, i.e.,

$$S = \text{sens} * O + \alpha \tag{18.1}$$

where α is the offset, usually compensated (Fig. 18.14).

Dynamic range is the ratio between the smallest $O_{\min}$ and largest physical inputs $O_{\max}$ that can be reliably measured by the sensor.

Resolution is the smallest variation of the measured quantity O that can be detected. Resolution is an important property of the sensor and higher resolution implies smaller minimum difference between two measurements. Often higher resolution is synonymous of higher precision.

Accuracy and precision of the sensor are, maybe, the two most important concepts describing the quality of the sensor itself and making it more or less suitable for the final application.

Accuracy, also called bias in the literature, describes the closeness between the true value of the measurand O^{True} and the measured value indicated by the sensor O^{Measured} [7]. The difference between the true value of the measurand and the measured value indicated by the sensor is called error.

$$\text{Error} = O^{\text{True}} - O^{\text{Measured}} \tag{18.2}$$

The higher the accuracy, the lower the error. Typically, the true value is defined in reference to some absolute or agreed upon standard. Accuracy is especially important when the user is interested in estimating the true value and is less important when measurement repeatability is the critical issue. Common synonyms include bias, systematic error, and trueness, albeit ISO has a different definition of accuracy from the common scientific usage.

Precision, also referred to as variability, describes the closeness of agreement between experimental measured values O_i, obtained by replicating measurements of the same quantity O under specified conditions. Measurement precision is usually expressed numerically by way of standard deviation. Some measurements require high precision, i.e., small variability in the measurement, and may tolerate a constant offset with respect to the true value, which in most cases is easily detectable and removable during the calibration procedure by means of compensation. Common synonyms are precision, jitter, variance, and standard deviation.

Figure 18.15 exemplifies the two concepts in the case of multiple measurements of a certain quantity O, distributed according to a Gaussian probability density function. Accuracy is the difference between the average O^{Measured} of the different measurements and the true value O^{True}, while precision is the measurement variance.

The lack of accuracy and precision of the sensor can be quantified by two types of errors in the measurement data: systematic errors and random errors, respectively [7].

Systematic errors occur always with the same value when acquisition and environmental conditions remain the same. They are predictable and once identified they can be removed through a compensation process.

Random errors are associated with different measurements and can be characterized by a mean and variance value. The variance can be reduced in general by averaging multiple measurements, while the mean can be incorporated with systematic errors, since the central limit theorem ensures that random errors tend to be normally distributed when many independent variables are added together.

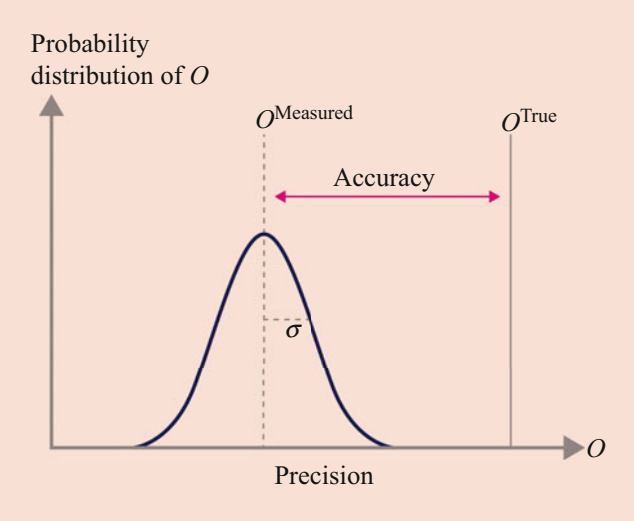

Fig. 18.15 Schematic representation of the concepts of accuracy and precision in a measure. (© 2018 by STMicroelectronics)

18.4 Microfabrication and Micromachining

Miniaturization of sensors thanks to microfabrication technologies typically results in improvements in the response time and the sensitivity of a device and in a reduction in the power consumption. Additional benefits of using micro-fabricated sensors are size, cost reductions, increased performances, improved reliability, and the possibility to integrate electronics directly in the devices, enabling even further reductions in size and cost. Last but not least, micro-fabricated sensors enable the integration of several different sensors on the same platform so that physical quantities can be measured simultaneously and the sensor becomes more accurate. Integration of a temperature sensor is a typical example, where the simultaneous measurement of the signal of interest and of the temperature can increase the accuracy of the overall sensor, thanks to an improved temperature compensation.

Perhaps one of the most powerful concepts facilitated by micro-fabricated sensor technology is that of massive parallelization thanks to either batch manufacturing techniques or possibility to integrate many equal sensors on a silicon die (like the CMOS image sensors). In the past, data describing the spatial variation of a parameter of interest was typically acquired by taking a single sensor and raster scanning it over the area of interest. The main drawbacks of this technique are the complexity involved in positioning the sensor and the time required to acquire the data. An alternative approach is to build an array of identical sensors and use them to

simultaneously acquire an image of the spatial variation of the parameter of interest. This concept has been exploited very effectively in optical imaging devices, such as the image sensor arrays currently found in all the smartphones. Some recently announced phones like the Samsung S10 include up to six cameras.

As we anticipated in the previous section, depending on the CMOS integration level, we have three classes of microfabricated sensors: CMOS monolithic, CMOS stacked, and CMOS hybrid/heterogeneous. The first two classes are also referred to as system on chip (SoC), while the last one is more commonly known as system in package (SiP). In the last 20 years, the market success of SiP approach versus the SoC one has been the subject of many time-consuming speculations written in many technical papers and specialized books and even debated in international conferences attended by experts and/or by financial market analysts. Each company has been arguing the intrinsic benefit of its own process selection. A posteriori all of us can admit that all these discussions were useless. Today most of commercially successful micromachined sensors follow the SiP approach, mostly because of flexibility in the choice of the best process and development time, while temperature sensors, Hall effect, ambient light sensors, and CMOS image sensors use the SoC approach.

Most of the silicon microfabrication processes were developed for the integrated circuit (IC) industry. Processing techniques such as lithography, thin film metallization, photoresist patterning, and chemical etching have found extensive use in the fabrication of micro-sensor. The ability to mass-fabricate many of these sensors on a single wafer (batch processing) using currently available semiconductor processing techniques helped to decrease the unit fabrication costs significantly and to manufacture sensors with increased reproducibility of response.

By combining these two-dimensional processes with three-dimensional micromachining technology, three-dimensional structures can be formed. Different micromachining techniques are available: surface/epitaxial techniques allow fabricating transducer masses with thickness from few up to 100 μm; bulk methods allow the realization of masses with thickness greater than 100 μm.

The techniques used in silicon micromachining fabrication include two key steps:

1. Chemical anisotropic and dry etching. Chemical anisotropic etching is an etching procedure that depends on the crystalline orientation of the substrate. For silicon etching, potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH) solutions are most commonly used as etching agents. Dry etching processes include ion milling, plasma etching, reactive ion etching, and reactive ion beam etching. These dry etching processes are not dictated or limited by the crystalline structure and thus enable greater freedom in the design of the sensor. The SF_6 dry etching process invented by Laermer et al. represents a big step forward in micro-sensor development [22].
2. Sacrificial layer method. The active structure is fabricated on a sacrificial layer that is subsequently chemically removed. In this way, the active structure becomes free to move.

18.5 Microsystem Back End

A microsystem is the combination of electrical and nonelectrical function. As we have seen in the previous section, some suppliers integrate the two functions on the same silicon die, while others use two separate silicon dice. These dice may be placed in different ways inside the package itself: stacked or side-by-side as shown in Fig. 18.16. Almost 12 years ago, the use of full molded packages enabled a strong cost reduction of micro-machined accelerometers and thus a wider consumer market adoption. Nowadays, while the package of physical sensors, like magnetic, inertial, and CMOS sensors, is very much cost-optimized, the same does not apply to chemical sensors, like gas sensors. The goal of research and development activity in this field is to continue to move MEMS packaging out of the jewelry space of custom solutions toward standard production rules and controls. The ultimate goal is to minimize manual interventions through utilization of automatic equipment and to lower the bill of material. This step is mandatory to increase both the level of global production and level of quality.

In the last decade, many attempts have been done to move standard wafer-level manufacturing steps to back-end plants (plants running assembly and testing operations). Many great innovative ideas, like package on package (PoP), fan-out, wafer-level molding, bare silicon, and thru-silicon vias (TSV), were proposed in the last decade, but although their beauty and elegance, most of them remained limited in volumes, mostly because of cost reasons. This does not mean they will not resurrect and find their way to the high-volume market, but as of today most of the sensors continue to be assembled with standard assembly processes (Fig. 18.17).

Assembly refers to the collection of industrial processes that are used in a specific sequence to create a package housing of the sensor. Packaging is the process of enclosing the sensor inside a package. The role of the package is to offer a proper interface between the sensor and the printed circuit board, on top of which it is soldered, while providing mechanical and environmental protection, to guarantee reliable operation during all its lifetime.

Testing is the sum of all electrical and nonelectrical tests performed to verify product functionality and to calibrate it properly. Calibration is an important step required by all

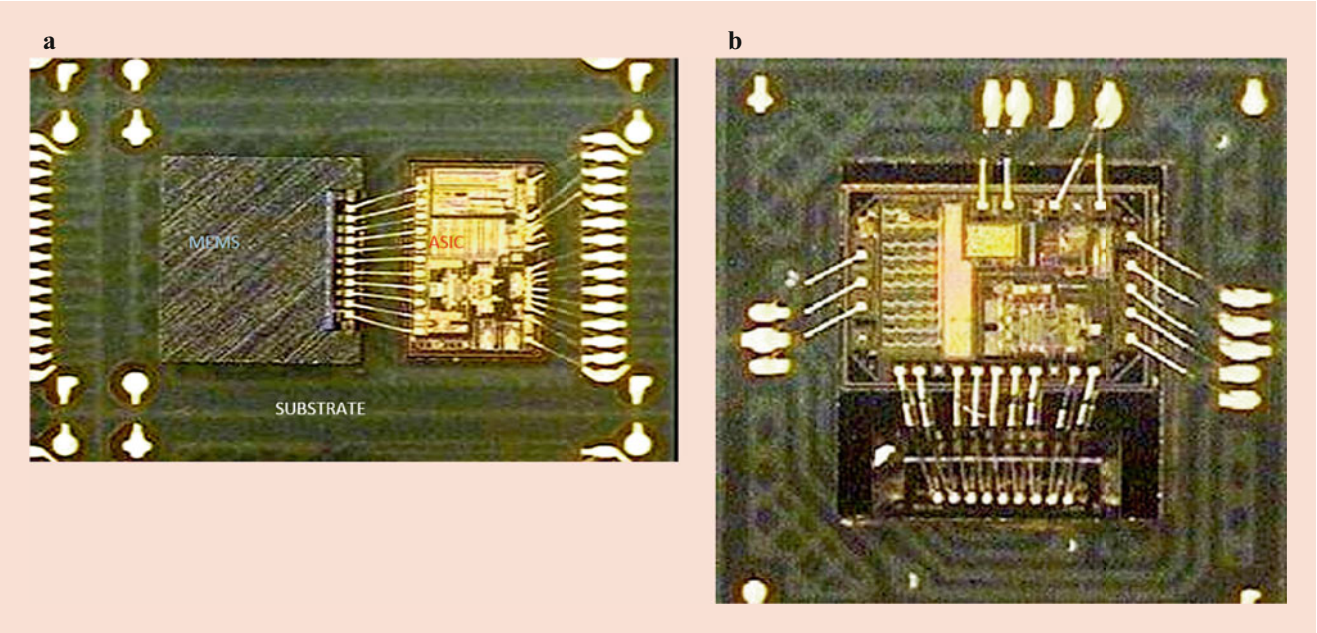

Fig. 18.16 (**a**) STMicroelectronics IMU, example of side-by-side chip configuration. (**b**) STMicroelectronics IMU, example of stacked chip configuration. (© 2018 by STMicroelectronics)

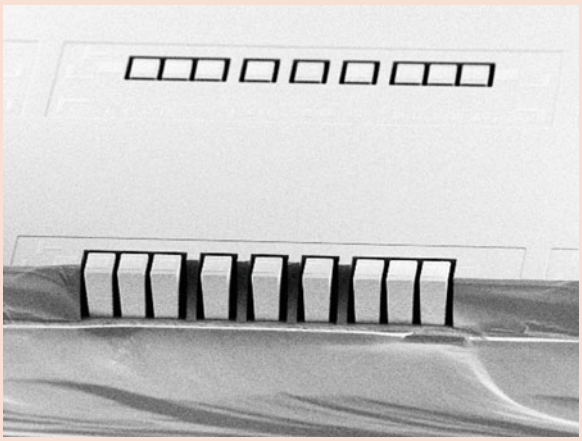

Fig. 18.17 Cross section of a wafer showing thru-silicon vias (TSV) in STMicroelectronics IMU. (© 2018 by STMicroelectronics)

kind of sensors. As explained in Sect. 18.3.2, the calibration curve is key for the usefulness of the sensor itself in the final application. No calibration, no sensor!

Packaging and calibration are extremely important for the sensor performances. Microfabrication technology can enable the best ever sensor performances, but then a wrong selection of the package and/or inaccurate calibration can make the sensor not adequate to its use in the final application. Packaging and calibration of sensors depend largely on the application and on the different type of sensors. For a more detailed discussion of sensor packaging, the reader is referred to Ref. [23].

18.5.1 Micro-sensor Assembly and Packaging

Silicon sensor assembly techniques are mainly derived from those developed for microelectronics . In contrast to integrated circuits (IC), where the package protects the electronics device from the outside world, the sensor package sometimes may need to provide direct physical interaction with the external world. At the same time, package protects the sensor from damage or failures in the assembly line and in the field. According to the different types of sensor packages, three classes can be identified:

1. *Hermetic* packages are intended to protect chips from external environment agents (i.e., particle contamination, moisture-induced corrosion, and stiction) that can prevent the devices from properly working. Inertial sensors, such as accelerometers and gyroscopes, and bolometers are examples of devices that require hermetic packages. In the 1990s ceramic packages were the only possible solution for hermetic packages. This was the case for the accelerometers of Analog Devices, mainly for automotive applications. With the dawn of the sensor consumerization wave, cost-effective solutions based on plastic full molded packages started to appear on the market (i.e., the accelerometer of STMicroelectronics LIS3L02AL used in the Nintendo Wii™ game console), and now full molded plastic land grid array (LGA) package is the standard for inertial sensors. If the package of inertial sensors evolved so much in the last years, the same cannot be said for the bolometers, where only shy attempts of new package

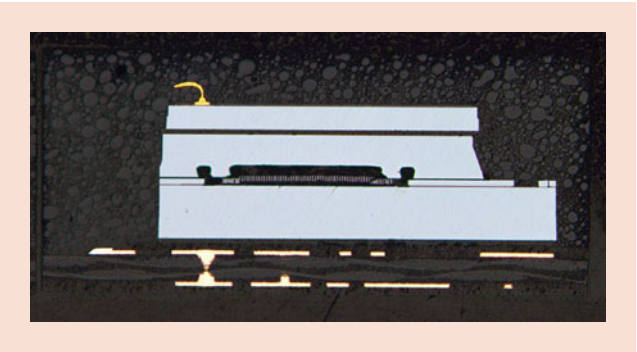

Fig. 18.18 Cross section of a STMicroelectronics inertial module. LGA substrate is visible at the bottom, with sensor in between and ASIC on top. MEMS die is made of a sensor wafer (on top of which suspended mass can be seen) and a cap wafer. Wafer-to-wafer bonding guarantees hermeticity inside sensor die. (© 2018 by STMicroelectronics)

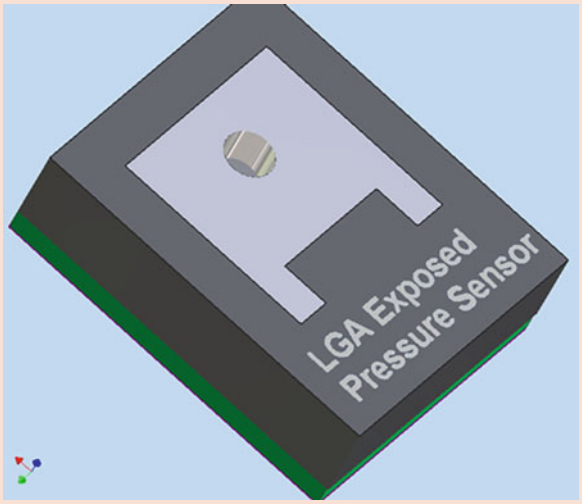

Fig. 18.19 Drawing of a holed land grid array (HLGA) package for STMicroelectronics pressure sensor. (© 2018 by STMicroelectronics)

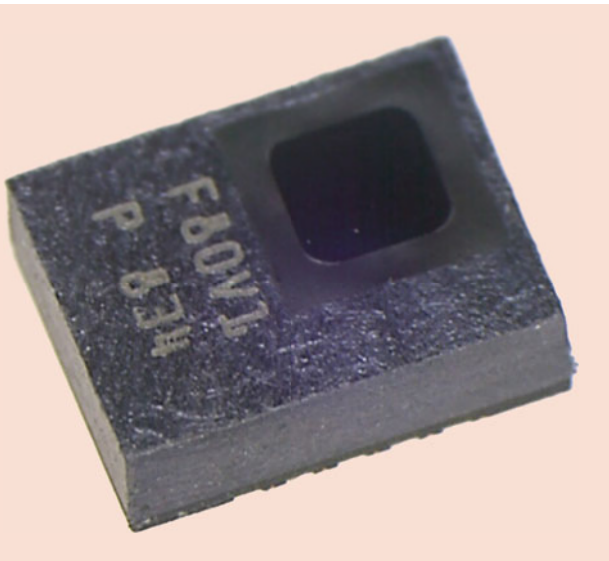

Fig. 18.20 STMicroelectronics optical sensor in plastic package with embedded IR window. (© 2018 by STMicroelectronics)

evolution can be found. Hermeticity of the package is usually guaranteed by low melting point glasses (glass frit) or metal alloys used to join two or more silicon wafers. Alternative techniques include high-voltage high temperature anodic wafer-to-wafer bonding, like the pressure sensor used in tire pressure monitoring systems of Infineon.

2. *Open* packages provide an interface between the sensor and the external world through one or more inlets. Typical examples of open package MEMS sensors are pressure sensors and microphones. Open packages are required whenever the external stimulus requires close physical or chemical contact with the transducer part of the sensor. Moreover, most of open packages are highly customized to fit the specific application they are designed for, and, thus, they involve special manufacturing designs and equipment. The manufacturing industry is still far from the standardization wave that involved hermetic sensor class, but the introduction of the holed land grid array (HLGA™) package of STMicroelectronics pressure sensor in 2013 represented the dawn of a standardization era also for pressure sensors.
3. *Semi-hermetic* packages are in the middle between hermetic packages and open packages. They do not have any inlet, but, being not hermetic, humidity can enter easily, and thus this kind of package is not suitable for stiction-prone sensors with a sensing element containing moving parts. Temperature sensors, magnetic sensors, and optical sensors, all without moving parts, fit into this category of packages (Figs. 18.18, 18.19, and 18.20).

Apart from the functional classification of the different kinds of packages, another fundamental difference exists in the material employed for the package: ceramic and plastic. In the plastic package family, a further difference can be made between full molded and pre-molded packages.

Though the full molded packages are cheaper and more easily scalable in high volume, nowadays there are many different packages on the market, depending on the requirement of the sensor itself.

Today, the manufacturing of high-volume micro-sensors is linked to the use of molded packages. In the field of consumer-related products, the only cost-effective and volume-scalable solutions for inertial sensors are full molded plastic packages. In the late 1990s, lead-frame solution packages based on SOIC (small outline integrated circuit) packaging were the first approach for mass production

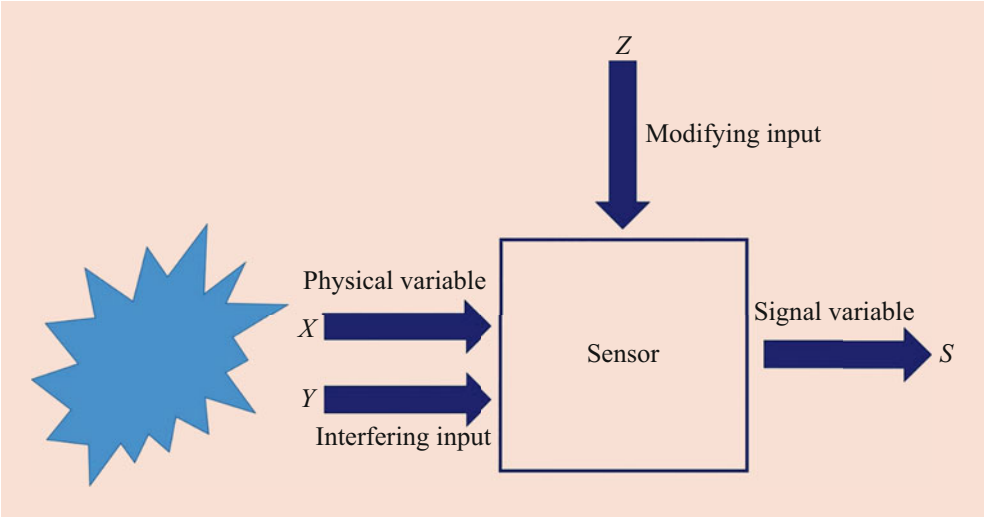

Fig. 18.21 Illustration of how interfering and modifying inputs may affect negatively the calibration curve of the sensor. (© 2018 by STMicroelectronics)

of a full molded package for accelerometers; later, LGA definitely became the standard solution.

MEMS sensors can be capped one by one in the packaging line or directly at wafer level in the clean room with wafer-to-wafer bonding technology process. Glass frit, a low melting point glass, is the most common technique used to seal the microstructure at wafer level. In the 1980s and 1990s, the inertial sensors were assembled and sealed one by one in ceramic hermetic packages, but since this approach did not scale well in mass production and since it induced quality issue (stiction) in the market, it was replaced by a wafer-level low-cost reliable technique, which is now employed by all large MEMS silicon manufacturers [23]. STMicroelectronics and Bosch use it for all their inertial sensors. For this full molded low-cost package transition, several technical challenges were successfully overcome at design level to gain performance in terms of thermal stability (over the required temperature range) and time stability (over the device lifetime), due to changing conditions in humidity and mechanical stress coming from the application board. Sensor suppliers keep experimenting innovative ideas to increase overall accuracy.

18.5.2 Micro-sensor Testing and Calibration

Testing equipment for sensors is designed to provide known physical stimulation to the packaged microsystems. Linear accelerometers must be calibrated by applying an external linear acceleration (measured in units of g, the Earth's gravity acceleration); gyroscopes require the application of an external known angular rate (measured in degree per second, known also as dps); CMOS image sensors require the application of an external known optical source.

While, for standard integrated circuits testing, the equipment apply only an electrical stimulus, the specificity of sensors testing is due to the need of applying to the device a nonelectrical signal. Therefore, a sensor handler is different from any traditional integrated circuit handler. In fact, the device under test (DUT) board must be properly designed to minimize the impact of the interfering or modifying inputs on the calibration curve. (See Fig. 18.21.)

Thus, the handlers and sockets must be customized to minimize any deformation or stress on the sensor element. DUT insertion and socket are key to avoid calibration errors on the curve that could limit the application of the sensor.

Innovative testing technologies typically require dedicated testing equipment, and thus a deep cooperation between sensor suppliers and testing equipment suppliers is required to be successful. In the last decade, testing equipment suppliers in cooperation with sensor manufacturers have constantly increased the degree of parallelism for the sake of higher productivity and thus lower cost. Many progresses have been done in this direction, but the high accuracy requirements imposed by new market application continue to demand further testing advances.

18.6 Accelerometers

MEMS accelerometers are transducers able to convert an acceleration input in an analog or digital electrical output. Acceleration input signal is either a result of a motion of the sensor in an inertial frame of reference, in which case the accelerometer is used as motion sensor, or the projection of the component of Earth's gravitational acceleration on the sense axis, in which case the accelerometer is used as

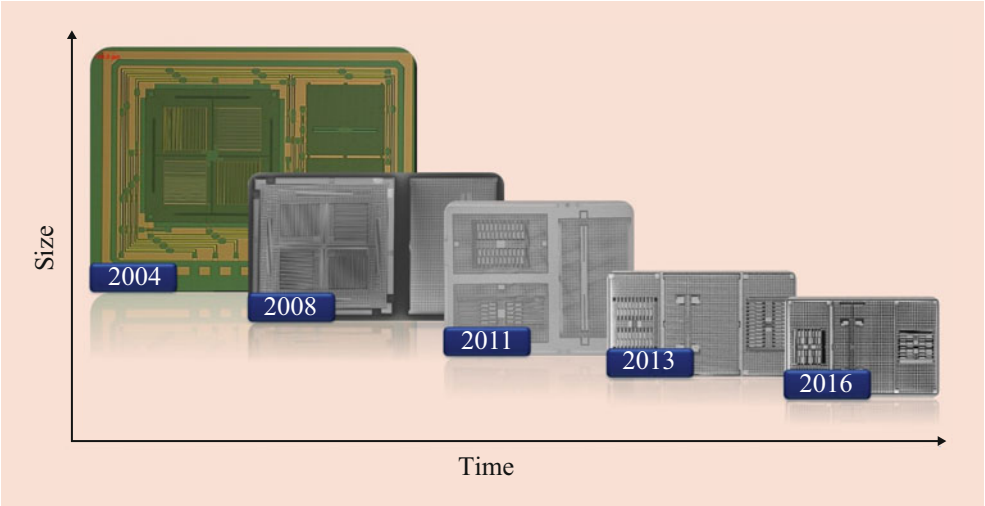

Fig. 18.22 STMicroelectronics three-axis MEMS accelerometers for consumer market: die size evolution (images in scale). Along with impressive die size reduction, capacitive MEMS accelerometer has also experienced a dramatic performance boost since early introduction in the 1990s to present. (© 2018 by STMicroelectronics)

an inclinometer. Acceleration signal is usually expressed in units of g, the common value of Earth's gravitational acceleration at sea level, and converts into 9.81 $\frac{\mathrm{m}}{\mathrm{s}^2}$.

18.6.1 Accelerometers Introduction

MEMS accelerometer was one of the first MEMS sensors to be recognized as potential application of mechanical silicon sensors [5] and one of the first MEMS sensors to achieve commercial success in the early MEMS stage due to its automotive applications to replace switches in airbag deployment. The requirement of high reliability crash sensors at reasonable cost for automotive industry has driven the early development of silicon motion sensors. In 1991, Analog Devices' ADXL50 accelerometer [24] was the first commercially available, high-volume manufactured accelerometer realized with surface micromachining and available in ceramic packages (Fig. 18.22).

As accelerometer was the driver of the first sensor consumerization wave for automotive applications in the 1990s, it led also the second wave of inexpensive, ubiquitous sensor adoption in consumer electronics devices. In the mid-2000s, MEMS accelerometers were adopted in game consoles, smartphones, and laptops in order to enable more intuitive user interfaces.

In this timeframe, MEMS accelerometers changed and evolved their main characteristics to penetrate new markets. Shrinkage of sensor dimensions and lower power consumption were a key driver to enable accelerometer adoption in small, battery-operated consumer devices. Better accuracy and reliability, high flexibility on full scale, and bandwidth are now driving the MEMS accelerometers to challenge traditional piezoelectric sensors in the industrial market.

18.6.2 Accelerometer Specifications

MEMS accelerometers today have widespread applications in all markets, and the target application strongly influences the specifications of the sensor. Key performance indicators of acceleration sensors are full scale, offset, sensitivity, noise, and bandwidth, along with power consumption of the system.

Full scale is the range of input accelerations that can be converted before saturation of the mechanical element or readout electronics. The traditional segmentation of MEMS accelerometers divides them into low-g sensors (with full scale ranging from 1 g to 32 g) and high-g sensors (with full scale ranging from 50 g up to 8000 g).

Offset is the output value of the sensor when no input signal is applied. In accelerometers, offset is usually referred to as zero-g level (ZgL), and its value is calibrated at final testing. The requirement for stability of ZgL during device lifetime, in the complete operative temperature range, can range from fraction of milli-g (mg) in high accuracy inclinometers up to few g in applications where DC acceleration is cancelled.

Output noise value, i.e., the fluctuation of the accelerometer output when input acceleration is not varying, is also differentiating sensors in the different applications. Typical values range from 0.1 $\frac{\mu\mathrm{g}}{\sqrt{\mathrm{Hz}}}$ in seismic exploration for oil and gas to 1 $\frac{\mu\mathrm{g}}{\sqrt{\mathrm{Hz}}}$ in industrial vibration monitoring up to 100 $\frac{\mu\mathrm{g}}{\sqrt{\mathrm{Hz}}}$ in mobile phones and wearable electronics applications.

Bandwidth is the frequency point at which sinusoidal acceleration inputs are attenuated by 3 dB. It is determined by the frequency response of the system, as a combination of the mechanical frequency response of the MEMS sensor combined with the dedicated analog or digital filtering on ASIC. The mechanical bandwidth is a function of the

resonance frequency and the damping ratio of the sensor, gas damping being the dominant dissipation source in several accelerometer designs.

Power consumption of MEMS accelerometers was one of the key advantages of micro-fabricated sensors. Power requirement strongly varies depending on the final application: industrial or automotive applications allow for few mW of power dissipation for each sense axis, while wearable electronics applications require few μW for a full three-axial device. At the limit of power requirement are medical implantable accelerometers for pacemakers or brain stimulators, targeting sub-μW power dissipation.

18.6.3 Accelerometer System

MEMS accelerometers are usually composed of an electromechanical element and a signal conditioning integrated circuit, usually referred to as application-specific integrated circuit (ASIC). The two silicon dice are electrically connected and protected by a dedicated package.

The mechanical element translates the acceleration signal in an electrical quantity (capacitance, voltage, frequency). Several transduction mechanisms were proposed and are used to sense acceleration. The most common sensing mechanism is capacitive, piezoresistive, or piezoelectric. The ASIC is electrically connected to mechanical element, usually by means of wire bonding (Fig. 18.23).

MEMS accelerometers can be operated in open or closed loop. In open loop mode, the signal chain is a single direction stream from acceleration to analog or digital output, the force acting on proof mass is in principle only acceleration, and ASIC has the main purpose of signal conversion (e.g., from capacitance to voltage), conditioning and filtering, and digitalization. Closed loop accelerometers instead apply a force on the proof mass to maintain the position fixed also in presence of external accelerations. This is performed with a dedicated control loop actively steering the sensor by means of electrostatic force. This is also known as force-to-rebalance working principle (Fig. 18.24).

18.6.4 Capacitive MEMS Accelerometers: Design Principles

In capacitive MEMS accelerometers, the acceleration is sensed by measuring the displacement of a movable mass with respect to its rest position in the inertial frame of reference on which the sensor is fixed. This displacement causes a differential capacitance change between a set of fixed electrodes (stator) and a set of movable electrodes (rotor). The change of capacitance is measured by means of a suitably designed readout electronics.

In the literature, different architectures for sensing linear acceleration in one, two, or three directions through mono-axial, biaxial, or three-axial solutions have been reported [25–27]. The most common solution adopted in the industry is to use a mono-axial architecture for each acceleration direction. In the next section, the basic working principle for in-plane and out-of-plane accelerometer is described (Figs. 18.25 and 18.26).

The displacement of an x-axis single-mass device can be modelled through the following 1-degree-of-freedom motion equation:

$$m\frac{\mathrm{d}^2x}{\mathrm{d}t^2} + b_x\frac{\mathrm{d}x}{\mathrm{d}t} + k_x x = ma_{\mathrm{ext}} \tag{18.3}$$

where m is the movable mass, b_x represents the damping term, k_x is the elastic stiffness, and $a_{\mathrm{ext}} = 9.8 \bullet g$ is the external acceleration applied to the inertial frame. The equation of motion can be translated to the frequency domain through the Laplace transformation in order to obtain the sensor displacement vs acceleration frequency response; see Fig. 18.27.

In this plot, the flat region corresponds to the sensing bandwidth of the sensors, and it is defined by the combination of the resonance frequency ω_0 and the Q factor. The static response to acceleration can be evaluated by setting all time-dependent terms in the previous motion equation to zero obtaining

$$\frac{\mathrm{d}x}{\mathrm{d}g} = \frac{9.8}{\omega_0^2} \tag{18.4}$$

from which results that the displacement of the movable mass is defined only by the resonance frequency of the mass-spring system. The stator and rotor electrodes form two set of capacitors, which can be expressed as.

$$C_1 = \frac{\epsilon NLt}{(g_0 - x)};\ C_2 = \frac{\epsilon NLt}{(g_0 + x)}; \tag{18.5}$$

where ϵ is the air permittivity, N is the number of parallel plate stator-to-rotor cells, t is the electrode thickness, and g_0 is the stator-to-rotor gap at rest. By combining the previous two equations and linearizing around $x = 0$ position, one can calculate the differential capacitance variation per unit of external acceleration also known as electromechanical sensitivity:

$$\frac{\mathrm{d}\Delta C}{\mathrm{d}a_{\mathrm{ext}}} = 2\frac{\mathrm{d}x}{\mathrm{d}a_{\mathrm{ext}}}\frac{\mathrm{d}C}{\mathrm{d}x}\bigg|_{x=0} = 2\frac{\epsilon_0 NLt}{g_0^2}\frac{1}{\omega_0^2} \tag{18.6}$$

The sensitivity of a MEMS capacitive accelerometer depends on three main parameters:

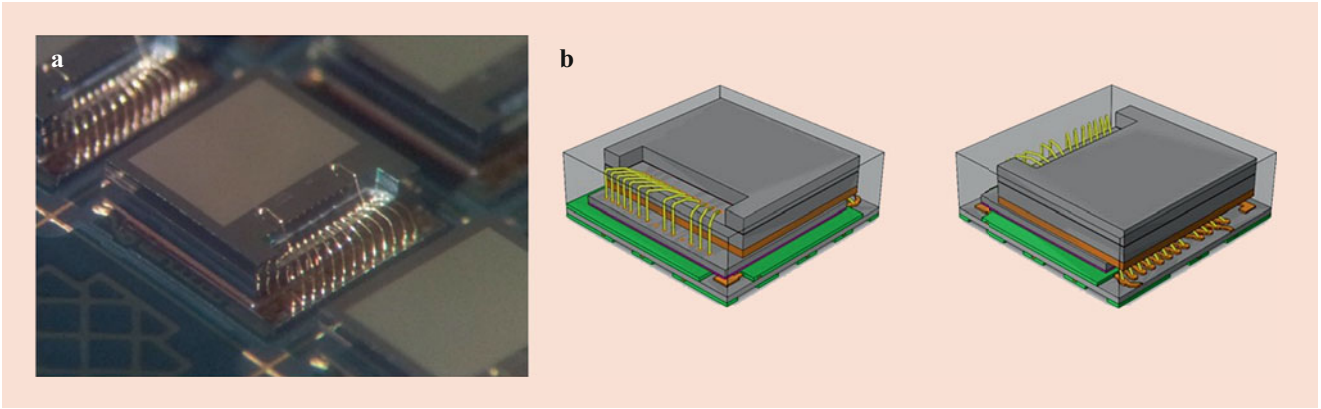

Fig. 18.23 In STMicroelectronics IMUs, the MEMS sensor and the signal conditioning ASIC are two separated silicon dice placed inside the same plastic system in package. The two dice are connected with wire bonding, providing electrical connectivity. (**a**) Image of stacked MEMS and ASIC dice attached to a plastic LGA substrate and wire bonded together, before the molding process. (**b**) 3-D view of the package after molding and singulation. ASIC is the bottom die, while MEMS sits on top. (© 2018 by STMicroelectronics)

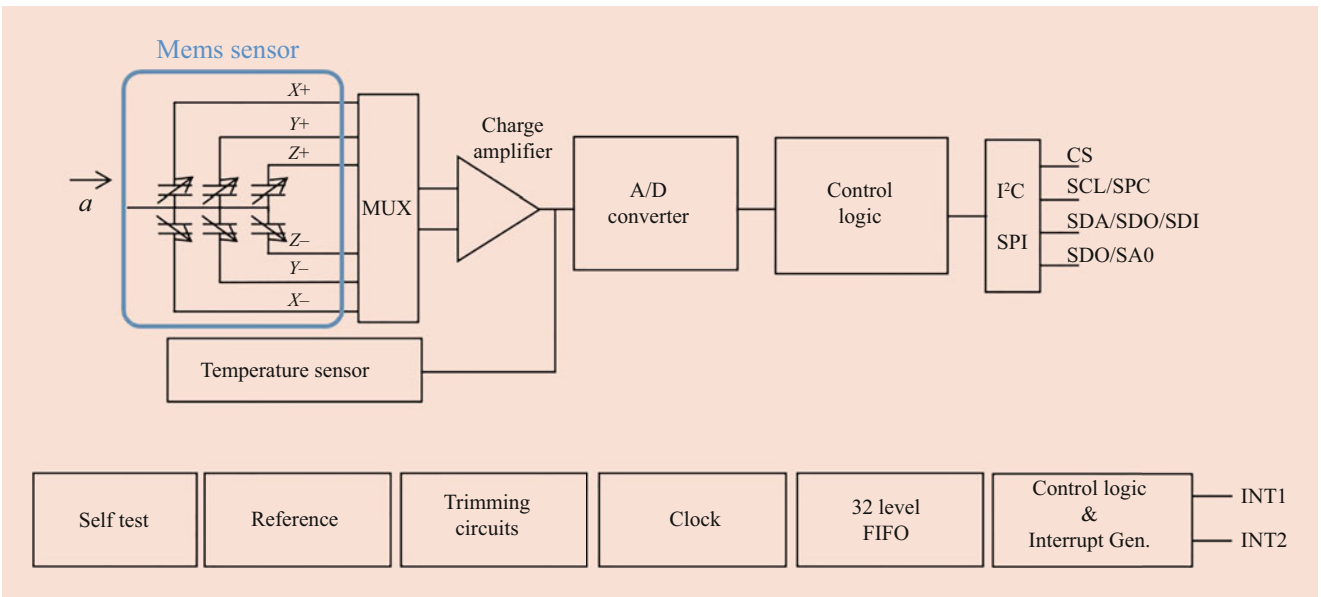

Fig. 18.24 Architecture of a capacitive digital MEMS accelerometer system: LIS2DW12 three-axis accelerometer from STMicroelectronics. The sensor, indicated by the variable capacitors in the blue box, is attached to a multiplexer and to a charge amplifier. The voltage signal from the charge amplifier and the temperature signal for temperature compensation are fed into an analog to digital converter, and the digital signal is then available to be filtered by onboard signal conditioning and elaboration. (© 2018 by STMicroelectronics)

1. The electrodes area NLt, which can be tuned by increasing the die size or increasing the thickness of the silicon.
2. The stator-to-rotor gap at rest g_0, which depends on the minimum critical dimension (CD) defined by the deep reactive ion etching (DRIE) process used.
3. The resonance frequency ω_0, which is defined by the ratio of the elastic stiffness k_x and the movable mass m, which depends on the intrinsic properties of silicon (Young's modulus, Poisson ratio, material density), on the spring geometry, and thus again on the DRIE capabilities.

In general, high sensitivity is required to ensure low noise and low power performance when the sensor is coupled with a dedicated readout circuits as well as to ensure high stability device.

18.6.5 Capacitive MEMS Accelerometers: Process Flow

Capacitive MEMS accelerometers can be manufactured with different micromachining techniques. An example of epitaxial micromachining process developed specifically for MEMS inertial sensors, STMicroelectronics ThELMA MEMS process, is described in the next section.

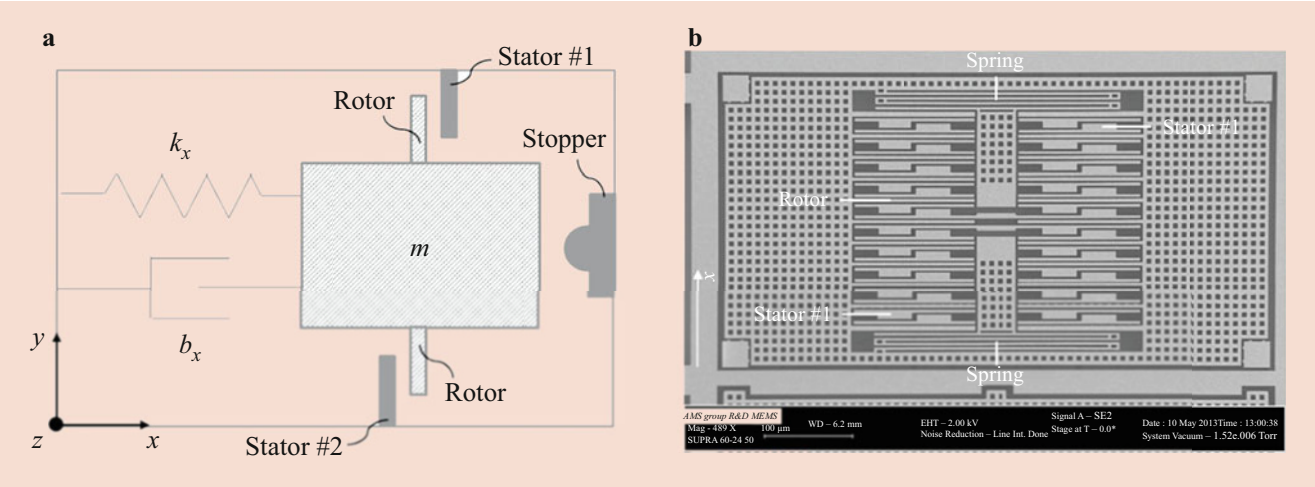

Fig. 18.25 MEMS capacitive accelerometer. (**a**) Schematic representation of an in-plane MEMS capacitive accelerometer based on 1DOF mass-spring-damper model. (**b**) SEM image of the *X*-axis of SK33 a MEMS accelerometer of STMicroelectronics. (© 2018 by STMicroelectronics)

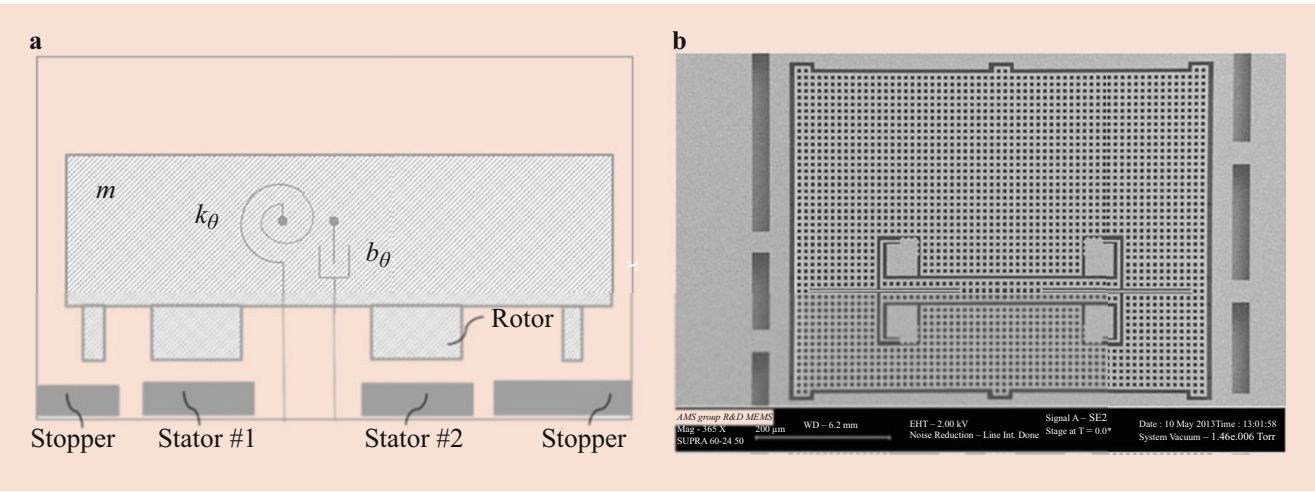

Fig. 18.26 (**a**) Schematic representation of an out-of-plane MEMS capacitive accelerometer based on 1DOF mass-spring-damper model. (**b**) SEM image of the *Z*-axis of SK33 a MEMS accelerometer of STMicroelectronics. (© 2018 by STMicroelectronics)

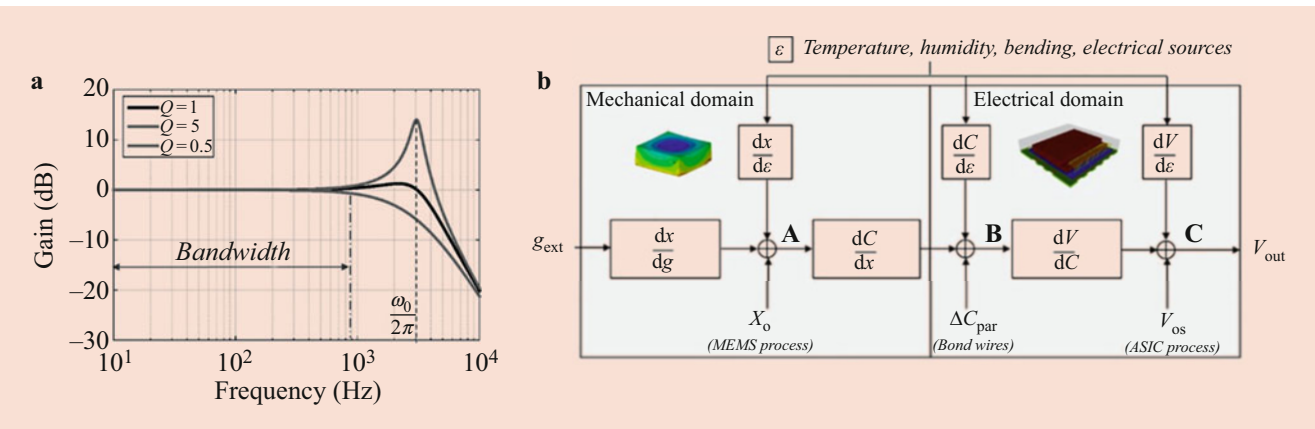

Fig. 18.27 (**a**) Frequency response example of a MEMS capacitive accelerometer. (**b**) Schematic representation of a MEMS capacitive accelerometer at system level including non-idealities from fabrication process (MEMS, ASIC, package) and external spurious effects such as temperature, humidity, bending, and electrical sources. (© 2018 by STMicroelectronics)

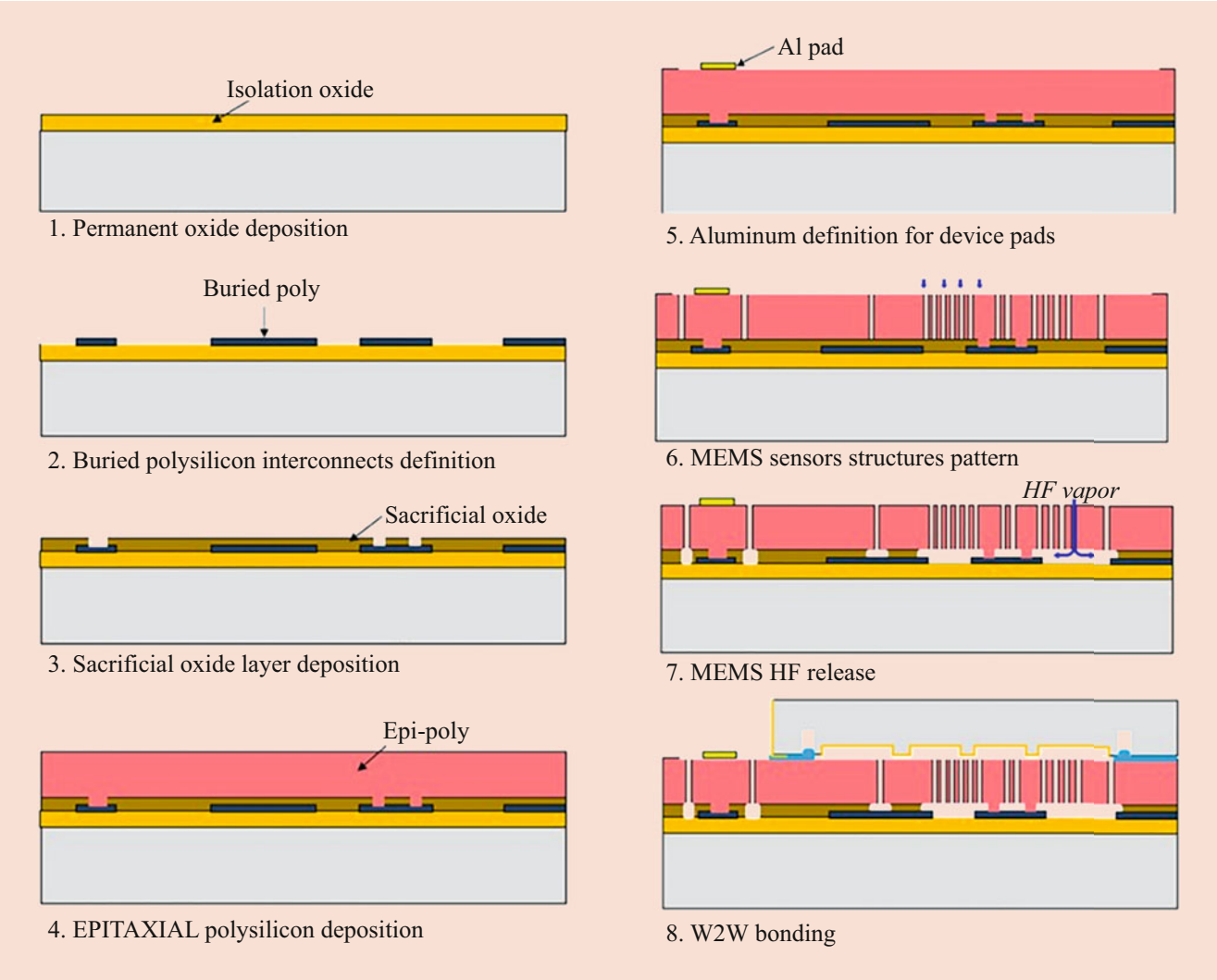

Fig. 18.28 Flow chart of STMicroelectronics ThELMA surface micromachining process for inertial sensors. (© 2018 by STMicroelectronics)

ThELMA is an acronym for thick epitaxial layer for micro-gyroscopes and accelerometers. ThELMA process is based on the fabrication of two wafers: the sensor wafer, which includes the micromechanical components, and the cap wafer. The two wafers are bonded together in the final part of the front-end process. Wafer-level bonding is needed in order to protect the micromechanical elements and enables to use standard back-end technologies like testing, dicing, and packaging, ensuring the reliability of the product over-time. Figure 18.28 shows a schematic process flow for a ThELMA accelerometer.

The sensor wafer process flows start with the growth of a thermal oxide, which is used to insulate the interconnections from the substrate. A thin polysilicon layer is used to design buried interconnections and electrodes for out-of-plane sensing structures. A sacrificial oxide is then deposited and defines the final *Z*-gap between the polysilicon electrodes and the rotor mass for vertical displacements (e.g., accelerometer *Z*-axis). This layer is patterned to define the anchoring areas and the ground areas where the rotor mass is connected to the buried polysilicon and to the substrate. Rotor mass is realized through an epitaxial polysilicon (EPI) growth, and the thickness could vary between 15 and 60 μm according to product requirements. This layer is patterned by DRIE process that defines proof mass, the sensing and driving electrodes, and the device spring. Finally, the sacrificial oxide under EPI structures is removed by HF vapor etching allowing the release of the MEMS sensing structures.

ThELMA technology allows manufacturing both in-plane and out-of-plane actuation and sensing electrodes by exploiting epitaxial polysilicon in the *X*-*Y* plane and buried polysilicon versus epitaxial polysilicon in the *Z* direction.

The cap wafer is a silicon substrate, which typically includes a cavity on the sensing area to allow the out-of-plane displacement of the rotor mass and pad window opening which provides access to the probing pads.

Sensor and cap wafers are then bonded together using glass frit bonding technology. Glass frit is a low melting temperature glass, which can be deposited on cap wafer by screen printing process. During wafer bonding, glass frit is heated and melts at temperature higher than 400 °C. After cooling, the glass frit layer solidifies, providing a hermetic seal joint between the sensor and the cap wafers.

The main competitive advantages of ThELMA versus other commercial technologies are:

1. The use of a thick low stress epitaxial polysilicon film; for high performance applications, thickness values up to 60 μm were implemented in production.
2. The use of the getter layer which improves the vacuum level inside the package; the use of getter allows also to integrate on the same die an accelerometer and a gyroscope (six-axis) working at different pressure values, as reported by Ferarresi [28].
3. A system architecture on which IC and MEMS are manufactured by different technological platforms. In fact keeping MEMS and the IC technologies separated increases technology development flexibility, removing from integration constraints between MEMS and the IC.
4. A long experience coming from more than 10 years' high-volume manufacturing and more than 10 billion devices sold, including accelerometers, gyroscopes, and combo devices.

18.6.6 Reliability Challenges for MEMS Accelerometers

The purpose of reliability is to estimate device lifetime versus device potential failure modes [29, 30].

In an industrial context, the challenge of reliability is to address new product and technology introduction, new material introduction, and manufacturing process change. The general methodology has to address both intrinsic and extrinsic potential failure [31–33]. Intrinsic failure mechanisms are strictly related to products design performance and relative vulnerability. Extrinsic failure mechanisms are related to all the supply chain steps involved in the product fabrication (wafer fabrication, assembly, testing, etc.).

During validation phase, the intrinsic vulnerability is assessed following standard international procedure (JEDEC) [32, 33]. In the specific case of MEMS, stress tests are customized in order to consider additional failure modes related to the strong interaction between environmental condition and mechanical elements that could affect device performances and mechanical robustness.

During MEMS production ramp-up phase, the extrinsic vulnerability is assessed. Generally, a time-reduced stress test is applied on a large amount of devices in order to investigate product marginality vs manufacturing process phase.

Several failure mechanisms have been found to be the primary sources of failure. Typical MEMS three-axis accelerometer failure mechanisms are:

- Lack of hermeticity.
- Parametric stability.
- Adhesion.

Lack of hermeticity is a serious failure mode, caused by presence of voids or cracks in the sealing material (glass frit or metal alloys) that is used to seal cap to sensor. It can be a time zero defect during wafer-to-wafer bonding or induced by thermomechanical stress that occurs during manufacturing (molding, soldering, etc.). Time zero defect can be detected at wafer level performing automatic scanning acoustic microscopy (SAM) control, while at package level it can be monitored submitting the plastic devices to moisture and performing accelerated THS (temperature humidity storage [33]) test. Customized THS is applied during product rump-up or reliability monitoring.

Parametric stability concerns zero-g level offset and sensitivity, and it is strongly affected by thermomechanical interactions between package and MEMS. Package thermomechanical stress induced by hygro-swelling for water absorption or high temperature excursion (e.g., soldering) can cause submicron displacement of movable parts that induces meaningful deviation on output parameters. In order to evaluate intrinsic susceptibility to hygro-swelling, dedicated reliability test should be performed during early qualification phase. This test may consist of putting device in a climatic chamber and monitoring sensor output (device soldered on application board) changing the percentage of relative humidity (Figs. 18.29 and 18.30).

Adhesion, for example, between movable mass and stoppers, is a phenomenon that appears when surfaces adhesion

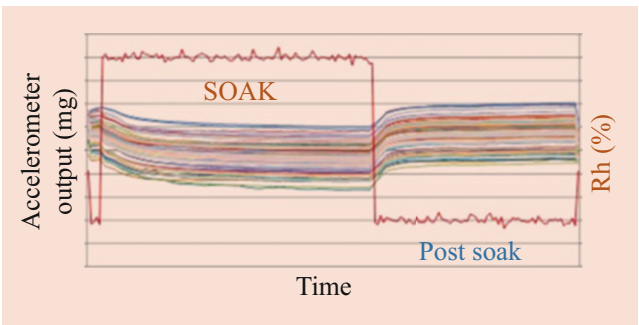

Fig. 18.29 Parametric output of an accelerometer sensor acquired during active soaking of the device in a variable humidity environment. This test has the capability to highlight potential weaknesses due to temperature and humidity – activated interactions between package and MEMS. (© 2018 by STMicroelectronics)

forces (electrostatic attraction, van der Waals forces, etc.) are larger than the mechanical restoring force of a suspended micromechanical element. It may occur during wafer manufacturing or device usage (in this case, it is known as in-use adhesion).

This phenomenon is activated in presence of electrical field, for instance, when device is powered and shocked with a low-g acceleration. Detection and characterization take place performing dedicated capacitance vs voltage (*CV*) measurements at electrical wafer sorting (EWS) and on final devices or monitoring the sensor outputs when a low-g acceleration is applied [34, 35]. This powered shock test is a good reproduction of possible in-use adhesion. In order to reduce the adhesion occurrence, the abovementioned tests are used to improve technology process and design, for instance, optimizing moveable mass stiffness.

18.6.7 Next-Generation MEMS Accelerometers

The evolution of MEMS accelerometers has improved dramatically the trade-off between conflicting requirements such as noise, full scale, accuracy, and power consumption.

Traditionally, high accuracy MEMS sensors were available only with very limited full scale, bulky packages, and power consumption in the mW region. Low-power accelerometers for consumer and wearable electronics applications, instead, offered state-of-the-art power consumption in appealing small packages at the expense of higher noise and limited accuracy.

High-g sensors were almost dedicated to automotive applications (airbag deployment, tire pressure monitoring systems – TPMS), where lower noise and offset accuracy performances could be easily forgiven (Table 18.3).

A clear path in next generation of MEMS accelerometers is the further improvement of the noise and accuracy vs full scale and power trade-off, due to the convergence of consumer, automotive, and industrial requirements [36].

Higher full scale of consumer accelerometers, beyond the traditional 16 g, could unleash a series of potential applications as shock monitor and detection that involves acceleration levels in the order of tens of *g* for human fall detection in wearable electronics equipment [37] up to thousands of *g* in the case of shock detection for mobile electronics. This would naturally be an add-on requirement to the standard accuracy and noise for low-g sensors, to preserve the level of user experience while adding more functionalities. Such high-g accelerometers can also be merged with accurate temperature sensors in order to provide valuable tracking information during shipment of goods.

Capacitive MEMS accelerometers are also tackling traditional applications usually served by bulk piezoelectric sensors. Good accuracy performances, together with high level of integration of the signal conditioning chain, small size, and reasonable cost, offer an appealing solution for industrial applications [38].

Preventive maintenance of mechanical equipment and structural health monitoring of buildings and bridges are key examples where the availability of affordable, reliable, and accurate sensors can make the difference in the cost-benefit analysis of the installation of sensor networks [39–41].

Integration of accelerometers in 6-degrees-of-freedom inertial measurement units (6-DoF IMUs) is today a mainstream direction for consumer and automotive non-safety applications.

18.7 Gyroscopes

Gyroscopes are sensors used to convert rotation rate input in an analog or digital output. Rotation rate, or angular velocity, is the amount of angle travelled in unit time during a rotation and is usually measured in degrees per second [dps].

18.7.1 Gyroscopes Introduction

MEMS gyroscopes are commonly based on Coriolis force, an apparent force arising in presence of a linear movement and a rotation of the frame of reference. The need for active excitation of the linear, or drive, movement and the higher intrinsic complexity in the design and realization of MEMS gyroscopes has slowed their introduction in the automotive and consumer applications, and only a decade after the successful introduction of MEMS accelerometers in the market, MEMS gyroscopes were commonly adopted in automotive and consumer electronics goods.

It was in the first half of 2000 that first quartz tuning fork gyroscopes achieved commercial success, and driver was again, as for MEMS accelerometers, automotive and aerospace industry. The availability of micromachining technology already matured for accelerometers enabled in the first years of 2010s the introduction of silicon MEMS devices matching the performance, size, and cost requirements of consumer electronics manufacturers.

At present, gyroscopes have a huge variety of applications, in the class of motion detection (e.g., in enhanced user interface in gaming consoles and smartphones, in rollover detection in automotive or in inertial navigation systems) or motion control (e.g., in antenna stabilization systems, electronic stability control in automotive or optical image stabilization in camera lens).

As happened for accelerometers, in the past years, MEMS gyroscopes evolved in several performance metrics, leading to small, accurate, and less power-hungry sensors (Fig. 18.31).

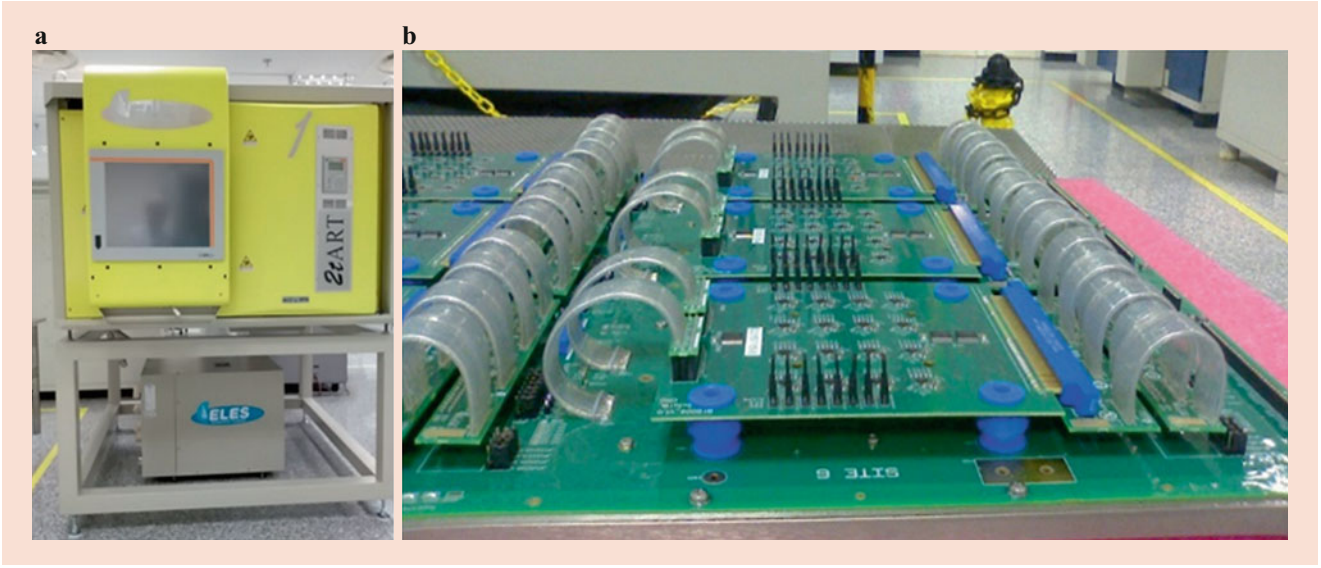

Fig. 18.30 (**a**) Dedicated climatic chamber with compressor outside (**b**) reliability board with adapter (16 parallel sites). Soft gimbals hold the board and flex cables connect board to adapter, minimizing external mechanical vibrations. (© 2018 by STMicroelectronics)

Table 18.3 Performance of Colibrys MEMS V1000 series accelerometers having different full-scale ranges. A great challenge for accelerometers is to break the trade-off full scale vs accuracy and noise, to enable applications based on shock detection without sacrificing traditional user interface functions

Parameter	Unit	VS1002	VS1005	VS1010	VS1030	VS1050	VS1100	VS1200
Full scale	**g**	±2	±5	±10	±30	±50	±100	±200
Noise	**μg/√(Hz)**	7	17	34	102	170	339	678
Bias temperature coefficient	**Mg/°C**	±0.2	±0.5	±1	±3	±5	±10	±20

Source: https://www.colibrys.com/product/vs1000-vibration-sensor/

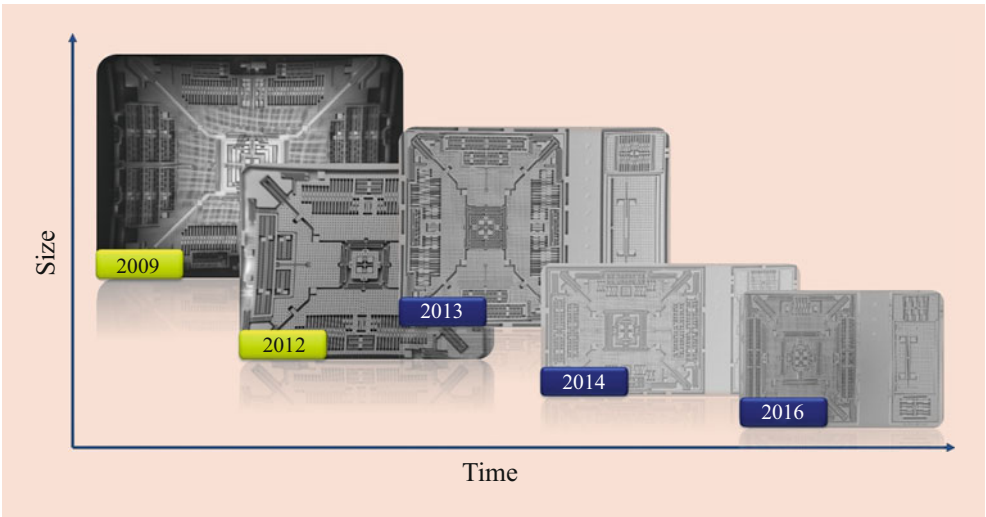

Fig. 18.31 STMicroelectronics three-axis MEMS gyroscopes and six-axis IMUs for consumer market: die size evolution (images in scale). In the case of six-axis IMUs, die size reduction and performance improvement progressed alongside with features integration. (© 2018 by STMicroelectronics)

18.7.2 Gyroscopes Specifications

Key performance indicators for gyroscopes are similar to the ones described for the MEMS accelerometers: most critical ones are offset or bias, scale factor or sensitivity, noise, and power consumption.

Offset or bias is the output value of the sensor at zero input, usually referred to as zero rate level (ZRL). ZRL

Table 18.4 Bias stability and scale factor accuracy level for gyroscopes as a function of the grade and application. MEMS capacitive gyroscopes have created the consumer market and strongly penetrated the industrial and low-end tactical grades. Strong efforts are still needed for MEMS to be a viable substitute for ring laser gyroscopes (RLG) or fiber-optic gyroscopes (FOG) in the highest grade markets

Grade	Application	Bias stability $\left[\frac{^\circ}{h}\right]$	Scale factor accuracy [ppm]
Consumer	User interface	30–1000	5000–10,000
Industrial and low-end tactical	Guided ammunitions	1–30	100–5000
Tactical	Platform stabilization	0.1–30	10–100
High-end tactical	Missile navigation	0.1–1	1–10
Navigation	Aerospace inertial navigation	0.01–0.1	<1
Strategic	Submarine navigation	0.0001–0-01	<1

and its variation due to temperature, vibrations, or aging are critical parameters for gyroscopes, and they can range from few degrees per second (dps) in low-end systems down to few degrees per hour $\left[\frac{^\circ}{h}\right]$ in low-end tactical applications.

Competing technologies have clearly defined a benchmark for gyroscopes based on the achievable accuracy in the reconstruction of the angular position. Almost all available MEMS gyroscopes are of the rate type (i.e., they measure angular velocity); therefore the motion reconstruction algorithms need an integration to obtain absolute angle information. Errors in offset and presence of noise in the gyroscope output lead to inaccuracy in the integrated signal, strongly limiting the performances of the sensor. As presented in Table 18.4, bias stability is a key performance parameter to differentiate gyroscope performances.

18.7.3 Gyroscope System

Silicon MEMS vibratory gyroscopes are composed of an electromechanical part and a signal conditioning ASIC, encapsulated in a protective package.

The most common transduction mechanisms to actuate the gyroscope and read back the Coriolis signal are electrostatic actuation and capacitance variation, even if few MEMS gyroscopes exploit piezoelectric actuation/readout with quartz crystals or AlN thin films.

A common operation mechanism in MEMS gyroscopes is closed loop driving and open loop sensing. ASIC has the purpose of providing the actuation signal for drive movement,

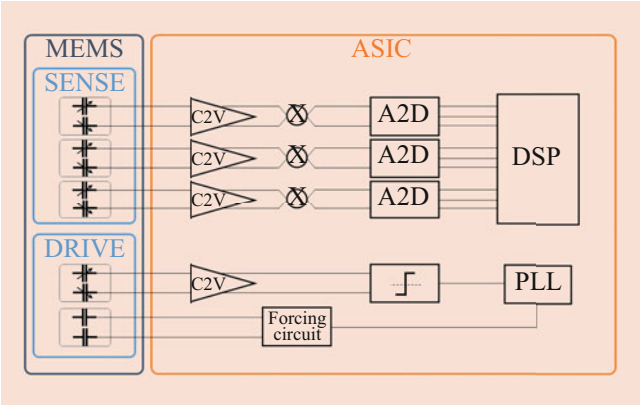

Fig. 18.32 MEMS gyroscope block diagram for sensor and ASIC. A common configuration for capacitive MEMS in consumer applications is closed loop drive and open loop sense. Differently from accelerometers, MEMS vibrating gyroscopes require a coherent demodulation to extract the rate value from the modulated Coriolis signal. (© 2018 by STMicroelectronics)

converting sense signal and operating coherent demodulation and proper filtering.

A feedback loop on ASIC collects the capacitance signal from the sense of drive electrodes, proportional to the MEMS displacement in the drive direction, and converts it to voltage through capacitance to voltage converter (charge amplifier). The signal is then filtered and squared to be fed into a phase locking loop (PLL) in order to adjust the phase difference and provide a forcing signal back to the drive electrodes on the MEMS.

The capacitance signal from sense electrodes is routed to a capacitance to voltage converter (charge amplifier) and then coherently demodulated. The baseband signal is properly filtered and then digitalized through an analog to digital converter (A2D). The digital signal is then processed by an onboard digital signal processor DSP (Fig. 18.32).

18.7.4 Capacitive MEMS Gyroscopes: Design Principles

A Coriolis vibratory gyroscope (CVG) is a classical 2-degrees-of-freedom oscillator. The first degree of freedom is commonly referred as the drive mode, which is kept at a fixed amplitude harmonic oscillation by a controlled closed loop to generate the Coriolis force on the perpendicular direction; the second degree of freedom is known as sense mode, or detection axis. An electrostatic force F_d is applied in the case of the drive mode to sustain oscillation: in most cases, this force is harmonic, of sinusoidal or square wave type, and it is applied at drive resonant frequency.

Regarding the sensing axis, the forcing term is represented by the Coriolis force, which is generated in the non-inertial

gyroscopic frame by the combination of the drive velocity due to harmonic oscillation and the external angular rate. The amplitude of this force F_{co} is.

$$F_{co} = -2mv_d \wedge \Omega_{ext} \tag{18.7}$$

A gyroscope can be seen as a system of two one-dimensional oscillators, one along the drive direction and one along the sense direction. In the case of a gyroscope made up of a two-symmetrical mass system, the above considerations remain valid, and the equation of motion for the drive axis oscillator will be

$$m_d\ddot{x} + r_d\dot{x} + k_d x = F_d \sin(\omega t) \tag{18.8}$$

where m_d, c_d, k_d, and $F_d \sin(\omega t)$ are, respectively, the mass, the damping coefficient, the stiffness, and the force applied to drive. If we introduce the quality factor term and the drive resonance frequency in above equation, we have as solution for the drive displacement amplitude Δx_d

$$\Delta x_d = \frac{\frac{1}{m}}{\sqrt{\left(\omega_d^2 - \omega^2\right)^2 + \left(\frac{\omega_d}{Q_d}\omega\right)^2}} F_d \tag{18.9}$$

where ω_d and Q_d are the resonant frequency and quality factor of the drive oscillator.

In a capacitive Coriolis vibratory gyroscope (CCVG), both the drive and sense axes are, respectively, forced and sensed by means of a set of electrostatic system of capacitors.

The electrodes exploited to actuate and read the oscillation signal of the drive axis are usually of comb-finger type, as showed in Fig. 18.33. This kind of capacitors is arranged as a comb-like interdigitated structure. A voltage difference is applied between the fixed stator fingers and the movable comb structures: this will result in a displacement of the movable mass by means of the electrostatic forces. The force exerted by a set of N comb capacitors is expressed by

$$F_d = \frac{1}{2}\frac{\partial C_d}{\partial x}\Delta V^2 \rightarrow F_d = \varepsilon N \frac{t}{g_0}\Delta V^2 \tag{18.10}$$

Since the dependence of force on voltage is quadratic, to eliminate the constant and the double frequency terms the voltage difference ΔV it is usually made up of a DC plus an AC term so that:

$$(V_{DC} + V_{AC}\sin\omega t)^2 = V_{DC}^2 + V_{AC}^2 \sin 2\omega t + 2V_{DC}V_{AC}\sin\omega t \tag{18.11}$$

The voltage difference is applied to a double differential set of electrodes, driven in antiphase with respect to each other (double differential forcing). According to this scheme, the forcing of the oscillating drive system will become

$$F_d = 4\varepsilon N \frac{t}{g_0} V_{DC}V_{AC}\sin\omega t = 2\frac{\partial C_d}{\partial x} V_{DC}V_{AC}\sin\omega t \tag{18.12}$$

Since the varying dimension is the lateral facing L of the comb fingers, this solution ensures high forcing linearity over the necessary displacement range.

For the same reason, the drive displacement too is read by means of a set of sensing drive electrodes. The capacitance variation, which is commonly fed into a feedback loop, is

$$\Delta C_{sd} = \frac{\partial C_{sd}}{\partial x}\Delta x_d \tag{18.13}$$

The displacement y of the sense electrodes is usually read by a set of parallel plate electrodes, which ensure higher capacitance change with respect to comb structures:

$$\Delta C_{PP} = \varepsilon A\left(\frac{1}{g_0 - y} - \frac{1}{g_0}\right) \approx \frac{\varepsilon A}{g_0^2} y \tag{18.14}$$

In these sensing structures, the variable dimension is the gap; therefore the electrostatic force will be dependent on displacement and nonlinearity. The electrostatic force will be directed along y-axis and its magnitude will be

$$FS = \frac{1}{2}\frac{\partial C}{\partial y}V^2 = \frac{1}{2}\frac{\varepsilon A}{\left(g_{0y} - y\right)^2}V^2 \tag{18.15}$$

The dependency of the force on the position, usually referred to as electrostatic softening, is crucial as it changes the actual elasticity, adding a term of this type to the equation of motion:

$$k_{el} = -\frac{\varepsilon A}{g^3}V^2 \tag{18.16}$$

An example of a ThELMA gyroscope design is the single-mass three-axis gyroscope, better known as the beating heart. Launched in production in high volumes on 2010, this design has been the first three-axis single-mass gyroscope design on the market. The mechanical structure design is explained with the aid of Fig. 18.34.

Four coupled plates, linked by springs, compose the structure; the first vibration modes of the mechanical structure consist in one drive mode and three sense modes: the primary mode (driving mode) is an auxetic expansion of the four masses in-plane. Two opposite masses host the actuation comb fingers used to generate the driving force, while the other two masses are forced to move in phase by the 45° coupling springs. Secondary vibration modes (sensing modes) are identified as pitch and roll modes, in which two opposite

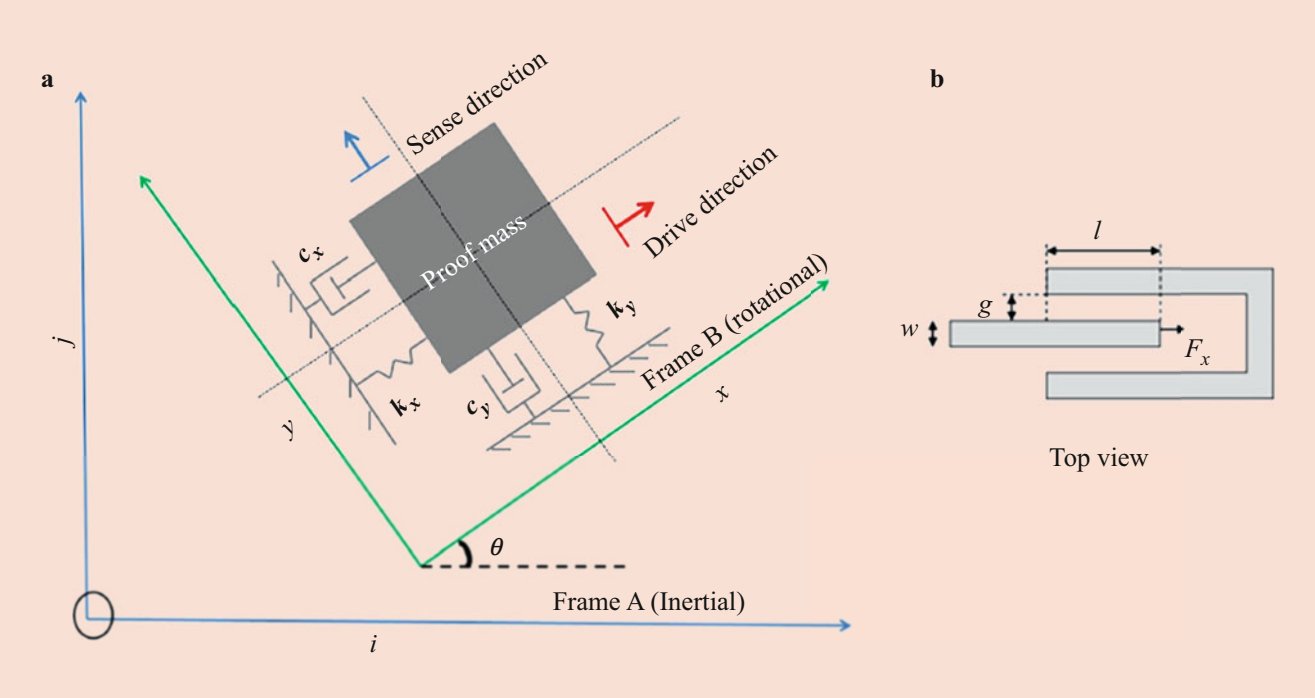

Fig. 18.33 (**a**) 2-degrees-of-freedom spring-mass damper system is shown as a lumped description of Coriolis vibrating gyroscope. The red arrow indicated the drive direction, while the blue arrow, perpendicular to the first, shows the sense direction of motion. (**b**) Schematic representation of a comb-finger capacitor structure, top view. (© 2018 by STMicroelectronics)

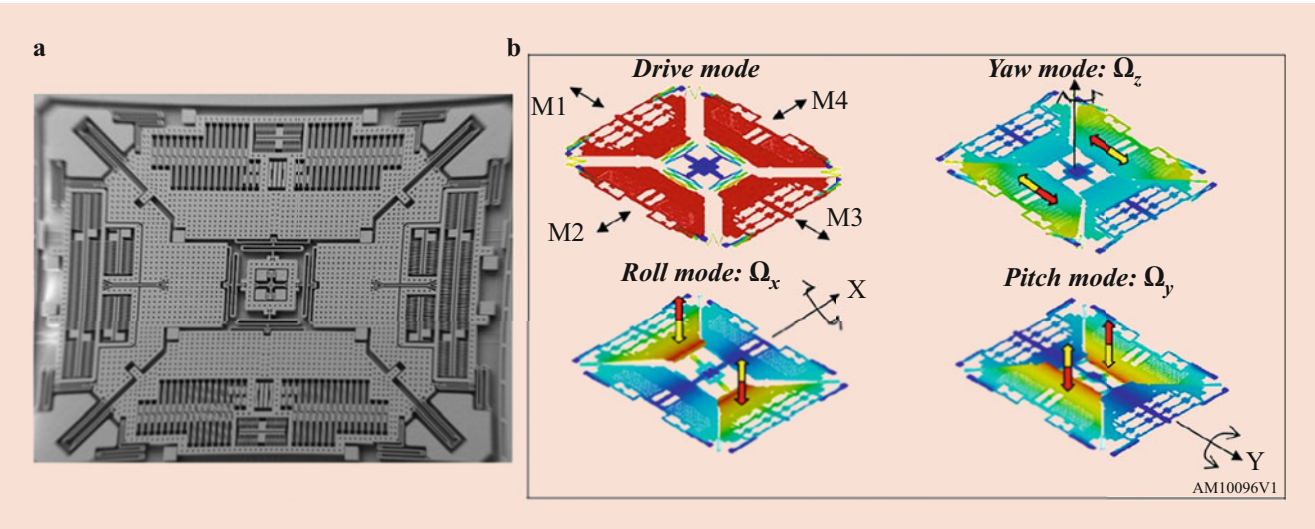

Fig. 18.34 Example of STMicroelectronics ThELMA three-axis gyroscope. (**a**) SEM image of the mechanical structure. (**b**) Vibration modes of the gyroscope. (© 2018 by STMicroelectronics)

masses vibrate in antiphase out-of-plane, and yaw mode, in which all the four masses rotate in-phase in-plane.

Sense pickup electrodes are located below the moving masses for pitch and roll modes, while yaw electrodes are constructed with parallel plates standing out from the substrate. The Coriolis force directly excites the sense modes, generating a movement of the proof mass in the sense direction and inducing a differential capacitance change in the sense electrodes [42].

18.7.5 Capacitive MEMS Gyroscopes: Process Flow

A key requirement for the wafer bonding for MEMS gyroscopes is the possibility to achieve low bonding pressure down to few tenths of mbar in the sealed cavity. In fact, the presence of an actuation mechanism in the gyroscope architecture implies a low damping of the drive motion in order to reduce the power consumption of the device.

High vacuum level can be achieved in MEMS gyroscopes thanks to the integration on the cap wafer of a getter layer. This layer allows the absorption of not inert gas species present in the bonding cavity, ensuring the achievement of a bonding pressure lower than 1 mbar and a reduced spread in the cavity pressure. This reduced spread translates also in more uniform electrical performances of the devices across wafer, wafer-to-wafer and run-to-run. In addition, getter films ensure the stability of the vacuum package over time due to film capacity to getter the gas species that are desorbed by the MEMS package surfaces during device lifetime.

18.7.6 Reliability Challenges for MEMS Gyroscopes

Since gyroscope shares with accelerometers a large part of the manufacturing flow, many failure modes are common to both accelerometers and gyroscopes. Some failure mode and their techniques of investigation reported hereafter were already discussed on previous accelerometer section. Nonetheless, gyroscopes have their specific critical issues related to the high Q factor of the resonance modes [31].

For gyroscope, typical failure mechanisms are:

- Lack of hermeticity.
- Parametric stability.
- Mechanical robustness.

Lack of hermeticity is a serious failure mode caused by presence of voids or cracks in the sealing material that is used to seal cap to sensor. It can be a time zero defect during wafer-to-wafer bonding or induced by thermomechanical stress that occurs during manufacturing (molding, soldering, etc.). This failure mode can be detected at wafer or product level, performing automatic SAM control or THS reliability test, as for accelerometers. In addition, since quality factor of gyroscope is strictly related to hermeticity, quality factor is a key parameter to detect lack of hermeticity with high accuracy, and this measurement is done at both electrical wafer sort and final test.

Parametric stability concerns zero rate level and sensitivity and it is strongly affected by thermomechanical interaction between package and MEMS. As said for accelerometer, also for gyroscope any package thermomechanical stress induced by hygro-swelling for water absorption or high temperature excursion can modify gyroscope quadrature having meaningful consequence on ZRL or sensitivity accuracy. One of most important reliability tests to evaluate gyroscope parameter stability against moisture is to put device in a climatic chamber and monitor sensor output changing the humidity. This method is the same used for accelerometer.

Based on our experience, gyroscope performance is influenced by debris produced by mechanical shock [43]. Besides, shock amplitude is amplified due to high-quality factor of gyroscope. Main procedures used to assess mechanical robustness are based on the following three reliability tests: vibration, mechanical shocks, and drops [34, 44].

Vibration test is suitable to reproduce the mechanical effects generated during transportation or normal usage in range of some tens of g. The test is not relevant for the evaluation of robustness versus usage incidents.

Mechanical shocks and drops are instead targeting shock acceleration level up to hundreds of thousands of g, well simulating effect during handheld stresses [35]. Mechanical shock test can be performed using a pneumatic machine, which combines falling height and pressurized air to produce mono-axial and repeatable shock. Adding a special fixture, acceleration level can range from 500 to 20,000 g (see Fig. 18.35).

Drop test is a free fall that can be done on various hard surfaces and from different heights. This method allows reaching very high acceleration levels up to 200,000 g.

Tumble is a rotating machine able to produce repetitive random free fall drops in a controlled repeatable manner (see Fig. 18.35). We exploited it performing drop test on high quantity of packaged gyroscope, allowing characterizing its mechanical robustness more accurately. This methodology can be applied during early qualification phase or reliability monitoring [45].

18.7.7 Next-Generation MEMS Gyroscopes

The evolution of MEMS gyroscopes has two clear paths to be followed: strong reduction of power consumption to enable low-power applications and improvement of sensor performances to tackle high-value applications in the tactical grade market.

Power consumption of state-of-the-art MEMS gyroscopes dramatically improved in last years, falling for consumer sensors more than one order of magnitude for high performance operative mode. The power reduction has been achieved in parallel to great increase of performances in terms of noise and bias stability. Nevertheless, power consumption gap is still huge compared to MEMS accelerometers, preventing gyroscopes to be used in ultralow-power, always-on applications popular in the current internet of things and activity monitoring era. Current state-of-the-art, ultralow-power MEMS capacitive gyroscopes operate with less than half mA current drain, more than two orders of magnitude higher power consumption than low-power accelerometers. The actuation of drive mode and the modulation of the signal over acoustic are fundamental differences between

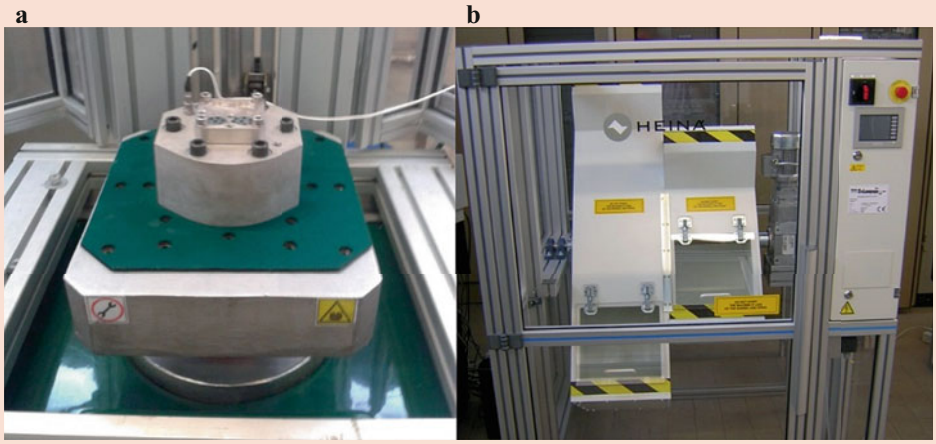

Fig. 18.35 (**a**) Pneumatic shock machine: particular of the carriage and fixture acting as shock amplifier. (**b**) Example of equipment used for tumble test. It is a rotating machine where devices are repeatedly dropped. (© 2018 by STMicroelectronics)

MEMS gyroscopes and accelerometers, limiting the power consumption reduction.

Accuracy improvement is the second trend driving MEMS gyroscopes' development in next years. In the automotive field, ADAS (advanced driver assistance system) and self-driving cars will soon demand performances close to low-end tactical grade sensors. This can be achieved with increased complexity in the architecture, with dedicated quadrature compensation structures and use of closed-loop quadrature cancellation and sense.

Another promising path is to use low-end sensors with good performance capabilities and either redound them or place in a controlled enclosure and compensate drifts of key parameters (bias, scale factor) with an external microcontroller.

Integration of accelerometers in 6-degrees-of-freedom inertial measurement units (6-DoF IMUs) is today a mainstream direction for consumer and automotive non-safety applications.

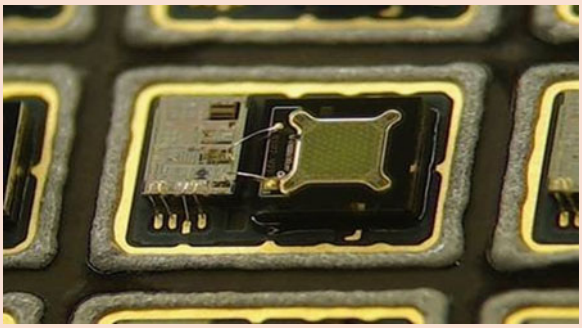

Fig. 18.36 Optical picture of a STMicroelectronics MEMS microphone in a strip, before cap attachment. MEMS sensor is on the right and ASIC on the left. Wire bonding connects MEMS to ASIC and ASIC to substrate. Solder paste for cap attachment is visible on the external ring. (© 2018 by STMicroelectronics)

18.8 Microphones

A microphone is an acoustic transducer able to convert sound into an electric signal. Sound is a pressure wave with frequency in the range 20 Hz–20 kHz (audio band) and pressure that ranges between 20 μPa (audible threshold) and several tens of Pa. In order to detect this physical quantity, microphones need a moving element, usually a membrane, vibrating when reached by sound, and some transduction principle (i.e., capacitive or piezoelectric) to convert this vibration in an electrical signal, i.e., a voltage or charge variation.

MEMS microphones are widely adopted in a large number of devices because of their small size, low cost, good performances, and high part-to-part repeatability. Moreover, a key feature of MEMS microphone success is compatibility with surface mounting, whereas electret microphones require a dedicated and more expensive soldering process.

18.8.1 Microphones Introduction

A MEMS microphone is made of a sensor, an ASIC, and a package, as shown in Fig. 18.36.

Sensors convert sound pressure into an electrical signal. Two transduction principles are commonly adopted in MEMS microphones: capacitance variation or direct piezoelectric effect. Fabrication adopts semiconductor technology blocks and dedicated micromachining process steps. Several possible implementations are possible and will be discussed in detail in Sects. 18.8.2 and 18.8.3.

ASICs have different functions: providing proper polarization to the sensor if needed, performing signal readout, conditioning, and elaboration (i.e., buffering, analog to digital conversion). Both analog and digital output are widespread. Digital signal is usually in PDM (pulse density modulation) format; I2S (integrated interchip sound) is also available.

Package is a key element in microphones. It protects sensing element and IC, as in all MEMS devices, but it also deeply affects performances of the system. Typical microphone package is a cavity, made of a land grid array (LGA) substrate and a metal or organic cap, as shown in Fig. 18.36. Sensor and ASIC are attached to the substrate and electrically connected, usually via wire bonding. A hole in the substrate or in the cap (sound port) allows sound entering the cavity. Dimensions of cavity and sound port have a significant effect on microphone performance.

A brief review of the most significant parameters for a microphone helps to understand the most important constraints in their design and fabrication.

Sensitivity is defined as output signal on input pressure where input pressure is 1 Pa RMS (94dBSPL) at 1 kHz. Unit is dBV (RMS voltage signal at 1 Pa) for analog microphone and dBFS (signal at 1 Pa related to ADC full scale) for digital microphones. Commercial products commonly adopt some standard levels (i.e., −38 dBV for analog microphones and −26 or −41 dBFS for digital microphones) in order to be fully compatible with the readout chain. Part-to-part spread is key: state of the art is sensitivity within ±1 dB.

Frequency response is the output behavior across the frequency range, as shown in Fig. 18.37. All MEMS microphones have a low-frequency roll-off: sensitivity decreases toward lower frequencies. Roll-off point is defined as the frequency where signal is 3 dB lower than its 1 kHz value. This phenomenon is due to the need of a ventilation hole in the membrane to equalize static ambient pressure: without this hole, microphone would act as a pressure sensor, since ambient pressure is several magnitude orders higher than sound pressure. This ventilation hole acts as an alternative path for the sound, subtracting part of the signal from the membrane. Roll-off frequency can be set by ventilation hole design and is usually below 100 Hz (a typical choice is 35 Hz).

At higher frequencies, package acts as a Helmholtz resonator: a resonance peak is therefore present in the range of 15–20 kHz or slightly above 20 kHz, as shown in Fig. 18.37. A wide and short sound port helps to move this peak toward higher frequencies.

Total harmonic distortion (THD) measures the alteration of the signal frequency content. It is given by the formula

$$\mathrm{THD} = \frac{\sqrt{A_2{}^2 + A_3{}^2 + A_4{}^2 + A_5{}^2}}{A_\mathrm{F}} \tag{18.17}$$

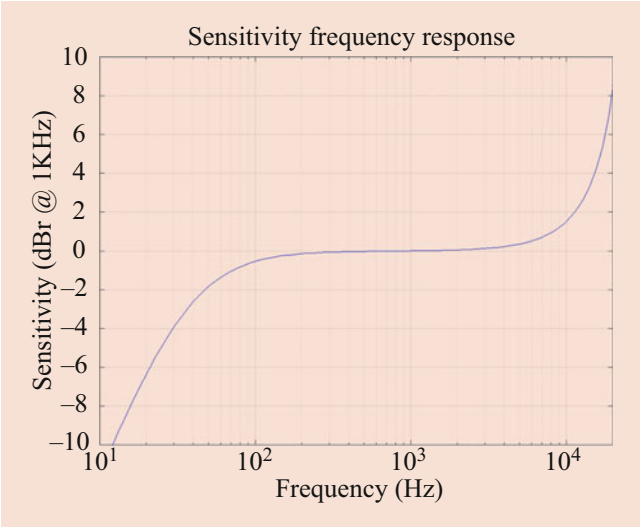

Fig. 18.37 Typical MEMS microphone frequency response. (© 2018 by STMicroelectronics)

where A_f is the amplitude of the fundamental component and $A_2, A_3, \ldots, A_\mathrm{n}$ are the amplitudes of the second, third, …, nth components, respectively. Usually, first five harmonics are included. For a signal at 1 kHz, state of the art for THD is below 0.1% at 94 dBSPL and below 4% at 130 dBSPL. Main contributors to THD are sensors' intrinsic transduction nonlinearity and amplifier nonlinearity.

Signal-to-noise ratio (SNR) is the ratio between sensitivity at 1 kHz and integrated noise floor in audio band (A-weight is usually applied). Noise contributions come from both sensor and ASIC. Sensor noise is generated by different dissipation mechanisms, both acoustic-mechanical and electrical: the most important are fluidic squeeze film damping in capacitive microphones and material losses in piezoelectric microphones.

Package strongly influences microphone performances. Cap cavity adds a backchamber compliance in series to membrane compliance. Backchamber is an additional stiffness that opposes to membrane movement, therefore affecting sensitivity. Backchamber compliance is defined as [48]

$$C_\mathrm{back} = \frac{V_\mathrm{back}}{\rho c^2} \tag{18.18}$$

where V_back is backchamber volume, ρ is air density, and c is speed of sound in air.

Therefore, the larger its volume, the lower the stiffening effect. To increase sensitivity, backchamber volume should be as large as possible: there is an evident trade-off with package miniaturization.

Another acoustic effect related to package is the high-frequency resonance peak described before, physically corresponding to a Helmholtz resonator, due to sound inlet and

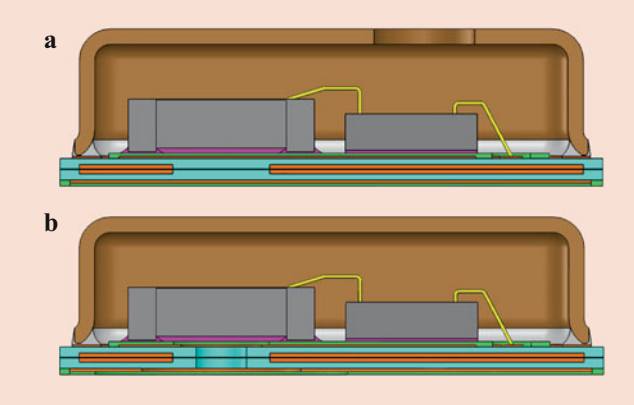

Fig. 18.38 (**a**) Scheme of a top port MEMS microphone. Sound inlet is located in cap. Backchamber is MEMS cavity. (**b**) Scheme of a bottom port MEMS microphone. Sound inlet is located below MEMS. Backchamber is the whole package volume. (© 2018 by STMicroelectronics)

frontchamber. In order to shift the resonance peak toward higher frequencies, frontchamber volume must be as small as possible, and sound inlet should be short and wide.

Microphone packages can adopt a top port or bottom port configuration, as shown in Fig. 18.38. The former has sound inlet in the cap, frontchamber is package inner volume, and backchamber is MEMS internal cavity. The latter has sound inlet in the substrate, below MEMS, frontchamber is MEMS internal cavity, and backchamber is package inner volume.

From what was discussed before, bottom port configuration gives better performances, both in terms of higher sensitivity (larger backchamber) and flatter frequency response (smaller frontchamber, corresponding to high-frequency resonance peak).

To understand microphone behavior and interactions between MEMS and package, it is possible to exploit an electromechanical-acoustic analogy. Interested readers can find more details in Ref. [46–48].

18.8.2 Capacitive MEMS Microphones

Capacitive sensing is the most widely used sensing principle in MEMS sensor industry. It is by far the most successful example of sensors.

A capacitive MEMS microphone is a capacitor where one of the plates is fixed and the other one is the membrane: its movement induces a capacitance variation.

In first approximation, MEMS sensor can be modelled as a parallel plate capacitor. Since plate area is much larger than air gap thickness, capacitance can be calculated as

$$C = \frac{A\varepsilon_0}{d_0 - kP} \tag{18.19}$$

where A is capacitor area, ε_0 is vacuum dielectric constant, d_0 is the initial air gap thickness, k is the equivalent mechanical spring constant of the membrane, and P is the applied acoustic pressure.

Under a sound pressure, membrane movement changes plate distance and capacitance varies accordingly. Capacitance is inversely proportional to displacement, i.e., the relation is nonlinear.

For small gaps, the capacitance change as a function of the displacement can be very large, making this technique suitable for high-resolution sensing of small displacements.

For a capacitor,

$$Q = C * V \tag{18.20}$$

If a constant charge is stored on the plates, a variation of C induces a variation of V: this voltage signal is read by the ASIC and further processed if needed. Constant charge is provided by the ASIC through a charge pump.

The basic structure of a capacitive microphone comprises several elements. A movable membrane acts as the first plate of the capacitor. Many geometries are possible and the membrane can be fully clamped on its entire perimeter or suspended via springs or bumps. Membrane design, materials, and thickness have a strong impact on microphone sensitivity.

The second plate of the capacitor is known as backplate. It must be much stiffer than the membrane since it is the reference side of the capacitor. Therefore, backplate is usually thicker and comprises a large number of acoustic holes for air to pass through. Both membrane and backplate must be conductive or comprise at least one conductive layer (electrode).

Between the two plates, an air gap is present: its thickness defines microphone sensitivity too. The air gap is fabricated using a sacrificial layer, removed at the end of the process.

A ventilation hole must be included to reject ambient pressure. In case of suspended membranes, any small gap between membrane edge and anchored area acts as a ventilation hole: generally, an overlap between membrane and substrate is present, and roll-off point can be controlled with a proper choice of overlap length and distance between membrane and substrate. Holes on membrane can also be added, in case of both suspended and fully clamped membrane.

MEMS sensitivity is determined by:

- Capacitance value, related to membrane area and air gap thickness.
- Membrane mechanical compliance, set by its thickness, residual stress, and spring geometry (if springs are present).
- Backchamber volume.
- Bias applied on the two plates.

ASIC applies a variable bias, so providing a sensitivity tuning. At final test, natural sensitivity of the microphone is measured and calibrated adjusting bias, in order to match tight sensitivity specifications.

All fluidic resistances are associated to a noise source. Main noise sources in the sensor are due to squeeze film damping. Figure 18.39 reports a typical power density spectrum of the different noise sources in the MEMS. A first noise source is the thin air gap between membrane and backplate. Proper design of acoustic holes in the backplate can minimize damping, but there is a trade-off between noise reduction and sensitivity (the larger the holed area, the less the capacitance area). An additional squeeze film damper is the ventilation hole, if membrane edge is not clamped. Sound inlet is a noise source too, even if generally less important.

Since noise is integrated in audio band, resonance peak position plays an important role. Noise transfer function has a resonance peak in the same position of sensitivity transfer function. Therefore, if resonance peak is close to the center of the band, integrated noise value will be higher than if the peak is close to band edge or outside audio band.

Final microphone SNR will depend on both MEMS noise, described above, and ASIC noise.

A typical process flow for capacitive microphones, illustrated in Fig. 18.40, comprises at first a deposition or growth of a first sacrificial layer and its patterning (a): a common choice is silicon oxide. Then the membrane is deposited and patterned (b): this layer must be conductive to act as the movable plate of the capacitor. A common choice is polysilicon or a stack of polysilicon and silicon nitride. This step is followed by deposition and patterning of a second sacrificial layer (c). Thickness of this layer will define air gap thickness. Silicon oxide is often used. Then the backplate is fabricated (d). Materials are usually polysilicon, silicon nitride, or a stack of the two. Silicon substrate etch allows opening a cavity below the active structure (e). This cavity is mandatory to allow sound to flow. Deep reactive ion etching (DRIE) or wet silicon etch can be used. Final release is used to free movable parts (f). HF wet etch is typically used for silicon oxide sacrificial layers.

18.8.3 Piezoelectric MEMS Microphones

Piezoelectricity is a property of several materials with noncentrosymmetric crystal structure. In these materials, a deformation of the structure can change the distance between the atoms, thus creating a polarization and a nonzero electric field (and vice versa).

In a piezoelectric material, a strain across the material induces a charge piling upon its surfaces (direct piezoelectric effect). On the other hand, when an electric field is applied, this generates a variation of strain in the material and, generally, a variation in its geometrical dimensions (converse piezoelectric effect).

Piezoelectric material can be integrated in silicon technologies as thin films: PZT (lead zirconate titanate) and AlN (aluminum nitride) are the most common materials.

Piezoelectric fundamental equations can be written in different forms. We just recall the linear equations in stress-charge form:

$$D_k = e_{kij} \cdot S_{ij} + \varepsilon_{ki} \cdot E_i \tag{18.21}$$

$$T_{ij} = c_{ijkl} \cdot S_{kl} - e_{kij} \cdot E_k \tag{18.22}$$

where D is the electric displacement vector, e is the piezoelectric constants matrix, S is the strain tensor, T is the stress tensor, ε is the dielectric constants matrix, c is the elastic constants matrix, E is the electric field vector in the material, and i, j, and k are matrix indices. From these equations, there is a full electromechanical coupling, i.e., both stress and electrical displacement depend simultaneously on mechanical properties (strain) and electrical properties (electric field). The piezoelectric coefficients e couple strain and electrical displacement: the larger these coefficients, the higher the charge piled up at a given strain.

Piezoelectric MEMS microphones exploit direct piezoelectric effect. A piezoelectric material is present somewhere in the sensor movable area. Membrane movement induces a strain inside the piezoelectric material and this generates charge piling up on the electrodes. Usually microphones are made of movable cantilevers or membranes. Piezoelectric material is on top of these mechanical elements, sandwiched between a top and a bottom electrode. Therefore, the most important piezoelectric coefficient is e_{31}, coupling in plane strain (due to thin structure deflection) and electrical displacement along Z-axis.

Typical embodiments of piezoelectric microphones are cantilever-like structure (not necessarily of rectangular shape) or membranes where piezoelectric material is deposited in the regions where strain is higher. Proper placement of the piezoelectric material is needed to achieve acceptable sensitivity and good linearity. Multilayers of piezoelectric material can be used to increase conversion efficiency. Sometimes the whole structure is made only of the piezoelectric stack, without any sustaining layer.

Most of the acoustic considerations done for capacitive microphones are valid for piezoelectric microphones too. Particularly, the interactions with the package are the same and the need for a ventilation hole is still present. This can be a hole in the membrane or can be the gap between different cantilevers.

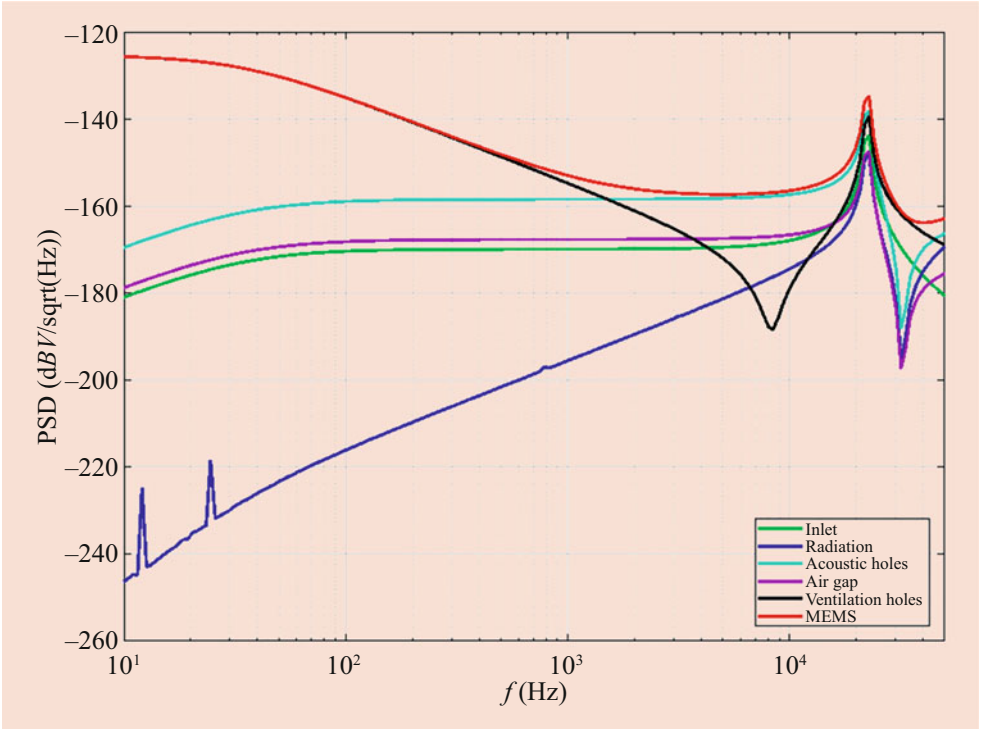

Fig. 18.39 Example of MEMS noise power spectral density. Each line is the contribution of a MEMS element; red line is total MEMS noise PSD. (© 2018 by STMicroelectronics)

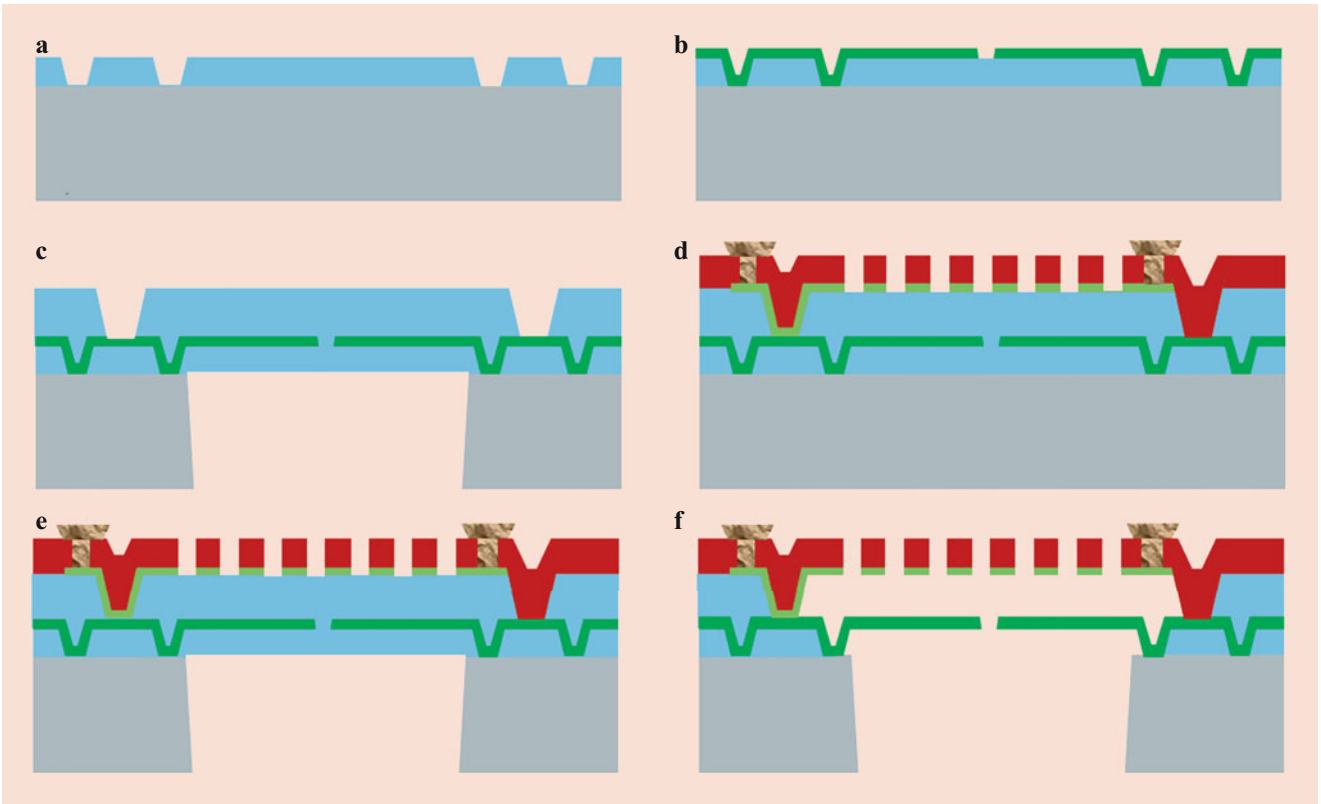

Fig. 18.40 Typical process flow for a capacitive MEMS microphone. Details of each figure in the text. (© 2018 by STMicroelectronics)

As far as noise is concerned [49], piezoelectric microphones generally have just one layer; therefore no squeeze film damping is present. On the other hand, main noise source in these microphones is piezoelectric material losses, i.e., unwanted charge flow from the electrode due to deviation of the piezo layer from the ideal dielectric. For this reason,

AlN is the preferred solution for microphones due to its very low material losses. This noise source can be modelled as a current generator in parallel with piezo capacitance and resistance. Resistance value is given in

$$R_p = \frac{1}{2\pi f C_p \tan(\delta)} \tag{18.23}$$

where f is frequency, C_p is capacitance of the piezoelectric element, and $\tan(\delta)$ is a parameter related to material losses. Noise therefore depends on both material properties and capacitance value.

MEMS sensitivity in piezoelectric microphones is determined by both piezoelectric coupling efficiency and acoustic and mechanical effects. Therefore, sensitivity depends on:

- Capacitance value, related to piezoelectric material area and thickness.
- Piezoelectric coefficients.
- Structure mechanical compliance, set by thicknesses, residual stresses, geometry of springs, and piezo stack.
- Backchamber volume.

No bias is applied by ASIC and sensitivity trimming is achieved only by changing amplifier gain. Proper control of residual stresses, affecting mechanical sensitivity, and piezoelectric coefficients is mandatory.

A typical process flow for piezoelectric microphones, illustrated in Fig. 18.41, comprises deposition or growth of a first sacrificial layer and its patterning (a): a common choice is silicon oxide. Then the active structure is fabricated (b). There can be a mechanical layer with piezoelectric stack on top in selected areas, or the whole structure can be made directly of the piezoelectric stack. Piezoelectric stack is generally made of a bottom electrode, piezoelectric layer, and a top electrode (c). Most common choice for piezoelectric material is AlN due to its very low losses. Common choices for electrodes are Mo and Ti. Multiple stack are possible: usually only unimorph or bimorph stacks are adopted due to technological complexity. Silicon substrate etch allows opening a cavity below the active structure (d). This cavity is mandatory to allow sound to flow. Deep reactive ion etching (DRIE) or wet silicon etch can be used. Usually, final release to free movable parts is not necessary, since there is just one single layer. Therefore, cavity opening is usually sufficient to release movable structure.

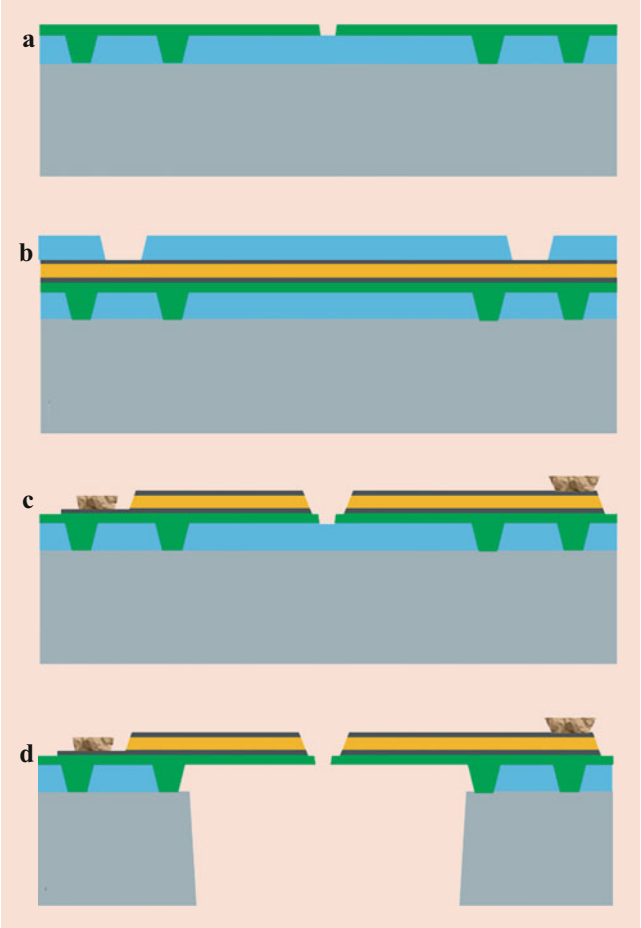

Fig. 18.41 Typical process flow for a piezoelectric MEMS microphone. Details of each figure in the text. (© 2018 by STMicroelectronics)

18.8.4 Reliability Challenges for MEMS Microphones

MEMS microphone qualification strategy involves both standard ICs tests and dedicated tests based on customer requests. In tests based on standard specifications, common to ICs, test conditions are defined by standards, and parts are measured in socket using standard final testing equipment. Some examples of standard test are HTOL (high temperature operating life), HTSL (high temperature storage life), TC (thermal cycles), ESD&LU (electrostatic discharge and latch-up), and so on.

Tests based on customer specification are usually carried on with parts soldered on quality boards and tested with a dedicated bench setup. Frequently, these tests are aimed to mechanical robustness. Some examples are MS (mechanical shocks), VFV (variable frequency vibrations), free fall, and CAT (compressive air test).

Main failure mechanism for MEMS microphones is contamination. Whereas inertial sensors are hermetic, microphones have a cavity package and a hole in the substrate or in the cap (sound port) and therefore are more exposed to external contamination. This contamination is killer for microphone functionality in terms of reduced SNR and sensitivity. Proper choice of assembly line class is therefore very important.

Another possible failure mode is cap detachment in the cavity package. Cap detachment is typically caused by mechanical overstresses but can also be caused by thermal stresses. Some examples of possible mechanisms causing cavity detachment are:

- Incomplete dispense of the solder paste or glue.
- Wrong reflow profile: if the reflow profile differs from the standard one, the glue on the package can be weakened, losing its fixing capability.
- Free fall over a rigid surface from more than 1 m.
- Wrong cut line in the separation of single components from the strip.
- Force exceeding a threshold (typically 2.5 g) for tape removal.

In the case of cavity detachment, a fail in any audio parameter (sensitivity, SNR, frequency response, THD) can be observed.

Another key aspect for quality and reliability of microphones is mechanical robustness. Smartphones are the main application of MEMS microphone and mechanical overstress related to drop event is common in the field: for this reason phone makers have defined specific tests, such as guided free fall test and tumble test. Such tests are performed with components mounted on a dedicated board with cover to simulate the phone dimensions and weight, in order to reproduce the real mechanical stress on MEMS and to investigate possible failure mechanisms related to package and solder joint reliability. Due to its very thin thickness, broken membrane is one of the main experienced failure modes. Backplate breakage is also possible.

18.9 Pressure Sensors

Pressure sensors have long been in service measuring pressure and flow in a variety of industrial, automotive, and medical applications. Micro-machined pressure sensors are fabricated in silicon with the physical sensing mechanism being either a variable resistance or a variable capacitance. The interface circuitry that converts resistance to voltage or capacitance to voltage can be integrated at chip level or at package level, as for motion sensors. The system in package solution guarantees faster commercialization time and higher flexibility for the customer.

18.9.1 Pressure Sensors Introduction

The fabrication of pressure sensors is either bulk or surface micromachining or a combination of the two. Standard silicon substrates or more expensive silicon-on-insulator substrates are equally used as a starting point [50].

The variable capacitance pressure sensor uses two parallel plates. One is fixed and the other is a thin diaphragm moving in an orthogonal direction to the plane of the chip under the pressure load. A very small change in capacitance then occurs between these two plates. Surface micromachining methods are preferred for this class of pressure sensors.

Piezoresistivity is among the oldest material properties used for the implementation of micro-machined silicon transducers. Since Charles Smith discovered at Bell Labs in 1954 [51] the exceptionally large resistance change in silicon and germanium samples, industry has produced increasingly complex sensors based on piezoresistivity with strain, force, pressure, acoustic, and inertial applications. All piezoresistive transducers operation is based on the deformation due to a load of a mechanical structure, on which piezoresistors are implanted or attached. Typically, a Wheatstone bridge is used to measure the resistance change by converting it in a voltage. Depending on the application, the form and the extension of the piezoresistors will vary together with the mechanical structure subject to the load.

The variable resistance pressure sensor uses the piezoresistive nature of silicon to convert stress in a small diaphragm into a very small resistance change. Bulk micromachining technology was for long the preferred technique. In the last 15 years, companies like Bosch [52] and STMicroelectronics have introduced single wafer surface micromachining processes to create a single crystal silicon membrane and vacuum cavity without any bonding steps.

No ideal manufacturing process exists, but each company follows the micromachining approach that best exploits its experience and its manufacturing assets. Nonetheless, because of the plethora of processes running in different semiconductor fabs, payers in the high-volume consumer market had to accept compromises related to price, size, and performance of the pressure sensor.

The first miniaturized devices had relatively low performance if compared with today's standards. Conventional silicon/glass pressure sensors were fabricated by anodic bonding technique, which translates in output instability in terms of offset drift, hysteresis over temperature, and humidity due to thermal mismatch or bonding interface built-in stress.

18.9.2 VENSENS™ Pressure Sensor

After the introduction of single wafer monolithic membranes, the consumer market became approachable for inexpensive packaged pressure sensors. The VENSENS™ process for pressure sensors by STMicroelectronics enabled high-volume production with 2.5 × 2.5 × 1 mm^3 package. A monolithic MEMS die, shown in Fig. 18.42, with a small

footprint (0.7 × 0.7 × 0.3 mm^3) combined with an ASIC was able to detect the altitude with good accuracy (±1 mbar) over the full temperature (−40 to 85 °C) and pressure (260–1260 mBar) range.

The VENSENS™ process begins with a standard silicon wafer. A proprietary process with successive steps of dry silicon etching, silicon epitaxial growth, and annealing enables the formation of a vacuum cavity layer with on top a single crystal silicon layer. (Fig. 18.43).

The thickness of the vacuum cavity can be tuned to be in the order of few micrometers and the same holds for thickness of the structural layer. The result is very similar to what is possible to get with bulk micromachining wafer-to-wafer bonding, but the big advantage is to have thinner, smaller, and mechanically more robust chips. Moreover, the sealing of the cavity requires no wafer-to-wafer bonding and thus the reliability of the sealing joint is definitely higher.

Because of the superior electrical properties of the monocrystalline silicon, high-quality, stable resistors can be integrated in the structural layer through implantation or diffusion process. Then these resistors are connected with an aluminum metal layer to realize the four branches of a Wheatstone bridge. The bridge is sensitive to pressure changes due to the excellent piezoresistive properties of the monocrystalline silicon layer.

The metal layer is then covered with a standard dielectric, like silicon oxynitride, to provide the required protection against the external corrosive agents.

18.9.3 Bastille™ Pressure Sensor

In addition to the fabrication cost, the sensor performance including output stability has become more and more an important concern. Applications like health and fitness monitoring, indoor and outdoor tracking altimetry, require more and more require accurate devices down to the centimeter of altitude error. In cost-effective consumer microsystem packaging, the sensor is soldered onto a printed circuit board (PCB). Traditional glue-stacked MEMS sensors easily suffer instability induced by packaging stress and thermal drift of the sensing signal. Temperature compensation methods are thus necessary, making the calibration stage the cost bottleneck of these high-volume devices.

Additional to the in-house calibration, soldering subjects a multi-stack device to thermal and mechanical constraints on the composing materials each with different recovery time constraint resulting in a time-varying drift that will compromise the above calibration performance.

Leveraging the VENSENS™ MEMS technology, STMicroelectronics commercialized in 2014 a full molded pressure sensor with only 2 × 2 × 0.7 mm^3 footprint. This technology eliminates the need for soft glue and plastic or metal caps by taking the decoupling task inside the MEMS. The membrane is suspended with a silicon spring, which acts as electrical interface as well. In this structure, thermomechanical external stresses related to soldering are absorbed by the spring resulting in a membrane located inside a stress-free area (Fig. 18.44).

Taking the decoupling complexity inside the MEMS permits to rely on the excellent linearity of silicon springs for drift-free pressure sensors and enables silicon-exposed cost-effective full molded package. The device features a typical absolute accuracy as high as 0.1 mBar in the range of 0–65 °C.

18.9.4 Reliability Challenges for MEMS Pressure Sensors

Main failure mechanisms for pressure sensors can be highlighted by the following reliability trials:

1. Reflow or THS (temperature humidity stress).
2. Mechanical stress test, like tumble or drop.
3. HAST (highly accelerated temperature and humidity stress test) [53] or autoclave [54].

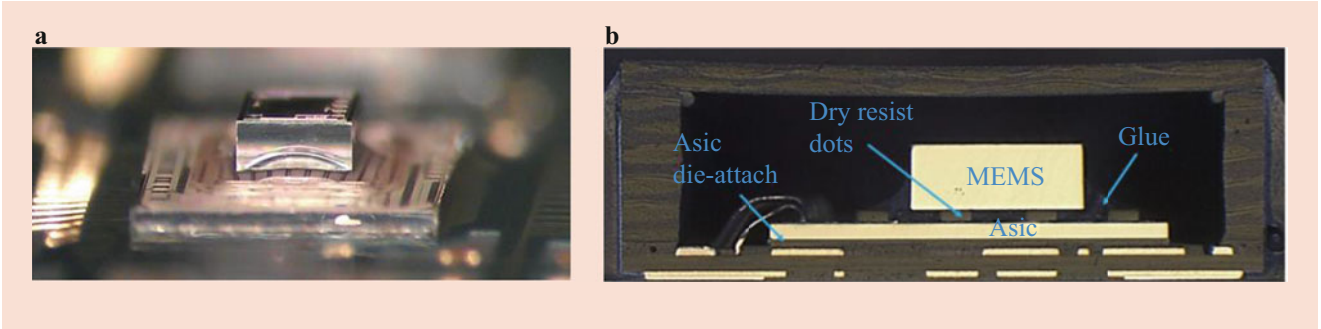

Fig. 18.42 (**a**) The VENSENS™ piezoresistive pressure-sensing element by STMicroelectronics, soft glue edge visible. (**b**) Package cross section together with ASIC cap and substrate (right). (© 2018 by STMicroelectronics)

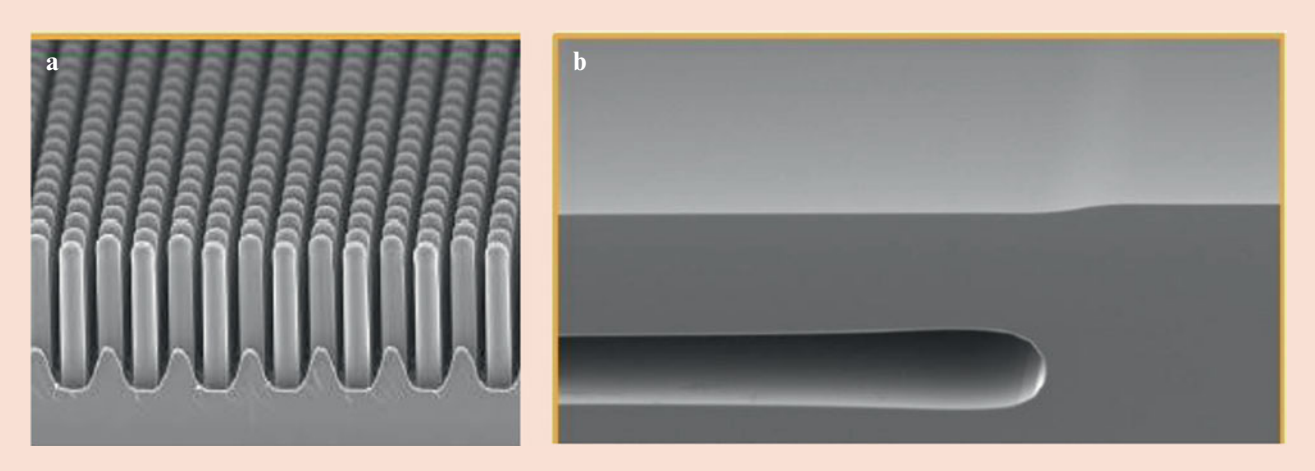

Fig. 18.43 (**a**) Dry etching of silicon pillars for cavity and membrane definition. (**b**) FIB (focused ion beam) cut of resulting single silicon crystal membrane and cavity on the right. (© 2018 by STMicroelectronics)

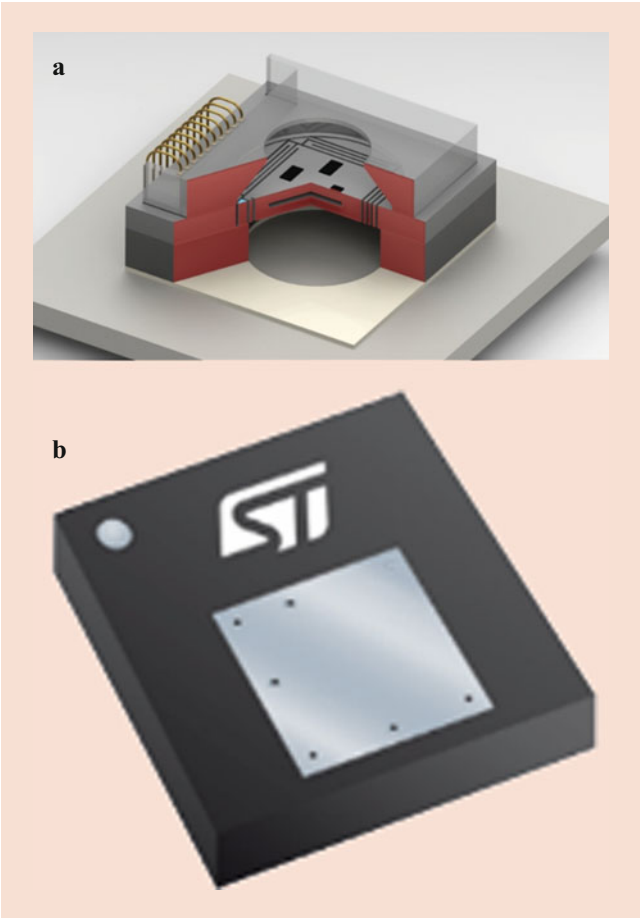

Fig. 18.44 (**a**) 3-D model of suspended membrane showing the springs around the piezoresistor's area (black rectangles). The organic substrate and the wire bonding are visible. (**b**) Full molded HLGA ($2 \times 2 \times 0.7$ mm^3) top view. Top surface shows exposed silicon and small vent holes. (© 2018 by STMicroelectronics)

Typically, after the test a readout is performed to assess accuracy drift. Some of these tests are specific for environmental sensors; others belong to the standard JEDEC flow.

Typical failure mechanisms are particles and corrosion.

A particle, which is a portion of material of a variable dimension, can be generated by process manufacturing flow or penetrate from the environment through the vent holes located on silicon cap. When they reach sensor area, they can potentially cause a pressure accuracy drift. Generally, this issue can be detected applying a thermal stress (reflow simulating soldering process).

Another possible failure mode is related to corrosion and can be studied via HAST or autoclave, also known as pressure cooker test (121 °C/100% RH). These tests are able to activate any potential leaky path through the whole structure, causing the contact between humidity and the exposed metal. Damages induced by corrosion cause electrical malfunction, typically an accuracy drift of a physical dimension (pressure, in our case).

Thanks to proper qualification process, very low return rates can be achieved. For pressure sensors, one-digit ppm (parts per million) return rate has been reached. Reliability plan includes both tests based on international standards (e.g., JEDEC) and customized trials with the aim to stress mechanical elements.

18.10 Magnetometers

Several different technologies and transduction mechanisms are used to measure magnetic field, since different applications require different sensor features.

18.10.1 Magnetometers Introduction

For instance, an e-compass needs a sensor highly sensitive and accurate in order to resolve the Earth's magnetic field change of direction, which means capability to solve very small fields, in the range of few hundreds of nT. Just as an example, an accuracy on field better than 0.4 μT is mandatory to guarantee a heading accuracy better than 1 degree at temperate latitudes. Full scale for e-compass from 1.6 mT to 5 mT is enough, just to avoid saturation in case of disturbing fields superimposed to the Earth's field.

On the other hand, magnetic sensors very appealing for industrial and automotive applications, like current or position sensors, have generally to measure larger magnetic fields and require larger full scale, i.e., tens or even hundreds of mT. In this cases, the magnetic sensor is generally placed quite close to the source of magnetic field (a magnet in the case of position or angular sensor, or a current line) in order to work in a region where the field to be sensed is larger enough than the expected disturbing fields. Also for these sensors, accuracy is important, but, differently from the case of compasses, it is possible to play with relative position with respect to the magnetic field source.

Furthermore, for some applications, like e-compass or position sensing, the possibility to sense magnetic field in any direction (three-axis) is mandatory, while for angular sensors two-axis sensing is generally enough, and for current sensing a mono-axial sensor is usually employed.

Among the transduction mechanisms exploited for magnetic sensing, magnetoresistive sensor (anisotropic, tunnel, or giant magnetoresistive sensor: AMR , TMR, and GMR, respectively) is particularly suited to solve small magnetic fields, as required by compass application. Indeed, combining high performing magnetic sensors based on magnetoresistors with three-axis accelerometer is possible to obtain six-axis modules especially suited for e-compass.

Furthermore, magnetoresistors can be employed also as angular sensors, as they are intrinsically sensitive to the direction of internal magnetization of a ferromagnetic layer and thus to the external magnetic field angle with respect to a reference direction. On the other hand, since magnetoresistances saturate for small magnetic fields, other technologies as Hall sensors are much more suited for position or current sensing. Since Hall sensor is based on a well-known working principle and can be easily integrated even in the same chip with electronic circuits used for processing sensor signal, they are very popular even for applications in which the Hall sensing is limited by its small sensitivity, as e-compass.

Hall effect and magnetoresistivity are the main transduction mechanisms employed in products for magnetic sensing provided by semiconductor companies, like STMicroelectronics, Infineon, Allegro, NXP, AKM, and Melexis. Other interesting mechanisms of transduction are based on the change of magnetization of a magnetic core in an inductance (magneto-inductive sensors) or in a core of a transformer (fluxgate). In the first case, it is possible to monitor the frequency of an LC tank whose L changes due to magnetization induced by the external magnetic field to be sensed. In the case of fluxgate, the transduction mechanism is more complicated and based on the change of coupling between primary and search coils, due to magnetization of the core induced by the magnetic field to be sensed.

Magneto-inductance and fluxgate can be very accurate and sensitive to small magnetic fields; thus they have been proposed for compass but generally require a larger power consumption and larger dimension than other magnetometers. Furthermore, in their version compatible with typical semiconductor fabrication processes, they can be at most two-axis sensitive.

A last interesting transduction mechanism for magnetic field leads to the only magnetometer that is really a MEMS, in the sense that is based on moveable parts. This last mechanism is based on Lorentz force. If a current line of length l is designed on a moveable part, it is possible to generate a force $\boldsymbol{F}$ on the mass, by driving a current $\boldsymbol{I}$ at a proper frequency, when an external magnetic field $\boldsymbol{B}$ is directed in proper direction:

$$\boldsymbol{F} = l\boldsymbol{I} \times \boldsymbol{B} \tag{18.24}$$

In this way, the movement of the mass is proportional to the magnetic field to be detected, modulated by the current signal driven by a proper ASIC conditioning the sensor. A signal proportional to the movement can be extracted via a capacitive sensing as typically done for inertial sensor and then demodulated to extract a signal proportional to the magnetic field. The driving frequency can be at resonance frequency or at a chosen mismatch to optimize sensor performance. Main semiconductor companies do not use Lorentz force magnetometers in their products, but very good performance has been shown in recent publications [55].

In the following, we will focus on the main sensing mechanism used in semiconductor industry to fabricate magnetic field sensors, i.e., Hall sensor and magnetoresistive sensors, with particular attention to AMR (Fig. 18.45).

18.10.2 Hall Sensors

Hall sensors work because of Lorentz force [55] too, but in this case, the force deflects the trajectory of electron or holes flowing in a semiconductor. Looking at the Lorentz force acting on the single charge q moving at a velocity $\boldsymbol{v}$, the force $\boldsymbol{F}$ deflects the trajectory of the charge according to

$$\boldsymbol{F} = q\boldsymbol{v} \times \boldsymbol{B} \tag{18.25}$$

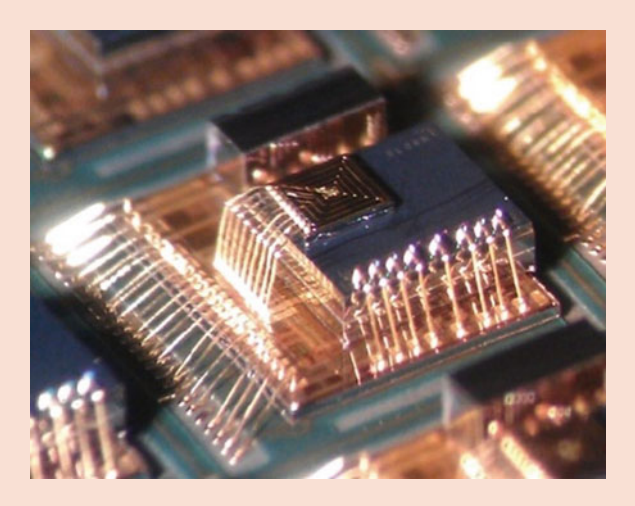

Fig. 18.45 Example of 6× modules for e-compass from STMicroelectronics (3× magnetometer + 3× accelerometer) in production from 2012. (© 2018 by STMicroelectronics)

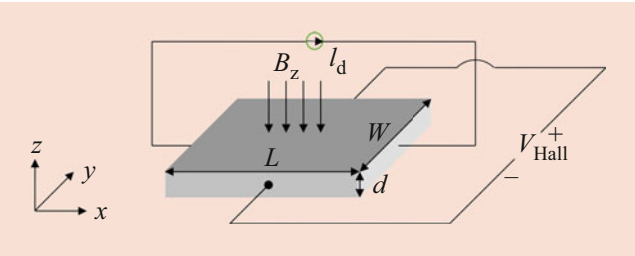

Fig. 18.46 Ideal structure for a Hall sensor. (© 2018 by STMicroelectronics)

Now, considering a flow of charges in a semiconductor plate as in Fig. 18.46, if a current I_d flows between two terminals of a four-terminal structure, at the other two terminals, electric fields perpendicular to current flow are generated by the charge distribution change, due to Lorentz force-induced trajectory deflection.

It is possible to calculate the hall voltage V_{hall} starting from previous equation and fixing the condition of equilibrium between electric field and Lorentz force. In case of a bias current, I_d, we have

$$V_{hall} = \frac{1}{qnd} I_d B_z \tag{18.26}$$

where n is the number of charge q flowing in the plate, d the plate thickness, and B_z the magnetic field perpendicular to the plate. In case of driving a voltage V_d instead of a current, we have the equivalent formula:

$$V_{hall} = \frac{1}{qnd} I_d B_z = \mu \frac{W}{L} V_d B_z \tag{18.27}$$

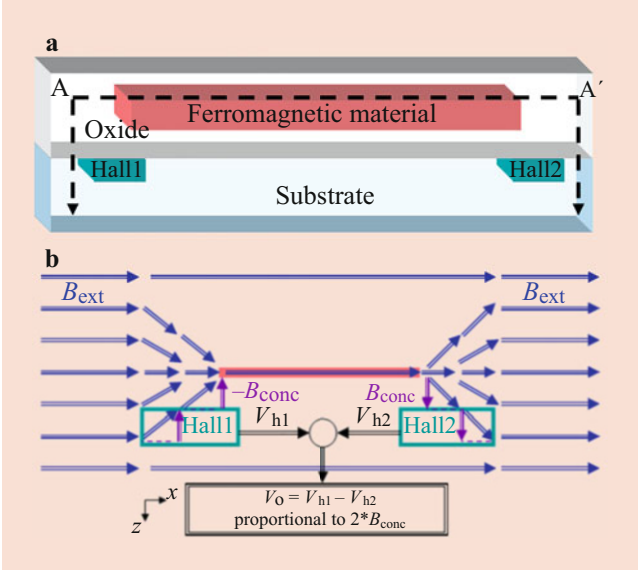

Fig. 18.47 Working principle of a magnetic field sensor based on hall sensor with an integrated magnetic concentrator. (© 2018 by STMicroelectronics)

where W is plate width, L the length, and μ the carrier mobility.

A Hall sensor is easily implemented in a silicon-integrated process, by introducing a diffused well, or by using a well already available in the process. The well is a region of silicon with a majority of carrier n type or p type. Generally, to maximize the mobility of the carrier and thus sensitivity, n-type well is used with a low concentration of dopants.

In this way, Hall sensor can be used to detect magnetic field perpendicular to the chip (Z-axis), but not parallel to the chip (X and Y). This could be a limit, for example, if three-axis sensing is required, as in case of position sensing and compass. A common solution [56] is to integrate on top of the chip a ferromagnetic patterned layer able to deflect planar magnetic flux line so that part of the magnetic field is deflected in direction perpendicular to the chip (Fig. 18.47) and, finally, the Hall sensor can sense fields parallel to chip surface. By properly placing a couple of Hall sensors with respect to the ferromagnetic material, in-plane magnetic component generates magnetic field of opposite sign on the two hall cells, so that the effect due to the magnetic component perpendicular to the chip can be rejected as a common mode.

18.10.3 Magnetoresistive Sensors

Magnetoresistive sensors are based on ferromagnetic materials whose resistance depends on magnetization direction with respect to the current, or on a stack of ferromagnetic layers, whose resistance depends on the orientation of a

soft ferromagnetic layer with respect to a reference hard ferromagnetic layer.

In the first case, we speak about anisotropic magnetoresistance (AMR), while in the second we have tunnel magnetoresistance (TMR, also known as magneto-tunnel junction MTJ) and giant magnetoresistance (GMR).

AMR are generally made of NiFe resistors, whose resistance changes due to the angle θ between magnetization vector M and current density J flowing in the resistor. The resistance R can be written approximately as [57]

$$R = R_0 - \Delta R \sin^2\theta \tag{18.28}$$

where $\Delta R/R_0$ is the maximum change in resistance, which can vary from 2% to 3% for NiFe, depending on thickness and fabrication. In other words, when magnetization and current are perpendicular to each other, scattering for carriers in the resistor is minimum and so is the resistance, while when magnetization is parallel or antiparallel to current, the scattering is higher, and resistance is maximum. Typically, AMR are made of thin sputtered NiFe layer of thickness in the range of tens of nm.

On the other hand, GMR and TMR are basically stacks of at least three layers: a ferromagnetic hard layer, a nonmagnetic layer, and a soft magnetic layer. Current conduction occurs trough the nonmagnetic layer, which can be an electrical conductive layer in the case of GMR, or a thin insulating layer in case of TMR, so that in the first case a standard current conduction occurs while in the second case a tunnel-effect conduction takes place. In the most simplified structure (Fig. 18.48), the first ferromagnetic layer is a hard ferromagnetic material, also known as pinned layer, which shows very high coercive field, i.e., requires a very huge external magnetic field to change direction and or magnitude of magnetization. Thus, it cannot be changed by an external magnetic field and it is fixed during the fabrication process, unless such a field is extremely high. Instead, the second ferromagnetic layer, the free layer, can change direction under the effect of an external magnetic field in the range of measurements of the sensor. Therefore, resistance changes due to the interaction between magnetization and the electron spin. Considering electrons with spin 1/2 and spin −1/2, scattering of electrons at each interface is dependent on magnetization direction and spin, so that if pinned layer and free layer have magnetization antiparallel direction, electrons with positive spin are scattered back at the first interface, while electrons with negative spin are scattered back at the second interface. On the other hand, if the magnetizations are parallel, at least one of the two groups of electrons (positive or negative spin) is much less affected by scattering, so that the resistance is significantly reduced going from an antiparallel to a parallel direction of magnetization [57, 58]. Practically the free layer magnetization rotation can close or open a valve for the electron passage. Typically, GMR/TMR layers are very thin, in the range of few nm.

18.10.4 Anisotropic Magnetoresistive Sensors

AMR sensors exploit the fact that some materials as NiFe change their resistance depending on the angle between magnetization and current as shown in Ref. [58]. Nickel/iron ratio is usually set to have both good sensitivity ($\Delta R/R_0$) and low magnetostriction coefficient, i.e., to have no sensitivity to mechanical stresses introduced by the package. This is an important advantage with respect to Hall sensors, which show a non-negligible dependence on stresses through piezoresistive effect, being Hall sensor generally very similar to a diffused resistor as shown in the dedicated section. Typical nickel/iron ratio to obtain both good magnetic sensitivity and low sensitivity to stress is 81/19 [57].

NiFe layer for AMR is anisotropic in the sense that the hysteresis of film magnetization M vs magnetic field depends on the direction. Generally there is a direction, the so-called easy axis, along which the magnetization is easily aligned,

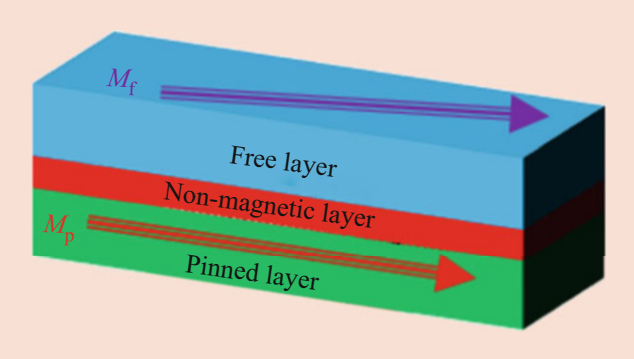

Fig. 18.48 Typical stack for a spin valve magnetoresistor (GMR, TMR). (© 2018 by STMicroelectronics)

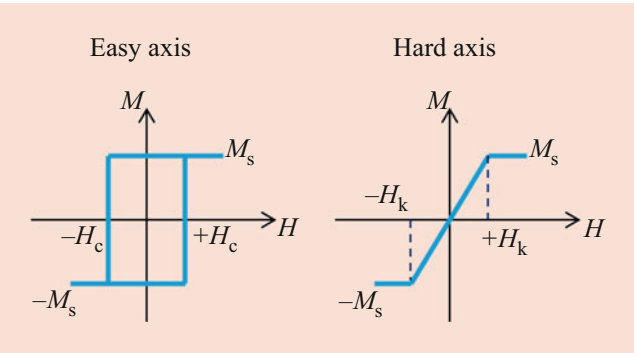

Fig. 18.49 Different behavior of magnetization vs magnetic field for easy and hard axis. (© 2018 by STMicroelectronics)

as well as a second axis, orthogonal to the first one, along which the relationship $M(H)$ is at least in a certain range linear and with very low hysteresis (Fig. 18.49). In a thin film, the easy axis direction lays always in-plane, i.e., parallel to chip surface.

The anisotropy/easy axis direction of a patterned layer is generally fixed by the contribution of material anisotropy and geometrical anisotropy [57–59]. Geometrical or shape anisotropy is due to the fact that in a patterned film, due to the discontinuity between ferromagnetic and not ferromagnetic material, layer magnetization inside the magnetoresistor is not uniform, but is reduced. This reduction can be modelled by a demagnetizing field. Without going too much into details of demagnetizing field calculation, if, for example, a magnetoresistor is much longer than wide (Fig. 18.50a), demagnetizing field is much larger along the width than along the length of magnetometer. Thus, geometrical anisotropy leads the preferred direction of magnetization along length of resistor, even if material anisotropy is in another direction. A magnetoresistor like the one in Fig. 18.50a, after a first magnetization cycle, would have a magnetization aligned along X or along $-X$. Thus if a field in sensitivity direction (Y) rotates M with respect to current J, a change of resistance would occur, according to chart in Fig. 18.50b. The only problem of a simple element like the one in Fig. 18.50b is that resistance as a function of the angle and, consequently, as a function of the external magnetic field is not linear. Moreover, a simple magnetoresistor like this cannot discriminate external magnetic field direction ($\pm\theta$ rotation gives the same resistance variation).

To obtain linearity and sensitivity to field direction, a solution is to use the so-called barber poles, i.e., a conductive and not ferromagnetic layer as copper or aluminum, with conductivity much higher than ferromagnetic layer used as magnetoresistor. By depositing this layer directly on the NiFe and by patterning barber poles at 45° with respect to the ferromagnetic layer, the current direction in the ferromagnetic layer is rotated following the barber pole orientation so that the angle between magnetization and current is 45°, when external magnetic field is 0 (Fig. 18.51a). As shown in Fig. 18.50b and following Ref. [58], around this working point, the dependence of resistance on angle is linear. Furthermore, playing on barber pole orientation is also possible to set the initial angle between magnetization and current to −45°. Therefore, still following Fig. 18.50b, it is possible to have a first set of magnetoresistor showing an increase of resistance for a certain magnetization rotation and a second group whose resistance decreases of the same value with the same magnetization rotation.

This allows to design four magnetoresistors, two with initial angle between magnetization and current to −45° and the other two with initial angle 45°. Consequently it is possible to connect these magnetoresistors in Wheatstone bridge configuration.

Another element useful for AMR sensor is the auxiliary coil to set the initial state of magnetization. A set of the

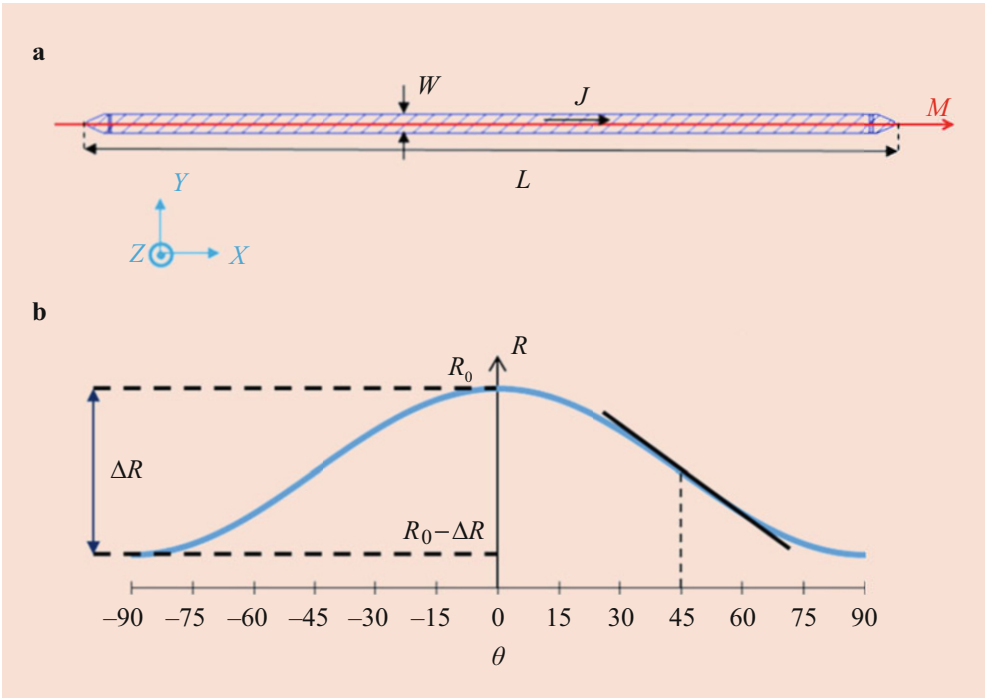

Fig. 18.50 (**a**) Example of AMR element, ferromagnetic layer only. (**b**) Typical behavior of such element vs angle between current and magnetization. (© 2018 by STMicroelectronics)

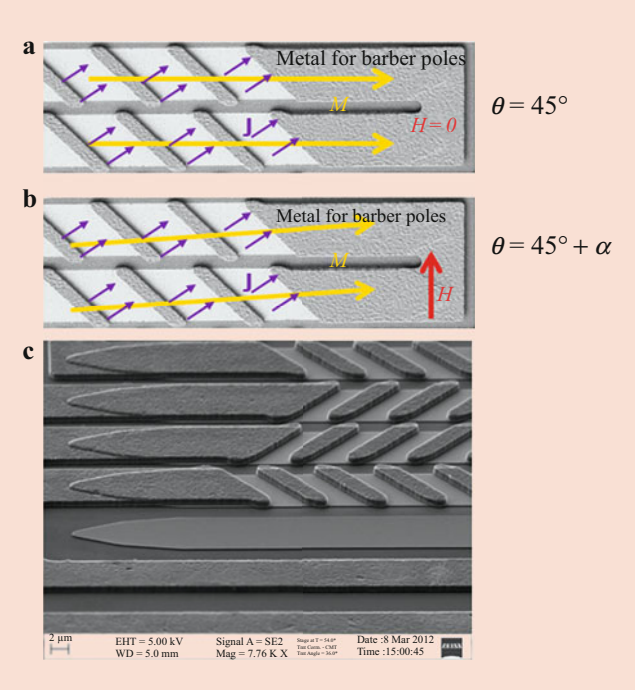

Fig. 18.51 Barber poles structure (dark gray layer) in a real STMicroelectronics sensor; added in purple the expected direction of current, in yellow magnetization, and in red external field. (**a**) Case with external magnetic field 0; (**b**) case with external field not zero; (**c**) perspective view of barber poles and NiFe stack from a STMicroelectronics device. (© 2018 by STMicroelectronics)

magnetization is required at the start-up of the sensor and periodically during sensor working to recover the correct operating point in case of high magnetic field exposure. A schematic example of the coil is shown in Fig. 18.52. When the magnetization set is needed, a short pulse of current is driven through the coil (direction following red arrows in Fig. 18.52) generating a pulse of magnetic field H_{set} (direction following black lines in Fig. 18.52). The amplitude of the pulse should be enough to set the magnetization M of the magnetoresistor and to ensure that it remains set after the removal of the pulse if external magnetic field is 0. Figure 18.53 shows a detail of a typical metal for set coil.

Set coil enables also another important feature of AMR sensors, i.e., the possibility to cancel the offset. Considering a magnetic field with a component H in sensitivity direction as in Fig. 18.52, after a set pulse, initial magnetization of the four magnetoresistors in the Wheatstone bridge is set so as the output of Wheatstone bridge and can be written as

$$V_{out} = SH + V_{offset} = \Delta R/R_0 * f\,(W, t, H_k)\;\; H + V_{offset} \tag{18.29}$$

where V_{offset} is the offset of the Wheatstone bridge, due to geometrical asymmetries among magnetoresistors and independent on magnetization condition of magnetoresistors, while S is the bridge sensitivity. Sensitivity is proportional to $\Delta R/R_0$ and to a function dependent on width W and thickness t of magnetoresistor, while length L is negligible if $L \gg W,t$. Sensitivity S depends also on the anisotropy field H_k, a magnetic property of the ferromagnetic film which can be defined as in Fig. 18.49 as the field required to saturate the flat film with a magnetic field oriented along the hard axis.

If, after a first measurement performed following the set pulse, a second current pulse is driven along the set coil in an opposite direction (reset pulse), the magnetic field pulse on Wheatstone bridge is in opposite direction with respect to the one in Fig. 18.52, so as magnetization direction inside magnetoresistors is reversed too. This results in a change of the initial angle between current and magnetization, which becomes 45° for resistor whose magnetization orientation was −45° after the first pulse, and −45° for resistor whose magnetization orientation was 45° after the first pulse.

Thus, sensitivity to H is still S but with opposite sign. If V_{os} is the output after the first (set) pulse and if V_{or} is the output after the second (reset) pulse, the two outputs are

$$V_{os} = SH + V_{offset} \tag{18.30}$$

$$V_{or} = -SH + V_{offset} \tag{18.31}$$

$$\frac{V_{os} + V_{or}}{2} = SH \tag{18.32}$$

The difference between these two consecutive measurements allows dynamically cancelling the offset, as well as its drifts and temperature dependence. Such AMR sensor feature is fundamental to obtain magnetometers with high accuracy.

18.11 Silicon Image Sensors and Evolutions of CMOS

Silicon is a material suitable for imaging application due to its crystalline properties and band structure. When light hits silicon, energy can be transferred to electrons generating a current flow and paving the way to a very wide range of applications for silicon imaging sensors.

18.11.1 Introduction

Silicon crystallizes into a diamond cubic crystal structure in which the atoms are covalently bonded. Silicon is a group IV element in the periodic table and is a semiconductor with a bandgap of 1.12 eV at 300 K. Semiconductors are

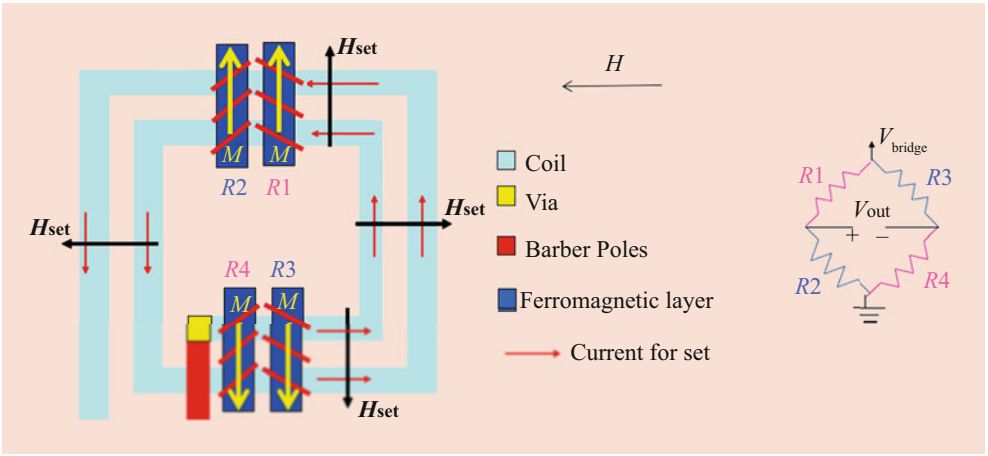

Fig. 18.52 Schematic representation of an AMR bridge with its set coil. (© 2018 by STMicroelectronics)

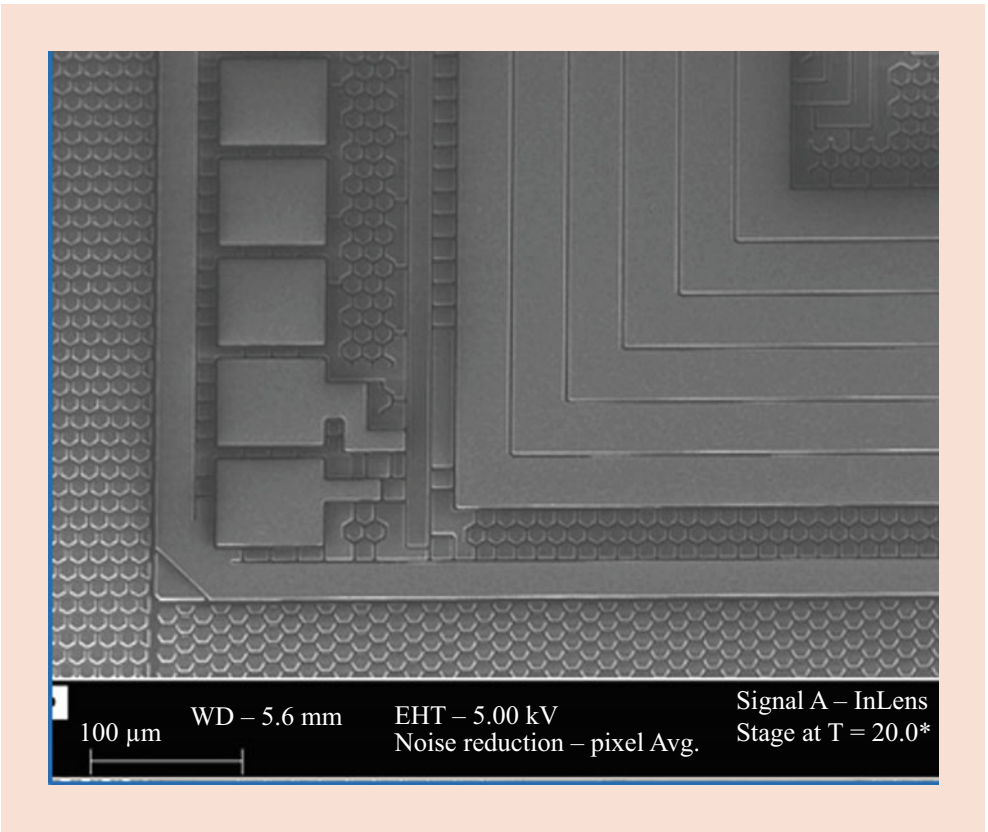

Fig. 18.53 Thick metal coil detail from a STMicroelectronics device. (© 2018 by STMicroelectronics)

materials that have electrical conductivities in between those of conductors and those of insulators. Doping, temperature, or illumination can modify the behavior and the electrical properties of silicon. For example, when silicon is exposed to light, several effects of interactions can occur, depending on the impinging photon energy. The energies of interest for everyday applications range from near infrared (NIR) to visible light and ultraviolet (UV), corresponding to a wavelength from 1100 nm to 200 nm. In order to calculate the energy of the radiation E_{ph}, the following formula can be used:

$$E_{\text{ph}} = h\nu = \frac{hc}{\lambda} \tag{18.33}$$

where ν is its frequency, λ its wavelength, h Planck constant, and c the speed of light.

The UV-NIR domain corresponds to energies between 1.12 eV and 6.2 eV. In this energy range, the dominant interaction mechanism is the creation of an electron-hole pair (EHP). When a photon is absorbed, its energy is transferred to the crystal, allowing electrons to jump to conduction band and move into the silicon lattice. An electron-hole pair is thus created. This mechanism can happen if the energy of the imping photon is higher than the energy gap. In this case, we have an internal extrinsic transition, which is the base of photo transduction in silicon, exploited by image sensors in the above domains.

EHP generation can occur in all semiconductors. Different materials can be chosen in order to detect also photons with lower energies (infrared) or photons with higher energies only. For infrared detection, germanium (Ge) and some III–V semiconductors (i.e., InGaAs) can be used, and dedicated doping can improve performances. Interest in this low-frequency range is due to several applications, such as material identification with optical spectrographs and lasers for LIDAR or 3-D scanning.

Every time an EHP is generated, the two charge carriers tend to recombine. The average time before the recombination of a hole in an n-doped region or an electron in a p-doped region is defined as minority carrier lifetime or recombination time τ. This recombination time is proportional to the diffusion length L, which is the distance minority carriers are able to travel before recombination:

$$\tau = \frac{L^2}{D} \tag{18.34}$$

where D is the carrier diffusivity.

EHP are also generated by thermal energy that may create band to band transition at temperature above the absolute zero (indirect silicon transition). This creates an undesired current, known as dark current, that must be taken into account as a critical design factor. Defects in the reticle (crystalline grid dislocation), chemical impurities, and dangling bonds at silicon interface promote spontaneous generation of EHP at low temperature and may increase dark current. These thermally generated carriers are the main responsible for noise in photodetectors and can be reduced by reducing defects.

Another important parameter for a photodetector is the spectral responsivity R, which is a sort of factor of merit or yield of the photodetector. It measures the output electric signal (voltage) with respect to the impinging radiation energy (in joule) per unit of area (square mm). The impinging radiation energy is computed considering the charge collection time or photocurrent integration time (T_{int}).

The spectral responsivity is directly related to quantum efficiency, defined as the number of electrons collected per incident photon per unit of area. This depends on the probability of an impinging photon to generate an EHP and on the probability of the electron to reach a determined sense node region without recombination.

The quantum efficiency (QE) as a function of wavelength is expressed by

$$\mathrm{QE}\,(\lambda) = \frac{J_{\text{ph}}}{q\Phi_{\text{ph}}\,(\lambda)}$$

where J_{ph} is the current density due to the generation of EHP resulting from the absorption of photons with energy E_{ph} greater than the semiconductor bandgap E_{g}, q is the elementary charge, and $\phi_{\text{ph}}(\lambda)$ is the impinging photon flux per unit of area.

18.11.2 CCD and CMOS

The first industrial proven photodetectors saw the light in 1970 as charge-coupled device (CCD) . The initial concept was to use an array of MOS (metal-oxide semiconductor) capacitors where charges, generated by light, shift from one cell to the contiguous one for the entire length of the array. In a modern CCD, an array of closely spaced MOS capacitors shifts data (in the form of packets of electrons) in a serial bit stream. The electrons finally reach a chip-level output amplifier where a charge to voltage conversion takes place.

At the beginning, independent readout paths for each pixel element were present; then this structure was replaced by one single readout path for each column of pixels, as this was advantageous to reduce the fixed pattern noise (FPN), afflicting the output signals. Good FPN was the stronger advantage versus the CMOS image sensors (CIS) structure for many years (Fig. 18.54).

Due to this shift-out mechanism in multiple stages, in a CCD there is a trade-off between transfer efficiency and frame rate.

CCD aim is image optimization; therefore it has only few integrated output amplifiers, with no other integrated circuitry, as the readout and the conversion stage are not in the same structure. On the other hand, CMOS continued to evolve toward smaller features (enabled by progresses in lithography) and integration of additional components, including readout circuits, that is not possible in the CCD structure. This feature and the strive for cost reduction were strong drivers toward wide spread of CMOS for imaging. In the late 1990s, CMOS technologies, optimized for image detection, started to be competitive in efficiency and cost when compared to CCD.

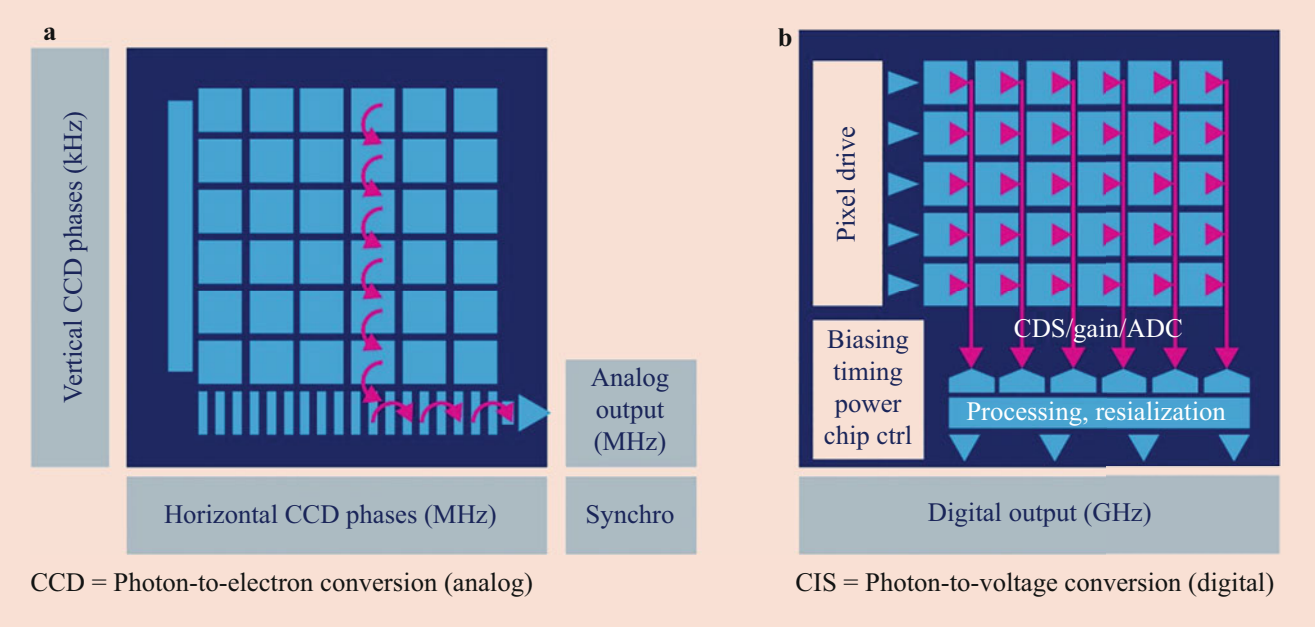

Fig. 18.54 Signal collection mechanism for CCD vs CMOS image sensors. (© 2018 by STMicroelectronics)

CMOS Structure: From Photodiode to Pixel Readout

The key element of a CMOS image sensor is the pinned photodiode (PPD). As depicted in Fig. 18.55, the PPD is formed by an n-well layer sandwiched between a P-type Si substrate and highly doped pinning P+ layer at the Si surface and connected to ground together with the P-type substrate. The concentration of the n-well layer is defined in such a way that it becomes fully depleted in reverse bias conditions. The P+ layer saturates (passivates) the dangling bonds at the silicon surface, drastically reducing the thermal EHP generation and the noise contribution from electron trapping and de-trapping mechanism. The PPD is associated to a polysilicon transfer gate (TG) which isolates it from a N+ output floating diffusion (FD). Generally, a small negative bias is applied to TG in order to suppress the dark current generated at the Si-SiO2 interface state under the gate itself.

In order to design a good PPD, signal-to-noise ratio (SNR) should be considered. SNR indicates the ratio in decibels between the signal level and the equivalent generated noise. If N_{sig} is the signal level in electrons and n_{sig} is the total noise at the given signal level, SNR can be calculated as

$$\mathrm{SNR} = 20\log\left(\frac{N_{sig}}{n_{sig}}\right)[\mathrm{dB}] \qquad (18.35)$$

At low signal levels, the readout noise is dominant, while at higher signal levels, the sensor noise, which is equal to the square root of the signal, becomes the dominant noise source.

SNR is related also to dynamic range (DR). Dynamic range is the capability of an image sensor to represent both high lights and dark shadows before to reach the full saturation. It is defined as the ratio between the maximum signal of a pixel and its dark noise level (typically expressed in decibels).

If V_{sat} is the saturation signal level in volts (which is related to the well capacity or the total charge each pixel can hold during integration time), V_{dark} is the dark noise or noise in volts at the output, N_{sat} is the signal charge at saturation in electrons, n_{dark} is the pixel noise floor in electrons (calculated by dividing the dark noise in volts by the image sensor's conversion gain without illumination and representing the smallest detectable input signal of the sensor), and then the DR can be expressed as

$$\mathrm{DR} = 20\log\left(\frac{V_{sat}}{V_{dark}}\right) = 20\log\left(\frac{N_{sat}}{n_{dark}}\right)[\mathrm{dB}] \qquad (18.36)$$

V_{sat} can be limited by the saturation of the readout electronics or by the full well capacity (FWC) of the detector, which represents the maximum amount of charge that can be collected by pixels.

A four transistors (4T)-based pixel, whose function is to transfer the charges generated into the space charge region (SCR) into the output stage, works in different steps. Once the TG and the reset transistors are both "on" (a U_{high} signal is applied to the gate of both reset transistor and TG), an electric field will be generated and will enable charges to move from the active region of the PPD to the FD. Those charges will cause a progressive voltage increase in the PPD region U_{PDD}, until the maximum voltage, related to the doping of the

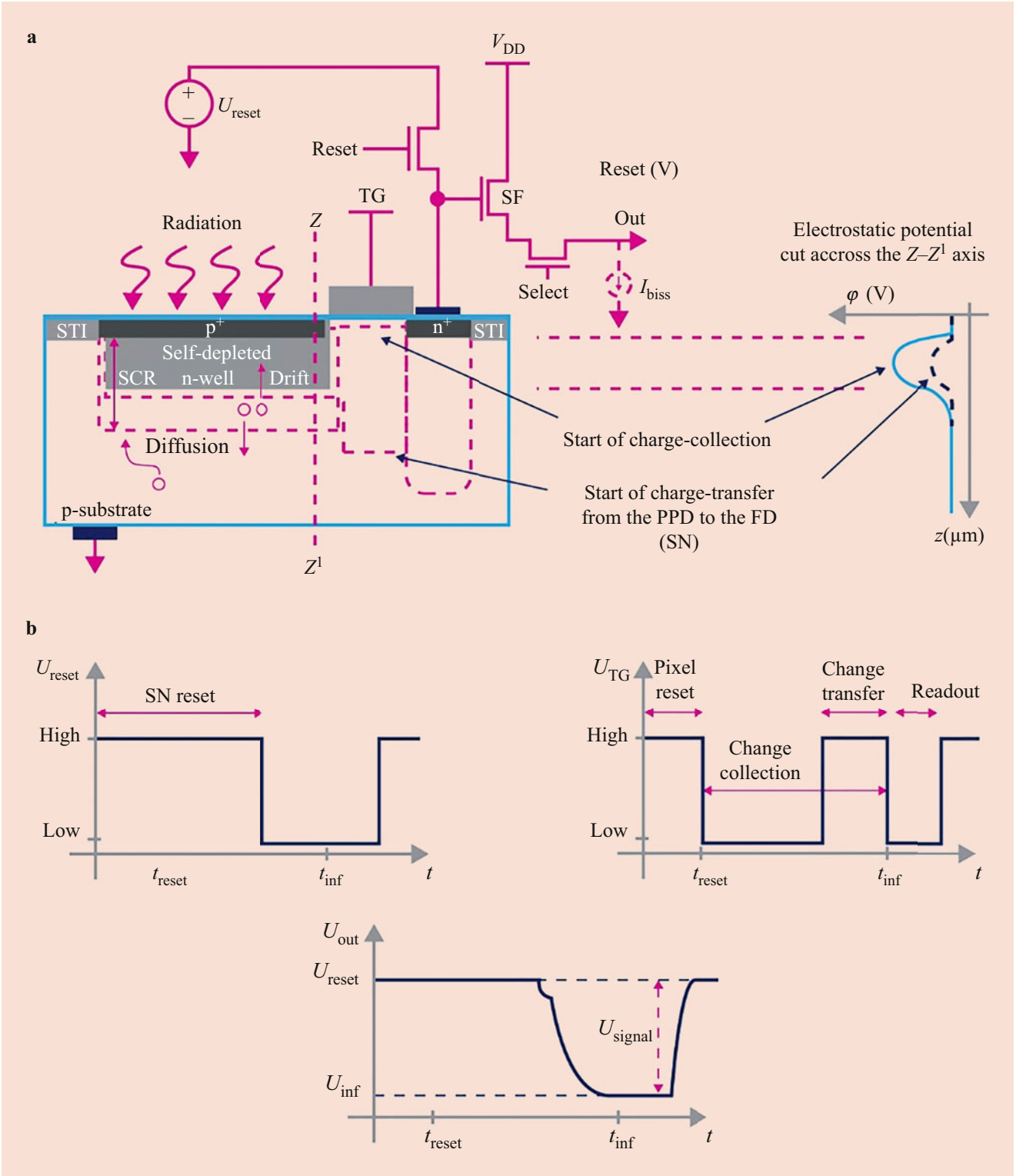

Fig. 18.55 Scheme of the charge transfer process. (© 2018 by STMicroelectronics)

different regions, is reached. When this maximum voltage or pinch-off voltage ($U_{\text{pinch-off}}$) is reached, the pixel is ready to register another event: pixel reset is concluded, and TG is set to "off" mode (U_{TG} is low).

To transfer the charges to the output, the FD remains in reset mode (U_{reset} is high), while the TG signal is low (TG is in "off"); thus the active region is electrically decoupled from the sense node (SN). In this case both thermally generated

and photo-generated electrons are physically in the active region, and its electrostatic potential starts decreasing below the $U_{\text{pinch-off}}$.

At a certain moment, defined by the sensor frame rate, the reset transistor is set to "off" mode and FD is left floating, while TG is on. At this point the output signal is collapsing to a minimum value before to be transferred to the output by putting in "off" mode also the TG, transferring all the charges to the output through the source-follower (SF; used as amplification stage), and saved at the input of the analog chain that will at the end process the signal. In general, a correlated double sampling operation (CDS) should be performed for noise optimization, and the signal must be stored at the input of CDS stage.

The capacitance of the SN can be tailored in order to increase the charge to voltage conversion factor, which at the end represents the pixel gain. FD also can be optimized and consequently designed as small as possible to minimize dark current and other leakage current contributions mainly linked to silicon substrates.

The reset K_{B}TC noise (where K_{B} is Boltzmann constant) originates from the statistical fluctuation of the potential across equivalent SN capacitance after reset. Its contribution depends on the mode of operation and on the pixel design and can be optimized with a trade-off.

The transistors of the readout chain also participate to the fluctuation of the output signal, with both low-frequency noise (1/f flicker noise) and white thermal related noise. During charge collection, in fact, the 1/f noise is primarily generated by the photodiode. It is due to surface recombination of carriers, and the fluctuation in bulk carrier mobility. For a reverse biased photodiode, the 1/f noise is not directly related to the total current. Instead, it is a function of the dark current, and it is typically much smaller than the dark current shot noise, and can thus be ignored. Different situation is happening in the readout circuit where the flicker noise is higher and increasing with the readout time.

FD design is also crucial for retention time, another important feature of the CMOS sensor. It should retain the signal information up to a desired time (several milliseconds) in order to collect the information to the readout: this retention time, reached with a proper design and equivalent capacitance dimensioning, is of essence for global shutter (GS) application, obtained with a (minimum) 4T architecture and by capturing the image simultaneously with all the available pixels. Today, most imaging devices have adopted GS mode to avoid distortion and artifacts; thus we can define GS efficiency as the difference between the original signal information and the signal change rate over time. CMOS image sensors using GS functionality are used in a variety of areas, including broadcasting, automotive, drone, and surveillance applications, as they can provide a perfect image of a moving object.

If pixel is not adopting a GS, then the image is sequentially scanned (from one side of the sensor, usually the top, to the other side, on a line by line basis), and we speak about a rolling shutter (RS)-based image sensor. In RS the pixels are registering a sequence of images rather than a complete synchronous image per pixel as in a GS. This time difference in RS results in specific error, especially for moving images.

Unfortunately, also GS system is suffering a specific error. When we acquire a frame and then suddenly close the shutter of the camera, the following frames should ideally be completely dark. In reality, this is not happening and we have what is defined the image lag error: after closing the shutter, we may observe a sort of ghost image, which slowly fades away as the successive frames are acquired.

SPAD and SiPM

If we consider the evolution of the sensor and the use of photodiodes, many applications arise including both image capturing and environment scanning to provide a tridimensional scansion. The possibility to have a photodiode able to detect single photon (SPAD: single-photon avalanche diode) is opening new possibility especially for 3-D scanning and particularly for time of flight solutions.

Both PPD and SPAD are reverse biased p-n junctions, but SPAD is operating in the so-called Geiger mode, in which the diode is biased slightly above the breakdown threshold voltage, where a single electron-hole pair, generated by absorption of a photon, can trigger a self-sustaining strong avalanche. The current rises swiftly to a macroscopic steady level in the milliampere range. If the primary carrier is photo-generated, the leading edge of the avalanche pulse marks the arrival time of the detected photon. The current continues until the avalanche is quenched by lowering the bias voltage below the breakdown threshold voltage; the lower electric field is no longer able to accelerate carriers to impact-ionize with lattice atoms; therefore current ceases. In order to be able to detect another photon, the bias voltage must be raised again above breakdown. This operation requires a suitable circuit (usually referred to as a quenching circuit), which has to:

1. Sense the leading edge of the avalanche current.
2. Generate a standard output pulse synchronous with the avalanche buildup.
3. Quench the avalanche by lowering the bias down to the breakdown voltage.
4. Restore the photodiode to the operative level.

The simplest quenching circuit is commonly called passive quenching circuit and comprises a single resistor in series with the SPAD. The avalanche current self-quenches simply because it develops a voltage drop across a high-value ballast load R_{L} (about 100 kΩ or more). After the quenching

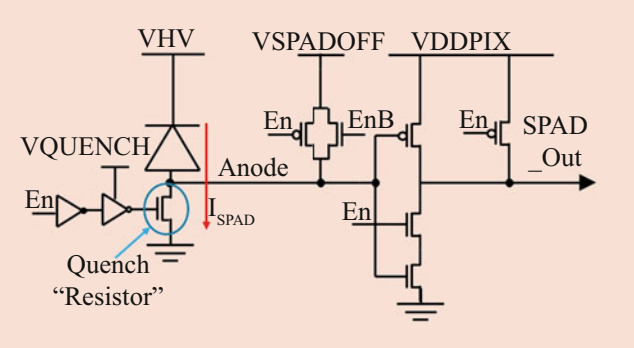

Fig. 18.56 SPAD circuitry with active recharging system. (© 2018 by STMicroelectronics)

of the avalanche current, the SPAD bias slowly recovers to above breakdown voltage, and therefore the detector is ready to be ignited again. A more advanced quenching is a scheme called active quenching. In this case, a fast discriminator senses the steep onset of the avalanche current across a 50 Ω resistor (or integrated transistor) and provides a digital output pulse, synchronous with the photon arrival time. The circuit then quickly reduces the bias voltage to below breakdown (active quenching) and then relatively quickly returns bias to above the breakdown voltage ready to sense the next photon (Fig. 18.56).

SPAD Structure

Not all photodiodes are able to work as SPAD. The structure must be designed in such a way to avoid concentration of the electric field, particularly at the edges; a circular guard ring, visible in red on the left of Fig. 18.57, must be designed to separate SPAD active region from the surrounding area. Particular manufacturing technology steps must be implemented to obtain very good quality of the silicon in terms of crystallographic defectiveness and to minimize the concentration of generation centers and traps levels, in order to reduce the rate of thermal generation of carriers.

SiPM

A silicon photomultiplier (SiPM) is an array of SPAD connected in parallel, where each pixel represents a group of connected SPAD. For specific applications, SiPM is not integrating the entire processing element, typically integrated on the CMOS, but just the photodetector.

Listed in the following are the common reading errors associated with the SPAD:

- Time jitter: The total uncertainty of a SPAD coupled to a time measurement device. It represents the incertitude in the time of the measurement linked to the fact the V_{op} is reached in a time that is not deterministically computed but based on a Gaussian. Since V_{op} is reached in a certain time distribution probability, a time error is included in the measurement.
- Dead time: After an avalanche a SPAD is unable to detect a further photon up to when free carriers will be eliminated and recharge, and quenching will reset back the SPAD to V_{op}. The time necessary to put back the SPAD in operation after a measure is representing the dead time. Dead time cannot be considered in reality an error.
- Electrical cross talk: A large number of connected SPAD with a shared V_{op} line fire at the same time, so any drop or increase in the voltage may cause a decrease of the V_{op} or a registration of an event, with a correspondent reading error.
- Optical cross talk: Can originate from photons emitted during the avalanche or coming from other sources (i.e., a VCSEL used for active illumination or a non-perfectly isolated circuitry from the external environment). Normally this is happening with highly and densely packed SPAD arrays.

18.11.3 CMOS Image Sensor: A Complete Solution

The key components in a CMOS image sensor (CIS) are:

- Photodiode (PD) and pixel readout.
- Circuit for analog to digital transduction.
- Micro lens and optic module.

A light sensor element (pixel) includes a light-sensitive element and a readout circuit. The sensitive element is usually a pinned photodiode, but also a SPAD can be used. Floating diffusion, source-follower, and other transistors form the pixel readout. Signal conditioning is composing the rest of the CIS as reported in the block diagram here below (Fig. 18.58):

The most widely implemented pixel design is known as an active pixel sensor (APS). Three to six transistors are commonly used and they provide gain or buffer the pixel from large column capacitance.

A color filter is used to separate out the red, green, and blue (RGB) components of reflected light. Finally, the micro lens gathers light from the inactive portion of the CIS and focuses it down to the photodiode (Fig. 18.59).

A pixel can be defined as a sensor converting photons into voltage, while the signal processing circuit function, embedded in the image sensor, is similar to that of other sensors. This signal processing stage must guarantee high speed, low consumption, and reduced noise. All of these requirements are strongly linked to the circuit design of CMOS image sensor, particularly to analog signal processing and analog to digital converter (ADC) embedded in the CMOS.

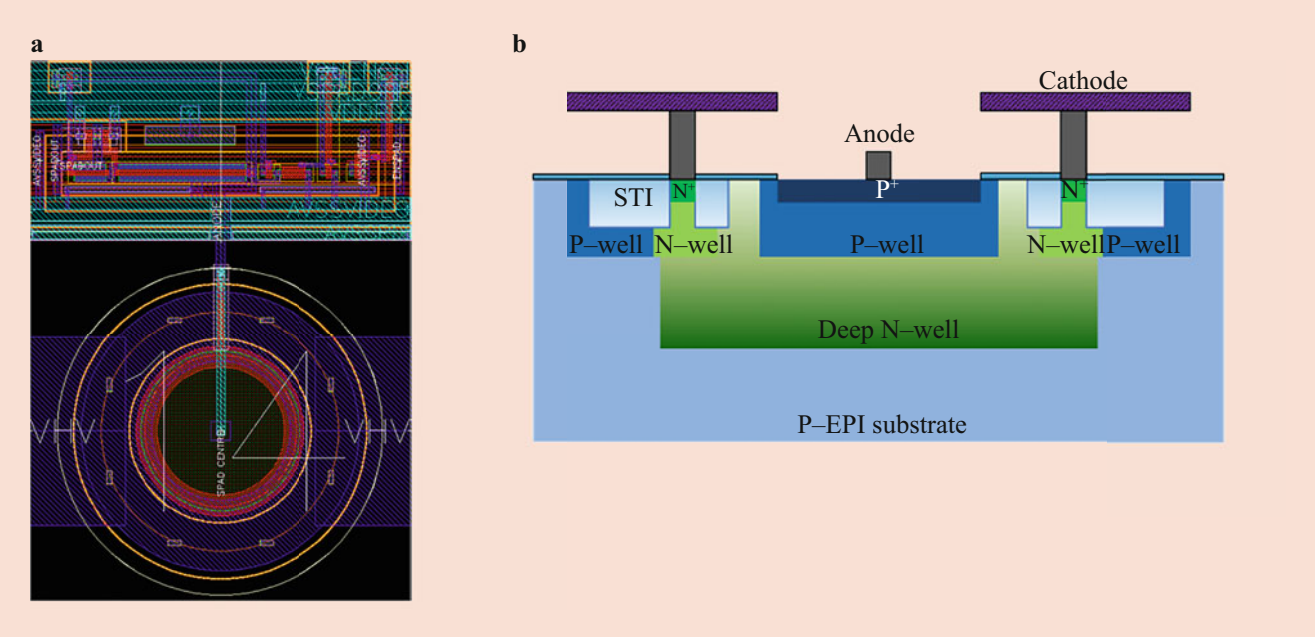

Fig. 18.57 (**a**) Real SPAD structure with guard ring visible in red. (**b**) SPAD schematic cross section. (© 2018 by STMicroelectronics)

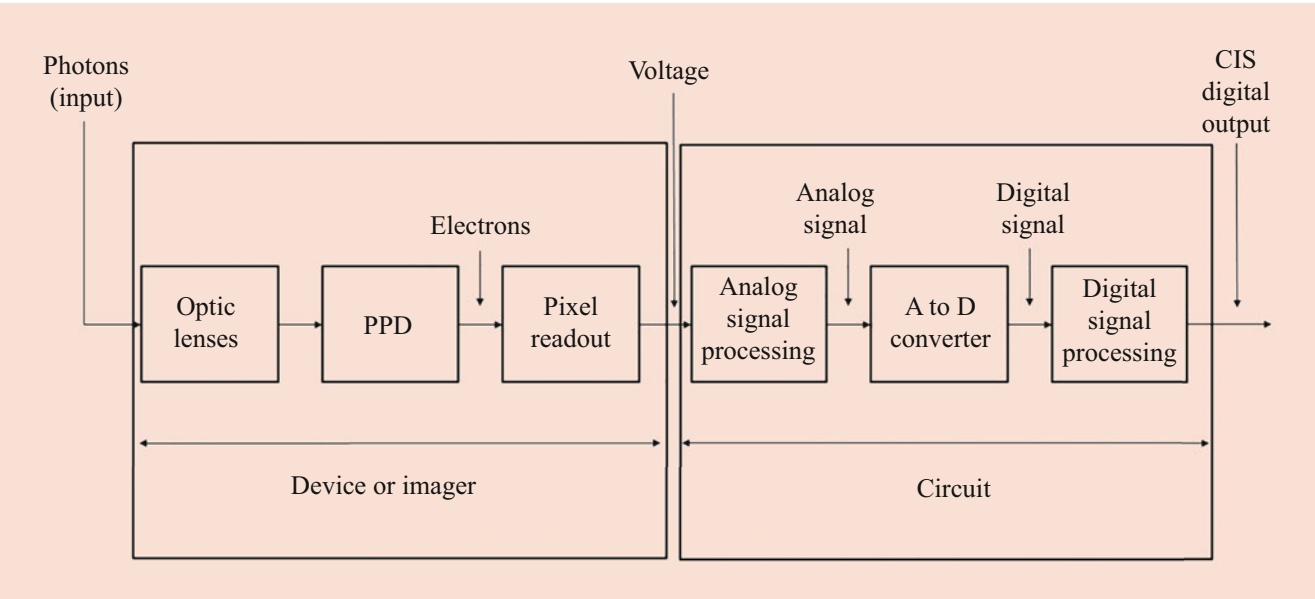

Fig. 18.58 CMOS image sensor block diagram. (© 2018 by STMicroelectronics)

In order to achieve good SNR, different sampling methods and amplifier designs are adopted, according to different specifications and design architectures. Normally, this processing chain is implemented as column circuitry. In CMOS image sensors, correlated double sampling (CDS) is widely used to reduce reset noise and offset. Different sampling technologies have been proposed for noise reduction.

Analog to digital conversion of the pixel output affects image quality, frame rate, power consumption, and form factor. According to their location, ADCs can be sorted into three categories:

- Chip-level ADC: Connected at the output of the analog signal of the sensor. This methodology is not allowing high-speed processing, as all pixel outputs are time-multiplexed to the input of the global ADC.
- Column-level ADC: Ideal for high speed and high resolution, as the input of the column-level ADC is connected

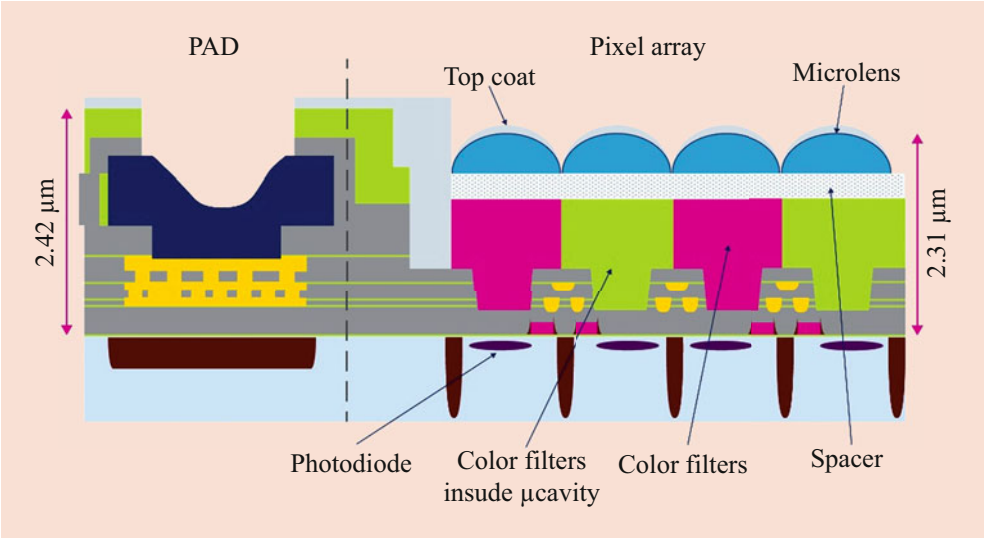

Fig. 18.59 Schematic cross section of a CMOS image sensor, including micro lenses and color filters. (© 2018 by STMicroelectronics)

to one group of the column circuit outputs. By increasing the number of ADCs working in parallel, frame readout time is reduced. The main challenge of this design is due to the insertion of the ADC in the layout: its width should be smaller than corresponding pixel pitch. Therefore, this solution is in contrast with pixel shrinkage trend.

- Pixel-level ADC: When ADC is included at pixel level, SNR can be increased, since conversion occurs at single pixel and only digital data are transmitted. Additional advantages include low power and high speed. Since every pixel includes an ADC, the fill factor of the pixel decreases.

CMOS and Sensor Integration

In conclusion, CMOS presents some advantages if compared with CCD:

- Higher integration: As already mentioned, the CMOS image sensor can integrate readout circuit, ADC, and even the digital signal processing module in one chip.
- Lower cost: CMOS technology is taking advantage of lithography roadmap, whereas CCD cannot. System integration in one chip can further decrease area, with manufacturing cost reduction. Moreover, CMOS diffusion in different markets and multiple applications is a driver for photolithography reduction and miniaturization, with strong scale economy.
- Power consumption: Since CCD requires multiple power supplies per column, a CMOS image sensor can achieve lower power consumption.
- Speed: CMOS image sensor can achieve a more flexible readout integrated mechanism, which results in a higher speed for reading the light than CCD, also with the advantage to integrate memory directly in the pixel. CMOS is the favorite choice when high speed is necessary: this is the case, for example, of 3-D cameras for industrial, consumer, and automotive application.

The real limit of the CMOS image sensor is actually the higher level of integration, limiting the access of photon to the active area of the pixel. To minimize this problem, primarily optimization of metal layers was implemented, and then few other options were experimented, in particular BSI and hybrid or 3-D stack options.

Pixel Manufacturing, FSI, BSI, and 3-D Stack

In the classic structure known as frontside illuminated (FSI) structure , metal contacts on the top surface of CMOS devices limit the amount of photons impinging the pixel. Moreover, light travelling from lenses to photodiode must cross passivation and dielectric layers, and this causes losses, due to reflections, and cross talks, due to light scattered from adjacent pixels. All these effects decrease QE and SNR.

Some optimizations have been implemented in order to increase the efficiency of the sensor. Some of those changes conceived to improve the CMOS performance include:

- Increasing and optimizing lens surface to increase the amount of photons impinging the active area.
- Reducing the distance from the lens to the PD in order to reduce the optical path and increase the amount of photons per area of the PD, avoiding also inter-pixel cross talk.

Micro lenses optimization in form factor and efficiency is key. Micro lenses array fabrication includes two methodologies:

- Direct: The lens is formed using the principle of surface tension effect, when the material used is in a thermoplastic transition or in liquid state (typically induced by heating in controlled atmosphere). Normally this process is very efficient in cost and performance, but, when complex shapes are needed, is not effective. Thermal reflow, microplastic embossing, or microdroplet jetting are all direct techniques.
- Indirect: Lens is fabricated via injection molding or hot embossing using a preformed concave shape. This methodology is more expensive and is chosen for complex geometries.

The basic process is obtained starting from a classical photolithography step followed by a thermal treatment in controlled atmosphere. The melting is obtained with a consequent controlled shape of the formed lens (Fig. 18.60).

A certain amount of QE may be lost for cross talk due to the fact a photon is hitting the active area of another adjacent pixel (cross talk). Therefore, optical isolation between all the PD must be designed. Cross talk can be split into [60]:

- Spectral cross talk: related to color filters properties.
- Optical cross talk: happening when an EHP is generated in the active area from an impinging photon collected by an adjacent pixel.
- Electrical cross talk: electrical charges (electrons or holes depending on the pixel type) that may diffuse among adjacent pixels.

The evolution of the different image sensors to obtain this optical isolation moved from the initial simple shallow trench isolation (STI), characterized by a higher cross talk, to a barrier created with a dedicated p+ deep implant, to vertical deep diode up to deep trench isolation (DTI). DTI guarantees a higher level of immunity and is widely used in CIS (Fig. 18.61).

Deep trench isolation is normally obtained by etching a trench to isolate two adjacent pixels and filling it by oxide in order to create a SiO_2-Si interface, after the formation of the shallow trench isolation (STI). Then around the trench a sidewall implantation (SWI) is made. Thermal treatments and annealing process are necessary to clean up the interface around the trench and minimize dark current.

Sidewall implantation is an improvement able to guarantee a higher immunity to dark current. By this flow, 1:25 aspect-ratio trench can be achieved and it is also used as passivation methodology. Thanks to both DTI and SWI, average dark current is reduced by an order of magnitude, with a net improvement for QE.

A further improvement is capacitive deep trench isolation (CDTI) in which the trench is filled with SiO_2 and polysilicon, allowing a very effective solution for active suppression of cross talk due to diffusion or photo-generated carriers. We can consider CDTI as an active sidewall passivation as, to operate, must be activated. Activation is made by biasing the structure with a negative voltage in order to obtain an equivalent SWI along the whole vertical length of the trench. When negatively biased (around -1 V), CDTI is actively creating hole barriers along the whole trench in a well-controlled and thin region, with a minimal impact on the FWC and PD active area.

In conclusion, CDTI can improve dark current, full well capacity, and indirectly QE, as the active area of PD is optimized. Both SNR and dynamic range increase.

CMOS photolithography node has been progressively shrunk, requiring a drastic improvement related to metal options and their connections. Copper metal process has been introduced to reduce the form factor and increase where possible power density. Copper introduction allowed a further acceleration to photolithography reduction, but the use of copper requires some specific intermediate dielectric layers, whose effect to some specific wavelength is equivalent to the one of an optical filter. This intrinsic problem related to copper metallization is one of the most important issues limiting the CMOS node shrinkage on image sensor, whose race to miniaturization is slowing down compared with standard CMOS.

Despite all the improvements in pixel isolation, pixel reduction is also limited because in FSI the optical path may be extremely reduced. Some possible solutions include reducing metallization layers and creating preferred optical paths to increase the number of impinging photons per area in the PD. For the latter technique, one of the most adopted solutions is the so-called light pipes: they are channels obtained by deep vias filled with material at high reflective index, leading the light from the micro lenses directly upon the PD.

These techniques are often very complex due to small pixel dimension: to overcome this problem, a backside illuminated (BSI) structure has been conceived. In this structure, photodiode is directly exposed under the chip lenses (Fig. 18.62).

BSI optimized structure can be obtained through a complex process flow, implementing some specific manufacturing techniques. Standard diffusion allows realizing PD and interconnections. Then some dedicated process steps are performed:

- Wafer-to-wafer bonding: Surface is cleaned by chemical-mechanical polish (CMP) and micro-roughness is critical for bonding quality. After CMP, surfaces are plasma-activated and direct bonding is performed.
- Wafer thinning: Made on the flipped wafer. Good surface finishing and thickness control are key in this process.
- Passivation of the PD: One method is to implant the wf backside with a shallow P+ implant. The implant

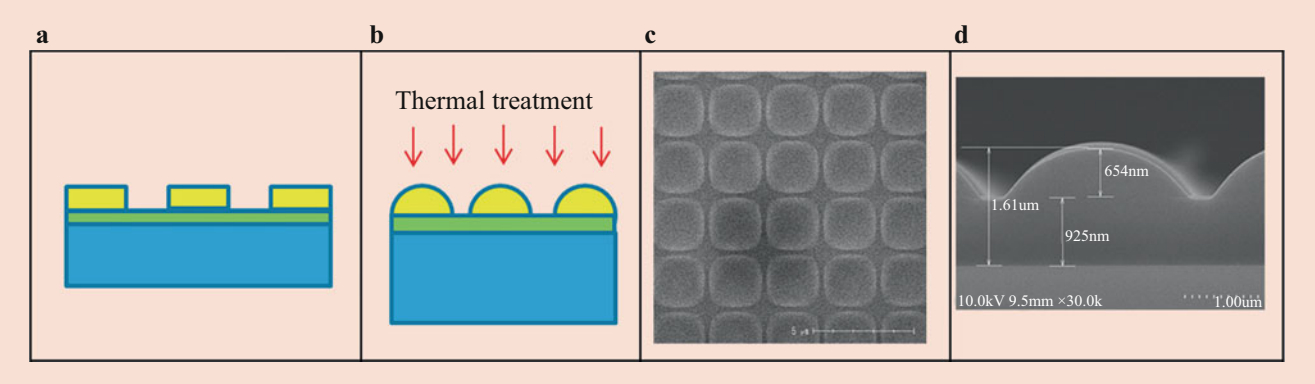

Fig. 18.60 Basic manufacturing steps of a thermal reflow methodology for CMOS micro lenses and top and cross-section images of the formed lenses. **(a)** Classical photolithography process. **(b)** Melting process for final μLens shape. **(c)** Top view post thermal treatment (melt). **(d)** X section post melting process step. (© 2018 by STMicroelectronics)

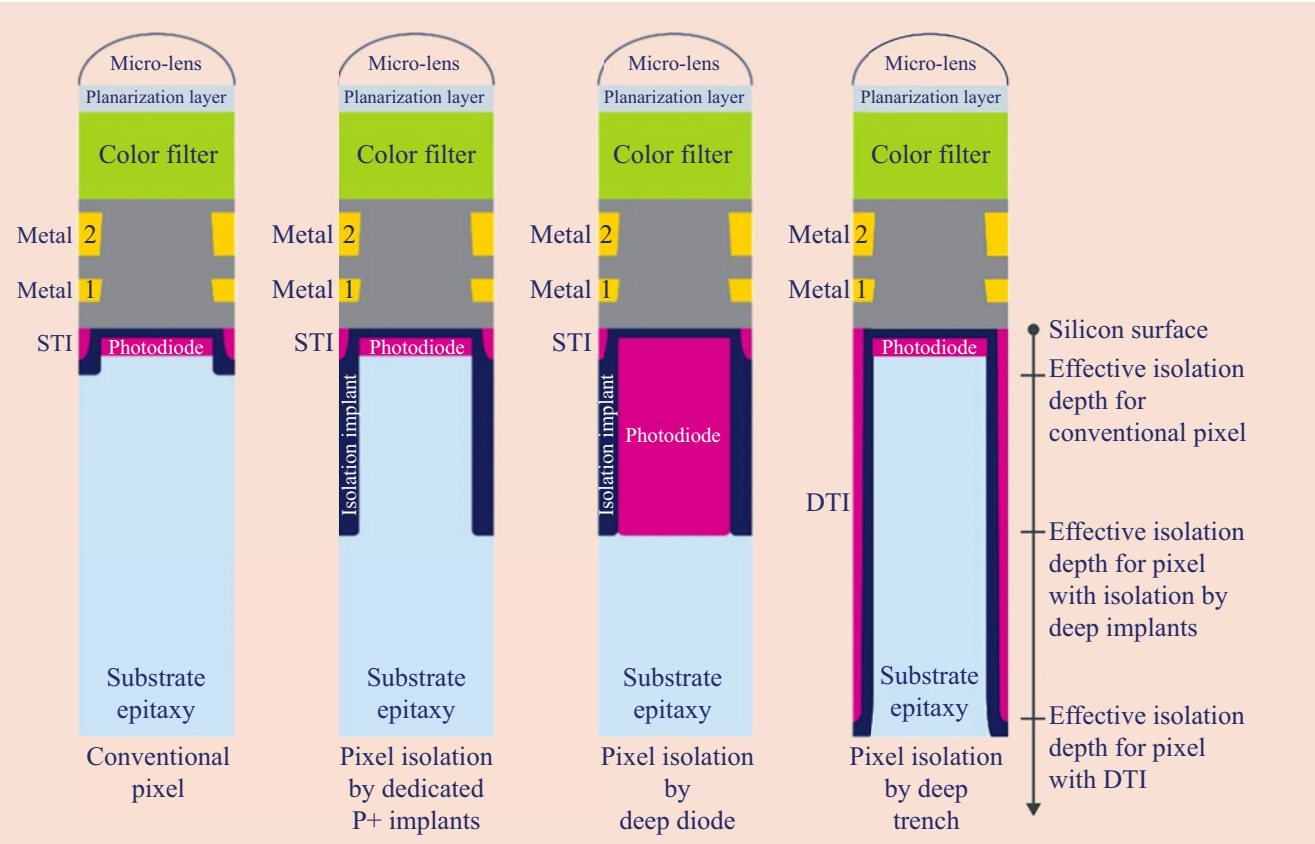

Fig. 18.61 Evolution of the techniques for pixel isolation. (© 2018 by STMicroelectronics)

is annealed and activated by a powerful laser beam pulse, capable to provide high energy for 100–200 ns. In this way, a localized thermal treatment is applied, and the temperature in the metallization area of the wafer does not change. Despite this methodology being now consolidated for CMOS, the equipment to perform laser annealing are expensive and not standard for regular CMOS foundries. Another option is the deposition of high K passivation (Ta_2O_5 on HfO_2 or Al_2O_3) materials. These materials are optimized as antireflective coating (ARC) in order to increase quantum efficiency (Fig. 18.63).

Adopting a BSI flow, the photodiode is directly below the lens and the filters, with the metallization located in the back of the flipped wafer.

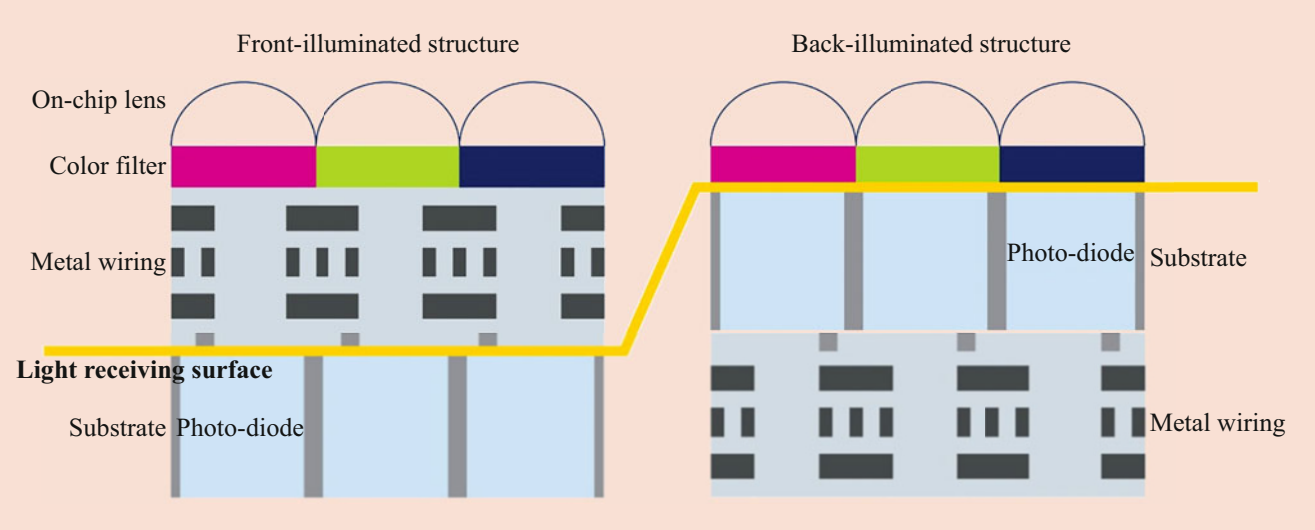

Fig. 18.62 Schematic cross section of a FSI and BSI CMOS image sensor pixel. (© 2018 by STMicroelectronics)

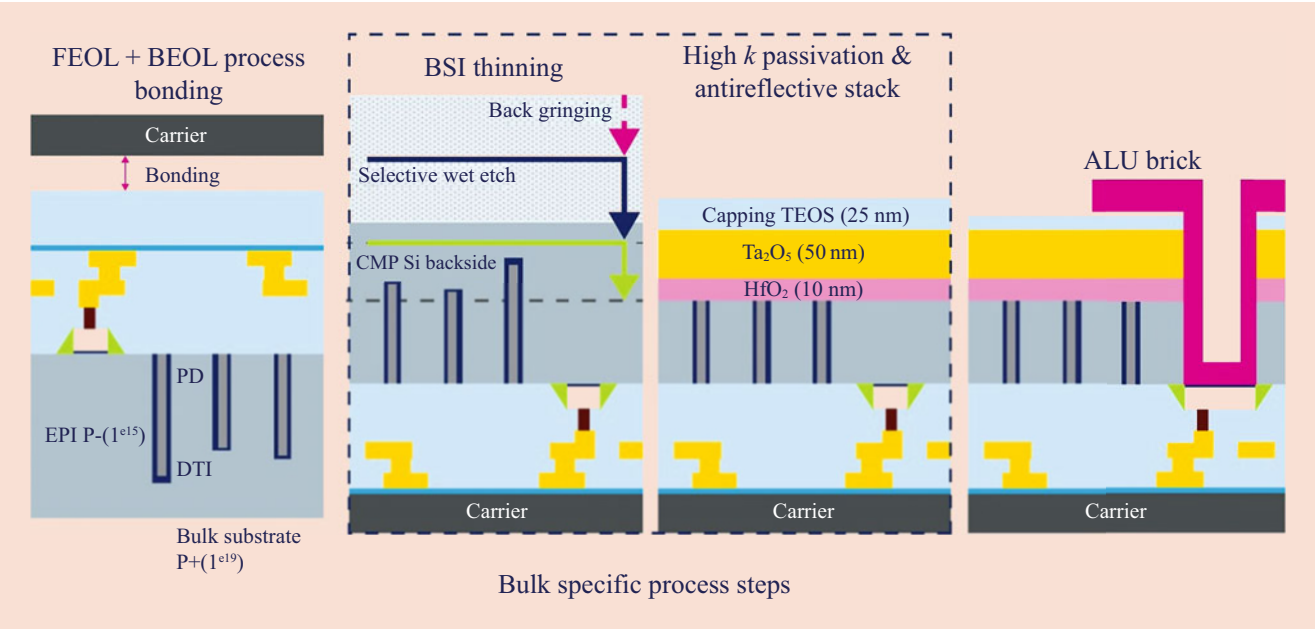

Fig. 18.63 Illustration of BSI schematic process flow with high *k* passivation. (© 2018 by STMicroelectronics)

The advantages of BSI are several: quantum efficiency increases (more photons reach the active area), and a higher fill factor can be obtained; metal backscattering is suppressed and losses are reduced; chief ray angle is improved.

3-D Integration

CMOS evolution takes advantage from lithographic node reduction, while in CMOS for imagers, this evolution is limited by the search for QE, and, despite the new BSI option, there are still manufacturing limitations.

3-D integration is the technique to stack wafers, whose technology may be also completely different, in multiple layers (heterogeneous integration), to form a single device monolithically packaged (Fig. 18.64).

In the past, this integration was obtained with techniques showing several limitations. Wire bonding interconnections have limited maximum current density, electromagnetic interference issues in case of high frequency in operation, and reliability issues. Flip chip is an expensive process and only two dice can be assembled.

Nowadays, more sophisticated manufacturing options are available and 3-D integration can even reach a pixel-level scale. A pixel can be made of a BSI imager stacked on a CMOS die containing the analog and digital circuitry

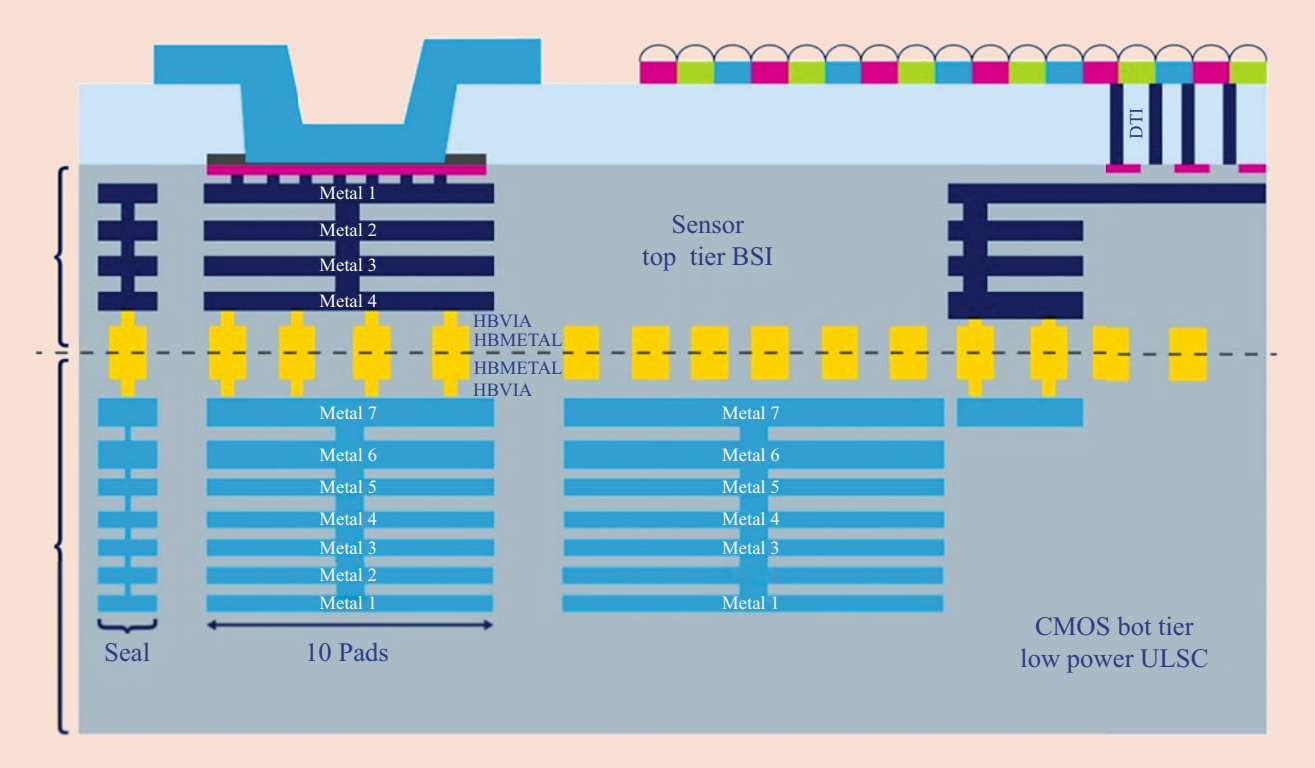

Fig. 18.64 Example of heterogeneous integration of multiple layers in a single device. (© 2018 by STMicroelectronics)

(sometimes including also a memory). The alignment of the wafers is crucial to avoid a drastic reduction of QE and optimize the SNR (Fig. 18.65).

In 3-D stacked BSI, wafer-to-wafer alignment is done with specific equipment allowing a precision in the range of about 0.2 μm. Wafer-to-wafer bonding includes two phases. In the first step, after surface preparation by plasma activation, direct bonding of the silicon oxide on the surface of the two wafers is performed. This process is also known as molecular bonding. Then an annealing induces copper thermal dilatation and coalescence between copper metals of the two wafers. This methodology can guarantee a scalable process for pixel pitch up to 1 μm (Figs. 18.66 and 18.67).

3-D Sensing

3-D sensing is a depth sensing technology that augments camera capabilities for facial and object recognition in augmented reality, gaming, autonomous driving, and a wide range of application. 3-D sensing can be achieved using a number of different technologies among which are stereo light, structured light, and time of flight.

Stereo Light

Stereo light is split into two clusters: active and passive stereo vision. The main advantage, using this technology, is the possibility to obtain 3-D images with a very high resolution and to use the multiple cameras already present, for example, in the top models of mobile phones to obtain a complete 3-D vision with a good depth resolution. In most cases, it is used for professional applications, as this modality requires a high computation from the main video processor and increased depth resolution is strictly dependent on the base line increase as per the following formula:

$$\Delta z \propto \frac{z^2}{b \cdot f} \tag{18.37}$$

where Δz is depth error, z is depth of point of interest, b is the baseline, and f is the focal length.

To avoid the several mistakes associated with parallax error, a tight calibration is required; for this reason, there could be systems where active light option is used, bundled with a time of flight system. Most probably, the 5G and higher performances in the processor, together with some specific entertainment applications (3-D high-resolution scanning, interactive movies), may boost this system. For nomadic systems the calibration costs, power consumption, and baseline form factor will remain in any case a limitation versus other options. On top, depending on the environment, the system can make systemic mistakes if in presence of plane structures with the same color scale (i.e., a white desk with a white wall in the back). In this case, an active stereo solution may be required or, in order to avoid too complex solutions, a ToF can be used.

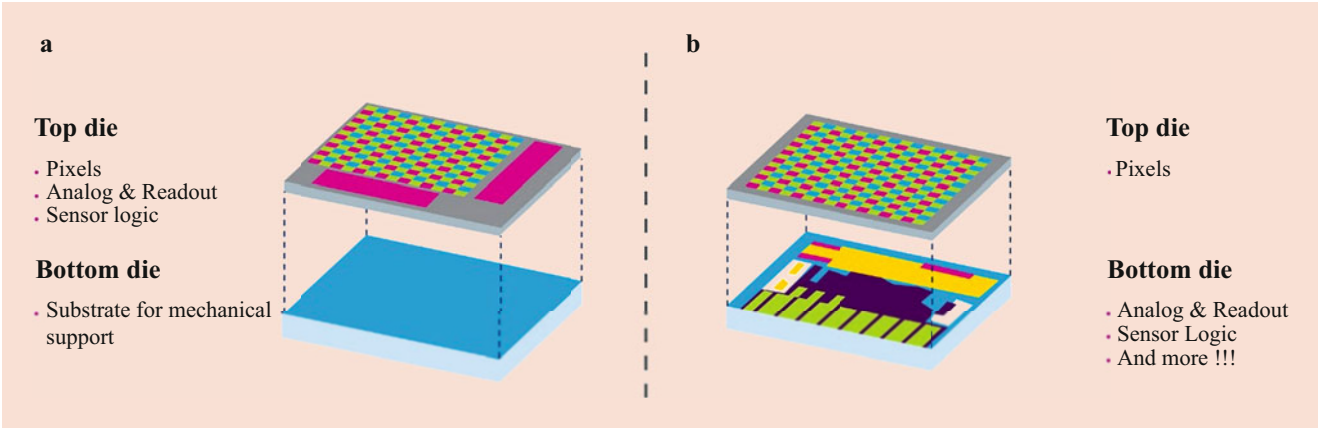

Fig. 18.65 Comparison between (**a**) traditional and (**b**) 3-D stacked BSI. (© 2018 by STMicroelectronics)

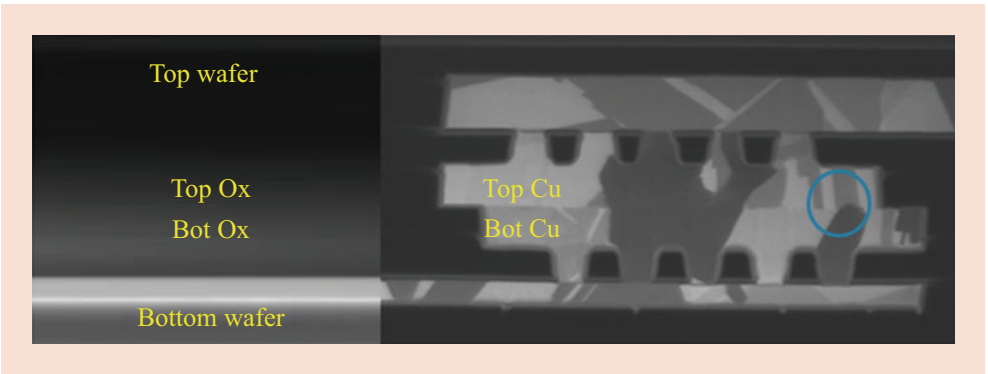

Fig. 18.66 Cross section of an interface after molecular bonding. Both SiO_2 and copper regions are visible. (© 2018 by STMicroelectronics)

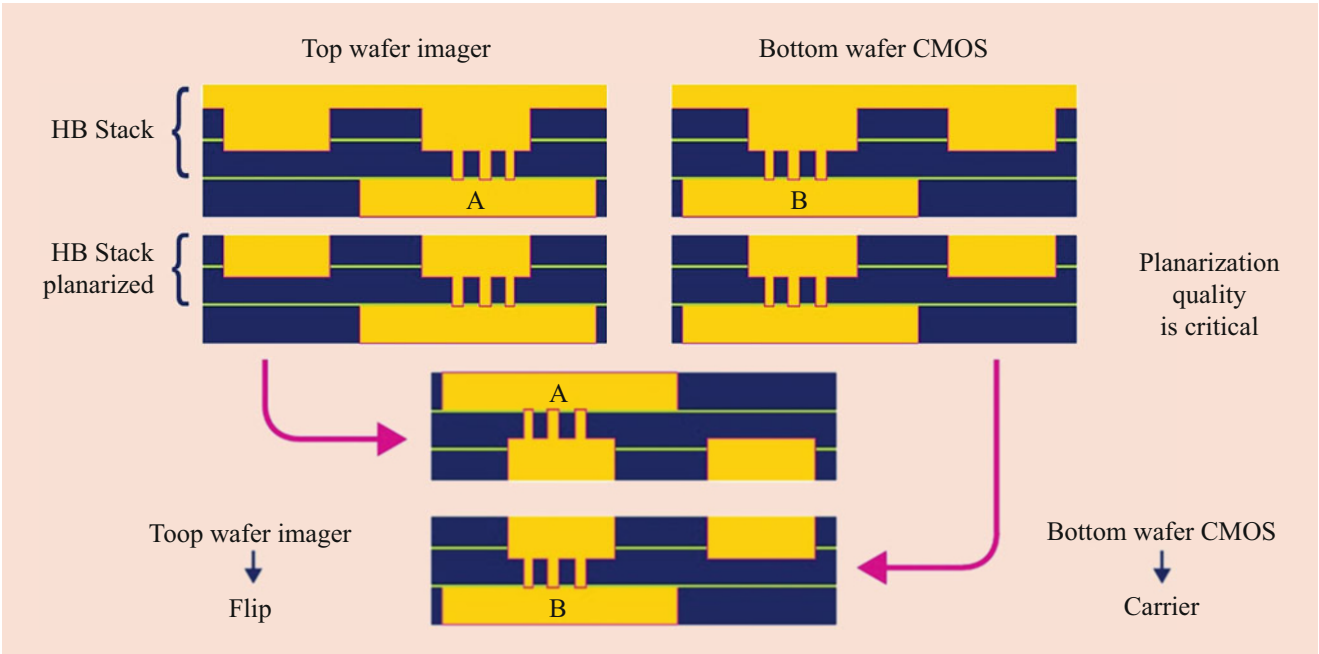

Fig. 18.67 Process flow for 3-D stack integration. (© 2018 by STMicroelectronics)

Structured Light

This is also a geometric system, but, different from stereo light, in general a low-resolution camera is adopted. The measurement is made projecting a finite number of dots (dot matrix or pattern) using the active illumination system (in general a VCSEL with a diffractive lens), creating a pattern in the area/geometry to be measured. The measure is the deviation between the expected position of the dot and the real observed position.

In this case, the baseline is the distance in between the light source and the sensing element, so the same formula for stereo light reported before is still valid. Consequently, the baseline is of essence to increase the distance of the measurement.

One of the most intuitive uses of the structured light is face recognition: the higher the number of dots, the better the image depth precision is. This method implies a lighter processing with respect to the stereographic view and allows higher precision at shorter distance, making the system ideal for face recognition in the front camera of the mobile phones and in security applications.

In addition, this technique requires a rigid calibration with very low tolerances, high precision, and stability in order to guarantee measurement precision in the whole range of operative conditions. Calibration can be simplified by using integrated modules with both sensor and light emitter integrated. This solution is widely adopted in consumer and mobile applications, even if there are limitations due to baseline dimension.

In general, a low-resolution camera QVGA is used bundled with near-infrared (NIR) VCSEL. NIR is ideal to have a detection with different light environment; a flood illuminator may be required to mitigate the external light when very intense. With respect to ToF, in this case, scanning speed and accuracy are higher at lower distance, but processing is more intense than ToF, and calibration is much more complex. Since the light is rigidly controlled, interference with other similar projectors illuminating the same image is less frequent than with time of flight system, assuring a better immunity.

Time of Flight

Time of flight solutions are based on sensor elements that can measure a distance by analyzing the reflected light emitted by a punctual light source (a LED or a VCSEL in general). The illuminator is projecting a controlled light on an object that reflects it. A receiver (SPAD) captures reflected light. Analyzing the reflected light and the time occurred from the emission to the reception of the light, the system is capable to measure the distance. Each pixel encodes the distance to the corresponding point in the scene (Fig. 18.68).

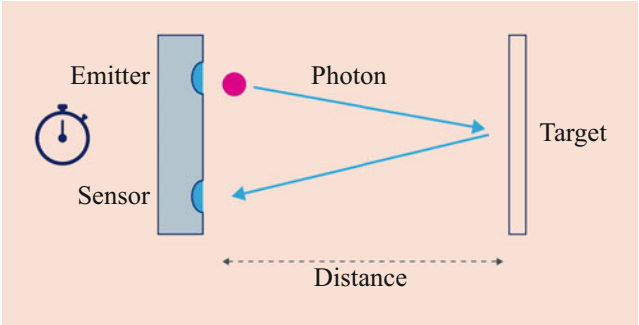

Fig. 18.68 Time of flight principle. (© 2018 by STMicroelectronics)

The methodology is not triangulating any distance as in the previous examples; thus the calculation of the video processor and the calibration are simplified.

The unique sensing architecture of the ToF camera means that a raw depth image contains both systematic and non-systematic bias that have to be resolved for robust depth imaging. The most frequent problems are related to low depth precision and low spatial resolution, as well as errors caused by radiometric, geometric, and illumination variations of the environment, including also interferences due to the contemporary presence of several ToF. We can consider time of flight a valid and reliable solution with fast scanning, low consumption post-processing, and easy calibration, even if less accurate than other methods and generating some specific errors. Other advantages are relaxed mechanical tolerances and rigidity requirements (not relying on geometrical assumptions), simpler calibration, stability during lifetime, and less power-consuming self-calibration.

Main disadvantage is that ToF cameras today typically have a relatively low resolution (maximum 1MP and often much lower). Therefore, to create a 3-D high-resolution image, a composition and post-processing software solution must be used, increasing the computational power again. Ultimately for short distance range (about 1 m), structured light gives higher accuracy at higher speed and, for this reason, is used in the frontal camera of some mobile phone top brands.

Direct Time of Flight and Indirect Time of Flight

Time of flight can be split into two groups, depending on the way the system is measuring the distance: direct and the indirect time of flight (respectively, dToF and iToF).

In dToF, the system measures the time t_d of the echo returning from an object and derives distance z as

$$z = \frac{c \cdot t}{2} \tag{18.38}$$

where c is the speed of light.

In the iToF that requires modulation, the phase shift between outgoing and incoming radiation is measured, and the distance is computed according to the following formula:

$$z = \frac{c \cdot \varphi}{2 \cdot 2\pi f} \tag{18.39}$$

where f is the frequency of the modulated signal (in general a square or sine wave modulation is adopted).

A maximum operating range exists, due to the possibility of ambiguous signals. If the light travels back and forth during a period longer than the period of the modulated light, then the distance calculation will be wrong, as the sensor is not capable to make a difference between a signal coming back from a far distance and another signal coming back from a closer distance with the same phase shift (Fig. 18.69).

In particular, if λ_m is the wavelength of the modulated signal, this critical distance is the following:

$$d = \frac{\lambda_m}{2} = \frac{c}{2f} \tag{18.40}$$

The unambiguous range is the one-way distance and equals half of the maximum distance the light can reach during a period. For example, at 15 MHz it will be 10 m.

Evolution of sensors and high capability of integration in particular on CMOS technology made ToF easy to miniaturize, adopting ultrafast photodiodes, a global shutter, and an analog storage capable of 100 frames per second. The global shutter with the storage system must collect the image got from the sensor, while the sensor must be synchronized with a fast light source emitter.

Optical Parameters and Field of View

In ToF, light is generally coming from a source (LED or VCSEL) operating in the near-infrared range. The sensor is sensitive to the ambient light over-imposed. A high ambient light value will lower the signal-to-noise ratio (SNR). Typical signal shows a plateau, due to environment and dark current, and a peak, corresponding to the signal. Thus, the noise is distributed in time and can be consequently filtered.

Several noise sources can be identified in the complete optical module, related to signal transmission and reception (Fig. 18.70).

In order to gather light reflected from the scene, a lens is adopted, determining the field of view (FOV) of the sensor and the consequent amount of modulated light that this lens will gather on the sensor to create the depth image.

Focal length is the distance from the back of the lens to the plane of the image formed of an object placed infinitely far in front of the lens. The angular field of view of a lens is related to the focal length as for the following equation:

$$\mathrm{FOV} = 2\tan^{-1}\left(\frac{h}{2f}\right) \tag{18.41}$$

where f is the focal length and h is the horizontal dimension of the lens.

The shorter the focal length, the shorter the distance needed to obtain the same FOV compared to a longer focal length lens. The lower the focal number, the better the SNR.

Another issue in ToF is the problem of occlusion shadows, a limiting factor for 3-D vision. FOV is strictly affecting this issue since the critical distance of the object projecting a shadow is related to the FOV.

A last important effect that may produce artifacts is the motion blur. Motion blur is linked to relative motion of the camera with respect to the target, causing errors in the calculation of the depth.

Non-systematic errors can also occur:

- Light scattering: Different levels of illumination in two different objects at different distance may cause a depth distortion.
- Multipath error: Linked to the quoting of concave shapes. In this case the captor is not coherently interpreting the reflection coming from adjacent points, giving back a distorted image.
- Object boundary error: When the edge of an object in foreground and a wide background have similar color, the edge of the object in foreground is distorted.

ToF has also systematic intrinsic depth errors in particular due to:

- Amplitude ambiguity: The amplitude of an IR signal depends on the distance but also on the color of the measured object. This may lead to misinterpretation of the phase shift and consequent distance errors.
- Integration time based: Longer integration time is giving higher accuracy.
- Temperature and IR demodulation.

In conclusion, we can compare the different systems for the 3-D sensing solution using the following table (Table 18.5).

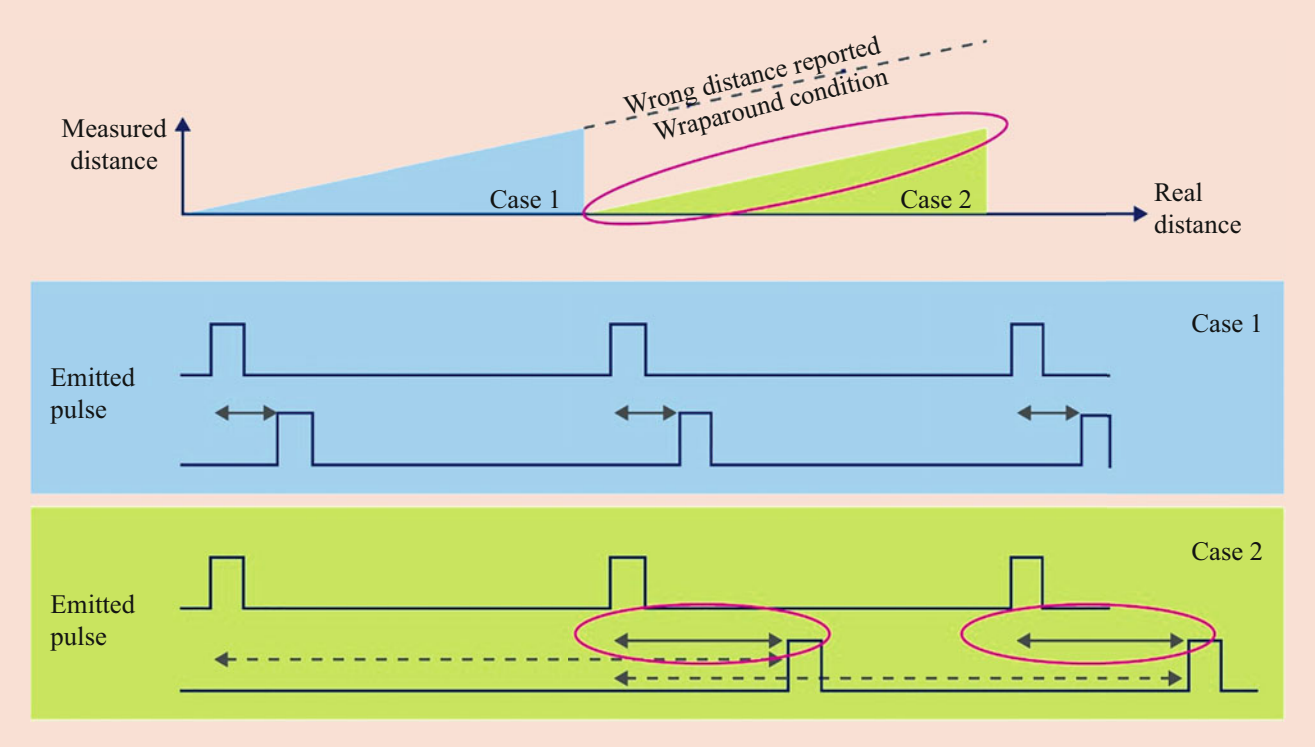

Fig. 18.69 Representation of the issues related to modulating period. (© 2018 by STMicroelectronics)

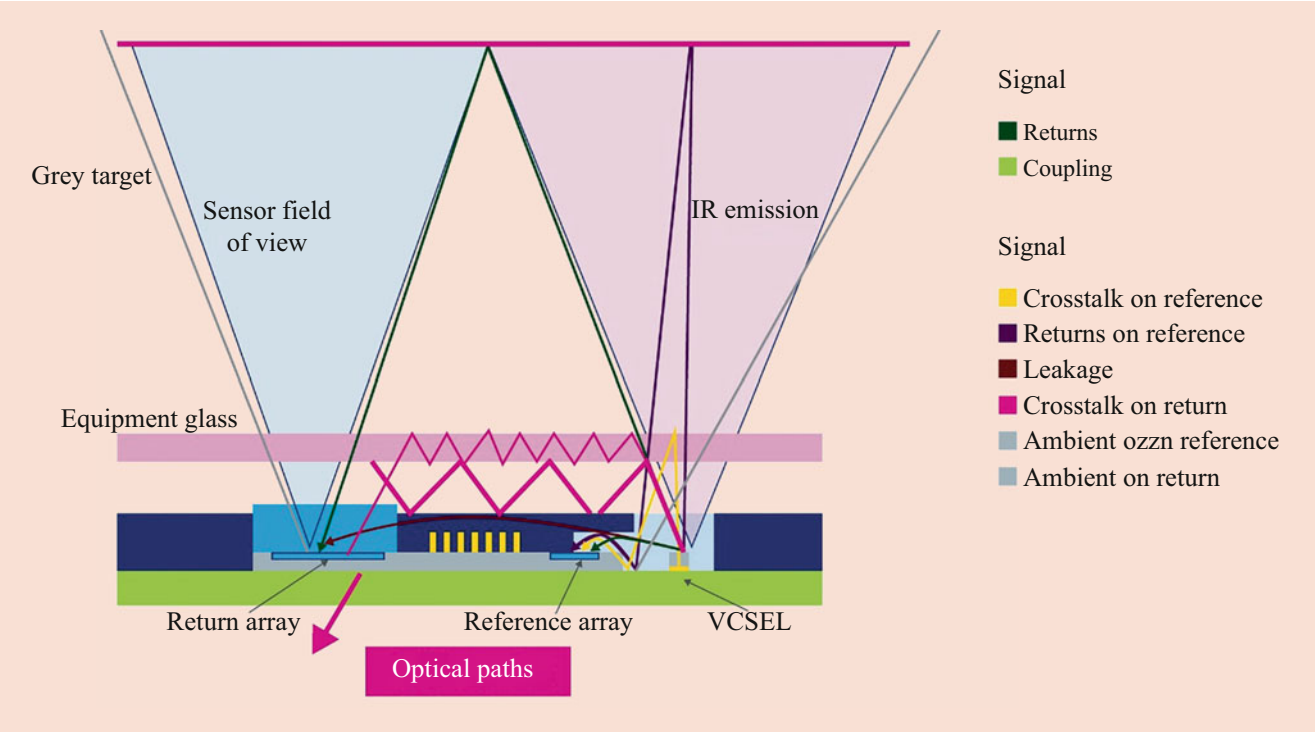

Fig. 18.70 Schematic representation of signal and noise paths. (© 2018 by STMicroelectronics)

Table 18.5 Comparison between different 3-D imaging techniques

Key feature	Stereo	Structured light	dToF	iToF
Baseline constraint	Yes	Yes	No	No
Mechanical alignment	Yes	Yes	No if all-in-one package	No if all-in-one package
Calibration cost	Much higher	Much higher	Much lower	Much lower
Optics	Standard	Standard and dedicated	Standard and dedicated	Standard and dedicated
Illumination	None, or diffuse	VCSEL, with coding lens	VCSEL, pulsed	VCSEL, modulated
Imager technology	Standard	Global shutter	SPAD	Fast photodiode
Number of pixels	Several Mpxl	1–3 Mpxl	< 100 Kpxl	100 kpxl to 1 Mpxl

Total system cost may vary, but we can affirm that ToF is about 30–40% cheaper than structured light. On the other hand, structured light is more accurate and more suitable for secure application (i.e., payment with people identification), allows an easier 2-D extraction (ideal for eye tracking in cabin driver monitoring), offers higher resolution, and is less prone to ToF errors.

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Solar Cells

19

Stephen M. Goodnick and Christiana Honsberg

Contents

19.1 Background and Basic Operation of Solar Cells 700

19.2 Solar Spectrum and Optical Properties 702
19.2.1 Solar Irradiance 702
19.2.2 Optical Properties of Photovoltaic Materials 703

19.3 Theory of Operation of Conventional Solar Cells ... 705
19.3.1 Dark Current and Recombination 706
19.3.2 Photocurrent 710
19.3.3 Series Resistance 712
19.3.4 Heterojunction Cells and Carrier Selective Contacts ... 714

19.4 Performance Comparison of Single Junction Technologies 719
19.4.1 Performance Limits of Si- and GaAs-Based Technologies 719
19.4.2 Thin Film Technology 721
19.4.3 Organic Solar Cells 721

19.5 Efficiency Limits for Photovoltaic Converter 722
19.5.1 Shockley-Queisser Limit 723
19.5.2 Overcoming the Shockley-Queisser Limit 723

19.6 Multijunction Solar Cells 724

19.7 Nanotechnology-Based Approaches 727
19.7.1 Nanomaterials 727
19.7.2 Dye-Sensitized and Quantum Dot Solar Cells 728
19.7.3 Light Management in Photovoltaics 730
19.7.4 Nanowire Solar Cells 731

19.8 Advanced Concept Photovoltaics 733
19.8.1 Intermediate Bands 733
19.8.2 Multiple Exciton Generation (MEG) 734
19.8.3 Hot Carrier Solar Cells 737

19.9 Summary 740

References 740

Abstract

In this review chapter, we present the current state of the art of photovoltaic device technology. We begin with an overview of the fundamentals of solar cell device operation, and the nature of the solar energy spectrum and light absorption in devices. We then go into detail of the basics of solar cell operation, and the effects of various factors on the primary figures of merit, the open circuit voltage, short circuit current, and fill factor. In particular we focus on recombination, both in terms of the photocurrent and the dark current affecting the cell voltage. We then discuss heterojunction solar cells, and the general concept of carrier selective structures, which improve solar cell performance. We summarize the main single junction technologies and their efficiencies historically, starting with Si wafer-based technology and GaAs, then thin film technology, and organic solar cells, ending with recent developments of hybrid perovskite-based solar cells.

The limits of solar cell performance in terms of energy conversion efficiency are discussed, where we introduce the concept of detailed balance to derive the Shockley-Queisser limit for single junction cells. Methods of circumventing this single gap limit are discussed, which set the stage for discussing multijunction or tandem solar cells which currently hold the record for highest conversion efficiency in any solar technology. We then discuss nanotechnology in general, and how it is increasingly incorporated in modern solar cells. In this context, we discuss the use of nanostructures in improving light management in solar cells by enhancing light trapping beyond the classical limit. We discuss quantum dot/nanoparticle-based cells such as dye-sensitized solar cells and nanowire solar cells. Finally, we conclude by discussing advanced concept solar cell structures such as intermediate band, multiexciton generation, and hot carrier solar cells, and their theoretical capability of greatly exceeding the Shockley-Queisser limit.

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Keywords

Solar energy · Photovoltaics · Nanotechnology and solar · Advanced concept solar · Shockley-Queisser limit

19.1 Background and Basic Operation of Solar Cells

Solar cells are semiconductor-based devices primarily, which convert sunlight directly to electrical energy through the *photovoltaic effect*, which is the appearance of a voltage and current when light is incident on a material. The photovoltaic effect was first reported by Edmond Becquerel in 1839, who observed a voltage and current resulting from light incident on electrochemical cells. Later in the 1800s, the first solid-state solar cells were developed based on platinum-selenium junctions. The first semiconductor-based pn junction cell was developed in the late 1930s and patented in 1946 by Russell Ohl at Bell Laboratories. The first practical solar cell devices utilizing the solar spectrum were demonstrated in 1954 at Bell Laboratories. While too expensive at the time for terrestrial applications, the burgeoning space industry found the first commercial applications of solar cells, as lightweight and long lifetime power sources replacing traditional battery technology for spacecraft in the late 1950s. Photovoltaics has since developed into the fastest growing source of terrestrial renewable energy, with an installed global capacity of over 600 GW peak energy by the end of 2019. This growth in capacity has been driven by the exponential decrease in the manufacturing cost for photovoltaic panels, which has dropped from $75/watt in the late 1970s to under $0.30/watt today, as a result of continuous improvements in materials, device efficiency, and manufacturing scale-up. Coupled with this dramatic cost reduction, the lifetime of solar panels is in excess of 25 years, which has dramatically reduced the levelized cost of electricity (LCOE) from photovoltaics, with some recent utility-scale installations priced below $0.02/kWhr, cheaper than any other current source of electricity.

Figure 19.1 illustrates the photovoltaic conversion process in a *pn* homojunction (same material on each side). It shows the energy band diagram (representative of the potential energy of electrons) as a function of position across the junction, where E_c is the minimum energy of the *conduction band*, which is primarily in unfilled state, and E_v is the maximum energy of the valence band which is almost completely filled. They are separated by an energy gap, E_g (1.12 eV in the case of Si at room temperature, the dominant semiconductor material), where no states exist in the ideal material. The junction occurs between an n-type semiconductor material (intentionally doped with donor atoms that contribute electrons to the conduction band) and a p-type material doped with acceptors, which remove an electron from the valence band, leaving behind a positively charged *hole*, which behaves as a positive charge carrier. The degree of filling of either the conduction band by electrons or the valence bands by holes is represented by the Fermi energies on the n- and p-sides, denoted E_{fn} and E_{fp} in the figure. At equilibrium, the Fermi energies are the same across the junction. At the junction, because of the huge gradient of positive charge on one side and negative on the other, a *space charge region* (SCR) is established at the junction, which is devoid of free carriers, and has a high electric field which opposes the flow of free charge from the n-region to the p-region and vice versa. As shown in Fig. 19.1, this results in a potential barrier for electrons on the n-side (right side) to cross the junction, while it is likewise a potential barrier for holes from the p-side (left side) to move across (since the diagram is of electron potential energy, increasing hole potential and kinetic energy is downward).

In the quantum mechanical description of photovoltaics, photons (quanta of electromagnetic radiation) are absorbed if their energy, $h\nu$ (ν is the frequency of the incident light), exceeds the bandgap, and, in so doing, excite an electron from a filled state in the valence band to an empty state in the conduction band, creating *electron-hole pairs* (EHPs) as shown. Photons below the bandgap are not absorbed, which is the first major loss mechanism in terms of conversion of optical to electrical energy. The photoexcited electron and hole each have an excess kinetic energy above or below the conduction and valence band edges, respectively, and on a very short time scale (picoseconds), they relax to the their respective band edges through thermal losses to the underlying semiconductor material (through phonon emission, where quantum mechanically, phonons are quanta of the wave-like vibrational motion of the crystal). Hence, all the excess energy of the photon above the bandgap is lost, which is the second major loss mechanism, limiting the conversion efficiency of a solar cell as discussed in Sect. 19.5.

Once an EHP is created by absorption of a photon, what is required is charge separation of the electron and hole to opposite contacts to establish a *photocurrent*. This process requires some sort of symmetry breaking in the material, which is provided by the SCR shown in Fig. 19.1, where, as shown, the photoexcited electron on the p-side, if it reaches the edge of the SCR through diffusive motion, is swept across by the high electric field contributing to the photocurrent. The corresponding hole of the initial EHP sees a barrier at the junction on the other hand and so preferentially finds its way to the contact in the p-type material where it is extracted. The opposite process occurs for photons absorbed on the n-side but with the result of a photocurrent in the same direction. If the electron or hole created on a given side of the SCR *recombines*, i.e., the conduction band electron annihilates a

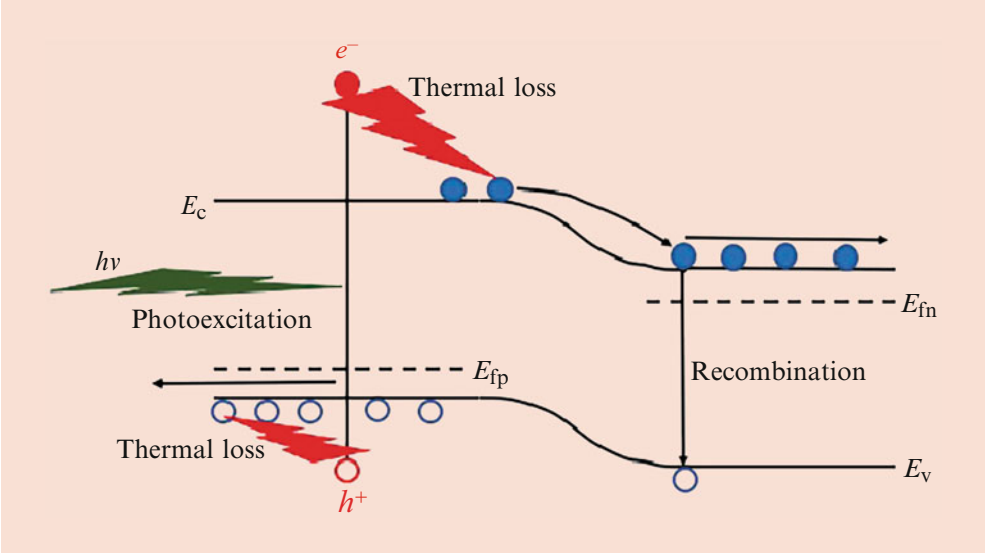

Fig. 19.1 Illustration of the physics of the photovoltaic effect in a *pn* junction solar cell

hole in the valence band either through being trapped in a defect state (Shockley-Read-Hall recombination) or directly via band to band recombination and light emission (radiative recombination), then that EHP is lost to the photocurrent generation process. Therefore, another contribution to the overall conversion efficiency is the competition between extraction of the carriers and recombination before carriers are separated by the junction.

In terms of the solar cell delivering power to an external load, Fig. 19.2 illustrates the equivalent circuit model for a solar cell and its load. It consists of an ideal current source corresponding to the photocurrent, I_{ph}, in parallel with a diode, representing the *pn* junction. For a *pn* junction in the dark, when it is forward biased with a positive voltage applied to the p-side with respect to the opposite side, a large current can flow, due to the lowering of the potential barrier in Fig. 19.1, whereas in reverse bias, this barrier is increased by the bias, creating a large barrier to charge flow and hence small current. The general form of the diode current for junction devices is exponential

$$I_D = I_0 \left(e^{qV_D/nkT} - 1\right) \tag{19.1}$$

where V_D is the voltage across the diode (the same as V, the voltage across the load in Fig. 19.2), q is the charge of an electron, n is the ideality factor which varies between 1 and 2 usually, and I_0 is the reverse saturation current, which physically is a result of recombination of electrons and holes in and near the junction. As discussed in Sect. 19.3.1, recombination can be radiative, where a photon is emitted when an electron decays into a hole state; it can occur through intermediate trap states in the bandgap, or through Auger processes, and typically has an exponential dependence on the bandgap over the thermal voltage, i.e., $-E_g/kT$. Eq. 19.1 shows that for positive V_D the current increases exponentially whereas in reverse bias, for negative V_D, the current goes to a small value, I_0. In terms of the equivalent circuit in Fig. 19.2, under short circuit current conditions ($R_L = 0$), the short circuit current equals the photocurrent, $I_{sc} = I_{ph}$. As the resistance of the load increases from zero, there is an increasing voltage across the diode, $V_D = V = IR_L$, due to the photocurrent which forward biases the diode, increasing I_D, and hence decreasing the net current to the load. The load current decreases until it goes to zero, corresponding to open circuit conditions when $R_L = \infty$. Under open circuit conditions, $I_D = I_{ph} = I_{sc}$. Equating the diode current with the short circuit current in Eq. (19.1) at open circuit voltage conditions, $V_D = V_{oc}$, leads to

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{I_{sc}}{I_0} + 1\right) \tag{19.2}$$

The open circuit voltage depends most importantly on the reverse saturation current, I_0, characteristic of the *pn* junction, and, as mentioned above, decreases exponentially with bandgap. Hence the open circuit voltage scales linearly with bandgap, increasing for increasing bandgap materials, and empirically is found to be about 0.4 V less than the bandgap for a given material in well-developed technologies, i.e., $V_{oc} \approx E_G(in\ volts) - 0.4$ V.

Figure 19.2 also illustrates the current-voltage characteristic of the solar cell in the dark, and under illumination, where the convention has been used of defining the net solar cell current, I, as flowing into the device, corresponding to negative power in terms of the product of IV, or power generation. As can be seen, the I-V characteristic under illumination is

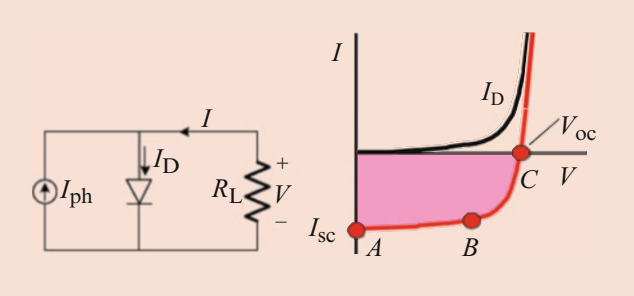

Fig. 19.2 Equivalent circuit of the solar cell and the corresponding current-voltage characteristics and important points along the *I-V* curve

shifted rigidly downward, which illustrates the assumption of *superposition*, that the dark current and photocurrent can be treated independently, which is not generally the case. The points *A*, *B*, and *C* along the curve denote the short circuit current, the maximum power point, and open circuit. The maximum power at point *B* is $P_m = I_m\, V_m$, which is less than the product $I_{sc}\, V_{oc}$, due to the "roundness" of the *I-V* curve as seen in Fig. 19.2, characterized by the *fill factor* (*FF*), i.e., $P_m = \mathrm{FF} I_{sc}\, V_{oc}$. In terms of the total optical energy incident on the device area, P_{in}, the optical to electrical conversion efficiency, η, is given by

$$\eta = \frac{V_{oc} I_{sc} \mathrm{FF}}{P_{in}} \tag{19.3}$$

The optical to electrical conversion efficiency,η, I_{sc}, V_{oc}, and the fill factor, FF, are all figures of merit related to the performance of different photovoltaic technologies, discussed in more depth throughout the rest of this chapter. In what follows, we go into more depth into the materials and physics of present-day photovoltaics technology, starting with the properties of the solar spectrum, and then beginning with Si-based solar cells that are currently the dominant technology worldwide, and continuing through thin film and organic technologies. Due to space limitations, we only provide the basics of solar cell device physics, which are covered in more detail in [1]. We then look at what limits the efficiency of conventional solar cells, and look at more advanced approaches to high efficiency performance in terms of multiple junction solar cells, as well as advanced concept approaches, and implementations thereof using nanotechnology, and some perspectives on future developments in the field.

19.2 Solar Spectrum and Optical Properties

In the present section, we first introduce the properties of the solar spectrum in terms of its blackbody characteristic from the sun incident on Earth, and atmospheric absorption and scattering effects on the corresponding terrestrial solar spectrum which are relevant for solar energy conversion at different locations on Earth. We then discuss the physics of optical absorption in semiconductors, and some basic design considerations for solar cells in terms of maximizing absorption and the corresponding photocurrent.

19.2.1 Solar Irradiance

The solar spectrum in space is modeled to a high level of accuracy by Planck's blackbody radiation law, where the intensity as a function of wavelength is given by

$$I(\lambda) = R_{sun}^2/D^2 \times \frac{2\pi hc^2}{\lambda^5 \left(\exp\left(\frac{hc}{\lambda kT}\right) - 1\right)} \tag{19.4}$$

where R_{sun} is the radius of the sun, D is the distance from the sun, T is the temperature of the sun, λ is the wavelength, c is the speed of light in vacuum, h is Plank's constant, and k is Boltzmann's constant. In terms of the photon flux associated with this intensity, the number of photons per unit time per unit area is simply found by dividing by the photon energy.

$$N(\lambda) = I(\lambda)/(h\nu) = \frac{\lambda I(\lambda)}{hc}; \quad \lambda\nu = c \tag{19.5}$$

where N is the photon flux in terms of number per unit time per unit area per unit wavelength.

Figure 19.3 shows the ideal blackbody intensity assuming a temperature of 5250 C in Eq. (19.4) (the solid curve), compared with the solar spectrum at the top of the Earth's atmosphere, where the difference is quite small. The red curve shows the actual spectrum somewhere on the Earth's surface, where absorption and reflection losses from atmospheric constituents (water, CO_2, etc.) as well as Raleigh scattering (at shorter wavelengths) reduce the intensity of light, particularly at certain preferential absorption wavelengths.

Integration of Eq. (19.4) over all wavelengths (assuming the temperature of the sun is 5762 K) gives a value of 1366 W/m^2, referred to as the *solar constant*, representing the maximum available solar power reaching the Earth. The intensity on Earth is reduced due to atmospheric absorption as evidenced in Fig. 19.3. While local fluctuations in intensity occur due to various local atmospheric effects such as clouds and humidity, in general, the solar intensity at the surface is reduced due to the increasing path length through the atmosphere, and consequent absorption and scattering, which increases with increasing latitude. The increase in path length is characterized by the *air mass*, which is defined as the ratio of path length through the atmosphere normalized by

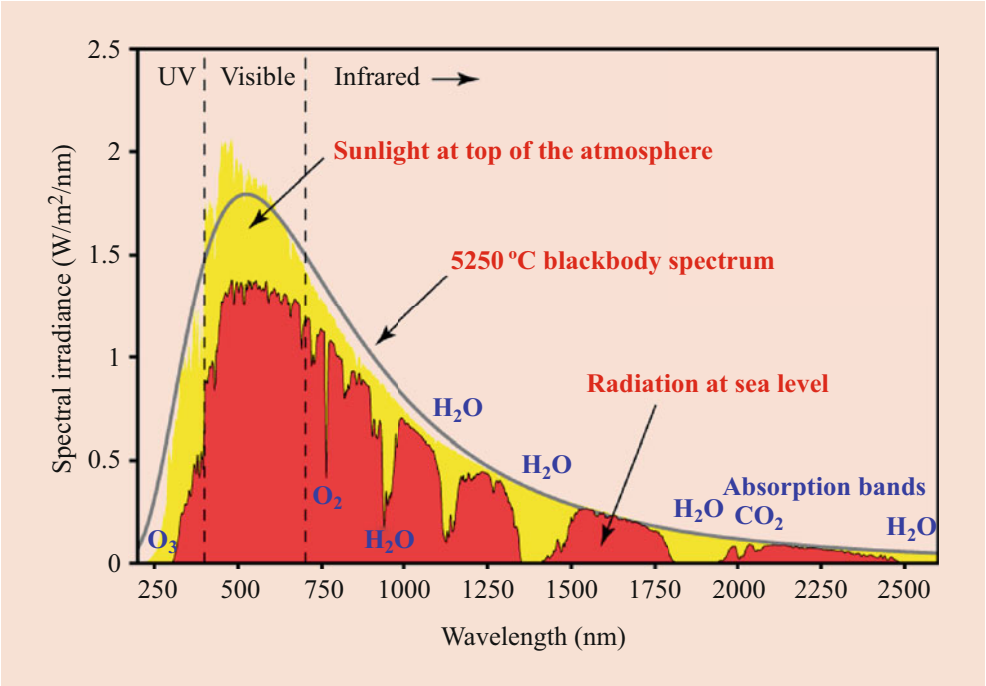

Fig. 19.3 Solar spectrum showing the incident power versus wavelength in outer space and on the Earth's surface. The solid curve is the ideal blackbody spectrum. (Source: the Wikimedia Commons)

the shortest path length at the equator. Geometrically, the air mass is approximately given by

$$\mathrm{AM} = 1/\cos(\theta) \tag{19.6}$$

where θ is the angle between the sun at a given latitude and the normal to the atmosphere at the equator. Equation (19.6) comes from just the geometrical increase in path length in a rectangular geometry. If the curvature of the atmosphere itself is included, and empirical correction to Eq. (19.6) is given as

$$\mathrm{AM} = \frac{1}{\cos(\theta) + 0.50572(96.07995 - \theta)^{-1.6364}} \tag{19.7}$$

AM0 is top of atmosphere, therefore AM = 0. For the sun directly overhead, AM = 1. Given the air mass, AM, the solar intensity at any point is given by the approximate formula [1]

$$I \approx 1.1 \times 1366(0.7)^{\mathrm{AM}^{0.678}} \tag{19.8}$$

A widely used air mass is AM1.5, corresponding to a latitude of 48.2°, representing an average latitude of temperate zones in either the northern and southern hemispheres. The AM1.5 intensity is approximately 930 W/m^2, significantly reduced from the solar constant. Because of atmospheric scattering (Raleigh) as well as dust particles, water vapor, etc., a fraction of the radiation incident on the solar panel is indirect, in the form of diffuse radiation, which comes in from all angles rather than directly from the disk of the sun itself. Both components, diffuse and direct, should be considered in modeling of photovoltaic system performance.

19.2.2 Optical Properties of Photovoltaic Materials

In the previous section, we discussed the intensity and spectral content of solar radiation. For describing solar cell design and operation, what is critically important is the absorption of the incident photons as a function of wavelength, described by the absorption coefficient of the semiconductor described in more detail below.

Optical absorption in semiconductors depends on band to band transitions from the valence band to the conduction band. Due to the quantum nature of light, the absorption of photons can only occur when $h\upsilon > E_G$ (although in fact sub-bandgap photons can be absorbed through impurities and other states in the gap). The nature of such transitions and the strength of absorption depends on whether the semiconductor is a direct or indirect gap material. In the former case, transitions occur directly from valence to conduction band leading to strong absorption when the photon energy exceeds the bandgap. For indirect materials, the conduction and valence

band minimum and maximum, respectively, occur at different crystal momentum, and therefore at the bandgap, a second-order phonon-assisted process is required, and hence absorption is reduced until a direct conduction band minimum is bridged by the photon energy.

The quantity characterizing absorption is the absorption coefficient, α, which is basically the inverse of the average depth a photon penetrates a material before being absorbed. Mathematically, this may be written

$$N_{\mathrm{ph}}(x) = N_{\mathrm{s}} \mathrm{e}^{-\alpha x} \tag{19.9}$$

where $N_{\mathrm{ph}}(x)$ is the photon flux at distance x relative to the surface and N_{s} is the photon flux incident on the surface. The change in the number of photons gives the generation rate, such that

$$G(x) = -\frac{\mathrm{d}N_{\mathrm{ph}}}{\mathrm{d}x} = \alpha N_{\mathrm{s}} \mathrm{e}^{-\alpha x} \tag{19.10}$$

The above equation for the generation rate shows that G varies not only with the wavelength of light but also with distance into the material. Figure 19.4 plots the absorption coefficient as a function of wavelength for several materials. As can be seen, the absorption coefficient for Si is weaker compared to GaAs and InP due to its indirect bandgap for the same relative photon energy to the gap itself (similarly for thin film materials like CdTe), with the consequence that the thickness of Si required for high quantum efficiency (i.e., the number of electrons collected per incident photon) is much higher than for direct gap materials like GaAs.

As illustrated in Fig. 19.4, the absorption coefficient is weakest for a given material for long wavelength photons just above the bandgap in energy, while shorter wavelength photons are absorbed within a short distance from the surface. Thus, the design of a Si solar cell reflects the spectral nature of the absorbed photons. This is illustrated in Fig. 19.5 for a basic Si cell design, where longer wavelength red light has a relatively long absorption depth, whereas short wavelength blue light is absorbed near the surface.

The structure of a commercial Si solar cell device (left panel of Fig. 19.5) typically has a thick base region (here p-type), a narrow emitter layer that is highly doped to minimize lateral resistance, heavy doping near the back contact to reduce recombination of photogenerated electrons there (back surface field), and a grid top contact to the emitter

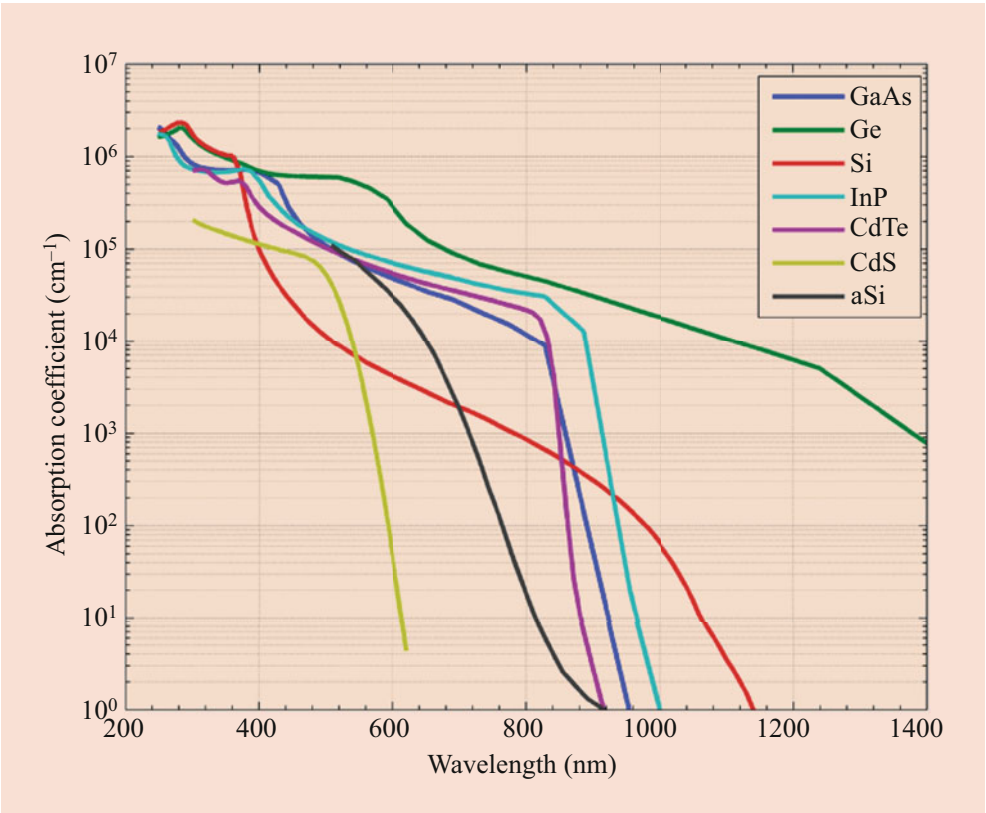

Fig. 19.4 Absorption coefficient versus wavelength for several direct gap materials (GaAs, InP, CdTe, CdS) and two indirect gap materials (Ge, Si) as well as amorphous Si. (With permission from PVEducation.org)

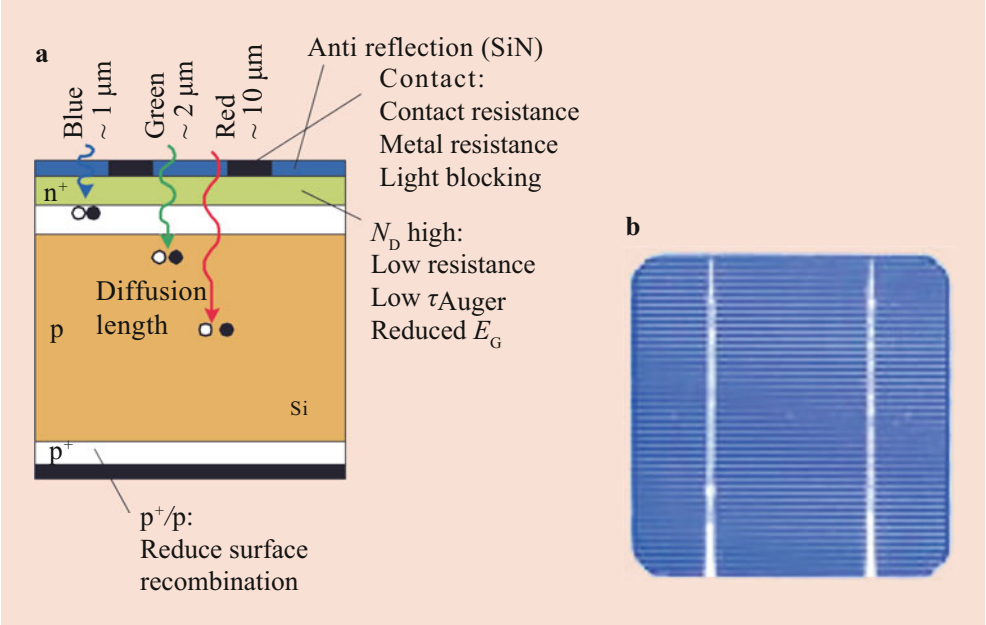

Fig. 19.5 Cross-sectional view showing the structure of a typical Si homojunction solar cell (**a**) showing the penetration of different metallization allowing light absorption and carrier collection with minimal shading (**b**)

which has narrow fingers to minimize optical reflection (right panel is a top view of the grid structure). The design of the top grid involves a trade-off between the shading due to the area of the grid, which reduces the optical absorption through reflection, and the lateral spreading resistance due to current flow in the emitter (n^+) region toward the fingers. Another optical consideration is the reflection of light from the semiconductor surface due to the refractive index difference between the cell and the air (or glass). As shown in Fig. 19.5, the design of the basic cell structure includes an antireflection (AR) coating of a material with refractive index between that of the semiconductor and air (here, e.g., silicon nitride), with the thickness optimized for minimum reflection across the solar spectrum (Fig. 19.3). A number of different wide bandgap insulating materials are used for AR coatings such as SiO_2, MgF_2, and others. Additionally, transparent conducting oxides (TCOs) are often employed, especially in more advanced solar cell architectures, which are wide bandgap materials ($E_G > 3$ eV) and typically heavily n-type self-doped materials due to defects and other sources. In addition to providing a role as an AR material, they provide a conducting surface layer which mitigates spreading resistance effects. As discussed in more detail in Sects. 19.3.2 and 19.7.3, other schemes under the general category of *light management* are employed to increase the path length of light within the semiconductor and thus increase absorption, including a back optical reflector and texturing the front surface to deflect normal incident light into random angles inside the absorbing layer.

19.3 Theory of Operation of Conventional Solar Cells

Homojunction solar cells are basically *pn* junction solar cells from conventional single crystal or multi-crystalline semiconductor wafer-based materials such as Si and GaAs that some authors [2] have referred to as first generation due to their early appearance in the historical development of photovoltaics discussed earlier. Here we provide a brief introduction to the theory of homojunction solar cells but refer the reader to more in-depth treatments of the subject in a number of textbooks [1, 3–6].

As discussed in Sect. 19.1, the overall current-voltage (*I-V*) relationship for a solar cell under illumination is assumed to be a linear superposition of the dark *I-V* of the underlying *pn* junction and the light-induced photocurrent which flows in the opposite direction. The dark current is ultimately dependent on minority carrier (i.e., holes in n-type material) recombination (including the contacts themselves), and as such, an understanding and control of this phenomena are critical to high performance. The photocurrent depends on both the optical generation process discussed in the previous section and on collection of the photogenerated carriers at the junction (shown in Fig. 19.1), which converts minority carriers into majority carriers. The collection process itself depends on minimizing recombination before the carriers reach the junction. The superposition approximation turns out to be well obeyed in state-of-the-art Si and III–V

technologies, although less so in thin film and organic-based technologies, where the nonlinear dependence of recombination on intensity and other factors leads to a breakdown of this approximation. Nevertheless, we begin by considering recombination and its effect on dark current, followed by the photocurrent and control of series resistance effects, and then look at advances in performance through heterojunctions and carrier selective contacts, ending with a discussion of current performance limits of single crystal and multi-crystalline Si and GaAs technology.

19.3.1 Dark Current and Recombination

In the following, we discuss the various recombination mechanisms in semiconductors, and the role of recombination in the dark current of conventional junction solar cells.

Recombination and Minority Carrier Lifetime

Solar cells are highly dependent on the effective minority carrier lifetime, such that the minority carrier lifetime is one of the most important parameters in a solar cell. Solar cell technology can be described as maximizing the effective minority carrier lifetime, given practical constraints such as cost or scalability. The minority carrier lifetime affects both the short circuit current and open circuit voltage as mentioned above. Note that the effective minority carrier lifetime includes the effect of surfaces.

The minority carrier lifetime is dependent on multiple parameters, including the processing history of the material, the type and number of defects in the material, the solar cell operating point, and other device parameters. Here we seek to develop equations and values for the minority carrier lifetimes in terms of relevant material parameters.

The term *minority carrier lifetime* can refer to different physical recombination mechanisms. We define the general term to refer to the effective minority carrier lifetime, which is a combination of both bulk and surface recombination mechanisms. The effective minority carrier lifetime is related to the minority carrier lifetime from individual physical processes by the equation below

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{Auger}}} + \frac{1}{\tau_{\text{radiative}}} + \frac{1}{\tau_{\text{SRH}}} + \frac{1}{\tau_{\text{Surf}}} \tag{19.11}$$

where the four lifetimes correspond to Auger recombination, radiative (direct) recombination, trap-based recombination (Shockley-Read-Hall), and surface recombination. The effective minority carrier lifetime is the parameter, which is usually measured and then de-convolved into its individual components by either additional measurements or by fitting calculations.

Radiative recombination is proportional to the density of electrons in the conduction band, and the density of holes in the valence band, expressed as

$$R_{\text{rad}} = Bnp \tag{19.12}$$

where R_{rad} is the radiative recombination rate of electron-hole pairs (EHPs), the proportionality constant, B, is the recombination coefficient, while n and p are the electron and hole concentrations, respectively. The net radiative recombination of *excess* minority carriers is the total radiative recombination minus the radiative recombination at equilibrium (where $np = {n_i}^2$, with n_i the intrinsic concentration of the material)

$$U_{\text{rad}} = R_{\text{rad}} - R_{\text{rad}}^{\text{eq}} = B\left(np - n_i^2\right) \tag{19.13}$$

The minority carrier lifetime for radiative recombination can be found by

$$U_{\text{rad}} \equiv \frac{\Delta n}{\tau_{\text{Rad}}} = B\left(np - n_i^2\right) \tag{19.14}$$

Letting $n = \Delta n + n_0$ and $p = \Delta n + p_0$, where n_0 and p_0 are the equilibrium carrier concentrations, and using $\Delta n = \Delta p$ (due to charge neutrality) gives

$$\tau_{\text{Rad}} = \frac{1}{B\left((n_0 + p_0) + \Delta n\right)} \tag{19.15}$$

For low-level injection in n-type material ($n_0 \gg \Delta n$ and $n_0 \gg p_0$), where $n_0 \cong N_{\text{D}}$, the donor concentration, the minority carrier recombination due to radiative recombination becomes $\tau_{\text{Rad}} = 1/BN_{\text{D}}$, while for the same case in p-type material, $\tau_{\text{Rad}} = 1/BN_{\text{A}}$. Thus under low injection conditions, the value of the lifetime depends on the doping, but it does not depend on the number of carriers, which is determined by the injection level (the voltage of the solar cell).

For high-level injection on the other hand, $\Delta n \gg (n_0 + p_0)$, and $\tau_{\text{Rad}} = 1/B\Delta n$, which means the radiative lifetime decreases with increasing injection level, which is one way to differentiate this type of recombination in experiments such as time-resolved cathodoluminescence in which the injection level is controlled with the pump beam intensity.

Auger recombination is a three-particle interaction which occurs via two similar processes: (i) the recombination of an electron in the conduction band with a hole in the valence band, where the excess energy is given to an electron in the conduction band, and (ii) the recombination of an electron in the conduction band with a hole in the valence band, where the excess energy is given to a hole in the valence band.

In the first case, the particles involved in the recombination process are two electrons and a hole, and in the second, it is two holes and an electron. In each case, we subtract the recombination at equilibrium. The overall Auger recombination rate for these two processes is then

$$U_{\text{Auger}} = C_{\text{n}} n \left(np - n_i^2\right) + C_{\text{p}} p \left(np - n_i^2\right) \tag{19.16}$$

where C_{n} and C_{p} are the Auger recombination coefficients. Since Auger is often calculated in highly doped or highly excited material, we can usually neglect the $n_i{}^2$ term to get

$$U_{\text{Auger}} \cong C_{\text{n}} n^2 p + C_{\text{p}} p^2 n \tag{19.17}$$

Using the simpler form above and substituting $U_{\text{Auger}} \equiv \frac{\Delta n}{\tau_{\text{Auger}}}$, and also writing $n = \Delta n + n_0$ and $p = \Delta n + p_0$ and using $\Delta n = \Delta p$ (due to charge neutrality), gives

$$\tau_{\text{Auger}} = \frac{1}{C_{\text{p}} \left(n_0^2 + 2n_0 \Delta n + \Delta n^2\right) + C_{\text{n}} \left(p_0^2 + 2p_0 \Delta n + \Delta n^2\right)} \tag{19.18}$$

We sometimes only need the sum of these terms and this is called the ambipolar Auger coefficient C_{a}.

Similar to the radiative case above, under low-level injection conditions, the minority carrier recombination due to Auger in low-level injection becomes

$$\tau_{\text{Auger}} = \frac{1}{C_{\text{p}} N_{\text{D}}^2} \qquad \tau_{\text{Auger}} = \frac{1}{C_{\text{n}} N_{\text{A}}^2} \tag{19.19}$$

for holes in n-type material and electrons in p-type material, respectively. Here the Auger lifetime decreases as the square of the doping concentration, which imposes a limitation in terms of high doping. Under high-level injection conditions, the lifetime depends inversely on the square of the injected carrier concentration (i.e., Δn large)

$$\tau_{\text{Auger}} = \frac{1}{\left(C_{\text{p}} + C_{\text{n}}\right) \Delta n^2} \tag{19.20}$$

Finally, *Shockley-Read-Hall* (SRH) *recombination* is recombination mediated by traps. It is derived by considering the downward and upward transitions for an electron (hole) in a single trap level located at energy E_{T} with density N_{t}. Electrons in the conduction band are assumed to be captured with a rate proportional to the capture cross section, σ_{n}, traveling with a thermal velocity $v_{\text{th}} = \sqrt{3kT/m^*}$

$$\frac{1}{\tau_{p0}} = v_{\text{th}} \sigma_{\text{p}} N_{\text{t}} \tag{19.21}$$

with a similar expression for holes in the valence band. Exponential activation of electrons out of the trap to the conduction band (and electrons from the valence band to the trap level) is assumed as well, leading to the SRH recombination rate

$$U_{\text{SRH}} \equiv \frac{\Delta n}{\tau_{\text{SRH}}} = \frac{np - n_i^2}{\tau_{\text{p0}} \left(n + n_1\right) + \tau_{\text{n0}} \left(p + p_1\right)} \tag{19.22}$$

where

$$n_1 = n_i \exp\left(\frac{E_{\text{T}} - E_i}{kT}\right); p_1 = n_i \exp\left(\frac{E_i - E_{\text{T}}}{kT}\right) \tag{19.23}$$

where E_i is the intrinsic Fermi energy (approximately midgap). For low-level injection, and assuming the trap is located at the intrinsic level, i.e., midgap, the electron and hole minority carrier lifetimes reduce to τ_{n0} and τ_{p0}, respectively.

Surface recombination occurs due to traps at an interface or surface, with a two-dimensional density of trap states. Such states occur intrinsically due to the breaking of the translational symmetry of the crystal, and from dangling or differently bonded states on the surface. Since surface recombination occurs at a plane at a definite location, rather than distributed through the bulk of the solar cell, its effect in terms of the net recombination rate due to surface recombination depends on the distance from the surface. For that reason, the effect of surface recombination is often treated as a boundary condition on the flux due to recombination

$$D_{\text{n}} \frac{\text{d}n_{\text{p}}}{\text{d}x} = S_{\text{n}} \left(n_{\text{p}} - n_{\text{p0}}\right) \tag{19.24}$$

where for minority carrier electrons (n_{p}), D_{n} is the diffusion coefficient and S_{n} is a parameter called the surface recombination velocity, which is a proportionality constant between the excess carrier concentration at the surface, Δn_{p} (the rhs), and the flux toward the surface (lhs). S_{n} itself is proportional to the density of traps at the surface. An ohmic contact, in which equilibrium is established in the contact, can be thought of as surface recombination with an infinite recombination velocity (i.e., $n_{\text{p}} = n_{\text{p0}}$).

Dark Current

A *pn* diode is characterized by the presence of a space charge region (SCR) at the junction between the n- and p-regions due to the balance between the forces of carrier drift (due to electric fields) and diffusion (due to concentration gradients) between the different regions. The SCR is ideally assumed to be devoid of free carriers across its width W, with a fixed charged density due to ionized acceptors and donors for the p- and n-regions, respectively. This charge density is responsible for an electric field across the junction, which opposes the diffusion of carriers into the SCR (within the drift diffusion model of carrier transport), which in turn leads to a built-in potential between the two sides

$$V_{\mathrm{bi}} = \frac{kT}{q}\ln\left(\frac{N_{\mathrm{D}}N_{\mathrm{A}}}{n_i^2}\right) \tag{19.25}$$

and a corresponding width of the depletion region assuming an abrupt doping profile

$$W = \sqrt{\frac{q\left(N_{\mathrm{D}}+N_{\mathrm{A}}\right)\left(V_{\mathrm{bi}}-V_{\mathrm{D}}\right)}{\varepsilon_{\mathrm{s}}N_{\mathrm{D}}N_{\mathrm{A}}}} \tag{19.26}$$

where ε_{s} is the permittivity of the semiconductor, and we have included for generality the forward voltage, V_{D}, applied to the p-side with respect to the n-side.

Under forward bias conditions in the dark, the conventional description of behavior of a *pn* junction device is that the equilibrium state of the semiconductor is broken, leading to a quasi-equilibrium in which excess minority carriers are injected across the junction from their corresponding majority carrier n- and p-regions, due to the lowering of the built-in potential across the junction, as given in the equations above. The dark current in a *pn* junction device then arises from recombination currents due to this excess carrier, both in the bulk of the n- and p-regions through diffusion outside the SCR, as well as recombination within the SCR.

The quasi-equilibrium approximation assumes that the effect of the forward bias is to increase the minority carrier concentrations on either side of the junctions at $x = 0$ and $x' = 0$, as shown in Fig. 19.6, which illustrates an *n* (emitter) and *p* (base) structure. Under low-level injection conditions, the concentrations at these two points may be written

$$n_{\mathrm{p}}\left(x=0\right) = n_{\mathrm{p0}}\mathrm{e}^{qV_D/kT};\; p_{\mathrm{n}}\left(x'=0\right) = p_{\mathrm{n0}}\mathrm{e}^{qV_D/kT} \tag{19.27}$$

where $n_{\mathrm{p0}} = n_i^2/N_{\mathrm{A}}$ and $p_{\mathrm{n0}} = n_i^2/N_{\mathrm{D}}$ are the equilibrium concentrations of minority carrier electrons and holes on the p- and n-sides, respectively.

The regions outside the SCR defined by W in Fig. 19.6 are assumed to be charge neutral with no electric field. Hence, we can solve the semiconductor minority carrier diffusion equations in both regions

$$\begin{aligned} D_{\mathrm{n}}\frac{\mathrm{d}^2n_{\mathrm{p}}(x)}{\mathrm{d}x^2} - \left[U_{\mathrm{n}}(x) - G_{\mathrm{n}}(x)\right] = 0;\; D_{\mathrm{p}}\frac{\mathrm{d}^2p_{\mathrm{n}}\left(x'\right)}{\mathrm{d}x'^2} \\ - \left[U_{\mathrm{p}}\left(x'\right) - G_{\mathrm{p}}\left(x'\right)\right] = 0 \end{aligned} \tag{19.28}$$

where $U_{\mathrm{n,p}}$ and $G_{\mathrm{n,p}}$ are the recombination and generation rates for minority carriers, with $G_{\mathrm{n,p}}(x)$ given by Eq. (19.7), and the holes are solved in the x' coordinate system on the left (positive x' to the right). The solutions require two boundary conditions (BCs); Eq. (19.24) for the excess carrier concentration injected across the boundary serves as BCs at $x, x' = 0$. At the other boundaries, we assumed the surface recombination conditions

$$\begin{aligned} D_{\mathrm{n}}\frac{\mathrm{d}n_{\mathrm{p}}}{\mathrm{d}x}\bigg|_{x=W_{\mathrm{p}}} &= S_{\mathrm{n}}\left(n_{\mathrm{p}}\left(W_{\mathrm{p}}\right) - n_{\mathrm{p0}}\right); \\ D_{\mathrm{p}}\frac{\mathrm{d}p_{\mathrm{n}}}{\mathrm{d}x}\bigg|_{x'=W_{\mathrm{n}}} &= S_{\mathrm{p}}\left(p_{\mathrm{n}}\left(W_{\mathrm{n}}\right) - p_{\mathrm{n0}}\right) \end{aligned} \tag{19.29}$$

For the case of the dark current, $G_{\mathrm{n,p}}(x) = 0$, the general solutions are in the form of hyperbolic functions due to the combination of exponential solutions to the ordinary differential equations above.

The current densities on either side of the junction are expressed in terms of the diffusion current of charge carriers diffusing away from the junction in terms of the carrier gradients

$$J_{\mathrm{n}} = qD_{\mathrm{n}}\frac{\mathrm{d}n_{\mathrm{p}}(x)}{\mathrm{d}x};\; J_{\mathrm{p}} = -qD_{\mathrm{p}}\frac{\mathrm{d}p_{\mathrm{n}}\left(x'\right)}{\mathrm{d}x'} \tag{19.30}$$

The total current is the sum of these two in the general form of Eq. (19.1)

$$J = J_0\left[\mathrm{e}^{qV_{\mathrm{D}}/kT} - 1\right] \tag{19.31}$$

where the reverse saturation current density, J_0, is given in general by.

$$\begin{aligned} J_0 = \Bigg(& \frac{qD_{\mathrm{n}}n_i^2}{L_{\mathrm{n}}N_{\mathrm{A}}}\cdot\frac{\cosh\left(\frac{W_{\mathrm{P}}}{L_{\mathrm{n}}}\right) + \frac{D_{\mathrm{n}}}{S_{\mathrm{n}}L_{\mathrm{n}}}\sinh\left(\frac{W_{\mathrm{P}}}{L_{\mathrm{n}}}\right)}{\frac{D_{\mathrm{n}}}{S_{\mathrm{n}}L_{\mathrm{n}}}\cosh\left(\frac{W_{\mathrm{P}}}{L_{\mathrm{n}}}\right) + \sinh\left(\frac{W_{\mathrm{P}}}{L_{\mathrm{n}}}\right)} \\ & + \frac{qD_{\mathrm{p}}n_i^2}{L_{\mathrm{p}}N_{\mathrm{D}}}\frac{\cosh\left(\frac{W_{\mathrm{N}}}{L_{\mathrm{p}}}\right) + \frac{D_{\mathrm{p}}}{S_{\mathrm{p}}L_{\mathrm{p}}}\sinh\left(\frac{W_{\mathrm{N}}}{L_{\mathrm{n}}}\right)}{\frac{D_{\mathrm{p}}}{S_{\mathrm{p}}L_{\mathrm{p}}}\cosh\left(\frac{W_{\mathrm{N}}}{L_{\mathrm{p}}}\right) + \sinh\left(\frac{W_{\mathrm{N}}}{L_{\mathrm{p}}}\right)}\cdot\Bigg) \end{aligned} \tag{19.32}$$

where $L_{\mathrm{n,p}} = \sqrt{D_{\mathrm{n,p}}\tau_{\mathrm{n,p}}}$ is the diffusion length for electrons (*n*) and holes (*p*), which is the average distance they diffuse before recombining, and the equilibrium minority carrier concentrations, n_{p0} and p_{n0}, have been written in terms of the doping concentrations on either side of the SCR, $n_i^2/N_{\mathrm{A,D}}$, respectively. Here the form of the diode equation has an ideality factor $n = 1$. In the more general case including recombination in the space charge region and high-level injection at high bias, the ideality factor can vary between $n = 1$ and 2 depending on the bias.

The above expression simplifies in two cases, one in which the thicknesses of the emitter and base regions W_{n} and W_{p} are much larger than L_{p} and L_{n}, respectively (short base/emitter), and the other, which corresponds to the opposite, in which the regions are so short that no recombination occurs (short-/base), further assuming ohmic contacts with infinite S_{p} and S_{n} (short base/emitter). This may be written generally as

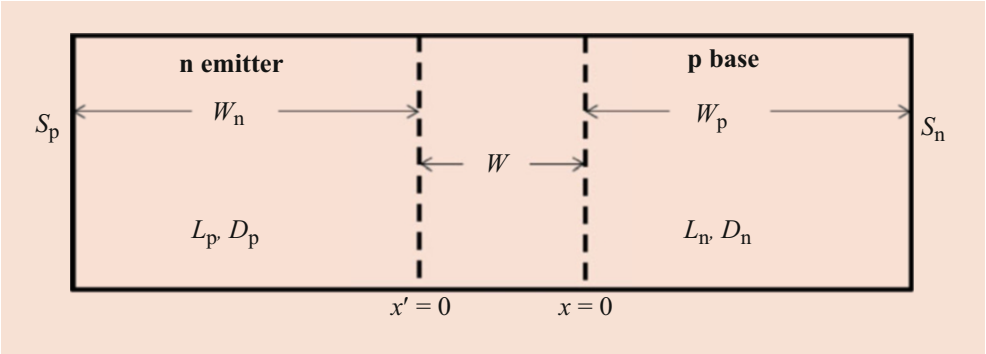

Fig. 19.6 Solution domain for the minority carrier diffusion equations for an *np* junction device

$$J_0 = \left[q\frac{D_n n_i^2}{X_n N_A} + q\frac{D_p n_i^2}{X_p N_D} \right] \tag{19.33}$$

where $X_{n,p} = W_{p,n}$ for the short base/emitter case and $X_{n,p} = L_{n,p}$ for the long base/emitter case.

The open circuit voltage given in Eq. (19.2) can be rewritten in terms of the current densities as

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{J_{sc}}{J_0} + 1\right) \tag{19.34}$$

Clearly V_{oc} depends on minimizing the dark current, characterized by J_0, which arises due to recombination in the various regions and surfaces. Several general trends can be observed from the expression for J_0. Increasing the doping on both sides increases the built-in potential and correspondingly $V_{oc.}$ However, the diffusion coefficients, $D_{n,p}$, are proportional to the carrier mobility, which degrade with increasing doping due to ionized impurity scattering. Further, for very high doping, there is increased recombination due to Auger processes which decreases the diffusion lengths, as well as bandgap narrowing effects, which increase n_i due to its exponential dependence on the bandgap. Figure 19.7 shows the dependence of the open circuit voltage on doping in a conventional architecture, where the degradation of the diffusion length with doping correlates with a degradation of V_{oc}.

The above analysis did not address specifically the role of surface recombination on the open circuit voltage, but looking at Eq. (19.30), with infinite recombination velocity, the dark current is clearly much larger than the case limited by the diffusion length. Thus, reducing $S_{n,p}$ through *passivation* of the front and back surfaces is critical in good cell performance, particularly considering that in state-of-the-art Si solar cells, the diffusion length is typically much longer than the entire wafer thickness.

Figure 19.8 illustrates the solution of the minority carrier diffusion equation in the limit that the based width W_p is much less than the diffusion length, L_n, in Fig. 19.6, where the solution is just a straight line. In the case of a conventional ohmic contact, where $S_n = \infty$, the minority carrier concentration goes to zero at the boundary, and the current is given by the slope of the line times the diffusion coefficient for minority carrier electrons, D_n. As S_n decreases, so does the slope and the corresponding minority carrier current. Asymptotically, the solution goes back to the long base solution as $S_n \to 0$.

Reducing the minority carrier current extracted through the front and back is therefore a major strategy in the design of solar cells for maximizing V_{oc}. However, at the same time, we have to extract majority carriers through low resistance contacts, which is somewhat of a contradiction. Design of contacts which have high majority carrier extraction but low minority carrier extraction is the goal of carrier selective contact design, discussed in more detail in Sect. 19.3.4.

A traditional strategy for reducing minority carrier recombination in the contact region is the use of a back surface field (BSF), which usually involves having a higher doped region in the vicinity of the back contct. The isotope junction formed between a p^+ and p-region results in a SCR with a field that opposes the flow of electrons toward the *p* contact, reducing the effective surface recombination velocity. This results in a V_{oc} increase of several tens of mV.

The above analysis has considered the current density in a one-dimensional analysis, but another approach to reducing the effective recombination on the back is to minimize the contact area laterally through selective contacts to the base with local BSFs, where the rest of the back surface is highly passivated by a dielectric layer. Here the ratio of the passivated area is high compared to the actual contact area, with a commensurate reduction in dark current. This structure is the basic architecture of the PERC (passivated emitter and rear contact) solar cell, which is presently (in 2020) the dominant commercial Si technology, and has demonstrated cell efficiencies greater than 24% [7].

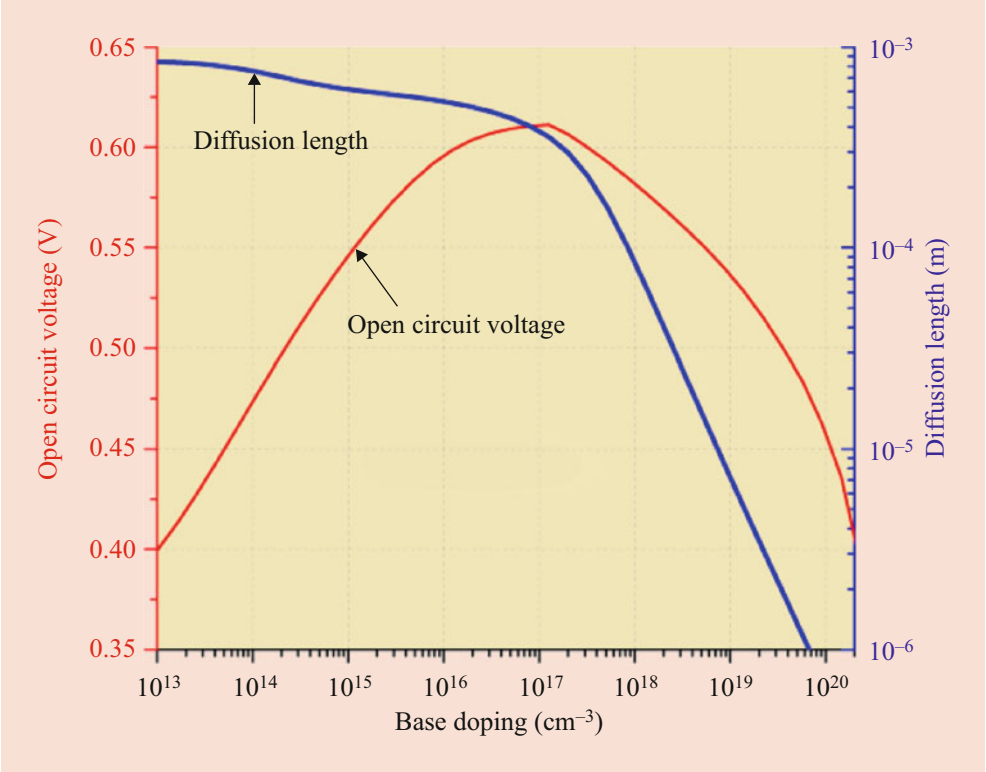

Fig. 19.7 Dependence of the open circuit voltage and carrier diffusion length on the base doping in a homojunction solar cell. (With permission from PVEducation.org)

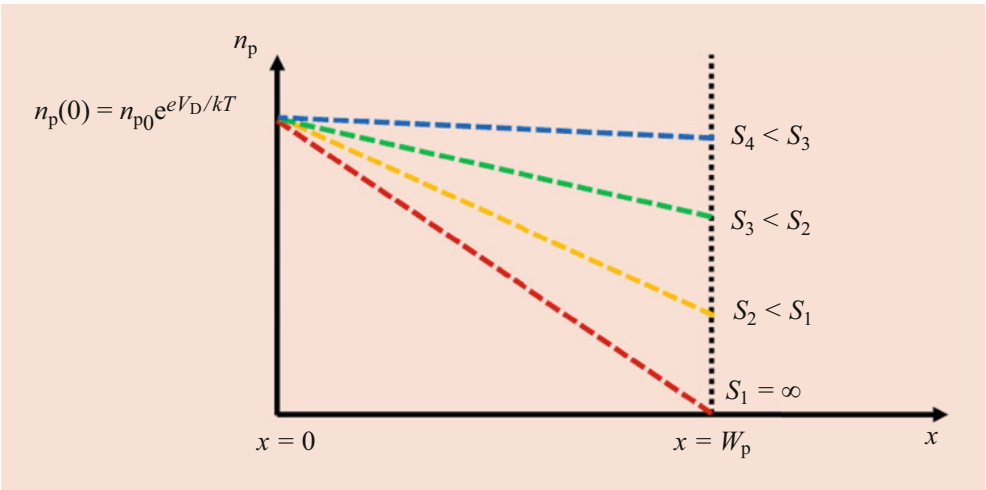

Fig. 19.8 Illustration of the solution of the minority carrier diffusion equation on the base side for different surface recombination velocity values

19.3.2 Photocurrent

The short circuit current density, J_{sc}, is directly related to the photocurrent density, resulting from light absorption in the solar cell, and is equal to this quantity when nonideal effects such as shunt and series resistance are minimized. Maximizing the short circuit current involves two main design factors: one is absorbing the maximum amount of light above the bandgap, and the other is maximizing the collection of light-generated carriers throughout the volume of the cell.

Maximizing the amount of light absorbed involves minimizing reflection both from the metallic front contact grid and from the surface of the cell where light is transmitted. As mentioned earlier, minimizing the front contact grid shading is a design optimization between the spacing and width of the fingers and the spreading resistance of the top layer which

impacts the fill factor of the cell. Minimizing reflectance involves the design of an optimal AR coatings based on the spectral response characteristics of the cell as discussed in Sect. 19.2. In addition to the optical coating, texturing of the front (and back) surfaces is employed in commercial Si solar cells to increase the capture of light into the cell. Finally, either the thickness of the cell has to be sufficiently thick that light is not lost through the back side of the cell due to incomplete absorption, or light trapping techniques have to be employed so that photons make multiple passes through the absorber. The most straightforward approach is simply having an ideal reflecting back side, so that photons make at least two transits of the cell thickness. Texturing of the front surface leads to a high probability of being scattered again back into the cell rather than exiting the front surface. The maximum number of passes is expressed in the classical light trapping limit [8] for the maximum optical path length in the cell, $\langle l \rangle = 4n_s^2 W$, where n_s is the index of refraction of the absorber and W is its thickness. Light trapping is discussed in more detail in Sect. 19.7.3. Reflection and absorption depend on characteristics of sunlight, solar cell optical properties, E_G, and solar cell thickness, so that the optimum design is a nontrivial task.

The second important quantity associated with the short circuit current is the collection probability of the cell for the photoexcited carrier distribution, which is nonuniform and wavelength dependent due the wavelength dependence of the absorption coefficient. The collection probability is illustrated in Fig. 19.9. It represents the probability that an electron generated at some point relative to the SCR will be collected, where in the SCR it is commonly assumed that 100% of the carriers are collected due to the high electric field there.

In terms of the collection probability, the short circuit current can be written as an integral

$$\begin{aligned} J_{sc} &= q\int_0^{W_s} dx G(x) CP(x) \\ &= q\int_0^{W_s} dx \left(\int d\lambda \alpha(\lambda) N_s(\lambda) e^{-\alpha(\lambda)x} \right) CP(x) \end{aligned} \tag{19.35}$$

where Eq. (19.7) has been substituted for the generation rate, and we have integrated over all wavelengths. The upper panel of Fig. 19.9 illustrates the overlap of the generation rate and the collection probability for one wavelength. As mentioned earlier, shorter wavelengths have a generation rate profile close to the top surface, whereas longer wavelength photons result in generation throughout the structure. The dependence of the collection probability with distance relative to the SCR depends on recombination, both bulk and surface recombination, through the solution of the minority carrier diffusion equations, as discussed below. Qualitatively, the effects of low and high bulk recombination, as well as low and high surface recombination (often referred to as the degree of surface *passivation*), are illustrated in Fig. 19.9, where the realization of high short circuit current requires both a high minority carrier lifetime in the bulk and well-passivated front and back surfaces.

A simple case in which analytical expressions can be derived is considering the solution of the minority carrier diffusion equations again on either side of the junction, with a constant G (both in terms of position and wavelength) throughout the device, which would be the case of a light source with a small absorption coefficient relative to the width of the cell. The minority carrier diffusion equations in Eq. (19.25) then have a simple inhomogeneous constant, which, in the limit of the diffusion lengths being much shorter than the widths of the emitter and base regions, gives the analytical form for the current density as the sum of the dark and light currents

$$J_{total} = \left[q\frac{D_n n_i^2}{L_n N_A} + q\frac{D_p n_i^2}{L_p N_D} \right] \left[e^{qV/kT} - 1 \right] - qG\left(L_n + L_p + W\right) \tag{19.36}$$

where W is the width of the SCR, and it has been assumed that all the carriers generated in the SCR are collected. This analytical model gives the simple interpretation that all the carriers generated within a diffusion length of the edge of the SCR on either side of the junction are collected in addition to those generated within the SCR, and the short circuit current is the sum of these three contributions. Qualitatively, this situation corresponds to the collection probability profile illustrated in Fig. 19.9 for the low diffusion length case. As mentioned earlier, in state-of-the-art crystalline Si solar cells, the diffusion length is actually greater than the width of the base region, and passivation of the front and back surfaces plays a critical role in both the photocurrent and dark current.

An important characterization of the photocurrent response of a solar cell is in terms of its *quantum efficiency* (QE), which is defined as the ratio of electron-hole pairs collected to incident photons on the cell within a certain wavelength interval. Once the QE is known, the short circuit current density can be obtained from the integration of the QE with the spectrally resolved incident photon flux

$$J_{sc} = q\int_0^{\infty} d\lambda N_s(\lambda) \, QE(\lambda) \tag{19.37}$$

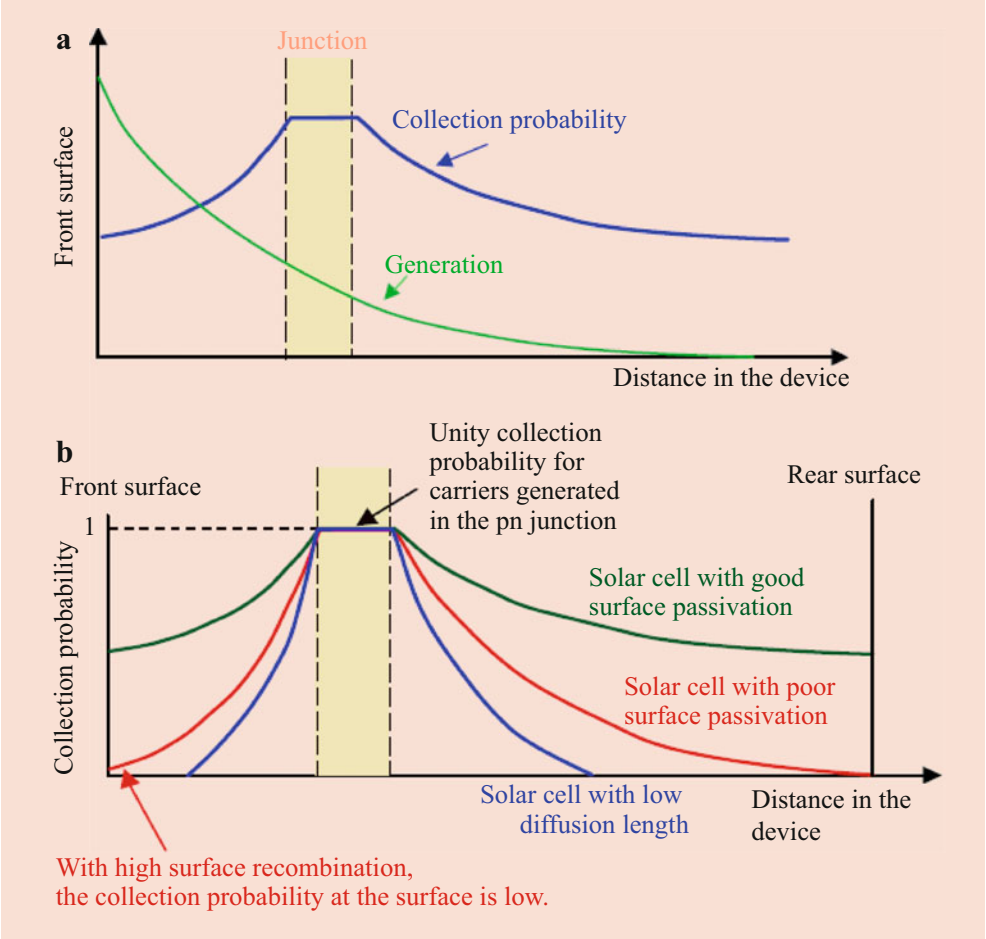

Fig. 19.9 Sketch of the collection probability versus distance in the device. The shaded region represents the SCR where the collection probability is unity. The panel (**a**) compares the collection probability with the generation rate, while the panel (**b**) shows the effect on the collection probability of surface passivation and diffusion length. (With permission from PVEducation.org)

The quantum efficiency provides useful information on the limiting mechanisms controlling the short circuit current. Fig. 19.10 shows a typical QE versus wavelength plot. The ideal quantum efficiency is zero below the bandgap and then jumps to unity above the bandgap and remains constant. In reality, there is reflection from the front surface, which depends on wavelength (in addition to the uniform loss due to the grid pattern, which reduces QE). At long wavelengths, the QE degrades due to the increased absorption depth of photons close to the bandgap energy, where they either are lost due to being absorbed further than a diffusion length from the junction or from not being absorbed due to the cell being too thin. For short wavelengths in the blue region, carriers are absorbed very close to the front surface, where surface recombination exists resulting in loss of collection in a traditional Si cell architecture. Thus, the quantum efficiency of a solar cell is an important characterization used in the optimization of the cell design.

19.3.3 Series Resistance

The simple equivalent circuit model of a solar cell shown in Fig. 19.2 neglected two important parasitic effects that degrade mainly the fill factor defined in Eq. (19.3), that of shunt and series resistance. Figure 19.11 shows the modified equivalent circuit including these two effects modeled simply as linear lumped parameter elements. In general, these resistances are nonlinear, depending on the operating point of the device, but for analysis of the main effects, the linear model is sufficient.

The effect of the shunt resistance is to effectively short the junction, leading to a parallel leakage current component which degrades the ideal diode behavior, with a corresponding degradation of the fill factor. Ideally, the shunt resistance is semi-infinite in a good device. Shunt leakage paths can originate due defects such as dislocations or grain boundaries that bridge SCR leading to a current transport separate from the ideal recombination currents discussed

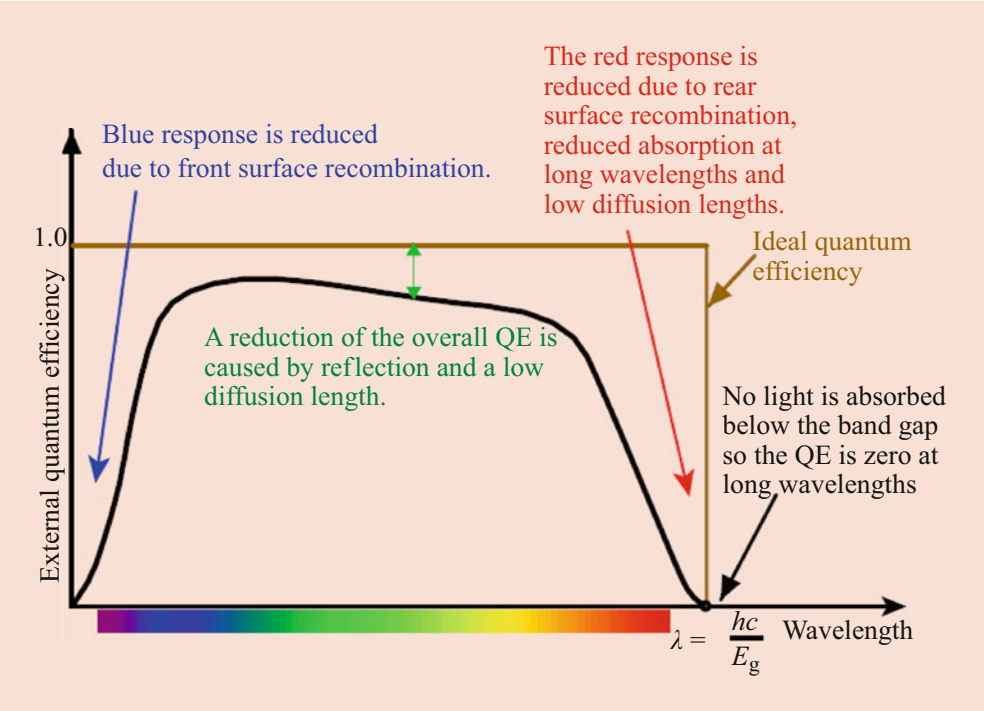

Fig. 19.10 Illustration of the quantum efficiency of a solar cell compared with the ideal quantum efficiency illustrating the various factors affecting its wavelength dependence. (With permission from PVEducation.org)

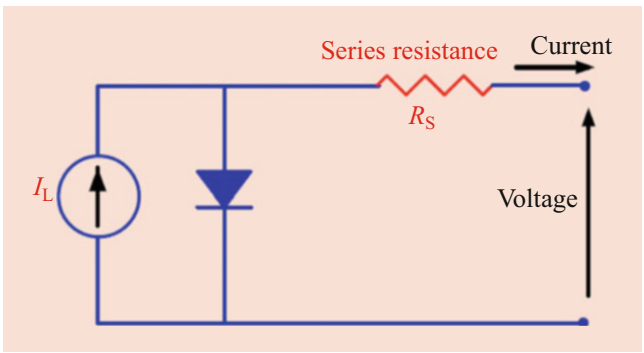

Fig. 19.11 Solar cell equivalent circuit including both shunt (R_{sh}) and series resistance (R_s). (With permission from PVEducation.org)

earlier. It can also originate from leakage around the edges of the cell due to poor isolation and potential metallization problems with the final cell design.

Series resistance can arise from the bulk resistance, contact resistance, the resistance of the metal top grid in the fingers, and importantly the spreading resistance in the emitter as the current spreads laterally to reach the fingers of the top contact metallization, illustrated in Fig. 19.12. Typically, the base resistance is small in comparison to the spreading resistance as the cross-sectional area is quite large. The metal contact resistance between the metal and the semiconductor, defined in terms of the specific contact resistance, is usually well behaved in commercial solar cells as well, and not the main source or resistance loss, while the resistance of the metal itself is not problematic if the finger width is sufficiently large. So the main component of series resistance of concern is usually the emitter spreading resistance, and the design of the finger spacing to minimize the power loss due to this resistance.

The emitter is typically quite thin, and current transport is primarily lateral in this layer. Therefore, it is more usual to talk about the sheet resistance of the emitter in terms of

$$R = \frac{\rho_e L}{tW} = \rho_{sh}\frac{L}{W} \tag{19.38}$$

where ρ_e is the bulk resistivity of the material, t is the thickness, while L and W are the length and width of the material that current is passing through. The quantity ρ_{sh} is the *sheet resistance* in ohms/square (Ω/□).

The problem requires solving the resistive power loss associated with the distributed current flow problem in which the current density is changing in the y direction relative to the grid finger as illustrated in the geometry shown in Fig. 19.13. The incremental power loss in a section dy is given by

$$dP_{loss} = I^2 dR; \quad dR = \rho_{sh} dy/b \tag{19.39}$$

The current flowing into the left finger is zero in the middle and increases linearly as y increases

$$I(y) = Jyb \tag{19.40}$$

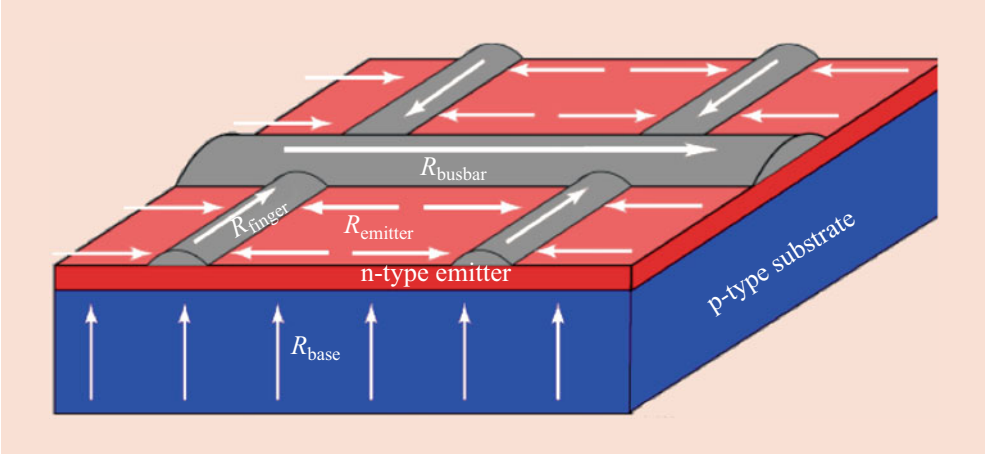

Fig. 19.12 Illustration of the different components of series resistance in a solar cell. (With permission from PVEducation.org)

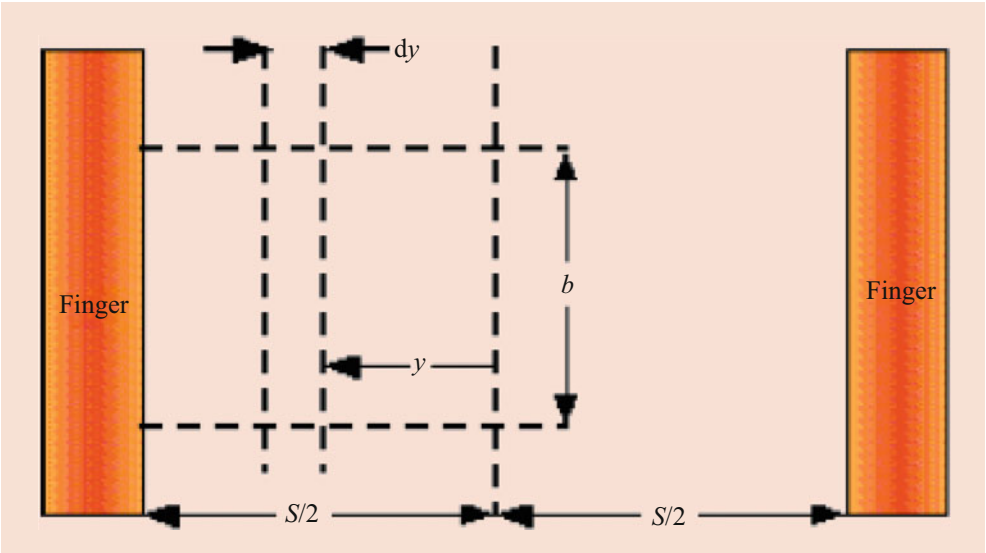

Fig. 19.13 Schematic of the finger geometry for calculating the spreading resistance in the emitter of a photovoltaic device. (With permission from the PVEducation.org)

The total power loss due to the current flowing into the left finger is therefore

$$P_{loss} = \int dRI(y)^2 = \int_0^{S/2} \frac{J^2 b^2 y^2 \rho_{sh} dy}{b} = \frac{J^2 b \rho_{sh} S^3}{24} \quad (19.41)$$

At the maximum power point, the generated power is given by

$$P_{gen} = J_{mp} b \frac{S}{2} V_{mp} \quad (19.42)$$

where J_{mp} and V_{mp} are the current density and voltage at the maximum power operating point of the current-voltage characteristic of Fig. 19.2. Therefore, the fractional power loss is given by

$$P_{\%loss} = \frac{P_{loss}}{P_{gen}} = \frac{\rho_{sh} S^2 J_{mp}}{12 V_{mp}} \quad (19.43)$$

As S increases as well as the sheet resistance, so does the fractional power loss. For ρ_{sh}=40 Ω/□, J_{mp} = 30 mA/cm^2, V_{mp} = 450 mV, $S < 4$ mm is necessary for less than 4% total power loss. The optimal grid design minimizes this power loss while simultaneously minimizing shading loss.

19.3.4 Heterojunction Cells and Carrier Selective Contacts

Here we discuss heterojunction solar cells and the efficiency improvements due to the heterojunction, followed by a more general discussion of carrier selective contacts, of which heterojunctions can be considered a subset.

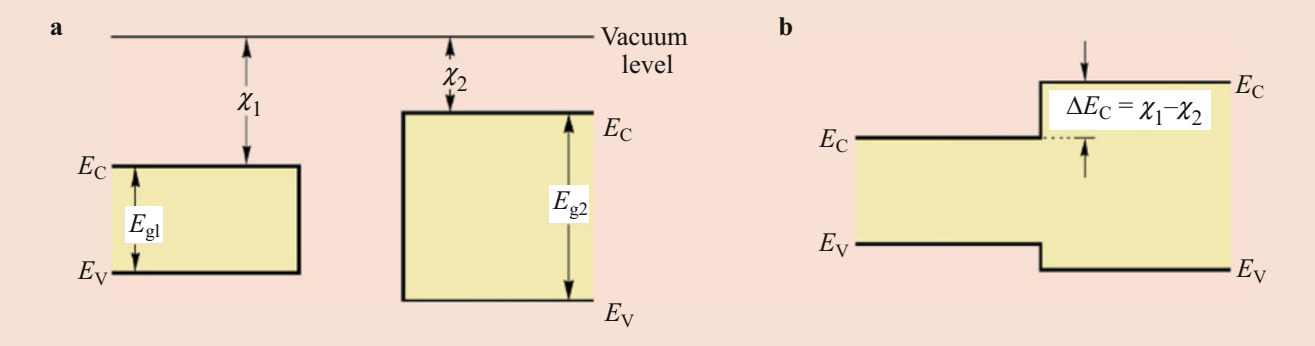

Fig. 19.14 Band diagram of (**a**) two separated semiconductors and (**b**) two different semiconductors in contact. The semiconductors have bandgaps E_{g1} and E_{g2} and electron affinities χ_1 and χ_2

Heterojunctions

The highest efficiency solar cell technologies, either single junction or multijunction, employ heterojunctions between dissimilar semiconductor materials. Figure 19.14 illustrates the ideal band alignment between the two materials based on the electron affinity rule or Anderson model. This model assumes that the vacuum level can be treated as a reference level, which is assumed continuous in forming the heterojunction band diagram. The band offset in the conduction band is then the difference between the two electron affinities, $\chi_1 - \chi_2$. The conduction and valence band alignment can either be such to confine both electrons and holes (type I), either electrons or holes (type II), or staggered such that the VB of one material overlaps the CB of the other (e.g., InAs/GaSb). This model works well for some systems, e.g., InAs/GaSb and Si/Ge. However, deviations from Anderson model generally occur due to interface dipoles which allow the electrostatic potential to change discontinuously. Typically the band offsets are determined experimentally from capacitance voltage, photoemission, photoconductivity, and other techniques.

There are a variety of heterojunction structures in photovoltaics used in high performance devices in various technologies. In the context of conventional wafer-based technologies such as Si and GaAs, these include amorphous Si (a-Si)/c-Si (crystalline Si) heterostructures as a passivating as well as carrier selective contact (discussed in the next section), as well as TCO-based heterostructures, for example, ITO (indium tin oxide)/Si structures and a-Si/c-Si structures. GaAs typically employs $Al_xGa_{1-x}As$ ternary compounds as a heterojunction "window" layer to mitigate surface recombination and serve as a carrier selective contact.

From the standpoint of the ideal diode equation for the dark current as discussed in Sect. 19.3.1, the derivation can be slightly modified to account for the difference in bandgaps, which results in different intrinsic carrier concentrations, n_i, on either side of the junction. The modified reverse saturation current is then given by

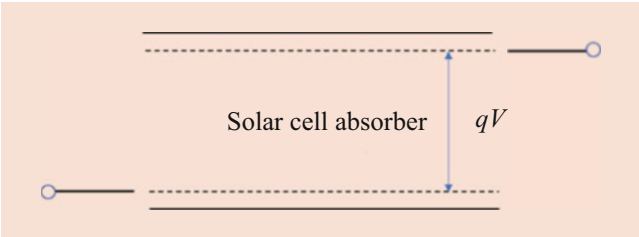

Fig. 19.15 Band diagram of an idealized solar cell as modeled in detailed balance. The solar cell absorber material generates a quasi-Fermi-level separation due to light-generated carriers, which are extracted from the device at the quasi-Fermi level

$$J_0 = q\left(\frac{D_{p1}n_{i1}^2}{X_{p1}N_{D1}} + \frac{D_{n2}n_{i2}^2}{X_{n2}N_{A2}}\right)\left(e^{qV_D/kT} - 1\right) \qquad (19.44)$$

where the parameters have the same definition as Eq. (19.32) except that the intrinsic concentrations are different and significantly reduced in the wider bandgap material by a factor

$$\frac{n_{i1}^2}{n_{i2}^2} = Ae^{-\Delta E_g/kT} \quad \Delta E_g = E_{g1} - E_{g2} \qquad (19.45)$$

Hence, one component of the minority carrier reverse saturation current is exponentially reduced by a factor involving the bandgap difference, leading to an increase in V_{oc}. In general, however, reductions in J_0 may be realized by selective controlling the minority carrier injection, which is the basis of the general topic of carrier selective contacts in the next section.

Thermodynamic and Detailed Balance Definition of Ideal Contacts

The ideal thermodynamic or detailed balance solar cell structure consists of an absorber material with a given quasi-Fermi-level separation, with the light-generated carriers extracted from the material at the quasi-Fermi-level energy as shown in Fig. 19.15 (see Sect. 19.5).

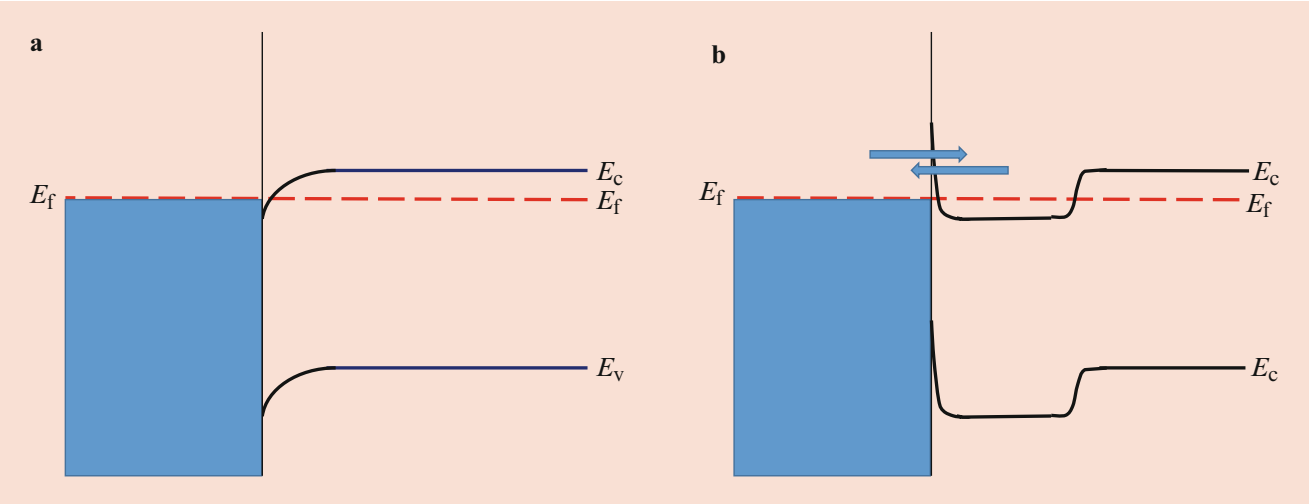

Fig. 19.16 Band structure of an ohmic contact. (**a**) The ideal band diagram of an ohmic contact. (**b**) Practical implementations of an ohmic contact. In all cases, there is a large density of allowed energy states in the contact (a metal), such that there the concentration of minority carrier is low and the quasi-Fermi level is identical to the Fermi level

However, such a structure encounters several practical barriers relating to extracting the light-generated carriers. An ohmic contact (with the band diagram shown in Fig. 19.16) has high recombination for minority carriers, and therefore the carriers are extracted at the Fermi level rather than the quasi-Fermi level. This fact drives the need for a *pn* junction; we need to have two different Fermi levels in the semiconductor, and hence we need the *pn* junction used by the majority of solar cell structures.

The thermodynamically ideal contact for a detailed balance structure was termed a selective carrier contact by Würfel [5]. It consists of a contact which allows one type of carrier to be extracted, with the band diagrams shown in Fig. 19.17, consisting of a Fermi level in the contact material aligned with the quasi-Fermi level in the absorber material. The band structure has a large number of allowed energy states *above* the Fermi level in the contact material, and no allowed energy stated below the Fermi level of the contact material. The band structure diagram shows that a selective carrier structure is the "inverse" of the band structure of an ohmic contact.

Detailed balance and thermodynamic calculations also show that even a carrier selective contact incurs substantial losses in that extracting carriers from a carrier population with an energy given by a quasi-Fermi level loses substantial energy as the quasi-Fermi level is near the bottom of the energy distribution, and hence the higher energy of some carriers is lost. Solar cells which extract carrier at energies above the quasi-Fermi level are generally called hot carrier solar cells, and the contacts to such device are called energy selective contacts. They are discussed in Sect. 19.8.3. Their band structure is similar to a carrier selective contact structure, except that the allowed density of states is a narrow band.

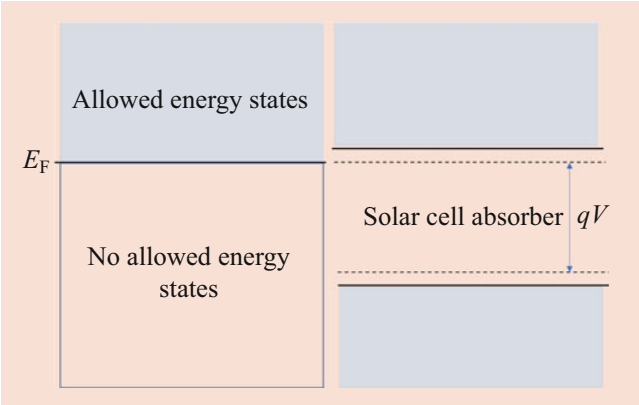

Fig. 19.17 Ideal band structure of a selective carrier contact

Overall, the type of contacts indicated by thermodynamic or detailed balance analyses is shown in Table 19.1.

A substantial optimization in solar cells has centered on minimizing the nonideal recombination associated with an ohmic contact. This involves addressing two features: (1) ensuring that the Fermi level is close to the quasi-Fermi level and (2) minimizing the recombination at the metal-semiconductor interface. Increasing doping, particularly using higher doping near the contacts, is an effective way to minimize both effects. However, high doping itself introduces non-idealities including bandgap narrowing and increased Auger recombination. The introduction of selective carrier contacts, initially through the HIT (heterojunction with thin intrinsic region) and later through a greater variation of structures such as TOPCon, has allowed solar cell efficiencies to more closely approach thermodynamic ideals. The

Table 19.1 Overview of contact approaches

Type of contact	Ideal structure	Energy at which carriers can be extracted or injected	Implementation
Ohmic contact	Fermi level of the metal aligns exactly with Fermi level in semiconductor	Carriers are extracted or injected at the Fermi level; quasi-Fermi level is equal to the Fermi level at the contact	Ohmic metal-semiconductor contacts
Carrier selective contact	Fermi level of the contact aligns with the quasi-Fermi level of the semiconductor	Carriers are extracted or injected at the quasi-Fermi level	Passivated contacts; heterojunction contacts
Energy selective contact	Fermi level of the contact is above the quasi-Fermi level and Fermi level in the material	Carriers are extracted as "hot" carriers – i.e., they have not equilibrated with the lattice or other carriers	Quantum dot contacts; resonant tunneling contacts

next subsection describes the implementation of a selective carrier contact in the constraints of commercial silicon solar cell technologies, and examples of silicon selective contact solar cells.

Silicon-Based Selective Carrier Contact Solar Cells

The ideal implementation of a carrier selective contact consists of a material with a zero density of states below the Fermi level of the contact material, and a large density of states above it. There are several ways in which we can approximate such a band structure. The conceptually simplest way is to use a very wide bandgap semiconductor with quantum well used to adjust the Fermi level to the quasi-Fermi level in the absorber material. This is similar to a hot carrier contact in which the requirement of a narrow band for the density of states is relaxed to a wide band for the density of states above the lowest energy level, and hence quantum wells can be used instead of quantum dots.

In practice, however, particularly for large area silicon and thin film solar cells, a quantum well contact is not readily commercially feasible. A far simpler implementation is to use a very thin wide bandgap layer. The bandgap of the material needs to be wide enough such that there are theoretically no allowed states near the silicon band edge as shown in Fig. 19.18a. However, adjusting the Fermi level of this wideband material by doping is typically not useful, as the introduction of allowed energy levels from the dopants introduces energy states, which increase recombination. Further, because of the difficulty in doping wide bandgap materials or oxides, even with high doping, such materials are unlikely to have sufficient conductivity to avoid large resistive losses given the large currents from a solar cell. Instead of doping, we adjust the Fermi level in wide bandgap region adjacent to the solar cell by putting a doped wide bandgap semiconductor on top and using band offsets to achieve large band bending. The separation of an ideal selective carrier into two layers introduces the need to examine the transport, usually by tunneling and/or thermionic emission across the thin wide bandgap region.

There are several solar cell architectures which meet the above requirements. One group of solar cell structures uses silicon heterojunctions, initially developed using amorphous Si layers on a crystalline Si solar cell. These approaches are often called HIT solar cells (heterojunction with intrinsic thin layers) or SHJ (silicon heterojunctions). The HIT structure is shown in Fig. 19.20. It achieved an efficiency of 24.7% in 2014 [9], reaching the previously long-standing silicon efficiency record from the *pn* junction-based PERL solar cell. Since then numerous improvements have allowed solar cells based on silicon heterojunctions to reach 26.6% [10] in an interdigitated back contact structure (Fig. 19.20). Several companies have large-scale commercial production of HIT solar cells, including Panasonic and Tesla Solar. Key challenges for broader adoption of SHJ solar cell relate to the consistency in large-scale manufacturing and more expensive metallization for these solar cells. Metal screen printing for HIT solar cell uses different pastes and processing since SHJ require low temperature processes, and cannot use the high temperature sintering steps in conventional solar cells. A variety of other metallization processes are used to address these issues including using wires (SmartWire), copper plating, or metal stencils.

Overall, a selective carrier contact for a commercial solar cell generally consists of several features (Fig. 19.19): (1) a wide bandgap material often called a membrane with (a) sufficiently low interface defects where the defects have a minimal impact taking into account the band bending at the Si surface and (b) thin enough to support high tunneling/thermionic emission currents; (2) layers on the surface of the wide bandgap to adjust the Fermi level and to support lateral transport to the contacts; and (3) an approach in the silicon absorber to reduce the impact of interface defects.

Another selective contact technology is the TOPCon technology [11]. It is used as a rear contact approach for solar cells in which the emitter already closely approaches the ideal structure shown in Fig. 19.21. In the TOPCon structure, SiO_2 is used as the membrane wide bandgap region. The Fermi level is adjusted by a polysilicon doped layer on the SiO_2, and reducing the impact of interface states is accom-

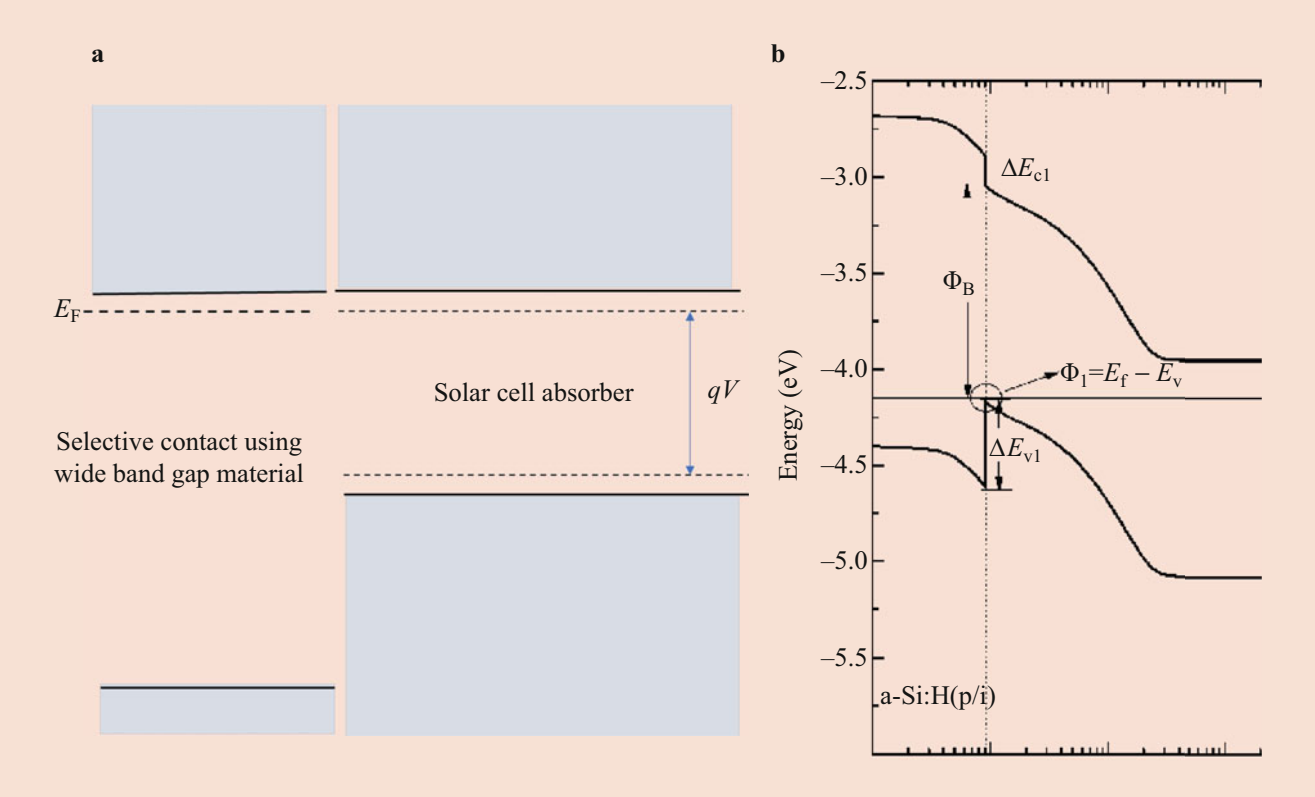

Fig. 19.18 Idealized selective carrier contact with a wide bandgap material

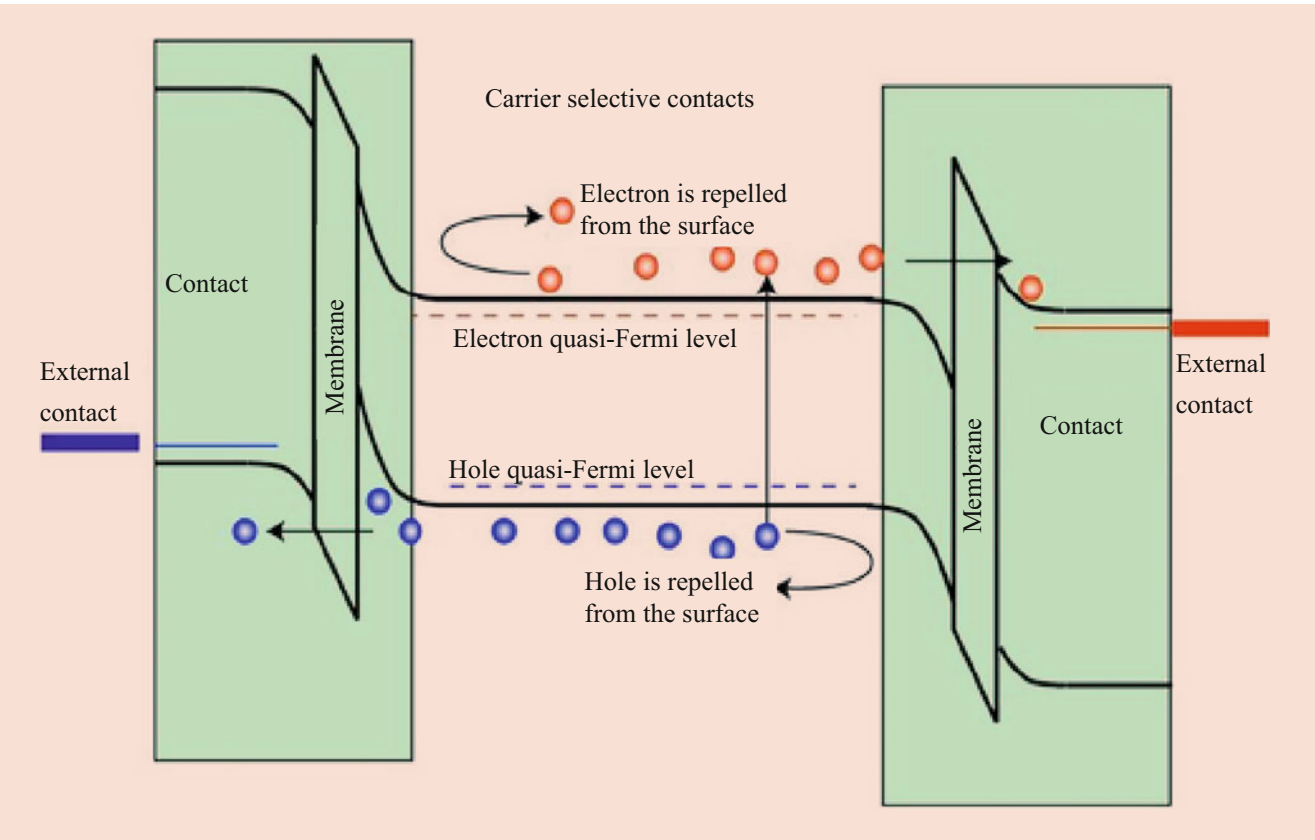

Fig. 19.19 Components of a carrier selective contact solar cell

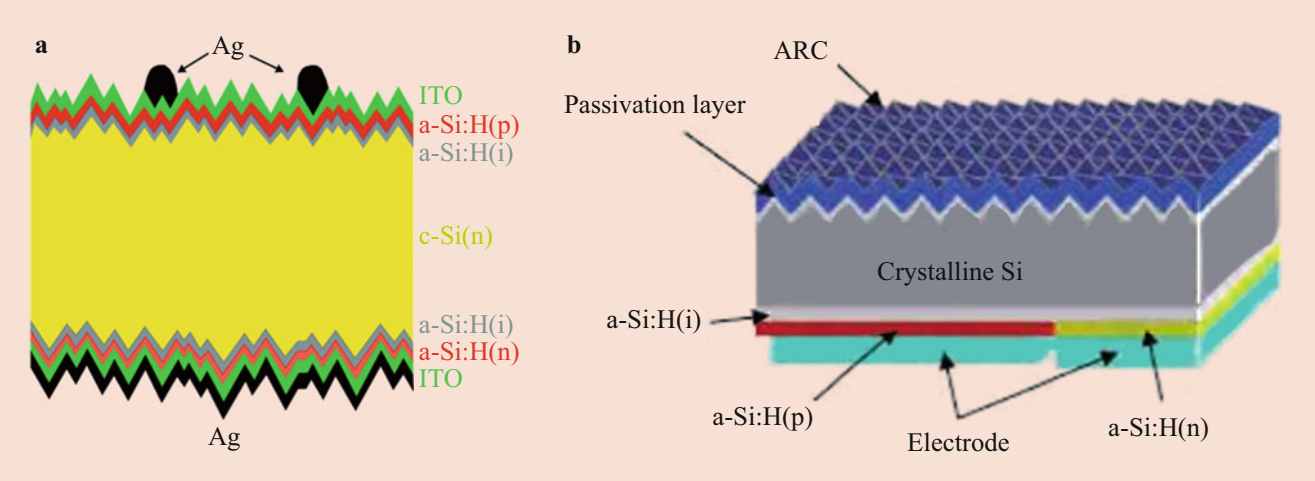

Fig. 19.20 (**a**) HIT solar cell schematic; (**b**) IBC HIT solar cell

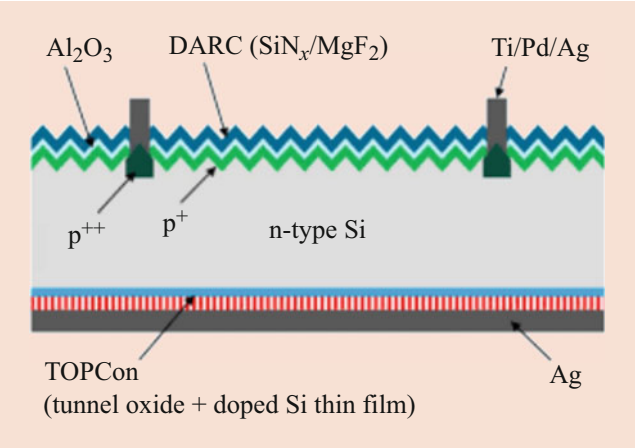

Fig. 19.21 Schematic of a TOPCon solar cell. (With permission from [11])

plished by a thin doped layer in the silicon (which is diffused through the oxide). TOPCon solar cells have achieved 25.7% efficiency [12].

19.4 Performance Comparison of Single Junction Technologies

In the following, we compare the performance of different single junction technologies, including Si, the III–V materials, II–VI and chalcogenide materials, and finally organic and perovskite-based cells. All are referenced to the conversion efficiency versus time of the various technologies, as discussed below.

19.4.1 Performance Limits of Si- and GaAs-Based Technologies

A primary performance metric for solar cells is the solar to electrical energy conversion efficiency, defined earlier by Eq. (19.3). The National Renewable Energy Laboratory (NREL) publishes annually a comparison of the efficiencies of all solar cell technologies versus time shown in Fig. 19.22. Silicon solar cell technology dominates 95% of the current world photovoltaic market, through both single crystal and multi-crystalline Si technologies [13], as shown by the various blue curves in Fig. 19.22. The current high efficiency record (as of 2020) reported for single junction Si device technology under 1 sun illumination to date is 26.7%, based on a heterojunction HIT structure (see Sect. 19.3.4) using a crystalline Si substrate with thin layers of amorphous Si (a-Si), which forms a heterojunction due to the larger bandgap of a-Si (~1.7 eV) [10]. This cell record was demonstrated on a large area device, with an interdigitated back-side contact as shown in Fig. 19.20.

The highest efficiency for any single junction technology was reported by Alta Devices for a heterojunction AlGaAs/-GaAs single crystal solar cells where they achieved 28.8%, as shown by the purple curves in Fig. 19.22 (see Ref. [14] for discussion). III–V semiconductor solar cells are normally too expensive for terrestrial flat plate solar applications due to the costs of the substrate materials. However, III–V-based cells, as well as their multijunction realizations (shown in purple below), are standard technologies for space applications, where radiation tolerance and efficiency versus weight are the main performance drivers.

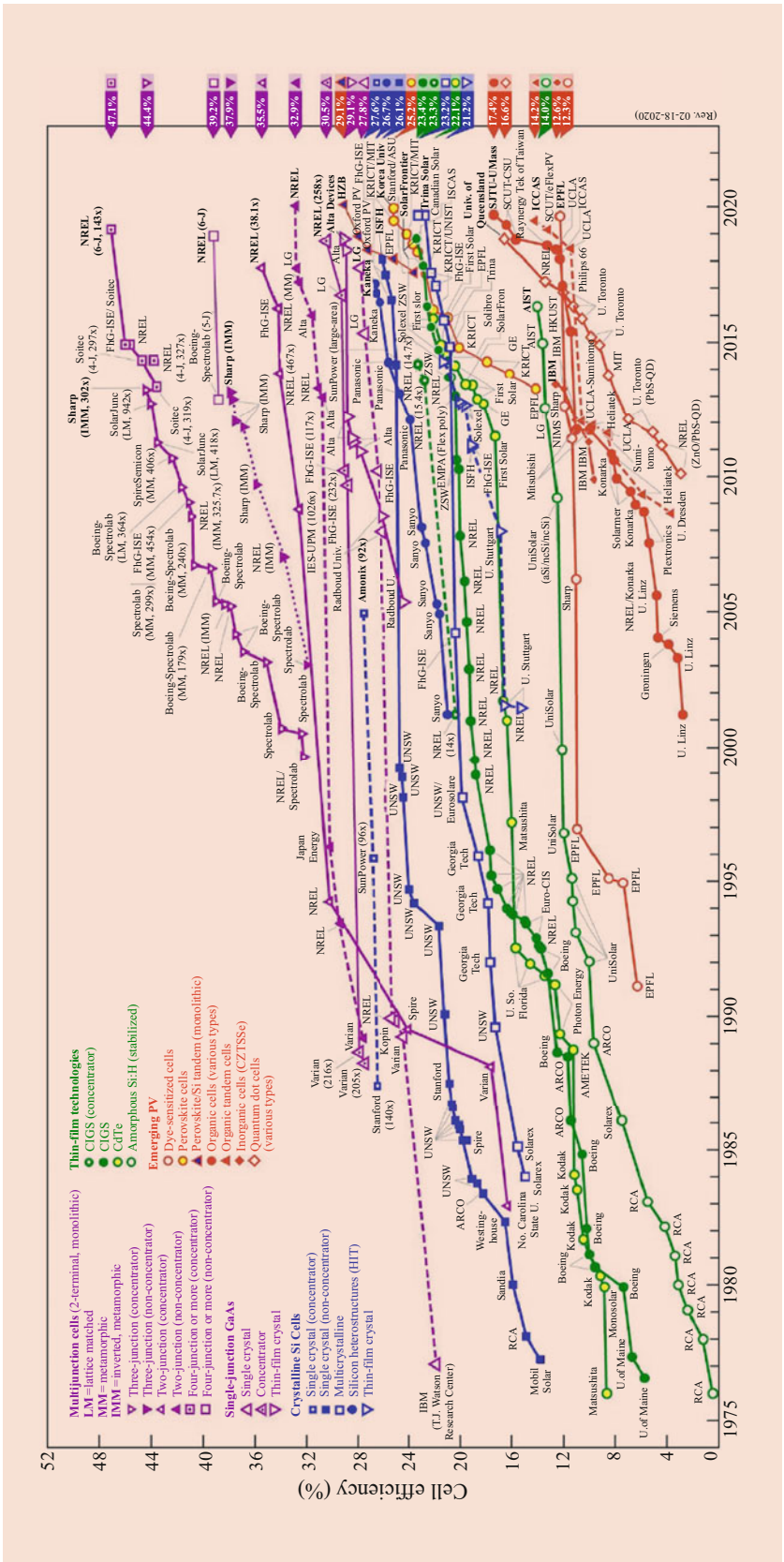

Fig. 19.22 Measured solar cell efficiency records for various technologies versus time (NREL https://www.nrel.gov/pv/). (This plot is courtesy of the National Renewable Energy Laboratory, Golden, CO)

19.4.2 Thin Film Technology

The Si and III–V technologies described in the previous section are mainly wafer based, which is a major contribution to their cost in terms of materials. Thin film solar cells, in contrast, are deposited using thin film technology onto a low-cost substrate material such as metal or glass. Since the quality (as characterized by its minority carrier lifetime and surface recombination velocity) of the deposited material is inferior to that of single crystal materials, thin film cells typically have lower efficiency but lower fabrication and material costs, thus achieving lower $/W cost, the other main metric of solar cell technology. Amorphous Si (a-Si) thin film solar was the dominant thin film technology several decades ago but has since been supplanted by II–VI CdTe heterostructure technology. A schematic cross section of a CdTe cell is illustrated in Fig. 19.23. Typically a heterostructure is used, with a wider bandgap "window" layer (here CdS with a bandgap of 2.5 eV), while CdTe has a bandgap of 1.32 eV. The structure is an inverted structure in which glass is used as the supporting substrate, followed by a thin transparent conducting oxide as the front contact through which light enters the cell. The wider bandgap CdS layer is deposited first followed by the polycrystalline CdTe layer (typically a few microns thick), and finally rear contacts. As shown in Fig. 19.22 by the green sets of data, CdTe cells have demonstrated over 21% performance by First Solar [15], and this is the basis for a number of large (>200 MW) utility-scale solar installations worldwide. Chalcogenide-based materials such as CIGS ($CuInGaSe_2$) have demonstrated even higher efficiencies >23% [16] and are competing for market share.

19.4.3 Organic Solar Cells

Organic solar cells are basically thin film solar cells based on organic semiconductor materials rather than inorganic semiconductors. In analogy to the energy band diagram of Fig. 19.1, organic materials are defined by their HOMO (highest occupied molecular orbital) and LUMO (lowest unoccupied molecular orbital) levels, which play the same role as the valence and conduction bands in inorganic semiconductors, respectively. A heterojunction is formed due to the lineup of the HOMO/LUMO levels of the two different materials (called donor and acceptor materials), rather than through doping in a *pn* junction. Excitonic effects play a strong role in organic materials; photoexcitation of an electron from a filled HOMO level to an empty LUMO level creates a strongly bound exciton, which diffuses as a bound (neutral) state to the heterointerface, where it dissociates at the barrier into separate free electrons and holes on either side of the heterojunction, which are then collected at the contacts giving rise to a photocurrent. Typically the lifetime of the exciton is quite short, leading to short diffusion lengths,

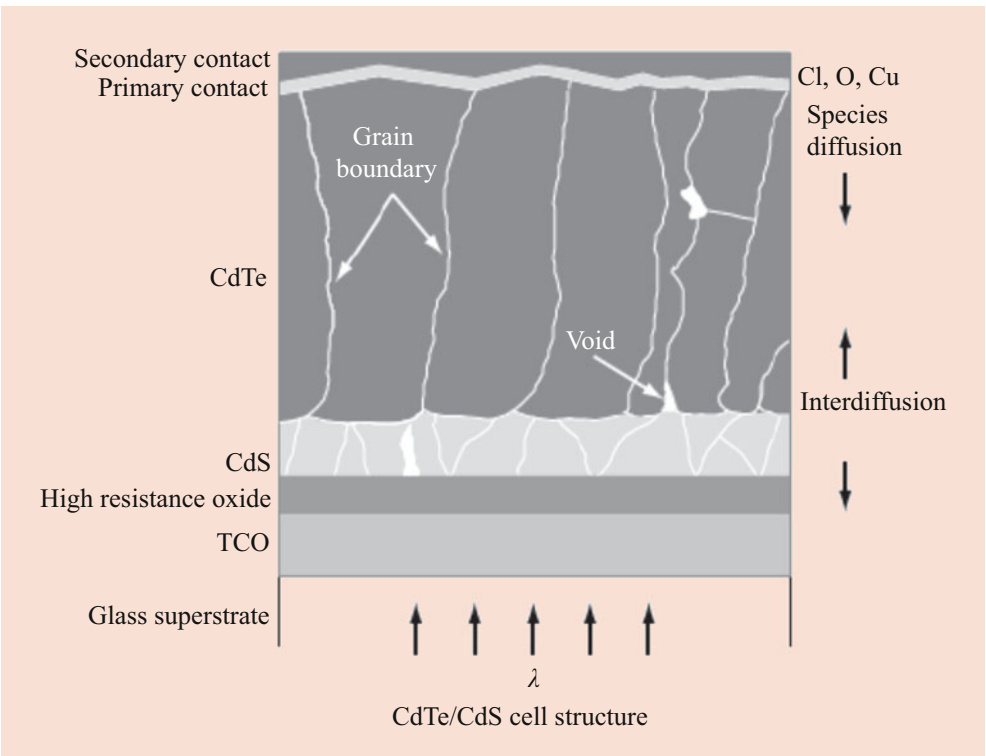

Fig. 19.23 Schematic of the structure of a CdTe-based thin film solar cell

and hence problems with charge collection. To circumvent this diffusion limitation, *blended heterostructures* with the donor and accepter materials interdiffused into a random network are employed, which provide better charge collection and short circuit current. A conventional organic solar cell includes P3HT (poly(3-hexylthiophene)), which acts as a donor material, and PCBM (6,6-phenyl-C61 butyric acid methyl ester), which acts as an acceptor material [17]. While efficiencies are generally lower than inorganic thin film approaches, the fabrication process for organic is much less expensive; organic layers can be sprayed or spun on, hence not requiring vacuum deposition or high temperature processing. Recent high performance organic cells have increasingly used more conventional thin film processing, however [18]. The improvement in efficiency with time of conventional organic cells is shown by the solid red circuits in Fig. 19.22 and tandem (discussed in Sect. 19.6) organic cells by the red triangles.

While research work on commercial ventures in niche markets continues on all organic photovoltaics, including incorporation of advanced concept and nanotechnology-inspired approaches discussed in more detail in Sect. 19.7, remarkable advances in performance have been achieved over the past decade on cells fabricated from hybrid organic-inorganic perovskite materials. These hybrid perovskite materials have the general perovskite crystal structure ABX_3, most commonly methylammonium lead trihalide, $CH_3NH_3PbX_3$, where A is the organic methylammonium, B is Pb, and X is a halogen (I, Br, or Cl) [19]. The bandgap ranges from 1.55 eV to 2.3 eV depending on the halide, where $CH_3NH_3PbI_3$ corresponds to the lower value. This bandgap is well suited for terrestrial photovoltaics in terms of its maximum theoretical efficiency discussed in the next section. Perhaps more importantly, the transport properties of the hybrid perovskites are superior to those of the typical organic materials discussed in the preceding paragraph, with electron and hole mobilities comparable to inorganic semiconductors, and diffusion lengths on the order of microns. Excitonic effects are relatively weak as well. The early high performance results report for perovskite solar cells was based on the nanostructured dye-sensitized solar cell architecture [20], discussed in Sect. 19.7.2, in which the hybrid perovskite is infused into a mesoporous wide bandgap TiO_2 structure which acts as an electron acceptor from the perovskite, while holes are extracted in an electrolytic liquid cell structure. This efficiency was greatly improved by replacing the liquid electrolyte with a solid organic hole transport layer (spiro-MeOTAD) [21], which is the basis of the current high efficiency cells shown in Fig. 19.22. In a further breakthrough leading to high efficiency cells, the Cambridge group further demonstrated that high performance devices may be fabricated in a planar structure in which $CH_3NH_3PbI_3$ is essentially a polycrystalline semiconductor [22], resembling an organic thin film solar cell. As seen in Fig. 19.22, the performance of perovskite solar cells has one of the steepest slopes of any technology over a very short time period, reaching a record as of today of 25.2% at the Korea Research Institute of Chemical Technology (KRICT)/MIT, surpassing that of thin film inorganic technologies such as CdTe and CIGS. The advantage of perovskite technology is the low manufacturing cost, similar to those of organic and thin film processing, where solvent spin coating and vapor deposition are the two main synthesis methods. The main barrier to commercialization presently is issues related to the long-term stability, where degradation occurs due to the sensitivity of the perovskite to water vapor, which can occur over a matter of hours or days. Different approaches to encapsulation and improved materials processing ameliorate these problems, but long-term field testing and accelerated life testing are necessary to assure the longtime reliability of the technology (e.g., commercial Si solar modules are guaranteed for lifetimes in excess of 20 years).

19.5 Efficiency Limits for Photovoltaic Converter

The record solar to electrical conversion efficiencies shown in Fig. 19.22 are all monotonically increasing with time for different technologies, albeit at different rates, and to date, less than 50%. Thermodynamics provides a guide to what the maximum conversion efficiency of a solar converter can approach. For example, the classical Carnot efficiency, $\eta_c = 1 - T_a/T_s$, representing a reversible engine working between the temperature of the Earth, T_a, and that of the sun, T_s, would predict efficiencies close to 95%. However, the Carnot efficiency assumes infinitesimally small amounts of work performed with no entropy production (inherent in the reversible assumption), which does not model a practical converter. de Vos has surveyed various thermodynamic engines for solar energy conversion [23], which have been reviewed by Green (Chap. 3, [2]). Considering the entropy production associated with blackbody radiation and absorption, a more realistic value closer to 85.4% is obtained.

It is clear that there is a substantial gap between the present operating limits of solar cells and their thermodynamic potential, which has driven considerable research on overcoming fundamental barriers to efficiency. In the following, we review the limits of efficiency including the constraints on current technology through an idealized analysis based on the concept of detailed balance, and how to circumvent the assumptions inherent in the derivation of a single gap absorber to reach the potential limits of efficiency.

19.5.1 Shockley-Queisser Limit

Shockley and Queisser's (SQ) analysis [24] of the limits of performance of photovoltaic devices, independent from their material parameters other than their energy gap, is the most well-cited work on this topic, although other such analyses appeared around the same time. The approach is based on the thermodynamic hypothesis of *detailed balance* and considers the only losses from the cell treated as an ideal blackbody absorber/emitter taking into account the chemical potential difference in the absorber due to absorption and external voltage. The idealized description assumes the following: (1) complete collection of all the photons incident on the absorber; (2) radiative recombination only; (3) one bandgap; (4) absorption across the bandgap in which one photon generates one electron-hole pair; (5) constant temperature in which the carrier temperature is equal to the lattice and ambient temperature; and (6) steady state, close to equilibrium.

The current density may be written as the sum of three terms, the first representing the incident photons absorbed above the bandgap of the semiconductor from direct blackbody radiation at the temperature of the sun given by Eq. (19.4), the second the diffuse blackbody radiation collected outside the incident cone of the direct radiation, and finally the third term the blackbody radiation from the solar cell (Eq. (19.4) modified by the quasi-Fermi energy splitting of the absorber equated to the external voltage)

$$J = qg\left[\left(fC\int_{E_G}^{\infty}\frac{E^2\mathrm{d}E}{\exp\left(\frac{E}{kT_{sun}}\right)-1}+(1-fC)\int_{E_G}^{\infty}\frac{E^2\mathrm{d}E}{\exp\left(\frac{E}{kT}\right)-1}\right)-\int_{E_G}^{\infty}\frac{E^2\mathrm{d}E}{\exp\left(\frac{E-qV}{kT}\right)-1}\right] \tag{19.46}$$

with

$$g=\frac{2\pi}{h^3c^2}\quad f=\left(\frac{R_{sun}}{D_{sun}}\right)^2 \tag{19.47}$$

Here C is the concentration factor, E_g is the material bandgap, and V is the voltage across the cell. If a solar spectrum other than the ideal blackbody spectrum is used, then the first term is simply replaced by the integral of the photon flux above the bandgap.

In Eq. (19.46), the "dark" current discussed in the previous section is only due to blackbody radiation from the semiconductor absorber, which in effect is due to radiative recombination within the semiconductor generating photons above the bandgap. The power density delivered by the cell is the product of $J(V)V$, which has a maximum power point

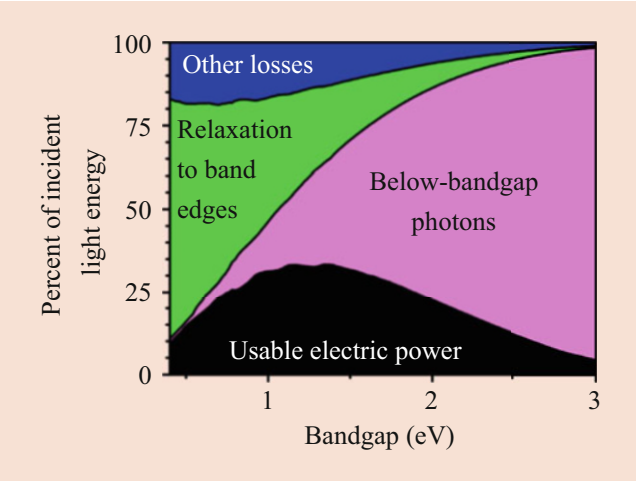

Fig. 19.24 The Shockley-Queisser efficiency limit (black curve) for a single gap absorber versus bandgap (AM1.5 solar spectrum). Also shown are the losses due to thermalization (green), transparency (pink), and entropy/heat loss (blue). (Source: Wikimedia Commons)

corresponding to the maximum conversion efficiency. The calculated results are shown in Fig. 19.24, where the black curve is the calculated efficiency versus bandgap for an AM1.5 terrestrial solar spectrum (hence the multiple maxima due to spectral features). The maximum efficiency without concentration is around 33.7% corresponding to maxima at 1.1 and 1.4 eV (conveniently close to Si and GaAs, respectively), while the effect of concentration is to increase the efficiency. The rest of Fig. 19.24 illustrates the principal losses compared to 100% efficiency. The main losses include loss of photons with energy below the bandgap (transparency) and loss of the excess energy of the photon above the bandgap (thermalization) in terms of energy relaxation of photoexcited carriers back to the band edges, with thermalization being the main loss for small bandgap materials and optical transparency the main loss for high bandgaps. Additionally there are other losses including unavoidable heat loss to the surroundings and irreversible entropy generation [25].

19.5.2 Overcoming the Shockley-Queisser Limit

The detailed balance efficiency versus bandgap shown in Fig. 19.24 has a number of assumptions built-in that may be circumvented in order to exceed the single gap SQ limit. Here we discuss some of those assumptions and strategies for avoiding them to overcome the single gap limitations.

Broadband Solar Spectrum: As discussed in Sect. 19.2.1, the solar spectrum is a broadband in nature as described by Planck's law, which leads to particular shape of the maximum

efficiency curve versus bandgap, representing a trade-off in losses between transparency and thermalization. If the input spectrum were monochromatic, for example, then the optimum bandgap would match the photon energy of such a source, and the efficiency would theoretically approach the thermodynamic limit since both transparency and thermalization would be eliminated. Transforming the solar spectrum to a narrower spectrum would therefore circumvent one of the assumptions in Eq. (19.46), and attempts at up/down conversion of portions of the solar spectrum through phosphors or two-photon absorption/emission have been pursued.

OneElectron-hole PairCreated Per Photon Absorbed: The assumption in Eq. (19.46) is that one EHP is excited per photon. However, if the excess energy of the electron or hole above their respective band edges is more than twice the bandgap, a second EHP may be created through the process of impact ionization, where the excess kinetic energy is transferred to creation of the second EHP. This process reduces the thermalization loss by converting excess photon energy into increased photocurrent. Kolodinski et al. considered carrier multiplication in the SQ limit of conventional Si solar cells [26]; however the effect was negligible due to restrictions on the threshold energy for impact ionization to occur due to momentum conservation in bulk crystals. In more recent years, strong multiplication effects have been measured in nanostructured systems such as quantum dots and nanowires in which momentum conservation is relaxed [27], discussed in more detail in Sect. 19.8.2. There the effect is referred to as multiexciton generation (MEG), as optical absorption occurs primarily through excitonic states in strongly confined systems like quantum dots and nanocrystals.

The Extracted Carrier Energies Correspond to the Band Edges: Ross and Nozik proposed the concept of hot carrier solar cells in the early 1980s [28], where electrons and holes are not collected at the band edges (and the voltage determined by the bandgap), but through energy selective contacts above and below the conduction and valence band edges, respectively. The operating voltage of the device would then be determined by energy separation of these energy selective contacts, while the photocurrent would be determined by the bandgap itself, thus circumventing the SQ limit. This concept requires that the absorber material has a low carrier energy loss rate to the lattice, so that the carriers can maintain sufficient average kinetic energy to be extracted through the energy selective contacts. Würfel and coworkers further considered the effect of impact ionization and carrier multiplication on the performance [29, 30]. Recent results are discussed in more detail later in Sect. 19.8.3.

Single Bandgap Absorber: The SQ model only considers a single bandgap material, but by the mid-1950s, it was already recognized that *multijunction* or *tandem* solar cells, discussed in more detail below, were capable of efficiencies above that of single gap devices. Tandem cells are most commonly fabricated as a stack of series connected junction cells, with the widest bandgap at the top, where it absorbs the blue portion of the solar spectrum, the next largest gap below, and so forth until the bottom cell which has the smallest bandgap. As shown in Fig. 19.22, III–V compound tandem cells demonstrate the highest efficiencies of any solar cell technology [31], with the record to date in excess of 47.1% in a six-junction metamorphic structure [32], compared to the single gap SQ limit of 33%.

19.6 Multijunction Solar Cells

Of the abovementioned approaches to circumvent the SQ limit, by far the most successful has been the demonstration and commercial development of multijunction or tandem solar cells. Such cells are the highest efficiency technology presently, particularly at high concentration. In tandem solar technology, multiple bandgap junction devices are connected together or simply grown sequentially on a substrate, where the multiple bandgaps reduce the thermalization loss and transparency issues of a single bandgap solar cell, as discussed in more detail below. The highest efficiency tandem devices are single crystal III–V materials grown epitaxially on top of one another, starting with the lowest bandgap material (which often is a Ge substrate which is lattice matched to GaAs) and ending with the highest bandgap, in terms of the direction of the incident radiation. In this way, the short wavelength light is absorbed in the top wide bandgap material, and the longer wavelength light is absorbed by subsequent layers. The cells are typically connected together in series with tunnel junctions, such that, overall, the current is the same through all the cells and the overall cell voltage is the sum of the voltages of the individual cells. The cost of the substrates and high-quality epitaxial growth (using, e.g., molecular beam epitaxy (MBE) or metal organic chemical vapor deposition (MOCVD)) makes the cost per cell quite high. The high cost of these devices is compensated for by using them in an optical concentrator (where the light intensity is 200× to 400× higher than typical sunlight), such that only very small areas are needed. The optical systems must track the sun, and these large systems are suited primarily for utility-scale applications. Three junction cells based on Ge/GaAs/GaInP or similar combinations have exceeded 40% efficiency as shown by the purple set of curves in Fig. 19.22, and the record as of the time of this writing is 47.1% from NREL in a six-junction structure, which is well in excess of the SQ limit for a single junction.

The detailed balance approach given by Eq. (19.46) can be generalized to consider multiple junctions, each with its own detailed balance equation, and with a modified spectrum according to the number of cells above or below (due to reabsorption of the emitted light) the particular junction in question. Consider an n-layer stack, in which cells are arranged in order of decreasing bandgap, with the highest bandgap closest to the top surface where radiation is incident. Consider the *i*th cell in the n-layer stack. The net absorption in this layer is due to absorption from incident light through upper layers plus re-emitted light from layers above and below. The current in the *i*th cell is then given by a generalization of the detailed balance equation for a single junction, Eq. (19.46), as.

$$J_i = qN = qg\left[\left(fC\int_{E_{G_i}}^{E_{G_{i+1}}}\frac{E^2\mathrm{d}E}{\exp\left(\frac{E}{kT_{\mathrm{sun}}}\right)-1}+(1-fC)\int_{E_{G_i}}^{E_{G_{i+1}}}\frac{E^2\mathrm{d}E}{\exp\left(\frac{E}{kT_{\mathrm{a}}}\right)-1}\right)-\int_{E_{G_i}}^{\infty}\frac{E^2\mathrm{d}E}{\exp\left(\frac{E-qV_i}{kT_{\mathrm{a}}}\right)-1}\right] + \underbrace{qg\int_{E_{G_{i+1}}}^{\infty}\frac{E^2\mathrm{d}E}{\exp\left(\frac{E-qV_{i-1}}{kT_{\mathrm{a}}}\right)-1}}_{\text{Reabsorbed photons emitted from cell above}} + \underbrace{qg\int_{E_{G_i}}^{\infty}\frac{E^2\mathrm{d}E}{\exp\left(\frac{E-qV_{i+1}}{kT_{\mathrm{a}}}\right)-1}}_{\text{Reabsorbed photons emitted from cell below}} \tag{19.48}$$

where the first two terms represent the light absorbed in the range of photon energies between the bandgap of the layer and the bandgap of the layer above due to both direct and diffuse light, the third term is the radiation emitted from this cell with V_i the voltage across the cell, while the last two terms represent absorption due to reabsorbed photons emitted from the cells above and below, respectively. Eq. (19.48) is then used for all the cells in the stack, in which the upper limits on the top cell go to infinity.

In the usual architecture, the cells are grown epitaxially on top of one another, which imposes stringent constraints in terms of lattice matching of the layers to minimize defect formation due to strain. The current then has to be the same in all the cells as they are series connected

$$J_1 = J_2 = \ldots J_n \tag{19.49}$$

Therefore, the voltage operating point of each of the cells described by Eq. (19.48) has to adjust such that the currents are the same, and the resulting operating voltage is the sum of the voltages of the individual cells when series connected.

The results of this calculation for maximum efficiency of different numbers of bandgaps for normal, low, and high concentration are shown in Fig. 19.25. As can be seen, concentration provides a significant improvement in performance for high number of junctions, which can be explained simplistically in terms of Eq. (19.3) for the open circuit voltage increase with photocurrent (proportional to concentration) and having junctions in series where the effect is additive, multiplying the concentration effect. For maximum concentration (set by étendue limits to 46,050X), one can approach the thermodynamic limit with an arbitrarily large number of junctions, where the thermodynamic limit for a solar energy converter is above 85%, as discussed in the preceding section.

As discussed earlier, commercial tandem cells are grown in series using epitaxial material growth technology, which is generally quite expensive compared to conventional Si solar cell manufacturing and has many material challenges to both optimize the bandgaps and have lattice-matched materials for low defect growth. Si-based tandems leverage the low cost of Si substrates in commercial technology today, with the efficiency advantages of a top cell grown on the underlying Si platform. Fig. 19.26 shows the calculated detailed balance efficiency versus bandgap for a two-terminal (2T), series constrained, top and bottom cell, which is peaked in a narrow bandgap range around 1.7 eV at 46%. A key challenge in tandems is that in series connected tandems, the maximum efficiency is achieved only for a narrow range of bandgaps as shown for a two-terminal structure, giving rise to the search for a 1.7 eV material that can be grown or deposited onto a silicon solar cell without an added substrate and yields stable, high performance. Realizing this bandgap with a material lattice matched to Si is quite challenging. What is also plotted in Fig. 19.26 is the efficiency versus bandgap when the 2T series constraint is relaxed. The dependence on bandgap is much weaker and shifted slightly higher to 1.9 eV, meaning that a range of bandgap options become available when current matching between the two cells is relaxed.

The main approaches to realizing 2J tandems in Si have been through III–V, II–VI, and perovskite top cells. The highest efficiencies have been reported by several groups for III–V cells bonded onto Si in a 4T configuration, with over 32% reported for 2J cells and 35.9% for 3J by EPFL/NREL [33]. However, the 4T approach generally requires a full III–V cell to be fabricated separately and bonded onto a Si substrate, which is most likely not cost competitive in terms

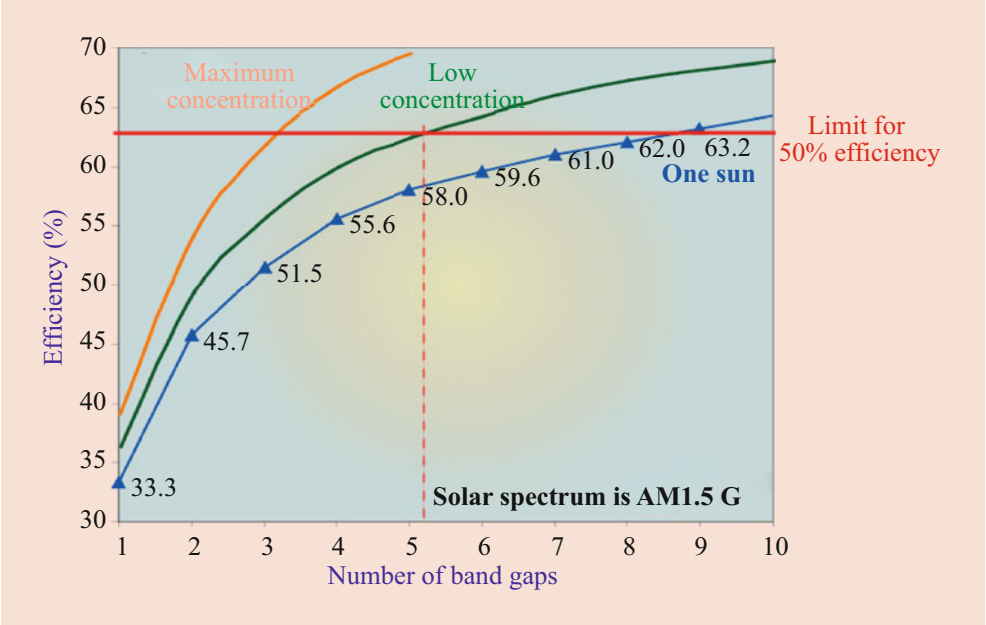

Fig. 19.25 Calculated detailed balance efficiency as a function of the bandgap number for a tandem cell, for three different concentrations of AM1.5 spectrum sunlight

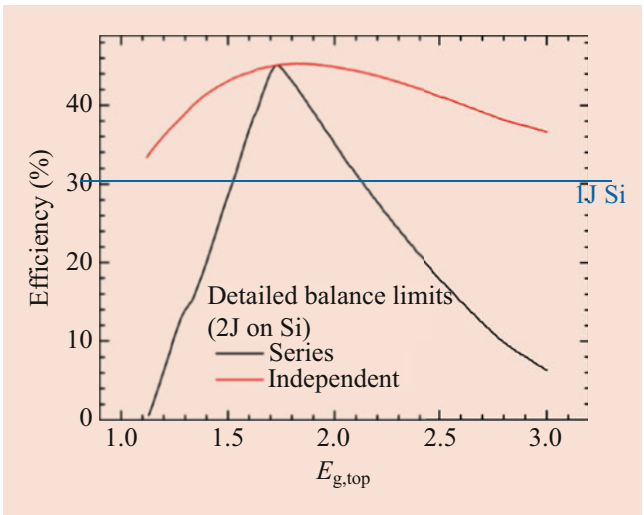

Fig. 19.26 Detailed balance efficiency versus bandgap of the top cell for a two-junction Si tandem

of current Si technology. II–VI materials are still in development for Si tandems, with basically only material growth demonstrations at present. The current highest efficiency in a monolithically grown series connected Si-based tandem is using a wider bandgap perovskite cell as the top cell [34]. The low temperature processing of the perovskite top cell is very compatible with integration with an already fabricated Si bottom cell. 2T perovskites on Si cells have recently exceeded 29% [35], the highest 2J performance reported to date for an integrated structure, as shown in Fig. 19.22 by the purple triangles. However, there remain many open questions about long-term stability of perovskites for solar applications, particularly with new higher bandgap materials.

From a stability, efficiency, and cost perspective, the direct growth of III–Vs on Si appears the most promising, with recent advances in the approaches and efficiencies of tandem structures. The key barrier to III–V/silicon solar cell is the lattice mismatch between silicon and most III–V materials. The importance and impact of III–V/Si integration means that many different approaches have been tried to overcome the lattice mismatch between Si and III–Vs. These include insertion of a layer that accommodates the strain [36, 37]; decoupling the III–V material from the Si substrate by limiting the direct contact between the two via techniques such as epitaxial lateral overgrowth [38–40] or nanostructures [41]; joining the III–V and Si by mechanical means such as bonding [42]; lattice-matched materials [43–47]; compositionally graded, metamorphic buffer layers; and the development of defect-tolerant materials [48].

GaP is the closest III–V material in terms of lattice constant for monolithic integration on Si; hence most approaches incorporate GaP, either for direct growth or as a grading layer for growth of other III–V materials. Grassman and coworkers have demonstrated 21.8% in a 2T tandem on Si using a GaP buffer and GaPAs grading layer to grow a GaAs top cell on Si [49, 50]. The University of Illinois and Arizona State University have collaborated on a graded junction cell on a GaP buffer, using graded GaAsP to grow a GaAsP top cell demonstrating 20% efficiency [51, 52]. Fraunhofer ISE has also used graded GaAsP growth to demonstrate a triple

junction cell with GaAs/GaInP top cells on Si exceeding 22% [53, 54]. Grading Si using a SiGe-based buffer as a template for further III–V devices has reached 20.6% [55]. An alternative option is to capitalize on defect and materials advances to develop a dilute nitride top solar cell [56]. Dilute nitrides are conventional III–V materials in which the introduction of a small amount of substitutional N (on the order of 1 to 2%) can lead to large changes in the bandgap and lattice constant, allowing for tunable materials to satisfy lattice and bandgap requirements in tandem cell applications. Dilute nitride-phosphides such as GaNPAs and GaInNP have been investigated for optoelectronic devices, including Si-integrated lasers and solar cells [57].

19.7 Nanotechnology-Based Approaches

Besides multijunction approaches, realization of many of the approaches listed for circumventing the Shockley-Queisser limit is difficult to realize in bulk semiconductor materials. For that reason, nanostructured materials have been an area of active investigation for so-called advanced concept or third-generation [2] photovoltaics. The advantages of nanostructured materials are in the ability to tune bandgaps through quantum confinement and surface effects, as well as modify the chemical and reactive properties of materials relative to their bulk forms. From the standpoint of optical properties, absorption is generally enhanced, and nanophotonic structures may be used to manage light in terms of light trapping and reflection losses. As discussed in connection with hot carrier solar cells, nanostructured materials may also have reduced energy loss rates, which help in terms of phenomena such as hot carrier extraction and carrier multiplication through impact ionization. The main detrimental effects are the increased surface to volume ratio, which may lead to increased recombination affecting both the short circuit current and the open circuit voltage as discussed in Sect. 19.3.1.

19.7.1 Nanomaterials

Nanostructure materials can be fabricated from the top down using nanoscale lithography such as deep UV, electron and ion-beam lithography, as well as direct manipulation of atoms on the surface using atomic force microscopy (AFM). At the same time, self-assembly of materials allows the growth from the bottom up of a variety of structures with atomic perfection. Some of the more interesting materials are summarized in the following. For an extensive review on the subject, see Chap. 2 of reference [58].

Layered Structures and 2D Materials: Already in the 1980s, epitaxial growth was exploited to realize nanostructure materials in one direction, the growth direction. The advent of molecular beam epitaxy (MBE) [59] and metal organic chemical vapor deposition (MOCVD) allowed atomic layer control of the growth of high-quality, lattice-matched heterojunctions. A *quantum well* (QW) corresponds to a layered structure of a narrow bandgap material sandwiched between two larger bandgap materials, which, as discussed in Sect. 19.3.4, can be type I or type II depending whether confinement exists for both electrons and holes (type I) or for just one (type II). A multi-quantum well (MQW) system is just a succession of QWs grown with sufficiently thick barrier material such that they are essentially isolated. If the barriers are sufficiently thin, then broadening of the QW states occurs and a superlattice (SL) is formed, with mini-bands. In all such materials, electronic confinement is only in one directly, and the motion in the plane is quasi-two-dimensional (2D), with a two-dimensional density of states.

In more recent years, true 2D materials have been synthesized and extensively characterized, beginning with work on *graphene* [60, 61], a 2D form of graphitic C, which forms a hexagonal honeycomb structure, and can be synthesized by exfoliation from graphite, chemical vapor deposition, as well vacuum graphitization of SiC. The electronic structure has a unique linear dispersion with no gap, where the conduction and valence bands meet at the so-called Dirac points, the discovery of which was awarded the 2010 Nobel Prize in physics. More recently, of 2D materials have been synthesized from transition metal dichalcogenide (TMD) monolayers, which are generally 2D semiconductors with bandgaps from 1 to 2 eV of the form MX_2, where X is a chalcogen atom and X is a transition metal [62]. Different 2D materials can be grown in layered structures called van der Waals heterostructures, which as the name suggests are bonded weakly in the vertical direction to form the equivalent of MQW and SL structures with unique optical and transport properties [63]. Because of their tunable bandgaps in the optimal range for solar energy conversion, there have been a number of demonstrations of photovoltaic effects, and proposals for energy converters based on such materials.

Nanowires and Nanotubes: These components are quasi-one-dimensional (1D) materials that are usually self-assembled, although they can be fabricated by top-down lithography as well. Carbon nanotubes (CNTs) are the most common nanotube structure, which are basically a rolled form of graphene, whose chirality (related to the direction along which the graphene sheet is rolled) determines whether they are metallic or semiconducting. Semiconductor nanowires (NWs) are solid crystalline, which may be grown using *vapor-phase synthesis*, in which nanowires self-assemble on from the gas phase onto a semiconductor substrate with a given crystallographic orientation. *Vapor-liquid-solid* (VLS) epitaxy is the most common method

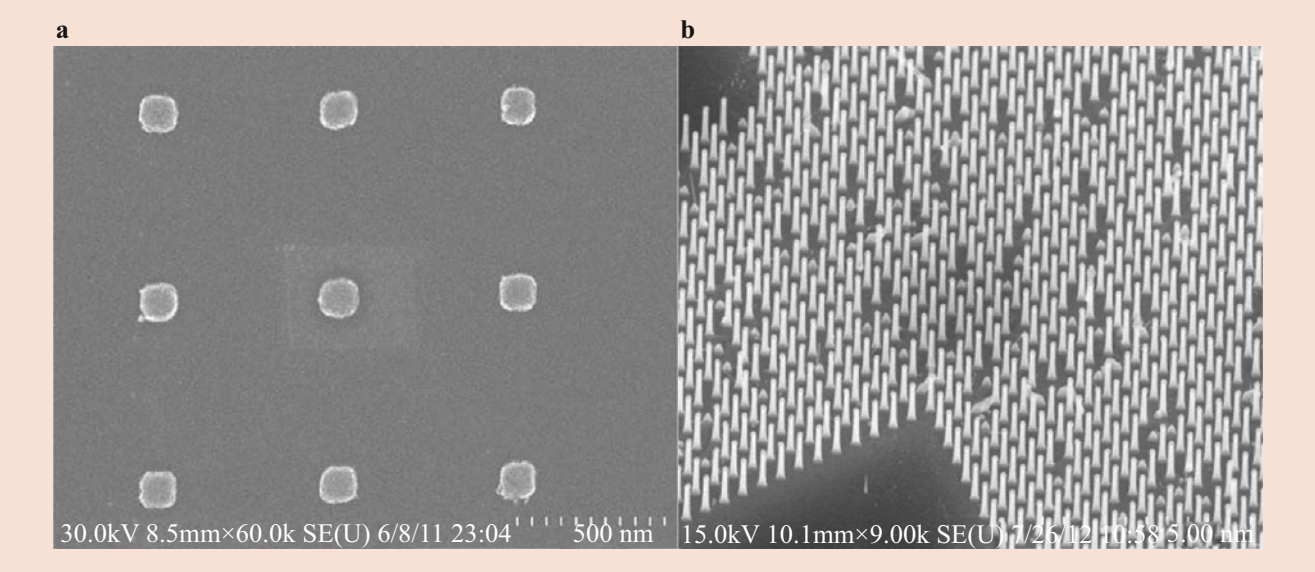

Fig. 19.27 Self-assembled growth of NWs using vapor-liquid-solid (VLS) epitaxy. (**a**) Scanning electron micrograph of Au seeds patterned with electron beam lithography. (**b**) Ge nanowires after growth on Si (111) [71]

of growth, in which metallic nanoparticles act as catalysts to nucleate the self-assembled growth of NWs, with the diameter of the NW directly related to the droplet size [64]. Fig. 19.27 shows a micrograph of Si NWs grown by the VLS method, where chemical vapor deposition (CVD) was used to generate the semiconductor precursors for VLS growth. The figure below also illustrates that the NWs may be deterministically placed using nanolithography techniques to pattern the catalyst.

Other methods may also be used for NW growth, however, including laser ablation and MBE. Growth of high-quality nanowires has been demonstrated in III–V (GaN, GaAs, GaP, InP, InAs) and II–VI (ZnS, ZnSe, CdS, CdSe) semiconductor NWs, as well as several different wide bandgap oxides (ZnO, MgO, SiO_2, CdO). Samuelsson and coworkers at Lund University have fabricated a variety of nanoscale electronic devices utilizing VLS-grown III–V semiconductor NWs as their active elements [65]. They have demonstrated that heterostructure nanowires of InAs and InP, as well as GaAs and InAs, can be realized that have very sharp heterointerfaces [66], both vertically and laterally (core-shell NWs, similar to core-shell nanoparticles; Fig. 19.28). Such heterostructure NWs have been used to fabricate nanoscale devices such as resonant tunneling diodes [67] and single [68] and multiply coupled [69, 70] quantum dots.

As discussed in more detail below, NWs can be used directly as the active absorber in solar cells (Sect. 19.7.4) and in terms of optical light management to increase absorption (Sect. 19.7.3).

Nanoparticles, Nanocrystals, and Quantum Dots: The names nanoparticles (NPs), nanocrystals (NCs), and quantum dots (QDs) are sometimes used interchangeably to denote either lithographically defined or self-assembled structures with characteristic dimensions on the order of 1–100 nm. If the NPs are single crystal structures, they are referred to as nanocrystals [72]. Nanoparticles can be metals, dielectrics, or semiconductors and are synthesized by a variety of techniques. Some mass-produced approaches include ball mill micro-machining, as well as pyrolysis and rf plasma techniques. High-quality NCs are synthesized through chemical solution methods, including sol-gel methods which result in colloidal solutions of nanoparticles. Self-assembled QDs of common III–V semiconductor materials (InAs, InGaAs, etc.) can form during epitaxial growth via the three-dimensional Stranski-Krastanov growth mode [73]. In this mode of growth, a thin layer of InAs is grown on top of a substrate of different lattice constant such as GaAs, where strain results in islanding of the epitaxial layer into 3D QDs, as shown by the micrograph in Fig. 19.28. Similar to NWs, QDs may become active components for realizing advanced concept solar cells discussed in the following sections as well as optical layers for light management beyond the texturing and antireflection coating approaches discussed in Sect. 19.3.2.

19.7.2 Dye-Sensitized and Quantum Dot Solar Cells

One of the first solar cell architectures that directly incorporated nanostructured materials as an active part of the absorber was the dye-sensitized solar cell (DSSC, or sometimes referred to as a Grätzel cell), which resembles an electro-

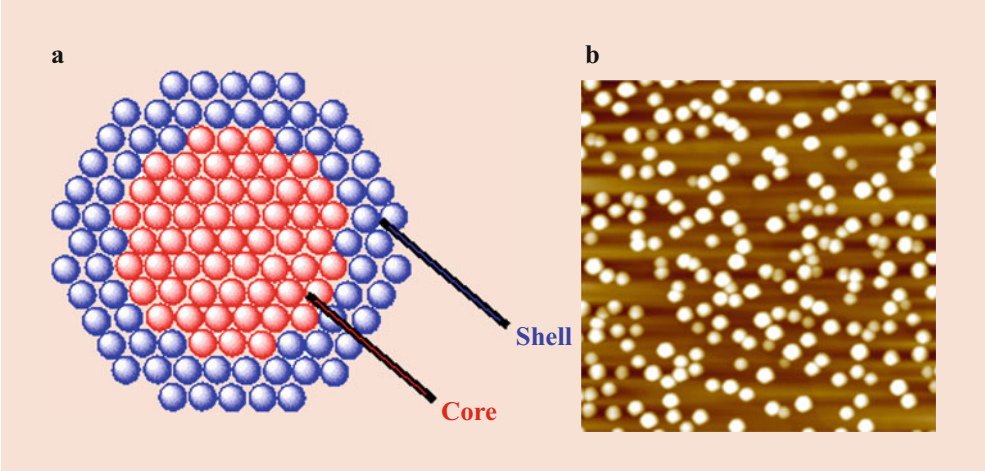

Fig. 19.28 (**a**) schematic of a core-shell nanoparticle (Wikimedia Commons). (**b**) micrograph of self-assembled InAs nanoparticles on a GaAs substrate [74]

chemical cell in design. The DSSC was first demonstrated by O'Regan and Grätzel in 1991 [75] and, as shown by the open red circles of Fig. 19.22, has reached efficiencies of over 11% with the conventional dye approach shown in Fig. 19.29. Conventional DSSCs have since been superceded by perovskite solar cells as discussed in Sect. 19.4.3, where the first high efficiency perovskite solar cells evolved from the DSSC architecture, and the highest efficiency perovskite cells still incorporate a nanostructured DSSC-like structure, albeit with the electrolyte replaced with a solid hole transport layer that is much more compatible with traditional thin film fabrication techniques.

The schematic of a conventional DSSC architecture is shown in Fig. 19.29. The absorber layer consists of nanoparticle or nanostructured TiO_2, which is a wide bandgap semiconductor with a bandgap of approximately 3.2 eV, coated with a dye such as ruthenium (Ru), whose HOMO-LUMO splitting is in the optimum range for the solar spectrum. The dye is usually spun on in liquid form to diffuse into and adhere to the TiO_2 nanostructure and is subsequently dried. The large surface to volume ratio of the nanostructured TiO_2 leads to an effectively large surface area, increasing light absorption. The whole structure is formed on a glass substrate as shown, coated with a TCO such as ITO or fluorine-doped tin oxide (FTO). When light is incident on the glass/TCO side, it is absorbed by the dye, and the excited e^- transfers from the excited LUMO level to the conduction band of the TiO_2 as shown. The electron diffuses through the TiO_2 matrix to the TCO and the external circuit. The positively charged hole left in the HOMO level reacts via a redox couple in the electrolyte, which is typically iodine based, consisting of I^- and I_3^- ions in solution. The dye is reduced by an electron being transferred to the dye through an oxidation process in the iodine, $3I^- = 2e^- + I_3^-$, where two holes in the dye are neutralized by converting three iodine ions into one I_3^- singly charged molecule, giving up two electrons to the dye. At

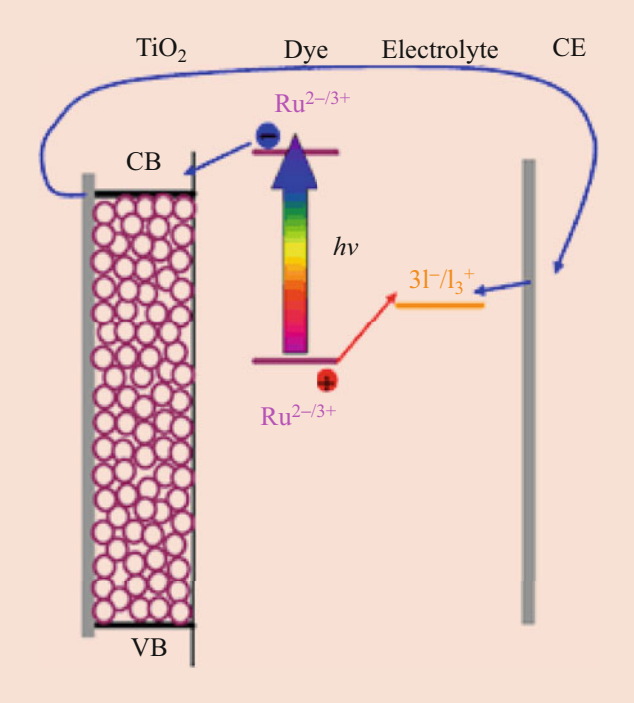

Fig. 19.29 Illustration of a dye-sensitized solar cell (DSSC) architecture. (Wikimedia Commons)

cathode, the positively charged ionic species, I_3^-,is reduced and converted back to $3I^-$ by the transfer of two electrons from the cathode, completing the circuit.

DSSCs have enjoyed some commercial success, particularly in niche applications such as building integrated PV, where different dyes corresponding to different colors provide some aesthetic benefits. Liquid electrolyte DSSCs suffer from stability issues as well as the complications of a panel structure involving liquid encapsulation. There are a variety of dyes, both natural and synthetic, that are suitable for DSSC

applications; however, they typically have a relatively narrow spectral absorption, which has led to the search for new dye materials such as inorganic NP-based dyes with broad absorption. Another problem arises due to recombination process occurring at the dye-TiO_2 interface, which lowers V_{oc}.

As discussed earlier in Sect. 19.4.3, a dramatic evolution of the DSSCs occurred with the development of the hybrid perovskite $CH_3NH_3PbI_3$ replacing traditional dyes, which could be introduced into the nanoporous TiO_2 matrix through low temperature processing. The liquid electrolyte was later replaced by a solid organic hole transport layer, which eliminated the issue mentioned above related to liquid-based cells, and a cell geometry more resembling that of a conventional thin film organic solar cell. More recently, the Cambridge group demonstrated that a planar hybrid perovskite thin film replacing the nanostructured TiO_2 could reach high efficiencies as well [22], which has increasingly become the dominant architecture, especially for tandem perovskite structures, although the mesoscopic approach continues to be investigated for high performance cells [76].

Quantum dot solar cells (QDSCs) have been of interest since the beginnings of the nanotechnology field [77]. As discussed in Sect. 19.8, QDSCs have many potential advantages in realizing advanced concept architectures in terms of multiexciton generation, hot carrier extraction, intermediate bands, and up-down conversion [78]. Like other nanomaterials, quantum confinement and surface effects allow tunable bandgaps for synthesizing ideal absorbers for single gap and multi-gap (tandem) cell applications. While MBE-grown QDs as described earlier have been used as absorbers in advanced concept architectures described later, colloidal quantum dots (CQDs) have been successful in realizing efficiency advances as shown in Fig. 19.22 by the open red diamonds.

There are several ways of incorporating CQDs into solar cell architectures. One is replacing the organic dyes in the DSSC structure above with semiconducting QDs such as InP, CdSe, CdS, and PbS [78]. More commonly, they are dispersed in an electron or hole conducting polymer forming, or in a ligand network ink, forming an organic solar cell architecture as discussed in Sect. 19.4.3. With the latter approach, the Toronto group in collaboration with KAUST demonstrated an 11.6% efficient PbS CQD-based device [79]. More recently, QDSCs based on inorganic perovskite CQDs ($CsPbI_3$) [80] (NREL) and hybrid perovskite CQDs of $FAPbI_3$ (where FA is formamidinium) (University of Queensland) [81] reached efficiencies of 13.4% and 16.6%, respectively. Of particular note is that the stability of these CQD-based perovskite materials appears superior to the bulk hybrid perovskites discussed earlier. While these recent perovskite-based QDSC results are quite promising, there are still many obstacles to overcome in terms of cost and stability which are active areas of research presently [82].

19.7.3 Light Management in Photovoltaics

As discussed in Sects. 19.2.2 and 19.3.2, maximizing solar light absorption in the semiconductor is critical in obtaining good short circuit current, which generally means getting photons into the semiconductor (no reflection from the front), and absorbing the photons before they can escape from the back or front of the cell. The necessary path length for absorption is directly related to the inverse of the absorption coefficient, $\alpha(h\upsilon)$, which is a strong function of wavelength, being small for photons just at the bandgap, and increasing strongly for shorter wavelengths. In terms of the path length, the fraction, f, of photons absorbed is given by

$$f = [1 - R(\lambda)]\left(1 - e^{-\alpha(\lambda)l}\right) \tag{19.50}$$

where R is the reflection coefficient from the front surface and l is average path length of photons in the absorber. Clearly one wants to minimize reflectance, while at the same time increasing the path length or correspondingly the absorption coefficient, which are the main objectives of light management.

Figure 19.30 illustrates the classical "ray optics" trajectory of light incident on a generic absorber, which has a textured surface which refracts light away from normal incidence, and a back-side reflector, which is in general textured as well to randomize the direction of the light. Due to internal reflection considerations, on the front surface, the ray is reflected and executes a number of bounces between the front and back surface before eventually exiting the front surface again at a small angle relative to the normal. For an absorber of width W, if there was no texturing on the front, and no reflection from the back, the path length is simply $l = W$. Adding an ideal back reflecting and assuming zero reflection when incident on the front surface leads to $l = 2\ W$.

Yablonovitch [8] used statistical arguments assuming ideal diffusive scattering from the front and back surfaces and classical ray optics, to derive the so-called classical light trapping limit for the enhancement of the path length in an absorber such as in Fig. 19.30

$$\langle l \rangle = 4n_s^2 W \tag{19.51}$$

where n_s is the index of refraction of the absorber. Taking Si as an example, with $n_s \approx 3.8$ for long wavelengths, a maximum path length enhancement of 58 is predicted. The implication is that one could reduce the thickness of the Si wafer from a typical value close to 200 μm to just a few microns, which would lead to substantial savings in terms of material costs (if one could process such thin Si), and actually lead to a boost in the cell voltage somewhat analogous to the effect of concentration.

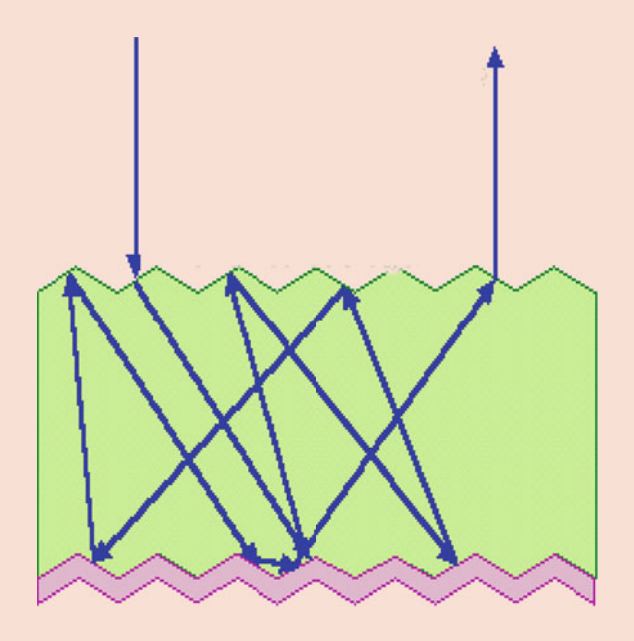

Fig. 19.30 Illustration of the classical path of light in a general semiconductor absorber structure including texturing of the front, the back, and a back reflector. (With permission from PVEducation.org)

Nanostructured materials offer the potential to go beyond the classical light trapping limit given by Eq. (19.51) [83], with characteristic dimensions corresponding to the regime of diffraction-limited optics. In recent years, there has been considerable interest in periodic arrays of optical scatterers forming *photonic bandgap* materials [84, 85], which are analogues to the band structure in semiconductor materials, in which gaps are opened up in the spectrum due to Bragg scattering. Such modification of the optical dispersion leads to passbands and stopbands for the propagation of electromagnetic radiation at certain frequencies. Such arrays can then be used to reflect or selectively enhance absorption, allowing the classical light trapping limit to be superceded, at least for certain bands of frequencies.

A common way to realize photonic bandgap structures is to grow or fabricate periodic arrays of NWs or nanopillars, as shown on the left side of Fig. 19.31. There, particular nanopillars were fabricated top-down using *nanosphere lithography*, in which silica nanoparticles are deposited on the surface of Si in a close packed hexagonal structure, followed by reactive ion etching through the nanospheres to form a periodic array [86]. The right side of Fig. 19.31 shows the measured reflectance (dashed curves), comparing the reflectance from different height nanopillars compared to bare Si. The solid curves correspond to full-wave finite difference time domain (FDTD) solutions of Maxwell's equations, where the ratio of the incident to reflected waves determines the reflectance. As can be seen, the nanopillars significantly decrease the reflectance due to light trapping, and that this reflectance is well described by the full-wave electromagnetic solutions to Maxwell's equations (as opposed to ray optics). The sharp features in the numerical simulations are due to the sharp features assumed in simulation, whereas experimentally, the nanopillars are somewhat tapered and the edges at the top and bottom are smoothed out. Atwater's group studied different NW arrays including both periodic and randomly spaced arrays and showed that the absorption properties of the arrays were evidence exceeding the classical light trapping limit over a limited band of optical frequencies [87].

Besides photonic bandgap structures, nanoplasmonic structures are also of interest in terms of enhanced light trapping. Plasmonic structures may correspond to metals adjacent to a dielectric, metal strips, and finally metallic nanoparticles on a surface or interface. Metal nanoparticles are similar to the semiconductor ones discussed in the Sect. 19.7.1 in terms of synthesis, where typically Au or Ag are used due to their low loss. Strong interaction between the incident electromagnetic waves and the collective charge oscillations of the metal structures results in the formation of hybrid surface plasmon polariton (SPP) modes. Such coupling is strongest close to the plasma frequency of the metal, and the SPP modes strongly favor propagation along the surface, which increases the effective path length manyfold, hence increasing absorption. Plasmonic structures may be incorporated at the front or back surface as well as within the absorber itself, and have been investigated in Si, III–V, and organic solar cells, where in particular they are used to try and improve the red response of cells, where absorption is usually weakest. For Si solar cells, for example, path length enhancements of seven to eight times were reported in Si cells [88], while plasmonic nanoparticle arrays of Au NPs on GaAs cells showed increase in short circuit current of 8% [89].

19.7.4 Nanowire Solar Cells

As discussed in the previous section, NW arrays have demonstrated good light management properties in terms of photonic bandgap properties, with the potential to exceed the classical light trapping limit. Semiconductor NWs may also act as the active optical absorber in photovoltaic applications, in which the effective absorption per volume of material is greatly enhanced compared to the bulk due to the nanophotonic enhancements in array structures. NWs also have the advantage of having good quasi-1D transport properties along the axis of the NW, allowing for separation and collection of photoexcited EHPs. III–V NWs are routinely grown on Si substrates, allowing for the possibility of Si-based tandems discussed in Sect. 19.6. In terms of lattice matching constraints and critical thickness limitations in

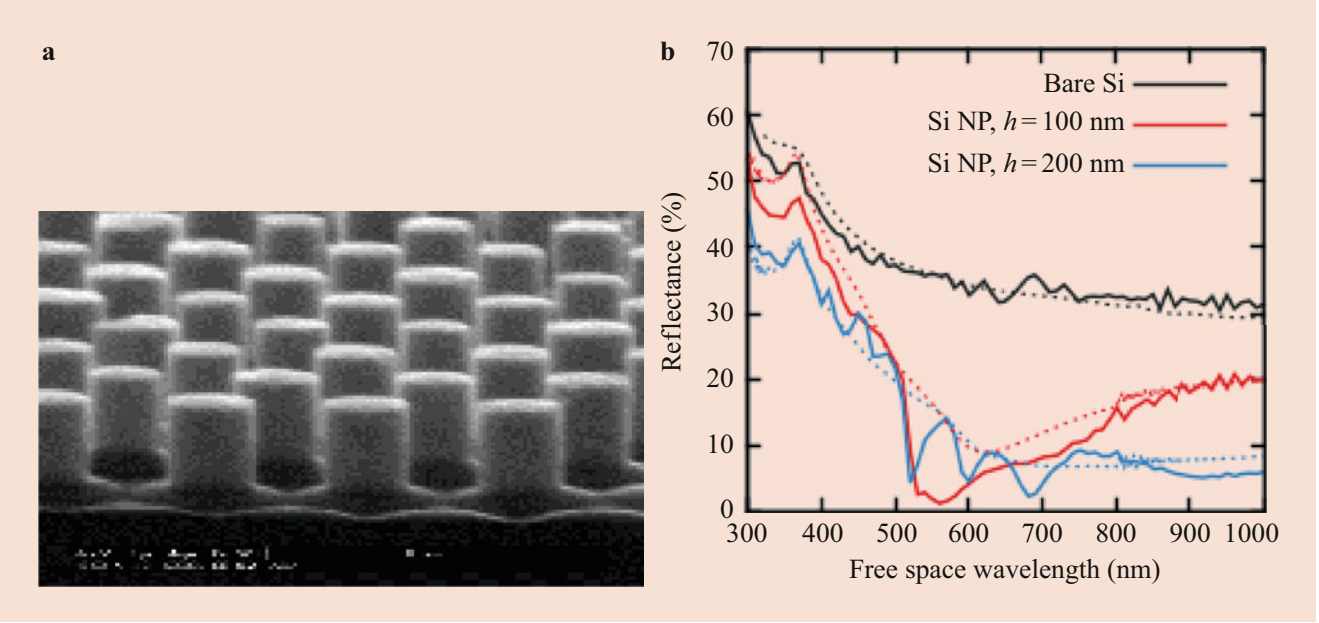

Fig. 19.31 (**a**) Micrograph of nanopillars fabricated using nanosphere lithography. (**b**) Measured (dashed) and simulated reflectance from a regular hexagonal array of Si nanopillars with period, $p = 600$ nm, for cylinder heights of a 100 (red) and 200 nm (blue) [86]

epitaxially grown layered structures, the finite lateral extent of NWs allows the strain to be accommodated in the lateral direction, allowing much more flexibility in the heterogeneous growth of different lattice constant materials. The ability to grow both vertical and lateral (core-shell) structures allows for the design of material systems to be used to realize advanced concept photovoltaics that cannot be realized with bulk materials. The main disadvantage of NWs (and all nanostructured systems) is that the large surface to volume ratio means that surface recombination effects are enhanced, which is detrimental to solar cell performance as discussed in Sect. 19.3. Surface passivation strategies are therefore critical. In the case of NWs, an effective strategy is growth of a core-shell structure with a large bandgap material as the outer layer, which reduces recombination [90].

There have been a number of studies of optoelectronic devices based on NWs including solar cells, starting in the mid-2000s [91–94]. The best performance in NW solar cells has been demonstrated in III–V compound semiconductors like GaAs, due to the high absorption associated with a direct bandgap material, and good transport properties. As mentioned above, one of the advantages of NW-based systems is that III–V materials may be grown on Si substrates, providing another approach for Si-based tandem solar cells. A schematic of an InGaAs NW array solar cell architecture is shown in the upper panel of Fig. 19.32. The NWs are core-shell structures, with InGaAs cores, and InP cladding layers, grown on Si (111) substrates. The (111) orientation is usually necessary to grow vertical NWs. This radial core-shell design has been used by the Technical University of Munich group for optoelectronic applications such as NW light-emitting diodes (LEDs) and lasers. [95]. As shown in the bottom panel of Fig. 19.32, regular arrays of NWs with well-defined periodicity are grown using nanolithographic techniques, in this case nanoimprint lithography, which is a low-cost method for nanofabrication. The main difficulty in such NW solar cell approaches is in making both p and n contacts. While the Si substrate serves as one contact, the top must be contacted separately as shown, which must be isolated from the substrate to avoid leakage.

Besides Si-based tandem solar cells, there is considerable interest in Si-based optoelectronics, integrating III–V-based photonic circuits with Si microelectronics. Chuang et al. [97] demonstrated the first NW GaAs LED and GaAs NW avalanche photodetectors (APD) grown on Si substrates using relatively low temperature processes compatible with CMOS technology. They later demonstrated the first InGaAs/GaAs core-shell NW laser grown on silicon [98].

For NW solar cells, one may either use lateral core-shell junctions or vertical junctions grown vertically along the axis of the NW. Colombo et al. reported a single GaAs core-shell NW p-i-n solar cell [99, 100] with an efficiency of 4.5% and a V_{oc} for GaAs cells of almost 1 V, which is comparable to that of high performance GaAs bulk solar cells. Radial GaAs junction arrays were reported by Mariani et al. [101] with efficiencies of 2.54%. In the past 5 years, remarkable improvement in the performance of NW solar cells has been reported. Axial InP p-i-n junction arrays were reported by Borgström et al. [102] with 13.8% efficiency in 2013. Sol

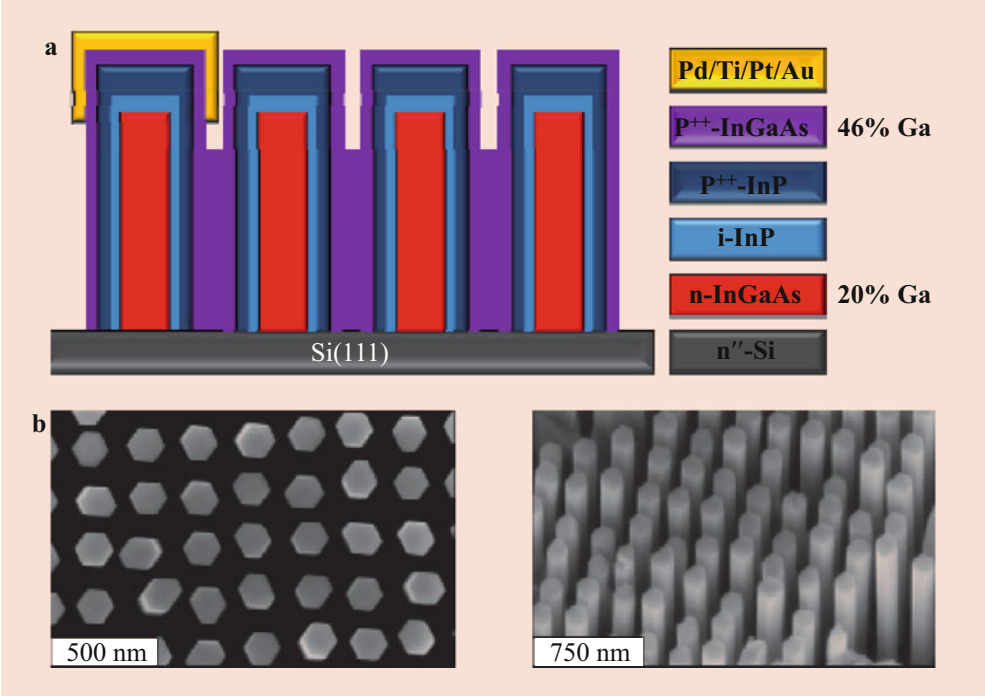

Fig. 19.32 (**a**) InGaAs core-shell nanowire solar cell structure. (**b**) SEM picture of arrays of NWs defined by nanoimprint lithography [96]

Voltaics and Lund University reported GaAs VLS-grown nanowire solar cells with independently tested efficiencies of 15.3% in 2016 [103]. In the same year, Eindhoven University reported a 17.8% InP vertical junction nanowire solar cell formed by etching and passivation [104]. The improvement in NW solar cell technology has occurred quite rapidly, from a few percent in 2009 to over 17% in 2017, similar to that of perovskite solar cells, although not represented on the NREL efficiency charts.

19.8 Advanced Concept Photovoltaics

Advanced concept is a term sometimes used to describe novel approaches to exceeding the Shockley-Queisser (QS) limit beyond the demonstrated approach of multijunction solar cells, based on circumventing the implicit assumptions in QS discussed in Sect. 19.5.2. Below we briefly review three such concepts, intermediate band, multiexciton generation, and hot carrier devices. There are also other approaches not discussed here, including up-down conversion using phosphors and nanoparticles to narrow the effective spectrum, as well as hybrid photovoltaic-thermal approaches, such as thermophotovoltaics, or spectral splitting approaches to use both photovoltaics and concentrating solar thermal for electrical energy production. Green's book on third-generation photovoltaics provides an excellent overview of these various approaches [2].

19.8.1 Intermediate Bands

Finally, rather than fabricating multiple junctions, another proposed approach to circumvent the SQ single bandgap assumption is to introduce multiple energy levels within the same material. Luque and Martı [105, 106] first proposed the concept of an *intermediate band* (IB) solar cell, although the same basic concepts were already investigated earlier in connection with MQW solar cells [77, 107, 108]. It consists of an intermediate band between the conduction and valence band of a bulk-like material. The most widely investigated approach is illustrated in Fig. 19.33, where the intermediate band arises from the introduction of either quantum wells or quantum dots into a wider bandgap material. Quantum wells have quantized levels as shown, which broaden in a MWQ or SL structure. However, there remains a continuum of states in the directions parallel to the growth direction, which is a disadvantage in realizing a separate intermediate band. Quantum dots on the other hand have true discrete density of states, which broaden into an intermediate band when grown as a SL. Besides IB QW and QD structures, bulk IB materials may be synthesized, for example, in alloy structures [109], where a narrow band exists between the conduction and valence bands.

Figure 19.33 illustrates the processes and energy separations in the IB concept. Here E_c and E_v represent the CB and VB edges of the higher bandgap material with bandgap E_G. The center of the IB is an energy E_{IV} above the VB, and E_{IC} below the CB. As shown, the IB allows sub-bandgap photons

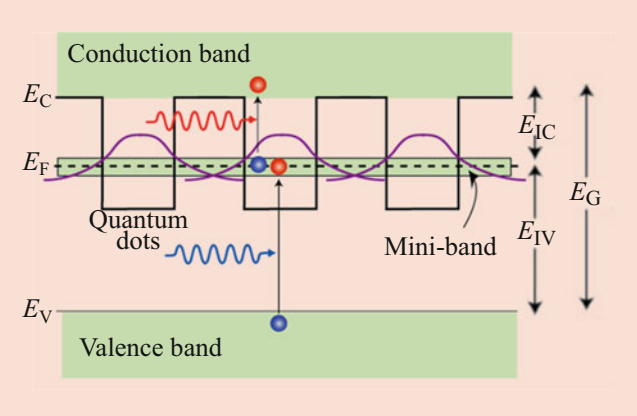

Fig. 19.33 Illustration of an intermediate band solar cell architecture based on quantum dot (or quantum wells) levels introduced within a wider bandgap host semiconductor [110]

to be absorbed, promoting electrons from the VB to the IB and promoting electrons in the IB to the CB. The third process is the direct band to band absorption from VB to CB. In order for the IB concept to provide an efficiency increase of the SQ limit, there must be a separate quasi-Fermi energy associated with the IB band which is separate from that of holes in the VB and electrons in the CB. For example, if the Fermi level of the IB is above the IB and close to the CB (the usual case under strong photoexcitation), then the IB states are all filled, and not transitions can occur to the IB. Hence, ideally, it should be half occupied. Likewise, if the IB and CB quasi-Fermi energies are common, then cell will be effectively a cell with a bandgap E_{IV}, with a drop in V_{oc}. Thus, having multiple quasi-Fermi energies is a necessary for efficiency operation.

Detailed balance may again be used to calculate the maximum conversion efficiency as a function of E_G and E_{IC} (E_{IV} being simply E_G-E_{IC} in this three-level approach). For any particular value of E_{IC}, there exists an optimum E_G for maximum efficiency. Luque and Martí used detailed balance to calculate the maximum efficiency versus E_{IC}, where the optimum combination corresponds to $E_G = 1.95$ eV and $E_{IC} = 0.71$ eV, corresponding to an efficiency of greater than 60% under concentration, clearly well above the SQ single gap limit.

There have been a number of experimental reports that demonstrate the presence of the three individual processes, in a number of different technologies including solar cells, quantum dot lasers, and quantum cascade lasers [111–115]. However, demonstration of independent quasi-Fermi energies necessary for IB cell performance is difficult. Marti et al. have demonstrated the ability to collect carriers at high energy using two low-energy photons [116], which is a necessary process for IB operation. In addition, early results from Nelson et al. in QW solar cells are explained [117] by a different Fermi level inside a QW than in the barrier. Thus there is the suggestion that multiple quasi-Fermi levels can exist in multilevel structures, although the demonstration of a high performance IB cell that convincingly exceeds the SQ limit effect remains elusive.

An extensive review of the state of the art of IB solar cell technology is given by Okada et al. [118], which the interested reader is referred to for more detail. A well-studied system is that of self-assembled multiple layers of InGaAs QDs grown on GaAs as discussed in Sect. 19.7.1 via Stranski-Krastanov strained growth mode. Although the combination of bandgaps and intermediate-level energies is nonideal from the detailed balance calculations mentioned above, single crystal defect-free structures may be grown, where the QDs tend to self-align during between subsequent layers, so that large numbers (10s of layers) may be grown. The main challenge in realizing a viable IB solar cell technology is demonstrating a significant increase in short circuit current due to the sub-bandgap absorption of photons while not degrading the open circuit voltage, which has been hard to simultaneously achieve if the occupancy of the IB level is tied to that of the CB. While this has been demonstrated to some extent in GaAs cells, typically the baseline GaAs cells for comparison have inferior V_{oc} (0.7–0.9 V) compared to the voltages of record GaAs cells which exceed 1.1 V [119]. Various schemes have been introduced such as doping the QDs, strain compensation, and other approaches, to both improve the optical efficiency and minimize recombination. For example, Bailey et al. have demonstrated GaAs-based IB cells with voltages over 1.0 V [114], with improvement in the short circuit current, although the efficiency was still less than the baseline cell.

19.8.2 Multiple Exciton Generation (MEG)

An energetic electron or hole in a semiconductor with a kinetic energy greater than the bandgap may lose its kinetic energy creating one or more EHPs depending on the energy. This process is generally called impact ionization, since promoting an electron from the VB to CB is equivalent to bond breaking. This may occur through acceleration of a charge carrier to the threshold energy for this process under high electric fields, or it may occur for photoexcited electrons whose excess energies are high enough to create a second EHP. Figure 19.34 illustrates the creation of multiple electron-hole pairs for different photon energies, assuming that electrons near the top of the VB are excited into the CB with an excess energy equal to the difference of the photon energy and the bandgap. As shown, there are different thresholds reached in energy when the photon energy in this picture is $h\nu = 2E_g$, $3E_g$, $4E_g$, etc., resulting in 2 EHPs, 3 EHPs, etc. When present in a solar cell, the quantum efficiency can

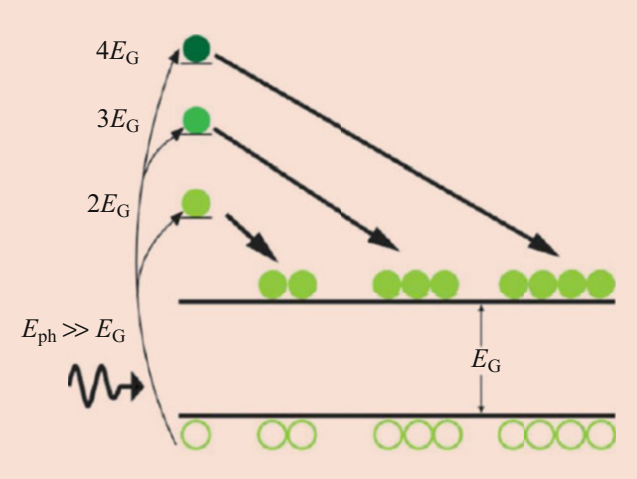

Fig. 19.34 The multiple carrier generation process for photon energies in excess of one, two, three, and four times the bandgap

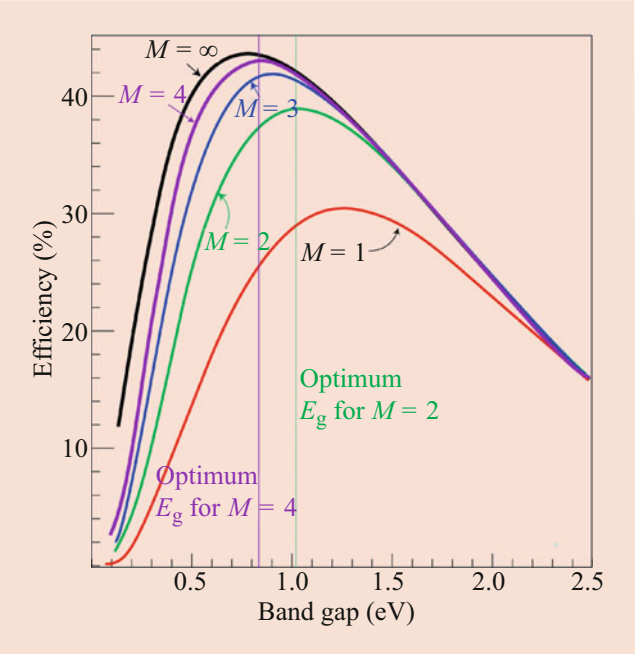

Fig. 19.35 Calculated detailed balance efficiency as a function of bandgap for the AM0 blackbody spectrum with consideration of increasingly higher order multiplication factors

now be greater than 100%, breaking the assumption of 1 EHP per photon, increasing the photocurrent, and allowing the SQ limit to be overcome.

Creation of multiple electron-hole pairs by energetic photons was already known for Ge in the 1960s. Kolodinski et al. measured the quantum efficiency in bulk silicon solar cells as a function of photon energy, where they showed greater than 100% QE occurring above 3 eV [26]. Such a high photon energy is beyond the useful range for the solar spectrum, due to the fact that the threshold for impact ionization in bulk crystals must simultaneously satisfy both energy and crystal momentum conservation, which shifts the threshold up by a factor of 1.5 using simple effective mass considerations with parabolic bands.

On the other hand, due to quantum confinement in nanomaterials, conservation of crystal momentum is relaxed, in particular for QDs. Experimentally using ultrafast absorption and other spectroscopies, threshold energies for carrier multiplication were found to be close to twice the fundamental gap in PbSe and PbS CQDs with quantum efficiencies in excess of 300% [120, 121]. The optically excited states of QDs are strongly excitonic in nature due to the strong confinement, hence the term *multiple exciton generation*, or MEG for short. Experiment [122] and theoretical calculations [123] suggest that MEG occurs over very short time scales and may be regarded as a coherent effect, rather than as two successive scattering processes, although there is still not agreement on this interpretation. MEG has now been demonstrated in a variety of nanomaterials, including CQDs of PbSe, PbS, InAs [124], PbTe [125], Si [126], and CdSe [127].

The effect of MEG on the detailed balance efficiency is easily incorporated into Eq. (19.46) [128]. The incident photon flux includes both the direct and diffused terms, which in the SQ analysis is equated to the photocurrent assuming 1 EHP per photon, which in the presence of MEG is weighted inside the energy integrals of the first two terms by the quantum yield (QY) as a function of photon energy, $Q(E)$, which is the number of EHPs produced per incident photon. For the ideal case, carrier multiplication is assumed to jump abruptly with each multiple of the threshold exceeding, represented mathematically by the staircase function

$$Q(E) = \sum_{m=1}^{M} m\Theta\left(E - mE_g\right) \tag{19.52}$$

where Θ is the unit step function, m is the number of electron-hole pairs generated per photon, E_g is the threshold energy (ideally the bandgap energy), and M is the maximum number of EHPs per incident photon. Additionally, it is usual to weight the voltage term, qV, by $Q(E)$ in the third integration to account for the inverse process to MEG (Auger recombination in the bulk), i.e., multi-electron recombination [2]. Assuming the blackbody spectrum form with a unity concentration factor in Eq. (19.46), the calculated detailed balance efficiency versus bandgap with different values of M in Eq. (19.52) is shown in Fig. 19.35. The result using the AM1.5 spectrum gives a similar and somewhat higher efficiency but less smooth as was the case in Fig. 19.24 due to spectral features.

The case of $M = 1$ is just the SQ limit for the blackbody spectrum. Already for $M = 2$, there is a sizable increase in maximum efficiency, which approaches 44% for the limit of

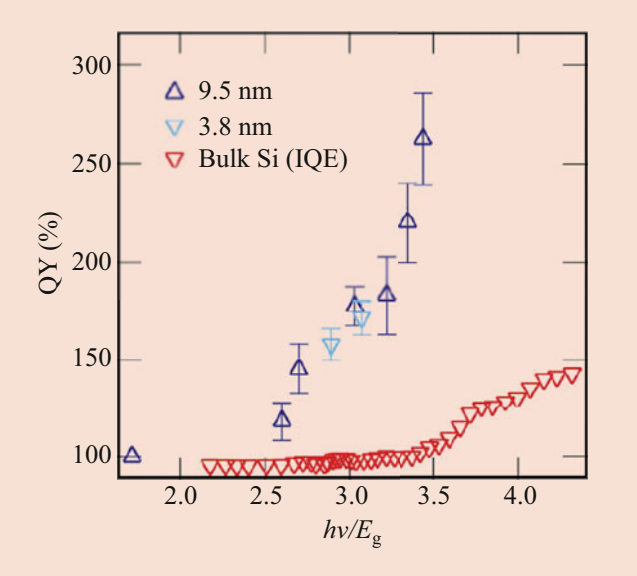

Fig. 19.36 Measured quantum yield versus photon energy (normalized by the bandgap) for bulk Si and two different diameters of nanoparticles. (With permission from [127])

M going to infinity. The optimum bandgap decreases with increasing multiplication factor M, as shown, going from 0.76 eV for large values to 1.05 for $M = 2$ [129], very close to that of Si.

The ideal quantum efficiency given in Eq. (19.52) is never in practice observed, as in experimental data shown in Fig. 19.36. The idea case assumes the existence of multiple separate, noninteracting MEG processes for excitation of 2 EHPs, 3 EHPs, etc. Also, the assumption that all excess energy of the photon is given to electrons in the CB is only true near the band edge for a high ratio of hole to electron effective masses. In the realistic case of photon energies exceeding twice the bandgap, the density of states of holes and electrons coupled by a high-energy photon is roughly equal, leading to a smearing out of the threshold energy for the onset of MEG.

Ultrafast spectroscopy has been primarily used to measure MEG by monitoring the transient state filling on a picosecond time scale at the bottom of the conduction band for different pulse excitation energies, which provides a measure of the QY in terms of the number of EHPs produced per incident photon. Fig. 19.36 plots experimental QY data for Si NPs measured spectroscopically by NREL [126] in comparison to the experimental internal quantum efficiency data of bulk Si solar cells [130]. As mentioned earlier, the threshold for turn-on (QY > 100%) for bulk Si does not occur until relatively high energy due to energy and momentum conservation constraints, while for Si NPs, the turn-on is much closer to twice the bandgap (including quantum confinement and excitonic effects in NPs). The NP data shows more of a linear slope past threshold rather than an abrupt turn-on, characteristic of most experiments. As mentioned above, the slope is related to the partitioning of the excess energy between electrons and holes, as well as the efficiency of the multi-excitation effect relative to competing energy relaxation effects due to phonons and other processes. While most evidence for MEG comes from ultrafast optical measurements in NPs, recently the internal quantum efficiency of PbSe quantum dot solar cells was reported by the NREL group in which for short wavelength photons above the threshold for MEG, quantum efficiencies greater than 100% were measured [131], which is promising for realizing MEG effects in real devices.

Besides MEG in NPs, other nanostructures have exhibited carrier multiplication effects. Evidence for MEG in CNTs was reported by Gabor et al. in CNT photodiodes [132]. MEG in multiexciton in PbSe nanowire/nanorod structures was demonstrated by Cunningham et al. where the performance of PbSe nanorods was significantly improved compared to PbSe NPs in terms of both the QY threshold and the slope after threshold (steeper) [133]. MEG in NWs would have potential advantages in terms of the NW solar cells discussed in Sect. 19.7.4, as efficient carrier collection may occur along the axis wire for vertical structures or transverse in core-shell structures, in contrast to NP-based structures which require some extraction mechanism such as tunneling for carrier collection.

As mentioned earlier, the efficiency of the MEG process depends on a competition between carrier multiplication processes like impact ionization and inelastic energy loss mechanisms such as electron-phonon scattering, which relax the excess energy of the electrons and holes back to the band edges (thermalization). Such energy relaxation processes are also important for hot carrier solar cells, discussed in the next section. In semiconductors, electrons lose (or gain) energy through acoustic and optical phonon emission (absorption). Due to the relatively large energy associated with optical phonon emission, on the order of 20–50 meV per event, optical phonon energy loss usually dominates, particularly in polar III–V and II–VI materials where the Fröhlich interaction (polar optical scattering) for zone center optical phonons is strong.

Nanostructures such as in QWs, NWs, and NPs have been experimentally observed to have reduced energy relaxation rates by a number of researchers discussed in more detail in the next section, for example, by Pelouch et al. [134]. In reduced dimensionality nanostructures, energy relaxation requires *intersubband* scattering in order for electrons and holes to reach their lowest energy states in the CB and VB, respectively, i.e., scattering between the quantized states associated with the spatial confinement in one or more directions. Due to this requirement, the optical emission rate may

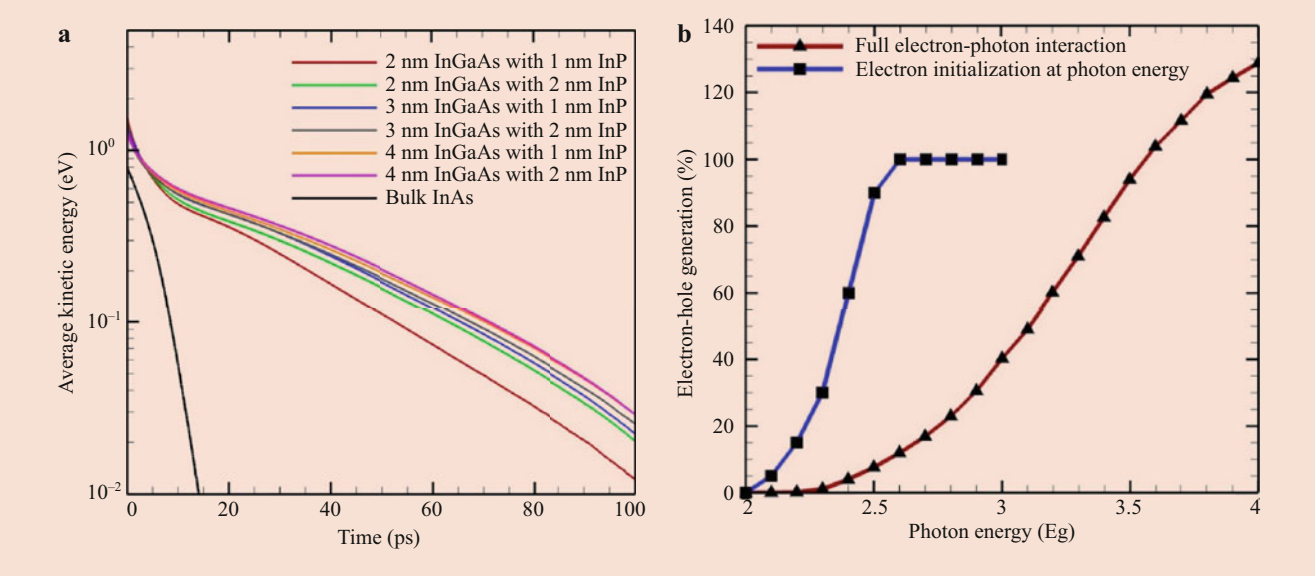

Fig. 19.37 (**a**) Full band Monte Carlo simulation of the average kinetic energy versus time for carriers excited in a short time pulse at an energy $2E_g$ above the CB edge (bulk) and lowest confined state (NWs) for different diameter NWs. (**b**) Simulated quantum yield (relative to the initial population) versus excitation energy for a 2 nm InGaAs NW and 1 nm InP cladding [135]

be suppressed due to so-called "phonon bottleneck" effects, when the subband spacing is such that there is no final state to scatter to. In 2D materials like QWs, there is a continuum of states associated with the free transverse motion which usually provides a channel for scattering. However, in 1D (NWs) and 0D (NPs, QDs), such effects become more important due to the spike-like density of states (DOS).

The left panel of Fig. 19.37 shows the simulated energy versus time of a short time pulse of photoexcited electrons in bulk InGaAs compared with narrow core-shell InGaAs/InP nanowires of various core and shell thicknesses using full band ensemble Monte Carlo simulation, a particle-based technique for simulating nonequilibrium carrier dynamics [135]. As shown, the energy loss rate, here limited mainly by polar optical phonon scattering, is significantly slower in the nanowire structures compared to the bulk. Such results are consistent with slow energy relaxation observed in semiconductor NWs. Optical studies in InP NWs using transient Raleigh scattering [136] and steady-state photoluminescence [137] showed energy relaxation times of several hundred ps and high carrier temperatures under steady-state excitation.

The right panel of Fig. 19.37 shows the simulated carrier multiplication versus photon energy based again on full band NW Monte Carlo simulation, including the calculated QY due to impact excitation rate in NW systems [135]. The blue curve corresponds to the simple assumption of all the excess photon energy going to the electrons, whereas the red curve is a more realistic calculation in which the dipole matrix element for direct band to band absorption is used to generate the electron and hole injected distributions, where the excess energy is more evenly split between the two systems. As can be seen, while the simple model leads to a more ideal (i.e., Eq. (19.52)) step-like QY, the full calculation of the optical absorption leads to a higher threshold and lower slope after threshold.

19.8.3 Hot Carrier Solar Cells

The final advanced solar cell concept discussed in this chapter is related to circumventing the SQ assumption that the carriers are collected at energies corresponding to the band edges, which are the main source of thermalization loss discussed in Sect. 19.5. The idea is to extract photoexcited carriers at energies well above the band edges before they lose energy to phonons as discussed in the previous section. Figure 19.38 illustrates the concept of a *hot carrier solar cell* proposed by Ross and Nozik in the 1980s [28]. The structure consists of an ideal absorber with a low energy loss rate for the photoexcited electrons and holes. *Energy selective contacts* extract electrons only on the left in a narrow energy window, and holes to the right as shown. Realization of such contacts is challenging; one of the main approaches is implementation of a resonant tunneling structure, such as a double barrier heterostructure, or tunneling through an artificial impurity such as a QD in a wide bandgap material [138]. The contacts themselves should be at temperature of the surround ambient as discussed by Würfel et al. [30], requiring that the absorber must be spatially separated from the cold metallic contacts; otherwise there will be strong energy

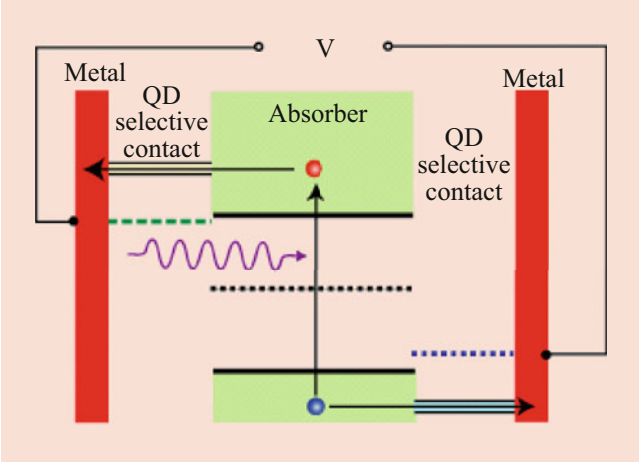

Fig. 19.38 Hot carrier solar cell architecture consisting of an ideal absorber with energy selective contacts [110]

loss mechanism due to cold contact electrons interacting with carriers in the absorber layer.

While the carriers in a hot carrier device ideally do not lose energy through phonon scattering processes, they do exchange energy among themselves through electron-electron, electron-hole, and hole-hole scattering. This can occur through two-particle scattering or scattering between charge carriers and collective excitations such as plasmons. Such scattering drives the distribution function of the carriers toward the equilibrium distribution represented by the Fermi-Dirac (FD) (or for nondegenerate carriers, Maxwell-Boltzmann, MB) distribution, however at an effective temperature, T_H, much greater than the lattice temperature, T_L.

Ensemble Monte Carlo (EMC) simulation has been used to simulate this nonequilibrium evolution of the carrier distribution [135], as shown in Fig. 19.39. The EMC simulations are for a quasi-2D system (10 nm GaAs/AlGaAs quantum well), which show the evolution of the electron distribution from a highly nonequilibrium distribution shortly after the pulse to a heated FD distribution. Scattering due to polar optical phonons, intervalley deformation potential, and carrier-carrier scattering (electron-electron, hole-hole, electron-hole) are included. Immediately after the optical pulse, the electron distribution is an athermal Gaussian-shaped distribution at the excess carrier energy. Even at these short times, an optical phonon *sideband* or *replica* is observed below the peak due to the effectiveness of polar optical phonon scattering. As time progresses, a series of phonon replicas appear showing that the initial cooling occurs through a cascade of optical phonon emission events. During this time, the distribution broadens due to electron-electron scattering, and eventually the phonon replicas vanish and are replaced by a what appears to be a heated FD/MB distribution, whose temperature continues to decrease with increasing time due to phonon emission.

Ross and Nozik considered the theoretical performance of hot carrier solar cells [28], based on the detailed balance approach discussed in Sect. 19.5. Within this approach, the electrical power delivered from the cell, P_{out}, may be written.

$$P_{out} = \left(I_{ph}/q\right) \Delta\propto_H T_a/T_H + \left(I_{ph}/q\right) \varepsilon_{ext} \left(1 - T_a/T_H\right) \tag{19.53}$$

where I_{ph} is the photocurrent corresponding to photons above the bandgap of the absorber, $\Delta\mu_H$ is the quasi-Fermi-level splitting in the absorber, T_a and T_H are the ambient and hot carrier temperature in the absorber (assuming a heated FD/MB distribution as discussed earlier), respectively, and ε_{ext} is the separation of the selective energy contacts or, more precisely, the Fermi energy separation of the metal contacts to the electrons and holes. In the limit that the ambient and hot carrier temperatures are the same, this just reverts to the usual SQ model where the voltage out is the quasi-Fermi energy separation. For high carrier temperatures, the first term is small, and the output voltage is determined by ε_{ext}, while the photocurrent corresponds to the gap of the absorber, which then favors small gaps. There is a limit on ε_{ext} set by the total energy available in the solar spectrum, so that assuming no energy loss and small bandgaps, the theoretical detailed balance conversion efficiency approaches the maximum thermodynamic conversion efficiency of 85.4% [139]. Würfel and coworkers later considered the effect of impact ionization on the ultimate efficiency of this concept [140, 141].

For the hot carrier solar cell to exceed the SQ limit, it's necessary that the energy loss rate in the absorber be very low such that a high carrier temperature may be maintained, as evidenced by Eq. (19.53). This is very challenging, since the energy rate due to optical phonons in the bulk and in quantum wells is subpicosecond. As seen in Fig. 19.39, even at very short times, polar optical phonon emission is already cooling the initial high energy distribution of carriers. As discussed in Sect. 19.8.2, the energy loss rate in NWs is reduced several times compared to bulk, although this rate is still too fast reaching high carrier temperatures under steady-state conditions. In QDs, the energy loss rate is further reduced, due to phonon bottleneck effects. As mentioned in the previous section, pump and probe as well as *cw* experiments in QWs have demonstrated greatly reduced cooling rates, and high carrier temperatures for high excited carrier densities, despite the fast polar optical phonon energy relaxation rate. Attempts have been made to utlize this in a hot carrier solar cell architectures, where researchers have demonstrated hot carrier transfer from quantum well absorbers to contacts [142], and photovoltaic conversion efficiencies above 10% [143].

One proposed explanation for strong hot carrier effects in nanostructure system is in terms of nonequilibrium optical phonons (hot phonons) [144, 145]. In nanostructures in con-

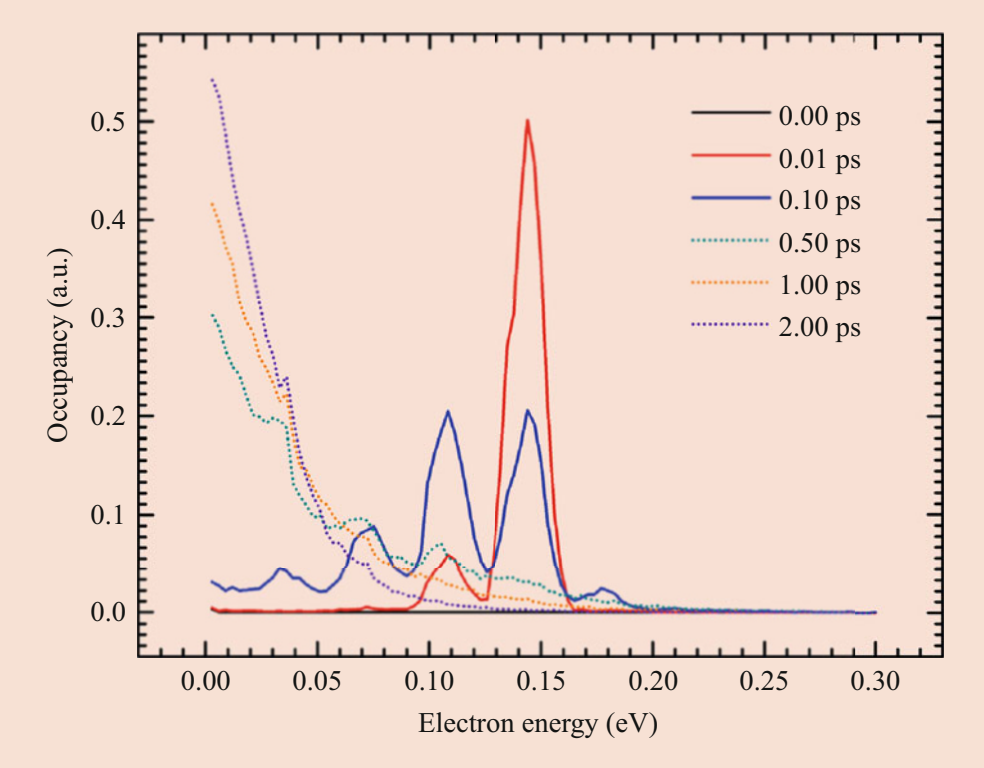

Fig. 19.39 EMC simulation of the time evolution of the electron distribution in the conduction band of a 10 nm GaAs quantum well at 10 K for carriers injected at 150 meV above the band edge, with an injected carrier density of $5 \times 10^{11}/\text{cm}^2$ [135]

trast to bulk systems, the excitation of EHPs occurs in a small volume spatially, and hence energy relaxation and phonon emission also occur in the same small volume. In particular, optical phonons have a very small group velocity, essentially zero at the zone center, and so remain in the excitation volume until they decay into acoustic modes through anharmonic three and four phonon processes, which propagate away from the excitation volume at essentially the sound velocity of the crystal. The nonequilibrium population of optical phonons increases the probability of phonon absorption, it transfers the energy lost back into the electron-hole system, and the excess kinetic energy of the EHP is retained in the coupled charge carrier/optical phonon system, essentially until the hot phonons decay into acoustic modes.

Time-resolved Raman scattering has been used in the past to measure nonequilibrium phonon effects during ultrafast photoexcitation and to directly measure the anharmonic phonon decay time through the time dependence of the anti-Stokes line (which is proportional to N_q, the phonon population at the relevant phonon wave vector). Measurement has been reported for a variety of III–V compound bulk and quantum well materials [146–149], where typical anharmonic decay times are in the 1–10 ps time scale. The UNSW group has argued that nonequilibrium "hot" phonons may play a critical role in reducing carrier energy loss in hot carrier solar cells, allowing for high electron/hole temperatures in the absorber. Engineering materials as absorbers with long phonon decays (phononics), both in the bulk and in nanostructured structures, are currently being investigated [150, 151].

Ensemble Monte Carlo (EMC) simulation as described in Sect. 19.8.2 has been used to simulate ultrafast carrier dynamics and nonequilibrium phonons in quantum well materials [152, 153], where hot phonon effects have been shown to lead to substantial reduction in carrier cooling. Figure 19.40 shows the simulated effect of phonon lifetime on carrier relaxation using EMC simulation, similar to earlier work on this topic [135, 144, 154]. In these simulations, electrons are injected via a 200-fs-wide 2 eV laser pulse within a 10 nm GaAs/AlAs QW. The injected carrier density is $5 \times 10^{11}/\text{cm}^2$ in all cases and the lattice temperature is 5 K. In Fig. 19.40, the simulated carrier temperature versus function of time is plotted, assuming different anharmonic phonon decay times, ranging from 0 (i.e., no hot phonons) to 100 ps.

Without hot phonons, the electrons cool rapidly and decay to the lattice temperature within ~5 ps. As the phonon lifetime is increased, the decay slows and starts to be governed by the anharmonic decay time rather than the electron-phonon emission rate. The effect is strongly density dependent, similar to experiment, since a higher injected density leads to a higher nonequilibrium phonon population, which increases the strength of the hot phonon effect. Hence, finding absorber

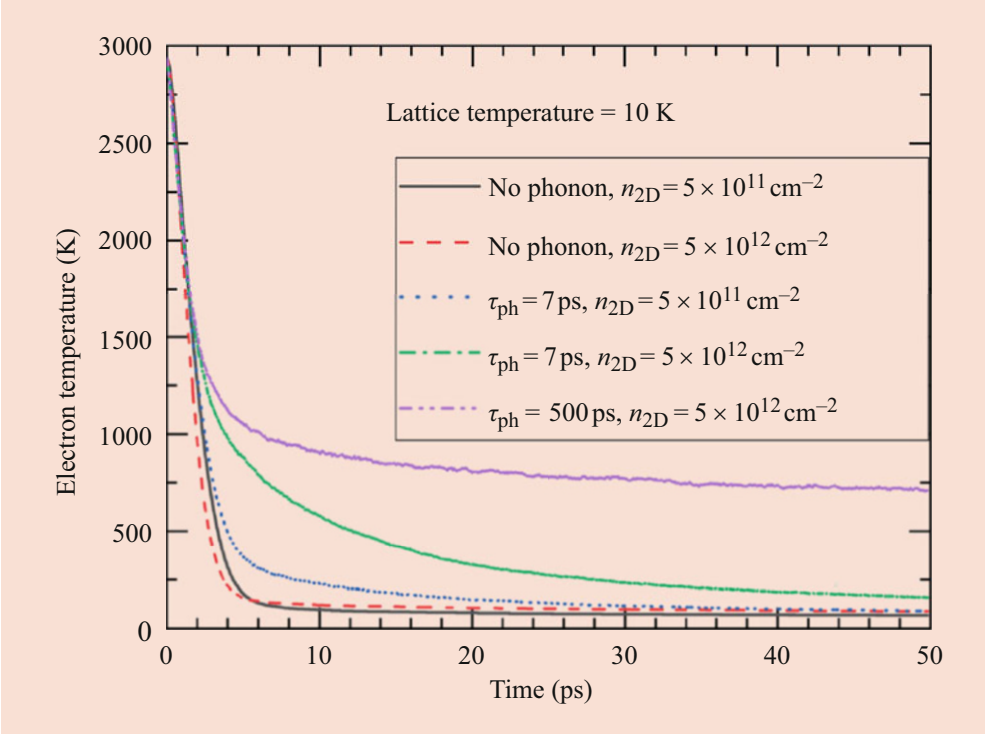

Fig. 19.40 EMC simulation of the electron temperature versus time in a 10 nm GaAs/AlAs QW for different phonon anharmonic decay times

materials with long phonon lifetimes is a possible approach to realizing hot carrier solar cell performance.

19.9 Summary

In this review chapter, we have discussed the state of the art with respect to photovoltaic device technology. We started with an overview of the fundamentals of solar cell device operation, and the nature of the solar energy spectrum and its absorption by the device. We then went into detail into the basics of solar cell operation, and what limits the main figures of merit, the open circuit voltage, short circuit current, and fill factor, where a particular emphasis was given on the role the minority carrier recombination plays. Methods of reducing such effects through passivation and carrier selective structures such as heterostructures were also introduced. We then provided an overview of the main technologies and their reported efficiencies starting with Si wafer-based technology and GaAs, then thin film technology, and organic solar cells, ending with recent developments of perovskite-based solar cells which are a hybrid of organic and inorganic cell architectures.

We then provided a synopsis of the limits of solar cell performance, and the use of detailed balance to derive the Shockley-Queisser limit for single junction cells. Methods of circumventing this single gap limit were discussed, which set the stage for discussing multijunction or tandem solar cells which currently hold the record for highest conversion efficiency in any solar technology, greater than 46%. We then discussed how nanotechnology may play a role in realizing other ways of circumventing the SQ limit in terms of advanced concept architectures. Nanotechnology is playing an increasing role in improving existing devices, as well as new device architectures seeking to improve efficiency while seeking lower cost. We discussed how, for example, nanostructures are playing an increasing role in improving light management in solar cells to improve light collection and allow thinner materials to be used reducing cost. Nanostructured materials play a central role in device architectures such as the dye-sensitized solar cell, which in turn became the basis for perovskite solar cells, which have rapidly overtaken thin film technology in terms of efficiency and approach that of crystalline Si solar cells. Nanowire solar cells have also shown tremendous improvement in recent years, with efficiencies over 15%. Research continues on realizing advanced concept solar cell structures such as multiexciton generation and hot carrier solar cells, and recent results show continued improvement in the design and architectures of such systems.

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X-Ray Detectors

20

Safa Kasap and Zahangir Kabir

Contents

20.1 Introduction and Fundamental Concepts 747
20.2 X-Ray Spectroscopic Detectors 752
20.3 Flat Panel X-Ray Image Detectors 754
20.4 Signal and Noise 758
20.4.1 Responsivity 758
20.4.2 Signal and Linearity 762
20.4.3 Noise Sources in the Detector 763
20.5 Image Resolution 765
20.6 Detective Quantum Efficiency (DQE) 767
20.7 Pixelated Detectors and Small Pixel Effect 769
20.8 Image Lag and Ghosting 769
References 770

Abstract

The basic principle of operation of an x-ray detector is described through the Shockley-Ramo theorem, and the ionization energy, i.e., electron and hole pair creation energy, is introduced and used in formulating the responsivity of the detector. Typical detector materials and structures are also described. The spectroscopic detector operation is explained and its resolution is discussed. One of the most extensive modern applications of semiconductor detectors is in medical x-ray imaging. Flat panel x-ray imagers (FPXIs) are described in detail due to their extensive use in imaging. In direct conversion (DC) FPXIs, the absorbed x-ray photons are directly converted to charges in the pixel's photoconductor. The applied field then drifts them to the collecting electrodes of the pixel. These FPXIs use either a thin-film transistor (TFT) active matrix array (AMA) on a glass substrate, based on a-Si:H technology or, in a smaller area, CMOS (complementary metal oxide semiconductor), CCD (charge-coupled device), or ASIC (application-specific integrated circuit) silicon chips as the sensor to read the image. The image is a charge distribution on the pixels of the TFT-AMA/CMOS. The TFT-AMA and CMOS are currently the most popular with larger size detectors based on the TFT-AMA sensor. A semiconductor, such as a-Se, HgI_2, and CdZnTe, is used with these readout technologies as the photoconductive medium. The current competition between TFT-AMA and CMOS sensors discussed and the advantages and disadvantages of various semiconductors are highlighted. Present DC FPXI principles are reviewed, important physical phenomena are underlined, and the sensitivity, responsivity, linearity, signal-to-noise ratio, noise sources, and resolution, in terms of modulation transfer function, detective quantum efficiency, and lag and ghosting properties of FPXIs, are examined and explained with examples and extensive references where details can be found.

Keywords

x-ray detector · Photoconductor · Flat panel x-ray imager · Direct conversion · Imaging detector · x-ray spectroscopy · Sensitivity · Detective quantum efficiency · Electronic noise · Resolution · Modulation transfer function · Small pixel effect

20.1 Introduction and Fundamental Concepts

X-rays have photon energies ranging from a few hundred eVs (electron volts) to a few hundred keVs, from soft to

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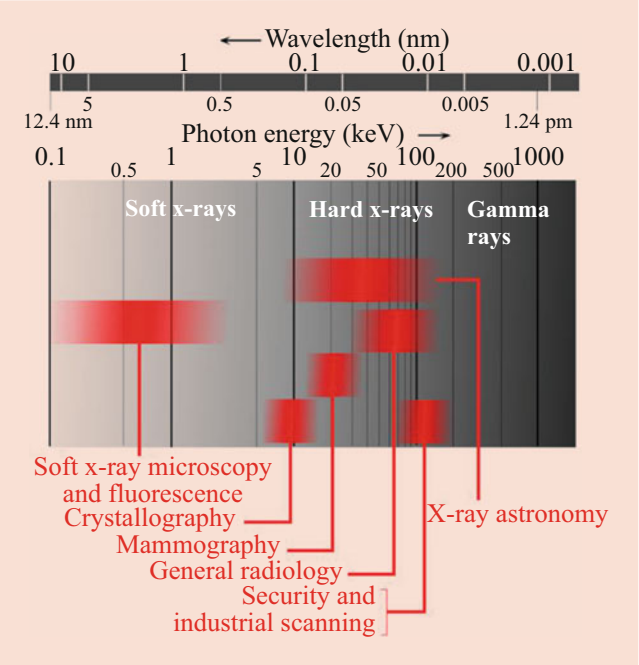

Fig. 20.1 The x-ray spectrum and applications over various spectral regions

hard x-rays, as shown in Fig. 20.1. Various modalities of medical x-ray imaging cover photon energies from roughly 10 keV up to 150 keV, whereas crystallography typically uses x-ray photons of energy roughly around 10 keV, and security scanning such as those at airports use hard x-rays, typically 80–160 keV. Soft x-ray microscopy and fluorescence spectroscopy cover approximately the range 0.1–3 keV and involve the imaging and compositional analysis of microstructures, including biological specimens. The whole x-ray range from 0.1 to 150 keV has a multitude of applications that require various specialized detectors.

Semiconductor x-ray detectors are among the most important class of detectors for detecting and measuring this type of radiation. These semiconductor detectors do more than just detecting and measuring radiation because, in the form of arrays, they can be used as imaging detectors and capture x-ray images, one of the most important applications of semiconductor detectors. Figure 20.2 shows a simplified functional classification of semiconductor x-ray detectors, which involves the measurement of dose, x-ray energy spectrum, and x-ray imaging in the form of arrays. The latter class of imaging detectors is probably the most important application that has experienced unmatched growth in the last two decades, which will be described in detail in Sect. 20.3 and thereafter.

The measurement of dose using a semiconductor detector is a well-established practice, and there are several semiconductor materials that are currently used for this purpose as summarized in Table 20.1. The measurement of the x-ray spectrum is more complicated because the detector must be able to measure the energy of the absorbed x-ray photon and needs to have external electronics to discriminate between different amounts of charge generated inside the semiconductor by different energy individual x-ray photons.

Consider a high resistivity semiconductor that is electroded and biased as shown in Fig. 20.3a. The electrodes do not inject carriers but allow excess carriers in the sample to leave and become collected by the battery so the dark current is negligible. The field F in the sample is uniform and $F = V/L$. This situation is almost identical to the intrinsic region of a reverse biased *pin* photodiode as depicted in Fig. 20.3b in which the p^+ and n^+ doped layers are very thin, the intrinsic (i-) layer is wide, and the detector is reverse biased. We are interested in the external current $i_{ph}(t)$ and the charge collected Q_c (the integration of $i_{ph}(t)$) when an x-ray photon is absorbed in the detector. When a single x-ray photon is absorbed at a position x from the left electrode as in Fig. 20.3a, it instantly creates N electron and hole pairs (EHPs) by the ionization of the medium. Consider initially only one pair of electron and hole. The electron and the hole drift in opposite directions with respective drift velocities $v_e = \mu_e F$ and $v_h = \mu_h F$, where μ_e and μ_h are the electron and hole drift mobilities, respectively. The transit time of a carrier is the time it takes for a carrier to drift from its generation point to the collecting electrode. The electron and hole transit times t_e and t_h, respectively, are marked on the t vs x diagram in Fig. 20.3c where

$$t_e = \frac{L - x}{v_e} \quad \text{and} \quad t_h = \frac{x}{v_h} \tag{20.1}$$

The external photocurrent $i_e(t)$ due to the drifting of the electron is given by the Shockley-Ramo theorem [1, 2], i.e.

$$i_e(t) = \frac{ev_e}{L}; \quad t < t_e \tag{20.2}$$

The simplest derivation of Eq. (20.2) for the present geometry involves equating the work done in moving the electron a distance dx ($= v_e\, dt$) in time dt to the energy delivered by the battery over the same time dt, which is $i_e\, V\, dt$ and taking the field $F = V/L$. Note, however, that strictly the field cannot be totally nonuniform because the injected charges modify the field at the electrodes. It is this change in the field, however small, at the electrode that actually draws carriers and results in an external current.

This current continues to flow while the electron is drifting, which is for a duration t_e, at the end of which the electron reaches the positive terminal of the battery. Thus, although the electron has been photogenerated almost instantaneously, the external photocurrent is *not* infinitesimally short and has a time spread of t_e as shown in Fig. 20.3d, i.e., it is a "pulse."

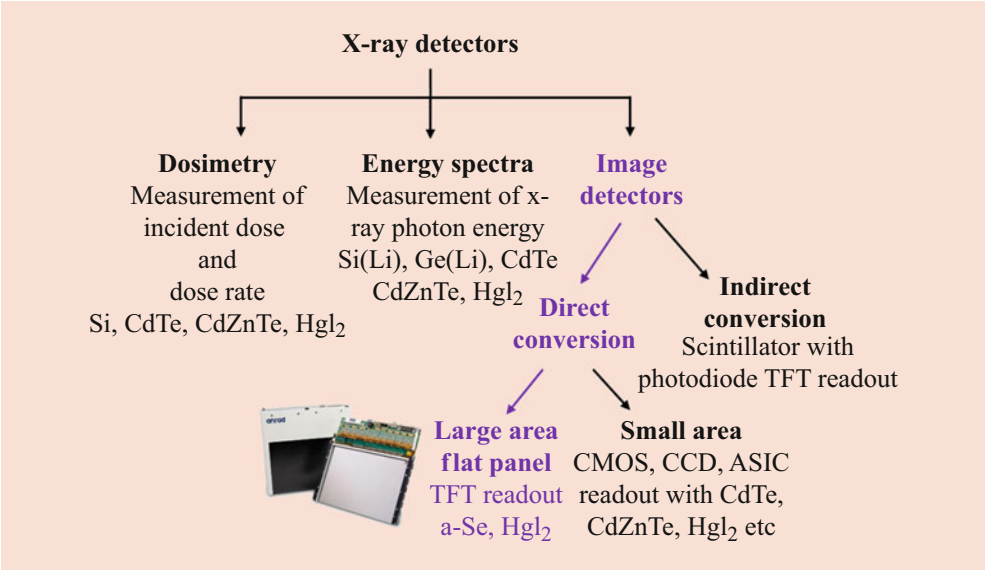

Fig. 20.2 A simplified classification of x-ray detectors. The highlighted branch is the emphasis in this chapter

Table 20.1 Selected examples of *single-crystal* semiconductors for use in x-ray detectors for the measurement of dose or energy spectra

Semiconductor (Z)	Detector type	Density (g cm^{-3})	E_g (eV)	W_i (eV)	F_N	Comments
Si (14)	*pn*, *pin*, or Schottky junction	2.33	1.12	3.62 (300 K) 3.77 (77 K)	0.08–0.13	Reverse biased to widen the depletion region. Can be used at room temperature. Used in various semiconductor detector probes in dosimetry
Si(Li) (14)	*pin*-like with an "intrinsic"-like region					Li doped Si *pn* junction behaves like *pin*. Operation needs cooling (e.g., liquid nitrogen) to prevent Li drift. Various commercial products
Ge Ge (Li) (32)	*pin*-like, metal/HPGe/metal	5.33	0.72	2.96	0.06–0.11	77 K values. Must be cooled. Can measure 0.3 keV to 3 MeV. Commercial spectroscopic detectors with high resolution
CdTe (48/52)	Schottky, *pin*, and photoconductive	5.85	1.44	4.43	0.06–0.09	Commercial room temperature spectroscopic detectors. $\mu_e\tau_e \approx 10^{-3}$ cm^2/V, $\mu_h\tau_h \approx 10^{-4}$ cm^2/V
CdZnTe (48/30/52)	Schottky and Photonductive	5.8	1.57	4.64	0.10	Commercial room temperature spectroscopic detectors. $\mu_e\tau_e \approx 3 \times 10^{-2}$ cm^2/V, $\mu_h\tau_h \approx 10^{-5}$ cm^2/V
HgI_2 (80/53)	Metal/HgI_2/metal	6.4	2.15	4.2	0.12	Small size detector. Room temperature spectroscopy. $\mu_e\tau_e \approx 3 \times 10^{-4}$ cm^2/V, $\mu_h\tau_h \approx 10^{-5}$ cm^2/V

E_g is the bandgap and W_i is the ionization energy. If the detector type is not fully known, metal/semiconductor/metal is shown. HPGe is high purity Ge. Data are typical values quoted in the literature as in [9, 25]. (F_N is difficult to measure and also has an energy and temperature dependence so the values are only estimates)

Similar arguments can also be applied to the drifting hole, shown in Fig. 20.3a–d, which generates a hole photocurrent $i_h(t)$ in the external circuit given by

$$i_h(t) = \frac{ev_h}{L}; \quad t < t_h \tag{20.3}$$

The total current in the external circuit is the instantaneous photocurrent, $i_{ph}(t)$, and is the sum of $i_e(t)$ and $i_h(t)$ as shown in Fig. 20.3e. If we integrate the external photocurrent $i_{ph}(t)$, as in Fig. 20.3f, to evaluate the collected charge $Q_c(1)$, due to the generation of one EHP at x, this would be

$$Q_c(1) = \int_0^{t_e} i_e(t)\,dt + \int_0^{t_h} i_h(t)\,dt = e \tag{20.4}$$

Thus, one e of charge is collected in the external circuit per EHP generated in the semiconductor, even though both the electron and hole drift inside the medium. Notice that

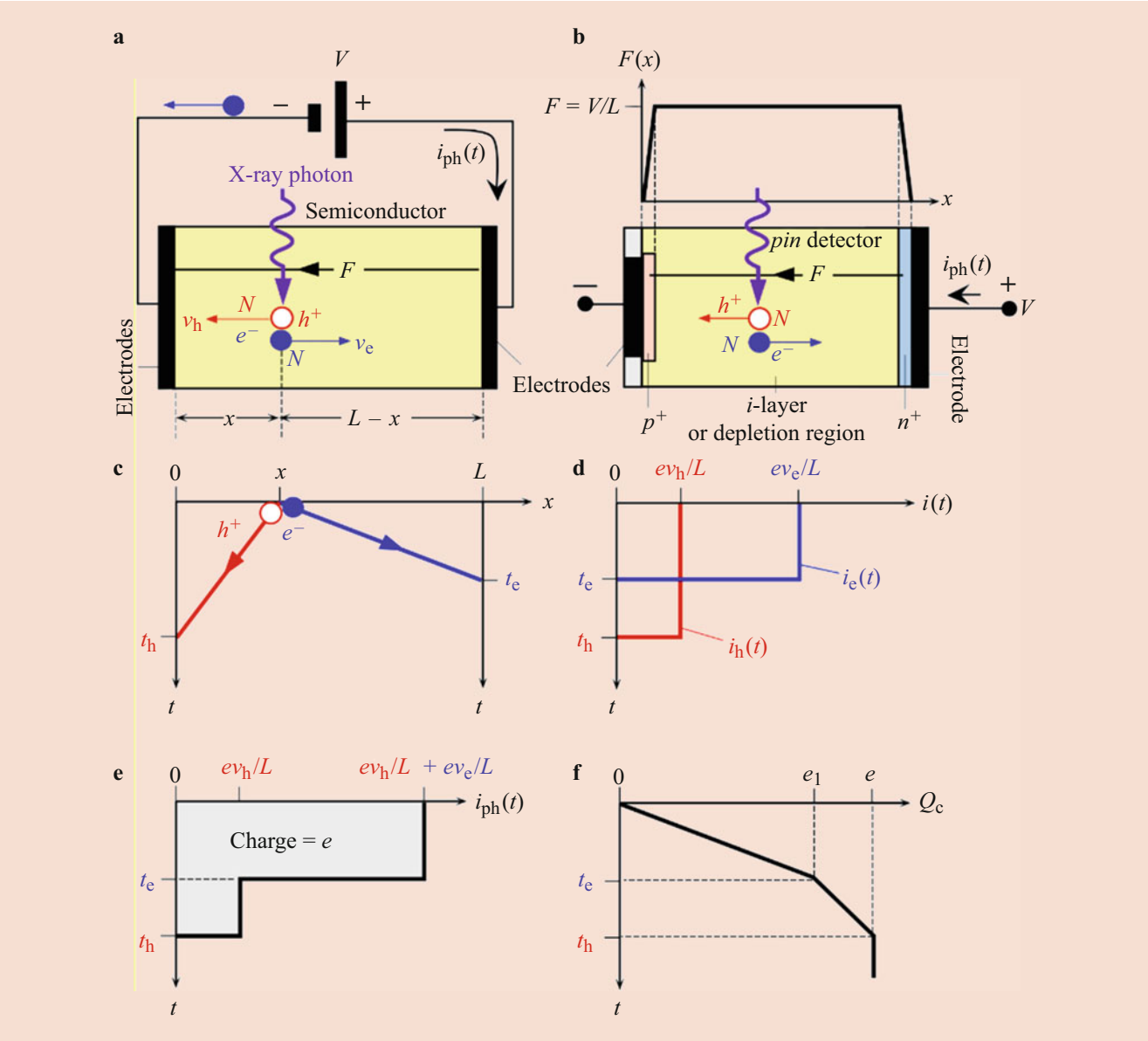

Fig. 20.3 (**a**) An electron and hole pair (EHP) is generated at position x. (**b**) The same photogeneration in an ideal reverse biased *pin* detector in which the n^+ and p^+ sides do not inject carriers; they effectively serve as noninjecting contacts. (**c**) The electron and the hole drift in opposite directions with drift velocities v_e and v_h, respectively. The electron arrives at time $t_e = (L–x)/v_e$ and the hole arrives at time $t_h = x/v_h$. (**d**) As the electron and hole drift, each generates an external photocurrent shown as $i_e(t)$ and $i_h(t)$. (**e**) The total photocurrent is the sum of the hole and electron photocurrents. (**f**) The instantaneous collected charge as a function of time. Eventually at time $t = t_h$, $Q_c = e$

when the electron reaches the positive electrode, the collected charge is $e_1 < e$ because we still have the drifting hole left, which must reach the negative electrode to yield a total collected charge of e. With N EHPs generated at x, the collected charge Q_c is then simply eN. In the presence of trapping, not all the x-ray ionized charge $Q_i = eN$ is collected and $Q_c < Q_i$. This is accounted by introducing a charge collection efficiency as described in Sect. 20.4.1.

Since N EHPs per absorbed x-ray photon result in a collected charge of $Q_c = Q_i = eN$, the only issue becomes relating Q_i (or N) to the energy of the absorbed x-ray photon and hence to the absorbed dose, which can be related to the incident dose. Suppose that an amount of energy $E_{absorbed}$ is absorbed from an incident monochromatic x-ray radiation. This may correspond to one x-ray photon or many. The conversion of this absorbed energy to electrical charges is gauged by a quantity known as the ionization energy W_i or the electron and hole pair (EHP) creation energy. (Also written as $W_\pm$ and W_{EHP}.) The absorbed x-ray photon first knocks out a projectile primary electron from an inner K or L shell. The latter primary electron interacts with the medium along its track and ionizes the medium to generate EHPs. Suppose that

N of these EHPs can escape from the track and then drift to the collection electrodes without experiencing any trapping or recombination, that is, there is no loss of carriers during bulk transport. These N electrons and N holes correspond to a charge of Q_i in the external circuit. The definition of W_i is the average energy absorbed from the radiation in creating one EHP

$$W_i = \frac{E_{absorbed}}{N} = \frac{E_{absorbed}}{Q_i/e} \tag{20.5}$$

The reciprocal of W_i is a measure of the x-ray photogeneration efficiency. The usefulness of W_i lies in the fact that this quantity for most semiconductors is a material constant that is related to the bandgap (E_g) and practically independent of the photon energy (over typical x-ray energies). Thus, once it is measured and known, the conversion efficiency from x-rays to charges is then a known quantity, and therefore the dose measurement becomes straightforward. The energy of the photon can also be inferred from Q_i, but one has to avoid photon pileup to ensure the measured Q_i corresponds to a single absorbed photon, in which case Q_i represents the energy of the x-ray photon as explained in Sect. 20.2.

The ionization energy W_i of various semiconductors has been studied as a function of photon energy and the applied field, and in nearly all crystalline semiconductors, W_i depends on the bandgap E_g through a relationship of the form

$$W_i = cE_g + W_{phonon} \tag{20.6}$$

where c and W_{phonon} are constants, as reviewed in [3]. Shockley's early semiquantitative arguments made $c = 2.2$ and W_{phonon} equal to the product of the average number of optical phonons and the average optical phonon energy involved in the ionization process per EHP [4]. The Klein relationship [5] makes $c = 2.8$ and casts Eq. (20.6) into $W_i = 2.8E_g + W_{phonon}$ where W_{phonon} is on the order of 0.1–0.5 eV, which supports the empirical rule that $W_i \approx 3E_g$ [6]. Table 20.1 also lists W_i values for a number of crystalline semiconductors where it can be seen that the Klein rule holds well for Si, only approximately for Ge, CdTe, and CZT, but not for HgI_2 (see [3]).

It should be apparent from the discussion above that the EHP creation in Fig. 20.3a, b should occur in the region of the semiconductor where there is a strong field to separate and drift the carriers to the collection electrodes and the sample geometry must allow the absorption of the incident radiation. Detectors based on the *pn* junction or a Schottky junction are reverse biased to ensure the depletion layer width should be as wide as possible because the electric field is actually within the depletion region. The reverse bias is normally such that it almost depletes the whole semiconductor by widening the depletion region. Recall that the depletion region is in the semiconductor side for a Schottky junction and on the n-side in a p^+ n junction. The field in the depletion region is not constant, and hence *pin* devices are preferred not only because of their wider i-layer, or depletion layer width, but due to a relatively uniform and large field one can achieve in this layer. The i-region of a perfect ideal *pin* detector would be intrinsic, but generally there is always some doping in this region so it is a depletion region rather than a true i-region, and with reverse bias, the depletion region stretches fully between the p^+ and n^+ thin layers. The result is that the electric field is not exactly constant but has a gradient that represents the ionized dopants in the region, that is, if ρ_I is the net space charge density due to ionized dopants, $dF/dx = \rho_I/\varepsilon_o\varepsilon_r$.

Lithium doped Si detectors, Si(Li) (pronounced "silly"), are among various commercial detectors used in x-ray detection and spectrometers. Li is an interstitial donor in Si so a *pn* junction made by doping a p-Si crystal with Li would result in a *pn* junction. The Li atoms become Li^+ and can be drifted by an applied field deep into the p-side. The p-side has ionized acceptors (e.g., B^-), but in the region of acceptors and Li^+ ions, there is no net space charge, and the device resembles a *pin* detector. Once formed by drifting the Li^+ ions, the Si(Li) detector has to be operated at low temperatures. A Si detector without Li doping can be operated at room temperature.

A few selected compound semiconductors such as CdTe, CdZnTe ($Cd_{0.92}Zn_{0.08}Te$ – $Cd_{0.9}Zn_{0.1}Te$), and HgI_2 are already used as x-ray and γ-ray spectroscopic detectors. They do not need cooling and can be used at room temperature, which is a distinct advantage. Their properties have been extensively reviewed in literatures [7–15] and in recent books [16, 17] and chapter [18]. Smaller bandgap semiconductors such as Ge have a higher intrinsic concentration and thus a higher dark current, which adds noise to the signal. Both Ge and Ge(Li) are operated at low temperatures, e.g., 77 K, to keep the dark current small and avoid Li drift instability in Ge(Li) detectors. Table 20.1 summarizes the properties, including W_i, of a few selected single-crystal semiconductors for use in x-ray radiation detection and/or spectroscopy. It can be seen that the compound semiconductors CdTe and CdZnTe and HgI_2 can be operated at room temperature. Operation at lower temperatures improves the performance. There are many experimental semiconductors that are not listed, which have good commercial potential. For example, GaAs *pin* x-ray detectors for spectroscopy have been demonstrated [19]. GaAs arrays have been also demonstrated for x-ray spectroscopy with high resolution [20]. SiC is another possible x-ray detector material that has favorable properties for x-ray spectrum measurements and can be used in harsh environments [21, 22]. Owens and Peacock provide a comprehensive review and several tables of properties for a large number of potential x-ray detector materials, though their emphasis is on spectroscopic detector application [7]. A recent extensive review of semiconductors for x-ray detec-

tor applications, including tables of properties, growth and characterization, and detector principles, can be found in Owens' recent books [16, 17] and chapter in [18].

The advantage of using a reverse biased *pin* detectors is that under reverse bias, the p^+-layer and n^+-layer do not inject carriers into the *i*-layer and the only current in the dark is due to thermally generated EHPs in the *i*-layer. Any carrier injection from the p^+-layer and n^+-layer into the *i*-layer is due to diffusion of minority carriers (e.g., minority carrier electrons in the p^+-layer diffusing into the *i*-layer) which is small as the gradient is very small [23]. The contact behavior of the electrodes to the n^+-layer and p^+-layer is assumed to be ohmic so they do not limit the current flow in either direction. Reverse biased *pn* junction behaves similarly in that there is no carrier injection in the dark into the depletion region and again the dark current is due to the thermal generation of EHPs in the depletion region. The reverse current in the Schottky junction is the emission of carriers from the metal over the Schottky barrier height (Φ_B) into the semiconductor, e.g., electrons from the metal into the conduction band for a metal/*n*-type Schottky junction. The reverse biased Schottky, *pn*, or *pin* junctions enable noninjecting contacts to be made to a semiconductor and thereby reduce the dark current. It is also possible to employ back-to-back Schottky junctions so that under bias one junction is always reverse biased to limit the current. These metal-semiconductor-metal Schottky junction detectors operate as photoconductive detectors. If a semiconductor has a sufficiently high resistivity, the detector resistance may be sufficiently high for it to be usable as an x-ray detector, i.e., the dark current may be sufficiently small. In such cases, the semiconductor need not have noninjecting contacts. The importance of contacts to semiconductors has been well-recognized in photodetector work and discussed in the literature, e.g., [16, 17, 24].

The discussion above has ignored two important factors that are needed to relate the actual collected charge Q_c to the incident radiation dose (not absorbed dose) or incident exposure. First is that not all incident x-ray photons will be absorbed, only a fraction determined by the quantum efficiency of the detector as described in Sect. 20.4.1. Second, not all carriers can drift and reach the collection electrode. Some carriers become trapped or recombined. The collected charge is then less than Q_i, i.e., $Q_c < Q_i$. This is represented by a factor called the charge collection efficiency and is also described in Sect. 20.4.1 The responsivity, i.e., the sensitivity, and the signal-to-noise performance of an x-ray detector are covered in Sect. 20.4.2 inasmuch as the concepts applied to the pixel of an imaging detector also apply to discrete x-ray detector devices, if one excludes the readout related pixel and peripheral electronics. Pixelated detectors such as detector arrays are discussed in Sects. 20.3 and 20.7. The response of a pixelated detector, the so-called small pixel effect, is described in Sect. 20.7 where the differences between the effects of carriers moving toward and away from the pixels are highlighted. Pixelated detectors provide unique advantages by favoring one type of carrier (that moving toward the pixels) over the other, which is also covered in Sect. 20.7. Section 20.2 describes the use of crystalline semiconductors in spectroscopic detectors where the detection system can measure the energy of the absorbed photon.

20.2 X-Ray Spectroscopic Detectors

Photon energy spectroscopy is probably the most important application of crystalline semiconductor detectors mentioned above, especially for x-rays and γ-rays. The basic principle of photon energy spectrum measurements using a semiconductor detector is illustrated in Fig. 20.4. The technique is called pulse height spectroscopy. The basic principles of x-ray spectrum measurements with semiconductor detectors are widely described in radiation detection textbooks such as in references [25–28].

Consider a stream of monoenergetic photons from a radioactive source in which the photon energy is E_{ph}. Photons are sufficiently separated so that one photon at a time is absorbed as in Fig. 20.4. When one of these photons is absorbed, an amount of charge Q_i is generated through the conversion in Eq. (20.5). In the absence of trapping, the external preamplifier in Fig. 20.4 will register a collected charge $Q_c = Q_i$. If the conversion process were identical for each absorbed photon, then there would be no fluctuations in Q_c, and we can infer the exact E_{ph} from Q_c, but the conversion process has its statistics. Put differently, W_i is an average quantity in Eq. (20.5) and has a probability distribution. We can use a pulse shaper after the preamplifier in Fig. 20.4 so that a pulse is generated and the height of the pulse represents Q_c. We can then connect a multichannel analyzer to the pulse shaper output to bin different amounts of charge collected into channels and hence draw a histogram in which the number of occurrences (counts) is plotted against Q_c (the channel number). We can suitably calibrate the measurement system for a known photon energy so that we can convert the Q_c to photon energy E and plot the number of occurrences (counts) against the photon energy E as in Fig. 20.4, which is called a pulse height spectrum. In the ideal case, we would find a Gaussian distribution which has a mean that corresponds to E_{ph}, but the distribution has a finite width ΔE, which is measured as full width between half maximum (FWHM). There are two fundamental reasons for the observed ΔE that are directly related to the semiconductor material.

The conversion process of an absorbed photon to Q_i/e number of carriers has fluctuations; it is also known as x-ray photogeneration variance. It is not simply E_{ph}/W_i but fluctuates about this mean value. If the conversion (the ionization of the medium by the primary electron) was a string

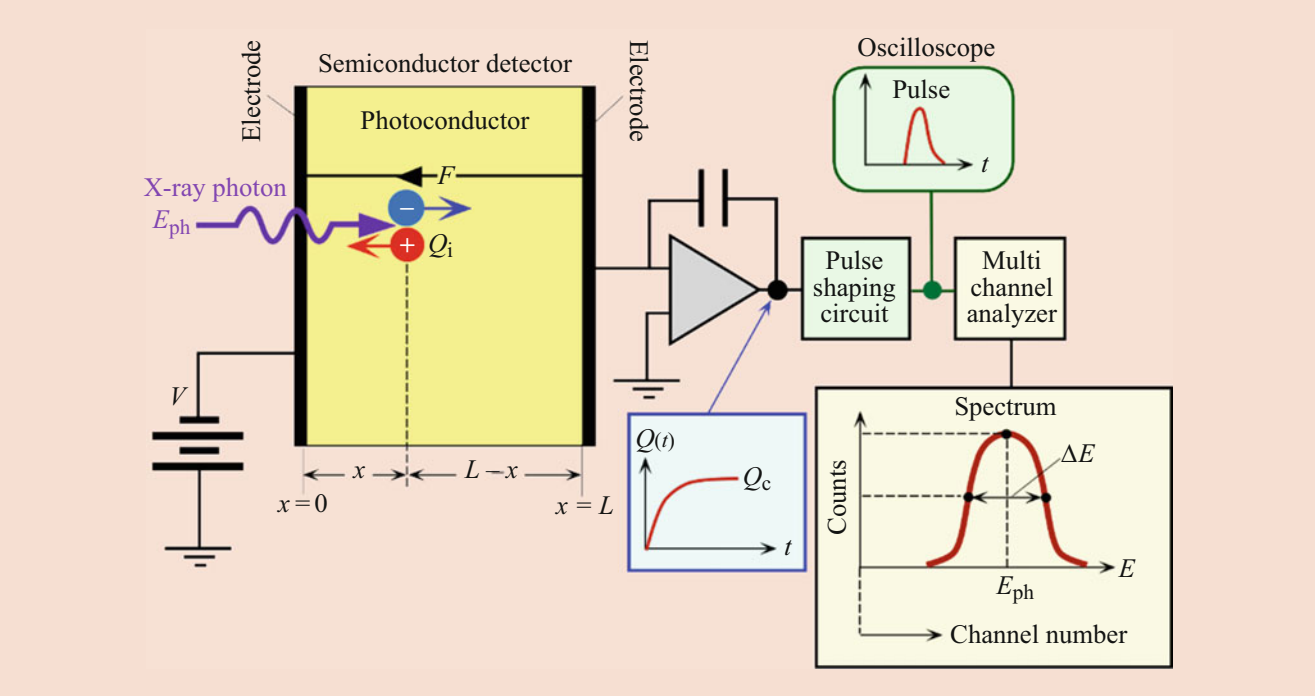

Fig. 20.4 The basic principle of photon energy spectrum measurements using a semiconductor detector. The technique is called "pulse height spectroscopy"

of independent events, the conversion statistics would be a Poisson distribution so that the variance of the conversion process would be Q_i/e and the root-mean-square variation would be $\sqrt{Q_i/e}$. However, in semiconductors, the statistics is modified by a Fano factor F_N [29], discussed in [30], so the variance of conversion is not Q_i/e but $F_N Q_i/e$. If $\Delta E_{conversion}$ is the FWHM in the pulse height spectrum in Fig. 20.4 from the statistics of the conversion process alone, then this would be

$$\Delta E_{conversion} = 2.355\sqrt{F_N E_{ph} W_i} \tag{20.7}$$

The Fano factors for many semiconductors are typically less than 1 and are listed in Table 20.1. $F_N < 1$ is accounted by the fact that EHP creation events in the primary track cannot be totally independent and must be correlated through energy conservation so that the spread in the collected number of carriers is less than that expected from Poisson statistics. A reliable experimental measurement of F_N requires that the photogenerated carriers suffer no trapping (all are collected) and the electronic noise in the measurement circuit is suppressed. F_N is usually inferred from an energy spectrum peak, i.e., ΔE in Fig. 20.4. F_N has been also reported to have an energy and temperature dependence [17].

The second important broadening mechanism is the effect of charge trapping during the drift of the carriers toward their collection electrodes. Those trapped changes are not fully collected as explained in Sect. 20.1 so the measured charge is less than Q_i. The collection efficiency η_{CC} due to charge generation as a point x in the sample is given by the Hecht collection efficiency [31] as

$$\eta_{CC} = \frac{Q_c}{Q_i} = \frac{\mu_e \tau_e F}{L}\left[1 - \exp\left(-\frac{L-x}{\mu_e \tau_e F}\right)\right] + \frac{\mu_h \tau_h F}{L}\left[1 - \exp\left(-\frac{x}{\mu_h \tau_h F}\right)\right] \tag{20.8}$$

where x is the point of generation of charge Q_i (from conversion) (Fig. 20.4); τ_e and τ_h are electron and hole lifetimes, respectively; μ_e and μ_h are electron and hole drift mobilities, respectively; and $\mu_e \tau_e F$ and $\mu_h \tau_h F$ are electron and hole schubwegs, respectively. The carrier schubweg represents the mean distance a carrier drifts before it is trapped or disappears by recombination. There are two intermingled fluctuations in Eq. (20.8): First is that not every photon is absorbed at x so there will be fluctuations in x and hence in Q_c. The absorption probability of a photon along the sample follows an exponential distribution exp $(-\alpha x)$ where α is the linear attenuation coefficient of the medium. Second, charge trapping during drift is a stochastic process, and there will be fluctuations in η_{CC} even if each photon was absorbed exactly at x. The analytical treatment for relating the fluctuations in η_{CC} to a corresponding spectral broadening, i.e., ΔE_{CC}, is not straightforward and may be found in references [32–34]. Semiempirical expressions have

also been suggested that relate ΔE_{CC} to the mean photon energy E_{ph} through a power law dependence [11].

The third contribution arises from the noise associated with the leakage current of the detector and the noise due to the electronic chain, starting with the preamplifier, to the final output. All these noise sources are lumped into a single quantity called the electronic noise and result in a FWHM broadening of $\Delta E_{electronic}$.

The overall width ΔE that is observed is then due to these three processes and can be written as

$$\Delta E^2 = \Delta E^2_{conversion} + \Delta E^2_{CC} + \Delta E^2_{electronic} \tag{20.9}$$

The semiconductor material of choice determines the first two and the electronics the last factor. Owens has reviewed the present semiconductors for radiation detection and spectroscopy and has provided a useful empirical relationship for calculating ΔE [9, 11, 17]; Equation (78) in Chap. 8 in [17] is an empirical relationship for ΔE that used three fit parameters (including the Fano factor) and has the electronic noise $\Delta E_{electronic}$ as input.

The resolution of a spectrometric detector is nominally quoted in terms of the FWHM width ΔE at the photon energy E_{ph}, as shown in Fig. 20.4. Obviously, the smaller is ΔE, the better is the resolution of the detector in discriminating different energy photons. High purity Ge detectors operated at low temperatures have especially high spectral resolution. For example, if the electronic noise can be reduced by special techniques, then a resolution of 345 eV at 59.5 keV or 0.57% is achievable at 100 K [35], though typical quoted values in various tables have been 670 eV at 77 K [17]. Typically, the energy resolution with compound semiconductor detectors at room temperature is approximately 2% or more, but less at low temperatures as discussed in reference [11]. Tables 4, 3, and 9.5 in references [9, 11, 17], respectively, provide the best values that are observed for a range of semiconductors at energies 5.9 keV and 59.5 keV.

20.3 Flat Panel X-Ray Image Detectors

This section and the remainder of the chapter describe the properties and the performance of direct conversion x-ray image detectors utilizing the x-ray photoconductivity of semiconductors. The emphasis is on large area x-ray image detectors that can be used in various x-ray imaging modalities. The last few decades have seen a nearly full transformation of x-ray imaging to modern digital imaging. The hardware for digital x-ray imaging needs a suitable x-ray detector that is capable of capturing and providing the image as an electrical signal [36–38]. The requirements on the detector technology have become more and more demanding as medical x-ray imaging today is not only about projection imaging but involves real-time imaging (fluoroscopy) and tomosynthesis, among other imaging enhancements such as dual energy imaging, photon counting, etc., each of which has its own demands on the detector technology [39–46]. The focus of this chapter is on semiconductor-based direct conversion flat panel x-ray imagers (FPXI), in which a semiconductor acts as a photoconductor and converts the absorbed x-ray photons to collectable charges [47]. A comprehensive and detailed review of flat panel image detectors, both direct and indirect, has been given by Rowlands and Yorkston [48]. Outside medical imaging, direct conversion imagers have shown potential for a number of applications from materials science (crystallography) to nondestructive testing and inspection [49–51].

In one of the most common types of FPXI, the basic readout of the signal is based on an active matrix array (AMA). AMA is a two-dimensional large array of pixels as shown in Fig. 20.5. An AMA is essentially a two-dimensional array of pixels in which each pixel has a thin-film transistor (TFT) that can be externally addressed. Each pixel is configured identically with the TFT gate G_i connected to a particular address line i and the source S_j to a particular data line j. The AMA has $M \times N$ number of gate and data lines, where M and N can be several thousand. The product $M \times N$ determines how many pixels will constitute the image. The intrinsic readout resolution of the detector is determined by the pixel pitch, which is typically 50–100 μm. The TFT array is laid out on a suitable flat rectangular glass substrate and is purchased by the detector manufacturing company as a component onto which the semiconducting photoconductor is coated. The TFT-AMA substrate makes use of the well-established hydrogenated amorphous silicon (a-Si:H) technology for displays.

The AMA substrate is vacuum coated with a photoconductive layer, such as stabilized amorphous selenium (a-Se), as shown in Fig. 20.6. The top surface is then contacted with a suitable electrode to apply a bias voltage, which establishes a field in the photoconductor. Upon the absorption of x-ray photons in the pixel, electrons and holes are generated, and these carriers drift and give rise to an x-ray photocurrent. Each pixel also has a charge storage capacitor C_{ij} as shown in Figs. 20.5 and 20.6. The x-ray photocurrent in the pixel photoconductor accumulates charges on this storage capacitor, and the total charge accumulated Q_{ij} is the signal on the pixel (i,j). Thus, C_{ij} integrates the x-ray photocurrent in the pixel. Although Figs. 20.5 and 20.6 specifically show a-Se, other semiconductors have also been tried. For example, HgI_2 has been coated by screen printing on a TFT AMA to fabricate a FPXI with good performance [53].

The a-Si:H TFT switch shown in Figs. 20.5 and 20.6, when switched on, allows the charge Q_{ij} on C_{ij} to be read out into the external circuit, which has a charge amplifier to amplify the signal toward digitization. Once the gate G_i of

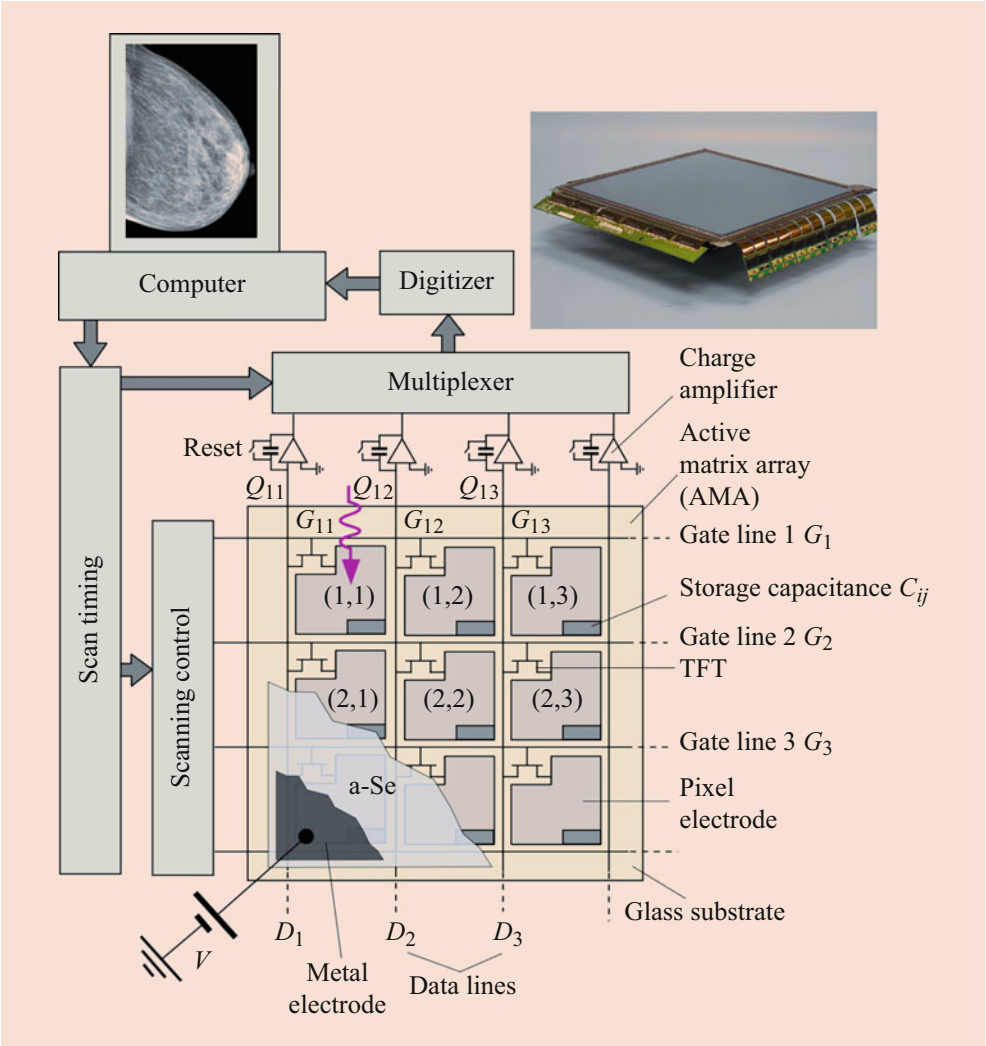

Fig. 20.5 The structure of a typical direct conversion active matrix array-based flat panel x-ray imagers. (Adapted from Kasap et al. [52])

the TFT_{ij} is activated, the TFT_{ij} switches on, and the collected charge on C_{ij} is readout as GQ_{ij} where G is the amplifier gain. The amount of charge Q_{ij} that is generated depends on the incident radiation X_{ij} on that particular pixel (i,j) because the electron and hole pairs generated in the photoconductor is proportional to the total absorbed radiation energy. Clearly, we can represent the x-ray image in terms of the charges Q_{ij} residing on the pixel storage capacitors of the FPXI. Historically, the first demonstrations of a-Se-based FPXIs were reported by Rowlands and coworkers [54–59] and by Lee, Cheung, and Jeromin [60–62] in the mid-1990s. Since those first demonstrations, much research has been done in characterizing and understanding the performance and imaging properties of these a-Se-based FPXIs, for example, as reported in references [63–65]. In hindsight, it should have been obvious that once the TFT-AMA technology was developed for the flat panel display industry, the development of FPXIs would ensue [66].

In the case of small area detectors shown in Fig. 20.2, the basic readout technology is CMOS, CCD, or, alternatively, a particular ASIC (application-specific integrated circuit) pixelated readout chip, with CMOS normally having a larger area among these. Other readout technologies have been also used. In direct conversion, usually an x-ray photoconductor such as CdZnTe crystals are indium bump-bonded (equivalent to "cold welding") to electrodes on a CMOS so that the x-ray generated charges can be fed into the CMOS (see for example [67, 68]). CdZnTe crystals have also been bonded to ASIC readout chips and CCDs again using indium bumps to produce high-resolution detectors for slot scanning x-ray imaging [69, 70]. Direct coating of the CMOS with a photoconductor has also been tried, for example, a-Se directly evaporated onto a defined area of the CMOS [71]. The CMOS chips are then tiled to assemble a full-size mammographic x-ray imager. In recent years, advances have been made in increasing the effective imaging area of

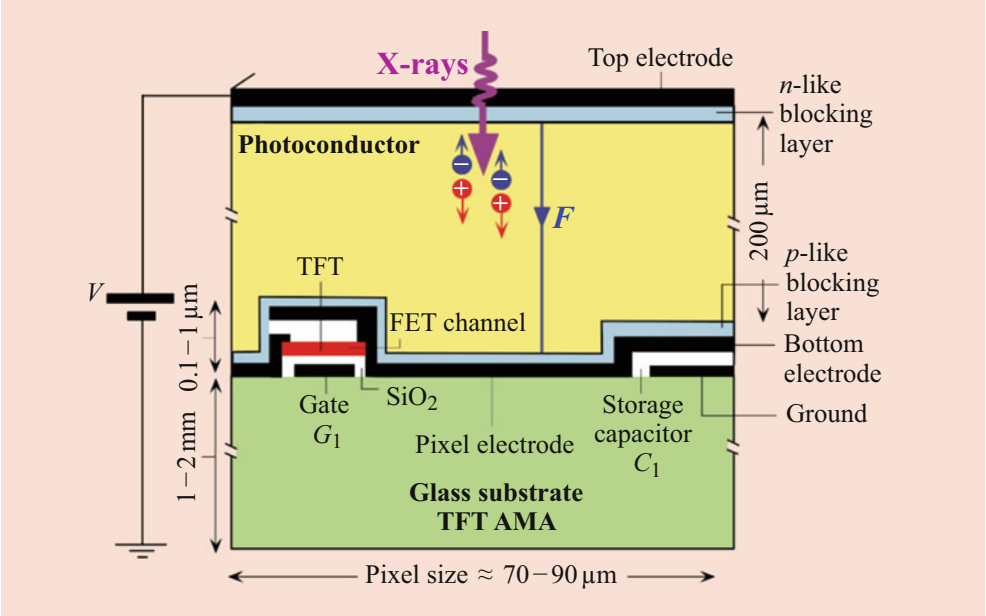

Fig. 20.6 A typical pixel structure of an a-Se direct conversion FPXI

wafer-size CMOS chips through stitching and tiling [72]. In another application, polycrystalline layer of HgI_2 was grown directly on a CMOS chip (10 cm × 10 cm) to construct an x-ray imager [73]. There are several distinct advantages to using crystalline photoconductors on CMOS readout chips. First is that the pixel size can be made very small and the whole operation can be very fast compared to TFTs arrays. The second is that most CMOS imaging chips have on-pixel MOS transistors and achieve on-pixel amplification to improve the DQE. Presently, the largest area commercial CMOS single sensors are about 11 cm × 14 cm and use indirect conversion as described in [74]. Manufacturers such as Dexela and Teledyne DALSA also offer CMOS tiled detectors for specific x-ray imaging applications that include not only medical imaging but also industrial imaging (e.g., nondestructive testing).

As can be seen from Fig. 20.5, the electrode in the pixel does not cover the whole pixel area. It gives the impression that not all the incident x-rays are utilized, that is, the regions outside the collection electrode form "dead zones" that are not involved in the conversion of the absorbed x-rays to the pixel signal charge. The fill factor (FF) of a FPXI quantifies what percentage area of the pixel is actually utilized in capturing the incident radiation and converting it to a signal. FF is the fraction of a pixel that is sensitive to the incident radiation. The apparent geometric FF for the TFT-AMAs used in direct conversion FPXIs depends on the AMA design and the application. Typically FF values are in the range 75–85%. The effective FF, what one observes in imaging characteristics, however, is higher, nearly 100% inasmuch as the field in the dead zone bends toward the pixel electrode and enables x-ray generated charges above the dead zone to be collected [63].

Figure 20.6 shows a schematic cross section of a single pixel with its TFT, storage capacitor, and photoconductive layer. Figure 20.7, on the other hand, shows a simplified equivalent circuit of a pixel. In current commercial FPXIs, the semiconductor of choice for the photoconductive layer is stabilized a-Se. Stabilized means that a-Se has been alloyed with 0.2–0.5% As so as to prevent the crystallization of pure a-Se and then doped with Cl in the ppm amounts to control the charge transport (see [75] and recent review in [76]). The actual photoconductive layer is not a simple single layer but rather a multilayer structure. The pixel detector structure in Fig. 20.6 has thin blocking layers between the photoconductor and the electrodes to prevent charge injection from the contacts to reduce the dark current. The x-ray absorption, the charge generation, and the drift of electrons and holes occur in the thick so-called *i*-like layer in which both electrons and holes are mobile with long carrier ranges. The *i*-layer has electron and hole schubwegs $\mu\tau F > L$, the thickness of the photoconductor, so that hardly any charges are lost. This a-Se *i*-layer in mammographic detectors is about 200 μm thick and absorbs nearly all the incident radiation. There is a thin *n*-like layer between the positive electrode and the *i*-layer. This layer traps holes but allows electrons to drift, i.e., $\mu_e\tau_e F > L > \mu_h\tau_h F$. The *n*-layer has a high percentage of As for stabilization and has been doped with an alkaline dopant. Trapped holes in the *n*-layer modify the electric field profile and reduce the field right at the electrode, which reduces the rate of hole injection and hence the dark current [77]. The thin *p*-layer between the *i*-layer and the negative electrode is

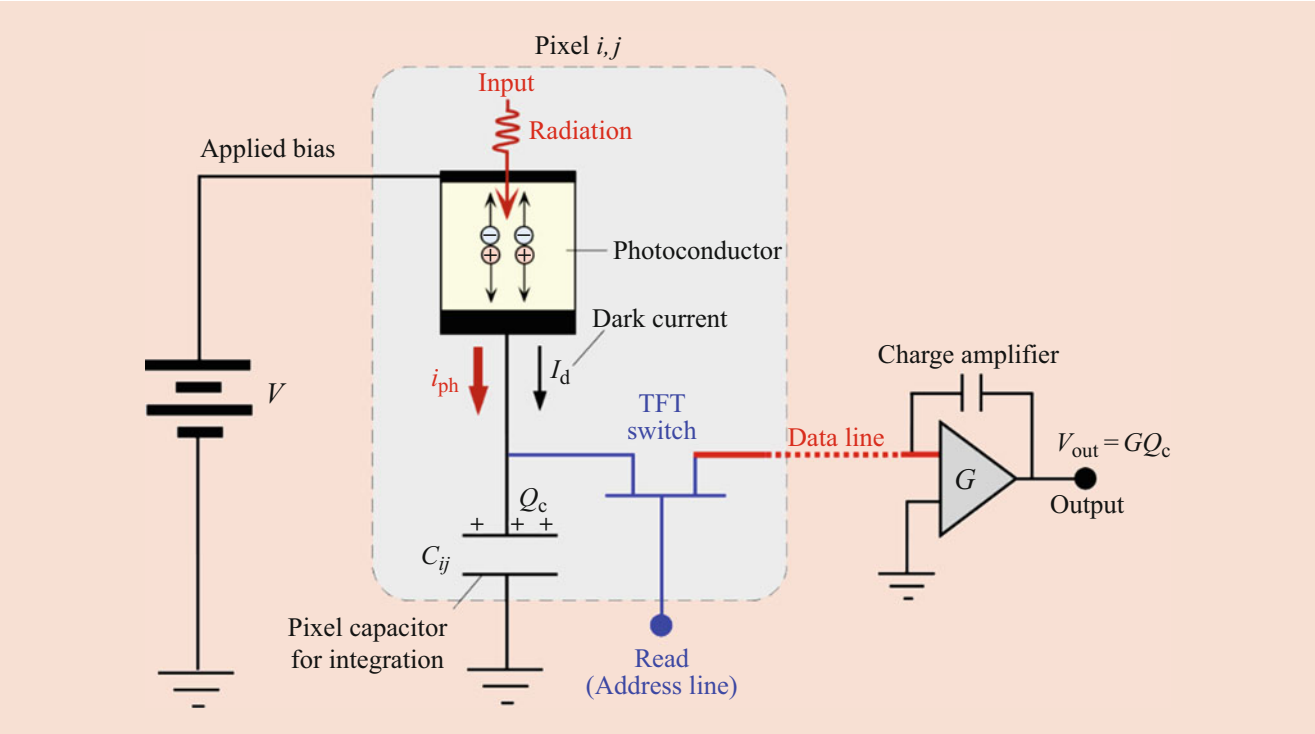

Fig. 20.7 A simplified equivalent circuit of a pixel

an amorphous As_2Se_3 film, which allows hole transport but traps electrons. Trapped electrons in the *p*-layer reduce the field at the negative electrode and hence the rate of injection of electrons from the contact. The *p-i-n* structure was the key to the success of the a-Se-based FPXI because it allowed the dark current to be extinguished to an innocuous level [78–80]. It is important to emphasize that the terminology of *n*-, *i*-, and *p*-layers does not follow the conventional definitions in crystalline semiconductor theory based on electron and hole concentrations or the position of the Fermi level. The terminology in the amorphous semiconductor field is based on the relative magnitudes of the electron and hole ranges, i.e., the $\mu\tau$ values: $\mu_e\tau_e \gg \mu_h\tau_h$ for *n*-type, $\mu_h\tau_h > \mu_e\tau_e$ for *p*-type, and $\mu_e\tau_e \approx \mu_h\tau_h$ for *i*-type.

The imaging properties of a-Se-based FPXIs for various medical imaging modalities have been well-examined and analyzed (see for example [65, 81–89]). There have been a number of other photoconductors, such as polycrystalline layers of TlBr [90, 91], PbI_2 [92–95], HgI_2 [53, 96–108], CdTe [109], CdZnTe [110, 111], PbO [112–116], and various perovskite methylammonium lead halides (MA Pb-halides) [117–121] that have been investigated to replace a-Se. Some of these, in particular HgI_2 and some of the MA Pb-halide perovskites [122, 123], have shown much potential for use in commercial FPXI applications. HgI_2 can be prepared by evaporation or by screen printing, both of which are suitable for large area detector applications. MA Pb-halide perovskites, in polycrystalline form, can be easily and cheaply prepared in large areas from solution (in contrast to vacuum deposition) and have already shown very good performance in photovoltaics and photodetector applications [124]. Their use in x-ray detector applications seems a natural research and development path for this class of materials that can easily absorb x-rays. The basic underlying problem with most of these semiconductors is that either they exhibit an unacceptably large dark current under high fields needed to extract all x-ray generated charges or they do not possess sufficient charge collection efficiency because they need to be operated at a low field to prevent a large dark current [52]. Notice that the electron and hole $\mu\tau$ products for the polycrystalline CdZnTe layers in Table 20.2 are much less than those for the single crystal in Table 20.1. The $\mu\tau$ products have been observed to decrease with the polycrystallinity of the layers, e.g., $\mu_e\tau_e$ in polycrystalline HgI_2 layers decreases with decreasing grain size [104]. In some cases, there are technological problems in manufacturing a homogeneous layer over a large area. Table 20.2 provides a summary of the properties of current photoconductive layers that either are used or have potential for use in large area FPXIs. Material issues related to compound semiconductors for FPXI applications have been reviewed in [52, 125, 126]. The most developed at present is stabilized a-Se with several commercial companies manufacturing and marketing flat panel x-ray image detectors, especially for mammography

Table 20.2 Properties of a few selected large area x-ray photoconductors

Photoconductor State Preparation	δ at 20 keV δ at 60 keV	E_g (eV)	W_i (eV)	Electron $\mu_e\tau_e$ (cm^2/V)	Hole $\mu_h\tau_h$ (cm^2/V)
a-Se Amorphous Vacuum deposition	49 μm 998 μm	2.2	45 at 10 V/μm 20 at 30 V/μm	$3 \times 10^{-7} - 10^{-5}$	$10^{-6} - 6 \times 10^{-5}$
$Cd_{.95}Zn_{.05}Te$ Polycrystalline Vacuum deposition (sublimation)	80 μm 250 μm	1.7	5	$\sim 2 \times 10^{-4}$	$\sim 3 \times 10^{-6}$
HgI_2 Polycrystalline PVD	32 μm 252 μm	2.1	5	$10^{-5} - 10^{-4}$	$10^{-6} - 10^{-5}$
HgI_2 Polycrystalline SP	32 μm 252 μm	2.1	5	$10^{-6} - 10^{-5}$	$\sim 10^{-7}$
PbI_2, Polycrystalline Normally PVD	28 μm 259 μm	2.3	5	7×10^{-8}	$\sim 2 \times 10^{-6}$
PbO Polycrystalline Vacuum deposition	12 μm 218 μm	1.9	8 – 20	$10^{-9} - 5 \times 10^{-7}$	4×10^{-8}
$CH_3NH_3PbI_3$ perovskites Polycrystalline SP	52 μm 365 μm	1.6	5	$\sim 10^{-6}$	$10^{-6} - 10^{-4}$
TlBr Polycrystalline Vacuum deposition	18 μm 317 μm	2.7	6.5	Small	$(1.5–3) \times 10^{-6}$

Data combined from various sources
PVD physical vapor deposition, SP screen printing

[43, 127]. Large area photoconductors for x-ray imaging have been recently reviewed in [128].

20.4 Signal and Noise

20.4.1 Responsivity

Consider a photoconductive detector that is irradiated for a certain duration with an amount of radiation X, which may be measured in grays (Gy) in air or in roentgen. As shown in Fig. 20.7, we can integrate the x-ray generated photocurrent $i_{ph}(t)$ on the pixel capacitance and hence find the collected charge $Q_c = \int i_{ph}(t)\, dt$. The x-ray sensitivity is defined as charge collected per unit incident radiation, $S_x = Q_c/X$. The sensitivity depends on four factors as highlighted in Fig. 20.8, which will be discussed below. Let α be the linear attenuation coefficient of the semiconductor medium and L be the photoconductor thickness. The dependence of α on the photon energy for a few selected semiconductors is shown in Fig. 20.9. Then, the quantum efficiency η_Q in the medical detector field is defined as the fraction of x-ray photons that are attenuated inside the medium as illustrated in Fig. 20.10 (top image) and is given by

$$\eta_Q = 1 - \exp(-\alpha L) \tag{20.10}$$

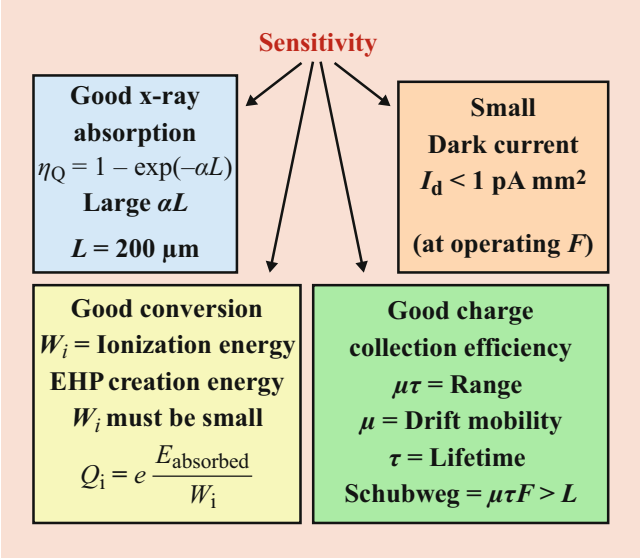

Fig. 20.8 The x-ray sensitivity and the signal-to-noise ratio depend on four factors

The reciprocal of α is the attenuation depth δ ($= 1/\alpha$). It is the depth from the detector surface within which 63% of the incident photons have been attenuated (absorbed or scattered), i.e., $\eta_Q = 0.63$. At a distance of 2δ, i.e., $L = 2\delta$, 86% of the radiation is attenuated. α depends on the x-ray

photon energy and also on the atomic number and density of the medium. The current a-Se mammographic detectors have $L = 200$ μm, so that, as apparent from Fig. 20.9 (or Table 20.2), $\delta \approx 50$ μm at 20 keV, which means that nearly all the incident radiation is attenuated in the photoconductor. At a photon energy of 60 keV, a-Se has $\delta \approx 1000$ μm, which is one of its drawbacks because to attenuate 86% of the radiation we would need a layer that is 2 mm in thickness. To maintain an operating field of 10 V/μm, we would need to apply 20 kV, which has its own practical problems such as eliminating corona discharges. Fluoroscopic a-Se detectors actually use a layer of thickness 1 mm since peak of the x-ray spectrum is at 70 kVp and the average photon energy is roughly 40 keV. From Fig. 20.9, it should be apparent that semiconductors with heavy elements such as CdZnTe, PbO, PbI_2, and HgI_2 have a distinct quantum efficiency advantage over a-Se in the general radiology range (40–100 keV). Perovskites contain lead halides and also exhibit strong x-ray absorption.

Consider a monoenergetic x-ray beam as the input to the detector. Suppose that Φ_0 is the incident photon fluence defined as the number of incident photons per unit area and per unit roentgen of exposure at a given photon energy. $\Phi_0(E)$ is the incident photons per unit area and per unit exposure. The photon fluence $\Phi(x)$ in the semiconductor will decay exponentially with distance, following a $\Phi(x) = \Phi_0 \exp(-\alpha x)$ behavior as shown in Fig. 20.10. In a small interval x to $x + dx$, $\alpha\Phi\, dx$ photons are attenuated, which can be integrated from $x = 0$ to $x = L$ to find the fraction η_Q of the incident photons that are attenuated as in Eq. (20.10). If α_{en} is the energy absorption coefficient of the medium, then the energy absorbed from an attenuated photon of energy E is $(\alpha_{en}/\alpha)E$. If A is the detector area that receives the radiation, then the energy absorbed from attenuated photons is the product of $A\Phi_0$, η_Q, and $(\alpha_{en}/\alpha)E$, which means the total energy absorbed is

$$E_{\text{absorbed}} = A\Phi_o \left[\frac{\alpha_{en}(E)}{\alpha(E)}\right] E\left\{1 - \exp\left[-\alpha(E)L\right]\right\} \quad (20.11)$$

If the input radiation is a spectrum from E_1 and E_2, then Φ_0 needs to be replaced by $\Phi_0(E)\, dE$, which is now defined as the number of photons per unit area per unit exposure in the photon energy interval E to $E + dE$, and then the whole expression on the left in Eq. (20.11) needs to be integrated with respect to E from E_1 and E_2 over the spectrum.

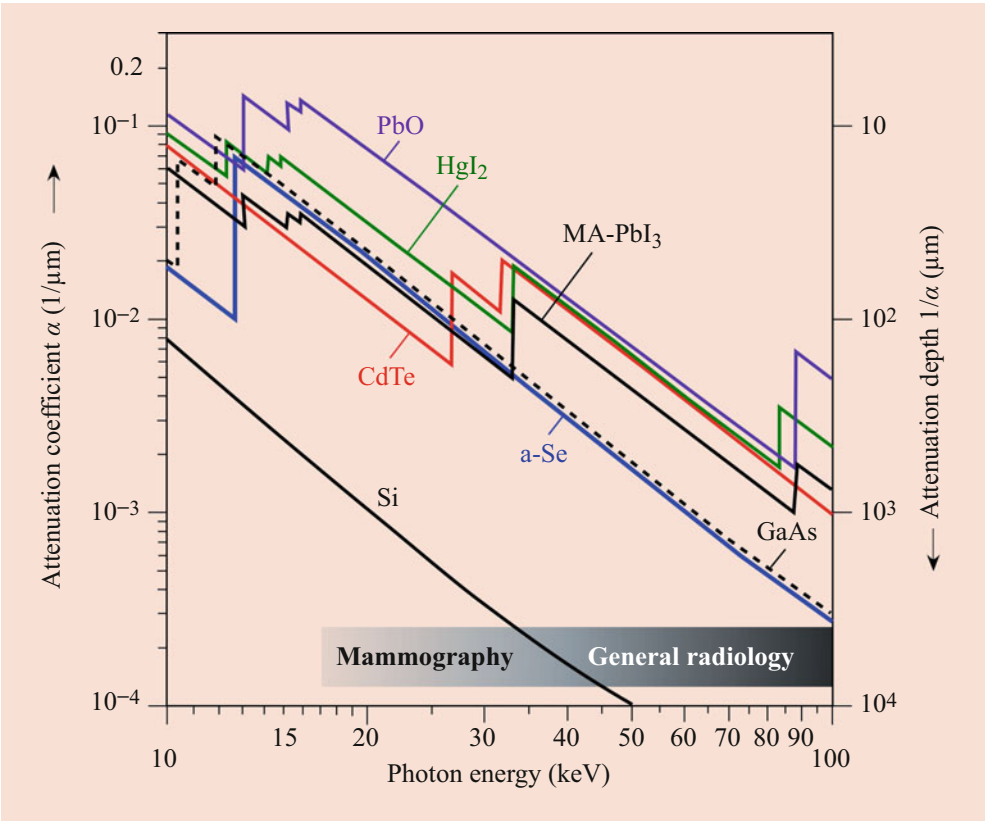

Fig. 20.9 X-ray attenuation coefficient α and attenuation depth $1/\alpha$ for selected semiconductors as a function of photon energy. (The densities of PbI_2, HgI_2, and PbO were assumed to be the same as those for the corresponding single-crystal values, which may not generally be the case inasmuch as the deposited layers would be polycrystalline and likely to have voids)

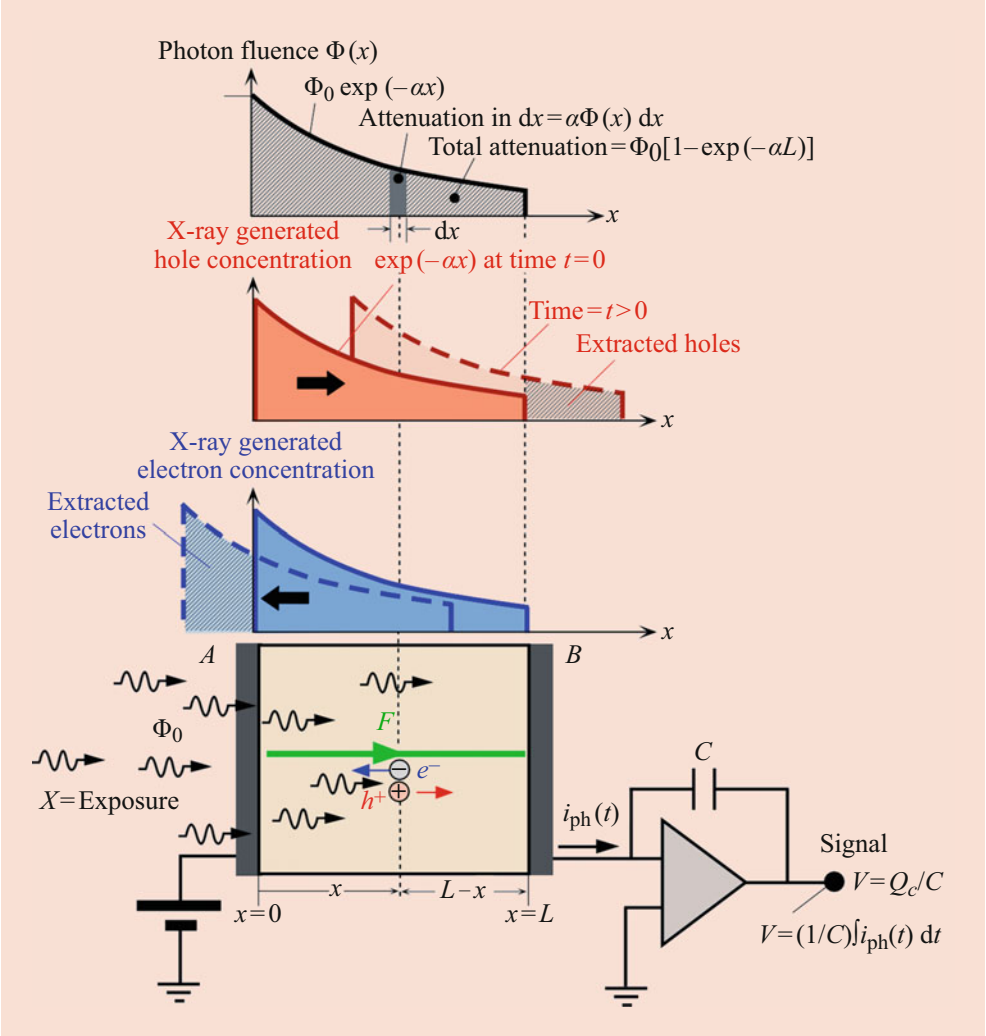

Fig. 20.10 The principle of operation of an integrating x-ray detector. The photon fluence through the sample, hole, and electron profiles at photogeneration ($t = 0$) and at a later time (before collection) and the detector with an electron and hole created at a position x. The signal is the external photocurrent $i_{ph}(t)$ integrated to deliver a charge Q_c which appears as a voltage $V = Q_c/C$

As introduced in Sect. 20.1, the conversion efficiency of the deposited energy $E_{absorbed}$ in Eq. (20.11) to electrical charges is gauged by the EHP creation energy W_i in Eq. (20.5). The charge generated is $Q_i = eN$. If all these N electrons and N holes drift to the collection electrodes (Fig. 20.7) without being trapped or recombined and become collected, then the charge collected in the external circuit by the integration of the photocurrent is Q_i. Thus

$$Q_i = eN = e\frac{E_{absorbed}}{W_i} \tag{20.12}$$

Clearly W_i represents the first step conversion efficiency; some W_i values are listed in Tables 20.1 and 20.2.

As mentioned in Sect. 20.1, the Klein relationship for crystalline semiconductors predicts $W_i = 2.8E_g + W_{phonon}$, where W_{phonon} is on the order of 0.1–0.5 eV. Que. and Rowlands argued that in amorphous semiconductors, one has to relax the **k** vector conservation rule and proposed that $c = 2.2$ in Eq. (20.6) [129]. Crystalline Si has a bandgap of 1.1 eV and a W_i of 3.61 eV [130] which agrees well with the Klein rule since $2.8E_g + 0.5$ eV is 3.58 eV. a-Si:H has a bandgap of 1.7 eV and a W_i that is 3.4–4.4 eV [131], which is much closer to Que and Rowlands rule than the Klein rule. a-Se is an exception to both rules because its W_i is significantly larger than $2.2E_g$ or $2.8E_g$ and depends on the electric field as indicated in Table 20.2 as well as the photon energy [132]. In a recent study, W_i for a-Se was examined up to very large fields (e.g., 80 V μm^{-1}) and found to saturate at about 8–9 eV. A useful empirical relationship for a-Se over typical x-ray diagnostic energies, for fields up to about 30 V μm^{-1} and at room temperature, is $W_i \approx W_{i\infty} + B/F$ where $W_{i\infty} = 6$ eV and $B = 440$ eV/F, where the field is in V/μm [133]. The field and temperature dependence of W_i can be

explained by using Langevin recombination of diffusion and drifting ionized electrons and holes in the primary electron track [134, 135]. (See reviews in [76, 136].)

The electrons and holes photogenerated by the absorbed radiation follow the exponential decay of the photon fluence as shown in Fig. 20.10. For simplicity, assume that the incident x-ray radiation is a very short pulse. The electrons and holes initially have exponential distributions of $n(x,t)$ and $p(x,t)$, and then the latter drift with $p(x,t)$ toward the negative electrode and $n(x,t)$ toward the positive electrode as shown in Fig. 20.10. In the absence of any trapping or recombination in the bulk, the collected charge Q_c would be the same as Q_i. However, we need to consider carriers lost during the drift of N electrons and N holes that are distributed exponentially as in Fig. 20.10 so that Q_c becomes

$$Q_c = Q_i \eta_{CC} = Q_i \eta_{CC}\,(\Delta, x_h, x_e) \tag{20.13}$$

where η_{CC} is a Hecht-type collection efficiency and a function of the ratio $\delta/L = \Delta$ and x_e and x_h are, respectively, the electron and hole schubwegs per unit length, $\mu_e \tau_e F/L$ and $\mu_h \tau_h F/L$

$$\eta_{CC} = \eta_{CCh} + \eta_{CCe} = x_h \left[1 + \frac{\left(e^{-1/x_h} - e^{-1/\Delta}\right)}{(\Delta/x_h - 1)\left(1 - e^{-1/\Delta}\right)}\right] + x_e \left[1 - \frac{\left(1_e - e^{-1/\Delta - 1/x_e}\right)}{(\Delta/x_e + 1)\left(1 - e^{-1/\Delta}\right)}\right] \tag{20.14}$$

where the collection efficiencies of holes and electrons have been separated into η_{CCh} and η_{CCe}. The radiation receiving electrode is assumed to be positive [33, 137–141]. In this simple model of the detector, the output Q_c is proportional to Q_i and hence to the incident radiation X, which means that we can use linear system concepts to extend the above model for a delta pulse input to any shape of x-ray excitation. While Eq. (20.12) strictly applies under small signal conditions, that is, the perturbation of the field by the injected charge is negligible, the equation shows much resilience even under strong injection, and errors are not as large as one may anticipate [142]. Further, Eq. (20.14) assumes that the semiconductor properties are homogenous, that is, the carrier ranges (mobility × lifetime product) do not vary across the sample. It is possible to continue to use Eq. (20.14) in cases where the carrier ranges are not uniform in the sample by suitably defining effective carrier ranges as discussed in [143].

The charge collection efficiency for a given photoconductor depends on x_e and x_h and hence on the applied field. For x-ray photon absorption very near the radiation receiving electrode, $\Delta << 1$, η_{CC} passes over to the classical Hecht collection efficiency [31] for the carrier that has to traverse the whole photoconductor thickness (holes for positive bias on the radiation receiving electrode). It should be emphasized that the analytical expressions for η_{CC} usually assume small signals and hence neglect the space charge perturbation, which can affect η_{CC} [144, 145]. Figure 20.11 is a plot of the collection efficiency of holes and electrons, that is, η_{CCh} and η_{CCe}, respectively, as a function of $\mu\tau F/L$ for each carrier for

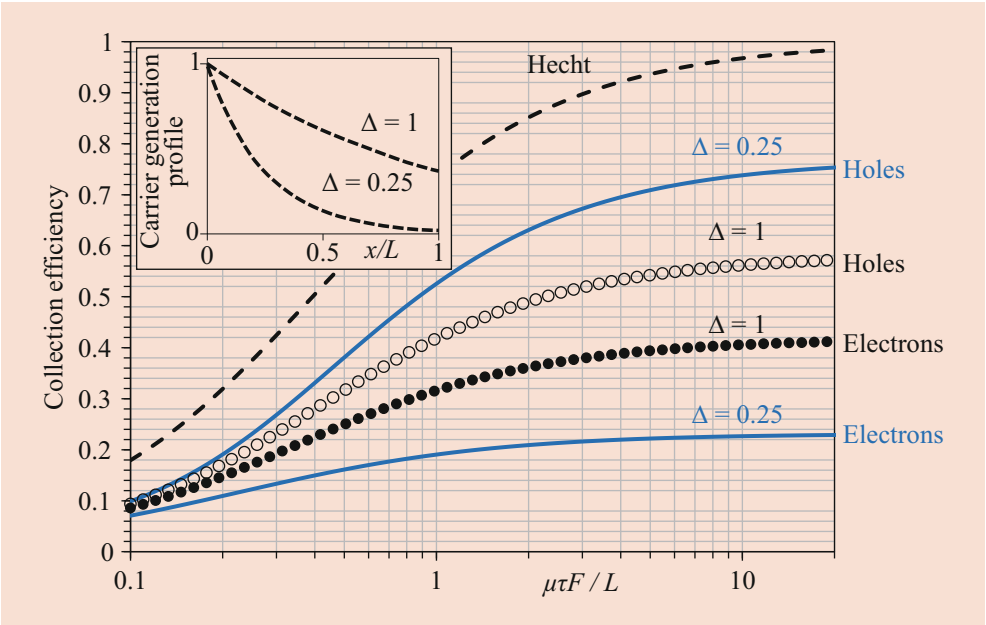

Fig. 20.11 Collection efficiency vs normalized schubweg ($\mu\tau F/L$) for electrons and holes with two different photogeneration profiles, $\Delta = 1$ and $\Delta = 0.25$

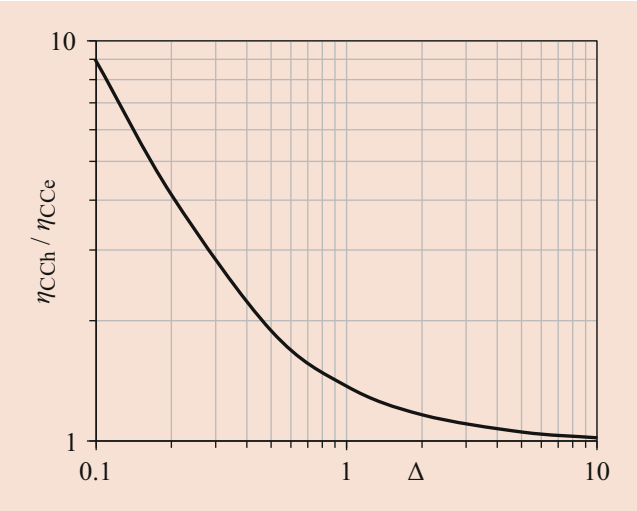

Fig. 20.12 Ratio of hole charge collection efficiency to electron collection efficiency (η_{CCh}/η_{CCe}) vs Δ ($= \delta/L$)

two different x-ray attenuation profiles, $\Delta = 1/\alpha L = 1$ and $\Delta = 0.25$. Notice that holes make a bigger contribution to the collected charge Q_c than electrons and their contribution increases as Δ becomes smaller, eventually reaching the Hecht curve. Most semiconductors have asymmetric $\mu\tau$ products as apparent in Table 20.2 with one type of carrier being favored over the other. It is therefore important to ensure that the carrier with the longer range is drifted toward the bottom electrode. Figure 20.12 highlights how, under positive bias, with decreasing x-ray attenuation depth (decreasing Δ), the collected charge Q_c is more and more dominated by the collection of holes.

20.4.2 Signal and Linearity

The signal from a single pixel in the x-ray image detector in Fig. 20.7 is given by Eq. (20.13), in which Q_i depends on the absorbed energy in Eq. (20.11) so that at a photon energy E the signal is

$$Q_c = \eta_{CC} Q_i = e\eta_{CC}\left[\frac{(\alpha_{en}/\alpha)\,E}{W_i}\right](A\Phi_0)\,\eta_Q \qquad (20.15)$$

and is proportional to the incident fluence Φ_0. Increasing the photon fluence Φ_0 increases the signal Q_c in a linear fashion. Equation (20.15) needs to be integrated over the energy spectrum of the input radiation for a polyenergetic spectrum. Q_c in Eq. (20.15) is per unit exposure such as 1 R or 1 mR and hence needs to be scaled for any arbitrary exposure X

$$Q_c = e\eta_{CC}\eta_Q \frac{(\alpha_{en}/\alpha)\,E}{W_i} A\Phi_0 X \qquad (20.16)$$

It is important to emphasize that the highly desirable linear relationship between Q_c and X is lost under high exposure rates (large signals) or for semiconductors with less than ideal carrier ranges, e.g., $\mu\tau F$ is comparable to L. Under high doses delivered to the sample, x-ray generated electrons and holes create a bulk space charge, distorting the field; they can recombine with each other, become trapped, and recombine with oppositely charged trapped carriers, and there may be x-ray-induced defects created that can trap carriers. Space charge due to trapped carriers needs to be considered as well. All these factors were needed to explain the deviation of an a-Se detector response from the linear behavior under very large doses operating at 2 MeV radiation [146]. Correct approach, beyond the scope of this chapter, to modeling large signals is to solve the continuity equation, trapping and recombination rate equations with trap filling as well as new trap generation, and the Poisson equation. Generally, only numerical solutions can be obtained as described in [146]. The main result is that η_{CC} becomes dependent on the rate of charge generation or rate of dose delivery and the actual Q_c vs X behavior falls below the small signal linear behavior.

The derivation of Eq. (20.16) assumes that the accumulation of charge Q_c and hence the buildup of voltage (Q_c /C_{ij}) on the pixel capacitor do not significantly modify the voltage across the photoconductor, which would modify the field F and hence the sensitivity of the pixel; the responsivity would be poorer at smaller fields. In nearly all cases, Q_c /C_{ij} << V, the applied voltage.

Equation (20.16) is the pixel response to an incident exposure of X (in roentgen) at the pixel. It is no different from the response of any photoconductive x-ray detector used in the integrating mode. For monoenergetic radiation, the fluence Φ_0 as photons cm^{-2} R^{-1} can be obtained from [147]:

$$\Phi_0 = \frac{5.45 \times 10^{13}}{(\alpha_{en,air}/\rho_{air})\,E} \qquad (20.17)$$

where $\alpha_{en,air}$ is the energy absorption coefficient of air, ρ_{air} is the density of air, and E is the photon energy in eV. Alternatively, Φ_0 in photons mm^{-2} per mR is given by Boone [148] over the photon energy range 1–150 keV as

$$\Phi_0 = \left[a' + b'\sqrt{E}\ln E + \frac{c'}{E^2}\right]^{-1} \qquad (20.18)$$

where E is the photon energy in keV and $a' = -5.0233 \times 10^{-6}$, $b' = 1.8106 \times 10^{-7}$, and $c' = 0.0088387$. The conversion from exposure in roentgen to dose in air in Grays is straightforward.

20.4.3 Noise Sources in the Detector

The evaluation of signal-to-noise ratio (SNR) involves considering various noise sources that corrupt the signal in Eq. (20.16) on the pixel capacitor C_{ij} in Fig. 20.7. Since charge signal on C_{ij} has to be read out, it is not possible to exclude the noise from the readout and peripheral electronics, including the quantization noise in converting the analog signal to a digital form. (The analog-to-digital converter has to be at least 14 bits to cover dynamic range of the pixel signal.) If the readout of a pixel occurs at every Δt seconds, then during Δt, the pixel capacitor C_{ij} accumulates charges from the dark current I_d shown in Fig. 20.7. Although the dc value of this charge in the dark can be subtracted from the total charge read, its fluctuations represent noise and corrupt the signal. These charge fluctuations are expressed as root-mean-square (RMS) number of electrons, often abbreviated to rmse. Further, the read and reset operations of the TFT also result in charge fluctuations on C_{ij}. As we move from the TFT, along the data line to the charge amplifier in Fig. 20.7, more noise is added. A proper evaluation of the detector noise involves several factors from the photoconductor to the charge amplifiers in Fig. 20.7, starting with the incoming radiation. The detailed analyses can be found in references [48, 149], whereas the treatise below is a descriptive semi-quantitative approach in considering only the most important contributions.

The quantum noise in the incident radiation is due the Poisson statistics of photons. If Φ_0 photons are incident, then the RMS noise is ${\Phi_0}^{1/2}$ and since the signal is proportional to Φ_0, SNR $= \Phi_0/{\Phi_0}^{1/2} = {\Phi_0}^{1/2}$, which improves with higher exposure, i.e., it is worse at lower exposures. The quantum efficiency η_Q in Eq. (20.6) is an average value for the attenuated photons based on the fact that the probability of absorption along the detector length is an exponential distribution of the form $\exp(-\alpha x)$. Therefore, η_Q has a variance given by $\eta_Q(1-\eta_Q)$ which vanishes for full absorption, hence the need to absorb as much of the incident photons as possible. It is a maximum at $\eta_Q = 0.5$.

Consider the absorption of a single photon that deposits an energy $E_d = (\alpha_{en}/\alpha)E$. Assume $\eta_Q = 1$. The conversion process of this absorbed photon to charge carriers also has fluctuations as explained in Sect. 20.1. It is not simply E_d/W_i but fluctuates about this mean value. The variance of this conversion is $F_N(E_d/W_i)$, where F_N is the Fano factor. The corresponding RMS fluctuations in the converted charge is $\Phi_0(F_N E_d/W_i)^{1/2}$. However there is also the conversion of photon noise in the input radiation to carriers, i.e., $(\Phi_0)^{1/2}(E_d/W_i)$; thus, the conversion noise $N_{conversion}$ in rmse for converting Φ_0 photons is given by

$$N^2_{conversion} = \Phi_0^2\left(\frac{F_N E_d}{W_i}\right) + \Phi_0\left(\frac{E_d}{W_i}\right)^2 \qquad (20.19)$$

The Fano factor for many semiconductors is typically less than 1 (e.g., $F_N \approx 0.1$ for Si). a-Se is an exception to this observation. There are no systematic and replicated experimental studies on F_N, but inferences from pulse height spectrum measurements and simulations indicate that F_N is not less than unity and is likely to be more [132, 150]. The free EHP creation process in a-Se involves two intermingled independent processes: first, the generation of electrons and holes in the primary electron track and, second, the diffusion and drift of these electrons and holes in the track in which they experience Langevin recombination. Those electrons and holes that escape recombination and hence the track constitute the observed W_i [135]. Both of these process have a variance that leads to an overall effective Fano factor that is likely to be greater than unity. In addition, the presence of K-fluorescence escape and reabsorption complicates not only W_i but also the statistics in Eq. (20.19), which adds variance to the converted charge statistics due to x-ray photons around the K-edge. The fluctuations in the number of collected charges per incident x-ray photon from a-Se have been measured and show higher fluctuations (more noise) around the K-edge (12.7 keV) which highlights the K-edge fluoroluminescence escape and reabsorption effects [151].

The charge collection efficiency, as represented by η_{CC}, is an average value for the collected charge Q_c. As explained in Sect. 20.2, charge trapping is a stochastic process, which means that η_{CC} has to be viewed as a mean value and the charge collection process possessing a certain variance [33, 34]. Provided that the collection efficiency is high, the variance in the latter can generally be neglected compared to other fluctuations.

The shot noise of the dark current through the photoconductor causes fluctuations of the charge accumulated on the pixel capacitor C_{ij}. Suppose that the capacitor is read every Δt seconds (frame time) so that the dark current integration time is Δt. The mean value of the number of accumulated charges is $I_d \Delta t/e$. Shot noise follows Poisson statistics so that the RMS noise N_d in the number of carriers collected on C_{ij} is

$$N_d = \sqrt{I_d \Delta t/e} \qquad (20.20)$$

Most analyses of photoconductor noise in the imager pixel consider only the shot noise in Eq. (20.20), due to the fact that usually not much information is available on the excess noise behavior of the photoconductor under consideration. Excess noise is a form of noise that is in excess of shot and thermal noise. All semiconductors would exhibit excess noise if measured down to sufficiently low frequencies. There are several forms of excess noise as reviewed in detail in [152–156], but the most important three sources for x-ray photoconductors are generation-recombination (GR) noise, flicker noise, and contact noise. The first two fluctuations

are in the conductance of the medium. Contact noise is due to fluctuations of carrier injection from the contact or variations in the current due to phenomena at the surface or near the contact surface (e.g., in the depletion region). If the dark current is a leakage current over the device surface, it can easily exhibit flicker noise in which the noise depends on the surface conductance.

The quantity of interest in describing noise is its spectral noise power density S_i, the square of the current fluctuations in a small frequency interval Δf averaged many times per unit frequency, i.e., $<i^2>/\Delta f$. GR noise follows a Lorentzian spectrum, whereas for flicker and contact/surface noise, the spectra are approximately $1/f$ type, but they have different dependences on the dc current and detector geometry. Table 20.2 summarizes the main features of the three types of excess noise considered.

The GR noise invariably involves a single defect level in the bandgap that aids recombination and generation, which results in the fluctuations in the number of carriers N and hence in the conductance. It can also be caused by the fluctuations in the rate of trapping and detrapping of carriers through a set of traps at a well-defined discrete energy level. In the latter case, a straightforward expression is provided by Copeland for a discrete level of traps in an extrinsic semiconductor [157, 158]. S_i depends on $I_d{}^2$ and has a $1/f^2$ roll-off at high frequencies and a flat spectrum at low frequencies, i.e., a Lorentzian spectrum. It scales inversely with the active volume of the device. It is quite often observed in intrinsic semiconductor crystals with defects, for example, Ge [159], Si [160], $Al_xGa_{1-x}As$ [161], etc.

Both flicker and contact noise can be represented by an equation of the form

$$S_i = \frac{C_n I_d^b}{f^\alpha} \tag{20.21}$$

where C_n is a device-specific constant and different for flicker and contact noise and α and b are constants that characterize the nature of observed noise, with $\alpha = 1$ being "pure $1/f$ noise." One of the differentiating features between flicker and contact noise sources is in the dc current dependence. Normally, $b = 2$ for flicker noise since it is fluctuations in the conductance of the medium, whereas $b < 2$, often $b = 1$, for contact noise. Further, in flicker noise, the constant C_n is inversely proportional to the total number of carriers and is usually written as $C_n = \alpha_H/N$, where α_H is called the Hooge parameter, a characteristic parameter that gauges the relative measure of fluctuations in the medium. On the other hand, for contact noise, C_n depends on the surface area involved between the metal and the semiconductor.

In the case of contact noise, usually some kind of carrier emission over a barrier height Φ_B is involved as in a Schottky junction. Small variations in Φ_B at the metal-semiconductor interface can easily lead to a $1/f$ type noise with $\alpha \approx 1$ and $b \approx 1$ [162]. $1/f$ noise can also arise from a distribution of surface traps at the contact or near the surface. One of the examples directly related to x-ray detector materials is the excess noise in CdZnTe single crystals with different contacts [163]. This noise has been found to exhibit $1/f$ type excess noise behavior, and its magnitude has been correlated with the surface conditions of the crystal and the metallization used for the contact. In the case of ohmic contacts, as in In-CdZnTe, in which the current is limited by the bulk material, the excess noise has a GR origin.

Flicker and contact noise are the most dominant excess noise sources in x-ray photoconductors used in both small and large area detectors. Table 20.3 provides a summary of the three excess noise sources that usually contribute to the photoconductor noise with examples on a few semiconductors.

The effect of $1/f$ noise in integrating detector performance has been described in [171, 172], and a proper analysis requires establishing a low cutoff frequency f_0 for the low-frequency fluctuations. Its exact value is not too critical since the dependence of RMS of the fluctuations on f_0 is a $(\ln f_0)^{1/2}$ behavior, i.e., a very slow change with f_0. In general, flicker noise contribution with background subtraction can be written as

$$N_{\text{flicker}} = (1/e)\,\kappa C_n^{1/2} I_d \Delta t \tag{20.22}$$

in which κ is a numerical constant that depends on a number of factors such as f_0 and the sampling scheme. If double sampling and subtraction are used, such that the period before exposure, during exposure, and after exposure are sampled, and each has a duration Δt, then $\kappa = (8 \ln(2))^{1/2} = 2.35$, and there are other sampling possibilities [172]. The importance of C_n cannot be underestimated, and there are sampling sequences that can lower the overall SNR. The RMS fluctuations from shot and $1/f$ noise are typically less than 100 rmse if the dark current is sufficiently suppressed, probably of the order of 50 electrons.

There are several noise sources associated with the particular readout technology used, e.g., TFT vs CMOS or passive pixel vs active pixel. The active pixel sensor (APS) has additional transistors in the pixel to introduce gain. For the TFT technology, these have been reviewed by Yorkston and Rowlands [48]. We consider only the significant sources. There is a so-called *reset* noise or *kTC* noise from the TFT and the capacitor C_{ij} circuit because when the TFT is addressed, it transfers the charge and discharges C_{ij}, but thermal fluctuations across the TFT channel resistance lead to an amount of random charge with a variance (kTC_{ij}/e) to be left on the pixel capacitor. Strictly, C_{ij} should be replaced with an effective capacitance C_{in} that includes C_{ij} and the input capacitance of the TFT. If C_{ij} is 1 pF, this switching noise

Table 20.3 Summary of excess noise sources in semiconductors suitable for x-ray detection

Noise	Fluctuation source	Typical spectral power spectrum	Typical selected examples
Generation-recombination (GR)	Conductance	$S_i \propto \left(\frac{I_N^2}{V}\right) \frac{\tau}{[1+(2\pi f\tau)^2]}$	S_i for a given set of traps or a recombination center at a single energy level. τ is the characteristic time associated with the GR process Pure crystals with discrete defects, e.g., Ge [159], Si [160], epitaxial $Al_xGa_{1-x}As$ [161]
Flicker or 1/*f*	Conductance	$S_i \propto \frac{I_d^2}{Nf^\alpha}$	Ge [164], CdTe [165], PbI_2 [166], CdZnTe, GaAs [167], InSb [168], a-Se [169], a-Si:H [170]
Contact	Injection from contact	$S_i \propto \frac{I_d}{f^\alpha}$	Metal/semiconductor contacts, e.g., metal/Si [162], metal/CdZnTe [163]

N is the total number of free carriers involved in the conduction and *V* is the volume of the sample

corresponds to charge fluctuations of $(kTC_{in})^{1/2}$ or to about 400 rmse. The TFT switch is operated twice, reset and read, so we should multiply by $\sqrt{2}$ to get $(2kTC_{in})^{1/2}$ or about 560 electrons [48]. This noise is part of the TFT operation and arises from the channel resistance of the TFT.

Beyond the pixel and the TFT, there are two more important noise contributions, associated with the charge amplifiers and the data lines. These noise sources are lumped into a single quantity called the data line noise and quoted as a number of electrons referred to the input of the charge amplifier. In TFT arrays, this is roughly 800–2000 electrons and is a function of the lumped data line capacitance, data line resistance, and readout speed. In general, the data line noise dominates all other noise sources in passive pixel TFT arrays. This large noise can be reduced by using a source follower or an amplifier at the pixel level, which makes the pixel an active pixel, rather than passive with just a TFT switch. Active pixel architectures in which the pixel has an embedded amplifying transistor have attracted much interest due to their improved overall SNR in which readout noise per pixel can reach sub-500 electrons for a-Si:H TFTs and less, below 200, for CMOS detectors. a-Si:H-based TFT arrays with on-pixel amplification have been studied and show improved SNR with respect to passive pixel sensor (PPS, with only a TFT switch) [173–175]. Although the electronic noise from the data line and charge amplifier can be significantly reduced, the 1/*f* noise in the a-Si:H channel of the amplifying TFT begins to dominate. Therefore, solutions based on replacing a-Si:H TFTs with poly-Si (polycrystalline silicon) have been explored, and these show potential to realize a reduction in the overall pixel noise, for example, down to around 600 electrons or less [176]. Amorphous In-Ga-Zn-O (IGZO) TFTs arrays have been also demonstrated with lower noise than a-Si:H TFTs and with higher TFT gain because of the higher carrier mobility in a-IGZO than in a-Si:H [177]. However, IGZO TFTs tend to be more susceptible to x-ray radiation damage and are not commonly employed as yet in APS designs although PPS designs have started to see commercial use. It is important to mention that nearly all sensitive CMOS imaging chips already have on-pixel amplification, which means that coating these with a suitable photoconductor can lead to high DQE imagers even though there is the cost of stitching and tiling them. As mentioned above, CMOS imagers also have smaller pixel size as a distinct advantage.

The quantum noise-limited SNR decreases with increasing dose. On the other hand, the electronic noise is usually independent of the incident radiation dose. Therefore, the detector could be quantum noise-limited if the incident dose is sufficiently high to overcome the effect of the electronic noise. When the incident dose is reduced down to very low levels, the detector performance is mainly controlled by the electronic noise. Therefore, the schemes for the reduction of electronic noise become essential for low-dose imaging applications.

20.5 Image Resolution

Resolution or resolving power is the ability to record separate images of small objects that are placed very closely together. The resolution is normally examined in the spatial frequency (*f*) domain. Spatial frequency is similar to temporal frequency except that distance (usually in mm) is used instead of time. In the spatial frequency domain (mm^{-1}), smaller objects correspond to higher frequencies, and larger objects correspond to lower frequencies in the image. The spatial resolution of an imaging device or a system can be described in terms of the modulation transfer function (MTF) which is the relative response of the system as a function of spatial frequency. The x-ray image is two-dimensional, and thus, a two-dimensional MTF(f_x , f_y) is required, which is the two-dimensional Fourier transform of the point spread function (PSF). This is the response of an imaging system to a point input (infinitesimally thin spatial pulse). For a rotationally symmetric system, MTF is also rotationally symmetric and can be expressed in terms of single radial frequency *f*, which is the Fourier transform of the line spread function (LSF). When an imaging system is stimulated with a signal in the form of a line, the LSF is constructed by evaluating the system response perpendicular to the line. The size of the picture element, the *pixel*, in an image sets a limit on what can theoretically be resolved in that image. While images

with small pixels have the *potential* to deliver high spatial resolution, many other factors also affect spatial resolution, and in many cases, it is not the pixel size that is the limiting factor in spatial resolution.

The effect of a digital detector on its image has been described as a two-step process: (i) integration of interacting input quanta in each element to produce a pre-sampling detector signal and (ii) sampling of the pre-sampling detector signal. In the spatial frequency domain, these two processes are described in terms of (i) pre-sampling MTF and (ii) aliasing as determined by the sampling spacing. Therefore, the shape of pre-sampling MTF contains all the information on signal blurring of the detector. The MTF of an imaging system can be described as a cascade of several stages where the overall MTF is simply the product of the MTF of all the individual stages. The pre-sampling MTF of an image detector can be expressed as

$$\mathrm{MTF}(f) = \mathrm{MTF_m}(f) \times \mathrm{MTF_{tr}}(f) \times \mathrm{MTF_a}(f), \qquad (20.23)$$

where $\mathrm{MTF_m} = p_{\mathrm{pe}}\mathrm{MTF_{pe}} + p_{\mathrm{k}}\mathrm{MTF_k} + p_{\mathrm{c}}\mathrm{MTF_c}$ is the weighted MTF including the MTFs due to the range of the primary photoelectron, K-fluorescence reabsorption, and Compton scattering [178], $\mathrm{MTF_{pe}}$ is due to the range of the primary photoelectron, $\mathrm{MTF_k}$ is due to the K-fluorescence reabsorption, $\mathrm{MTF_c}$ is due to Compton scattering, $\mathrm{MTF_{tr}}$ is due to the charge carrier trapping, and p_{pe}, p_{k}, and p_{c} are the relative probabilities of the released charge carriers being from the photoelectric primary electron interaction, K-fluorescent x-ray reabsorption, and Compton scattered photon, respectively. $\mathrm{MTF_a}$ is the modulation transfer function associated with the aperture function of the pixel electrodes. $\mathrm{MTF_a}$ arises due to averaging the signal over a pixel area and describes how spatial frequencies are passed through the detector elements. If the aperture is a square with a dimension a, then

$$\mathrm{MTF_a}(f) = |\mathrm{sinc}(af)| = \left|\frac{\sin(\pi af)}{\pi af}\right| \qquad (20.24)$$

The spatial resolution in direct conversion FPXIs is usually high and closer to the aperture function, as compared to phosphor-based FPXI [36]. The signal blurs due to the range of primary photoelectron, and Compton scattered photons are insignificant for diagnostic x-rays (up to 100 keV) [178, 179]. Therefore, the charge carrier trapping and the reabsorption of K-fluorescent x-ray photons are the two dominant mechanisms responsible for the loss of resolution [180, 181] in direct conversion FPXI. Some of the K-fluorescent x-ray photons may be reabsorbed at different points within the detector volume from the primary x-ray photon interaction point. This generates additional EHPs and creates a lateral spreading of signal. The loss of resolution due to fluorescence reabsorption is maximum (although not very substantial) just above the K-edge of the photoconductor. This effect can be ignored when (i) the incident x-ray photon energy is lower than the K-edge of the photoconductor or (ii) the mean energy of the x-ray beam and the K-edge occurs at widely different energies [180]. Que. and Rowlands [178] described a numerical method to calculate the $\mathrm{MTF_k}$ by considering the PSF of the detector and subsequent two-dimensional (2D) Fourier transform of the PSF. Later, a simplified and convenient semi-analytical model to calculate $\mathrm{MTF_k}$ by determining the LSF and a subsequent 1D Fourier transform was developed and applied to a-Se and HgI_2 detectors [182]. The charge carrier trapping has a significant effect on the resolution of these direct conversion x-ray image detectors, which is discussed below.

The direct conversion FPXI geometry consists of a photoconductor layer sandwiched between two electrodes; the electrode at one side is a continuous metal plate and the electrode on the other side of the photoconductor is segmented into an array of individual square pixels of size $a \times a$ as shown in Fig. 20.13a. The *geometric* pixel aperture width in a flat panel detector is smaller than the pixel pitch (center-to-center spacing between two pixels). However, it is shown that the effective fill factor (the effective fraction of pixel area used for image charge collection) of a photoconductive flat panel detector is close to unity [183, 184]. Therefore, the *effective* pixel aperture width a is virtually identical to the pixel pitch. Some of the x-ray generated carriers become captured by deep traps in the bulk of the material during their drift across the photoconductor. Suppose that a carrier is trapped in the photoconductor above a particular (central) pixel electrode of a pixelated image sensor. This trapped carrier induces charges not only on the central pixel electrode but also on neighboring pixel electrodes as shown in Fig. 20.13b and consequently there is a lateral spread of information and hence a loss of image resolution.

Straightforward analytical expressions for the MTF due to distributed carrier trapping in the bulk of the photoconductor have been described in [185], where the effect of charge carrier trapping on the resolution of a direct conversion FPXI has been examined as a function of charge carrier ranges. Trapping of the carriers that move toward the pixel electrodes degrades the MTF performance, whereas trapping of the other type of carrier that moves away from the pixels improves the sharpness of the x-ray image.

The a-Se-based x-ray detectors use thin blocking layers between the bulk layer (nearly intrinsic) and the metal contacts (Figs. 20.6 and 20.13) in order to minimize the dark current at the operating electric field. The operating electric field refers to the applied field that ensures the x-ray generated charges are mostly collected. The thicknesses of these blocking layers are few microns (usually 4–8 μm), whereas the total photoconductor thickness is at least few

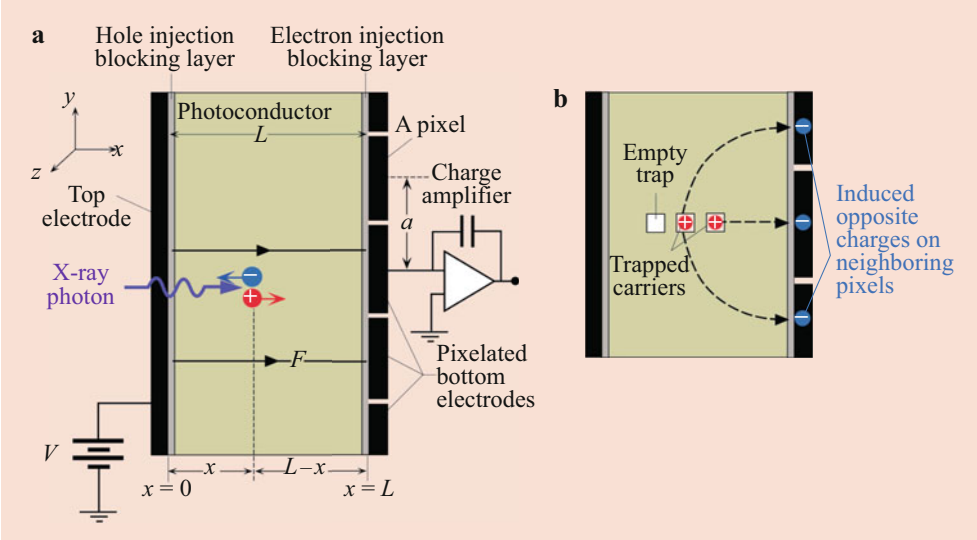

Fig. 20.13 (**a**) A cross section of a direct conversion pixelated x-ray image detector. (**b**) Trapped carriers in the photoconductor induce charges not only on the central pixel electrode but also on neighboring pixel electrodes, spreading the information and hence reducing spatial resolution

hundred microns. The amount of trapping/defect states in the blocking layer is much larger than the bulk photoconductor layer. Therefore, one can expect much more trapped carriers in the blocking layers than in the bulk photoconductor layer. If charge carrier trapping occurs right at the interface between the photoconductor and blocking layer only, then its corresponding MTF can be calculated by a simple analytical expression [181, 186].

Figure 20.14 shows the measured MTF for various flat panel x-ray image detectors for mammographic applications. The thicknesses of a-Se, HgI_2, and CsI (indirect conversion) layers are 200, 127, and 150 μm, respectively. The measured MTF data for a-Se detector are extracted from [187]. The plotted values for HgI_2 and CsI:Tl are based on published MTF results of [53, 188], normalized to correspond to the 85 μm pixel aperture. The MTF of a direct conversion detector (e.g., a-Se and HgI_2) is close to a sinc function (i.e., MTF_a). The charge carrier trapping and the reabsorption of *K*-fluorescent x-ray photons are the two dominant mechanisms responsible for this little difference. The state-of-the-art MTF of the indirect conversion detectors (CsI detectors) is still much worse than that of direct conversion detectors. The omnidirectional propagation of x-ray generated optical photons (i.e., optical scattering) in the CsI layer is the dominant cause of loss of resolution in indirect conversion detectors.

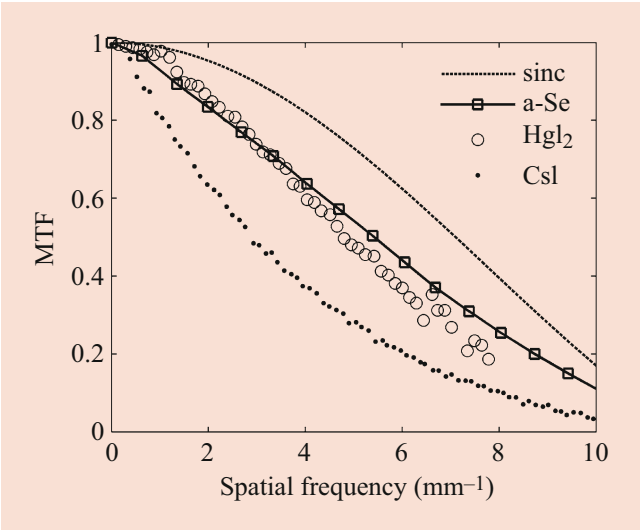

Fig. 20.14 Measured MTF for various flat panel x-ray image detectors. The dashed line is MTF_a based on 85 μm aperture size. The measured MTF on a-Se, HgI_2, and CsI detectors are adapted from [53, 187, 188], respectively

20.6 Detective Quantum Efficiency (DQE)

Detective quantum efficiency (DQE) measures the ability of the detector to transfer signal relative to noise from its input to its output. The random nature of image quanta gives rise to random fluctuations in image signals contributing to image formation and hence creates random noises. Images are partially degraded by various sources of statistical fluctuations, which arise along the imaging chain. The relative increase in image noise through an imaging system as a function of spatial frequency f is expressed quantitatively by DQE(f) which represents the signal-to-noise transfer efficiency at different frequencies of information in an image. The DQE(f) is defined as

$$\mathrm{DQE}(f) = \frac{\mathrm{SNR}^2_{\mathrm{out}}(f)}{\mathrm{SNR}^2_{\mathrm{in}}(f)}, \tag{20.25}$$

where $\mathrm{SNR}_{\mathrm{in}}$ and $\mathrm{SNR}_{\mathrm{out}}$ are the signal-to-noise ratio at the input and output stages of an image detector, respectively, and DQE(f) is unity for an ideal detector.

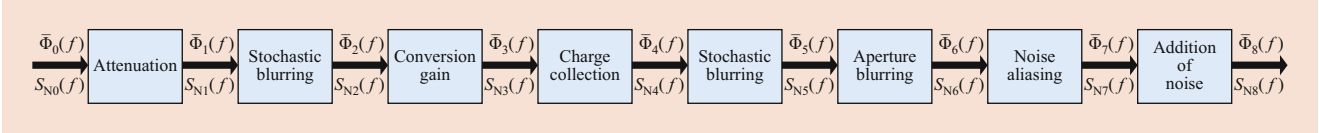

Fig. 20.15 The block diagram shows the propagation of signal and NPS through the eight stages of a direct conversion x-ray imaging detector

The SNR(f) is a function of the MTF and the noise power spectrum (NPS). The extent of noise in an image is quantified by its variance, but it does not quantify the noise *texture* (the way the noise looks). To get the noise texture, we need to find the frequency dependence of the noise variance, which is quantified by NPS(f). Indeed, the integral of the NPS over all frequencies equals the variance σ^2. The scattering of image quanta gives rise to image blurring which is quantified by MTF(f) as described above. The MTF(f) describes how well an imaging system *processes signal*, and the NPS(f) describes how well an imaging system *processes noise* in the image. The noise in the number of x-ray quanta incident on the detector follows a Poisson process and is uncorrelated. If the Φ_0 is the average number of x-ray photon incident on the detector, then its variance is $\sigma^2 = \Phi_0$ and thus the input NPS(f), $S_{N0} = \sigma^2 = \Phi_0$. The input $\text{SNR}^2 = \Phi_0$ (see Sect. 20.4.3). Therefore, the DQE(f) can be written as

$$\text{DQE}(f) = \frac{K[\text{MTF}(f)]^2}{\text{NPS}(f)\Phi_0}, \tag{20.26}$$

where K is a constant that converts units. For simplicity, we are often interested in measuring DQE ($f = 0$) of an imaging detector since it represents signal quality degradation due to the signal and noise transfer characteristics of the system without considering signal spreading. In that case

$$\text{DQE}(f) = \frac{\text{DQE}(0)[\text{MTF}(f)]^2}{\text{NPS}_0(f)}, \tag{20.27}$$

where $\text{NPS}_0(f)$ is the noise power spectrum of the system normalized to unity as f approaches 0.

The DQE can be conveniently calculated by developing an appropriate cascaded linear system model [189, 190]. In the cascaded linear system model, an imaging system is described as cascades of simple and independent elementary stages. The effect of charge carrier trapping on the DQE(f) has been analyzed in [191, 192]. Zhao et al. [193] have studied the effects of K-fluorescence on DQE(f) by developing a cascaded linear system model with a combination of series and parallel processes [194]. Recently, a cascaded linear system model for calculating the DQE(f) of a direct conversion x-ray detector has been developed that incorporates the effects of both charge carrier trapping and the reabsorption of K-fluorescent x-rays [182]. In the latter work, the authors have examined various effects on DQE(f) and also verified their model by fitting with the experimental results on a-Se and HgI_2 detectors. The K-fluorescence phenomenon has a significant effect on DQE(f) performance if the average incident x-ray photon energy is relatively close to the K-edge of the detector material [182]. If the average incident x-ray photon energy is far from the K-edge of the detector material, one can use a relatively simpler model for calculating DQE(f) as described in [179].

The linear system model for the calculation of DQE(f) of a photoconductive detector consists of eight stages: (1) x-ray attenuation, (2) scattering of x-ray photons before EHP creation, (3) generation of charge carriers (conversion gain), (4) charge collection, (5) blurring due to charge carrier trapping, (6) aperture blurring, (7) noise aliasing, and (8) addition of electronic noise. The flowchart shown in Fig. 20.15 illustrates these eight separate stages and the signal and noise in different stages. Each of these stages can be categorized as one of the following five processes: (i) stochastic gain, (ii) stochastic blurring, (iii) deterministic blurring, (iv) aliasing, and (v) addition. The first, third, and fourth stages in Fig. 20.15 are considered as the stochastic gain stage. The stochastic gain enhances the noise associated with the quanta in two ways: first, the quantum noise is itself amplified, and second, noise associated with the stochastic nature of the amplifying mechanism is introduced into the output. The second and fifth stages are the stochastic blurring stages. Stochastic blurring is caused by random scattering of quanta in a distribution. That is, each quantum is randomly relocated to a new location with a certain probability. The integration of signal onto individual pixels in a digital detector is the deterministic blurring stage (sixth stage). The details of the signal and noise propagation through various stages are described in [179]. This cascaded linear system model has been applied to a number of different photoconductive detectors [180, 195, 196].

High conversion gain and high charge collection efficiency are required to improve the DQE performance of an x-ray image detector. The conversion gain Eq. (20.12) depends on W_i, which is a material property of the photoconductor. The charge collection efficiency can be improved by increasing F and improving the $\mu\tau$ products of the carriers. However, increasing F also increases the dark current dramatically, and thus, there is a practical limitation on F. DQE improves dramatically by reducing electronic noise (Sect. 20.4.3) in low-dose imaging applications [191].

20.7 Pixelated Detectors and Small Pixel Effect

The basic structure of a pixelated detector is shown in Fig. 20.13a where, as apparent, the rear electrode is pixelated with a pixel size of a. *Small pixel effect* is the phenomenon in semiconductor pixelated detectors in which the collected charge mainly depends on the motion of the charge carriers that move toward the pixel electrodes. Stated differently, the motion of charge carriers close to the pixel electrodes (near-field region) can produce almost full signal (collected charge) strength in the external circuit, and the motion of charge carriers outside this region induces very little signal. The reason is that the induced charge on a particular pixel electrode by a moving charge is very small when the charge is far away (the distance to the pixel is much greater than the pixel dimension) due to charge sharing among many pixel electrodes and increases rapidly when the charge is in the vicinity of this pixel. As a result, the change in induced charges in pixel electrodes due to the carrier motion through the near-field region is much higher than their motion in the outside of the near-field region (this change in induced charge produces electric current in the external circuit, and the integration of this current is the collected charge).

The Shockley-Ramo theorem [1, 2, 197] provides a convenient way to calculate the induced current flowing through an electrode of multielectrode detectors (e.g., pixelated image detector) due to the motion of charge carriers in the detector. The shape of the weighting potential across the photoconductor thickness determines the relative contribution of the induced signal strength for carrier movement across different segments of the photoconductor thickness. Analytical expression for the weighting potential of pixelated detectors having a square pixel can be found in [198] where the effects of small pixels on x-ray sensitivity of pixelated detectors have been considered. Figure 20.16a, b shows the individual carrier contributions to the normalized sensitivity (S_t and S_b) versus normalized pixel width (a/L) for various levels of trapping ($x_t = \mu_t \tau_t F/L$ and $x_b = \mu_b \tau_b F/L$). The subscripts t and b represent the carrier type that drifts toward the top and bottom electrodes, respectively. The quantum efficiency (Eq. 20.10) is $\eta_Q = 0.90$ and thus $\Delta = 0.4343$. The normalized sensitivity is the product of the charge collection efficiency and the quantum efficiency. That means, the normalized sensitivity represents the charge collection and absorption-limited detector sensitivity. S_t and S_b are the individual carrier contributions to the normalized sensitivity due to the carrier drifts toward the top and the bottom electrodes, respectively, and the resultant total sensitivity is simply $S_t + S_b$. The maximum total normalized sensitivity is equal to the quantum efficiency when both carrier lifetimes are infinity. S_t decreases with decreasing normalized pixel width. A very small fraction of carriers moves through the near-field region for the carriers that move toward the top electrode. Therefore, the induced signals due to the carrier drift toward the top electrode decrease with decreasing normalized pixel width and so does S_t. The sensitivity obviously decreases with increasing amounts of trapping as evident in Fig. 20.16a. Without carrier trapping and for small pixels, all the carriers that drift toward the bottom electrode pass through the near-field region. Therefore, the relative fraction of the total normalized sensitivity, S_b, contributed by the charges that drift toward the bottom electrode increases with decreasing pixel width, and the other type of carrier contribution becomes less important. Notice that S_b increases with decreasing pixel width for weak trapping but it decreases with decreasing pixel width under heavy trapping. The carrier generation profile is exponential across the photoconductor thickness. Most of the carriers become trapped before reaching the near-field region under heavy trapping for very small pixel detectors. Thus, S_b for very small pixel detectors is also small under heavy trapping. The extent of near-field region decreases with decreasing normalized pixel width. Therefore, this effect is more pronounced in detectors with pixel dimensions that are small compared with the detector thickness.

Since the charge collection efficiency of pixelated detectors mainly depends on the transport properties (mobility and lifetime) of the charges that move toward the pixel electrodes, the effects of poor transport properties of other type of carriers can be eliminated by having smaller pixels. Some of the potential photoconductors (e.g., a-Se, CdZnTe and HgI_2) for x-ray image detectors have asymmetric transport properties (mobility-lifetime products) for electrons and holes. Therefore, the charge collection efficiency of pixelated detectors can be improved by ensuring that the carrier (electron or hole) with the higher mobility-lifetime product is drifted toward the pixel electrodes.

20.8 Image Lag and Ghosting

The detectors should be free of image lag and ghosting effects. When the photoconductor is exposed to x-rays, a transient photocurrent starts to flow that reaches almost a steady value at the carrier transit time [199]. Ideally, the current should be present as long as the detector is subjected to x-ray exposure, and once the radiation is stopped, it should diminish to zero. In reality, some of the drifting carriers are trapped at various levels of defect states within the bandgap of the photoconductor layer, and these trapped carriers are released later. The release time from a trap depends on the energy depth of the trap from the transport band edge and hence can lead to significant lag [200]. As a result, in some detectors, a transient decaying current can be detected for several hundreds or thousands of seconds after the cessation

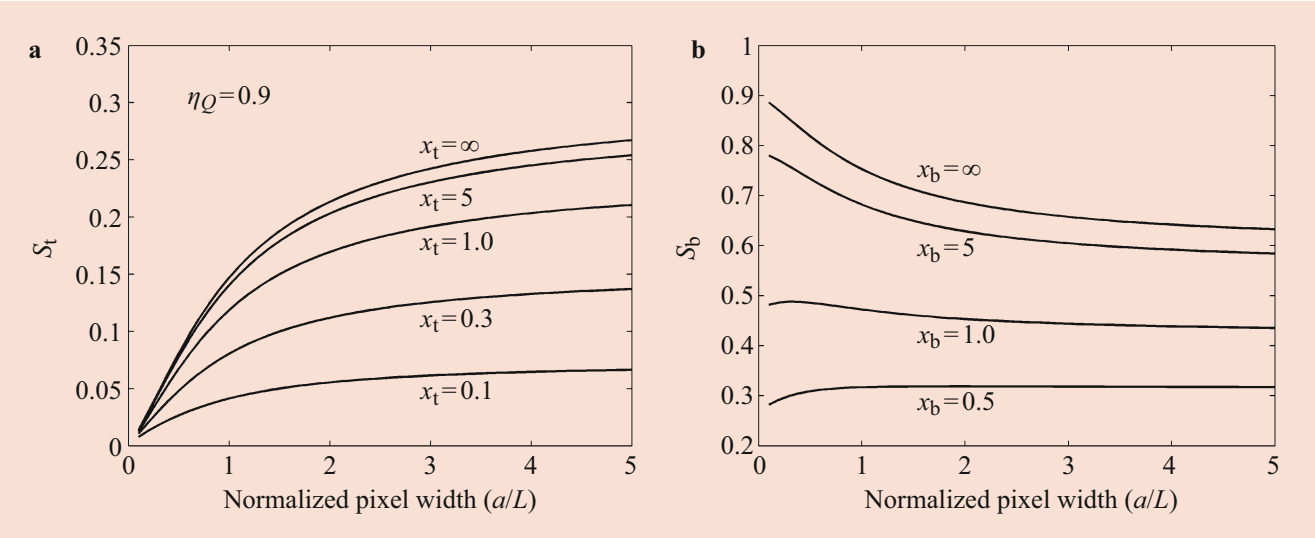

Fig. 20.16 (**a**) Normalized sensitivity due to transport of the carriers that drift toward the top electrode, S_t, versus normalized pixel width for various levels of carrier trapping. (**b**) Normalized sensitivity due to transport of the carriers that drift toward the bottom electrode, S_b, versus normalized pixel width for various levels of carrier trapping. The normalized absorption depth is $\Delta = 0.4343$. Normalized pixel width is a/L

of the excitation. This is known as the residual current or the lag signal and has been modeled for a-Se detectors in [199]. For most applications, this is an undesirable phenomenon because when part of the current from a previous exposure combines with the next one, the resulting image can be inaccurate, particularly when images are acquired in a fast sequence, e.g., in fluoroscopy. The image lag signal has been measured in most of the potential photoconductive detectors. The amount of image lag signal in a-Se detectors has been found to be negligible, whereas it is quite significant in some of other polycrystalline detectors [201].

The x-ray exposure can change the x-ray sensitivity of the exposed area and thus lead to a shadow impression of a previously acquired image which becomes visible in subsequent uniform exposure, which leads to what is called "ghosting" [202]. Ghosting can severely affect the diagnostic value of x-ray images. The causes of change in x-ray sensitivity and resolution and their recovery mechanisms in a-Se detectors have been systematically investigated in the last decade [203, 204]. Although the relative amounts of changes in sensitivity and resolution, arising from repeated exposure in commercial a-Se detectors, are below the tolerance level, they are due to the following probable mechanisms: (i) recombination of drifting carriers with oppositely charged trapped carriers [200], (ii) creation of x-ray-induced metastable trap centers [205, 206], and/or (iii) reduction of the free carrier generation due to space charge (i.e., due to a nonuniform electric field) [200, 204]. It is expected that the ghosting phenomenon may also be present in other photoconductive (e.g., HgI_2, CZT, PbO, and PbI_2) detectors, although a very limited number of reports are available in literatures [207, 208].

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Photodetectors Based on Emerging Materials

21

Jiantong Li and Mikael Östling

Contents

21.1 Background of Graphene-Based Photodetectors 778

21.2 Performance Metrics of Photodetectors 778
21.2.1 Responsivity (R_{ph}) 778
21.2.2 Quantum Efficiency 779
21.2.3 Noise Equivalent Power (NEP) 779
21.2.4 Detectivity (D^*) 779
21.2.5 Linear Dynamic Range (LDR) 779
21.2.6 Response Speed 779
21.2.7 Photoconductive Gain (G_{ph}) 779

21.3 Physical Mechanisms for Photodetection 780
21.3.1 Photovoltaic Effect 780
21.3.2 Photothermoelectric Effect 780
21.3.3 Bolometric Effect 781
21.3.4 Plasma-Wave-Assisted Mechanism 781
21.3.5 Photogating Effect 781

21.4 Practical Realization of Graphene Photodetectors 781
21.4.1 Metal-Graphene-Metal (MGM) Photodetectors (PV and PTE Effects) 781
21.4.2 Graphene-Based Bolometers 782
21.4.3 Plasmonics-Enhanced Graphene Photodetectors 783
21.4.4 Detectors Based on Photogating 783

21.5 Graphene-Based Heterostructures for Photodetectors 785
21.5.1 Graphene/Silicon 785
21.5.2 Graphene/III–V Semiconductors 786
21.5.3 Graphene/Organic Semiconductors 787
21.5.4 Graphene/Perovskites 790
21.5.5 Graphene/Other 2D Materials 790

21.6 Integrated Graphene Photodetectors 795
21.6.1 Integration with Optical Cavity 795
21.6.2 Integration with Waveguides 795

21.7 Graphene Photodetectors with Special Geometry or Architectures 797

21.8 Conclusions and Outlook 797

References 801

Abstract

Photodetectors that convert light into electrical signals have become an indispensable element for a large number of technologies to enable extensive applications, ranging from optical communications to advanced imaging and motion detection, to automotive industry particularly including self-driving cars, and to astronomy and space exploration under harsh environment. The present photodetector market is predominated by silicon (CMOS-based) photodetectors. With the continuous growth of application areas, highly desired are photodetectors of higher performance in terms of speed, efficiency, detectable wavelength range, and integrability with semiconductor technology. These necessitate the development of new photodetectors based on special materials, rather than the conventional silicon single crystals, as building blocks for various advanced photodetection platforms. To this end, we summarize in this chapter the recent status of advanced photodetectors based on the emerging material, graphene. Our discussion includes the performance metrics, working mechanisms, practical implementation, as well as opportunities and challenges, for graphene-based photodetectors.

Keywords

Graphene · Photodetectors · Photodetection mechanism · Heterostructure · Optical cavity · Waveguide · Charge neutrality point · 3D substrates

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21.1 Background of Graphene-Based Photodetectors

Photodetection is becoming more and more important in a wide range of applications, including the ubiquitous visible light cameras and video imaging, medical X-ray and near-infrared (NIR) imaging, night-vision and shortwave infrared (SWIR) surveillance, motion detection, machine vision, gas sensing, optical communications, and so on [1–3]. It primarily makes use of semiconductors to transduce photons of different energies (determined by the bandgap of the semiconductors) into electrical signals for subsequent signal processing and applications. Up to date, the predominant materials for photodetectors in modern electronics and optoelectronics are still crystalline silicon, thanks to the high performance, low cost, manufacturing maturity, and high-level integration with CMOS electronics [4]. Over the past decade, amazing progress has been made in implementing a wide variety of optical and electro-optical devices in silicon, including laser sources, modulators, detectors, waveguides, and filters [5]. With the integration of CMOS technology, large-scale arrays of photodiodes and phototransistors have been developed for fabricating multifunctional image sensors. The applicability is, however, strongly limited by the property of silicon. For example, for applications in the infrared (IR) spectrum which is below the energy bandgap of silicon, photodetectors based on non-silicon materials become necessary. With the rapid development of emerging applications, such as self-driving cars, authentication systems, augmented and virtual reality, and point-of-need health care [3], a new and important demand has arrived for advanced photodetectors based on special materials that possess ultrafast conversion, high-frequency communications, significantly wider detectable spectrum, and readily tunable bandgaps.

During the past decade, graphene and other 2D materials have received great interest in a large variety of research fields. These materials possess a combination of many exceptional properties, such as adjustable energy bandgap, direct bandgap of many monolayer 2D materials, easy stacking of different 2D materials for vertical heterojunctions by van der Waals force, scalable synthesis process and compatibility with traditional microfabrication technique, as well as being ultrathin and flexible. All these properties make them potentially extremely interesting in photodetector applications [4, 6]. Among them, graphene is the most famous and appealing material for the development of photodetectors. First, its zero bandgap enables charge carrier generation by light absorption over a very wide energy spectrum, ranging from ultraviolet (UV) to visible to IR to terahertz (THz) spectral regimes with a constant absorbance of ~2.3% per layer [7]. Second, its high carrier mobility allows to convert rapidly photons or plasmons to electrical currents or voltages [8, 9]. Third, the chemically passivated graphene surface greatly diminishes the influence of substrates and offers opportunities for integrated photonic devices on arbitrary substrates. Last, the strong quantum confinement resulting from the ultrathin 2D structure leads to many intriguing physical properties distinct from that of bulk materials [10]. For example, as a 2D material, its conductance is very sensitive to electrostatic perturbation by photogenerated carriers close to the surface [1], which is a desired property for high-gain photodetection.

Therefore, graphene can provide advanced or complementary techniques to silicon-based photodetectors. This chapter overviews the recent research progress of graphene-based photodetectors. We first summarize the performance metrics and basic physical mechanisms of photodetectors, then introduce the latest experimental realization of various photodetectors based on graphene, and finally discuss about the current challenges and outlook the future research directions.

21.2 Performance Metrics of Photodetectors

Typical figures of merit (FOMs) used to evaluate the performance of a photodetector include responsivity, detectivity, quantum efficiency, noise equivalent power (NEP), and response speed [1, 10]. Below is the introduction of these key metrics.

21.2.1 Responsivity (R_{ph})

Responsivity indicates the electrical output of a photodetector responding to an optical signal and is one of the most important characteristics for a photodetector. It is defined as the ratio of the photocurrent I_{ph} to the incident light power P_{in}, as

$$R_{ph} = I_{ph}/P_{in}; \tag{21.1}$$

or as the ratio of photovoltage V_{pc} to P_{in} as

$$R_{ph} = V_{pc}/P_{in}. \tag{21.2}$$

R_{ph} is often given in units of A/W. For a typical single-layer graphene (SLG) photodetector, responsivity is at the level of a few mA/W [10]. Also, responsivity is proportional to external quantum efficiency (EQE, the conversion rate from photons to electrons/holes) as

$$R_{ph} = \mathrm{EQE} \times \lambda q/hc, \tag{21.3}$$

where λ is the incident light wavelength, q is the absolute value of electron charges, h is the Planck constant, and

c is the light speed, and hence, the responsivity depends on the wavelength. For broadband photodetection, constant responsivity across a large spectral range is preferred, while single-color detectors need a sharp peak in a narrow range. In practice, power independent responsivity is also desirable in systems that respond linearly to optical input [10].

21.2.2 Quantum Efficiency

The external quantum efficiency (EQE) is the ratio between the number of electron-hole (e-h) pairs per second collected to produce the photocurrent I_{ph} and the number of incident photons per second, as

$$\mathrm{EQE} = \left(I_{ph}/q\right) / \left(P_{in}/E_{ph}\right), \tag{21.4}$$

where E_{ph} is the incident photo energy. Similarly, internal quantum efficiency (IQE) is the ratio between the e-h number and the number of absorbed photons, as

$$\mathrm{IQE} = \left(I_{ph}/q\right) / \left(A_{abs}P_{in}/E_{ph}\right), \tag{21.5}$$

where A_{abs} is the absorbed fraction.

21.2.3 Noise Equivalent Power (NEP)

The noise equivalent power (NEP) is the minimum measurable power [11] or the signal power for a given bandwidth when the signal-to-noise ratio is unity [1]. It is calculated as

$$\mathrm{NEP} = P_{in}/\sqrt{B} = i_n/R_{ph}, \tag{21.6}$$

where B is frequency bandwidth of the photodetector and i_n is the noise current. NEP is thereby in units of W $\mathrm{Hz}^{-1/2}$.

21.2.4 Detectivity (D^*)

The specific detectivity is another typical FOM used to characterize photodetector performance. It is the minimum detectable level of light and is calculated as

$$D^* = \sqrt{A \cdot B}/\mathrm{NEP} = \sqrt{A \cdot B}\, R_{ph}/i_n, \tag{21.7}$$

where A is the area of the photosensitive region. D^* is in units of Jones with 1 Jones = 1 cm $\mathrm{Hz}^{1/2}$ W^{-1}, in recognition of the work of R. C. Jones on sensitivity of radiation sensors [1].

21.2.5 Linear Dynamic Range (LDR)

The linear dynamic range (LDR) is the illumination intensity range within which the current response of a photodetector scales linearly with the light intensity [12] and is given by

$$\mathrm{LDR} = 20 \log \left(J_{ph}/J_d\right), \tag{21.8}$$

where J_{ph} is the photocurrent density measured at a light intensity of 1 $\mathrm{mW/cm}^2$ and J_d is the dark current density. In practice, a large LDR is desired so that a photodetector can detect both high- and low-intensity lights.

21.2.6 Response Speed

Response speed characterizes the capability of a photodetector to detect a signal at a certain rate [10]. In the frequency domain, speed is defined by the frequency at which responsivity is reduced to 50% of its maximum value. In the time domain, response time is used to characterize the response speed and defined as the time required for a transient output signal to reach 0.707 of its steady-state change upon a sudden change of the incident light. For some systems, the response time may be asymmetric between light switch ON and OFF. Then the response speed is characterized by the rise and fall times at 10% and 90% of the maximum photocurrent, respectively [12]. Fast operation (up to tens of GHz) is extremely important for telecommunication and interconnection, but for other applications such as sensing and imaging, only moderate speed (a few kHz) is required [10].

21.2.7 Photoconductive Gain (G_{ph})

Photodetectors are commonly benchmarked by their photoconductive gain , the number of carriers detected for each single incident photon. It can be quantified by the ratio of the lifetime (τ_{trap}) of the trapped carriers to the drift transit time ($\tau_{transit}$), as

$$G_{ph} = \frac{\tau_{trap}}{\tau_{transit}}, \text{ with } \tau_{transit} = L^2/\mu V_{bias} \tag{21.9}$$

where L is the source-drain separation distance (channel length), μ is the carrier mobility, and V_{bias} is the bias voltage.

It is worth mentioning that in many cases, trade-offs have to be made between different FOMs [10]. For instance, responsivity can be effectively increased through integration with extra light absorbers, but often the response speed is sacrificed. More relevant discussion is included in the following sections.

21.3 Physical Mechanisms for Photodetection

Several different mechanisms have been realized in graphene and 2D materials-based photodetection and other optoelectronic applications, including the photovoltaic effect, the photo-thermoelectric effect, the bolometric effect, the photogating effect, and the plasma-wave-assisted mechanism, as summarized in Fig. 21.1 and detailed below.

21.3.1 Photovoltaic Effect

Photovoltaic (PV) current is generated through separating photon-induced electron-hole (e-h) pairs either by built-in electric fields at a p-n junction or a metal-semiconductor Schottky junction [13, 14] (Fig. 21.1a) or by the external electric field under an applied bias voltage. As graphene is a semimetal, external electric field is not favored due to the very high dark current and power consumption. The built-in field can be created by several techniques, including local chemical doping [15], splitting gates [13, 16], or inherent work function difference between graphene and a contacting metal [17]. In a splitting gate structure, the doping can be tuned to be either p- or n-type, depending on the applied gate voltages. In graphene-metal junctions, the doping is fixed, typically as p-type for metals that have higher work function than graphene (4.45 eV). The electric field is the only factor to determine the photocurrent. Thus, photocurrents switch sign when going from p-n junction to n-p junction or from p-p^+ junction to p^+-p junction [1].

A special phenomenon for graphene is the carrier multiplication (Auger-type) impact ionization [10] where the strong carrier-carrier scattering, owing to the zero bandgap, leads to the conversion of one high-energy electron-hole pair into multiple electron-hole pairs of lower energy [18–20], which potentially enhances the overall photodetection efficiency. This process fundamentally differs from the impact ionization in traditional semiconductors where a sufficiently large electric field increases the kinetic energy of a carrier which then loses energy to create other low-energy carriers, resulting in avalanche breakdown [10].

21.3.2 Photothermoelectric Effect

The photothermoelectric (PTE) effect refers to the conversion of light-induced temperature gradient to an electric voltage. Due to the large thermal conductivity of graphene, the PTE effect generated by lattice heating is not significant. In contrast, significant photovoltage can be produced by photogenerated hot electrons. Due to the strong electron-electron interactions, photo-excited electron-hole pairs lead to ultrafast (~10–50 fs) heating of the carriers in graphene [21–23]. Because of the large optical phonon energy in graphene (~200 meV), the carriers can remain at a temperature much higher than the lattice temperature for a few picoseconds. The final thermal equilibration between the hot electrons and the lattice needs a nanosecond timescale due to the slower scattering between charge carriers and acoustic phonons [24, 25]. As a result, the temperature difference between hot carriers (e.g., in two graphene regions with different doping, Fig. 21.1b) can produce a photovoltage, $V_{PTE} = (S_1 - S_2)\Delta T_e$, where $S_{1,2}$ (in V K^{-1}) is the thermoelectric power (Seebeck coefficient) in the two different graphene regions and ΔT_e is the electron temperature difference between the regions. Photoresponse generated by hot carriers rather than lattice heat-

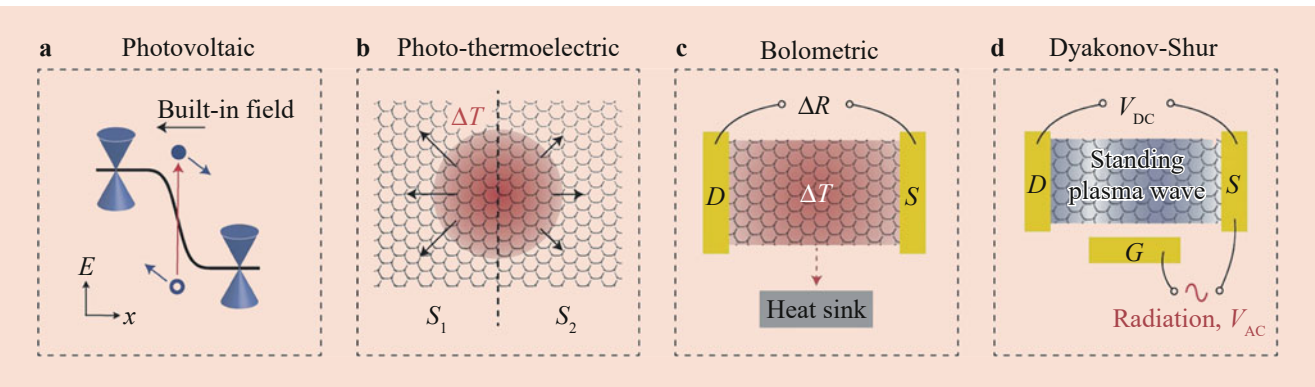

Fig. 21.1 Schematic of four typical photocurrent generation mechanisms: (**a**) photovoltaic (PV) effect where electron (solid circle)-hole (open circle) separation by an internal (built-in) electric field, (**b**) photothermoelectric (PTE) effect, (**c**) bolometric effect, and (**d**) plasma-wave-assisted mechanism. In (**b**, **c**), red-shaded area indicates elevated electron temperature where ΔT is the temperature gradient, ΔR is the resistance across the channel, and S_1 and S_2 are Seebeck coefficient in graphene areas with different doping. In (**c**, **d**), S and D indicate source and drain, respectively, and G the gate; V_{DC} photogenerated dc voltage; V_{AC}, ac voltage applied to the gate. (Adapted with permission from [1] Copyright (2014) Springer Nature)

ing can achieve wide bandwidths, like in the case of PV photodetectors. The PTE effect typically dominates in graphene p-n junctions [16, 26] or in suspended graphene [27].

21.3.3 Bolometric Effect

The bolometric effect refers to the change in the transport conductance caused by light heating (Fig. 21.1c). Because this photodetection relies on light-induced conductance change, instead of direct photocurrent generation, it requires an externally applied bias and can operate on homogeneous graphene (no p-n junction is needed). The conductance change may result from the temperature-dependent carrier mobility and/or the change of carrier density.

21.3.4 Plasma-Wave-Assisted Mechanism

In a field-effect transistor (FET), when exposed to an oscillating radiation field (Fig. 21.1d), a finite dc voltage may be generated. Based on this rectification, Dyakonov and Shur [28, 29] proposed a photodetection scheme. The 2D electron gas hosted in an FET can act as a cavity for plasma waves (collective density oscillations) [1]. For weakly damped plasma waves (the transport time of a plasma wave from the source to the drain is shorter than the momentum relaxation time), their constructive interference can be used to detect the radiation with a resonantly enhanced response. This is the so-called resonant regime of plasma-wave photodetection and can produce a signal 5–20 times stronger than the broadband nonresonant signal in the case of overdamped plasma waves (plasma waves launched at the source decay before reaching the drain) [29]. Dyakonov and Shur [29] showed that even if the incoming field is ac, the photovoltage response of a 2D electron system in a FET still contains a dc component, which provides rectification of the signal. This is particularly useful for the detection of THz radiation. Detection of THz radiation in graphene FETs has been theoretically discussed [30] and experimentally demonstrated [31, 32].

21.3.5 Photogating Effect

The photogating effect is based on light-induced modification of the graphene carrier density and hence its conductance [1]. Typically, one type of photogenerated carrier is captured by the trap centers or transferred from external source, both of which result in change of carrier density. Therefore, the photoconductive gain, G_{ph}, can be strongly enhanced by using a high-mobility conductor, such as graphene, and by a long lifetime. Also responsivity based on the photogating effect can be very large, up to millions of A/W because photo-induced carriers can move several times through the channel before recombination, providing a significant optical gain [10]. In contrast, responsivity in the PTE and bolometric regimes is limited to less than a few mA/W. However, longer photocarrier lifetime reduces the operation speed. And the photoconductive detectors may exhibit high dark current, which influences the noise equivalent power and detectivity.

21.4 Practical Realization of Graphene Photodetectors

In practice, a large variety of graphene photodetectors have been developed based on different mechanisms, heterogeneous junctions with other materials, and advanced architectures. This section summarizes the representative implementations of these photodetectors.

21.4.1 Metal-Graphene-Metal (MGM) Photodetectors (PV and PTE Effects)

The MGM photodetectors (Fig. 21.2) were the first and simplest class of graphene-based photodetectors to be investigated. In early reports [9, 33–35], photocurrent was generated through the PV effects by local illumination of one of the metal/graphene interfaces of a back-gated graphene FET. The field arising from charge transfer from the contact metal to graphene [36, 37] can thus be adjusted by choosing the proper metal [34, 38]. Besides the PV effect, the PTE effect may also dominate the photoresponse in the vicinity of p-n junctions or interfaces of SLG and bilayer graphene (BLG) [26, 27, 39]. The PTE effect can be distinguished from the PV effect according to the sign of the photocurrent. Different from the PV current, the PTE current reverses the direction in bipolar p-n junctions and also unipolar p^+-p or n-n^- junctions [26], due to the change of transconductance upon transport between different doping region transports. The relative contributions of the PTE and PV effects to the photocurrent can be controlled through adjusting the wavelength. At longer wavelengths, the PV effects become pronounced.

Because the photocurrent is only generated in the vicinity of metal/graphene interface region, interdigitated finger structures (Fig. 21.2b) with asymmetric electrode metals are often used to increase the effective photodetection area [9] and suppress the dark current. Thanks to the high carrier mobility and short carrier lifetime in graphene, MGM photodetectors can operate at high data rates. In single metal-graphene junctions, it has been demonstrated that photoresponse does not degrade at a modulation frequency of 40 GHz [8] and all-optical measurement gave an intrinsic bandwidth of 262 GHz. It is worthy of mentioning that

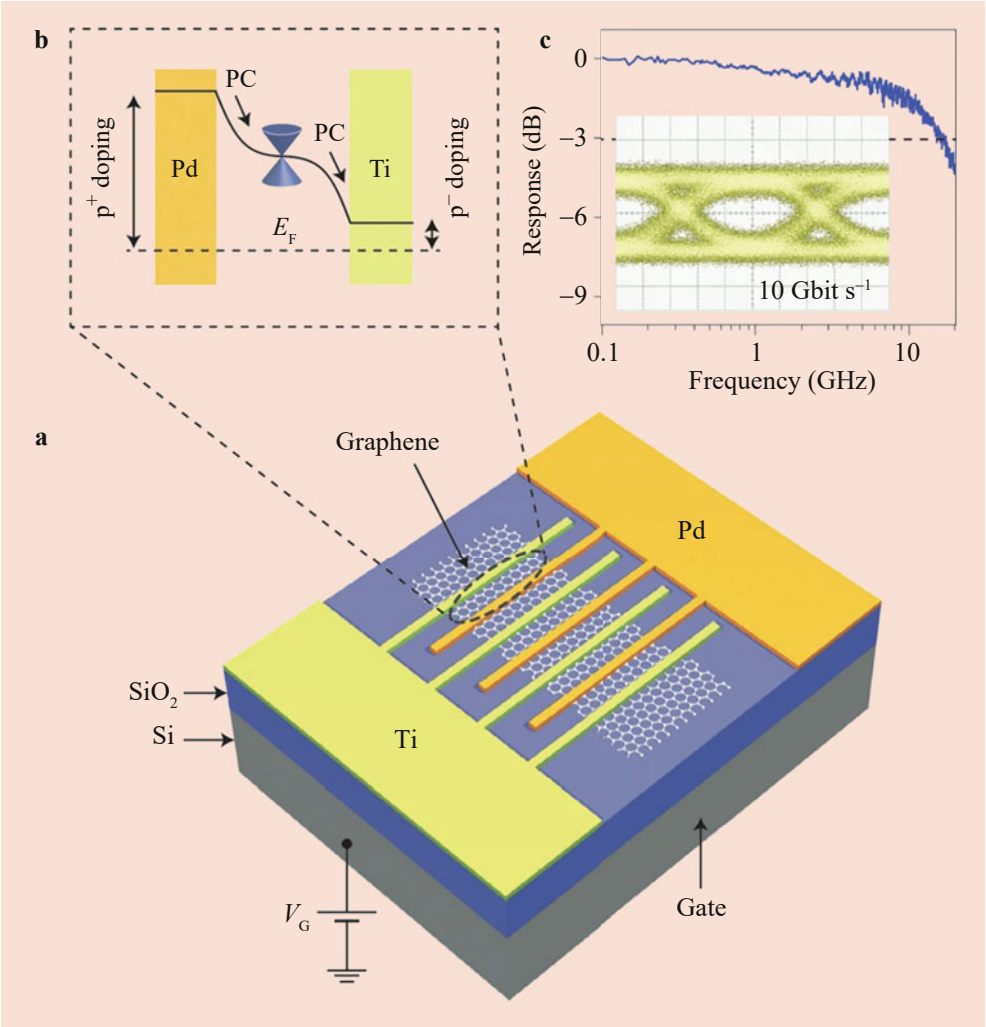

Fig. 21.2 A typical metal-graphene-metal photodetector with asymmetric contacts: (**a**) Three-dimensional schematic. (**b**) Energy band and profile, where the arrows and Dirac cone indicate the electron flow and the charge neutrality point, respectively. PC stands for photocurrent. (**c**) High-frequency response. Inset: eye diagram. (Reproduced with permission from [9] Copyright (2012) Springer Nature for (**a**, **c**) and from [1] Copyright (2014) Springer Nature for (**b**))

both PV and PTE effects are compatible with the high bandwidths owing to the decoupling of electron and lattice temperature [1].

21.4.2 Graphene-Based Bolometers

Bolometric responses have been observed at room temperature when SLG is biased [17, 40]. The dominant factor for the conductance change (either photo-induced excess carriers or temperature-dependent mobility) can be controlled through adjusting Fermi level (E_F) of graphene [17]. However, the weak temperature dependence of the electrical resistance in graphene [41] makes it difficult to extract the temperature difference through electrical transport measurements, resulting in a small responsivity at the level of 0.2 mA/W [17]. To solve this problem, several strategies have been demonstrated, such as introducing disorder [42], patterning nanostructures [43], and opening a bandgap in bilayer graphene [40]. As shown in Fig. 21.3a, an extra optically transparent top gate was applied to a dual-gated bilayer graphene device (Fig. 21.3a) to open a bandgap at the Dirac point [44, 45] and obtain electron temperature (T_e)-dependent resistance [44] to generate bolometric photoresponse [40]. The devices attain a high voltage of 2×10^5 V W^{-1} and a very low NEP of 33 fW Hz$^{-1/2}$ at 5 K as compared with commercial silicon bolometers (200–2000 fW Hz$^{-1/2}$). Their intrinsic speed exceeds 1 GHz at 10 K, three to four orders of magnitudes higher than commercial silicon bolometers and superconducting transition-edge sensors at similar temperatures. In addition, a graphene-superconductor tunnel junction bolometer (Fig. 21.3b) has also been demonstrated at radio-frequency regions [46], which should also apply for optical detection [1].

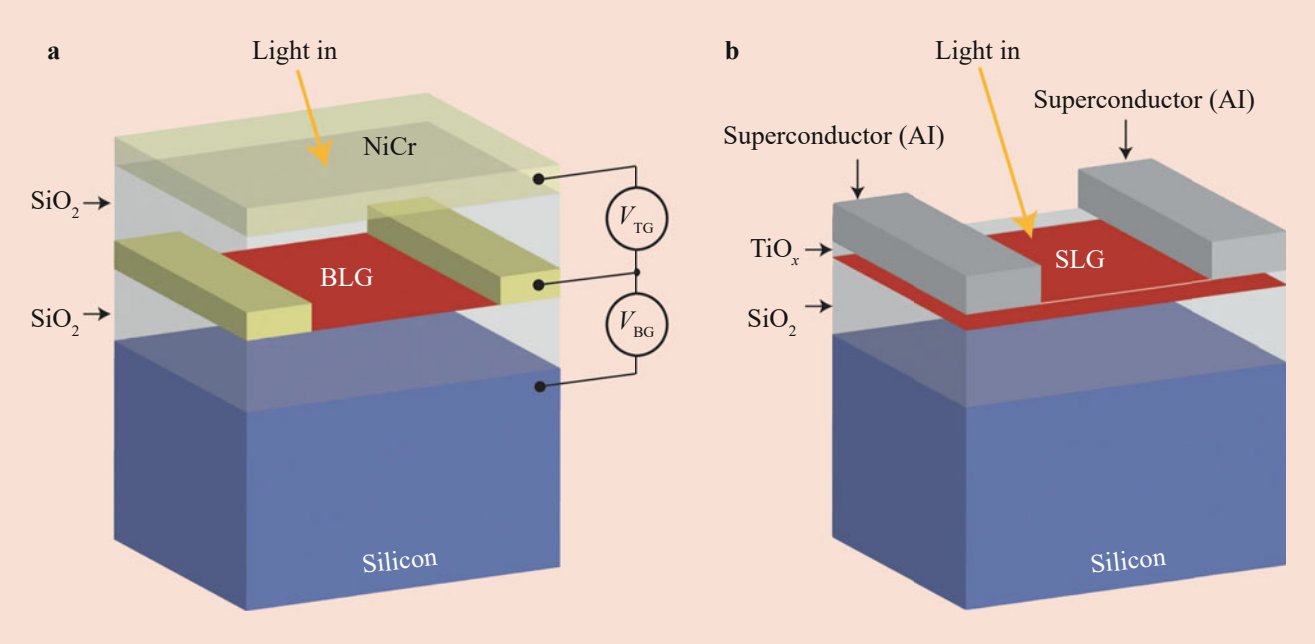

Fig. 21.3 Graphene-based bolometers. (**a**) Device structure of a dual-gated bilayer graphene bolometer [40]. V_{TG} and V_{BG} are top gate bias and back-gate bias, respectively. (**b**) Device structure of an SLG-aluminum tunnel junction bolometer [46]. (Reproduced with permission from [1] Copyright (2014) Springer Nature)

21.4.3 Plasmonics-Enhanced Graphene Photodetectors

The excitation of surface plasmons is an effective method to increase the photoresponse of graphene photodetectors. Localized plasmons in metal nanostructures were first used along with graphene to obtain surface-enhanced carrier density (Fig. 21.4a, b) [48] and Raman scattering [50] and to enhance strong fields in subnanometer gaps [51]. The introduction of plasmonic nanostructures near the contacts [49] of graphene-based photodetectors (Fig. 21.4c–e) has also been demonstrated to significantly improve the device performance (Fig. 21.4e). In addition, nanostructures with geometries resonant at desired wavelengths offer opportunities for selective amplification, potentially allowing light filtering and detection, as well as polarization determination in a single device [52]. As compared with traditional devices, the plasmonic structures greatly improve the frequency performance because their contribution to the capacitance (fractions of femtofarads) is negligible, whereas they can significantly reduce the contact resistance.

Besides, field enhancement by plasmons can also improve photodetection performance due to the intrinsic collective charge oscillations of the 2D electron liquid inside graphene (Fig. 21.4f, g). The high carrier mobility and 2D character of graphene greatly enhance its light absorption [53], which provides an ideal solution to make use of graphene as both photodetector and plasmonic enhancers. As is shown in Fig. 21.4e, graphene nanoribbon arrays on SiO_2 with different widths have been demonstrated as room-temperature tunable IR photodetectors with a performance improvement by 1500% [47].

21.4.4 Detectors Based on Photogating

A gain mechanism that provides multiple electrical carriers per single incident photon is crucial for photon detection at very low intensities, even approaching the single-photon level [1]. This can be achieved by effectively absorbing light with appropriate sensitizing centers and then transferring the carriers into the conductor (photogating effect, Fig. 21.5a) [54, 55]. It often results in a shift in the typical resistance versus gate-voltage curve, as shown in Fig. 21.5b. Graphene is excellent for room-temperature high-gain photodetection because of its high mobility (thus short carrier transit time) and its strong conductance dependence on the electrostatic perturbation by photogenerated carriers close to the surface. As a good example, colloidal quantum dots, such as PbS [54] (Fig. 21.5), CdS, or ZnO [56], are widely used to sensitize graphene. They have strong light absorption and bandgap tunability and can cover the absorption range from ultraviolet to SWIR [57]. Graphene decorated with PbS quantum dots can exhibit a high gain of 10^8 corresponding to $R_{ph} \sim 10^7$ A/W (at room temperature) for low light intensities

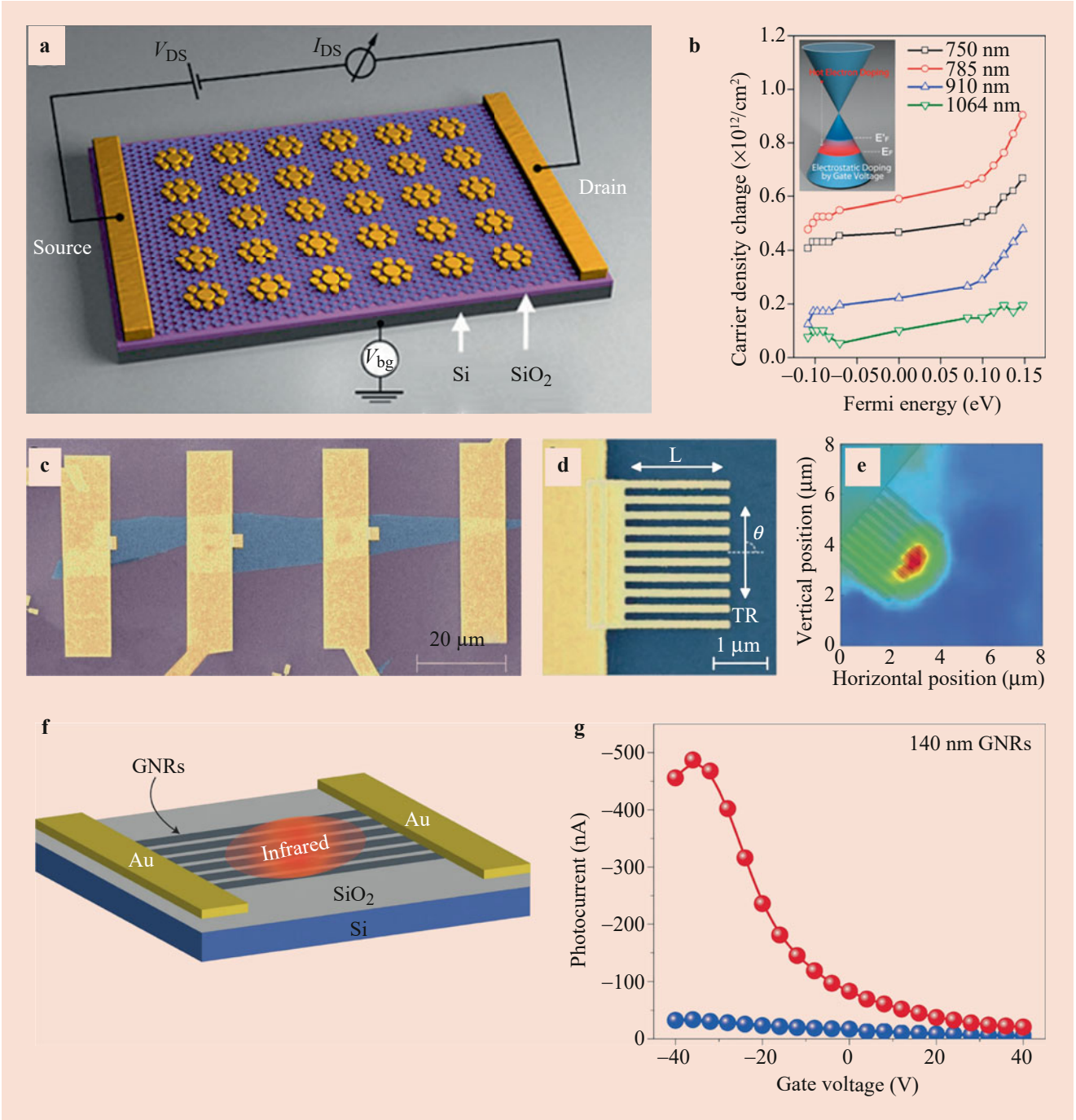

Fig. 21.4 Photodetectors enhanced by metallic plasmonic nanostructures and intrinsic plasmons. (**a**) Schematic of plasmonic antennas on SLG. (**b**) Light-induced carrier density change with respect to Fermi energy at selected wavelengths. Inset: energy diagram of the graphene Dirac cone, with antenna, under laser excitation. (**c**) Photodetectors with plasmonic nanostructures at the contacts (in false colors). Blue, graphene; purple, SiO_2 (300 nm); yellow, Ti/Au electrodes. (**d**) A contact with a "finger structure" in (**c**). Longitudinal (L) and transverse (TR) incident light polarizations are indicated. (**e**) Photovoltage map of one of the nanostructured contacts, similar to the one shown in (**d**). Color scale runs from −4 μV (blue) to 12 μV (red).(**f**) Schematic of a nanoribbon array infrared photodetector. GNRs: graphene nanoribbons [47]. (**g**) Photocurrent against gate voltage for the GNR (ribbon width 140 nm) detectors with (red spheres) and without (blue spheres) plasmon excitation [47]. (Reproduced with permission from [48]. Copyright (2012) American Chemistry Society for (**a**, **b**), from [49] Copyright (2011) Springer Nature for (**c**–**e**), and from [1] Copyright (2014) Springer Nature for (**f**, **g**))

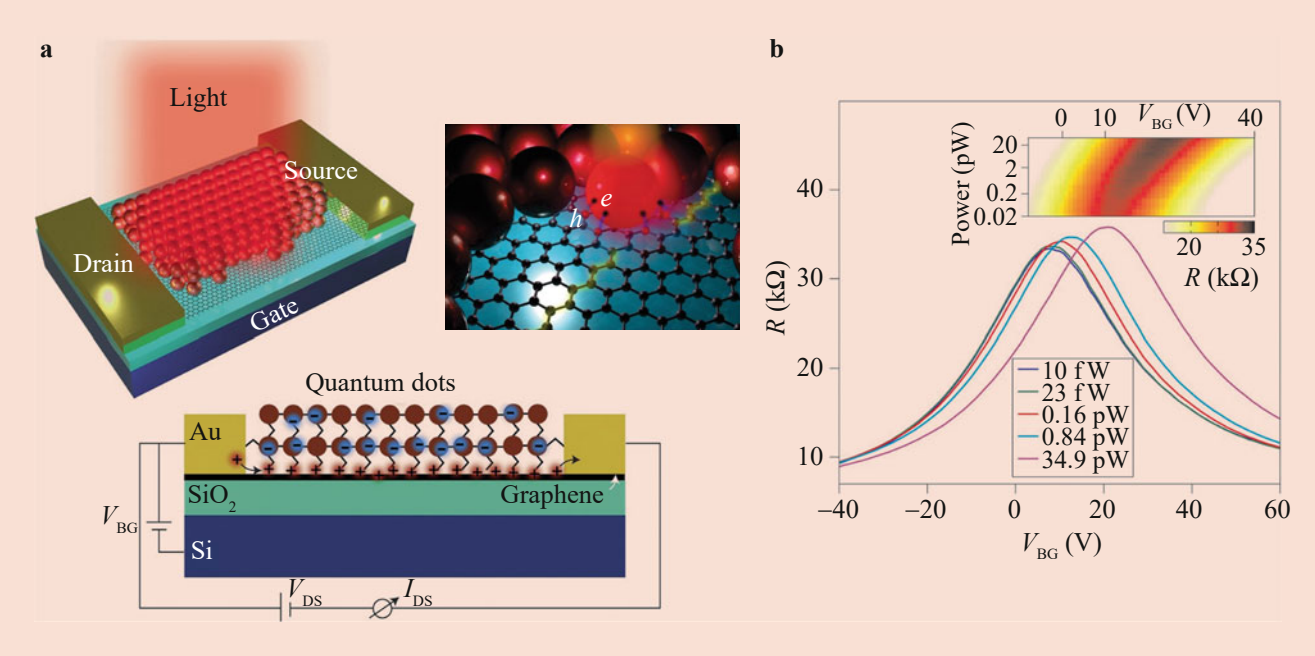

Fig. 21.5 Graphene photodetectors with sensitizing centers (photogating effects). (**a**) Schematics of photodetectors based on quantum dots (top left and bottom) and the *e*-*h* separation in the quantum dots (top right). (**b**) The dependence of resistance on the back-gate voltage (V_{BG}) in a graphene-PbS quantum dot hybrid structure. Under stronger illumination, the Dirac point shifts to higher V_{BG} due to the photogating effects. Inset: map of graphene resistance against optical power. (Reproduced with permission from [54] Copyright (2012) Springer Nature)

$\sim 10^{-14}$ W [54]. Given the high QE (>25%), specific detectivity of 7×10^{13} Jones, video imaging speed ~30–60 Hz, and low NEP $\sim 10^{-17}$ W (at the noise floor of 0.1 Ω $Hz^{-1/2}$), this hybrid system is a promising platform for visible and SWIR applications [1].

21.5 Graphene-Based Heterostructures for Photodetectors

Although graphene-based optoelectronic devices are being extensively studied and some have already reached a competitiveness level comparable to conventional semiconductor devices [1, 58], several intrinsic drawbacks of graphene still limit the applicability, including low light absorbance (only 2.3%) of SLG and short light-matter interaction length causing ineffective light harvesting, ultrashort lifetime of excitons in pure graphene leading to fast carrier recombination, and low sensitivity of graphene-based detectors. To essentially address these drawbacks, various graphene-based heterostructures have been developed for photodetector applications to improve the performance [1, 12]. Here, we summarize these heterogeneous structures with different materials.

21.5.1 Graphene/Silicon

Graphene/silicon Schottky junctions are among the most studied devices for graphene heterojunction photodetectors where silicon absorbs light and graphene acts as an optically transparent charge carrier collector. The zero-gap and semimetallic properties of graphene are very promising for the wideband photodetection from microwave to UV regimes. The heterojunctions significantly increase the speed of carrier separation due to the built-in electric field, while the photocarrier lifetime is not reduced evidently under 1550 nm illumination [61]. As a result, an IQE of 10% was obtained for graphene/Si junctions in contrast to an IQE ~1% in regular Schottky junctions. The device performance can be further improved through introducing metal nanoparticles (such as Pt nanoparticles) [62] or an extra MoO_3 layer [63] for surface doping. To reduce the leakage current in the graphene/Si Schottky junctions, a thin interface layer of SiO_2 can be employed [64]. In particular, through the scanning photocurrent measurement technique, Riazimehr et al. [59] find that higher photocurrent (corresponding to a responsivity about 0.3 A/W) is generated in the graphene/SiO_2/Si region as compared to the graphene/Si region (responsivity about 50 mA/W) at reverse biases above a threshold voltage (Fig. 21.6a, b). This behavior is independent of excitation

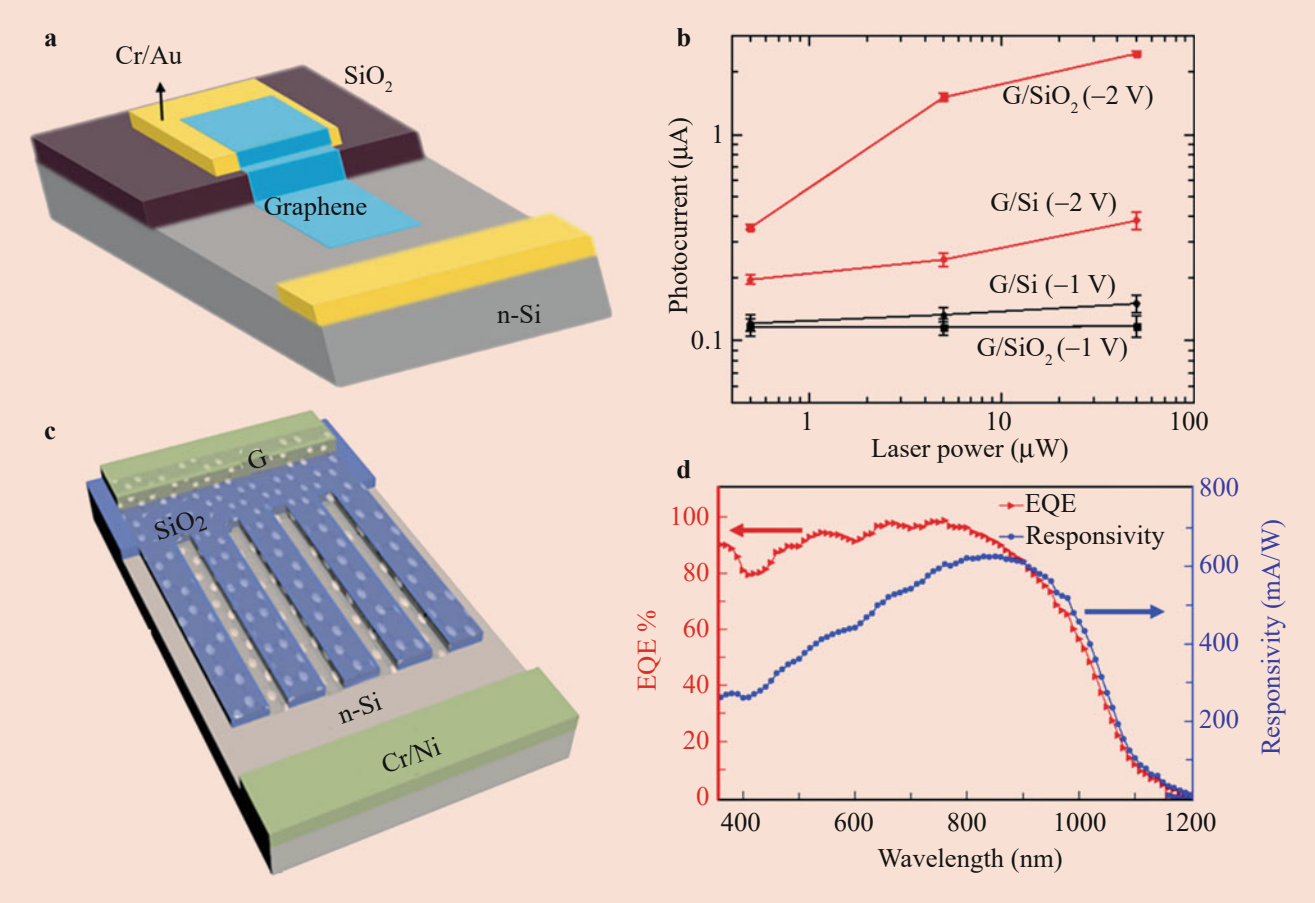

Fig. 21.6 Photodetectors based on graphene/siliconheterostructures. (**a**) Schematic of a graphene/silicon photodiode. (**b**) Photocurrent against laser power for the photodiode in (**a**) at different reverse biases in the graphene/Si (G/Si) and graphene/SiO_2 (G/SiO_2) regions. (**c**) Schematic of the patterned graphene/silicon photodiode where graphene is in contact with interdigitated SiO_2/Si structured substrates. (**d**) Wavelength-dependent EQE and responsivity of the patterned photodiode in (**c**). (Reproduced with permission from [59] Copyright (2017) American Chemistry Society (https://pubs.acs.org/doi/full/10.1021/acsphotonics.7b00285, further permission should be directed to ACS) for **a**, **b** and from [60] Copyright (2018) American Chemistry Society (https://pubs.acs.org/doi/10.1021/acsphotonics.8b00951, further permission should be directed to ACS) for **c**, **d**)

laser power and could be ascribed to the formation of an inversion layer in the Si layer under the graphene/SiO_2 junction. Furthermore, when the graphene/SiO_2/Si region is patterned in interdigitated structure (Fig. 21.6c) [60], a high EQE of >80% is achieved for wavelengths ranging from 380 to 930 nm with the maximum EQE of 98% at 850 nm, where the responsivity also peaks to 635 mA/W (Fig. 21.6d).

The performance improvement can also rely on porous Si and Si NWs. As shown in Fig. 21.7a–c, the graphene/porous Si Schottky diodes have achieved an excellent performance of responsivity up to about 0.3 A/W, as well as 60% EQE and 3 μs response time [65]. Alternatively, the NIR photodetectors based on a graphene/silicon nanowire array decorated with Au nanoparticles (Fig. 21.7d) [66] exhibit high performance of 10^6 light-to-dark current ratio (Fig. 21.7e) and high response speed (rise/fall time of 73/96 μs, Fig. 21.7f), possibly resulting from the enhanced optical absorption due to the strong optical trapping effect of silicon nanowire arrays and the surface plasmon coupling by Au nanoparticles.

21.5.2 Graphene/III–V Semiconductors

Heterojunctions between graphene and III–V semiconductors have also been used for photodetectors. GaN and GaAs are direct bandgap semiconductors with excellent optical/-electrical properties for various photodetection applications. Graphene/GaN Schottky diode [69] has shown high light-to-dark current ratio (10^5) under UV illumination. In addition, graphene/GaN nanowire array (Fig. 21.8a–c [67]) shows extremely high responsivity of 25 A/W at 357 nm, validating the promising application of graphene/GaN junctions in the UV region. On the other hand, graphene/GaAs Schottky

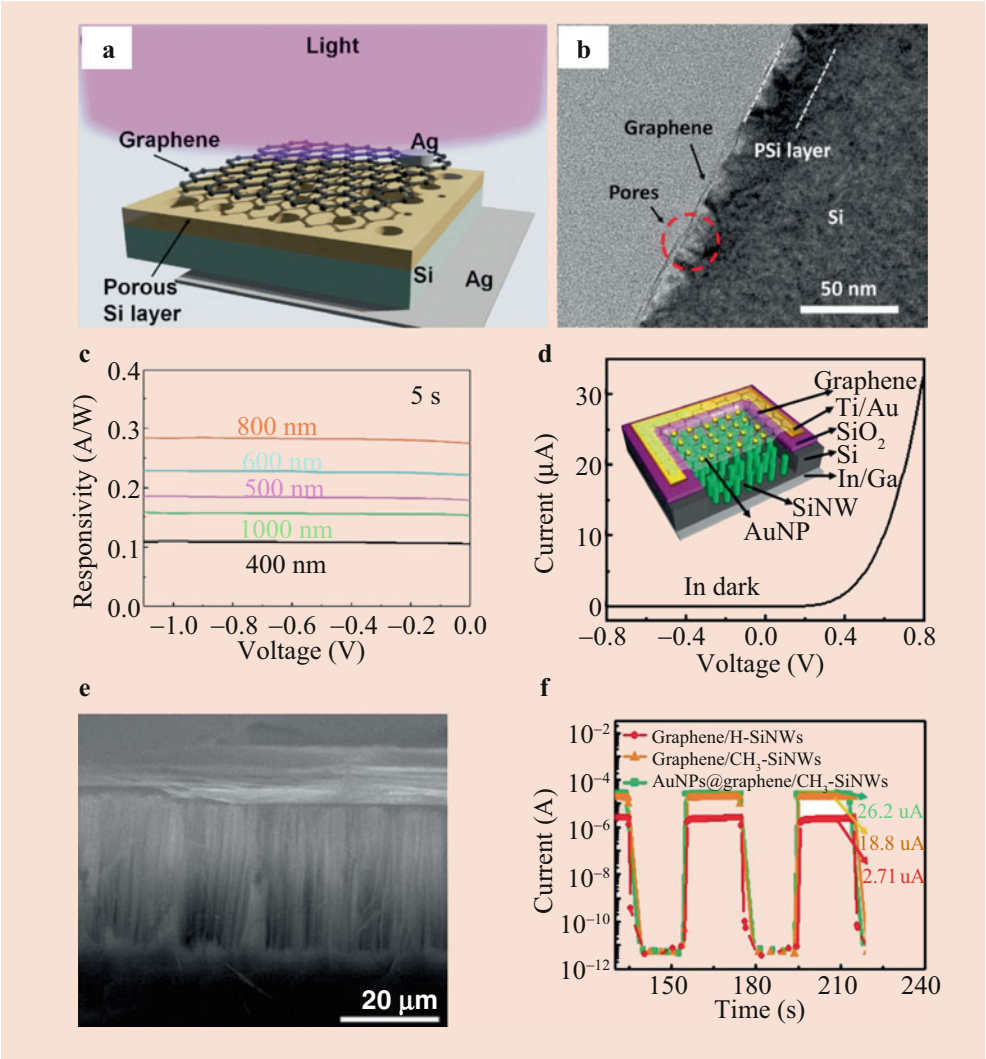

Fig. 21.7 Photodetectors based on graphene/silicon (porous or nanowire) heterostructures. (**a**) Schematic of graphene/porous silicon/n-silicon photodetectors with Ag top and bottom electrodes under light illumination [65]. (**b**) Cross-sectional transmission microscopy (TEM) image of graphene/porous Si junction. (**c**) Responsivity of a graphene/porous Si photodetector under illumination at various wavelengths from 400 to 1000 nm. (**d**) Schematic (inset) and current-voltage curves of the graphene/silicon nanowire array photodetectors enhanced by Au nanoparticles [66]. (**e**) Cross-sectional SEM image of the graphene/Si nanowire photodetector. (**f**) Photoresponse of three representative devices under alternate switching on and off of the NIR illumination (wavelength 850 nm, at the power of 3 mW/cm^2) at zero bias voltage. (Reproduced with permission from [65] Copyright (2014) American Chemical Society for **a**–**c** and from [66] Copyright (2014) Springer Nature for **d**–**f**)

junctions are promising for NIR light detection [68]. As shown in Fig. 21.8d–f, graphene/GaAs nanocone arrays exhibit reproducible photodetector performance of 10^4 light-to-dark current ratio, 1.73 mA/W responsivity, and fast response speed with rise/fall times of 72/122 μs. Recently [70], using a thin layer of AlO_x as a surface protective layer to suppress carrier recombination and a barrier to reduce dark current, the performance of graphene/GaAs NIR photodetectors can be further improved, with the responsivity increased to 5 mA/W and rise/fall times decreased to 320/380 ns.

21.5.3 Graphene/Organic Semiconductors

Thanks to their simple solution processability at low temperatures [71], flexibility, low cost, and lightweight, organic semiconductors have attracted great interest in forming heterojunctions with graphene for photodetector applications. As shown in Fig. 21.9, a graphene/pentacene heterostructure can be fabricated on flexible substrates to serve as a multifunctional photodetection with nonvolatile memory function for storing optical signals [72]. The device exhibits excel-

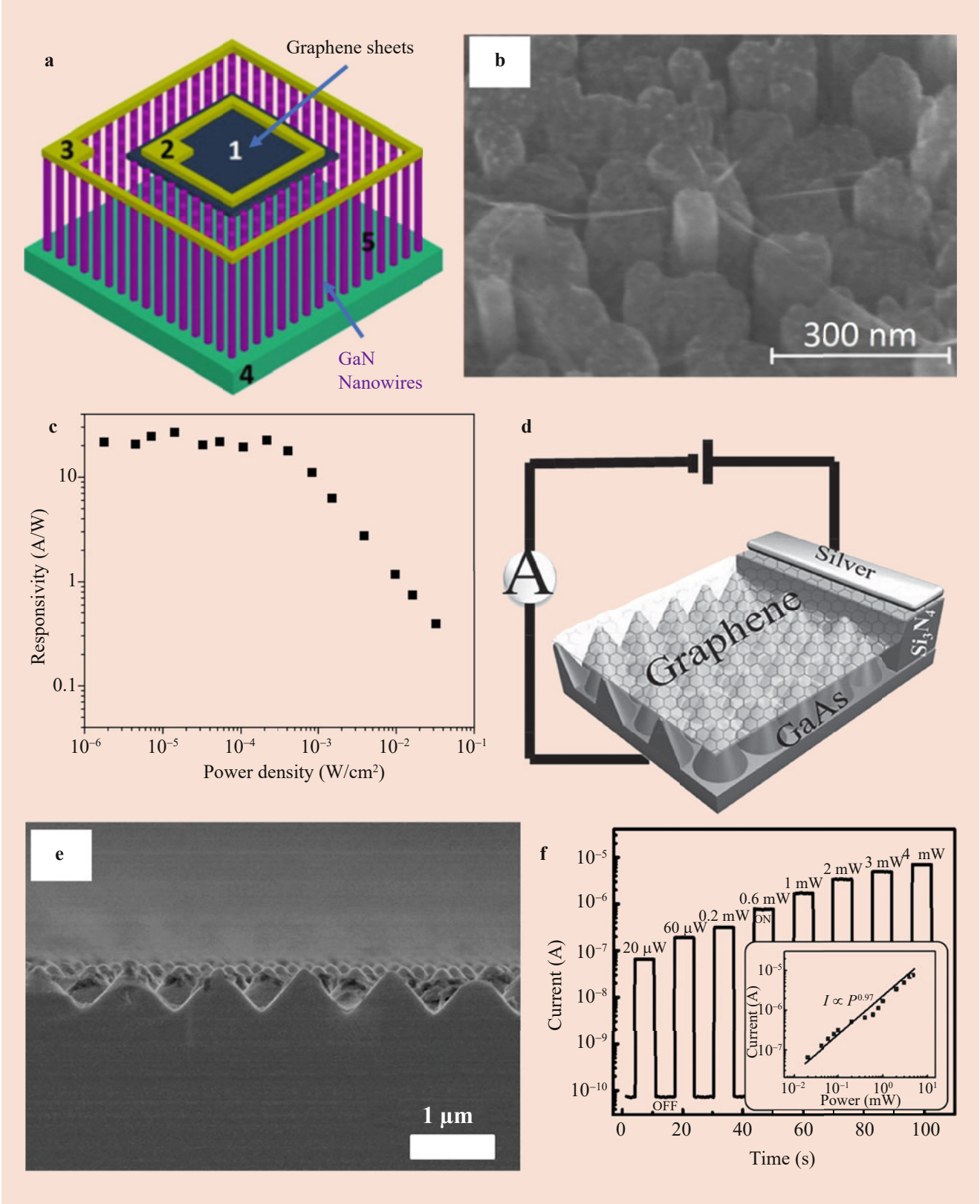

Fig. 21.8 Photodetectors based on graphene/III–V semiconductor heterostructures. (**a**) Schematic of a photodetector based on GaN nanowire array covered by graphene sheet. The yellow parts are electrodes. (**b**) Scanning electron microscopy (SEM) image of a graphene film on GaN nanowires [67]. (**c**) Responsivity for various incident power densities. (**d**) Schematic of a graphene/GaAs nanocone array photodetector [68]. (**e**) A typical cross-sectional SEM image of the n-GaAs nanocone array after etching. (**f**) Photoresponse of the graphene/GaAs nanocone array photodetector under various light intensities. Inset: the fitting of the relationship between the photocurrent and light intensity. (Adapted with permission from [67] Copyright (2013) AIP Publishing for **a**–**c** and from [68] Copyright (2014) John Wiley and Sons for **d**–**f**)

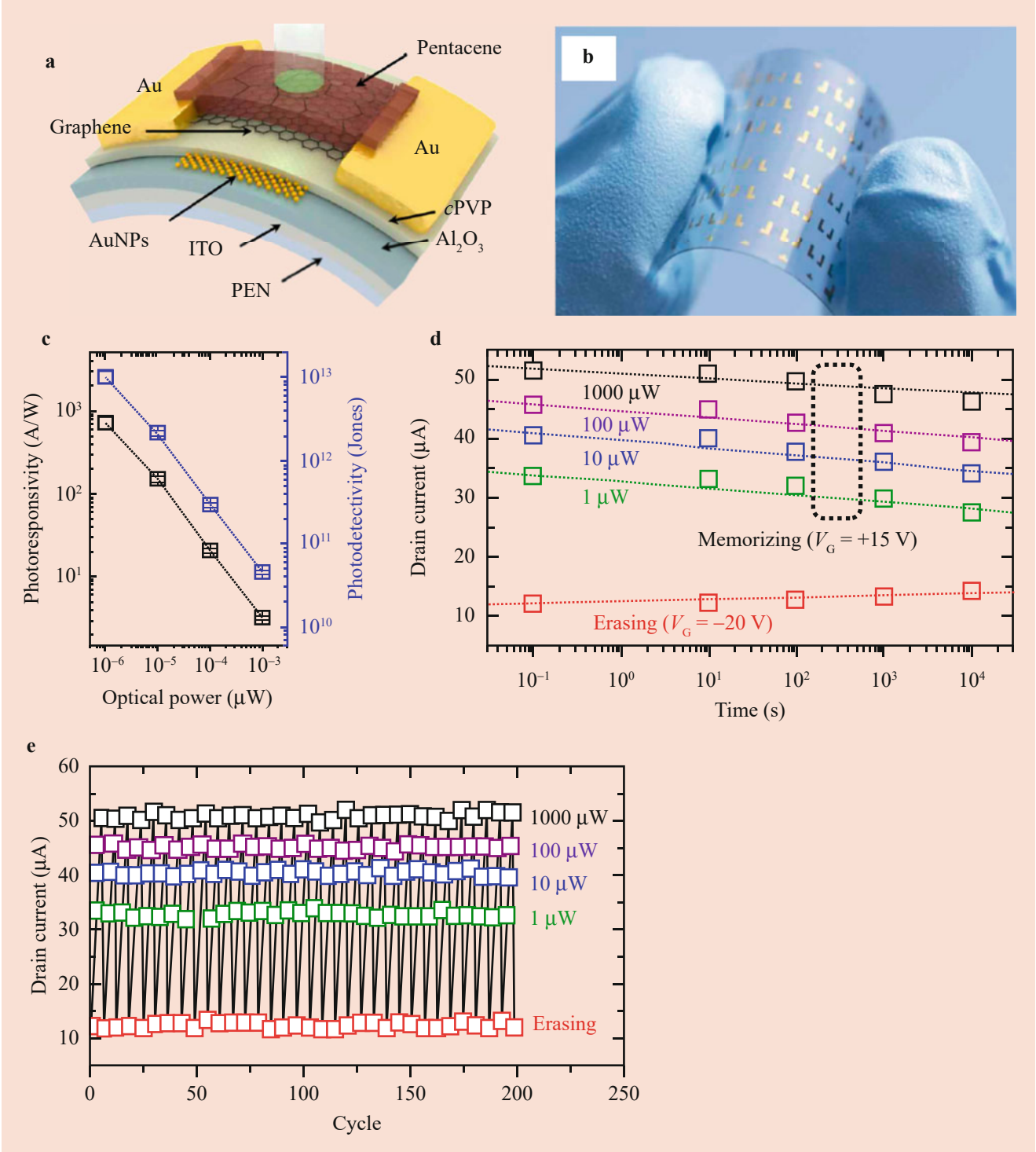

Fig. 21.9 Photodetectors based on graphene/organic semiconductor heterostructure. (**a**) Schematic of a graphene photodetector on flexible substrates with a pentacene light absorption layer and an Au nanoparticle charge trapping layer. (**b**) Photograph of the device. (**c**) Responsivity and specific detectivity at different incident illumination power. (**d**) Retention time and (**e**) cycling test of the device with a memory functionality under various illumination powers. (Adapted with permission from [72] Copyright (2015) American Chemical Society)

lent performance at 400–800 nm with maximum responsivity and specific detectivity of 700 A/W and of 10^{13} Jones (Fig. 21.9c), respectively. It can also retain the photocurrent for a long time exceeding 10^4 s (Fig. 21.9d). The photocurrent remains invariant for more than 200 cycles and increases with the illumination power (Fig. 21.9e).

In addition, monolayer organic C8-BTBT crystals can also be integrated on graphene by van der Waals epitaxy [73] to obtain high-performance photodetectors with the responsivity larger than 10^4 A/W. By using multilayer C8-BTBT, the responsivity can be further increased to 4.76×10^5 A/W. The excellent performance may be attributed to the ultrahigh photoconductive gain and the high interfacial charge transfer efficiency due to the high quality of C8-BTBT layer and graphene/C8-BTBT interface [12]. However, the multilayer photodetection has much longer response time (~830 ms) than the monolayer device (~25 ms), probably due to the interlayer hopping of trapped carriers within the C8-BTBT crystals.

21.5.4 Graphene/Perovskites

Organic-inorganic halide perovskite materials are widely used in solar energy applications and recently have been envisioned as excellent candidate for next-generation photodetector materials because of their high adsorption coefficient, tunable bandgap, small exciton binding energy, long carrier diffusion length, ambipolar charge transport, and high carrier mobility [12]. It has been demonstrated that graphene/perovskites, such as graphene/$CH_3NH_3PbI_3$ ($MAPbI_3$) hybrid, can achieve a responsivity of several hundreds of A/W at a response time shorter than 1 s [74, 75] (Fig. 21.10). The enhanced performance is mainly ascribed to the electron transfer from graphene to perovskite layer to fill its empty states in the valence band and hence reduce the photocarrier recombination. Furthermore, photodetectors based on vapor deposited ultra-flat $MAPbI_3$ films on graphene obtain an even higher responsivity of 1.73×10^7 A/W and specific detectivity of 2×10^{15} Jones [76]. In particular, when a thin layer of P3HT has been inserted between $MAPbI_{3-x}Cl_x$ perovskite and graphene as a hole-transport layer [77], the carrier diffusion length is significantly increased, resulting in more efficient transfer of photogenerated holes to graphene and electrons to perovskite layer. Remarkably, a record value of 4.3×10^9 A/W has been obtained for the P3HT-enhanced photodetectors.

21.5.5 Graphene/Other 2D Materials

Besides graphene, black phosphorus (BP) and transition metal dichalcogenides (TMDCs) are also popular 2D layered materials for optoelectronic applications [6]. BP is a direct bandgap semiconductor whose bandgap can tuned from 0.3 to 1.9 eV by reducing the number of layers [78]. It excels in photodetection due to the easy excitation by absorption of visible and NIR lights [79]. Its anisotropic crystal structure and hence anisotropic electrical and optical properties lead to promising polarization-dependent light detection. Similarly, TMDCs, such as MoS_2, $MoSe_2$, WS_2, and WSe_2, also show tunable bandgaps ranging from an indirect bandgap of ~1.1 eV in bulk crystal to a direct energy gap of ~1.9 eV in monolayer crystal [80, 81]. For example, TMDCs could be used to manufacture photodetectors with high on/off ratio, which is superior to zero-bandgap graphene. Recently, several III–VI group layered (transition metal monochalcogenide) materials have also been demonstrated as promising photoresponse materials, such as GaS, GaSe, and InSe [6]. They also exhibit good tunability in bandgaps through adjusting the layer number. In addition to 2D semiconducting materials, 2D insulating materials also play an important role in photodetection. For example, hexagonal boron nitride (h-BN) are usually used as appealing barrier layer to restrain the dark current, due to its good chemical stability and thermal conductivity [82].

Although a large variety of individual 2D materials have demonstrated promising photodetection applications, the more attractive property of 2D materials for photodetectors relies on their van der Waals interaction between neighboring layers without dangling bonds, which enables the integration of multiple 2D materials to form heterostructures and obtain fundamentally different properties [12]. In a common geometry, 2D layered semiconductors and graphene act as the light absorber and the electrodes, respectively, to form planar metal-semiconductor-metal phototransistors. Different from metal electrodes, the Schottky barrier between the graphene electrode and the 2D semiconductors can be tuned by adjusting the Fermi level of graphene, making it possible to obtain ideal Ohmic contact between the two 2D materials. Also, the photoresponse characteristics of the heterostructures can be adjusted by electrostatic gating or optical input control [12]. Up to now, heterostructures between TMDC, BP, and III–VI 2D semiconductors have all be developed for photodetectors, as introduced below.

Various high-performance photodetectors based on graphene/TMDC heterostructures have been demonstrated with the TMDC being MoS_2, $MoTe_2$, WS_2, WSe_2, and so on. Remarkably, a high responsivity of up to 10^{10} A/W has been achieved in phototransistors based on heterostructures between mechanically exfoliated graphene and MoS_2 [85]. The high responsivity relies on the local trapping of photogenerated holes in MoS_2 and the gate electric field-enhanced electron transfer to graphene. The trapped holes can even act as local gates to generate significant photogating effect on graphene through capacitive coupling. Meanwhile,

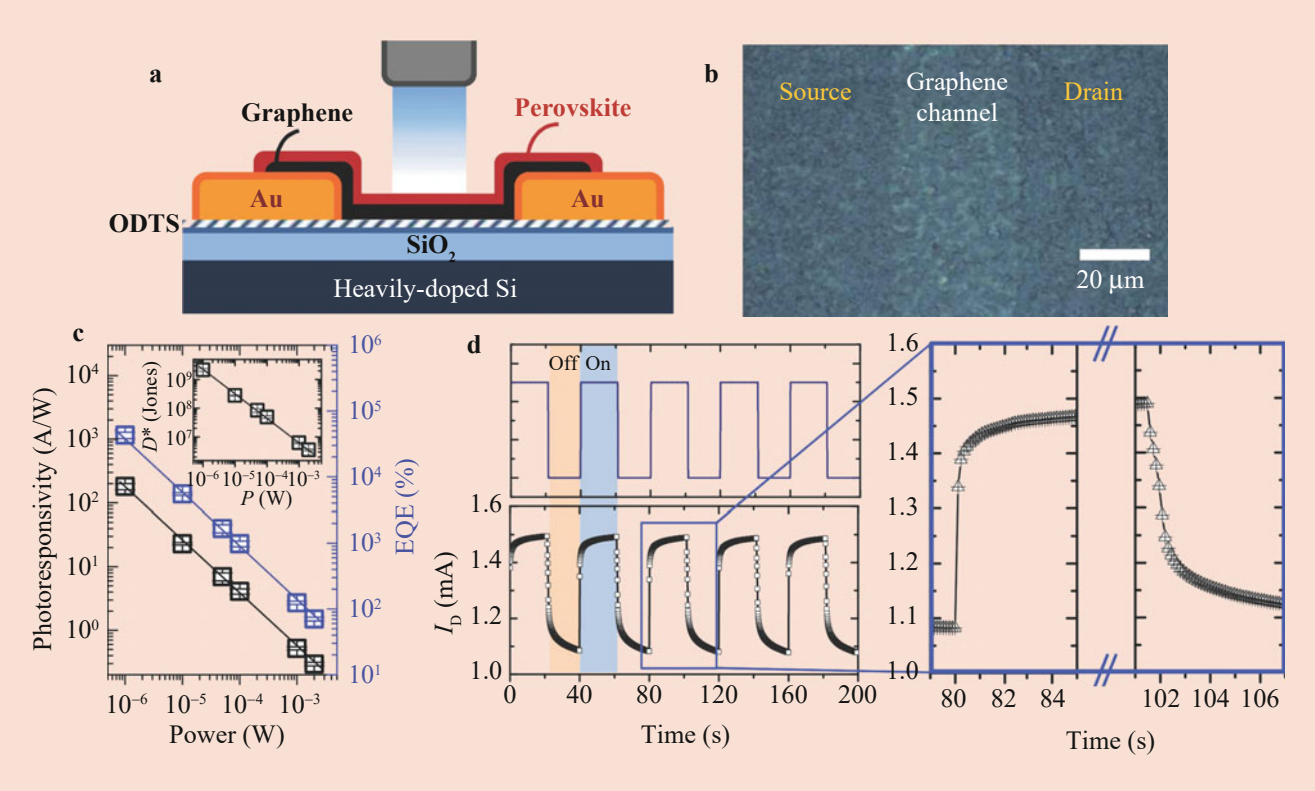

Fig. 21.10 Photodetectors based on graphene/perovskite heterostructures. (**a**) Schematic of the hybrid photodetector. (**b**) Optical micrograph of the $CH_3NH_3PbI_3$-graphene photodetector. (**c**) Responsivity, EQE, and specific detectivity (inset) under different illumination powers. (**d**) On-off switching characteristics of the photodetectors under alternative dark and light illuminations. (Adapted with permission from [74] Copyright (2014) John Wiley and Sons)

however, the trapped holes have long lifetime that evidently increase the response time of the photodetectors. In contrast, a graphene/WSe_2/graphene heterostructure [83] with a trilayer WSe_2 (2.2 nm thick) sandwiched between two graphene electrodes (Fig. 21.11a–c) exhibits fast response of around 5.5 ps and high internal quantum efficiency (70%). In another study, it is found that a graphene/WS_2/graphene heterostructure phototransistor shows abnormal dependence of the responsivity on incident light power [86]. The responsivity increases with the increasing optical power at a gate voltage of 0 V (off state), whereas it decreases at the gate voltage of 30 V (on state). The mechanism could be at on state; the photogating effect increases the Fermi level and reduces the contact resistance, so that the Fermi level of graphene is weakly influenced by illumination, thereby causing different power dependence of responsivity. Interestingly, a unique MoS_2/graphene/WSe_2 heterostructure-based photodetector (Fig. 21.11d–f) indicates the broadband response in the range from 400 to 2400 nm [84], with high responsivity and detectivity, respectively, of 10^4 A/W and 10^{15} Jones in the visible range, but decreasing to 0.1 A/W and 10^9 Jones at 2400 nm IR wavelength. The possible reason for the performance dependence on the incident light wavelengths is that short-wavelength light can be absorbed by all the three materials (WSe_2, graphene, and MoS_2) in the heterostructures, while long-wavelength light can only be absorbed by graphene which results in low photocurrents.

Recently, BP and III–VI 2D materials have also been integrated with graphene to fabricate wideband 2D heterostructure photodetectors. Highly efficient photodetectors operating at NIR wavelengths have been fabricated based on the graphene/BP heterostructures (Fig. 21.12) [87]. Thanks to the large photon absorption over a broadband wavelength range of the BP flakes, the graphene-BP heterostructure device exhibits a broadband photodetection from the visible to IR wavelengths and moreover shows a high responsivity up to ~3.3 × 10^3 A/W at 1550 nm, which is more than 3000 times higher than those of previously reported photodetectors operating at the same wavelength. All the devices with different BP thickness exhibit qualitatively similar behaviors, while thicker BP flakes give rise to higher photoresponse (Fig. 21.12d). The devices can be stable for at least 60 days when operating at ambient conditions (Fig. 21.12e). They also show a high photoconductive gain (1.13 × 10^9), an ultrafast charge transfer (41 fs, Fig. 21.12f), a polarization-

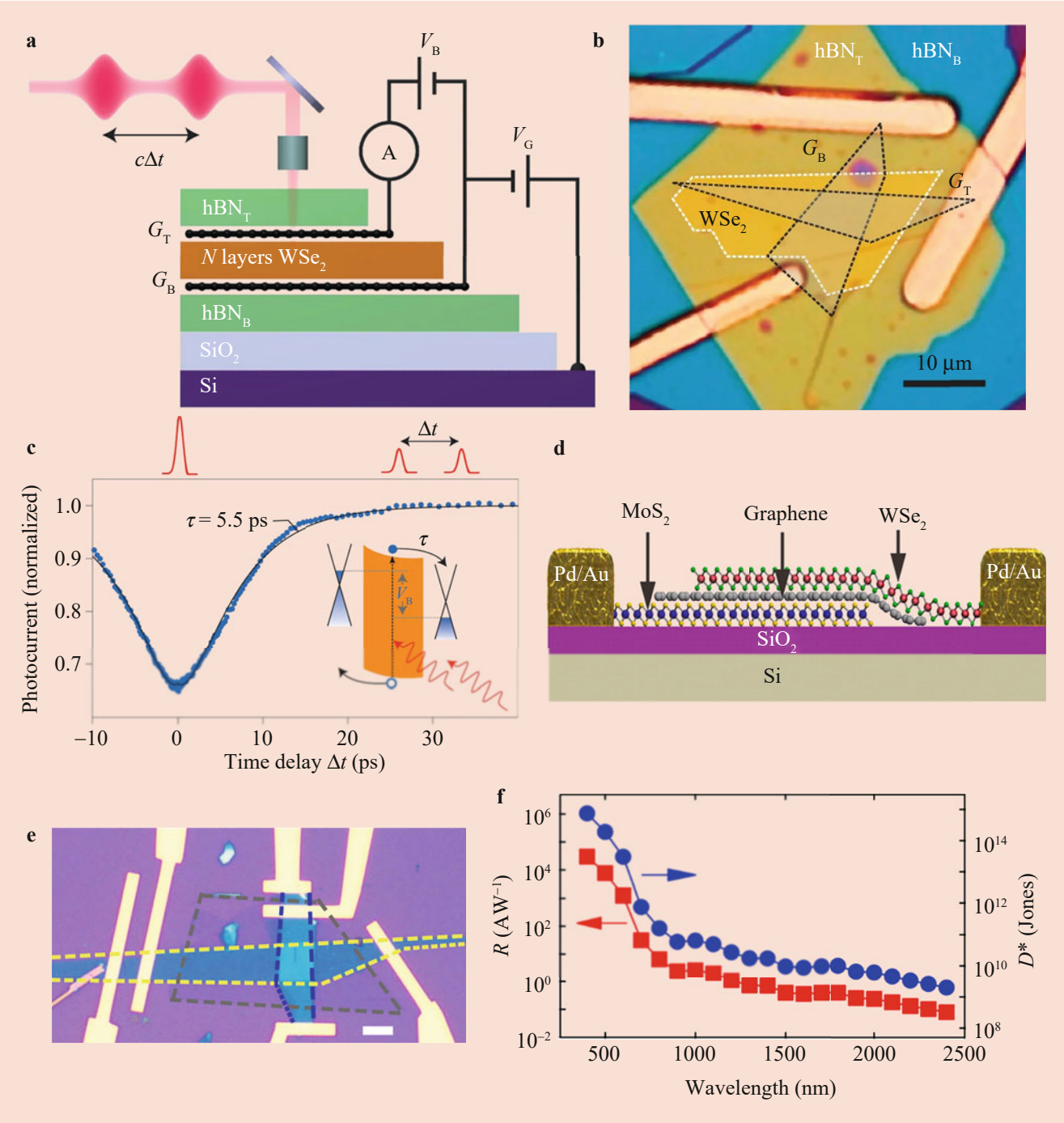

Fig. 21.11 Photodetectors based on graphene/TMDC heterostructures. (**a**) Schematic of a graphene/WSe_2/graphene heterostructure and the setup for detecting time-resolved photocurrent. Two ultrashort pulses, delayed by a controllable distance $c\Delta t$ (c is the speed of light), are focused on the device on a Si back gate to which a gate voltage (V_G) is applied between the top (G_T) and bottom (G_B) graphene layers to measure the photocurrent [83]. (**b**) Optical image of a heterostructure comprising a 2.2-nm-thick WSe_2 flake. The graphene and WSe_2 flakes are outlined and shaded for clarity. (**c**) The dependence of photocurrent on the time delay between two pulses Δt. (**d**) Schematic of cross section and (**e**) photograph of top view of a photodetector based on MoS_2/graphene/WSe_2 heterostructures [84]. (**f**) The dependence of responsivity and detectivity of the devices in (**d**) under different incident light wavelength. (Adapted with permission from [83] Copyright (2015) Springer Nature for **a**–**c**, and from [84] Copyright (2016) American Chemical Society for **d**–**f**)

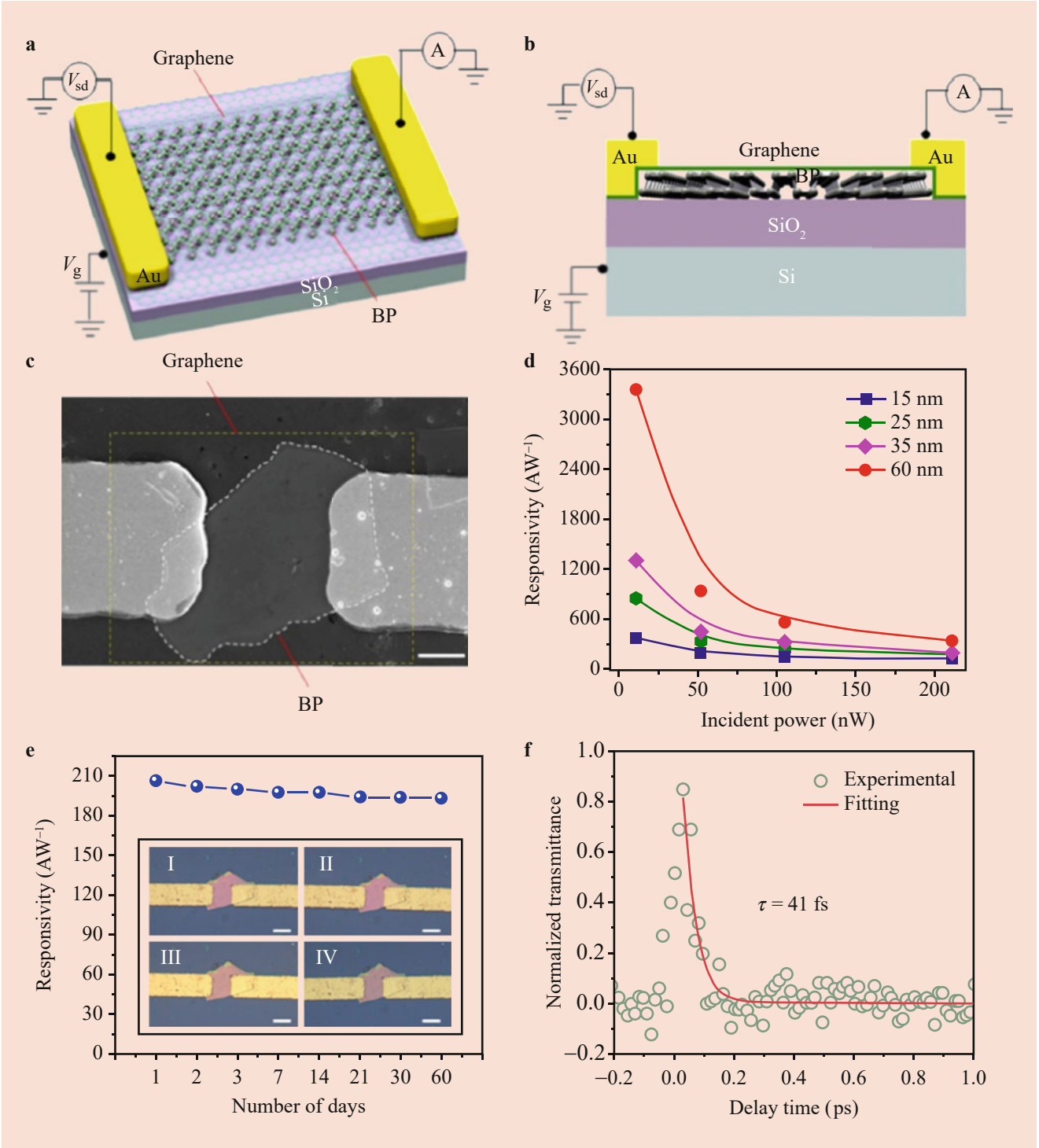

Fig. 21.12 A photodetector based on graphene/BP heterostructure. (**a**) 3D schematic and (**b**) schematic of cross-section view of the device. (**c**) SEM image of the graphene/BP heterostructured photodetector. Scale bar: 2 μm. (**d**) Responsivity as a function of incident power for different BP thickness. (**e**) Responsivity of a device under different exposure time. Inset: from I to IV, the exposure times are 1 day, 7 days, 30 days, and 60 days, respectively. Scale bars: 8 μm. (**f**) Measured transmitivity transients of graphene/BP heterostructure at 1550 nm with an average pump power of 800 μW. (Reprinted with permission from [87] Copyright (2017) American Chemical Society)

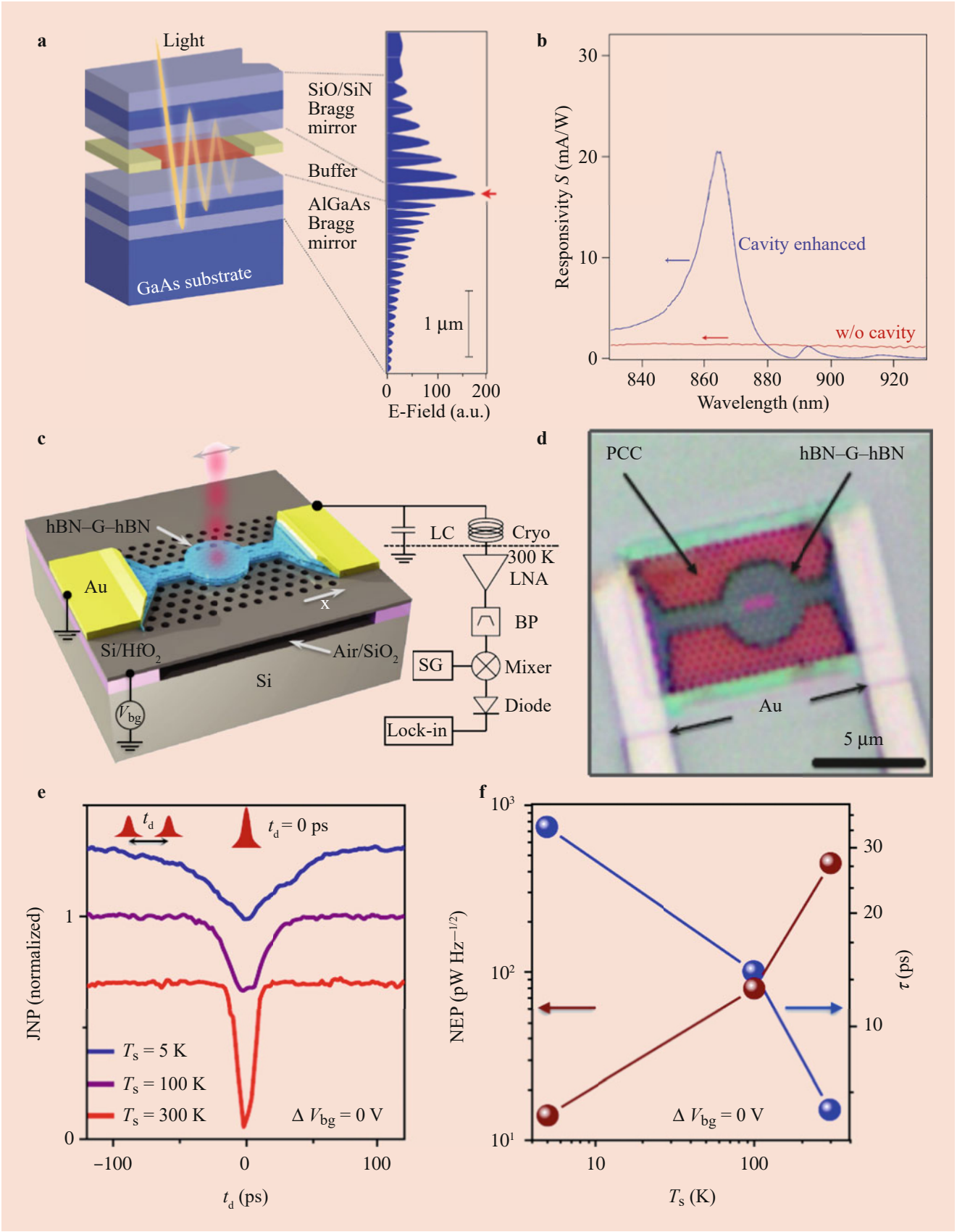

Fig. 21.13 (continued)

dependent photocurrent response, and a long-term stability at 1550 nm [87]. In another study, by using the broadband transparency of graphene and the favorable band lineup of graphene with InSe, wideband photodetectors with spectral response extending from NIR to visible spectrum have been fabricated based on planar graphene/n-InSe/graphene van der Waals heterostructures. The devices exhibit high responsivity of up to 10^5 A/W at wavelength of 633 nm and fast rise/fall times of 1/10 ms [88]. The high responsivity appears in the vertically stacked InSe and graphene layers with an optical window created by overlapping the two graphene electrodes, thus enabling sensitive photodetection.

21.6 Integrated Graphene Photodetectors

The low absorption of monolayer graphene (only ~ 2.3% of incident light) severely limits the overall responsivity of conventional graphene photodetectors to a typical value of a few mA/W. Highly desired are techniques that can effectively improve the optical absorption and responsivity. It has been discussed in Sect. 21.5 that integration of graphene photodetectors with light absorbers (such as quantum dots and perovskite) can improve the responsivity through the photogating effect. But typically these techniques result in lower operating speed [54, 74]. In this section, we discuss about the techniques of integrating graphene photodetectors with optical cavity and waveguides to improve the device performance.

21.6.1 Integration with Optical Cavity

It has been demonstrated as an effective way to significantly improve light absorption through embedding graphene into optical or photonic crystal cavities (PCC) [10]. Typically, optical cavities comprise arranged mirrors (either Bragg mirrors or metallic reflectors) [89, 91] with the gap equal to a quarter of the resonant wavelength so as to trap the electric field inside the cavities. When graphene integrates with an optical cavity, light may pass through it for several times which significantly increases the light absorption. Furchi et al. [89] integrated a metal/graphene/metal detector with a Bragg mirror-based microcavity (Fig. 21.13a, b) to reach a light absorption of 60% (about 26-fold enhanced) and a responsivity of 21 mA/W. However, it is worthy of mentioning that the sharp resonant peak of an optical cavity often reduces the operating bandwidth of photodetectors, because the Bragg mirror-induced optical confinement is only in the vertical direction [10]. In contrast, PCC permits very high-quality factor due to the three-dimensional optical confinement. Dmitri et al. [90] have demonstrated a proof-of-concept device (Fig. 21.13c, d) of a high-quality hBN/graphene/hBN heterostructure bolometer placed onto a suspended silicon PCC and integrated with a Johnson noise readout. The device operates at telecom wavelengths and exhibits an enhanced bolometric response at charge neutrality with a NEP about 10 pW $Hz^{-1/2}$ and a record fast thermal relaxation time <35 ps (Fig. 21.13e, f).

21.6.2 Integration with Waveguides

In addition, due to their very low losses and high optical mode confinement, silicon waveguides have enabled a large variety of new applications, including nano-optomechanics, biosensing, nonlinear optics, and very long-wavelength integrated photonics [96]. It has also allowed hybrid integration of new materials into the silicon system for extended functionality, for example, integrating organic materials to increase optical nonlinearities and bonding III–V materials to create on-chip light sources. Integration of graphene photodetectors with low-loss optical waveguides can also greatly enhance the light absorption. The waveguides confine and guide the evanescent mode of optical electric field which propagates parallel to graphene channels. Therefore, light interacts with graphene throughout its travel in the waveguide so as to maximize the optical absorption [10]. It has been demonstrated the light absorption of a graphene-integrated silicon waveguide based on a Mach-Zender interferometer [97] can be increased up to 50% and 90% in 15-μm- and 50-μm-long graphene samples, respectively. The responsivity is also increased to 0.05 A/W and 0.1 A/W for 24-μm- [98] and 50-μm [99]-long silicon waveguides, respectively. In particular, a high responsivity of 0.13 A/W is obtained (Fig. 21.14a) when a graphene/silicon heterostructure is naturally integrated with silicon waveguide on SOI substrate [92]. Also, a compact photodetector [95] is realized through embedding graphene *inside the slot layer* of high-*k* (Al_2O_3)

Fig. 21.13 Graphene-based photodetectors integrated with optical cavity. (**a**) (Left) Schematic drawing of a graphene microcavity photodetector, including a bottom Bragg mirror made from multiple periods weakly doped, alternating AlAs and $Al_{0.10}Ga_{0.90}As$ layers, a buffer layer of Si_3N_4 to maximize the electric field at the graphene sheet, the graphene layer (the graphene sheet is shown in red, and the metal contacts are in yellow), and a top Bragg mirror of SiO_2/Si_3N_4 layer. (Right) Electric field amplitude inside the cavity. (**b**) Comparison of responsivity of the bilayer graphene photodetectors with and without cavity [89]. (**c**) Schematic and (**d**) optical micrograph of a graphene bolometer on top of a suspended silicon photonic crystal cavity and a Johnson noise readout. (**e**) Normalized Johnson noise power probed with two laser pulses (delayed with time t_d) at different device temperature T_s and (**f**) NEP and thermal relaxation time (τ) of the graphene bolometer in (**c**, **d**). (Adapted with permission from [89] Copyright (2012) American Chemistry Society (https://pubs.acs.org/doi/10.1021/nl204512x, further permission should be directed to ACS) for **a**, **b** and from [90] Copyright (2018) Springer Nature for **c**–**f**)

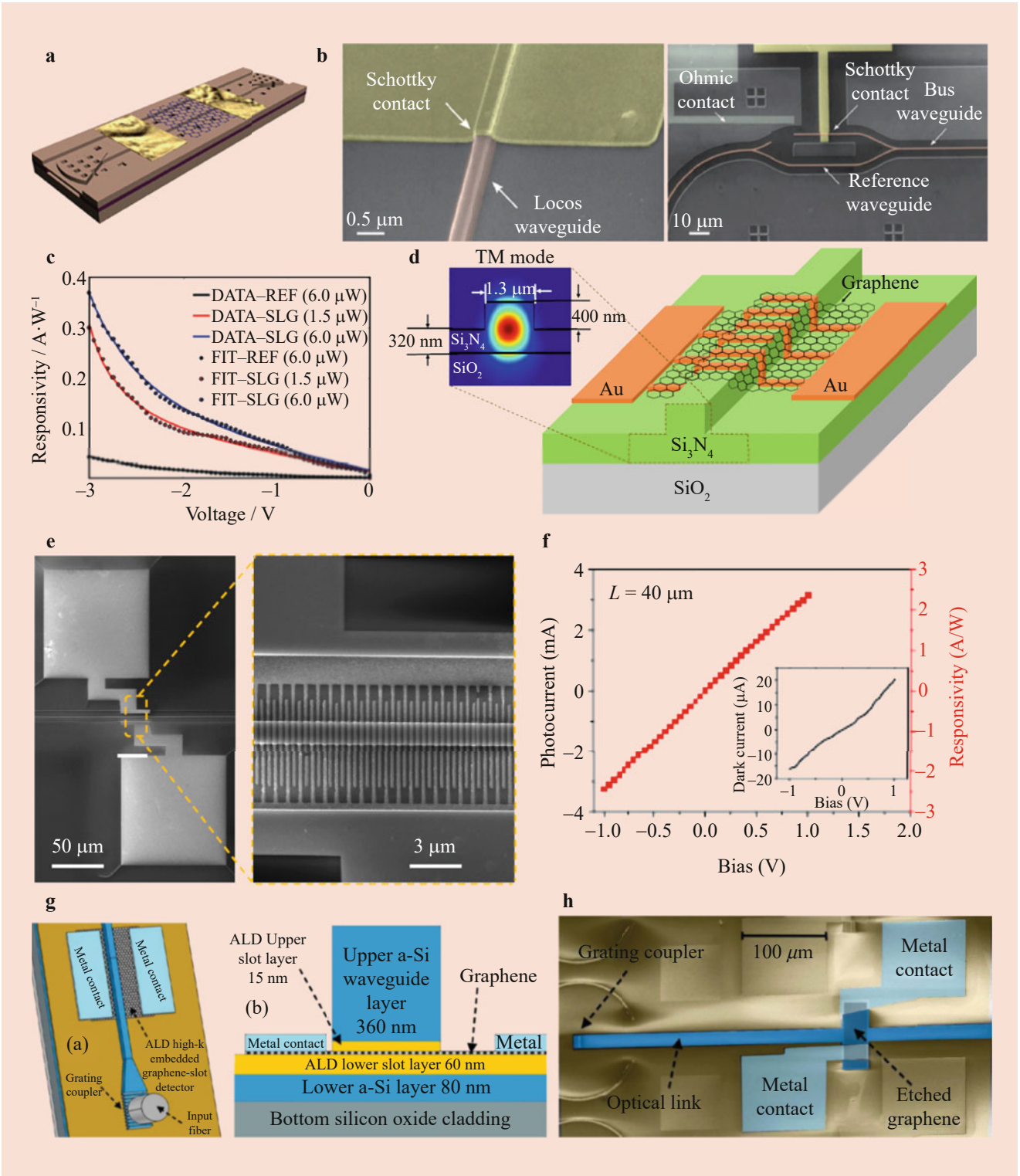

Fig. 21.14 Graphene photodetectors integrated with waveguides. (**a**) Schematic of graphene/silicon heterostructure waveguide photodetector on an SOI waveguide [92]. (**b**) SEM images of a graphene silicon Schottky photodetector: (left) graphene is coupled to a waveguide and (right) layout of the complete device [93]. (**c**) Responsivity of device in (**b**). (**d**) Schematic of a graphene-on-Si_3N_4 waveguide photodetector with transverse-magnetic (TM) mode distribution [94]. (**e**) SEM images of a fabricated photodetector before graphene transfer. (**f**) Photocurrent and responsivity as a function of bias with an input optical power of 1.314 mW to a photodetector with Si_3N_4 waveguide. Inset: dark current against bias. (**g**) Schematics of photodetectors with embedded graphene in the slot of Al_2O_3 waveguide (left, top view; right, cross section). (**h**) SEM image of the photodetector with integrated waveguide. (Adapted with permission from [92] Copyright (2013) Springer Nature for **a**, from [93] Copyright (2016) American Chemistry Society (https://pubs.acs.org/doi/10.1021/acs.nanolett.5b05216, further permission should be directed to ACS) for **b**, **c**, from [94] Copyright (2018) AIP Publishing for **d**–**f**, and from [95] Copyright (2014) IEEE Proceedings for **g**, **h**)

slot waveguides (Fig. 21.14). Due to the high mode concentration in the slot region, this structure leads to a high light-graphene interaction and hence a responsivity of 3.6 mA/W for a 40-μm-long graphene detector. Making use of the avalanche multiplication at high reverse biases of an integrated graphene/silicon Schottky photodetector (Fig. 21.14b, c), a high responsivity up to 0.37 A/W is achieved for 1.5 μm incident light [93]. A recent study [94] also demonstrated that graphene photodetectors integrated on silicon nitride waveguides (Fig. 21.14d–f) with interdigitated metal contacts (to reduce the channel spacing down to ~200 nm) exhibit a high responsivity of 2.36 A/W and bandwidth of 33 GHz at 1550 nm.

21.7 Graphene Photodetectors with Special Geometry or Architectures

Recently, it has been demonstrated that special geometry and architectures have potential to lead to new mechanism and functionalities of graphene-based photodetectors.

Despite the diversity of mechanisms in graphene-based photodetectors, such as PV and PTE effects, all of these photocurrents are prominent at high charge densities but are suppressed at the charge neutrality point (CNP). A recent research [100] has discovered a new photocurrent phenomenon in graphene that appears exclusively when the Fermi level is at the Dirac point and vanishes at high charge densities. For intrinsic graphene with special geometrical patterns, such as those in Fig. 21.15, the photocurrents emerge at free graphene edges (in area far away from the contacts) exclusively at the CNP where the Fermi level matches the Dirac point. At high charge densities where the Fermi level leaves away from the Dirac point, conventional photocurrents appear only near the graphene/metal contacts. The new mechanism originates in the asymmetry of electron-hole velocities in graphene [101]. Electrons and holes have an intrinsic velocity difference, and upon being excited by photons, they will diffuse at different speeds, separate, and produce a local electric field. Since the diffusion has no directional preference, the local electric fields are circularly symmetric around the excitation point and cancel each other out, resulting in zero total electric field in the electrical circuit. However, when light is shone on the edge of the graphene, the diffusion is no longer circularly symmetric, and this gives rise to a residual electric field to produce photocurrent in the circuit. Therefore, graphene with well-designed edges can serve as a photocurrent source [101]. As the CNP photocurrents are carried at the group velocity of unthermalized electrons, they should exhibit an ultrafast response time, possibly leading to ballistic photodetectors. Hence, the new mechanism is promising for ultrahigh-speed and ultra-broadband optoelectronics [100].

The attractive properties of graphene and 2D materials for photodetectors are not restricted to their unique electrical and optical properties, but also include their mechanical strength and flexibility and great compatibility with various substrates. For example, making use of heterostructure of single-layer graphene and MoS_2, Domenico et al. [103] developed flexible photodetectors on plastic substrates for visible wavelengths. The devices are gated by polymer electrolyte with external responsivity up to ~45.5 A/W (at least two orders of magnitude higher than that of conventional semiconductor membranes), photoconductive gain ~4 × 10^5, operation voltage <1 V, and optical transparency >82%. In addition, Wonho et al. [102] even integrate an array of graphene/-MoS_2 heterostructures on 3D substrates with complex and mechanically assembled 3D systems (Fig. 21.16). The 3D photodetectors exhibit a maximum responsivity of 38 A/W and rise and decay time of 290 ± 130 ms and 420 ± 210 ms, respectively. In particular, the overall photodetectors are optically transparent (~ 87% transmittance at 550 nm) which enables 3D systems to simultaneously detect the position, direction, intensity, and angular divergence properties of incident light. To realize the same functionality in 2D layouts, significantly more components are needed [102].

21.8 Conclusions and Outlook

The performance of representative graphene-based photodetectors is summarized in Table 21.1.

From Table 21.1, one may readily find that graphene-based photodetectors are being developed with intensive efforts from extensive research fields. So far, the focus is still on the performance improvement through integration with various materials, components, and systems. For many types of detectors, their performance has already surpassed the existing technologies, such as high responsivity (up to ~10^{10} A/W), wideband detection (UV-THz), and ultrafast response speed (down to ps). This can also be clearly seen in Fig. 21.17 which indicates a systematic comparison of performance metrics between standard and graphene (or 2D materials-)-based photodetector technologies [4]. Undoubtedly, graphene-based photodetectors have great potential to complement to or even replace the present silicon photodetectors in many applications. However, it should be mentioned that most techniques still make trade-off between different performance metrics. For example, heterostructures typically give rise to high responsivity, while the response speed is sacrificed. Integration with optical cavity increases the light absorption but significantly limits the operating bandwidth. So highly desired are comprehensive technologies that may integrate multiple complementary materials (especially new 2D materials) and components (especially optical cavity and waveguides)

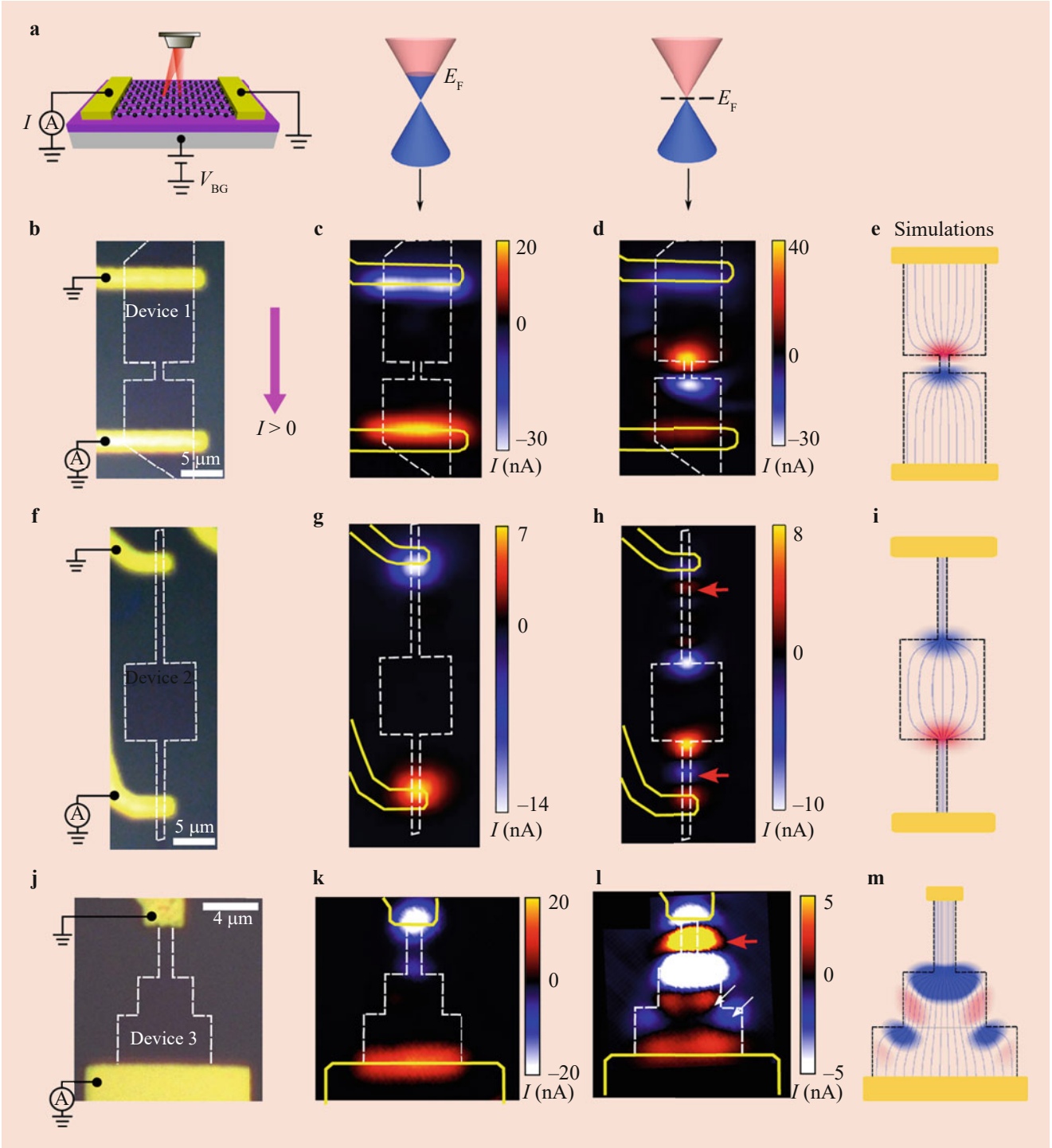

Fig. 21.15 Intrinsic long-range edge photocurrent in charge-neutral graphene with different geometries. (a) Schematic of a back-gated graphene device with scanning laser excitation. (**b–d**) Optical image (**b**) and scanning photocurrent images (**c**, **d**) of Device 1 with a narrower middle graphene channel. At high charge density (**c**), the photocurrent is mainly generated at the contact areas, whereas at the CNP (**d**) significant photocurrent occurs at the two ends of the middle graphene region. (**e**) Simulation of the photocurrent image for Device 1. (**f-i**) Similar figures to (**b–e**) for Device 2 with a wider middle graphene section. (**j–m**) Similar figures to (**b–e**) for Device 3 with three rectangular graphene regions with increasing widths. The white arrows in (**l**) indicate that the photocurrent is generated from the graphene edge. The red arrows in (**h**) and (**l**) denote the photocurrent along the straight edges. (Reproduced with permission from [100] Copyright (2018) Springer Nature)

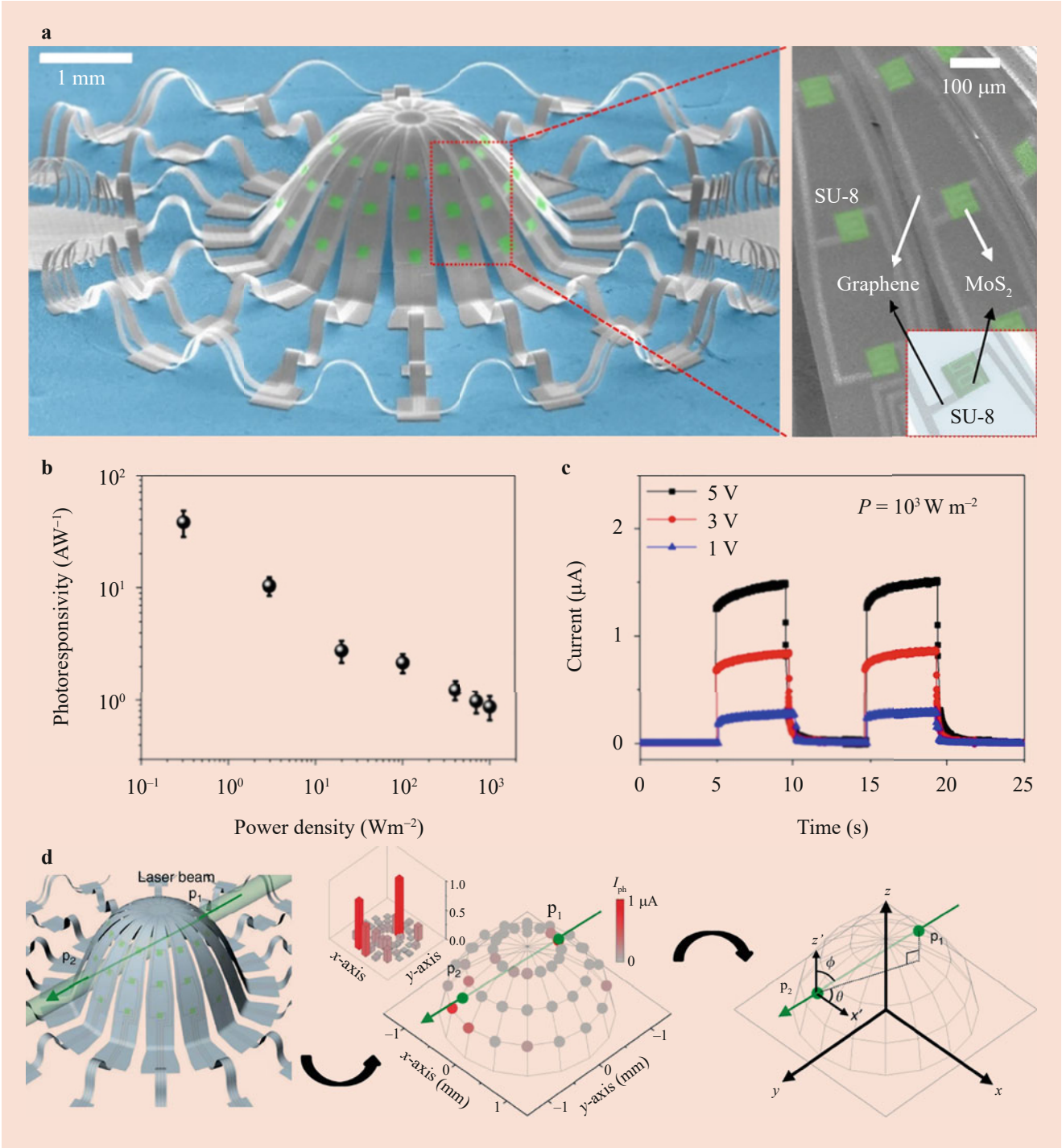

Fig. 21.16 Graphene/MoS_2 photodetectors on 3D hemispherical structure. (**a**) Colorized SEM image of photodetectors consisting of MoS_2 (green), graphene (light gray), and SU-8 (gray) on the hemisphere with 3D interconnects. (**b**) Responsivity of the photodetector at a bias voltage of 3 V for different laser power densities. (**c**) Time-resolved photoresponses of the devices under laser illumination at different power densities. (**d**) Operating principle of 3D photodetection: (left) penetration of the laser beam at two points of the 3D hemispherical surface, (middle) photocurrent distribution on the hemisphere surface in the scenario, and (right) principle of estimating the incident direction of the laser from the photocurrent map. (Adapted with permission from [102] Copyright (2018) Springer Nature under the terms of the Creative Commons CC BY 4.0 license)

Table 21.1 Performance of graphene-based photodetectors

Device structure	Mechanism	Responsivity R_{ph} (A W^{-1})	Noise equivalent power NEP (W $Hz^{-1/2}$)	Detectivity D^* (Jones)	Response time (s)	References
Metal/graphene/metal	Photovoltaic (PV)	6.1×10^{-3}				[9]
Dual-gated bilayer graphene	Bolometric	2×10^5 V W^{-1}	3.3×10^{-14}		$\sim 1 \times 10^{-10}$	[40]
Antenna on SLG with back gate	Plasmon induced doping	1×10^{-2}			$\sim 2 \times 10^{-6}$	[48]
Graphene-PbS quantum dots hybrid with back gate	Photogating	$\sim 10^7$	$\sim 10^{-17}$ W (at 0.1 Ω $Hz^{-1/2}$)	7×10^{13}	$\sim 10^{-6}$	[54]
Graphene/SiO_2/Si	PV, heterostructure	0.3				[59]
Graphene/SiO_2/Si (interdigitated)	PV, heterostructure	0.6				[60]
Ag nanoparticle/-graphene/porous Si	Plasmon, heterostructure	0.3			$\sim 3 \times 10^{-6}$	[65]
Au nanoparticle/-graphene/Si nanowire	Plasmon, heterostructure	1.5		2.5×10^{14}	$\sim 7 \times 10^{-5}$	[66]
Graphene/GaN NWs	PV, heterostructure	25				[67]
Graphene/pentacene	Hybrid	700		10^{13}		[72]
Graphene/C8-BTBT	Hybrid	1.6×10^4			2.5×10^{-2}	[73]
Graphene/$MAPbI_3$	Hybrid	1.7×10^7		2×10^{15}	0.9	[76]
Graphene/P3HT/$MAPbI_{3-x}Cl_x$	Hybrid	4.3×10^9			10	[77]
Graphene/WSe2/graphene	Heterostructure	2×10^{-2}	5×10^{-12}		5.5×10^{-12}	[83]
Graphene/MoS_2	Heterostructure	1×10^{10} at 130 K;5×10^8 at room temperature				[85]
MoS_2/graphene/WSe_2	Heterostructure	10^4		10^{15}	5×10^{-5}	[84]
Graphene/BP	Heterostructure	3.3×10^3			5×10^{-3}	[87]
Graphene/n-InSe/graphene	Heterostructure	10^5			10^{-3}	[88]
Microcavity-integrated graphene	Cavity-enhanced	2.1×10^{-2}				[89]
hBN/graphene/hBN with silicon PCC	Cavity-enhanced		10^{-11}		3.5×10^{-11}	[90]
Graphene/Si with Si waveguide	Heterostructure, waveguide-enhanced	0.13				[92]
Graphene/Si with Al_2O_3 waveguide	Heterostructure, waveguide-enhanced	3.6×10^{-3}				[95]
Graphene/Si with Si_3N_4 waveguide	Heterostructure, waveguide-enhanced	2.36	3.3×10^{-12}		1.2×10^{-12}	[94]
Pristine graphene with special geometry	Geometry-induced	1×10^{-3}			2.5×10^{-13}	[100]
Graphene/MoS_2 on 3D substrates	Heterostructure	38			0.3	[102]

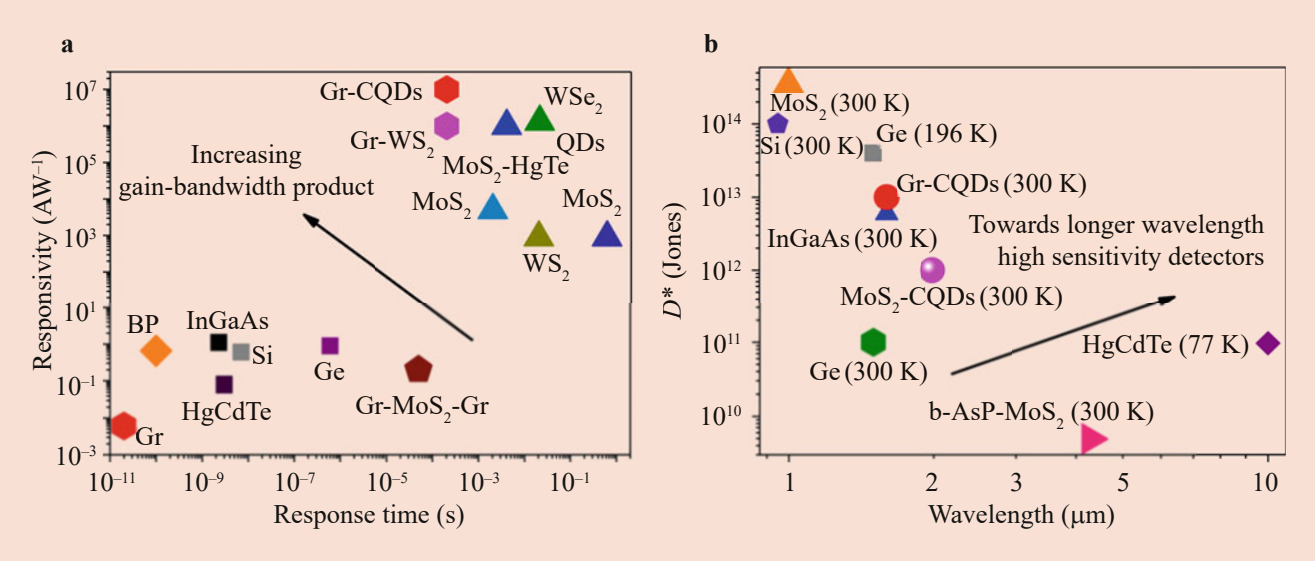

Fig. 21.17 Overview of performance metrics of standard and 2D-based photodetector technologies. (**a**) Responsivity against time response for various photodetector technologies. The top left region corresponds to high-gain bandwidth product detectors and should be the ultimate performance target of future photodetectors. (**b**) Plot of the specific detectivity D^* against absorption onset (bandgap) for various photodetector technologies. "Gr" means graphene. (Reproduced with permission from [4] Copyright (2018) Springer Nature under the terms of the Creative Commons CC BY 4.0 license)

with graphene to achieve thorough improvement of various performance metrics. Moreover, the exploration of new mechanisms, such as the geometry-dependent photoresponse in graphene [100], may offer opportunities to provide innovative solutions for groundbreaking performance to essentially eliminate the present dilemma in making trade-off among different performance metrics.

Besides the competitive photodetection performance, graphene-based photodetectors excel in compatible form factor with the standard silicon technology and ideal adaptability to a large variety of substrates, either rigid or flexible, single crystalline or amorphous, and planar or 3D curved. This greatly simplifies the integration and offers opportunities to develop multifunctional photodetectors to enable engineering unique system-level function through simple integration of devices on desired substrates. A good example is shown in [102]. Therefore, one may expect more advanced photodetecting systems based on graphene photodetectors can be developed in the near future to provide both high performance and multifunctionalities.

Finally, it is worthy of emphasizing that the most attractive points of graphene and other 2D materials for photodetector applications do rely not only on their outstanding photonic performance but also on their unique combination of many other properties. It is important to make use of the latter to develop in the future advanced photodetectors that integrate multiple functionalities and merits. For example, most 2D materials are compatible with liquid solution processes, which offer opportunities to develop solution-processed or solution-printed photodetectors based on 2D materials [3, 104] for both performance- and cost-competitive technology [4]. On the other hand, distinguishingly different sensors can be produced even when graphene is placed in the same device structure. For instance, a suspended graphene with simply contacted source and drain contacts can be both a good photodetector with increased responsivity [27] and an excellent pressure sensor with orders of magnitudes higher sensitivity than conventional pressure sensors [105]. Consequently, it is becoming a new trend to develop multifunctional graphene sensors which after integrating with decoupling techniques can detect both light illuminance and other environmental signs, so as to provide a compact solution to comprehensive systems (e.g., environmental monitoring, energy management, health care, feedback control of machines) where various types of sensors are normally needed [72, 106]. A final observation is that most of the above detector types, how promising they may all be, depend on reliable, reproducible, and cost-effective fabrication technologies which, at the moment, still are to be shown for large-scale production.

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Terahertz Electronic Devices

22

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Contents

22.1 Introduction 808

22.2 Gunn Diodes 810
22.2.1 Transit-Time Mode Gunn Oscillations 810
22.2.2 Materials for Gunn Diodes 811
22.2.3 Realisations of Gunn Oscillators 811
22.2.4 Perspectives 814

22.3 Schottky Diodes 814
22.3.1 Terahertz Schottky Junction 815
22.3.2 Parasitics of Terahertz Schottky Planar Diode 816
22.3.3 Terahertz Schottky Multipliers and Mixers 817
22.3.4 Driving Application of THz Schottky Diodes 819
22.3.5 Perspectives 820

22.4 Resonant Tunnelling Diodes 820
22.4.1 Resonant Tunnelling 820
22.4.2 RTD Oscillators 821
22.4.3 Frequency Limitations of RTDs 822
22.4.4 Applications of RTDs 823
22.4.5 Perspectives 823

22.5 Field-Effect Transistors 823
22.5.1 Frequency Limitations of FETs 824
22.5.2 FETs as THz Detector 825
22.5.3 FETs as THz Emitters 826
22.5.4 Perspectives 826

22.6 Heterojunction Bipolar Transistors 826
22.6.1 Physics of the Heterojunction Bipolar Transistor 827
22.6.2 Different Technologies of Heterojunction Bipolar Transistors 830
22.6.3 HBT-Based Circuits 834
22.6.4 Perspectives 835

22.7 Complementary Metal Oxide Semiconductor Transistors 836
22.7.1 Emitters 836
22.7.2 Detectors 837
22.7.3 Perspectives 838

22.8 Ballistic Rectifiers 838
22.8.1 Ballistic Formalism 839
22.8.2 BR Electrical Characteristics 840
22.8.3 THz BR Detection 841
22.8.4 Perspectives 842

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22.9 Conclusions 842
References 842

Abstract

The frequency band of the electromagnetic spectrum between microwaves and infrared is nowadays defined as the Terahertz band (1 THz corresponds to 10^{12} Hz). The development of specific applications for this area requires the use of devices able to operate (for instance, as emitters, detectors, amplifiers, etc.) in this domain of extremely high frequencies. For this purpose, it is necessary to cleverly combine favourable materials and charge transport properties with specific physical mechanisms and appropriate device topologies in order to reach electrical operation in conditions that, with respect to standard electronics, can be considered as extreme. Alternative strategies (not treated in this chapter) involve either the use of optical devices or a combination of electrical and optical systems. Here, we present an overview of the main electronic devices used for applications in the Terahertz frequency domain subdivided into two-terminal devices (such as Gunn, Schottky and resonant-tunnelling diodes) and three-terminal devices (such as field-effect, heterojunction bipolar and complementary metal oxide semiconductor transistors). A section devoted to non-conventional devices exploiting ballistic transport concludes the survey.

Keywords

Terahertz (THz) · Gunn diode · Schottky-barrier diode (SBD) · Resonant-tunnelling diode (RTD) · Field-effect transistor (FET) · Heterojunction bipolar transistor (HBT) · Complementary metal oxide semiconductor transistor (CMOS) · Ballistic rectifier (BR)

22.1 Introduction

When analysing the electromagnetic spectrum, the adjacent frequency band between microwaves and infrared is nowadays described as Terahertz (THz) band where 1 THz corresponds to 10^{12} Hz. Since the transitions between frequency bands are smooth, the low- and high-frequency limits of the THz band are not precisely defined. However, one commonly accepted determination considers that this band extends from 0.1 THz (i.e. 100 GHz) to 10 THz. It is also useful to convert these frequency limits into wavelengths using the relation

$$\lambda = c/f \tag{22.1}$$

where $c = 299,792,458$ m/s is the light speed in vacuum and f the frequency, or into wavenumbers ν using the relation

$$\nu = 1/\lambda. \tag{22.2}$$

The energy E can be derived from

$$E = hf, \tag{22.3}$$

where $h = 6.63 \times 10^{-34}$ Js $= 4.1 \times 10^{-15}$ eV s is the Planck's constant. The energy can be also converted into temperature T as

$$T = E/k_B, \tag{22.4}$$

where $k_B = 1.38 \times 10^{-23}$ J/K is the Boltzmann's constant. The THz band in terms of these different physical quantities is indicated in Fig. 22.1 by the coloured region.

To better understand the physical properties of the THz waves, it is useful to remember that a frequency of 1 THz corresponds to a wavelength in vacuum $\lambda = 0.3$ mm (submillimetre waves), to a wavenumber $\nu = 33.3$ cm^{-1} to an energy $E = 4.14$ meV and to a temperature $T = 48$ K. The characteristic photon energy of the THz radiation is much smaller than the band gap energy of common semiconductors as well as smaller than the ionisation energy of most atoms and molecules. For this reason it can be considered a non-ionising radiation.

The region of the spectrum between 20 μm and the millimetre region has been indicated for a long time as the "far-

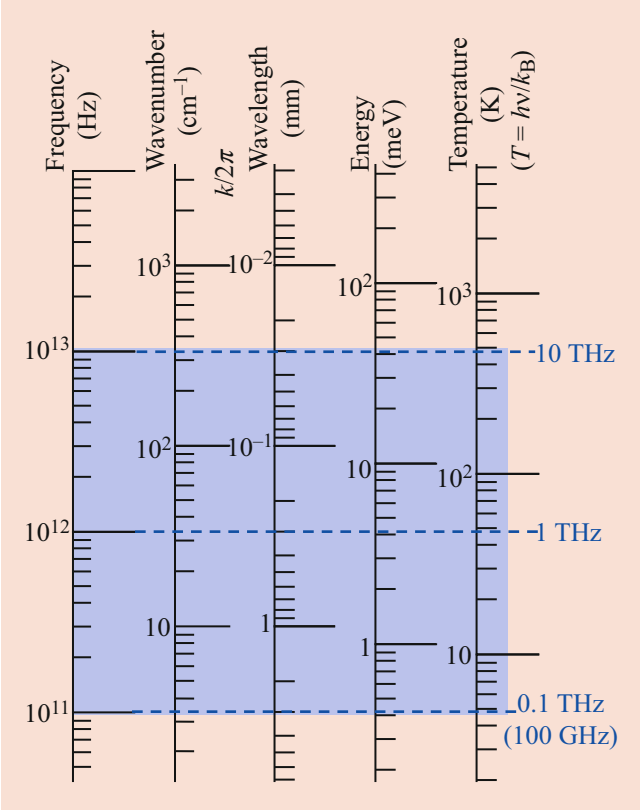

Fig. 22.1 Terahertz portion of the electromagnetic spectrum in terms of frequency, wavenumber, wavelength, energy and temperature

infrared" (FIR) region. Later it was proposed to indicate this portion as the "submillimetre", even if a cutoff at 1 mm was not entirely satisfying. In 1978, it was suggested to use an accurate, but rather long, title "short millimetre and submillimetre-wavelength range" (SMSMR), but this name did not become very popular. More recently the term Terahertz became to be used especially in association with the experimental technique called THz time-domain spectroscopy (TDS) [1, 2] but is now accepted and used in most of publications and specialised journals. A comprehensive historical description of the progressive development of THz science can be found in Ref. [3].

For many years the lack of efficient, reliable, low-cost and room-temperature emitters and detectors has limited the practical applications of THz devices and systems. However there has been recently significant progress in the development of continuous-wave and pulsed emitters that, coupled to lab-developed or commercially available detectors, has opened the way to the use of THz devices and systems in several domains. Nowadays the scientific literature on this domain is very large, and many review articles and books devoted to this topics can be found [4–14].

Historically it was in the 1970s that scientists realised that the THz portion of the electromagnetic spectrum offers unique opportunities in astronomical research [15, 16]. However the presence of vibrational and rotational levels of water vapour represents a major problem for research in this spectral region due to the very high absorption of the Earth's atmosphere [17]. As a consequence THz astronomy has been limited to research in the upper atmosphere, to high-altitude observatories and balloon flights.

In parallel to spatial telecommunications the need for larger bandwidths in standard telecommunications has become one of the strongest driving forces for THz applications. This is due, on one hand, to the need of cramming as many telecommunication channels as possible into single high-frequency carriers and, on the other hand, to the need of speeding up multimedia services and broadband interactive communications. Up to now, this demand has been satisfied by means of advanced modulation schemes and signal-processing technologies at microwave frequencies. However, it is now evident that only an increase of the carrier frequencies will provide the spectral resources needed to satisfy this growing need of ultrafast wireless communications. The huge bandwidth associated with the THz band (most of which has not been allocated for specific uses yet) represents a very promising opportunity for increasing the data rates further beyond 10 Gb/s. Even if THz communications has not entered the market yet and is in its early stage of development, many publications have clearly shown its potential in this field [18–25].

In the last decades another emerging application is that of biophysical and biomedical imaging due to the ability of THz radiation to penetrate deep into many organic materials without causing any damage associated with ionising radiation such as X-rays and also due to the possibility to simultaneously acquire both image and spectral information. For the above reasons it can be used for spectroscopic identification of biological signals, 2D and 3D imaging (including cancer detection [26]), pattern formation and recognition and THz tomography [27, 28]. Additionally, to enhance the efficiency of imaging systems, THz absorbers can be introduced into detectors. Due to the lack of naturally occurring dielectrics, artificially engineered resonant materials called metamaterials can be used [29]. Biological applications are also based on the specific spectroscopic fingerprints of biological matter (DNA, RNA, proteins, lipids, etc.) in the THz frequency domain involving vibrations of a substantial fraction of the atoms forming the molecule and motion associated with intermolecular hydrogen bond vibrations. These fingerprints provide information on the conformational state of the molecule but also on the effects of its environment such as the intensive absorption lines of water and other surrounding molecules [27, 30]. The bound water which influences the biological function represents also a strong absorbing medium for THz waves.

Besides biological matter, many other molecules have rotational and vibrational transitions in the THz range giving access to the spectroscopic analysis of a large variety of materials in security as well as various other areas such as air pollution, climate research, industrial process control, agriculture, food industry, workplace safety and many others [31–34]. Since most plastics, textiles and paper exhibit small absorption of THz waves, it becomes possible to detect chemical, biological, radiological and nuclear defence (the so-called CBRN) agents, explosives or illegal drugs [35]. While passive detection systems operate at frequencies where the background emissivity and reflectivity are rather different from those of the object of interest so that image contrast can be improved, active systems eliminate the background and can better detect and identify the objects at the cost of an increase in system complexity.

It is also worthwhile to mention the growing field of light-matter interaction which concentrates on physical phenomena at very high THz intensities. These intensities can be generated by optically pumped molecular lasers, free-electron lasers and femtosecond lasers. The physical phenomena in this domain include tunnelling processes in high-frequency fields, nonlinear absorption of radiation, nonlinear optics in the classical sense, hot electron dynamics, Bloch oscillations, ponderomotive action of the radiation field on a free electron gas, photoelectric and optoelectronic effects, and THz spin-dependent phenomena [36].

In the following sections we will systematically describe the basic principles and the main characteristics of the most used electronic devices forming the building blocks for the

design and development of THz detectors and emitters: first two-terminal devices (Gunn diodes, Schottky diodes, resonant-tunnelling diodes), then three-terminal devices (field-effect transistors, bipolar transistors, metal oxide semiconductor transistors) and finally ballistic devices. Other extensive reviews can be found elsewhere [37, 38].

We emphasise that the present chapter is intentionally restricted to an overview of electronic devices: the reader should be aware that there exists a whole domain of science and technology devoted to THz detection and emission using optical devices (such as quantum-cascade lasers or p-Ge lasers) and systems [3, 9, 39, 40].

22.2 Gunn Diodes

Gunn diodes are two-terminal semiconductor devices exhibiting negative differential conductance (NDC) at high electric fields that can be used to build free-running oscillators. Gunn oscillators have been found in many applications such as instrumentation, RADAR, imaging systems, weapons and communication systems. State-of-the-art Gunn oscillators operate at more than 300 GHz.

Gunn diodes, also called transferred electron devices (TEDs), were first demonstrated oscillating at 4.5 GHz on a 25 μm n-doped GaAs slab by J. B. Gunn in 1963 [41]. One year later, Kromer linked Gunn's experimental results with Ridley and Hilsum's theoretical studies [42–44] and concluded that the oscillations observed by Gunn resulted from the so-called transferred electron mechanism. The transferred electron mechanism appears in some semiconductor materials such as GaAs and InP that have lower Γ valley and higher L and/or X valleys (also called satellite valleys) in their conduction bands, as shown in Fig. 22.2a [45]. Under low electric fields (Ohmic regime), majority electrons stay in the Γ valley and travel at a speed proportional to the electric field. However, as the electric field increases and exceeds a critical value E_{th} (also called threshold electric field), that is approximately 3.2 kV/cm for GaAs, some electrons get "hotter" and start transferring to the higher L valley where electrons become heavier and slower because of the greater effective mass. Thus, the average speed of electrons decreases as the electric field is increased. This phenomenon is reflected in the current-voltage (electric field) characteristics (Fig. 22.2b) that shows negative differential conductance (NDC), i.e. a negative slope, above the threshold electric field.

Using NDC, one can apply Kurokawa's methods to design oscillators [46]. In fact, Gunn diodes may operate in different modes, and each mode has different limits on the oscillation frequencies and DC-RF conversion efficiencies. We will briefly describe the mechanism of the wide-used fundamental transit-time mode of oscillation in the next section. Information on other modes of oscillation can be found elsewhere [45, 47, 48].

22.2.1 Transit-Time Mode Gunn Oscillations

We assume that a piece of n-doped bulk GaAs sample has a length L and a doping level N (Fig. 22.3a). When an external bias V is applied to the sample between the anode and cathode, an electric field E is induced within the sample. The anode and the cathode are Ohmic and typically have a very high doping level N_0 ($N \ll N_0$) as shown in Fig. 22.3f. The electric field E_0 and drift velocity v_0 are at their lowest in the Ohmic contact regions (Fig. 22.3c, i). Ignoring the potential drop in the Ohmic contact regions, the electric field within the active region is $E{=}V/L$. For $E{=}E_1{<}E_{th}$ (Fig. 22.3b, c), the electron drift velocity v_1 (Fig. 22.3i) is proportional to the electric field E_1. If the applied electric field is greater than the threshold field, e.g. $E = E_2 > E_{th}$ (Fig. 22.3b, d), a small fluctuation of the electron concentration ΔN (Fig. 22.3g) can occur, typically arising from a nucleation event such as non-uniform doping or intrinsic noise. The result is a localized increase of the electric field, ΔE, or an electric field domain (Fig. 22.3d). As can be seen in Fig. 22.3b, the increase in electric field leads to a reduction in drift velocity of Δv as shown in Fig. 22.3j. The total current through the sample drops as well. At the same time, the electric field outside the domain drops because the total applied voltage between the anode and cathode is fixed.

If the applied electric field remains unchanged at the leading edge of the domain, electrons within the domain travel more slowly than the electrons ahead and outside of the domain. The faster electrons are accelerated at a lower electric field; thus the depletion region associated with the domain widens (Fig. 22.3h). On the other hand, at the trailing edge of the domain, electrons that are behind and outside the domain travel faster than the electrons within the domain; therefore more electrons accumulate behind the domain (Fig. 22.3h). As a consequence, the high field domain keeps growing while moving towards the anode and the space charge dipole also keeps developing. Meanwhile, both the electric field outside the domain and the electron drift velocity within domain keep reducing (Fig. 22.3k).

After a short while, when the domain velocity is equal to the electron drift velocity outside the domain, then the domain stops growing but travels to the anode at a constant speed, v_{domain}, until it disappears at the anode where the electric field is minimal. Meanwhile, the electric field within the sample is restored to its original magnitude, E_2, and a new domain starts nucleating near the cathode end of the sample, so that the process repeats. This periodic cycle of domain formation, transport and disappearance leads to the coherent current oscillation that was observed by Gunn.

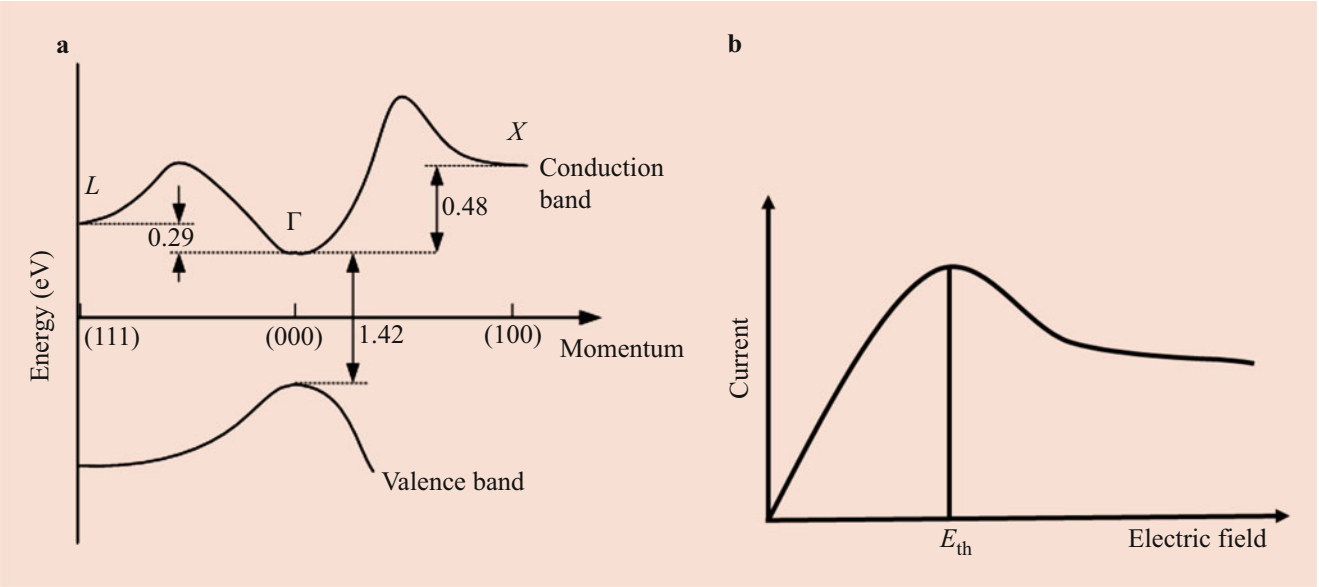

Fig. 22.2 (**a**) Simplified energy band structure of GaAs showing the band gap and the energy separations between the different valleys and (**b**) current versus electric field characteristics of the bulk material showing the threshold field E_{th} above which negative differential conductance appears

The oscillation frequency is approximately determined by the transit-time of the domain or the ratio of the domain velocity to the distance, L, that the domain travels. It is given by

$$f = \frac{v_{\text{domain}}}{L} \tag{22.5}$$

where the average domain velocity is equal to the average electron drift velocity v_{ave} which can be approximated using a numerical method as follows

$$v_{\text{ave}} = \frac{\mu_0 E + v_s (E/E_{\text{th}})^4}{1 + (E/E_{\text{th}})^4} \tag{22.6}$$

where μ_0 is the electron mobility at low electric field and v_s is the electron saturation velocity. To achieve higher oscillation frequency, one can either increase domain velocity by employing materials with high average drift velocity or reducing domain travel distance using advanced fabrication technologies.

22.2.2 Materials for Gunn Diodes

The general requirements of semiconductor materials for Gunn diodes are the following ones [45]:

- the band gap ΔE_g must be greater than the intervalley band difference ΔE between the minimum of the central valley and the minimum of higher satellite valleys so that avalanche breakdown will not occur before the onset of NDC;
- the intervalley band discontinuity ΔE must be several times greater than the thermal energy kT (approximately 0.027 eV at room temperature) so that the electron intervalley transfer is not due to the heating effect;
- the electron effective mass in the higher satellite valley must be larger than that in the central valley so that the electron mobility in the satellite valley is lower than that in the central valley.

The most commonly exploited materials for Gunn devices are n-GaAs and n-InP which were initially reported by Gunn. Since then, many other semiconductor materials have also been explored. These include n-Ge, n-CdTe, n-InSb, GaSb, ternary compounds $GaAs_xP_{1-x}$ ($x < 0.5$), $In_xGa_{1-x}Sb$, $In_xGa_{1-x}As$ and even the quaternary compound $Ga_{0.13}In_{0.87}Ga_{0.37}P_{0.63}$ [45]. However, those materials have yet to find commercial applications owing to poor material quality, high cost or difficulty of fabrication. Recently, there has been an increasing interest on GaN because of its promising thermal and power handling capabilities. Several reports based on numerical simulations show GaN has great potential in terms of oscillation frequency and radio-frequency power. However, experimental results are not yet available due to the poor quality of materials in terms of crystal defects, impurities, dislocations, etc. [49–51].

22.2.3 Realisations of Gunn Oscillators

Conventionally, Gunn diodes are made in a vertical format, as shown in Fig. 22.4a, which means the direction of current

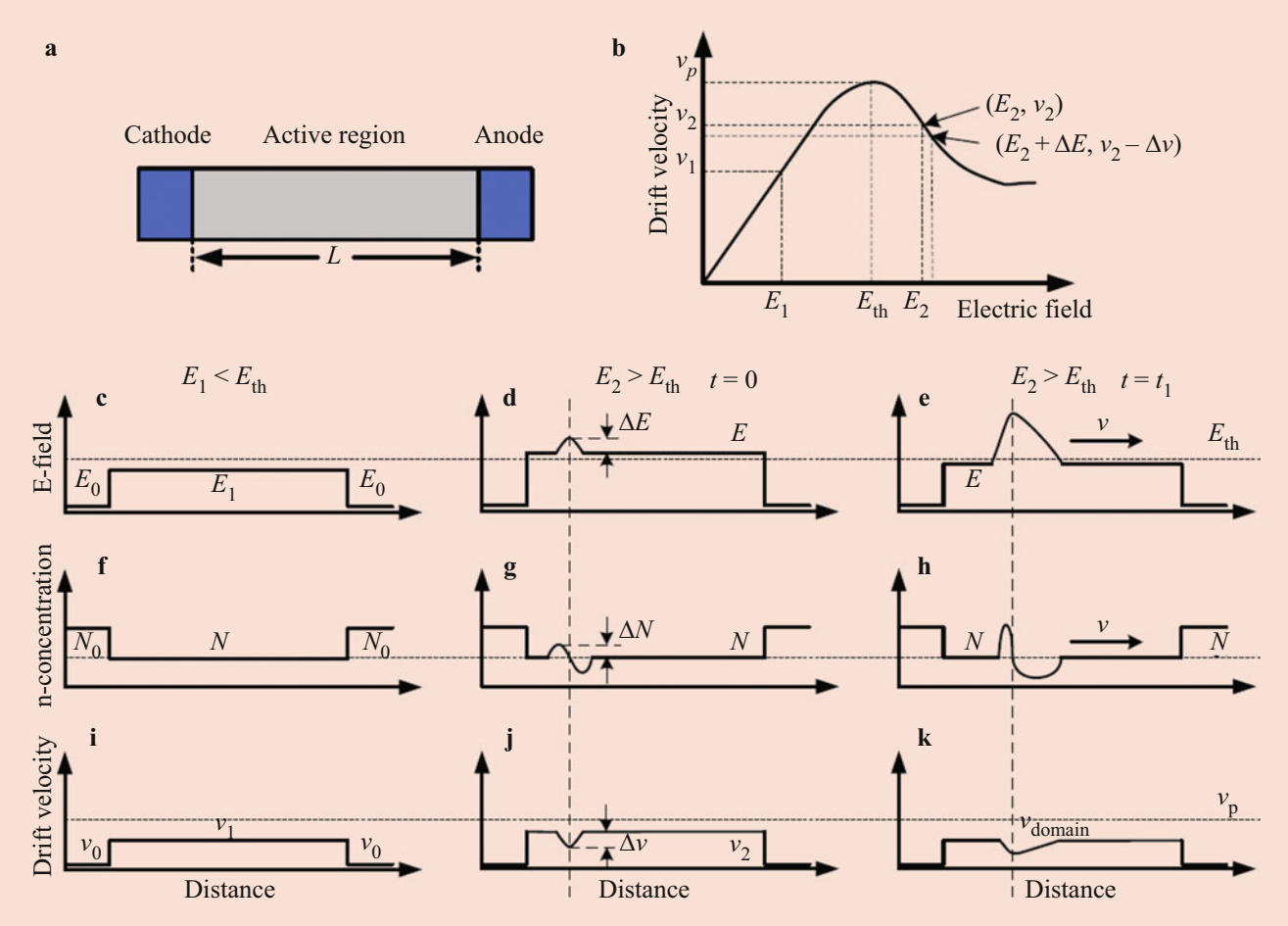

Fig. 22.3 (**a**) Scheme of a simple Gunn diode of length *L*. (**b**) Drift velocity versus electric field of the bulk material. (**c**, **d**) and (**e**) Illustration of the evolution of the electric field profile inside the diode for the formation of Gunn domain under transit-time mode of oscillation. (**f**, **g**) and (**h**) The same for the electrons concentration. (**i**, **j**) and (**k**) The same for the drift velocity [45]

flow is perpendicular to epitaxial layers of the device. To realise a Gunn oscillator, a vertical Gunn diode is embedded in a metallic waveguide cavity with a disc resonator, a radial line bias-tee, a sliding backshort and a heat sink as illustrated in Fig. 22.4b [45]. The disc resonator sitting on the top of the Gunn diode determines the output oscillation frequency. The radial line bias-tee allows DC bias to be applied on to the diode but prevents radio-frequency signals from leaking through. The heat sink beneath the Gunn diode helps dissipate heat generated as high current passes through the Gunn diode. The backshort serves as a tuner that improves circuit matching or frequency tuning by being manually moved forwards or backwards. The radio-frequency power is extracted from the rectangular waveguide. Gunn oscillators of this type are characterised by low phase noise, high-frequency stability and moderate power level. The highest oscillation from InP Gunn diodes is 160 GHz for its fundamental mode and 420 GHz from its third harmonics [53]. Although relatively high power is possible, the waveguide-based Gunn oscillators suffer from limited frequency tunability, lack of integration with integrated circuits, high cost of construction, difficulty of handling the thin and fragile diodes and poor reproducibility.

Forster et al. developed monolithic vertical Gunn diodes as shown in Fig. 22.4c [52,54]. Such Gunn devices are compatible with Monolithic Microwave Integrated Circuit (MMIC) process and have the potential for mass production. However, like conventional Gunn diodes, the oscillation frequency of these devices is still limited by the thickness of the mesa, and so far only 37.5 GHz has been demonstrated.

Alternatively, Gunn diodes can be configured in a planar form which has current flowing parallel to the epitaxial layers as shown in Fig. 22.4d. Compared with monolithic vertical Gunn devices, planar Gunn diodes have the advantages of lithographically controlled anode-cathode separation, and therefore the oscillation frequency of the device can be carefully controlled. Initial planar Gunn diodes only had a thin layer of n-doped material on the top of a substrate, and devices could operate at less than tens of gigahertz [57,58].

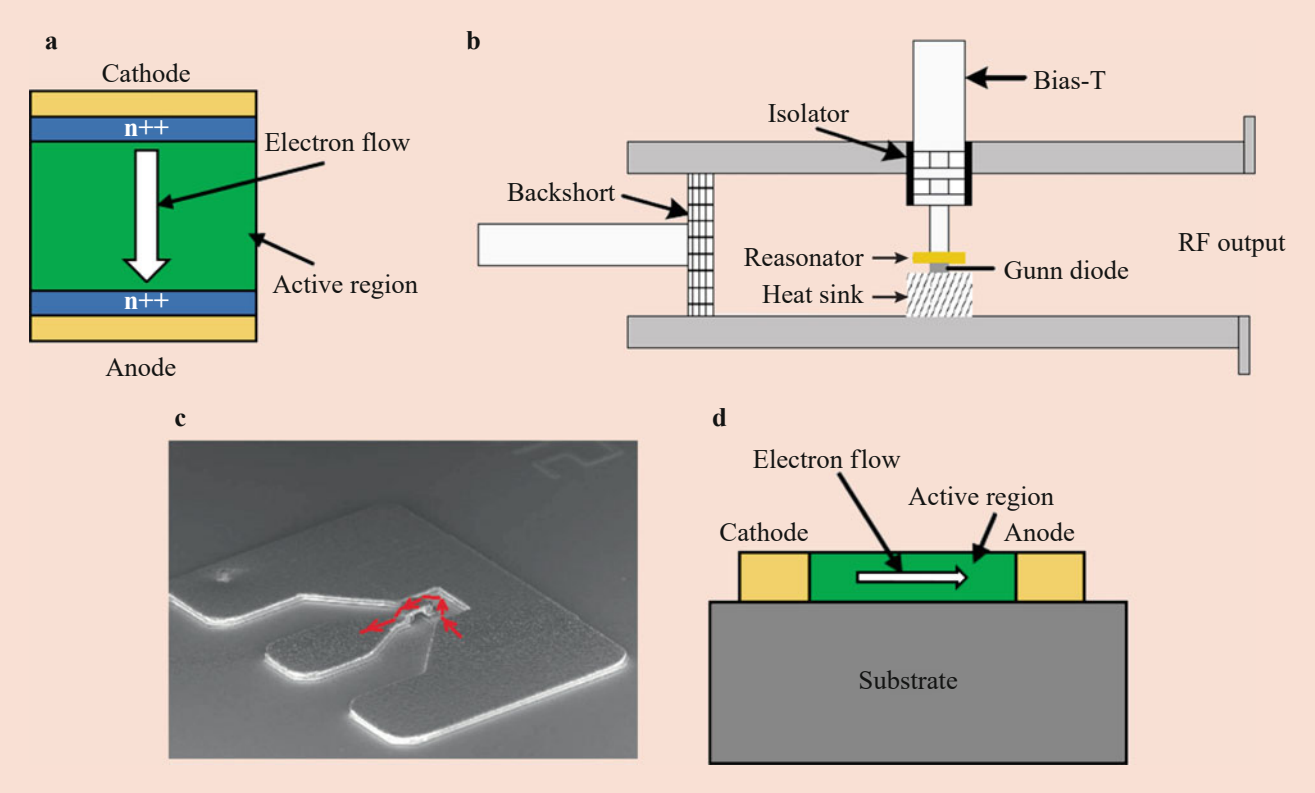

Fig. 22.4 Illustration of various configurations of Gunn diodes and oscillators. (**a**) Conventional discrete vertical Gunn diode and (**b**) its oscillator configured in rectangular waveguide cavity; (**c**) monolithic vertical Gunn diode [52] and (**d**) a planar Gunn diode

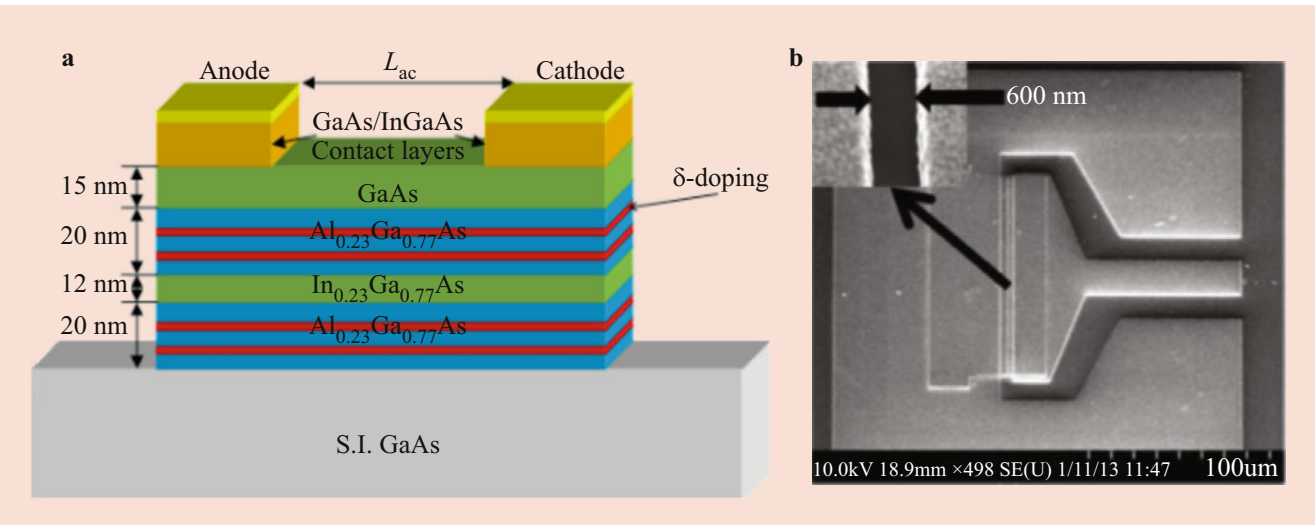

Fig. 22.5 Planar Gunn devices operating at frequencies greater than 100 GHz. (**a**) Schematic view of GaAs-based HEMT-like epitaxial layers [55], and (**b**) sub-micrometre planar Gunn diode oscillating at 307 GHz. (Reproduced from A. Khalid et al., *Journal of Applied Physics* **115**(11), 114502 (2014) [56], with the permission of AIP Publishing)

Recent developments of HEMT-like planar Gunn diodes, as shown in Fig. 22.5a, have significantly improved the fundamental oscillation frequency beyond 100 GHz [55, 59, 60]. The HEMT-like structure enables better electron confinement in the channel and higher drift velocity. With the advance of nanofabrication technology, planar Gunn diodes could generate oscillation beyond 300 GHz (Fig. 22.5b) [56].

22.2.4 Perspectives

Gunn diodes in planar configuration exhibit promising frequency performances which are highly desirable for future wireless and mobile communications, RADAR, imaging and other fields. There is still potential to improve the performances, such as frequency and power beyond 0.5 mW at 100 GHz [45] and 30 μW at 300 GHz [56]. Future research activities in this topic should include:

- improving oscillation frequency using materials with higher electron drift velocity, e.g. InAs or 2D materials, developing novel structures and decreasing channel length [61–64];
- enhancing output power by deploying multiple channels [45, 65], composite contact design [66] or materials with high bandgap, e.g. GaN [65];
- exploring new features and applications, for example, self-mixing effect and injection locking as detectors [67].

22.3 Schottky Diodes

Despite the continuous effort to develop new technologies to fill in the THz gap [4, 68–72], the Schottky-barrier diode (SBD) still offers unequalled performances at room temperature. It is used in the front-ends of heterodyne THz systems (Fig. 22.6) as ultra-wide bandwidth, stable, compact, tunable, spectrally pure and powerful emitter and/or to detect variation in sub-millimetre and THz radiation related to the physical temperature of optical blackbodies at a magnitude below 0.1 K and with a high resolving power up to 10^6. In addition to a proven operability for laboratory spectroscopy [73], SBDs have a historical background in practical implementation in many systems for signal generation or rectification. For instance, they have been successfully used in high-altitude balloons, airplanes or space-born telescopes for atmospheric science radiometry [74–77], in ground- and space-based astronomy and planetary science [78, 79]. These implementations have led to a growing demand of Schottky technology up to and above THz frequencies for a larger range of applications that span from biology and medicine [80], active imaging [81], telecommunication systems [24], astrophysics [82] to planetary science on our planet and the Solar System [83–85]. This plethora of applications makes it necessary to understand the operation of Schottky-based systems at their limits in order to reach the best performances. In the first part of this section, we address the basic principle of operation of the Schottky contact under zero DC bias and its frequency and temperature limitations related to material parameters. In the second part, we review the high-frequency limitations due to the parasitic elements located in the diode vicinity, and we discuss the associated effort in fabrication development (as illustrated in Fig. 22.7). Then, we extend the discussion to some of the configurations proposed to excite and balance the THz Schottky junctions in order to reach state-of-the-art performance. Finally, we review some of the future challenges in the main driving applications.

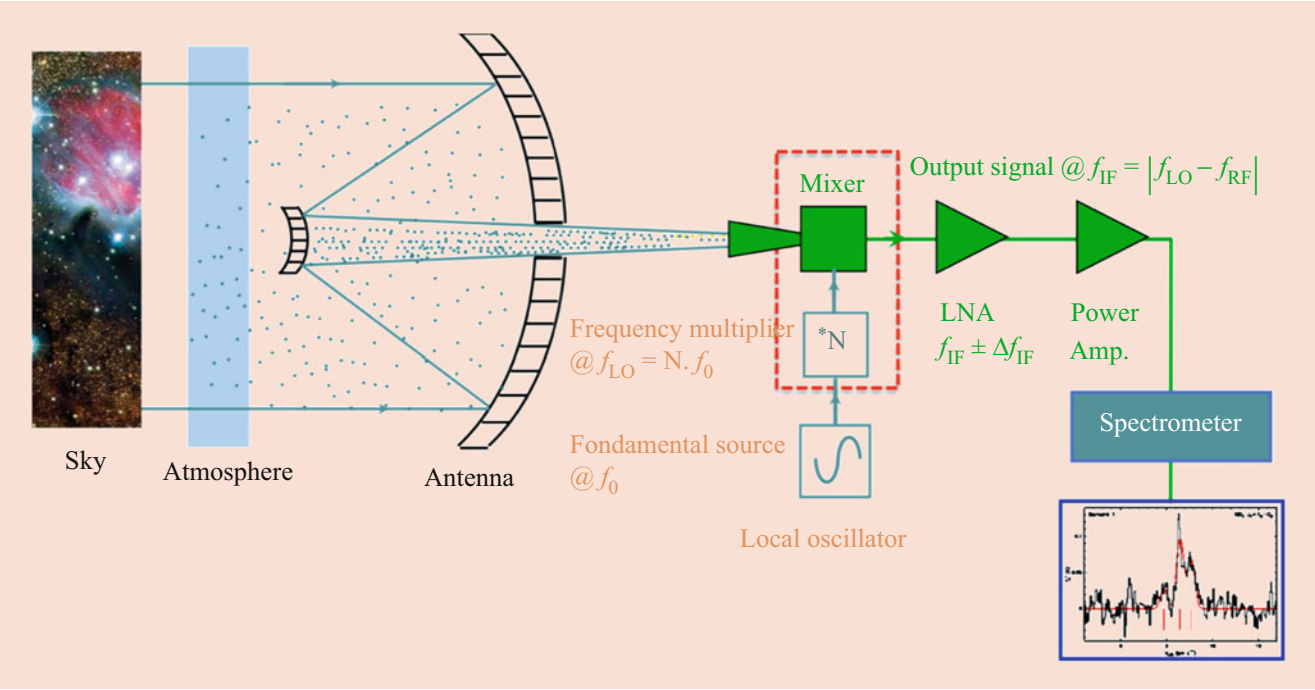

Fig. 22.6 Front-end heterodyne instrument showing detection mixer element and frequency multiplier

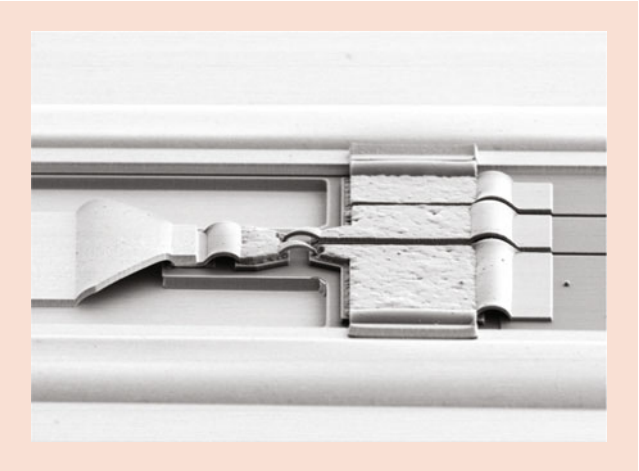

Fig. 22.7 Anti-parallel pair of Schottky diodes reprinted from [86] and developed for the 1200 GHz front-end of Jupiter Icy moon Explorer-Submillimetre Wave Instrument [85]

22.3.1 Terahertz Schottky Junction

The Schottky contact is formed by a metal to semiconductor contact. At room temperature, the current transport process is dominated by majority carriers through a thermionic emission over the barrier created by the unequal work functions of the two materials. The energy band structure of the junction is illustrated in Fig. 22.8, where E_F, *CB* and *VB* are the Fermi level, the conduction band and the valence band, respectively. As soon as the metal and the semiconductor are in contact, some of the free electrons in the semiconductor accumulate on the surface of the metal. The semiconductor is immediately depleted of electrons under the anode (the depletion region), and an electric field, which opposes further movement of electrons, is built between the anode and the semiconductor. As a result, a difference of potential is established between the semiconductor and the anode, that is, the built-in voltage V_{bi}.

The magnitude of the band bending V_{bi} and contact resistance depends on the semiconductor dielectric constant ε_{epi}, its epilayer doping density N and the Schottky barrier value $\varphi_B = \varphi_M - \chi_S$, where φ_M is the work function of the metal and χ_S the electron affinity of the semiconductor. The metal-semiconductor interface and the opposite boundary of the depleted area act like two capacitor plates in dynamic equilibrium, whereas the depletion region acts as a dielectric. By applying a bias voltage V to the junction, it is possible to influence the depletion width as

$$W(V) = [(2\varepsilon_{epi}/qN)(V_{bi} - V)]^{\gamma} \tag{22.7}$$

where q is the electron charge and γ the doping profile index, which depends on the junction geometry and the doping profile.

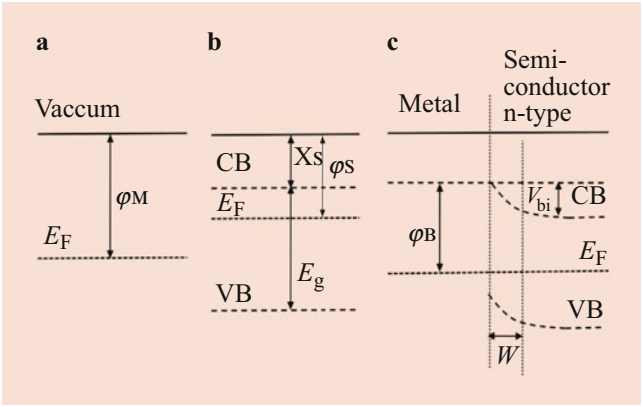

Fig. 22.8 (**a**) Energy band from metal, (**b**) semi-conductor and (**c**) metal/semi-conductor contact at thermic equilibrium

If we excite the junction with a large signal, the dopants electrons are emitted, pushed away and the depletion becomes wider in the reverse voltage region and narrower in the forward voltage region. The junction capacitance is calculated from the partial derivative of charge with junction voltage as

$$C_j(V) = A\gamma_c\varepsilon_{epi}/W(V) \tag{22.8}$$

where A is the anode area and γ_c a correction factor discussed in the next paragraph. The current-voltage relationship has been described in Ref. [87] by analogy with the drift-diffusion model of a $p-n$ junction as

$$I(V) = I_{sat}\exp\left(\frac{qV}{\eta k_B T} - 1\right) \tag{22.9}$$

with

$$I_{sat} = A^{**}T^2 W\exp\left(\frac{-\varphi_B q}{k_B T}\right) \tag{22.10}$$

where η is the ideality factor in order to compensate the non-ideal behaviour (with $\eta \geq 1$), k_B the Boltzmann constant, T the working temperature, I_{sat} the saturation current (ideally expressed as a function of temperature [88]) and A^{**} the modified Richardson constant [89]. These two non-linear regimes co-exist and are referred to as varactor and varistor modes. The excitation of the former or latter mode depends on the DC bias voltage value and polarity applied to the junction under operation. In the varactor case, the non-linearity of the capacitance dominates and favours high power handling capacities and harmonic generation with 100% theoretical efficiency at the junction level. The THz frequency limitation is driven by circuit and chain configuration [90, 91], breakdown voltage levels [90] or power handling limits [91]. In the varistor case, the non-linearity of the conductance is stronger in the vicinity of flat band. The varistor mode is preferably excited for mixing operation, and used in multiplier operation only when DC circuitry cannot be implemented. In this

case, the multiplier theoretical efficiency is reduced down to $1/m^2$, where m is the multiplying factor. The barrier cutoff frequency is defined as

$$f_c = \frac{1}{2\pi Z_s C_{tot}} \tag{22.11}$$

where C_{tot} is the capacitance of the depletion region under the Schottky contact and Z_s is, to a first approximation, the resistance of the undepleted semiconductor. This resistance extends to the Ohmic contact of the diode and is expressed for a circular anode as

$$Z_s = \frac{\rho_{epi} t_e \gamma_c}{R_o} \tag{22.12}$$

where t_e is the epilayer thickness, ρ_{epi} is the epilayer resistivity, R_o is the anode radius and γ_c is a correction factor between 0 and 1. As a result, the cutoff frequency varies linearly with the $\sqrt{N}\mu$ product, where μ is the electron mobility. The expression is extended below and above plasma frequency with different values depending on semi-conductor material, *i.e.* larger on n-type GaAs than on n-type Si Schottky contact [92]. These elementary considerations are used in order to optimize the anode size either analytically [93] or using Monte Carlo simulations [94]. GaAs THz mixers and multipliers typically feature sub-micron anodes diameters, 50–250 nm epilayer thickness and doping concentrations ranging from 10^{16} to 10^{18} cm^{-3}. For varactor operation at a given frequency, the anode size will be larger, the epilayer thickness thicker and the doping lower than for varistor operation. In addition, the temperature of operation is an important parameter in the functioning of the junction at THz frequencies. On one hand, the ever-increasing availabilities of driver emitters is pushing the power handling of multipliers, increasing the thermal stress and self-heating effect at the anode level, which can degrade the multiplier efficiency. To compensate this effect, Schottky junctions have been fabricated on semi-conductor materials such as silicon carbide (SiC) [95], gallium nitrite (GaN) [96, 97] and diamond, since they offer larger breakdown voltage and better thermal conductivity than GaAs. Other implemented solutions for a better thermal handling in multipliers consist in increasing the size and number of anodes, the substrate thickness and/or in transferring the substrate of THz GaAs planar Schottky onto quartz [98] or diamond [99]. On the other hand, cryogenic temperatures of operation are often implemented [100] when power is scarce, when the transmission line is lossy and most-of-all in order to minimize THz mixer and multipliers intrinsic and extrinsic noises. Under cryogenic operation, the conduction is no longer dominated by thermionic emission but by quantum tunnelling [101]. As the junction temperature drops, the ideality factor increases, and the junction knee moves to higher voltages. This effect can be compensated by modelling the multiplier or mixer efficiency at a maximum cryogenic temperature, by trading the series resistance with doping density [102] or by using semi-conductor material with high mobility and low-temperature electron freeze-out (typically 40 K for GaAs). Other materials are considered for they have higher electron mobility, implying that the knee of the I/V characteristics occurs at a lower voltage, such as InSb [103], offering a greater tradeoff between temperature of operation and local oscillator power requirement.

22.3.2 Parasitics of Terahertz Schottky Planar Diode

The size of the anode is quickly decreasing with increasing frequency. Indeed, an appropriate combination value of junction capacitance and series resistance implies sub-micron anode dimensions in the THz frequency range. For these dimensions, the efficiency of multipliers and mixers is strongly affected by the parasitic and fringing edge effects at the close vicinity of the junction. Therefore, the definition of the diode geometry and its integrated matching circuitry becomes a crucial part of the research development process [104]. The first millimetre wave and THz Schottky contacts were fabricated with a metal tip (whisker) inserted in a honey-comb structure. The latter structure presents a very little parasitic capacitance. Whisker mixers quasi-optically pumped with CO_2 lasers still keep the state-of-the-art performance around 2 THz [105] and up to 5 THz [106] and have flown in satellites [75]. Nevertheless, the whisker-mounted diode suffers from reliable repeatability. Thus, planar technology was pushed forward in order to keep the high capacity of the whiskered structure, while adding the robustness necessary for spatial qualification levels to the micronic structure [77, 86,90]. The first planar discrete diode flip-chip mounted onto a larger substrate [107] offered the possibility of using a different substrate material, such as quartz [108] or SiN [77,90], to reduce the line dielectric constant. However, this operation provides few microns positioning uncertainty between the diode chip and the matching network circuit, which is enough to affect the performance in terms of bandwidth. Therefore, at 600 GHz and up to 2.5 THz, GaAs monolithic fully integrated circuit technology [109] has been developed on micron-thick and high resistivity GaAs membranes. This way, one can limit substrate mode effects and control accurately both the parasitics and transmission line impedances (Fig. 22.9).

The planar diode discrete or integrated MMIC Schottky device is fabricated on a high-conductivity n-type GaAs substrate supporting a very pure, high conductivity n-buffer layer. This layer assures a low series resistance, and prevents the substrate impurities from diffusing into the epitaxial layer during the fabrication process. A very thin *n*-epitaxial layer is grown on top of the buffer. The contact of the metal anode to

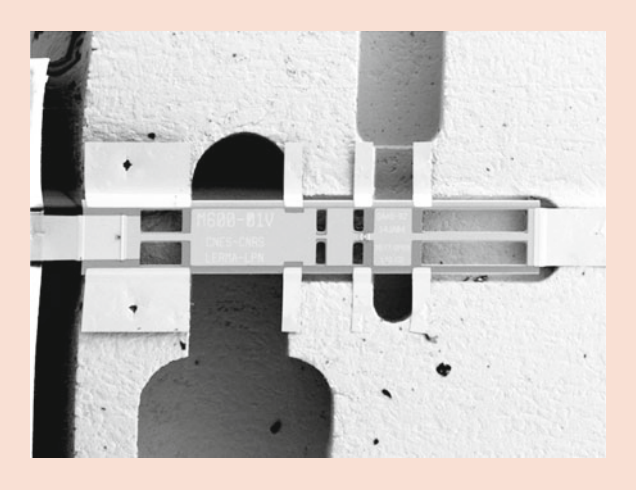

Fig. 22.9 MMIC integrated Schottky circuit configuration in split-block channels described in [110]

the epitaxial layer forms the rectifying junction, commonly made of gold-germanium, gold-platinum or gold-titanium for GaAs diodes. Finally, an Ohmic contact is formed by a metal layer on the substrate, which forms the cathode pad. The anode is defined on the top surface and is isolated by an oxide (SiO_2) layer. Different manufacturing processes based on similar fabrication steps prefer either contact lithography [109] combined (or not) with a more precise but expensive electron-beam system [107, 111, 112].

Figure 22.10 illustrates the SBD cross section and its parasitic lumped components identified in a planar SBD. The total parasitic capacitances C_{Tot} is noted:

$$C_{\text{Tot}} = C_{\text{j}}(V) + C_{\text{f}} + C_{\text{p}} + C_{\text{pp}} + C_{\text{gap}} \tag{22.13}$$

where C_{f} is the capacitance between anode finger and n^+-GaAs, and the sum of C_{p}, C_{pp} and C_{gap} is the total pad-to-pad capacitance $C_{\text{p,sum}}$. The quantity $C_{\text{j}}(V)$ is defined in Eq. (22.8) and depends on the correction factor γ_{c}, which is affected by the edge effect due to the small area of the anode. For a circular shape anode γ_{c} is given by [92]

$$\gamma_{\text{c}} = 1 + 4b_1 \frac{W(V)}{R_{\text{o}}} + 3b_2 . W^2(V) R_{\text{o}}^2 \tag{22.14}$$

where b_1 and b_2 are numerical value of, respectively, 0.36 and 0.34. For square shape anodes, γ_{c} becomes [113]

$$\gamma_{\text{c}} = 1 + 4b_1 \left[\frac{(L + l)W}{Ll} \right] \tag{22.15}$$

where L and l are the anode side dimensions. The model has been extended to the case of general shape and considering surface effects in Ref. [114]. For the anti-parallels pair structure described in the next paragraph, we note that $C_{\text{p,sum}}$ parasitic capacitance is short-circuited in the even-harmonic equivalent circuit. This is compensated by a supplementary mutual inductance between fingers that shall be minimized to avoid a resonance effect on the mixer conversion loss. In addition, the series impedance can be written as a sum of different impedances and resistances [104]

$$Z_{\text{s}} = R_{\text{s,epi}} + R_{\text{sheet}} + Z_{\text{spread}} + Z_{\text{skin}} + R_{\text{ohmic}} \tag{22.16}$$

where $R_{\text{s,epi}}$ stands for the resistance created by current flow through the un-depleted epitaxial layer, R_{sheet} corresponds to the current flow through the substrate depending on the plasma resonance correction factor [115], Z_{spread} stands for the bulk spreading impedance caused by expansion of the current after the small anode area and Z_{skin} is the skin effect impedance. The control of the 3D parasitics and its modelling [104] is crucial for operation optimisation at THz frequencies and can be accurately controlled and optimized with planar technology. Measurements lead to the extraction of the lumped elements [116]. Other structures have been fabricated to reduce the contribution of the spreading resistance, such as vertical diodes [117] or structures where the membrane is locally removed by back-side photolithography [118]. From the metal contact point of view, carbon nanotubes Schottky contacts could offer an alternative to their solid-state counterparts because of the nm diameter scale junction areas, high electron mobilities and low estimated capacitances [119].

22.3.3 Terahertz Schottky Multipliers and Mixers

The performance of the multipliers and mixers is evaluated on the basis of three indicators: the power efficiency in the case of multiplier, the conversion losses and noise temperature for a mixer. Altogether the Schottky contact quality, the balance and geometry of the circuit as well as its propagating lines dimensions have to be optimised with great care in the THz range. At these frequencies, the line loss starts to be significant enough to overcome the signal couplings, and the available local oscillator power is scarce. The current state-of-the-art THz circuit configurations introduced in the previous paragraph feature either planar SBD flip-chip mounted onto a thin substrate or integrated Schottky MMIC [109] that are inserted in a narrow channel. The signals are transposed from a TE_{01} mode in the waveguide input port to a quasi-TEM mode and progressively matched to the diode cell on each of the frequency bands (RF, LO and IF for a mixer and first and n^{th} harmonic for a multiplier). In addition, the arrangement of the diode in two or three terminal port structures [120, 121] illustrated in Fig. 22.8 favours even or odd mode harmonic generation or mixing, but also signal balancing including AM signal noise rejection and signal

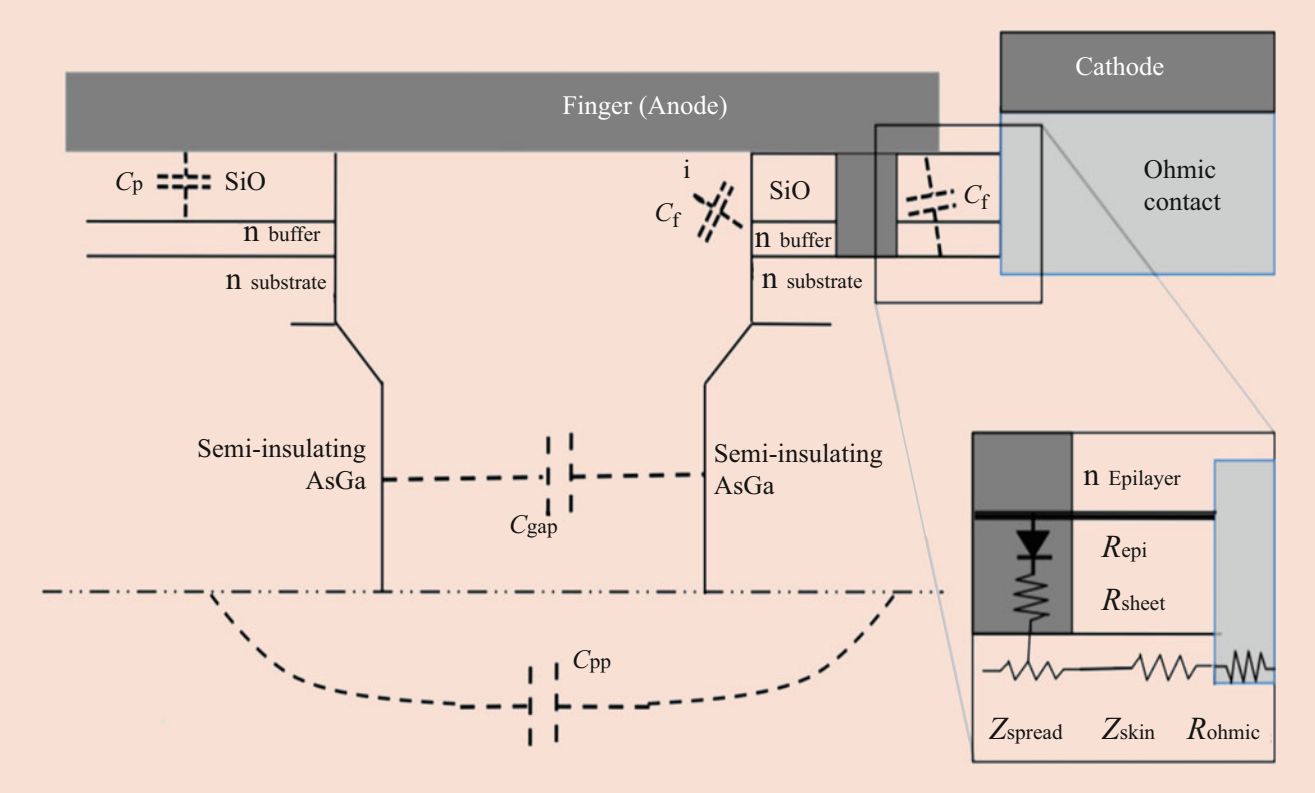

Fig. 22.10 Schottky-barrier diode (SBD) electrical model and its parasitic lumped components

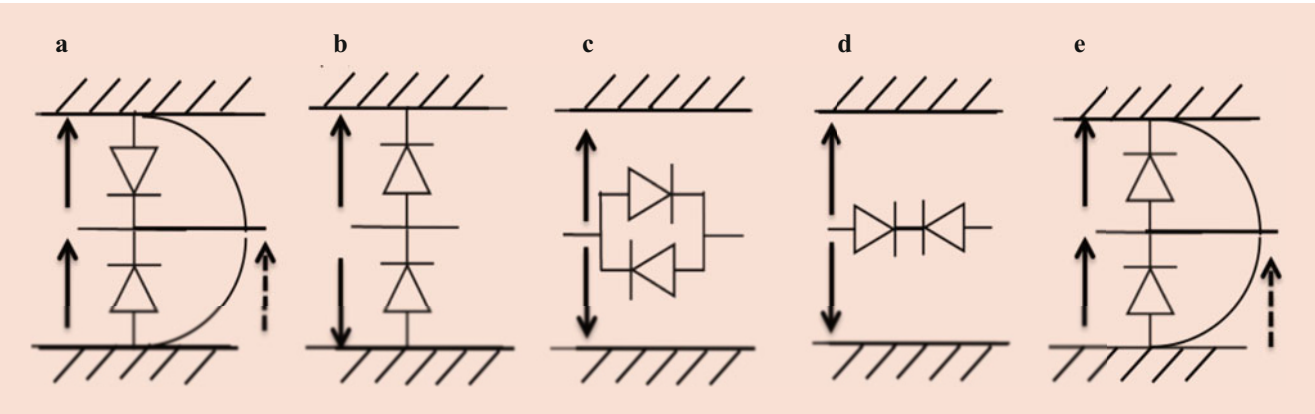

Fig. 22.11 Two and three terminal circuit configuration in split-bloc channels. The arrows represent the primary mode excited (TE_{01} mode in the waveguide input port) and quasi-TEM mode in the transmission lines. Configurations a, b, c, d, e and corresponding references are detailed in Table 22.1.

isolation in order to leverage emitter stability, interference and spurious signals.

In a mixer, a minimum of two balanced anodes guarantee minimum noise contribution, but the number of anodes can increase for multiplier operation in order to improve power handling capabilities. In both cases, the characteristic discrepancies of the diodes can have a significant impact on the total conductance and could be compensated by independent DC biasing. The DC bias of the diode is additionally necessary in varactor frequency multipliers where high power efficiency is required or in mixers to compensate from the low power availabilities of local oscillator emitters at THz frequencies. The implementation of DC biased circuitry at high frequency is particularly delicate, as it can lead to a breaking of the symmetry involved in the balance of the devices, produce cross-mode coupling and also in a non-negligible way pick up external spurious during operation.

Table 22.1 Selection of different implemented configuration

Configuration	*a*	*b*	*c*	*d*	*e*
Doubler	[91, 122]		[120]		
Tripler		[123]	[124, 125]	[126, 127]	
Mixer		[121, 128]	[86, 110, 121]		[129]

Figure 22.11 and Table 22.1 give a selection of different implemented configurations. Configuration *a* favours a very high third harmonic isolation in [122] for doublers. In [91] it is enhanced with a two-port parallel arrangement at each diode level in order to improve the power handling capabilities. Configurations *b* and *c* allow trapping the second harmonic in the diode loop. They are widely implemented in subharmonic mixing to reduce the LO frequency of operation down to half of the RF signal frequency. Configuration *b* is implemented in open-loop configuration triplers [123,124] or balanced subharmonic mixers [128]. However, configuration *c* strengthens the confinement and balance of the second harmonic signal, and provides wider channel dimensions not affordable by open-loop configuration, and thus introduces a larger range of low loss transmission lines for matching the input and output signals securing best mixer performances at 600 GHz [110] up to 1.2 THz [128] or varistor tripler [125]. A variation of configuration *c* with a split central line gives access to the even harmonics for doubler [120] or subharmonic mixing. It is also proposed for low noise and wide instantaneous IF bandwidth fundamental balanced mixers (FBM) predicting good noise temperature performance and more than 4 times typical RF and IF instantaneous bandwidths [130] or for frequency tripling over 50% relative bandwidth at 300–520 GHz in Ref. [130]. The DC bias circuit can be achieved in configuration *c* where the diode cell has to be revisited at a lower level to allow a DC path while keeping an anti-parallel arrangement at RF, LO and IF frequencies necessary for subharmonic operation [86]. The fabrication methods rely on fabrication accuracy supplementary insulator layer underneath the bridge in order to avoid DC contact from n^{++} layer to gold. A single DC path feeding the two anodes has been demonstrated in Ref. [86] at 1.2 THz (Fig. 22.6). Independent DC-paths for the diodes of an anti-parallel pair mixer have been proposed in Refs. [130]. Both solutions feature a multilayer process that leads to a high fabrication effort and rely on the quality of the insulators and pinhole density level. Another design of a subharmonic mixer based on a splitted microstrip transmission line (or slotlines) consists in applying the bias through the IF port avoiding multilayer process [131]. Finally, configuration *d* is an anti-series configuration, which epilayer has to be optimized for odd harmonic generation [126, 127] and configuration *e* is a balanced configuration used in fundamental mixing [129]. FBMs can theoretically reach better noise performance than SHMs [132].

22.3.4 Driving Application of THz Schottky Diodes

Both Schottky-based detectors and emitters have a long history of practical implementation in laboratory-, ground- or space-based systems. We will now review the main driving applications. These applications are actively shaping the technological development of Schottky-based THz multipliers and mixers. In THz astronomy the interest lies in both interstellar medium and planetary atmospheres, since they are incredibly rich in molecular species with spectral rotational and vibrational signatures that lie in the 1–10 THz frequency range. The Heterodyne Instrument for the Far-Infrared (HIFI), launched on the Herschel Space Observatory, has provided an unprecedented view of the Universe up to 1.9 THz [79]. Important discoveries, especially the abundance and structure of singly ionized carbon, have now been documented. However, many important molecule lines are beyond this frequency range [129]. For instance, the OH line located around 2.5 THz is a fundamental tracer of the interstellar chemistry of azote and oxygen and can be used for the study of diffuse clouds. Relatively close to this frequency the HD line is expected at 2.675 THz. This molecular line stands as the important tracer of the cosmological H/D ratio, the formation of the first generation of stars and of the evolution of the giant planets. Moreover, the HD line would provide planetary scientists critical information on the evolution of the atmosphere of rocky planets and moons. For all the reasons above, heterodyne receivers are most suitable for molecular detection in this THz frequency range as they offer high spectral resolution along an instantaneous bandwidth of few GHz. The mixer of choice is often based on superconductor technology, such as the Hot Electron Bolometer (HEB) mixer. HEBs work above superconductor-insulator-superconductor (SIS) mixer operating frequencies from 500 GHz to 5 THz with noise temperature around 800–1000 K, which is about 10–20 times the quantum limit. HEB and SIS detectors require 4 K or below for operation relying of costly cryocoolers or liquid helium cryostats. Commonly, they are actively coupled to room temperature solid-state technology LO system, *i.e.* the herein discussed Schottky-based multiplier emitters . These emitters offer the best output power with wide frequency band tuning and unequaled spectral purity. Their phase noise comes from the synthesizer's degrading naturally as a function of the order of multiplication. Recently, sustained effort has been done on building heterodyne receiver arrays below the THz frequencies, and many of them have been deployed on ground-based telescope at high altitude [133]. While the Schottky-based multiplier emitters also appear to be the best

option for developing a portable 2–3 THz receiver array [134], there is still a great effort to be done on improving their efficiency and their coupling to the detector detector and largely increase the power handling of multipliers to making state-of-the-art emitter and lower frequency driver stages reaching above 1 mW of continuous wave (CW) power at 1 and 1.5 THz [91, 135]. In THz radiometry, composition and wind measurements with a broad temporal and spatial coverage are critical for our understanding of the dynamics and coupling processes in the thermosphere/ionosphere system. They can be investigated by measuring dynamical variables such as neutral wind speeds, temperature and atomic oxygen density above approximately 100 km. The 2.06 THz emission is a promising line for remote sounding of thermospheric winds. The strong interest in this line is pushing towards the development of Schottky-based mixers for room or passively cooled temperatures (150–300 K) [118] that can fit in a 6U CubeSat for spaceflight or ultra-compact global radiometer system [136]. A larger user range of applications is being developed going from biology and medicine [80], active imaging [81] and telecommunication systems [24, 137], which are focusing on the implementation of adaptation of the systems to their particular use and environment. Regarding telecommunications, the trend in electronics consumer market is to transfer ever-increasing amount of information wirelessly to conceive standards able to accommodate data rates of hundreds of Gb/s and even Tb/s. Despite fibre optic extension, millimetre-wave backhaul (BH) market will still connect more than 50% of mobile sites with point-to-point (P2P) and point-to-multipoint (PMP) links for front- and back-hauling for dense urban scenarios. In this particular context, high-sensitivity sub-THz receivers preserve the amplitude and phase information of the incoming radiation to minimize the signal-to-noise-and-distortion-ratio (SNDR) characteristics, with best instantaneous IF BW [24, 137]. The next generation of Schottky-based solid-state instruments will have to keep their inherent performance in terms of spectral resolution, while achieving high portability related to their operative environment. They will open the path to new portable THz instruments with a flexible observation tradeoff between sensitivity, mapping speed and spatial coverage that could be adapted to in situ spectroscopic measurements and portable telecom systems.

22.3.5 Perspectives

The application mentioned above will benefit greatly from the potential improvement margin in sensitivity or continuous power generation performances of the SBD at THz frequency. This optimisation focuses on several aspects at different levels starting from the junction material, parasitics, frequency cutoff, and power handling (see Sects. 22.3.1 and 22.3.2), its implementation in an embedded RF circuit (see Sect. 22.3.3) and finally its use at system level (see Sect. 22.3.4).

22.4 Resonant Tunnelling Diodes

Resonant-tunnelling diodes (RTDs) have re-emerged in the recent years after almost two decades of oblivion as a viable active device for THz frequencies. Meanwhile, the fundamental operating frequencies of RTD oscillators have almost reached 2 THz, RTD oscillators work at room temperature, can have tiny dimensions and provide an output power close to mW level. They can also be used as detectors. Combination of all these salient features in one device suggests RTDs as a promising enabling technology for THz applications. This section will review the basic principles of operation of RTDs and RTD oscillators, the present status of the RTD sub-THz and THz radiation emitters and detectors, and it will outline several possible applications for RTDs.

22.4.1 Resonant Tunnelling

The resonant-tunnelling phenomenon is essentially a quantum-mechanical analogue to the transmission of light through a Fabry-Pérot resonator known for more than a century in optics. Resonant tunnelling has been described in a classical book on quantum mechanics already 70 years ago [138]. Due to resonant tunnelling, the double barriers become highly transparent for electrons, which are in resonance with one of the quantum well (QW) states between the single barriers [138] as described in

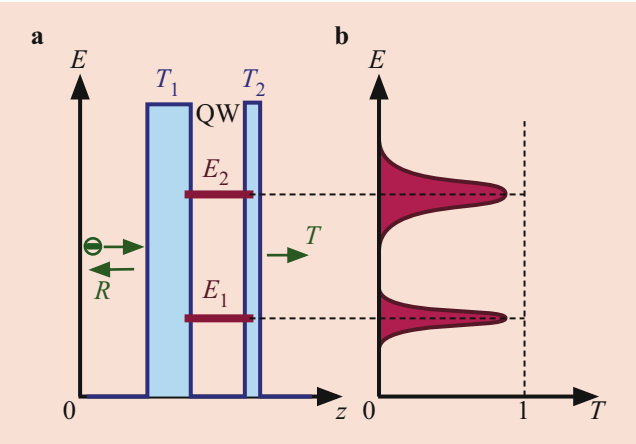

Fig. 22.12 (**a**) Tunnel double barrier consisting of two barriers with low tunnel coefficients ($T_i \ll 1$) and a QW with resonant states (E_i) between them. (**b**) The total tunnel coefficient of the double barriers (T) exhibits a series of resonant-transmission peaks, when the energy of the incident electron coincides with one of the resonant states in the QW. R indicates the reflection coefficient associated with carriers reflected by the barriers

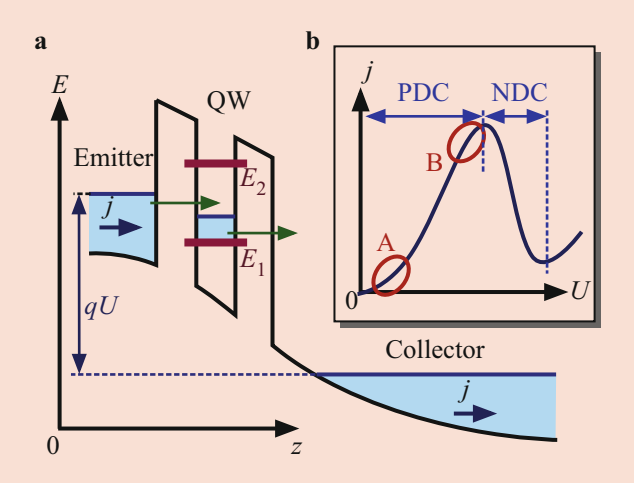

Fig. 22.13 (**a**) Band diagram of a semiconductor heterostructure RTD, where a double tunnel barrier is sandwiched between n-doped emitter and collector. The QW contains two energy levels (E_1 and E_2). A voltage difference U is applied between the emitter and collector contacts. (**b**) N-shaped RTD I-V curve with an NDC region. The region of the onset of the resonant tunnelling (**a**) and the positive-differential-conductance (PDC) region (**b**), where the current is starting to switch off, exhibit highly nonlinear I-V curve, which could be used in THz detectors

Fig. 22.12. If the barriers are symmetric, then the resonant-tunnelling transmission becomes as high as 1, i.e. the barriers become ideally transparent. The phenomenon could be used to construct tunnel devices with particular properties. Of special interest and importance are resonant-tunnelling diodes (RTDs) with an N-shaped I-V curve and a negative-differential-conductance (NDC) region; see Fig. 22.13. The RTDs are usually based on semiconductor heterostructures, where two (or sometimes more) tunnel barriers are sandwiched between highly doped contact regions. The electrons are resonantly tunnelling through the barriers from the emitter to the collector. With increase of the applied bias (U), at some point, the QW resonant state (2D subband in the QW) shifts below the conduction-band bottom in the emitter and, consequently, the resonant current due to elastic tunnelling through the QW states becomes impossible. This leads to a decrease in the RTD current (j) and appearance of an NDC region. This NDC region makes the RTD an active device, i.e. the RTD exhibits gain in this region of applied bias. The mechanism of NDC in RTDs with two and more barriers and even resonant-tunnelling transistors have been predicted and described more than half a century ago [139]. However, practically realisable RTDs have been described a decade later and experimentally demonstrated shortly afterwards [140].

An instructive analysis of coherent resonant tunnelling in RTDs (as outlined above) could be found in Ref. [141]. An alternative point of view (sequential-tunnelling model [142]) suggests that electrons can tunnel through the barrier in two steps: they tunnel into the QW first, then they loose their coherence due to a scattering event, and afterwards, as a second step, they tunnel further to the collector. Surprisingly, the RTD I-V curves turn out to be the same in both approaches [143], thus reproducing the NDC region equally well. By contrast, shot noise suppression below a value of 0.5 was found to discriminate resonant tunnelling from sequential tunnelling, where maximum suppression cannot achieve values below 0.5 [144].

Coulomb interaction has an ubiquitous effect on the DC and AC RTD characteristics. It leads to an increase in NDC, i.e. to a steeper decrease of the current in the NDC region. In high-quality RTDs, it can even transform an N-shaped I-V curve into a Z-shaped one with a hysteresis region [145,146].

22.4.2 RTD Oscillators

An RTD oscillator consists of a passive resonator (it could be a simple resonant LC circuit) connected to an RTD operating in the NDC regime. The NDC can compensate for the losses in the resonator thus bringing the resonator into oscillations. The high-frequency properties of RTDs enable operation of such oscillators even at THz frequencies, which are record-high for electronic devices.

The fundamental oscillation frequencies of RTD oscillators have been increasing very rapidly during the 1980s with a frequency of approximately 0.7 THz reported in 1991 [147]. The sub-THz oscillators at that time have been based on hollow-waveguide resonators with a whisker-contacted RTD mounted inside the waveguide. Fabrication of such oscillators was a challenging task, and higher operating frequencies could not be achieved in the subsequent almost 20 years; therefore the development and research on RTD oscillators has almost stopped at that time.

A breakthrough has been achieved around 2010, when two groups have demonstrated THz RTD oscillators at ≈1 THz [148] and ≈1.1 THz [149]. The oscillators were based on resonant slot antennas integrated with RTDs. This concept of RTD oscillators was demonstrated for the first time earlier in 1997 at 650 GHz [150]. Meanwhile, the frequency of almost 2 THz has been achieved with such RTD oscillators [151]. On-chip slot-antenna oscillators are usually mounted on a hemispherical Si-lens [148, 151], since antenna radiation is predominantly emitted into the substrate. The Si-lens makes such oscillator relatively bulky ($\sim$cm^3). On the contrary, slot-antenna oscillators on a membrane could be integrated with additional planar horn antennas, which leads to a very compact ($\sim$mm^2) THz emitter [149]; see Fig. 22.14.

In recent years, few other types of sub-THz and THz RTD oscillators have also been reported, e.g. RTD oscillators integrated with on-chip patch antenna at 0.5 THz [152]. It has also been shown that microstrip travelling-wave RTD oscillators should be operating at THz frequencies [153].

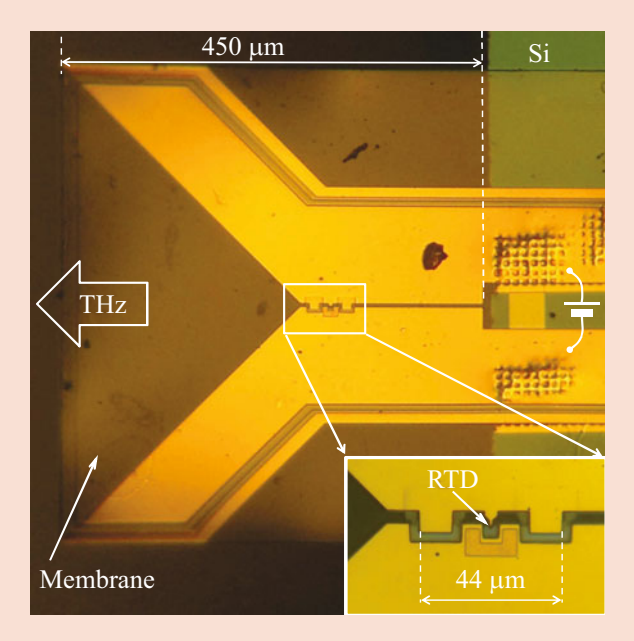

Fig. 22.14 Membrane slot-antenna THz RTD oscillator with an additional Vivaldi antenna. (Reprinted from [149], with the permission of AIP Publishing)

Such oscillators are similar to metal-metal THz quantum cascade lasers (QCLs), where the cascade is replaced by its single period, i.e. an RTD . Contrary to THz QCLs which require cryogenic cooling, microstrip RTDs and all other types of RTD oscillators are room-temperature devices.

GaAs RTDs with AlAs or AlGaAs barriers were usually used in the past [154–156], since it is a lattice-matched material system. Later on, InGaAs RTDs with AlAs barriers and InGaAs/InAs QW started to be used [150]. AlAs barriers are strained in this case, but they are higher (≈1.2 eV) than those in GaAs/AlAs RTDs, that allows one to suppress "valley" current and the peak-to-valley current ratio could be as high as ≈50 at room temperature in this material system [157]. In such RTD with very thin barriers (≈1 nm), a current density of ≈30 mA/μm^2 has been achieved [151], thus leading to high NDC and high gain. This material system is predominantly used nowadays [148, 149, 151, 158–160].

Antimonide RTDs have been studied as well in the last decades due to their type-II band offsets at the InAs/AlSb heterojunction and particularly low-resistance Ohmic contacts to InAs. For example, InAs/AlSb RTDs have been used in oscillators working at ≈0.7 THz [147]. GaN/AlN RTDs start to show promise in recent years; however their current density and the conductance of the Ohmic contacts are an order of magnitude lower than those in InGaAs/AlAs RTDs [161]. Another intriguing material system is based on graphene layers separated by a few-monolayer-thick boron-nitride barrier. NDC in such structures has been demonstrated recently [162].

22.4.3 Frequency Limitations of RTDs

Two obvious time constants could be identified in RTDs. One is the tunnelling time through a single barrier; it is extremely short [163] and not relevant for frequency limitations of RTDs. The second one is the tunnel lifetime (τ) of the quasi-bound (resonant) states in the RTD QW. τ can become arbitrary long, and when we reduce the tunnel transparency of the barriers, it might potentially limit the operating frequencies of RTDs [164].

However, the dynamics of RTDs is quite involved [160, 165–167]. It is determined by the QW-charge relaxation processes, which could be described in the linear response approximation by a relaxation time constant ($\tau_{\rm rel}$). If the Coulomb interaction effects are neglected, then $\tau_{\rm rel} = \tau$, but Coulomb interaction modifies $\tau_{\rm rel}$ considerably. In general, $\tau_{\rm rel}$ depends on the thicknesses of the RTD layers (RTD geometry), material parameters, doping profile and the operating regime of RTD. Particularly, $\tau_{\rm rel} < \tau$ and could be even $\tau_{\rm rel} \ll \tau$ in the positive-differential-conductance (PDC) region of the RTD I-V curve. On the contrary, $\tau_{\rm rel} > \tau$ and could be $\tau_{\rm rel} \gg \tau$ in the NDC region. These effects have been confirmed experimentally [168].

Another important consequence of the Coulomb interaction is the displacement currents, which provide a mechanism of current flow through the RTD barriers at high frequencies ($\tau_{\rm rel}\omega \gg 1$, ω is the angular frequency) [160, 165, 167]. Particularly, the real tunnel current can be flowing through the emitter RTD barrier, but the displacement current mechanism provides the current flow through the collector barrier. The mechanism leads to persistence of NDC to the frequencies, which are far beyond the inverse relaxation-time limit, i.e. when $\tau_{\rm rel}\omega \gg 1$. The high-frequency NDC is particularly large in RTDs with heavily doped collectors; see Fig. 22.15a. These effects have been demonstrated directly experimentally [168]. Further on, it was experimentally demonstrated that RTD oscillators can also work at frequencies far beyond or at least close to the inverse relaxation-time and tunnel-lifetime limits [149, 169, 170]. The frequencies covered in these experiments are up to 1.1 THz, but the analysis of the experimental data indicates that these are ubiquitous effects, which should extend to the higher frequencies as well.

Both the relaxation-time and displacement-current effects could be included into a general, but rather simple 4-element RLCR equivalent circuit of RTDs [160, 165, 167]; see Fig. 22.15b. The circuit corresponds to the following equation for the RTD admittance (Y_{RTD}):

$$Y_{\rm RTD}(\omega) = i\omega C_{\rm ec} + G^{\infty} + \frac{G^0 - G^{\infty}}{1 + i\omega\tau_{\rm rel}}, \qquad (22.17)$$

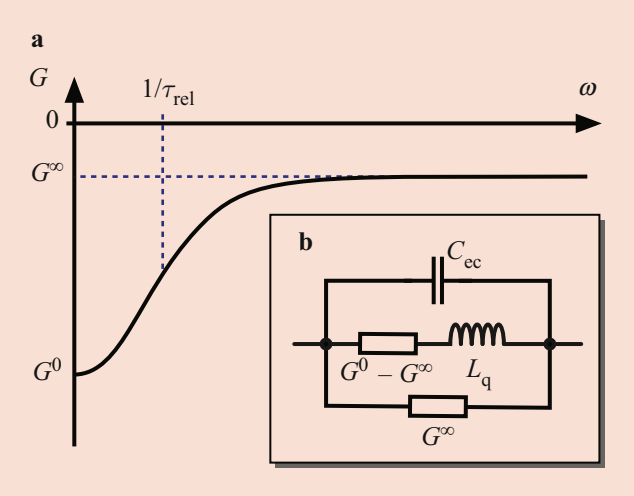

Fig. 22.15 (**a**) A sketch of the frequency dependence of the RTD conductance in the NDC region of a double-barrier RTD with a heavily doped collector. The DC RTD conductance (G^0) rolls off at the frequency of $1/\tau_{rel}$ and saturates at the level G^∞ with the further increase of frequency. (**b**) A general AC equivalent circuit of a double-barrier RTD

where C_{ec} is the geometrical emitter-collector RTD capacitance, L_q is a "quantum" inductance, equal to $\tau_{rel}/(G^0 - G^\infty)$. The circuit describes well the experimental data on RTDs and RTDs oscillators mentioned above [149, 160, 168–170].

Although the above inherent limitations of RTDs could be overcome by a proper design of RTD layers, the limitations due to parasitics will remain, and they are still limiting the operating frequencies of RTDs and RTD oscillators. The main parasitic contribution is coming from the RTD contact resistance, although other contributions are also important, especially at THz frequencies, e.g. the spreading resistance of the doped semiconductor layers, inductive contribution of an air bridge, Ohmic losses in the metal layers of the antenna and resonator, etc. [159, 160].

Nonlinearity of RTD I-V curve (Fig. 22.13b) can be used for THz radiation detection, the RTD acting as a passive device in this case. Additionally, it can be used to probe the inherent frequency limitations of RTDs. Such measurements have demonstrated a huge potential of RTDs: the nonlinear RTD response has been measured up to 3.9 THz already several decades ago [171, 172].

22.4.4 Applications of RTDs

RTDs are not used in practice yet. However, they do show great promise for practical applications in the last decade. RTD oscillators are evolving into a viable and enabling technology for THz and sub-THz emitters: they are quite simple devices [159, 160] of sub-mm dimensions [149], operating at room temperature and providing an output power close to a mW level while their power consumption is quite low (dc-to-THz conversion efficiency is at the level of few percent); they cover the frequencies from zero to 2 THz [151]. Combination of all these properties in RTD oscillators is unique for THz emitters.

The oscillator linewidth is an important parameter for practical applications. A free-running RTD oscillator has the linewidth in the range of ≈10 MHz [169], although with a phase-lock-loop stabilisation, it could be reduced to ≈1 Hz [173]. Another important parameter is the frequency tunability. Due to variation of the RTD capacitance with bias, RTD oscillators are tunable in a narrow frequency range of ≈1–2% [159, 160]. The tuning range can be increased to ≈10–20% by building an additional varactor into an RTD oscillator. Integrating several such oscillators in one chip, one can extend the tuning range even further, e.g. up to ≈40% [174].

Meanwhile, THz systems based on RTD oscillators have been also demonstrated experimentally. For example, imaging system and high-resolution spectrometer with RTD oscillators have been demonstrated at ≈300 GHz. High-data-rate wireless transmission has been also reported: single-channel 34 Gbit/s transmission at 500 GHz and two-channel 2×28 Gbit/s transmission [175] relying on frequency (500 GHz and 800 GHz) and on polarisation (2 orthogonal linear polarisations) division multiplexing.

SBD have been used as detectors in the above data-transmission experiments. However, nonlinear RTD detectors could be used instead: wireless system at ≈300 GHz based on RTDs as oscillators and detectors with the data-transmission rate of 9 Gbit/s has been reported recently [176].

22.4.5 Perspectives

RTD oscillators and detectors already have characteristics appropriate for some applications. However, the study of RTDs shows that there is much room for further development. Particularly, much higher output power and operating frequencies should be achievable with RTD oscillators, while much higher sensitivity should be within the reach of THz RTD detectors; thus RTDs evolve into an enabling technology for real-world THz applications.

22.5 Field-Effect Transistors

Even if the initial theoretical idea of Lillienfeld of building a transistor "for controlling electric currents" [177] was based on the unipolar field-effect concept, the field-effect transistor (FET) was not fabricated until 1952 by George

Clement Dacey and Ian Ross, at Bell Labs (in that case a JFET [178], with a PN junction as gate contact), some years after the bipolar junction transistor. The high input impedance of FETs (nowadays using gate electrodes based on metal oxide semiconductor junctions or Schottky contacts) makes them the privileged choice not only for digital circuits (based on Silicon) but also for high power systems (based on wide bandgap semiconductors such as gallium nitride or silicon carbide) and high frequency and low noise applications (based on III-V semiconductors), which will be our focus.

From one hand, in recent years the operation frequency of last generation FETs, called high electron mobility transistors (HEMTs) or Heterojunction FETs (HFETs), has well entered into the THz range. These transistors are based on different types of heterojunctions made with high mobility III-V semiconductors (mainly InP HEMTs with InGaAs/InAs composite channel) and with gate lengths shorter than 50 nm. After the first THz transistor fabricated at Northrop Grumman in 2007 [179], the THz HEMTs technology has also been developed at Fraunhofer [180], and more recently at Fujitsu [181] and it is now allowing the development of terahertz monolithic integrated circuits (TMICs) [182], for example, low noise amplifiers above 600 GHz [183], 850 GHz front ends for transmitter and receivers [184], the first circuit able to amplify signals above 1 THz [185].

On the other hand, MOSFETs based on III-V compounds are also envisaged as alternates to the Si CMOS technology for digital circuits in order to become the key for continuing Moore's law [186].

These important milestones have been reached by means of important technological efforts and by applying the traditional scaling rules, but also by focusing on the reduction of the parasitic effects (mainly the cross-talk contributions of the contact accesses to the gate-source capacitance C_{gs} and gate-drain capacitance C_{gd}), since the intrinsic limit of the cutoff frequencies of 100 nm-gate HEMTs is already within the THz range, as indicated by Monte Carlo simulations [187]. Indeed, the physical modelling of HEMTs has allowed the advance of the technology by avoiding the expensive trial and error approach when testing new architectures (as double gate transistors [188]), novel materials [189] or noise performances [190].

22.5.1 Frequency Limitations of FETs

Apart from the "classical" operation as amplifiers and digital switches, since recently, FETs are also being exploited as THz detectors at frequencies well above their typical cutoff frequencies f_T and f_{MAX}. In fact, by definition, these cutoff frequencies indicate the limit of operation of transistors as amplifiers (used as a 2-ports circuit) under different loads. f_T is related to the cutoff of the power gain with short-circuited output, and f_{MAX} to the cutoff of the maximum available gain, thus providing the maximum frequency of oscillation of a circuit using a transistor embedded into an optimum external passive feedback network.

In the last generation of THz FETs, the values of f_T and f_{MAX} are not only limited by the intrinsic gate capacitances but also by parasitic effects (mainly contact resistances and pad capacitances). On the other hand, when using FETs as THz detectors , the operating conditions are completely different (as well explained in Ref. [191]) with respect to their operation as amplifiers or oscillators, since they act as a one-port circuit, with just one AC input (RF or THz). Therefore, two possible approaches can be taken, whether superimposing an AC signal to the DC bias (i) at the drain (drain coupling conditions, DCC), or (ii) at the gate (gate coupling conditions, GCC), with source grounded in both cases.

Under DCC the gate contact is not used as an input port, but just to bias the devices. The output signal is commonly the DC drain voltage, measured in an open circuit, as shown in the large signal equivalent circuit of Fig. 22.16. The key point of that circuit is the nonlinear dependence of the drain current I_{D0} vs. drain voltage (i.e. the DC $I_D - V_{DS}$ curves), which provides a non-zero V_{out} when an AC signal is applied to the drain contact.

While in two-port configuration, the frequency limit of FETs is given by the total gate capacitance (the sum of C_{gs} and C_{gd}), when used as one-port detectors, the cutoff frequency is higher, since only one of the capacitances, C_{gs} or C_{gd}, is effective. Under DCC operation C_{gd} is the key, since the gate is AC grounded, so that C_{gs} is short-circuited and the influence of the gate resistance is null. Conversely, only C_{gs} is of importance for determining the limit frequency for signal detection in GCC. Interestingly, RF detection in GCC can only be performed above a certain frequency, when gate and drain can be considered as an AC short circuited (i.e. $1/(\omega C_{gd}) \rightarrow 0$), since an output signal can only be obtained when an AC drain voltage is applied.

The initial demonstrations of THz detection by means of FETs were made using commercial GaAs HEMTs fabricated by Fujitsu [192–194], and laboratory prototypes of HEMTs on different material systems: GaAs [195], GaN [193] and InP [196], but also with Si MOSFETs [197], all of them fabricated following the "classic" design rules for optimising their operation as amplifiers. The theoretical background for the THz detection was based on the plasma wave theory by Dyakonov–Shur [198, 199], so that FETs used for THz detection have been imprecisely labelled as "plasma-wave detectors ". Even if such theory has been the engine for the

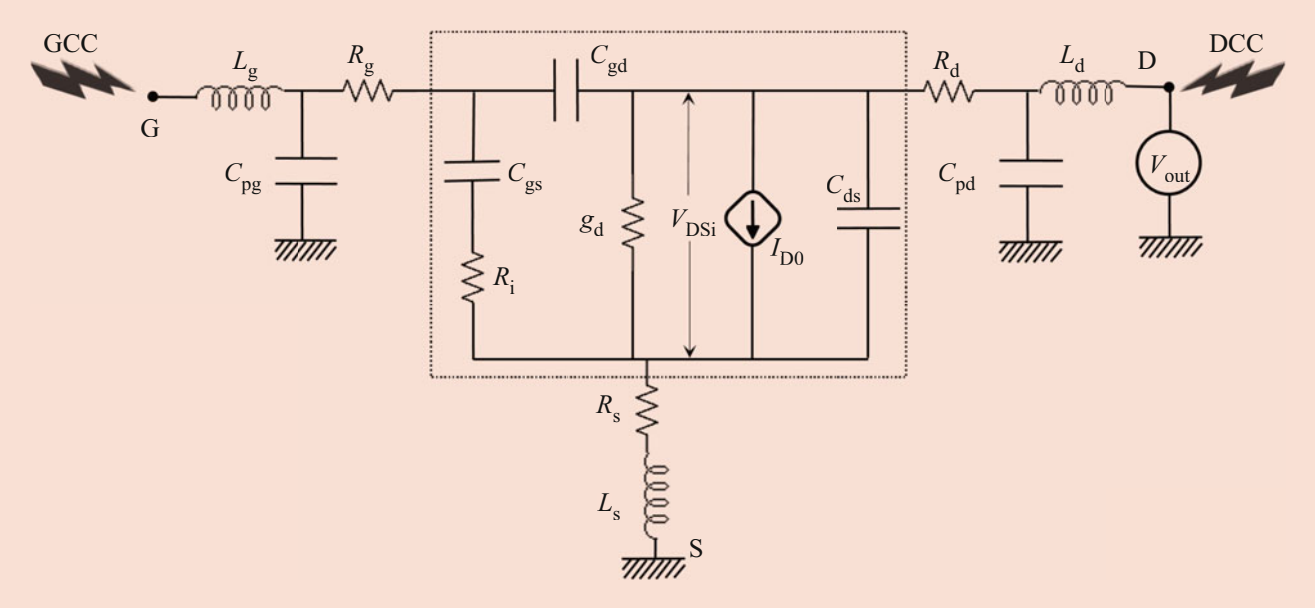

Fig. 22.16 Large signal FET equivalent circuit indicating the operation as RF detector in both DCC and GCC configurations. The intrinsic part of the transistor is enclosed in the dashed rectangle

fabrication of novel architectures of plasma-wave THz detectors [200, 201], like the asymmetrically interdigitated dual-grating gate (DGG) structures [202], a weak experimental support [194–196] of the resonant detection predicted in those seminal papers has been obtained, probably due to the too ideal assumptions about the device behavior introduced by the theory [203, 204]. Moreover, instead of the enhanced responsivity with frequency predicted by plasma-wave theory, a frequency roll off is found in experiments, which can well be interpreted in terms of a parasitic capacitance [205] or an increase of the effective resonant cavity due to cap layers [206].

The absence of a consensus about the plasma-wave origin of the experimental results has led to the search of other approaches, as the pseudo-two-dimensional hydrodynamic model [207] and the one presented in [191], using the well-established lumped element modelling of the transistors by means of the equivalent circuit of Fig. 22.16. This latter model is able to correctly explain the results obtained in graphene FETs up to 67 GHz and has been helpful for the optimisation of the design of the detectors. However, such quasi-static analysis and the lumped element model presented in [191] is valid only for low frequencies (<100 GHz); for higher frequencies the consideration of distributed elements is necessary [208]. It is also important to notice that this resistive self-mixing (rectification given by the nonlinearity of the $I_D - V_{DS}$ curves) can be further enhanced by resonant plasma waves at THz frequencies, but only to a very limited extent (much lower than expected by the Dyakonov–Shur theory) due to the high-frequency dependence of the channel impedance [209], not considered in the ideal plasma-wave models [198, 199].

22.5.2 FETs as THz Detector

Taking advantage of the better understanding of the FET detection mechanisms and making use of circuit models, the fabrication of THz detectors with FETs (TeraFETs) with specific designs (and often with integrated antennas for an improved free-space coupling) has been achieved recently. The concept of a heterodyne detector , based on the mixing of a beating photoexcitation and the incoming THz radiation, has also been proposed and theoretically studied [210].

Figure 22.17 reports a summary of the performances, both in terms of responsivity and noise equivalent power (NEP) for different technologies of TeraFETs. Apparently the best results are obtained with asymmetric DGG on InGaAs [211], reaching a NEP as low as 0.48 pW/Hz$^{1/2}$ @292 GHz. However, these results have been obtained after a normalisation of the input power taking into account the beam and the device area (results shown with dashed lines in Fig. 22.17). When the total optical power is considered, the results for those devices are modest when compared with the rest of technologies. Also, by using an amplifier at the output of a CMOS-based detector [208], the responsivity can be boosted, but the NEP (which is the important figure of merit) is significantly degraded. Figure 22.17 reports the available results for commercial GaAs Schottky-barrier diodes (SBDs).

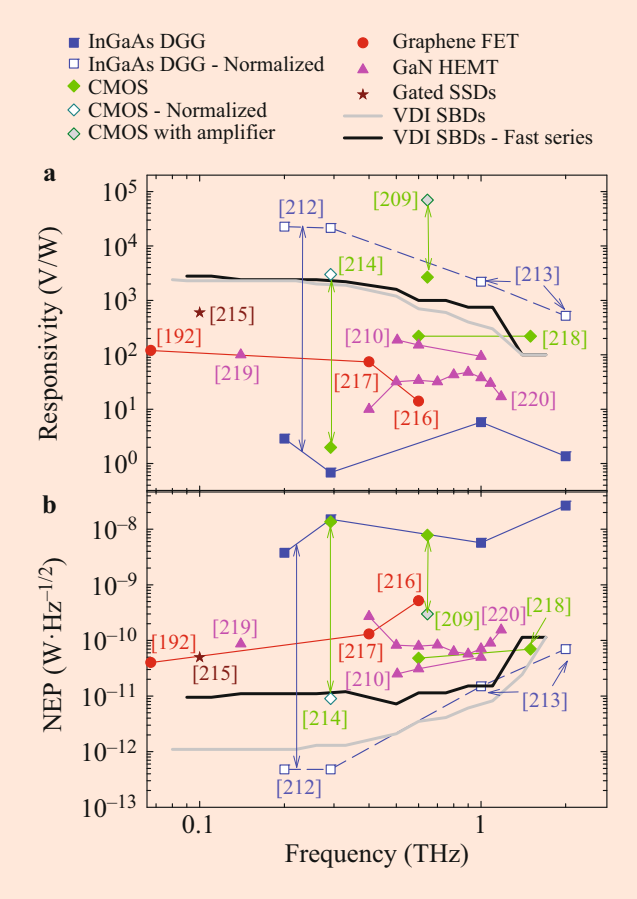

Fig. 22.17 (**a**) Responsivity and (**b**) NEP of different technologies of FET-based THz detectors found in the literature. Normalised values (using the detector and beam sizes) are shown with open symbols, and the corresponding raw values (connected with arrows) have been estimated. For comparison, the performances of commercial VDI THz detectors based on GaAs SBDs are also shown

It can be observed that, apart from the artificially normalised results of [211–213], no FET-based detectors have been able to obtain better results than SBD-based detectors. This is due to the fact that the nonlinearity of the SBDs is always higher than that of FETs (it is only approached near pinch off [214]). Not even graphene FETs, in spite of the promising characteristics of this material, are able to outdo the performances of SBDs [191, 215, 216]. Only at high frequencies (above 1.5 THz), 90 nm Si-CMOS [217] devices with integrated antennas and designed for improved impedance matching are able to compete due to the frequency roll-off suffered by SBDs. On the other hand, even if GaN does not seem to be the optimum choice for THz applications due to its much lower mobility, HEMTs with integrated antennas [218, 219] provide unexpectedly good performances as THz detectors. Also, exotic FETs based on GaN nonlinear asymmetric nanodiodes (gated self-switching diodes, G-SSDs) have also exhibited good THz response [214, 220].

These results, summarised in Fig. 22.17, seem to indicate that, presently, the technological maturity and a good design in order to correctly exploit plasmonic effects are the most important points for achieving good THz performances.

22.5.3 FETs as THz Emitters

THz emission by FETs has also been reported in the literature and interpreted in terms of the Dyakonov–Shur theory [198, 199] as the amplification of plasma waves upon reflection at the borders of the channel when appropriate bias and boundary conditions are fulfilled. As in the case of detection, emission takes place at frequencies beyond the typical cutoff frequencies of the transistors. Voltage-tunable emission, appearing in a threshold-like manner, has been observed in both InGaAs/InAlAs [221] and GaN/AlGaN transistors [222]. Plasmon-resonant terahertz emission has also been achieved by optically pumping an InGaP/InGaAs/GaAs HEMT incorporating DGG structures and a vertical cavity [223] or an AlGaAs/InGaAs/InP HEMT [224, 225]. Recently, emission from dedicated AlGaN/GaN high-electron-mobility transistors (multifinger and integrating antenna structures) has been measured, but it could not be attributed to plasmonic instability phenomena [226].

22.5.4 Perspectives

Due to the recent application of FETs to the field of THz detection and emission, there is still a lot of room for improvement of their performances. Indeed, up to now, apart from the integration of antennae or simple circuit elements (such as capacitors), the design of the devices has not been much modified with respect to that used for their classic operation as amplifiers. Most of the recent efforts made for optimising the performance of FETs acting as detectors have been made on GaN- and graphene-based devices, with promising results. However, classic high-mobility semiconductors such as InGaAs or InAs could also be a good option for obtaining the best frequency performances (at least until high-mobility graphene can be steadily obtained). On the other hand, a better understanding of the influence of the plasma waves on the practical performances of FET-based THz detectors and their possible use for the fabrication of emitters must be achieved by means of realistic modelling techniques accounting for all the complexities of the real devices (mainly parasitics and power losses).

22.6 Heterojunction Bipolar Transistors

A heterojunction bipolar transistor (HBT) is a bipolar transistor where the emitter-base junction (EBJ) is a heterojunction allowing an optimisation of the doping of the base and emitter layers to perform higher frequency operation.

22.6.1 Physics of the Heterojunction Bipolar Transistor

The PN Junction

Only NPN HBTs are addressed. Without detailing the physics of the PN junction which is a key element of microelectronics, we are interested in its dynamic behaviour. At high frequency, the electrical equivalent circuit of the junction, shown in Fig. 22.18 for forward biases, is such that, for reverse biases, the junction conductance G_d becomes very small and only the depletion part, C_T, of the capacitance remains. The resistance R and the self-inductance L in series account for anode and cathode accesses including the metal contact and the quasi-neutral region (QNR), with voltage drop and inductive effect.

The capacitance C_d results from the diffusion of minority carriers. It reproduces the ability of minority carriers to follow the electrical modulation. For a long diode, the cutoff frequency depends on recombination mechanisms of minority carriers, but this is less true for HBTs where the base thickness is small in comparison with the diffusion length. Parasitic capacitances around the junction contribute to the cutoff frequency, with an increasing importance for small junction area.

Such a circuit is valid for low and high frequencies but is questionable for sub-millimetre waves and THz frequency regimes. Beyond 300 GHz, the circuit should include elements to account for the non-stationary behaviour of carriers transport. If there is no publication on PN junction modelling at THz frequency, we can take a look at forward biased SBD: in these diodes, the transport only involves majority carriers. Even if the transport of minority and majority carriers is different between an abrupt PN junction and a Schottky junction, similar mechanisms can be converted with RLC cells in series (Fig. 22.19) able to reproduce inertial effects along the junction. Index d, N and N^+ are associated with depletion region below the anode metallisation, undepleted N region and heavily doped N^+ region for low resistivity cathode contact. The Schottky model in the THz frequency range may suggest the improvement of Fig. 22.18 model of the PN junction in the THz domain.

The Bipolar Transistor

Figure 22.20a shows the NPN bipolar junction transistor (BJT) built with two back-to-back PN junctions where the same P-type region is thin enough with regard to the electron/minority carrier diffusion length. In normal operation, emitter-base junction (EBJ) is forward biased, while collector-base junction (CBJ) is reverse biased.

The forward voltage V_{BE} allows to inject electrons from the emitter to the base (I_{nE}), as illustrated in Fig. 22.20b, and reciprocally holes towards the emitter (I_{pE}). The reverse voltage V_{BC} generates an electric field to collect electrons that diffuse through the base (I_{nC}), but this field lets few holes to diffuse from the collector to the base (I_{pC}) with an almost negligible intensity. Recombination mechanisms in each region, I_{RN} in the base QNR, I_{RE} in the EB Space Charge Region (SCR) and I_{RC} in the CB SCR, contribute to the holes current of the base (I_{pB}). When the electric field is high enough in the CB SCR, impact ionisation occurs, leading to I_{CBII}. Recombination current occurs in the volume as well as at the surface and interface of the transistor.

Without I_{CBII}, net values of the current at each terminal are: $I_B = I_{pE} + (I_{RE} + I_{RN} + I_{RC}) + I_{PC}$, $I_E = I_{nE} + I_{pE}$ and $I_C = I_E - I_B$. The injection efficiency factor, an important parameter for the NPN BJT, can be written as

$$\gamma = \frac{I_{nE}}{I_E} = \frac{I_{nE}}{I_{nE} + I_{pE}} = \frac{N_D W_E D_{nB}}{N_D W_E D_{rB} + N_A W_B D_{pE}} \quad (22.18)$$

where N_A and N_D are the P-type doping level in the base and the N-type doping level in the emitter, respectively, W_B and W_E are the thickness, and D_{nB} and D_{pE} are the diffusion coefficients of minority carriers in their respective regions. A high current gain (I_C/I_B) needs γ as close as possible to 1. The relative value of each parameter requires to moderate the BJT's base doping level. This leads to a high base resistance which affects dynamic performances.

Figure 22.21 shows the small-signal equivalent circuit used here to discuss important parameters involved in high-frequency figures of merit, where parasitic capacitances and distribution effects are removed. In common emitter, the transconductance g_m and the dynamic resistance R_π are

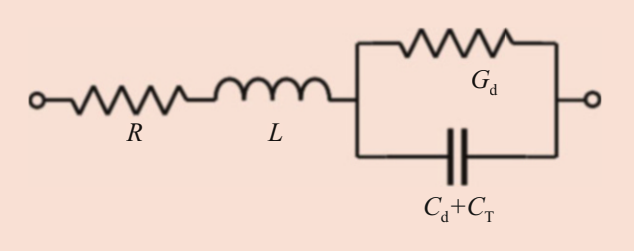

Fig. 22.18 Small-signal equivalent circuit of the PN homojunction (forward biased)

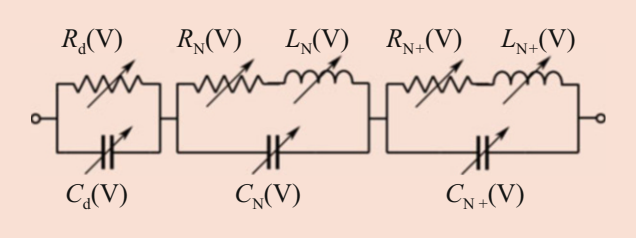

Fig. 22.19 Direct small-signal equivalent circuit of a Schottky diode at 1 THz including inertial effects

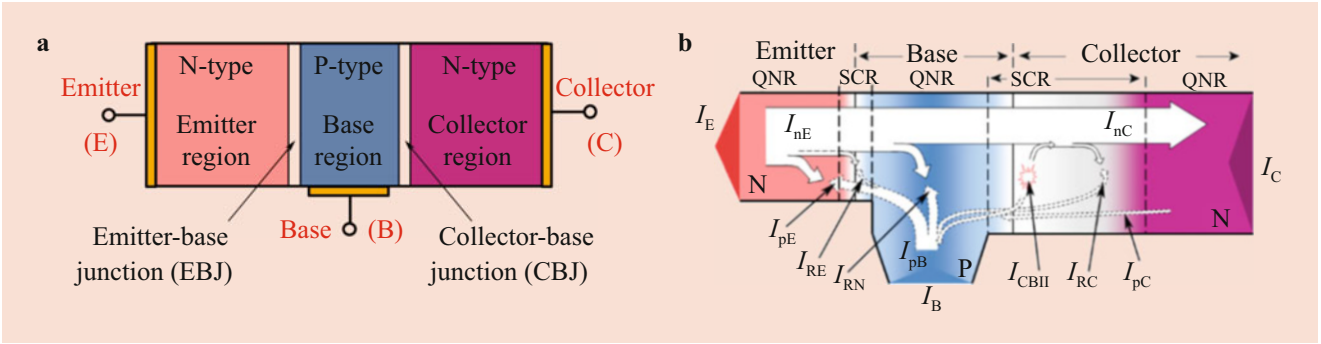

Fig. 22.20 (**a**) Schematic representation of the NPN transistor with emitter, base and collector terminals, and (**b**) sketch of different electron (I_n) and hole (I_p) current components (the size of the arrows highlights the magnitude of the current)

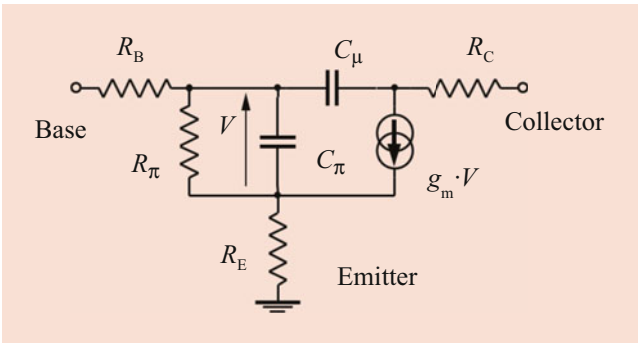

Fig. 22.21 Simplified small-signal equivalent circuit of the bipolar transistor (Π-topology)

$$g_m = \frac{qI_c}{k_B T} \quad \text{and} \quad R_\pi = \frac{k_B T}{qI_B} \tag{22.19}$$

where q, k_B and T are, respectively, the elementary charge, the Boltzmann constant and the device temperature. Intrinsic capacitance and access resistance complete this circuit.

The high values of the transition frequency where a gain crosses 0 dB are often extracted at lower frequencies corresponding to the measurement range of the network analyser (taking into consideration a –20 dB/dec frequency dependence of the gain). The transition frequency f_T of the current gain can be written as

$$f_T = \frac{g_m}{2\pi \left(C_\pi + C_\mu \left(1 + g_m \left(R_B + R_C\right)\right)\right)} \tag{22.20}$$

Among the different power gains, the invariant and unilateral gain of Mason U and its transition frequency can give the maximum oscillation frequency f_{max}, as

$$f_{max} \approx \frac{1}{4\pi} \sqrt{\frac{g_m}{R_B C_\mu \left(C_\pi + C_\mu \left(1 + g_m \left(R_B + R_c\right)\right)\right)}} \tag{22.21}$$

High performances require high value of f_T and of f_{max}. It is impossible for a BJT to build a thin and highly doped base layer leading to a low value of R_B (required for a high f_{max}) without degrading γ and inducing a lower value of g_m. A low value of R_B can be obtained with a thicker, lower doped base layer, but this leads to a higher value of C_π that affects f_T. Also a low doping level of the base reduces the current threshold of the limiting base punch-through and induces a detrimental high early effect. Such a limit for the BJT highlights the effort that needs to be done for the base design to reach THz transition frequencies.

The Heterojunction Bipolar Transistor (HBT)

In order to build a thin highly doped base layer without reducing the injection efficiency, EBJ is made with a heterojunction with a higher band gap for the emitter than for the base. Equation (22.18) can be derived as

$$I_{pE} = \frac{J_{nE}}{J_{pE}} = \left[1 + \frac{1 + \frac{D_{nB}}{S_{nE} W_B}}{1 + \frac{S_{nE} W_B}{S_{pE} W_E}} \frac{n_E^2 D_{pE} N_{AB}}{n_B^2 D_{nB} N_{DE}} \frac{W_B}{W'_E}\right]^{-1} \tag{22.22}$$

where n_{iB} and n_{iE} are the carriers' intrinsic densities of each region, and their ratio benefits from the difference of band gap ΔE_G:

$$\left.\frac{n_{iE}^2}{n_{iB}^2}\right|_{HBT} \approx \left.\frac{n_{iE}^2}{n_{iB}^2}\right|_{BJT} \times \exp\left(\frac{\Delta E_G}{k_B T}\right) \tag{22.23}$$

In the case of InP/InGaAs HBT, the ratio n_{iE}^2/n_{iB}^2 is about 10^{-10}, enabling a wide range of doping levels. With a lower doping level of the emitter near the EBJ, the transition capacitance can be lower. A high doping level of the base is possible, reducing all drawbacks already discussed for the BJT, and also limiting current-crowding effect.

Due to negligible value of I_{pE} in III-V HBT, the base current, I_{RN}, is mainly due to recombination among which mostly Auger effect dominates, which leads to a moderate current gain. The smaller Auger effect in Si/SiGe HBT (in

comparison to InP HBT) does not control the base current, and then the current gain can reach very high values.

High values of f_T and f_{max} need a high electron mobility in the highly doped base as well as a high current density. Moreover, at high-currents, the Kirk effect affects the transition frequency [227]. This is due to the spreading of the neutral base layer into the collector region of the device. The base layer spreading mechanism derives from an analysis of the effect of the current-dependent buildup of the mobile-carrier space-charge density in the collector transition layer. For a single heterojunction bipolar transistor (SHBT), the threshold current density associated with the Kirk effect is

$$J_K = qv_{sat}\left(N_{DC} + \frac{2\varepsilon_s\left(V_{CB} + V_{bi}\right)}{qW_c^2}\right) \tag{22.24}$$

where V_{CB} is the applied collector base voltage, V_{bi} the built-in voltage and W_C, the thickness of the collector layer of doping N_{DC}. One can conclude that the threshold of the Kirk effect is controlled by the collector doping and the collector thickness. The Kirk effect is a key physical mechanism in the modern HBT optimisation because the reduction of the whole delays across the device imposes the highest current density such as 15–25 mA/μm^2 at maximum f_T/f_{MAX} for InP HBTs and up to 34.4 mA/μm^2 for the highest f_T/f_{MAX} SiGe HBTs reported in 2016.

Some drawback effects also occur in THz HBT, limiting the performances such as the self-heating effect or impact ionisation. Some other mechanisms have to be taken into account in details for further performance improvement such as band gap narrowing (BGN) [228], minority transport properties in the heavily doped base [229] or the Kirk effect [227]. Let's focus on self-heating and breakdown voltage. Very high current densities of 15–30 mA/μm^2 are reached with relatively small area of EBJ and CBJ, whose EBJ is 100–200 nm wide, and few μm long. Self-heating becomes important and contributes to limiting dynamic performance because carrier transport properties are degraded with increasing temperature. SiGe HBTs can benefit from a better thermal conductivity of the Si substrate (κ_{Si} = 148 W/K/m) than for GaAs (κ_{GaAs} = 46 W/K/m) or InP (κ_{InP} = 68 W/K/m). Metallic levels have a higher contribution to thermal dissipation in III-V compounds, with wider contacts closer to the heat source and less interconnect levels than in BiCMOS. The size of the chip and the thickness of the substrate are crucial parameters as well as the spreading of the heat source in separated emitters. Mesa structure and trench isolation increase the thermal resistance, but substrate thinning, metallic through-wafer vias and the transfer of the initial substrate to a higher conductivity material such as SiC or diamond are proposed to reduce self-heating. The breakdown voltage also limits performances due to impact ionisation (II). For II, a large electric field across the collector depletion region induces hot electrons able to generate electron-hole pairs. The BV_{CEO} breakdown voltage is current gain dependent, in favour to larger values for III-V HBTs with lower current gains than for SiGe HBTs [230].

Complete Small-Signal Equivalent Circuit

Figure 22.22 shows the complete small-signal equivalent circuit where the CBJ capacitance is distributed in two parts to account for the base resistance repartition with a wider CBJ under the EBJ. Extrinsic capacitances and inductances are also included as well as intrinsic CB and output resistance. The transconductance g_m also brings an extra high-frequency delay τ_{hf} specific for the Π-topology circuit, but not included in charging and transit times.

In addition to the first simplified circuit, the high-frequency performance can be described with transit times and delay between the emitter and the collector, τ_{EC}, extracted from f_T: $\tau_{EC} = (2\pi f_T)^{-1}$. τ_{EC} sums up charging times and transit time along the structure

$$\tau_{EC} = g_m^{-1}\left(C_\pi + C_{be}\right) + \left(g_m^{-1} + R_E + R_C\right)\left(C_\mu + C_{bc}\right) + \tau_E + \tau_B + \tau_C \tag{22.25}$$

where C_{be} and C_{bc} are the extrinsic capacitances of the transistor between B/E and B/C.

The advantage brought by the band gap difference for EBJ for the injection efficiency contributes to reduce the emitter transit time τ_E. A simplified relation for the diffusion of holes in the emitter is

$$\tau_E \approx \frac{W_E^2}{2D_{pE}}\frac{G_B}{G_E}\exp\left(-\frac{\Delta E_G}{k_B T}\right) \tag{22.26}$$

where G_B and G_E are base and emitter Gummel numbers [230]. The base transit time depends on the fraction of electrons in diffusion $\tau_B = W_B^2/(\eta_B D_{nB})$ relaxed in the

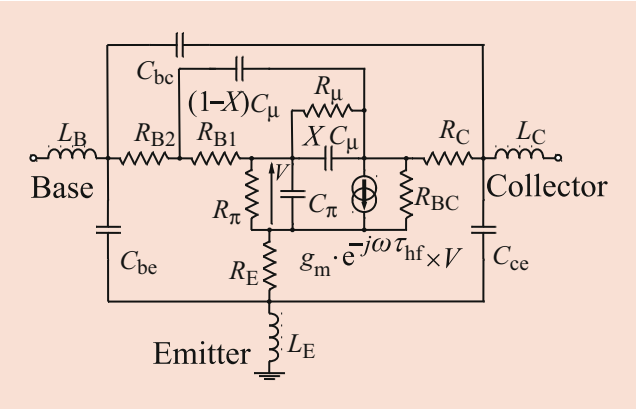

Fig. 22.22 Complete small-signal equivalent circuit of the bipolar transistor (Π-topology)

conduction band, and electrons with few interactions, in non-stationary regime at velocity v_B: $\tau_B = W_B/v_B$ (v_B can be higher than saturation velocity, v_{SAT}). The collector transit time is $\tau_C = W_C/(\eta_C\, v_C)$ where W_C and v_C are, respectively, the thickness of the CBJ SCR and the collector velocity ($v_C \approx v_{SAT}$). The factor η_C accounts for the collector transport specific case and is equal to 2 when electrons reach rapidly v_{SAT} with no overshoot velocity.

Reduction of the Total Emitter-Collector Transit Time τ_{EC} and the Base Resistance

Increasing f_T or decreasing τ_{EC} leads to an overall reduction of charging and transit times. Charging times can be reduced by lowering the access resistance, by increasing doping level at vicinity of wider Ohmic contact and thinning QNR. The improvement of the contact resistance between the semiconductor and the metal of the electrodes requires the use of suitable metal alloys. The EBJ dynamic resistance is a reverse function of the I_C collector current, and the maximum of f_T is obtained for a high I_C value. This current value indicates the end of "normal" operation of the transistor with the progressive occurrence of the Kirk effect. Thus, pushing back the Kirk effect by increasing the collector doping while reducing its thickness allows to increase the limit of the collector current density and thus the maximum value of f_T. However the impact ionisation threshold is lowered and the collector capacitance can increase.

One can try to decrease the depletion capacitances by decreasing the surface of the junctions, in particular the dissymmetry between EBJ and CBJ. These capacitances can also be reduced by decreasing the doping level in SCR or by acting on the doping profile. The electrostatic extrinsic capacitances should not be underestimated.

The emitter transit time related to the diffusion of charges from the base to the emitter can be reduced by increasing the energy barrier height of the EBJ heterojunction. A small base thickness, a band gap gradient and injection of "hot" carriers from the emitter will promote a low transit time in the base. Finally, the reduced thickness of the moderately doped collector will allow a shorter collector transit time.

All this requires a tradeoff because, for example, the increase of collector doping favourable to the decrease of the EBJ dynamic resistance (collector current—Kirk effect) also leads to an increase of the depletion capacitance. Breakdown voltage is also seriously affected, and the increase of self-heating due to the increase of the current density causes a temperature rise that degrades transport properties thus inducing higher transit times.

For the base, the tradeoff concerns the value of the base resistance which must not be too high in order not to penalise f_{max}. The leverage margins are the increase in base doping level jointly with the reduction of the EBJ width and of the distance to the lateral base contact.

For silicon-based devices, with the increase of the doping levels, sometimes at the limit of solubility, the shrinking of the whole HBT dimensions is limited by the diffusion of species, in particular with respect to the overall thermal budget (activation annealing, compatibility with other devices using high temperature process). The band gap discontinuity height needed to compensate for the decrease in the difference of doping levels of EBJ must also be taken into account.

Performances and Limitations of HBTs

In comparison with III-V field-effect transistors (FETs), III-V HBTs are volume devices with higher transconductance and current density, exhibiting uniform "threshold" voltage controlled by built-in voltage and less restrictive for lithography. However they require complex and expensive epitaxy. It appears easier to better control the thickness of the intrinsic base through epitaxy than the gate length of a tenth of nanometre through lithography. High transport properties of III-V material follow to be attractive for state-of-the-art HBT based on an ultra-thin and highly doped base. Such material open opportunities for the THz frequency range. Concerning SiGe HBT, the cutoff frequencies of the best RF-CMOS processes come close to those of SiGe HBTs, but at the expense of a significantly more advanced lithography, typically at least three lithography nodes [231].

The output conductance g_d of the HBT is low, and then the ratio g_m/g_d is very high (above 200). HBT are far less sensitive to capacitance parasitics associated with interconnections than FET for devices exhibiting the same f_T because the intrinsic capacitances are higher in the bipolar transistor. For instance, after a de-embedding step, the f_T value of HBT is closer to the raw f_T [231].

The output power can also be increased with device size. While it increases the device-related capacitances in both HBTs and MOSFETs, an increase in emitter length alone reduces all resistances in series in HBTs but a corresponding increase of the FET gate width leads to a larger gate resistance [231].

The flicker noise ($1/f$ noise) in III-V HBT, and thus the phase noise of the oscillator, can be lower than in FET-based circuits. SiGe HBTs also have much lower corner frequencies than MOSFETs, in which $1/f$ noise keeps increasing for more advanced nodes. HBT may show low HF noise despite the base current. Overall, HBTs appear to have a distinctive advantage in the area of mm-wave and THz amplifiers from a technical circuit design perspective [231].

22.6.2 Different Technologies of Heterojunction Bipolar Transistors

III-V HBTs

THz III-V HBTs commonly consist of an InGaAs base layer, featuring a single heterojunction at EBJ (SHBT) with an

InP emitter or consists of a double heterojunction (DHBT) with InP collector, or, alternatively, of a GaAsSb base layer between InP emitter and collector. The first HBTs have used AlGaAs/GaAs and GaInP/GaAs emitter heterojunctions. With AlGaAs/GaAs it is possible to reach high f_{max} (216 GHz [232]). The HF figure of merit of GaInP/GaAs was small but the HBT exhibits high linearity and low turn-on voltage. Nevertheless GaAs HBTs suffer from various drawbacks such as high self-heating, electron transfer in L Valley in the base and dramatic surface recombination. Therefore GaAs-based HBTs seem to be not good candidates for THz applications.

Most III-V HBTs are triple-mesa devices, with one layer built on top of the other with a pyramid shape: the upper layer always acts as a mask for the one below; therefore it is a self-aligned process. The emitter and the base-collector mesas form the transistor, while the third mesa is etched down to a semi-insulating substrate to provide isolation of devices. The transistor structure is designed emitter-up, since this layer sequence greatly simplifies the fabrication of the transistors for high-speed applications [233].

Figure 22.23 shows the drawing of such an HBT bordered by metallic contacts around the narrow EBJ and CBJ. The emitter under-cut reduces the extrinsic base resistance by reducing the space between the base metallisation and the active zone, while the base under-cut reduces the collector resistance and the CBJ capacitance (the $(1 - X)C_{\mu}$ part in Fig. 22.22).

One alternative to base under-cut is a collector up device. Then f_{max} can increase significantly up to 1.15 THz, as obtained in 2001 nearly 20 years ago [234], but it can require transferred-substrate process which is not compatible with MMIC technologies.

Some of the highest f_T and f_{max} figure of merit are represented in Fig. 22.24 for the two III-V HBTs and SiGe HBT discussed later.

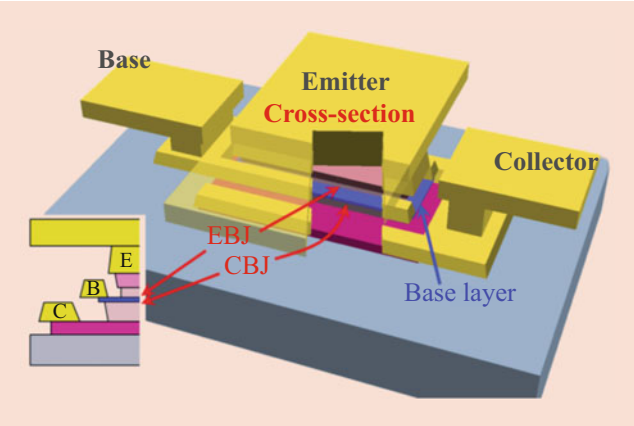

Fig. 22.23 Drawing of the HBT with metallic contact around the mesa, with a cross-section underlining the location of the EBJ over and CBJ under the base layer in blue

InP/InGaAs HBT InP-based HBTs realise an excellent tradeoff between a high output power, high f_T and f_{max} values and low noise. They are also fully compatible with 1.55 µm telecom wavelength systems technology.

The first InP HBTs were based on InP/InGaAs and AlInAs/InGaAs emitter heterojunction. State-of-the-art f_T and f_{max} were obtained with single heterojunction and double heterojunction. Figure 22.25 shows the layer stack and bands profile of an InP/InGaAs DHBT.

InP HBT exhibit some advantages when compared with GaAs ones: (i) better transport properties of electrons in InGaAs than in GaAs. (ii) $\Delta E_V = 0.37$ eV at the InP/InGaAs interface which is higher than in AlGaAs/GaAs heterojunction, while $\Delta E_C = 0.24$ eV. Such a low conduction band discontinuity leads to a low threshold voltage, but it is enough to boost the energy of injected electrons and reduce the base transit time. (iii) Surface recombination velocity is slower in $In_{0.53}Ga_{0.47}As$ than in GaAs (that is in favour of size reduction). (iv) Better thermal conductivity of InP substrate than in GaAs even if the $In_{0.53}Ga_{0.47}As$ thermal conductivity is 10 times smaller than the GaAs one. Chemical etching selectivity between InP and InGaAs is far better than between AlGaAs and GaAs and close to selectivity between GaInP and GaAs.

The breakdown voltage is very low in SHBT (with InGaAs collector layer). DHBT using InP emitter and collector regions are preferred due to the higher breakdown voltage provided by the wider band gap InP collector, even if it requires a complex quaternary alloy epilayers stack. However, current blocking effects can be observed at the CBJ due to ΔE_C. A proper base-collector gradual design is critical to avoid current blocking and to enable high current density operation. High-performance DHBTs have been realised with both InGaAs and GaAsSb base layers.

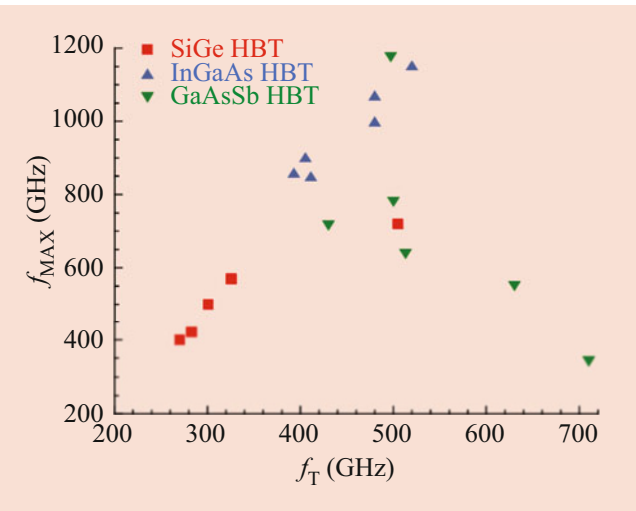

Fig. 22.24 Figure of merit f_{max} vs f_T for highest reported performances for SiGe, InGaAs and GaAsSb HBT [231, 235, 236]

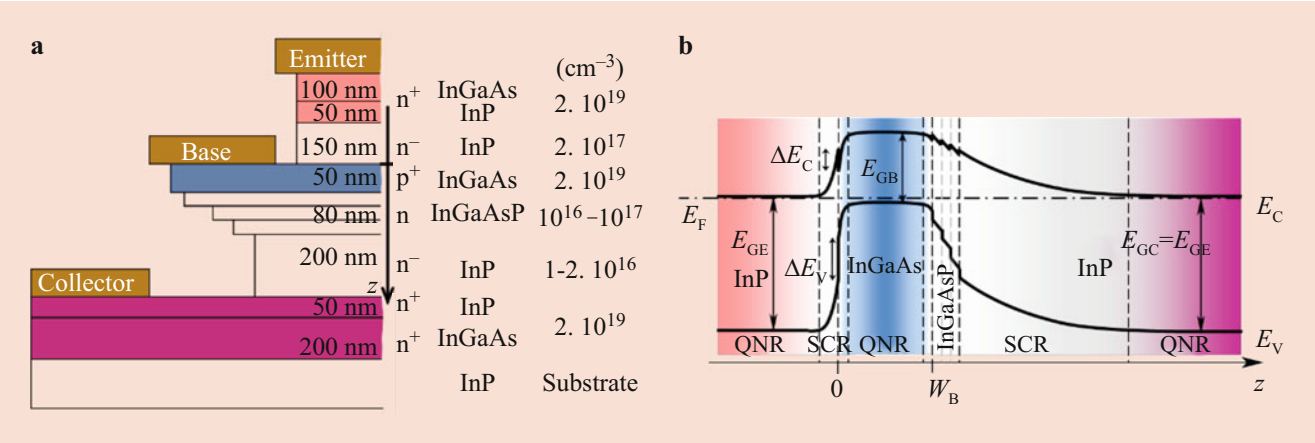

Fig. 22.25 (**a**) Layer stack and (**b**) bands profile of an InP/InGaAs HBT [237]

In state-of-the-art, InP/InGaAs HBT the base-collector region consists of a chirped superlattice of InAlAs/InGaAs layers with a linear varying composition followed by a pulse doping layer to compensate for the induced quasi-electric field [235].

The improvement of InP HBT technologies involves an increase of f_T and a steadily decrease of transit times thanks to the reduction of the base thickness. To a large extent, the improvement of f_T stems from the reduction of parasitics (capacitances and resistors) allowed by the self-alignment, by the reduction of EBJ area and by the increase of the Kirk effect threshold.

For THz devices, the base thickness is typically smaller than 30 nm, and base doping levels are made as high as possible to minimise layer and Ohmic contact resistances, while reducing the lateral spacing between EBJ and extrinsic base contact. P-doping levels greater than 8×10^{-19} cm^{-3} are routinely realised using a carbon doping source in both InGaAs and GaAsSb devices. Typical base sheet resistance for scaled-InP HBT epitaxy is in the range of 500–1000 Ω/sq. Ohmic contact resistivities are critical to down-scaled HBT performance. Very low Ohmic contact resistivities based on proper surface preparation and contact selection have been reported to highly doped n-type and p-type InAs and InGaAs layers [235]. Contact resistivities of $0.2 - 1 \times 10^{-8}$ Ωcm^2 were obtained for molybdenum-based contacts to n-type InAs layers with 8.2×10^{19} cm^{-3} active carrier concentration in [235]. To avoid surface oxidation and contamination, contacts were deposited in situ in the MBE growth chamber immediately after epitaxy growth [237].

As it can be seen in Fig. 22.24, the highest performances for InGaAs HBTs are $f_T = 520$ GHz and $f_{max} > 1100$ GHz [237]. Breakdown voltages are about 3.5–4.5 V. Further improvement of HF figure of merit will be obtained by the ongoing shrinkage of the emitter width and contact resistivity lowering.

InP/GaAsSb HBT InP/GaAsSb DHBTs are developed as an alternative to InP/InGaAs DHBTs. For InP/InGaAs/InP and AlInAs/InGaAs/InP DHBTs, the main concern is the conduction band potential barrier between the InGaAs base and the InP collector [236].

The staggered band alignment at InP/GaAsSb heterojunctions enables the use of a simplified device structure with a pure InP collector layer. Pure InP collectors increase the junction symmetry and provide good thermal conductivity as well as high breakdown voltages. GaAsSb has an additional advantage: it can be easily p-doped with carbon to levels of 1×10^{20} cm^{-3}. However, hole mobilities in GaAsSb are lower than those of InGaAs, resulting in higher base sheet resistances at comparable thicknesses and doping levels [233].

Even though GaAsSb-based DHBTs eliminate electron blocking at the base-collector heterojunction, InGaAs-based DHBTs remain highly competitive. The use of InP/GaAsSb emitters leads to fast junction turn-ons with collector current ideality factors of $n_C = 1.0$, which cannot be attained in abrupt InP/InGaAs or AlInAs/InGaAs emitters. Since the ternary GaAsSb alloy is characterised by a lower electron mobility than its InGaAs counterpart, one must employ base grading quasi-electric fields to speed up electron transport across the base layer [236].

Among the values shown in Fig. 22.24, InP/GaAsSb DHBTs were demonstrated f_T / f_{max} of 503 / 780 GHz with a breakdown voltage of 5 V [238].

At present, the highest reported f_{max} is 882 or 1175 GHz depending on the extraction method used with measurement limited to 110 GHz [239], with W_E of 200 nm and BV_{CEO} of 4.1 V, while f_T has reached 710 GHz for a 250-nm GaAsSb DHBT, where the thin collector layer is realised by a gradual InGaAs compound and with a breakdown voltage of 1.75 V [240].

The InP/GaAsSb DHBT energy band diagram at equilibrium is shown in Fig. 22.26. It consists of an InP emitter, a

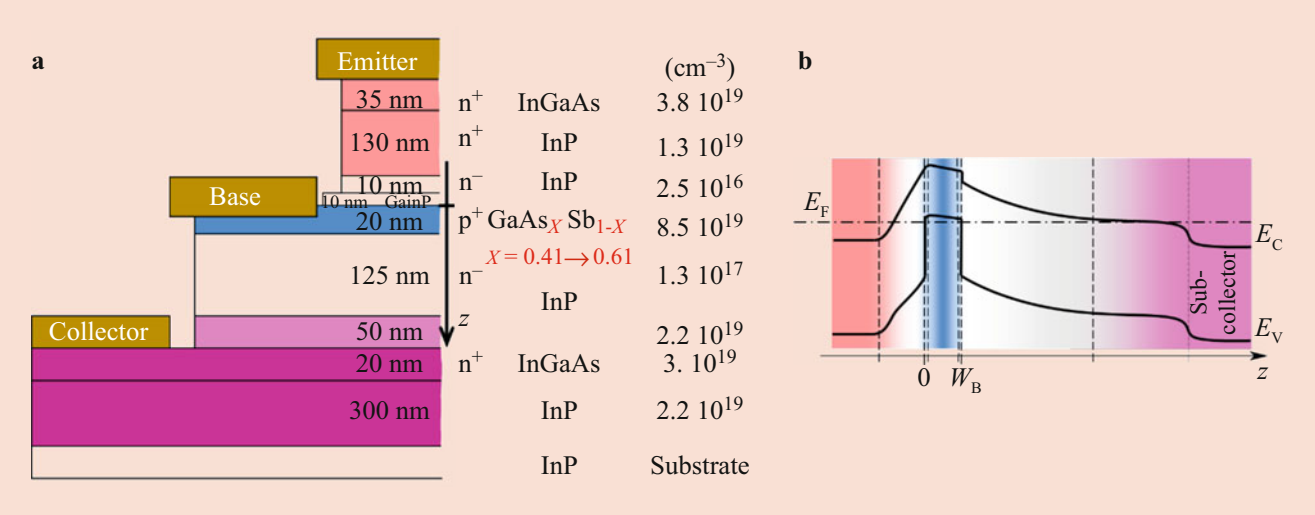

Fig. 22.26 (**a**) Layer stack and (**b**) bands profile of an InP/GaAsSb HBT [238]

$GaAs_xSb_{1-x}$ base and InP collector epitaxial layers [236]. The base layer has a non-constant composition. The purpose of the compositional grading is to generate an electron drift field and thus to reduce the base transit time. The base is built with an As fraction x linearly increasing from the collector to the emitter side and a doping grading N_B, from 0.41 to 0.61 and 4.5 to 9.2 $\times$ 10^{19} cm^{-3}, respectively, from CBJ to EBJ. Thus, the slope of the conduction band in the base creates an accelerating quasi-electric field that pushes electrons towards the collector. The higher doping at the base-emitter interface enables a low contact resistance and thus good base contacts.

The type-II InP/GaAsSb heterojunction between the emitter and the base layer results in conduction (ΔE_C) and valence (ΔE_V) bands discontinuities of 0.1 and 0.73 eV, respectively. To minimise electron blocking with ΔE_C, a thin gradual GaInP layer is added between GaAsSb base and InP emitter [233]. The edge of the conduction band of the $Ga_{0.22}In_{0.78}P$ emitter region is aligned to the conduction band of the $GaAs_{0.61}Sb_{0.39}$ base layer. The valence band edge at the heterojunction $Ga_{0.22}In_{0.78}P/GaAs_{0.61}Sb_{0.39}$ has a large offset which practically eliminates the injection of holes from the base into the emitter, and it enables very high base and low emitter doping levels. This allows to significantly reduced EBJ capacitance and base resistance. The InP collector provides a high breakdown voltage and therefore a high output power [236]. The low doped collector layer where the CBJ SCR can spread is followed by a highly doped sub-collector to provide good collector contact with low sheet resistance.

Further improvement of the device performance (in particular high-frequency figures-of-merit such as f_T and f_{max}) requires lateral and vertical scaling, together with an optimisation of the epitaxial layer design [236] like for InP/InGaAs device. Lateral scaling is beneficial to the reduction of charging times. Vertical profile scaling of the epitaxial base and the collector layers reduces transit times. Transistor scaling necessarily involves an optimisation of the device parasitics because they become progressively more significant with the decreasing size of the devices. The fabrication process and the epitaxial layer design must therefore be improved to broaden the transistor bandwidth [233]. In order to improve the figures of merit, some quaternary alloy, InGaAsSb, are investigated for the base [241] because the $\Gamma - L$ valley discontinuity can be higher in InGaAsSb than in GaAsSb and improvement of low field electron mobility at very high acceptor doping level could be observed like in GaAs or in InGaAs [229].

SiGe HBT SiGe HBT takes benefit from the high integration capabilities of silicon technology. This device is more recent than III-V transistors and band engineering take advantage of III-V HBT research. The core of the device is the SiGe base while the emitter and the collector use a silicon layer. Modern HBTs have a valence band discontinuity at EBJ with a moderate Ge content, and an internal electric field can exist when the Ge content increases gradually from EBJ to CBJ. Strain effects associated with carbon insertion in the base limit strongly the effect of boron diffusion even for doping as high as 5×10^{19} cm^{-3}. If the doping profile is limited by the thermal budget requested for CMOS compatibility, such SiGe HBTs are much more limited for enhancement towards THz figure of merit.

Figure 22.27 shows an HBT from STMicroelectronics with the effective EBJ width of about 100 nm. BiCMOS processes allows self-aligned architectures such as the double-polysilicon self-aligned (DPSA) using a selective epitaxial growth (SEG) of the base. The SEG of the base produce the boron-doped SiGe:C intrinsic layer and the link with the

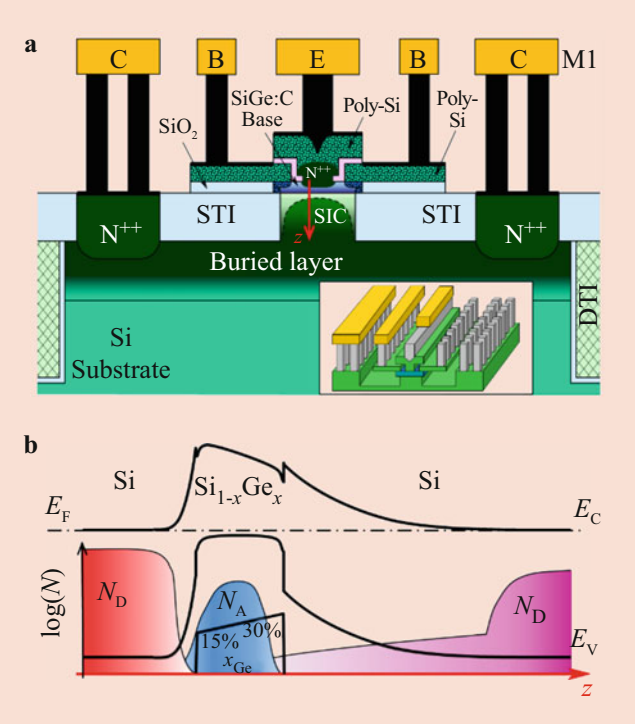

Fig. 22.27 (**a**) Schematic view in CBEBC configuration and (**b**) band and doping profiles of gradual base Si/SiGe HBT

boron-doped polysilicon (Poly-Si) of the base. The collector is built with a buried layer, an epitaxy, N^{++} collector sinker and shallow and deep trenches isolation (STI and DTI). It is used in production in the STM 55-nm BiCMOS technology with patterning capability that enables to reduce the difference between EBJ and CBJ area [236].

Doping, epitaxy layer growth and passivation steps are closely associated in silicon technologies leading to more compact devices than in III-V technologies. Here again, the increase of current densities and the reduction of extrinsic capacitances are crucial points to reach the THz domain. Above the heavily doped sub-collector, the low doped collector completed by the selectively implanted collector (SIC) allows to lower the $(1 - X)C_{\mu}$ and C_{bc} capacitance while maintaining a high Kirk effect threshold. STI reduces the collector capacitance. The process for the emitter with an epitaxial highly doped Si, the emitter poly-Si, and the thin spacer between the emitter and base poly-Si is used to reduce the emitter resistance R_E, the base resistance between the EBJ and the base poly-Si, and the parasitic collector capacitance.

Within the data displayed in Fig. 22.24, such HBTs exhibit f_T/f_{max} of 325/375 GHz with a breakdown voltage of 1.5 V [242] with an EBJ width of 100 nm. The main drawback of the DPSA HBT is the intrinsic to extrinsic base link (SEG to poly-Si) completely dependent of the SEG, restraining base resistance reduction. This can be overcome by replacing base poly-Si by sacrificial nitride, etched after the emitter formation and replaced by a well-controlled epitaxy of the extrinsic base [243].

Low temperature processing with millisecond annealing, with non-selective epitaxial base for optimised vertical doping profiles, self-alignment arrangement for EBJ and CBJ and later base link formation, in a small footprint BEC configuration, all together producing low resistances, capacitances and transit times, have led to half-THz f_{max}. The first results have shown values of f_T/f_{max} of 300/500 GHz in 2010 [244] with an EBJ width of 120nm. In 2016 these values have been improved to f_T/f_{max} of 505/720 GHz [245] with an EBJ width of 105 nm and a breakdown voltage of 1.6 V. The ability to produce high performance SiGe HBTs if the BiCMOS technology move from bulk Si to FD-SOI substrates currently used in CMOS must pay attention to achieve highly doped collector sinker and buried sub-collector and how to manage the thermal dissipation due to the less conductive Silica layer.

III-V and SiGe HBTs Comparison

The advantages of the silicon-based material system are mainly its low cost, its high yield of integration and its manufacturability. A main disadvantage of III-V technologies is their fairly low integration level and yield as well as the difficulty of structural downscaling due to strong surface recombination and the resulting low current gain. Hence, it will be difficult to leverage these technologies to their full extent to enable both more complex mm-wave systems and, in particular, mass-market wafer volume in the future. As a consequence, III-V material-based technologies do not achieve the same enhancement in functionality and energy efficiency as those of silicon technology, which in turn makes it difficult for them to compete also on cost. In addition, the relatively large process variations and the lack of accurate modelling tools have notoriously hampered efficient III-V circuit design. Therefore, the III-V semiconductor industry and the related investment have been focused strongly on high-frequency/high-speed low-volume niche applications [231].

22.6.3 HBT-Based Circuits

Compact Modelling for Circuit Design

HICUM is probably the best compact model for the design of THz circuits based on HBT transistors. The relevant physical effects occurring in advanced HBTs have been included in HICUM/L2 [246] which has been developed over many years simultaneously with SiGe and InP HBT technology, partially within large-scale research projects. HICUM is presently released in all commercial circuit simulators. Besides the main equivalent circuit representing the 3D device structure directly, some additional networks try to address non-quasi-

static (NQS) effects, HF noise correlation and self-heating. However, there is a lack of compact model validation above 300 GHz. Moreover, some physical mechanisms, such as Band-Band Tunnelling [230, 247] and impact ionisation, are not properly taken into account.

Performances of HBTs-Based Circuits

By operating at sub-millimetre wavelengths, the available gain per stage of amplifiers is relatively low, due to the small margin up to the transistor f_{max}, and with an increasing part of losses to compensate for all passive components. Designers should prefer CB topology rather than CE to avoid the Miller capacitance limiting effect. However, such a CB configuration is less stable. For instance, the base inductance coming from the grounding connection and the narrow base-metal contact along the emitter has a high impact on stability and bandwidth [235]. With f_{max} close to 1.1 THz, a 9-stages amplifier using 3 µm emitter-long, 130 nm wide InP HBTs reached 24 dB at 670 GHz, with a saturated output power ($P_{S,sat}$) of −4.0 dBm [248]. The same HBTs in a differential design topology are able to minimise bandwidth reduction, and stability issues give 20 dB gain at 620 GHz, with $P_{S,sat}$ of 2.8 dBm at 585 GHz [249].

In a 200 nm InP technology where the substrate is replaced by a high thermal conductivity SiC, a 9-stages CE amplifier demonstrated 9 dB gain at 521 GHz, while a 5-stages CB amplifier is able of 19 dB gain at 576 GHz, thus 3.8 dB per stage [250].

HBT amplifiers can be compared favourably with InP HEMT amplifiers with 10 stages of which 30 dB is achieved at 660 GHz using 30 nm gate-length HEMT (f_{max} ∼ 1.2 THz) [183], and 17 dB at 850 GHz [251], and 9 dB at 1 THz with 25 nm HEMT [185].

Fixed or voltage controlled oscillators use the fundamental frequency or less efficient harmonics when CW generation is close to f_{max}, requiring subharmonic filtering. For instance, with a 250 nm InP HBT technology (f_{max}∼ 660 GHz), oscillators based on CB cross-coupled topology can deliver 10 dBm at fundamental 280 GHz with a Wilkinson combiner and −17.4 dBm at the 2nd harmonic with 591 GHz in a push-push topology [252]. Such circuits are integrated as local oscillator for mixers and subharmonic mixers for direct or heterodyne THz imagers. Transmission signal demonstrator is also designed with transmitter and receiver circuits operating at 570 GHz with a 130 nm HBT technology [235].

Front-end development for mm-wave is also addressed by the SiGe HBT technology with the demonstration of fully integrated transceiver systems [231]. Triple-push type oscillators have been designed supplying −17 dBm at 490 GHz on chip for a single-ended oscillator [253], while 16 individual differential oscillators in parallel radiating in free-space with ring antennas generate 0 dBm at 530 GHz [254]. Output power of −6.3 dBm is radiated at 430 GHz from a frequency doubler fed with a fundamental differential Colpitts oscillator [255].

From a stable low-frequency source, a cascaded ×18 multiplier chain with 2 tripler stages followed by a balanced doubler generates −3 dBm at 325 GHz [256].

From a 0.25 µm SiGe BiCMOS technology (f_{max}∼ 435 GHz), an imager was built using a frequency multiplication chain of a lower frequency source for 164 GHz fundamental generation and using six harmonic mixers to cover from fundamental to the sixth harmonic around 1 THz. The radiated power generated for the fifth harmonic (820 GHz) reached −25 dBm that enables 90 dB SNR [257].

Original circuits are also investigated, like Terahertz Oscillations from Optical Hot Carrier Injection [258]. Radiation from ultrafast accelerating charges in Si or SiGe can be generated from femtosecond laser pulse excitation and first demonstration showed oscillations around 4.5 THz [259]. Photo-generated electron-hole pairs are separated with increasing velocity under high electric fields. Such a hot carrier transport property should be better understood to link radiation to saturated and overshoot velocity mechanisms in carrier separation.

22.6.4 Perspectives

Pushing HBTs to even higher frequencies needs to overcome limiting factors already discussed, such as self-heating, charge carriers transit time and parasitics. This addresses both fabrication aspects and modelling/simulation tools from the physics at the heart of the transistor, to a more precise circuits design for highest frequencies. The roadmap pushes to reduce the emitter and collector junction area, by thinning the base with high doped layer to maintain low access resistance and low junction capacitance, and by spreading the heat closely from the hot spot to surrounding 3D. InP MMIC integration on SiGe Bipolar CMOS (BiCMOS) can offer the best of each part for THz circuits, while MOS-like FET digital circuits aspire to a low power use for the bipolar counterpart. Concerning more specifically the III-V HBT, we can point out its integration on the same chip with MOS technologies (hetero integration), for optical telecoms and low-cost Terabits transmissions in datacentres. Concerning the application domains, the prospects for very fast silicon bipolar transistors fall fairly conventionally into three categories:

1. In telecom, the rise in frequency of networks with millimetre 5G but also 6G whose frequencies discussed are between 100 GHz and 300 GHz is an area that is already the subject of research in BiCMOS.
2. In THz sensors (or radars), but the CMOS/ BiCMOS positioning remains to be determined because the BiCMOS

will only really make a difference if power is required, especially for transmission. On this subject, we know that BiCMOS is potentially interesting but the field of THz sensors being vast and the markets still poorly identified, we remain in a hypothetical vision.

3. In more exotic applications such as radio-astronomy and quantum computing (signal processing circuits).

22.7 Complementary Metal Oxide Semiconductor Transistors

Over the past several decades the performance of silicon-based technologies, i.e. complementary metal oxide semiconductor (CMOS) and Bipolar CMOS (BiCMOS), has been improved at a remarkable rate. Field-effect transistors (FETs) and, in particular, silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) now report cutoff frequencies f_T and maximum oscillation frequencies f_{max} reaching or going above 300 GHz which directly enters into the THz frequency range [260].

This improvement of performance of FETs originates from the reduction in the minimum feature size as well as innovations, such as shifting to high-k dielectrics, implementing silicon-on-insulator (SOI), strained active regions, etc. The progress is driven almost exclusively by the requirements of higher density and efficiency in digital systems. From the progress in the field of analogue CMOS integrated circuits, there are indications that CMOS FETs already approached to their speed limits at about 45 nm and 65 nm nodes. However, a theoretical analysis of SiGe HBTs indicates that operating frequencies of 1 THz and beyond are plausible in the future [261].

The main advantage of the development of silicon technologies for applications in the THz frequency range, besides the ability to fabricate large-scale circuits, comes from the possibility to form large collaborative acting clusters that can offer opportunities different from other established technological approaches for the THz frequency range or even to enable new functionality for applications that other technologies cannot provide.

Here we will review the progress in the field of THz emitters and detectors concentrating on CMOS-based devices.

22.7.1 Emitters

In comparison with compound semiconductor technologies based on GaAs or InP and others, which are commonly used for high-frequency applications, the use of standard CMOS-based electronics is severely restricted by lower f_T and f_{max} frequencies and considerably low breakdown voltage of typical devices which, in addition to limitations in frequencies, poses a limitation in power. In order to achieve generation at THz frequencies, a number of different solutions for CMOS-based emitters have been proposed. For example, the rectified signals of several phase-shifted oscillators can be summed in order to produce higher harmonics by the so-called linear superposition technique and resulted in the first report of −46 dBm at 324 GHz [262]. One of the first reports to implement a signal emitter using device nonlinearity for simultaneous harmonic generation resulted in −49 dBm at 410 GHz [263]. The latter concept relies on the realisation of a strong fundamental oscillation, which typically is close to the half of f_{max} and efficient extraction of the harmonics. The schematics of two oscillators which got mostly used to implement this concept are given in Fig. 22.28. The oscillator schematics presented at the left side employ three transistors with inductive loads and inductive elements to provide a 120° shift. This, so-called triple-push, configuration provides several advantages over a two-transistor based push-push oscillator by allowing fundamental oscillations near f_{max} and higher voltage swing which is advantageous for higher harmonic generation [264]. The implementation of this concept, based on on-wafer measurements, resulted into generation of −7.9 dBm at 482 GHz frequency [264]. On the other hand, an efficient coupling of a number of oscillators was reported to generate −1.2 dBm at 290 GHz and −3.3 dBm and 320 GHz [265].

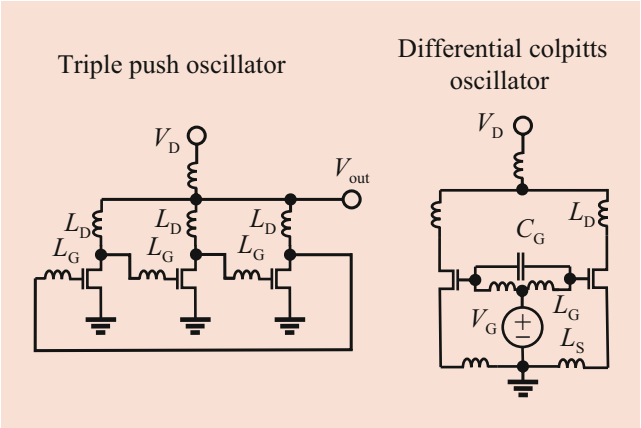

Fig. 22.28 Simplified schematics of triple-push and differential Colpitts oscillators

One of the common ways to extract generated power from the oscillator requires designing efficient antenna. Typically this is performed by driving a differential antenna and requires to perform special modifications for these purposes. Coupling between neighbouring oscillators imposes challenges for achieving maximal output levels. However, an efficient realisation allows emission into the free space of up to −4.1 dBm at 288 GHz [266].

The right side of the Fig. 22.28 presents the dual transistor design which is commonly named as differential Colpitts

oscillator. The fundamental oscillation frequency is primarily set by the *LC* resonator connected between the gates of transistors. This concept is also well suited to drive differential antenna and ensures efficient nonlinear conversion. Whereas first implementations into 90 nm CMOS technology resulted in −8.8 dBm at 217 GHz frequency [267], the shift to 65 nm technology and optimisation of the circuit allowed to improve the level of emitted power to −2.7 dBm at 293 GHz [268] and also to achieve currently the highest frequency for CMOS-based oscillators of 615 GHz with a −17 dBm of total emitted power [269]. Furthermore, with the help of an external synchronisation, an array of 30 equivalent densely packed emitters produces up to +9 dBm at 280 GHz [270].

Besides the technical availability to form clusters of oscillators which can be used for power combining, the maturity of CMOS technologies also offers the possibility to implement an array of synchronised devices which allows for beam steering at 338 GHz with angles of 45° and 50° along two axes [271] or making the part of spectroscopic THz instrumentation based on a set of circuits with different functionalities such as a 550 GHz frequency synthesizer [272].

Figure 22.29 presents a summary for total radiated power achieved with CMOS emitters. The closed symbols belong to nonlinear conversion-based concepts whereas open symbols represent results of multiplier-based (varactor-based) emitters being either active [273] or passive [274]. Although both nonlinear oscillator and varactor-based approaches produce comparable levels of output power below 600 GHz, the separation of nonlinear elements allows for a more efficient conversion and, therefore, to extend the frequency operation up to 1.4 THz [275]. It is worth noting that the development of radiation emitters relies, to a large extent, on the availability of high-frequency models for devices. Such models are typically validated for the GHz frequency range, yet their application to the THz range becomes disputable due to the increasing importance of high-frequency transport related phenomena such as skin currents or the excitation of plasma waves which gain importance in this frequency range and can affect the efficiency of mixing [276]. However, since the limits of operation of the active part is predetermined by unity gain frequencies which, for CMOS technologies, lay below 300 GHz, even existing models allow creating successful designs also for the extended frequency range.

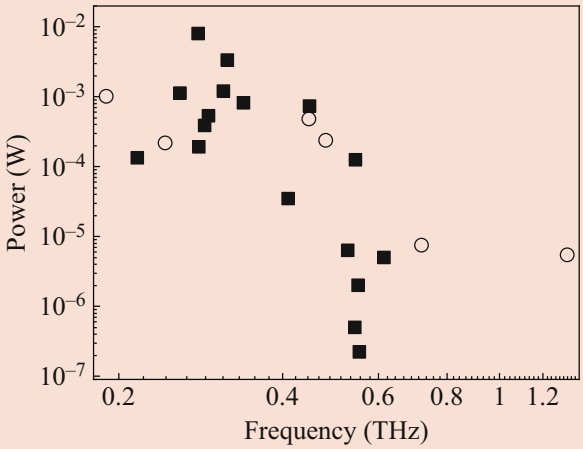

Fig. 22.29 The total radiated power is reported as a function of frequency for the state-of-the-art CMOS sources. The closed symbols correspond to nonlinear conversion-based concepts whereas open symbols represent results of multiplier-based emitters

22.7.2 Detectors

Similar to the situation with THz emitters, there are many different physical phenomena which can be used with CMOS technologies in order to produce detectors sensitive to THz radiation. These devices can be subdivided into two groups: thermal detectors (bolometers) and electrical nonlinearity-based rectifiers and mixers. The bolometer measures the increase of local temperature due to absorbed THz power and can be implemented on micromachined CMOS [277] with silicon devices used to measure the temperature change or in CMOS-compatible technology process [278]. The rectifier directly responds to electrical signals, and the detection is based on the nonlinear current-voltage dependence which is characteristic for diodes and transistors. It is interesting to note that a conventional diode with *pn* transition, due to transport limitations of minority carriers, is considered to be too slow. The small node size achievable with CMOS technologies allows fabricating devices with zero-bias cutoff frequencies in the 1–2 THz frequency range with reported efficient detection at 0.78 THz [279]. Being the standard for other technologies, Schottky-diode approach can be used for the implementation of efficient detectors in CMOS and BiCMOS technologies [263, 280]. The diode-like characteristics can be realised with diode-connected field-effect transistors (FETs) [281]. However, it has been shown that efficient detection can be realised in antenna-coupled CMOS detectors even when the detection frequency is much higher than the transistor cutoff frequency [208]. The modelling and optimisation of devices for the efficient detection of radiation which extends deeply into the THz frequency range require accounting for peculiarities of high-frequency electrical transport which is captured by the hydrodynamics-based physical models.

The first investigations about using silicon-based transistors for THz detection were performed on devices without appropriate antennas for radiation coupling [197, 282] as a part of research dedicated to prove predictions made by Dyakonov and Shur [198]. Initially, the first antenna coupled devices achieved comparably moderate sensitivity values.

The sensitivity of power detectors is typically characterised by the level of input power which produces electrical signal equal to the amplitude of detectors electrical fluctuations with 1 Hz equivalent noise bandwidth, i.e. noise equivalent power (NEP). The first devices designed for 600 GHz frequency range reported NEP of 300 pW/$\sqrt{\text{Hz}}$ [208]. The currently achieved optical performance is now approaching the value of 10 pW/$\sqrt{\text{Hz}}$ [283]. Moreover, detectors with substrate lens demonstrate broad-band operation with nearly flat frequency response from 400 GHz up to 1.5 THz [217] and can be used with THz radiation generated using low-average-power emitters like photomixers [217] or photoswitches [284].

The summary of published noise equivalent power values for state-of-the-art CMOS detectors is given in Fig. 22.30. Performance of FETs-based detectors is given with open symbols, whereas closed symbols represent the shot-noise limited NEP of CMOS-based Schottky diodes. One can note that although a database for FET detectors is much larger than that of CMOS detectors, deep in the THz frequency range both detector concepts experience a similar roll-off with comparable performance values for FETs [205,285] and for Schottky diodes [280].

For the case of emitters, one of the key advantages of silicon technologies is the ability to form detector arrays which can be used for imaging applications [286, 287]. Moreover, the availability of both types of components, i.e. emitters and detectors, makes it possible to realise all-electronic silicon-based applications spanning from raster-scan imaging [288] to near-field imaging [289] or even time-domain like spectroscopy [290]. Later applications either partially or fully employ the BiCMOS approach, which is extending the frequency range of operation of FET-based CMOS devices for emitters with higher oscillation frequencies as well as for detectors. A broad overview of the performances achieved using both technologies and their comparison can be found in Ref. [260].

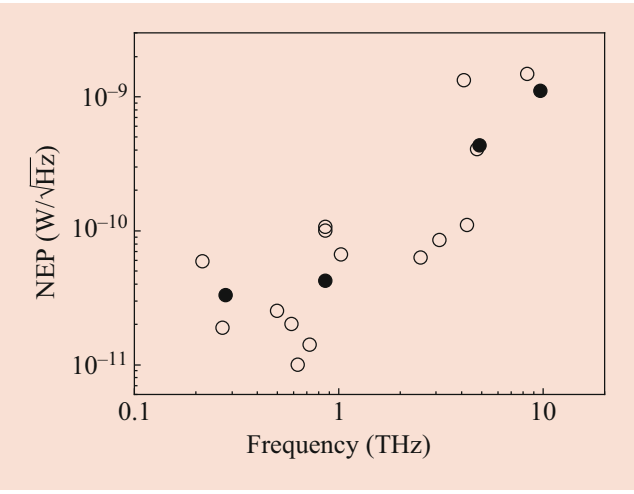

Fig. 22.30 Summary of reported noise equivalent power values for state-of-the-art CMOS detectors. Open symbols represent FETs, closed symbols—shot-noise limited NEP of Schottky diodes

In summary, over the last decade analogue electronic device concepts in silicon technologies advanced deeply into the THz frequency range. Literature reports on a variety of emitters reaching up to 1.4 THz, detectors enabling sensitive detection in the 0.3–10 THz frequency range and lighter and more compact systems able to promote new and emerging applications.

22.7.3 Perspectives

Over the last two decades the technological progress achieved in CMOS technologies enabled implementations of high-frequency analogue circuits which can directly compete with other established technologies. By now, the oscillation frequencies of fundamental oscillators fabricated directly in CMOS can easily exceed 100 GHz, whereas nonlinear conversion-based devices such as multipliers, mixers or detectors are proven to operate even above 1 THz with the state-of-the-art performance. Furthermore, one of the key advantages that CMOS technologies is offering to the development of THz electronics is its exceptional affinity to form circuits on the large scale thus allowing the combination and integration of hybrid electronic and photonic concepts on a chip level. This allows for improvements of the performance and efficiency of current concepts as well as provides with the potential for the invention of novel devices.

22.8 Ballistic Rectifiers

Ballistic rectifiers (BRs) are fundamentally different from most rectifying elements in the sense that they do not rely on any doping junctions or tunnelling barriers. Instead, their non-linear behaviour arises from the ballistic regime of electron transport where the mean free path of carriers is longer than the characteristic length of the device. This leads to the carriers scattering of the edges of the sample rather than random crystal defects and phonons in the conductive medium. As will be explained in this section, the 2D nature of the device and its zero threshold operation are ideal for THz detection applications. To date there has been no indication of a cutoff frequency in BRs fabricated from graphene up to 1 THz [291].

While it has been possible to observe ballistic effects for many years (in 2D III-V quantum wells at cryogenic temperatures), nanostructures below about 100 nm are necessary to observe these effects at room temperature [292]. The emergence of graphene and subsequent advancements in fabrication techniques allows for mean free paths above

1 μm without the need to cool the sample [293]. This section will explain how BRs operate and review how they could be used as THz detectors .

22.8.1 Ballistic Formalism

Figure 22.31 is a schematic of two different types of BR; both are four terminal devices with two input leads and two output leads. The grey region denotes the conductive region of the device, and the orange regions are the contacts. In both schematics shown the input contacts are labelled Source (S) and Drain (D), while the output contacts are labelled Lower (L) and Upper (U). While the geometry of the devices depicted in Fig. 22.31a, b is different, the operating principle is similar. Figure 22.31b has the narrowest part of the current injector S labelled W_{SD} (the width of both S and D leads is designed to be the same), similarly for the narrowest part of the channel between L and U (W_{LU}). A naive explanation describing the operation of these devices is to consider carriers like billiard balls on a table shaped like the device in the figure. The carriers are free to travel down potentials and bounce off the edges of the sample. In both cases the two input leads are angled such that most carriers arriving from either source or drain (forward and reverse bias) end up at one of the two output leads. In the figure, typical carrier trajectories are shown with arrows to guide the eye. The result of this is that an AC or indeed an RF signal applied between S and D is rectified into a DC voltage between L and U (indeed the voltage drop between L and U keeps the same sign).

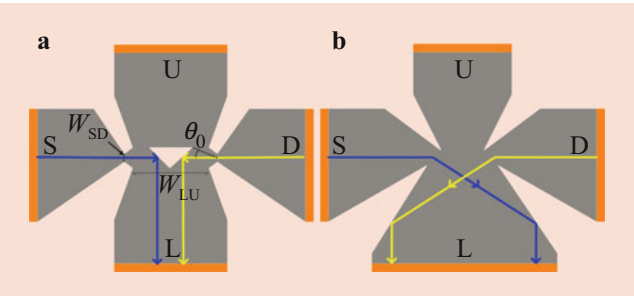

Fig. 22.31 Schematics of two ballistic rectifiers both with and without a triangular scatterer (etched region to scatter electrons), (**a**) and (**b**), respectively. In case (**b**) scattering takes place at the edges of the structure. The grey regions denote the conducting regions, and the orange regions represent the contacts. The input contacts are labelled Source (S) and Drain (D). The output contacts are labelled Lower (L) and Upper (U) with blue and yellow lines demonstrating typical carrier trajectories through the device. W_{SD} has been labelled for S to indicate the narrowest part of the current injectors, similarly for W_{LU}. The angle θ_0 has been labelled to indicate above what angle electrons exiting D will reach U instead of L

The billiard ball model for the ballistic regime of electron transport only goes so far to describe the behaviour of these devices. Instead, a more rigorous approach would be to use an extended Landauer-Büttiker formalism generalised for many conductance channels [294, 295]. In this model the conductance between lead β and α is given by

$$G_{\beta\alpha} = \frac{2e^2}{h} T_{[\beta,\alpha]}(I_{[\beta,\alpha]}) \,, \tag{22.27}$$

where e is the charge of an electron, h is Planck's constant and $T_{[\beta,\alpha]}(I_{[\beta,\alpha]})$ is the transmission probability from contact α to β (which can be S, D, L and U in our case); $T_{\beta\leftarrow\alpha}(I_\alpha)$ if the chemical potential in lead α $\mu_\alpha > \mu_\beta$ or $T_{\alpha\leftarrow\beta}(I_\beta)$ if $\mu_\beta > \mu_\alpha$. Setting the boundary conditions $I_S = -I_{-SD}$, $I_L = I_U = 0$ and $V_S = 0$ reduces the fourfold conductance matrix to a threefold matrix (**G**). Taking the inverse of this matrix gives you the matrix of resistances **R**. To model the device output we need the four probe resistance $R_{SD,LU} \equiv V_{LU}/I_{SD}$ (analogous to Hall resistance):

$$R_{SD,LU} = \mathrm{Det}(\mathbf{G})^{-1}(G_{US}G_{LD} - G_{UD}G_{LS}) \tag{22.28}$$

Reference [295] goes into detail how Eq. (22.28) can be used to determine $R_{SD,LU}$ for various geometries of BR with a triangle. This leads in this specific case to

$$R_{SD,LU} \approx -\frac{h}{e^2}\frac{3\hbar}{4eE_F N_{SD}}\frac{\sin 2\theta_0}{2N_{LU} - 3N_{SD}(1-\sin\theta_0)} I_{SD} \tag{22.29}$$

Here, N_{SD} and N_{LU} are the number of conduction modes that can travel through the narrowest constrictions of S or D and L or U, respectively. N_{SD} is related to the width of the narrow input leads by $N_{SD} = \frac{k_f W_{SD}}{\pi}$ where k_f is the Fermi wavevector of the carriers; the equivalent is true for N_{LU}. θ_0 is the angle relative to the normal vector of the narrowest part of the S or D leads where a carrier ejected from the lead will end up at U rather than L. These geometric factors (W_{SD}, W_{LU} and θ_0) have been labelled on Fig. 22.31a for clarity.

An important step during the derivation of Eq. (22.28) is including the excess momentum of carriers emerging from the narrow junctions, a result of the large potential drops and high field gradients over these regions. The effect of this is to collimate emerging carriers and decollimate carriers travelling towards these leads. This collimation and decollimation is a non-linear effect and is the true origin of the rectification in a device of this type. While the model is simple and ignores some of the subtleties, such as how the resulting trajectories change for higher numbers of modes and electron-electron interactions, it does give some insight into what we can expect from the output of the device. Firstly, there is a quadratic dependence of voltage on current and

therefore a linear voltage output with input power for small input signals; this can be shown from Eq. (22.29):

$$V_{\mathrm{LU}} = R_{\mathrm{SD,LU}} I_{\mathrm{SD}} \approx -\frac{h}{e^2}\frac{3\hbar}{4eE_{\mathrm{F}}N_{\mathrm{SD}}} \frac{\sin 2\theta_0}{2N_{\mathrm{LU}} - 3N_{\mathrm{SD}}(1-\sin\theta_0)} I_{\mathrm{SD}}^2 \quad (22.30)$$

Secondly, we can expect the device to work best when there are fewer conduction modes; this is the case when the dimensions of the device are small.

There are several reasons to use a BR rather than a different THz rectifier such as a Schottky diode or a metal-insulator-metal (MIM) diode. The two-dimensional nature of BRs reduces parasitic capacitance to a minimum thus decreasing the *RC* time constant. This is an important value to consider when looking at cutoff frequencies for such devices and could indicate that BRs may operate at higher frequencies, although they have not been tested above 1 THz at the time of publication. At the present time, BRs are among the most sensitive THz diode detectors with a high responsivity at room temperature [291]. They have relatively low resistances and can even be stacked in parallel for even better impedance matching, one of the most important characteristics for a high-frequency device. BRs demonstrate very low noise values; this is because the input and output contacts are mostly decoupled so that the output signal is largely uninfluenced by the noise of the input signal. This decoupling allows the resistance between L and U to be low without compromising the sensitivity of the device by changing the resistance between S and D. They have a zero voltage onset due to the fact that they do not rely on any doping junctions of barrier structures allowing them to rectify very small signals. They have a linear voltage response with power input (which is not the case for most diode detectors), a desirable feature in sensing technology. In some applications it might be useful to be able to tune the resistance of the device by changing the carrier density dynamically with a small local gate; for the case of graphene BRs the polarity of the output could even be changed. Moreover, the planar nature of the device also means that its fabrication is simple and scalable, no need for very challenging nano-scale alignment accuracy between structures in different layers. Finally, the planar nature also makes it straightforward to integrate a planar antenna to the BR without need for interconnects.

Conversely, BR devices also require materials characterised by a high mobility of majority carriers ($30{,}000\,\mathrm{cm^2V^{-1}s^{-1}}$), and for most commercial applications this must be true at room temperature. While GaAs quantum wells have extremely high mobility at low temperature, this is not true at room temperature. Graphene, on the other hand, can have a mobility of $200{,}000\,\mathrm{cm^2V^{-1}s^{-1}}$ at room temperature but not yet in scalable samples. However, the mobility and scalability of these materials is always improving.

22.8.2 BR Electrical Characteristics

Work started on BRs in the late 1990s as fabrication procedures became sufficiently advanced to reliably produce sub-micron devices in GaAs-AlGaAs and GaInAs-InP compounds, initially for DC [296, 297] and then for RF up to 50 GHz [298]. graphene, being one of the materials with the highest carrier mobility at room temperature, is a very promising candidate for BRs with DC and AC measurements [299–301] and then RF up to 700 GHz [291] with no sign of a cutoff frequency.

As discussed in the previous section BRs are expected to have symmetric quadratic DC I-V characteristics, while this is the case, experimental results often show some asymmetric components; see Fig. 22.32a. These asymmetric components are a consequence of small fabrication defects. However, this effect averages out when an AC input is applied and only the non-linear component of the I-V characteristic needs to be considered. The figure shows when electrons dominate (positive V_{G}) the curvature is negative; the opposite is true for holes.

In Fig. 22.32b the DC output V_{LU} is plotted against gate voltage (V_{G}) for a range of different applied AC currents. The output demonstrates the same ambipolar behaviour where electrons give a positive V_{LU} and holes give a negative one. What is true for both carrier types is that as the neutrality point is approached V_{LU} increases due to a reduction in the number of conduction modes through the channel reducing the spread in trajectories from each lead and increasing the effect of collimation. Close to the Dirac point there is a linear change in carrier type; this is a direct result of competing electron and hole conduction coexisting due to thermal excitation. Figure 22.32c shows how V_{LU} depends on AC and DC input power (P_{SD}) for two different gate voltages corresponding to peeks in the output for electrons and holes. At low power the device demonstrates a linear dependence of the output voltage vs input power; however there is a clear saturation effect at higher powers; this is likely due to an increase in phonon scattering from Joule heating. The peek responsivity of the device shown here was 23,000 V/W, an extremely high value for a THz diode detector. However, it is important to note that this is only a measurement of the intrinsic device properties which ignores effects such as impedance mismatch which often dominate losses at high frequency.

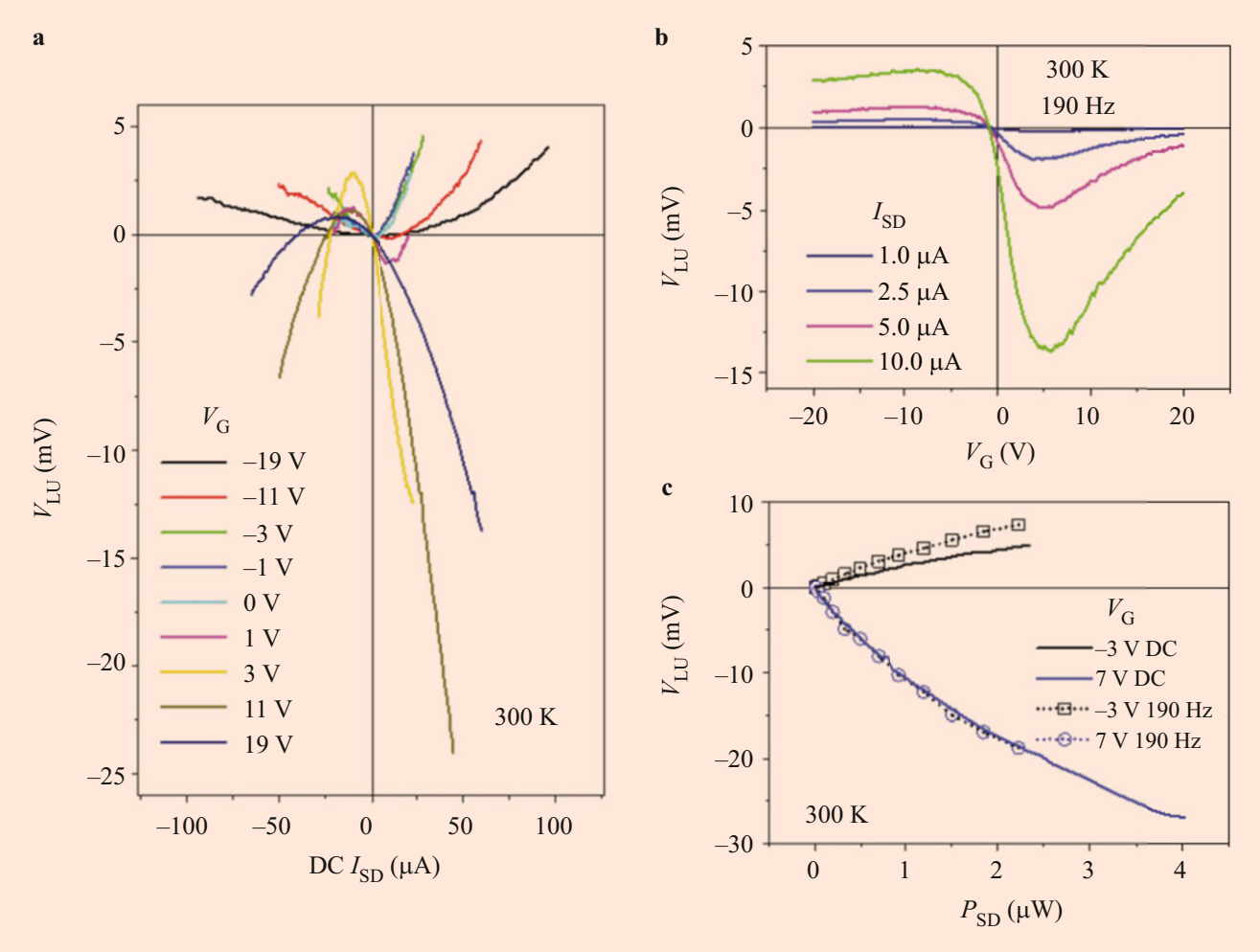

Fig. 22.32 (**a**) shows the DC I-V characteristics of a graphene BR with no triangle at various gate voltages (V_G). (**b**) and (**c**) demonstrate the rectifying properties of the same device while V_G is changed (for various input currents) and while input power is changed, respectively. (Adapted with permission from [301])

22

22.8.3 THz BR Detection

The initial high-frequency characterisation of BRs made from GaAs 2DEGs was done using a specially designed RF mesas where the ground plane wraps around the input and output contacts so they behave like strip lines. The strip lines allow microwave power to be applied to the device with the use of an RF probe station in conjunction with a vector network analyser (VNA) with minimal losses. Reference [298] shows how a BR made from InGaAs/InP can be used to rectify a 50 GHz signal at room temperature. Here the responsivity of the device at high frequency is nearly 2 orders of magnitude lower than at low frequency because of impedance mismatch with the contacts and VNA. Impedance mismatch is one of the limiting factors for all diode detectors because VNAs typically need to be matched at 50 Ω.

In order to detect THz radiation a BR must be coupled to a suitable antenna. The combination of an antenna with a rectifier is known as a rectenna and is the primary potential use for the BR . The rectenna was first demonstrated by Brown in the 1960s for wireless microwave power transfer to a small helicopter with an array of 28 rectennas operating at 2.45 GHz, and the helicopter was able to reach a height of 20 m [302]. Today they have been demonstrated as wireless on-chip interconnects [303, 304], energy harvesting devices [305, 306] and wireless power transfer in medical applications [307]. However, most of these examples are below 10 GHz and do not take advantage of the unique properties of the THz part of the EM spectrum. In Ref. [291] the BR is demonstrated to have a peak responsivity of 764 V/W, a minimum noise equivalent power (NEP) of 34 $pWHz^{-1/2}$, a linear voltage response over 3 orders of magnitude power

input and no signs of a cutoff frequency up to 700 GHz. The same paper demonstrates BRs as a tool for imaging THz radiation in transmission mode.

With regard to the cutoff frequency in the BR, it is likely to be very high due to the fact that the resistance of the BR is relatively low (as low as 1 kΩ) and the capacitance of the device is extremely small due to the planar nature of its structure. The dominant sources of the capacitance come from the antenna/device contact and from the self-capacitance of the device. When graphene is encapsulated by boron nitride, 1D contacts can be made where the same polymer mask is used to reveal the graphene edge and perform lift-off after metallisation allowing for self-aligned contacts with <10 nm of overlap [301]. This small overlap minimises contact capacitance and decreases the resistance of the contact [308].

22.8.4 Perspectives

BRs are a young but exciting technology, still not used outside of research laboratories. They require further development before they can be used in practice. They could have one of the highest cutoff frequencies of any diode detector. They have demonstrated very high sensitivities and low noise levels with linear output voltage to input power ratios over a wide range. These properties make them ideal for use in conjunction with an antenna for a wide variety of applications in THz security imaging, medical imaging, power transfer and communications. At even higher frequencies they could be used for heat energy harvesting and recovery.

22.9 Conclusions

In this chapter we have provided a summary of the most important electronic devices used for the development of THz detectors, emitters and associated systems. The information can be used as the starting point for advancing fundamental and applied research and to better understand the physical principles exploited in the field of THz-wave technologies. It is evident that the involved technologies, even if well developed since some years, still need great advances in many theoretical and experimental domains: in particular, while different types of detectors (direct and heterodyne) are already commercially available, the choice of emitters (CW or pulsed) is more limited, and probably it will represent the main technological bottleneck for the next years. When a large range of detectors and emitters with different performances and costs will become available, more and more circuits and systems will be developed and realised opening the way to a huge panel of practical applications.

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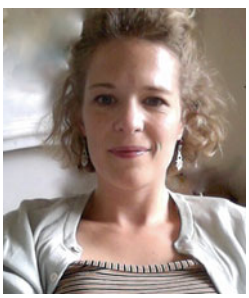

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Semiconductor Lasers

23

Martin R. Hofmann and Stephan W. Koch

Contents

23.1 Fundamentals 851
23.1.1 Gain Medium 851
23.1.2 Pump Process 854
23.1.3 Resonator 855

23.2 Technical Properties 856
23.2.1 Introduction 856
23.2.2 Fundamental Behavior 857
23.2.3 Dynamics 857
23.2.4 Spectral Properties and Coherence 857
23.2.5 Beam Quality 858
23.2.6 Polarization 858
23.2.7 Optical Power 858
23.2.8 Temperature Dependence 859

23.3 Materials and Architectures 859
23.3.1 Semiconductor Materials 859
23.3.2 Quantum Confinement Structures 860
23.3.3 Quantum Cascade Lasers 860
23.3.4 Microcavity Lasers 861

23.4 Applications and Outlook 862
23.4.1 Applications 862
23.4.2 Outlook 863

References 863

Abstract

This article discusses the basic operation principle, material engineering aspects, and different architectures for the design of semiconductor lasers. The laser fundamentals are summarized in Sect. 23.1, whereas technical properties and a discussion of device dynamics are presented in Sect. 23.2. Section 23.3 addresses more detailed aspects such as materials and architectures for different diode laser systems. Finally, Sect. 23.4 reviews the most relevant application fields and gives an outlook on technological challenges and future developments.

Keywords

Semiconductor lasers · Semiconductor fundamentals · Optical gain · Resonator · p-n-junction

23.1 Fundamentals

The three major ingredients of any laser are the (optical) gain medium, the pump process required to achieve population inversion in the gain medium, and a resonator to provide optical feedback. In the following, we discuss these basic aspects for the semiconductor laser systems separately before we proceed to the analysis of more specific properties.

23.1.1 Gain Medium

Crystalline solids have a characteristic band structure $E_\lambda(\boldsymbol{k})$, which specifies the quantum mechanical states that can be occupied by the crystal electrons. Here, the band is labeled by λ and $\boldsymbol{k}$ denotes the quasi-momentum vector of the electron. Of particular importance for the optical and electronic properties of a material are the energetically highest bands that are *completely filled* by electrons – the valence bands – and the next higher band – the conduction band – which is partially filled by electrons in metals but completely empty in insulators. As semiconductors, one usually denotes insulators where the energetic difference between the top of the valence bands and the bottom of the conduction bands, i.e., the bandgap E_g, is

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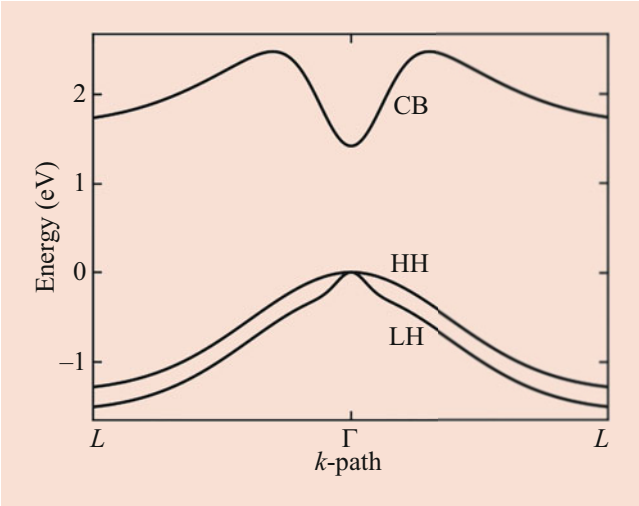

Fig. 23.1 Computed band structure (energy versus carrier momentum) of bulk GaAs in the vicinity of the Γ-point where the direct optical transitions take place. Shown are the conduction band (CV) together with the heave-hole (HH) and light-hole (LH) valence bands

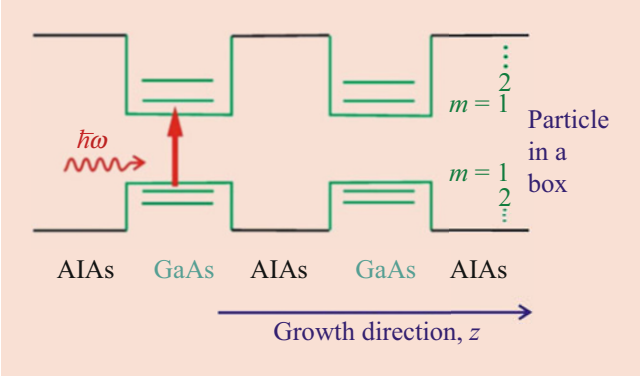

Fig. 23.2 The direct band gaps of GaAs and AlAs are plotted as function of the growth direction. The GaAs parts of the structure form the quantum wells which provide quantum confinement in one dimension. The corresponding eigenstates for the particle-in-a-box, here a one dimensional box, are indicated and it is shown how a resonant optical excitation induces a transition between the quantum confined states

in the energy range of visible light or below. The value of E_g defines the energy needed for light to resonantly interact with the particular semiconductor system.

To be useful as laser gain medium, a semiconductor material has to efficiently couple to the light field. For this, its bandgap has to be *direct*, i.e., the conduction-band minimum and valence-band maximum have to occur at the same $\boldsymbol{k}$ value. Furthermore, it needs conduction and valence bands with the proper symmetries that allow for a large matrix element of the optical dipole operator, i.e., a significant value of the dipole moment.

The best known material satisfying the necessary requirements is the binary compound semiconductor GaAs which was discovered by Heinrich Welker in the early 1950s [20]. An excerpt of the GaAs band structure in the region interesting for semiconductor laser applications is shown in Fig. 23.1.

In fact, the historically first semiconductor laser was based on bulk GaAs [18]. However, the breakthrough for these devices came with the invention of semiconductor *heterostructures* which typically consist of several layers with different material compositions. Most noteworthy in this context are the $Al_xGa_{1-x}As$ compounds, where the Aluminum concentration x can be up to 40% for the material to have a direct bandgap which increases with increasing x. Since the lattice constants of GaAs and $Al_xGa_{1-x}As$ are almost identical, heteroepitaxy allows for the lattice matched layer-by-layer growth of materials with different compositions.

Sandwiching several atomic layers of $Al_xGa_{1-x}As$ with a low x_{QW} between layers with higher aluminum concentration, $x_{\text{barrier}} > x_{\text{QW}}$, yields a so-called quantum well (QW) structure where the low x compound constitutes the well and the higher x material acts as barriers, see Fig. 23.2. Such a heterostructure arrangement inhibits the movement of low energy carriers in the growth direction, i.e., they experience a one-dimensional potential well. At the same time, the carrier mobility is unrestricted in the two-dimensional plane perpendicular to the growth direction.

Quantum mechanical treatment of such a particle-in-a-well configuration results in discrete energy states whose spacing scales inversely with the square of the well thickness. The energetically lowest state is determined by the fundamental uncertainty principle, representing the zero-point motion of the quantum confined electron. Effectively, in semiconductor QWs this ground-state energy occurs additively to the bandgap energy with the consequence that the minimum energy for resonant optical excitation increases as a consequence of the quantum confinement in one dimension. Since energy and wavelength are inversely proportional to another, one often refers to this energy increase as a *blue shift* of the optical transition.

The width of a QW can be chosen relatively freely in the epitaxial growth process thus allowing for a certain degree of freedom to engineer important aspects of the optical material properties. Additional design flexibility can be gained by realizing that modern growth techniques not only allow for the realization of heterostructures using materials with the same lattice constant. To some degree also lattice mismatched compounds can be utilized, provided that the mismatch is not too large. Under ideal conditions, epitaxial growth leads to an adaption of the lattice constant in the growing layer to that of the underlying substrate. Effectively, the resulting deviations from the lattice constant of the unperturbed material are equivalent to a certain degree of elastic strain which can be tensile or compressive, depending on whether the lattice

constant of the growing layer is larger or smaller than that of the underlying substrate, respectively.

In such strained layer QWs, one has to carefully monitor the amount of accumulated strain such that the formation of fractures, islands, or other unwanted features is avoided. However, the advantages outweigh the structural problems since strained-layer growth not only broadens the range of suitable materials but also allows one to deliberately use the strain effects to modify the in-plane QW band structure in a desirable way. Therefore, many commercially available semiconductor lasers these days are based on gain media consisting of a QW heterostructure made of lattice mismatched semiconductor layers.

In addition to the band structure, also the quantum mechanical interactions in the semiconductor material system strongly influence its laser gain medium properties. In the fundamental light absorption process, a single photon excites an electron from the filled valence band into the conduction band of the medium. Starting from the original unexcited state with N negative elementary charges in the valence band, $N(-e)$, the excitation leads to $(N-1)(-e)$ in the valence band and a single negative charge $(-e)$ in the conduction band. Since the *removal of a negative charge* is equivalent to the *addition of a positive charge*, $(N-1)(-e) = N(-e) + (+e)$, one introduces the concept of the positively charged *valence-band hole* , or simply *hole,* as a new semiconductor quasi-particle. Referring to the conduction-band electron as *electron*, one describes the absorption of a single photon as a process in which an *electron-hole pair* is created. Similarly, the system can emit light when a conduction-band electron jumps back into the valence band and releases its excess energy to the photon. Since this process involves the generation of a photon under simultaneous annihilation of an electron and a hole, it is referred to as *radiative electron-hole* recombination.

From basic electrodynamics, we know that positive and negative charges experience the mutually attractive Coulomb interaction. On the elementary particle level, this may even lead to quantum mechanically bound states with the hydrogen atom as the most prominent example where a single electron is Coulomb bound to a positively charged proton. In a very similar fashion, there are bound electron-hole-pair states in semiconductors which are referred to as *excitons*. However, despite the identical physical concepts, the properties of excitons are significantly different from hydrogen, showing up most prominently in the much smaller value of the binding energy which is close to 13.6 eV in hydrogen and only around a few *meV* for most semiconductor excitons.

In order to utilize a semiconductor structure as a laser gain medium, one has to *pump* the system, i.e., one has to prepare a condition where the probability for light emission is larger than for absorption. In an electron-hole plasma, the possibility for light emission from a state $\mathbf{k}$ is determined by the probability $f^{\mathrm{e}}_{\mathbf{k}}$ to find an electron in that state times the probability $f^{\mathrm{h}}_{\mathbf{k}}$ to find the matching hole, i.e., $\propto f^{\mathrm{e}}_{\mathbf{k}}\, f^{\mathrm{h}}_{\mathbf{k}}$. This probability for emission has to be larger than that for absorption which needs unoccupied electron and hole states, i.e., $\propto (1 - f^{\mathrm{e}}_{\mathbf{k}})\,(1 - f^{\mathrm{h}}_{\mathbf{k}})$. Note that for Fermions, the Pauli exclusion principle applies with the consequence that the maximum occupation probability of a given state is unity, such that the probability to find a free state is unity minus its occupation probability. For emission to exceed absorption, $f^{\mathrm{e}}_{\mathbf{k}} f^{\mathrm{h}}_{\mathbf{k}} > (1 - f^{\mathrm{e}}_{\mathbf{k}})\,(1 - f^{\mathrm{h}}_{\mathbf{k}})$, or

$$\left(f^{\mathrm{e}}_{\mathbf{k}} + f^{\mathrm{h}}_{\mathbf{k}} - 1\right) > 0 \quad \text{(condition for electron-hole population inversion)} .$$

The term $(f^{\mathrm{e}}_{\mathbf{k}} + f^{\mathrm{h}}_{\mathbf{k}} - 1)$ is referred to as the (population) *inversion* factor, which has to be positive under light amplification conditions. Whereas details of the pump process are discussed in Sect. 23.1.2, all we need to know at this point is that pumping is utilized to promote a reasonably large number of electrons from the valence into the conduction band to create a positive inversion for the quantum states contributing to the lasing process. Under room-temperature conditions, the resulting configuration is referred to as an *electron-hole-plasma* state.

The relatively high density of electron-hole pairs in the plasma leads to a significant weakening of the effective Coulomb interaction potential via *plasma screening*. As a result, the attractive interaction is typically no longer strong enough to allow for the formation of bound excitons under room-temperature lasing conditions. However, Coulombic effects are still very important for a quantitative modelling of the semiconductor gain medium properties. Referring to the literature for more details [3, 7, 11], we just mention here as important consequences of the microscopic interaction effects the phenomena of (i) band renormalization, (ii) carrier scattering, and (iii) excitation induced dephasing (EID).

(i) The most obvious consequence of the band renormalization is the gap reduction with the consequence that the lowest energy for optical transitions is no longer the bandgap E_{g} of the unexcited material but the renormalized gap, $E^{\mathrm{ren}}_{\mathrm{g}} < E_{\mathrm{g}}$. Hence, we have a red shifting of the optical transitions that becomes more and more prominent with increasing electron-hole-pair density.

(ii) In a typical electron-hole plasma in semiconductor lasers, the elastic Coulomb scattering among the charge carriers leads to the very fast equilibration of the electrons and holes. Thus, on the timescale of tens to hundreds of femtoseconds ($1\ \mathrm{fs} = 10^{-15}\ \mathrm{s}$), the carriers assume Fermi distributions within their respective bands. This scenario is called *quasi-equilibrium*, since it is characterized by thermodynamic equilibrium

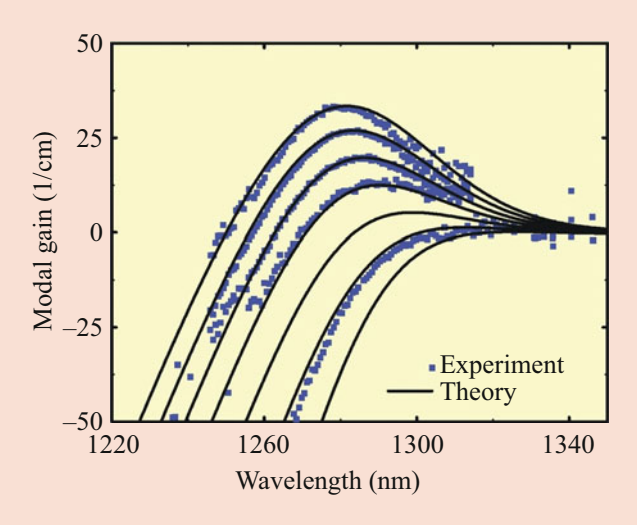

Fig. 23.3 Experimentally measured (squares) and theoretically calculated (solid lines) gain spectra for a (GaIn)(NAs)/GaAs semiconductor heterostructure. The different curves are obtained for increasing electron-hole densities (lowest on the bottom). (From Ref. [9])

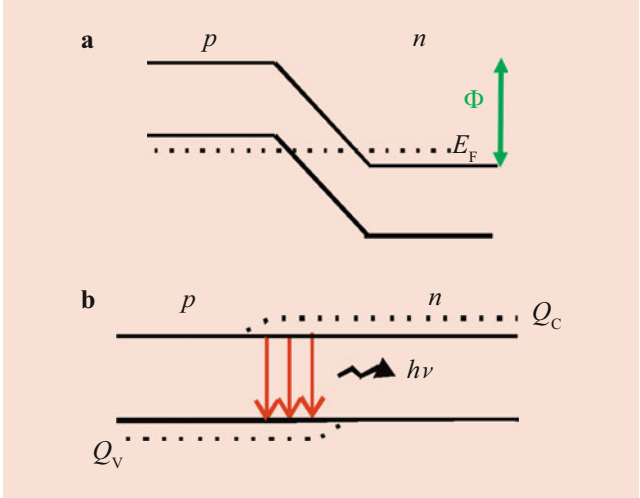

Fig. 23.4 Band diagram (Energy versus space coordinate in growth direction) of p-n-junction without (**a**) and with (**b**) applied bias

conditions among the carriers *within each band*. Clearly, the overall state of the semiconductor is still far away from true thermodynamic equilibrium since this would amount to the unexcited configuration where no electrons are in the conduction band.

(iii) An often overlooked and underappreciated Coulombic interaction effect is the phenomenon of EID. With the term *dephasing*, one usually refers to the loss of coherence, i.e., to the temporal decay of an electromagnetic wave. However, transforming this scenario from the time into the frequency domain, the dephasing determines the spectral lineshape of the signal which can be expressed via a lineshape function $L(\omega,\mathbf{k})$. Since this function enters in the equation relating the population inversion to the gain spectrum the detailed spectral shape of the gain strongly depends on the microscopic interactions via EID, i.e.,

$$g(\omega) \propto \int d^3k \left(f^{\mathrm{e}}_{\mathbf{k}} + f^{\mathrm{h}}_{\mathbf{k}} - 1\right) \; L(\omega, \mathbf{k}) \,.$$

Including all the discussed effects in a systematic microscopic theory allows for the calculation of the optical spectra for a wide variety of semiconductor compounds [3, 7, 11]. An example of a successful theory/experiment comparison is shown in Fig. 23.3.

23.1.2 Pump Process

To generate and maintain a population inversion in the semiconductor laser gain medium, one needs to supply a sufficient influx of energy which "pumps" carriers from the valence into the conduction band. The presence of a population inversion constitutes a non-equilibrium situation which would spontaneously decay without pumping.

Technically, the pumping process can be realized in several different ways. The most straight forward concept is *optical pumping* where light is absorbed to excite carriers from the valence into the conduction band. This optical excitation requires an intense light source providing the pump light with higher photon energy than the laser emission. This usually adds considerable complexity to the overall laser configuration with the consequence that optical pumping is typically not used in semiconductor lasers with the notable exception of vertical external cavity surface emitting lasers (VECSELs) which will be discussed in a subchapter below.

Most commercial semiconductor lasers today are *electrically pumped* by carrier injection via a p-n-junction. To understand the fundamental principle of this electrical pumping, we look at the schematic band diagram in the space domain in Fig. 23.4 [18].

After the generation of contact between a p- and an n-doped region, diffusion drives electrons into the p-region and holes into the n-region, respectively. The electrons leave positively charged atoms and the holes negatively charged atoms behind (space charges) which induce an electric field. In equilibrium, the corresponding field current balances the diffusion current with the consequence that there is no net current. The space-charge region is characterized by a built-in electric field and a potential step Φ which is characteristic for a p-n-junction, see Fig. 23.4a.

When a voltage V in forward direction is applied to this configuration, the potential step is reduced. As soon as V reaches the value of $V = \Phi/e$ (with the electron charge e), the potential step disappears as shown in Fig. 23.4b. Under

this condition, a current flows and delivers electrons and holes into the active region where they contribute to the inversion. In an idealized quasi-equilibrium situation where the occupation probabilities $f^{e}_{\mathbf{k}}$ and $f^{h}_{\mathbf{k}}$ can be expressed by quasi-Fermi functions, the carrier inversion condition from Sect. 23.1.1. can be translated into the condition that the difference between the quasi-Fermi levels Q_C (for the conduction band) and Q_V (for the valence band) becomes larger than the bandgap E_g. Far away from the p-n-junction, the energetic distance between Q_C and the conduction band edge with bias (right scheme in Fig. 23.4) is equal to the energetic distance of the Fermi energy E_F to the conduction band edge in equilibrium (left scheme in Fig. 23.4). The same holds for Q_v, E_F, and the valence band edge. Altogether, this implies that inversion by carrier injection can only be achieved for very strong doping of the n- and p-regions so that the Fermi-level is above the conduction band edge in the n-region and below the valence band edge in the p-region, respectively.

A simple p-n-junction like the one shown in Fig. 23.4 fundamentally allows one to achieve inversion and, as a consequence, semiconductor laser action. However, even though it was used in the first demonstration of a semiconductor diode laser in the early 1960s, this so-called homojunction scheme is rather inefficient. As a consequence, inversion can only be obtained at rather low temperatures using strong and temporally pulsed injection currents in order to avoid excess heating. The reason for the unsatisfactory pumping efficiency is the rather low achievable electron-hole pair density in the active region. The injected carriers are spread out over a rather large region which is only limited by the finite carrier diffusion length – typically on the order of micrometers – which limits the depth of penetration for the electrons into the p-region and the holes into the n-region, respectively.

A spatially reduced extension of the active region for the same number of injected carriers amounts to a higher density thus that inversion conditions can be realized much more easily. For this purpose, one resorts to a so-called double heterostructure arrangement, which is similar to the quantum well configuration discussed in Sect. 23.1.1, with the exception that the barrier material on the one side of the well is n-doped and on the other side it is p-doped, respectively. Such a structure not only provides a potential well for the electrons and holes but also allows for effective carrier injection. In this configuration, the extension of the active region is determined by the well thickness which typically is in the range of 100 nm. The carrier confinement in double-heterostructure p-n- junctions dramatically decreases the required current for laser operation and thus enables room-temperature operation with a few 10's of mA operation current. Moreover, the layer sequence in the double heterostructure also constitutes a refractive index profile acting as a transversal waveguide for the propagating laser light. Thus, the heterostructure not only provides carrier but also photon confinement. In so-called quantum well structures, the well thickness is typically below 10 nm such that quantum effects come into play as discussed in Sect. 23.1.1. In that case, carrier and photon confinement have to be handled separately (see Sect. 23.3).

Modern diode laser structures typically contain more complex layer sequences [1]. Some examples are discussed in Sect. 23.3 (Materials and architectures).

23.1.3 Resonator

Besides the gain medium, one also needs optical feedback to initiate and sustain laser action. In most configurations, this feedback is provided by a resonator (or optical cavity) which should be considered an integral part of the diode laser structure.

Since many of the materials used for semiconductor lasers, such as GaAs, have a high refractive index of about 3.5, the interface between semiconductor and air provides a reflectivity around 32%. Hence, the easiest realization of an optical cavity is a Fabry-Perot type resonator achieved by cleaving the semiconductor crystal such that the facets act as plane parallel mirrors. To check if 32% reflectivity is sufficient for laser operation, we look at the gain-loss conditions. The gain needed for laser operation (threshold gain g_{th}) can be estimated by balancing gain and loss for each roundtrip of the light in the cavity. The result is:

$$g_{th} = b_I - 1/2L \ \ln (R_1 R_2)$$

where b_I denotes the internal losses, L is the cavity length and R_1 and R_2 are the facet reflectivities. The internal losses combine radiative losses due to spontaneous emission not into the laser mode, Auger losses due to carrier recombination where the excess energy is not transferred to a photon but rather used to excite another carrier into a higher band, as well as losses due to defects, imperfections, etc. Typical cavity lengths are in the range from a few hundred micrometers up to a few millimeters and, for cleaved facets, $R_1 = R_2 = 0.32$. To modify these values, one may apply high reflection coatings (increased R) or antireflection coatings (decreases R).

In order to allow for stationary laser operation, the resonator feedback provided at each roundtrip of the light in the cavity has to be in phase. This means that stable operation can only occur for selected wavelengths λ for which the optical cavity length L fulfills:

$$nL = m\,\lambda/2 \text{ with the refractive index } n \text{ and } m = 1, 2, 3, \ldots$$

These selected wavelengths are called *resonator modes*. In the frequency domain, the eigenfrequencies are defined by

$$\nu_m = m\, c/2nL$$

which corresponds to an equidistant comb of modes

Since the semiconductor gain spectrum is relatively wide, the inverted semiconductor medium provides optical gain not only for one photon energy or wavelength but for a rather broad wavelength range. Generally, laser operation starts as soon as the gain overcomes the losses at one of the resonator modes. Since a semiconductor gain spectrum is rather flat on the scale of the intracavity mode separation, it happens frequently that the gain exceeds the losses for more than one mode. As a consequence, diode lasers with Fabry-Perot resonators often exhibit multi-mode emission behavior. Since such a multi-mode operation is undesirable for certain applications, one has developed concepts such as external cavity configurations, distributed feedback (DFB), or distributed Bragg reflector (DBR) scenarios [1].

For external cavity configurations, usually one of the diode laser facets is antireflection coated. The light output from this facet is then collimated with a collimation lens and coupled to an external resonator. To enforce single mode operation with narrow linewidth, this resonator includes a diffraction grating for wavelength selective feedback. Whereas this may be arranged in different ways, most commonly one utilizes the Littrow- or Littman geometries.

In the Littrow configuration, the light coupled out of the antireflection coated facet is directed onto the grating and the first diffraction order is redirected into the diode. One may tilt the grating to tune the feedback wavelength and thus the emission wavelength of the laser. However, usually the 0th order beam, i.e., the reflection from the grating, is used as the laser output. For the Littrow geometry, the direction of the output changes with tuning which is uncomfortable for applications. In contrast, in the Littman geometry, the first order diffracted beam is directed onto a mirror and the tilting of this mirror provides the tuning. In that case, the direction of the 0th order output beam remains stable. External resonator diode lasers with Littrow and Littman geometry provide tunable single mode emission with linewidths in the kHz range. Thus, they are attractive sources for spectroscopy applications.

Applications in optical data transmission require stable single mode emission even under modulation. External cavity configurations are too complex for these applications and therefore, alternative feedback concepts have been developed and implemented. These are based on so-called distributed feedback. The fundamental principle of distributed feedback is a periodic modulation of the refractive index in the laser diode. When, for a certain design wavelength λ_0, the periodicity of the refractive index modulation is $\lambda_0/4$, the partial waves reflected from this refractive index modulation add up constructively.

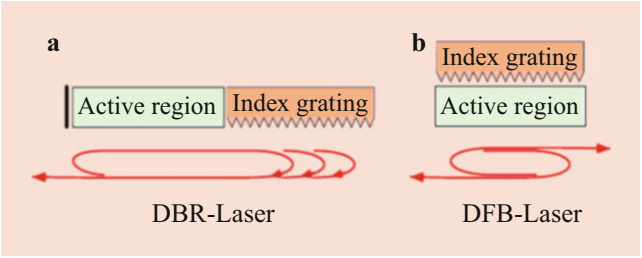

Fig. 23.5 (**a**) DBR-Laser, (**b**) DFB-Laser. Green areas: active regions, orange areas: structured refractive index [15]

The explicit reflectivity spectrum and the mode structure of such DFB lasers are usually calculated with the help of coupled mode theory. For a standard DFB laser, the structured refractive index extends over the entire device length as shown in Fig. 23.5b. Typically, both facets of the device are antireflection coated in order to suppress feedback from the facets. For this geometry, coupled mode theory predicts the emission of two modes separated by the so-called stop band. These two modes are of the same strength in the ideal case. In reality, residual reflections from the facets often disturb the system and lead to the desired single mode operation. However, in order to achieve a well determined single mode emission, a distortion of the periodicity is implemented in the form of an intentional $\lambda/4$ phase shift. For that case, coupled mode theory predicts one single mode in the center of the stop band.

A DBR laser as shown in Fig. 23.5a is a possible alternative to a DFB laser. In such a DBR laser, distributed Bragg reflection areas and gain areas are separated from each other. Such DBR lasers also provide single mode emission. They enable wavelength tuning but they also introduce higher technological effort in production as compared to DFB lasers.

23.2 Technical Properties

23.2.1 Introduction

Due to their specific architecture, semiconductor lasers have many properties which are different from other lasers. Besides the favorable aspects such as the compact dimensions and low price of laser diodes, there are unfavorable features including their relatively low output power and relatively poor beam profile. We discuss some of these aspects in the following sections and analyze their physical background. Further details can be found in Sze [18], Chuang [4], Bhattacharya [1].

23.2.2 Fundamental Behavior

Most commercial semiconductor lasers except for vertical external cavity surface emitting lasers and quantum cascade lasers (see Chap. ▶3) are electrically pumped via a p-n-junction. Their operation requires currents of a few *mA* at voltages of a few *V*. Current and voltage are related via the Shockley relation for a semiconductor diode. When the output intensity is recorded as a function of current one obtains the following characteristic behavior: For currents lower than the threshold current I_{th}, there is no laser operation. The laser diode emits spontaneous emission which is spectrally broad and often modulated by the Fabry-Perot modes of the cavity. When reaching the threshold current, the gain compensates the losses and lasing starts. The emission spectrally narrows down to one or a few modes. Further increasing the current above the threshold leads to an ideally linear increase of the emitted light intensity. The slope of the curve in that regime determines the internal or differential quantum efficiency $\eta_{diff} = \frac{e}{h\nu}\frac{\partial P_{opt}}{\partial I}$ with the electron charge e, Planck's constant h and the frequency ν. The external quantum efficiency is $\eta_{ext} = \eta_{diff}\frac{E_g[I-I_{th}]}{I^2eR+IE_g}$ where E_g is band gap energy and the series resistance of the diode is denoted by R. Here, one considers the ratio between emitted optical power and invested electrical power. In real devices, external quantum efficiencies above 50% can be achieved rendering laser diodes by far as the most efficient laser systems.

23.2.3 Dynamics

The dynamical behavior of laser diodes is governed by the coupled charge carrier – photon system. This coupled carrier-photon system has an intrinsic eigenfrequency which is called relaxation oscillation frequency ω_r. Using simple rate equations, the relaxation frequency can be derived as

$$\omega_r \approx \sqrt{\frac{a v_{gr}\ \rho_{av}}{\tau_{ph}}}$$

where a is the differential gain, i.e., the derivative of the gain with respect to the carrier density. This differential gain is a material property depending on the active material. The other parameters are the group velocity v_{gr}, the average photon density ρ_{av}, which is proportional to the average emitted power and the photon density τ_{ph} [1].

The laser reacts to perturbations, such as a sudden switch-on or a rapid change in operating conditions, with a damped relaxation oscillation. In practical applications, this feature may be utilized for the generation of short optical pulses. The concept is to use short (a few hundred picoseconds) current pulses in order to start relaxation oscillations, but make the current pulse sufficiently short such that only the first spike of the relaxations is emitted. This approach, which is called gain switching, may provide pulses as short as a few tens of picoseconds at a repetition rate determined by the sequence of the driving current pulses. Unfortunately, however, the generated pulse sequences usually exhibit a high temporal jitter since each pulse starts statistically independent from spontaneous emission. Shorter pulses with less timing jitter can be obtained by mode locking [5, 8], which will be mentioned later in this article in the context of microcavity laser systems.

The modulation response of a diode laser shows a strong resonance at ω_r and drops with ω^2 for higher frequencies. The maximum modulation frequency is thus determined by the relaxation oscillation frequency and can become only slightly higher than this value. Due to the intrinsic limits given by the parameters that determine ω_r, the best results obtained so far are somewhat below 50 GHz. The differential gain can be optimized by band structure engineering, for example by using strained quantum wells in the active region. The photon lifetime cannot be reduced too far as that would also decrease the cavity quality. Finally, the average intensity, respectively, the photon density $\rho_{av,}$ is typically chosen as high as possible but is limited by the maximum emission of the laser. So no further dramatic increase of ω_r and thus of the maximum intensity modulation frequency can be expected.

23.2.4 Spectral Properties and Coherence

As mentioned above, edge emitting diode lasers with Fabry-Perot cavities tend to emit on multiple longitudinal modes. The width of the emission spectrum is directly linked to the coherence properties of the emitted light. For multimode lasers, typical values of the coherence length, $l_c = c/\Delta\nu$, are in the range of a few hundred micrometers. While for some applications, this may be advantageous, for example to avoid speckle patterns in imaging, in many cases higher coherence or narrower spectral linewidth is desired. This can be achieved with DFB or DBR lasers which enable single mode emission even under strong modulation.

A simple rate equation analysis shows that in the case of single-mode emission, the semiconductor-laser linewidth is determined by a modified Schawlow-Townes formula [17]:

$$\Delta\nu = \frac{\beta}{4\pi\tau_{ph}\left(\frac{I}{I_{th}}-1\right)}\left(1+\alpha^2\right)$$

The standard Schawlow-Townes formula describes the linewidth of a laser governed by the spontaneous emission coupling β, the photon lifetime τ_{ph}, and the intensity. The spontaneous emission factor quantifies the amount of spon-

taneous emission coupled into the lasing mode. The intensity is expressed here by the deviation of the current I from the threshold current I_{th}. The modified Schawlow-Townes formula for diode lasers includes the multiplies $(1 + \alpha)^2$ where the so-called linewidth enhancement factor α phenomenologically considers the strong coupling of real and imaginary parts of the refractive index in semiconductors. Typical values for α depend on the detailed operation conditions and vary between 0 and approximately 10. The typical linewidths for single mode emission are in the range of cm to m, but narrower linewidths down to the kHz range can be realized with external cavity configurations. Such systems have coherence lengths in range of tens of km.

23.2.5 Beam Quality

Typical diode lasers are very compact and their emission aperture is small and asymmetric. The thickness of the active region is only a fraction of a micrometer while its width depends on the detailed laser architecture. In so-called ridge waveguide lasers, the lateral mode dimension is confined to a few micrometers by a lateral refractive index profile. Thus, the laser operates in its fundamental lateral mode. But the small dimensions in lateral and transversal directions lead to diffraction which causes a large beam divergence. Due to the asymmetry, the divergence is different in transversal and lateral direction. Typical emission angles are >30° for the transversal and around 10° for the lateral direction. Moreover, the emission beam is astigmatic, i.e., the origins of the lateral and the transversal beam cones are at different positions. Consequently, the collimation of the diode laser emission is not trivial and requires either combinations of suitable cylindrical lenses or more complex collimators.

In contrast to ridge waveguide lasers, broad area lasers have no lateral mode confinement by a refractive index profile. Here, the lateral beam extension is determined by the current path through the device and can reach several hundred micrometers. Thus, the emitted power may be much higher than for ridge waveguide lasers with the drawback that the lateral mode profile becomes more complicated. In particular, this profile contains higher lateral modes and it may even split up in filaments with complex spatiotemporal dynamics. Thus, beam shaping of the broad area laser output is even more challenging than for ridge waveguide lasers. In fact, the beam quality of broad area lasers is often too poor for applications where well controlled laser beam or a diffraction limited laser spot is required.

23.2.6 Polarization

Diode lasers usually emit linearly polarized light with the laser architecture, its waveguide geometry and the active material as the polarization direction determining factors. Typically, the waveguide and mirror losses are a bit smaller for transversal electric (TE) polarization than for transversal magnetic (TM) polarization. Thus, for active media with isotropic gain, like bulk material in standard double heterostructures, the emission will be TE-polarized with the electric field oscillating in the plane perpendicular to the growth direction.

When the active region contains quantum wells, the polarization selection is more complex. The optical dipole selection rules that can be derived from a quantum mechanical analysis of the optical transitions in the semiconductor band structure, determine which transitions support which polarization [3]. The transition from conduction band to the heavy hole band, for example, supports only the TE polarization whereas the transition from the conduction band to the light hole band supports the TM polarization more than the TE polarization. For bulk active materials, heavy- and light hole bands are degenerate in the vicinity of the band edge. Therefore, both polarizations are equally supported and the gain is isotropic. In a quantum well, the degeneracy of light and heavy hole bands is lifted and the light hole band shifts away from the band edge. Thus, the optical transitions take place between conduction band and heavy hole band and the TE-polarization dominates.

As discussed in Sect. 23.1.1, strain can be introduced if the lattice constant of the quantum well material is chosen to be slightly different from the surrounding barrier material. This strain has an influence on the band structure by shifting the relative positions of light – and heavy-hole bands. Typically, for tensile strain, the light-hole band shifts up in energy with respect to the heavy-hole band and may become the dominant band for optical transitions. Then, the dominant emission is TM polarized. So, diode lasers with tensile strain in the quantum wells emit TM polarized light when the amount of strain is strong enough. A clever material design with strained quantum wells may be implemented to create equal TE and TM gain for polarization insensitive semiconductor optical amplifiers (for more details see, e.g., [3])

For other quantum structures like quantum wires or quantum dots, the optical selection rules and thus the polarization properties of the gain depend on the geometry of the structure. The optical selection rules have to be determined for the specific design in order to predict the polarization of the emission.

23.2.7 Optical Power

The optical output power of a laser diode strongly depends on its architecture. A standard ridge waveguide laser diode typically emits a few mW of average power. With optimized design even above 100 mW can be achieved with laterally

single mode emission. For higher powers in the W to kW range, other laser types have to be used. Broad area lasers, for example, provide much higher output power than ridge waveguide lasers but, as mentioned above, they yield a poor beam profile with multiple lateral modes. The same holds for laser bars which consist of groups of single emitters arranged in arrays in the lateral direction. To obtain high power with good mode profile, tapered amplifiers and lasers have been developed. They contain a ridge waveguide section and a tapered gain section in which the single lateral mode defined by the ridge waveguide section is smoothly expanded and dominantly maintains its lateral single mode structure.

23.2.8 Temperature Dependence

Many of the fundamental semiconductor laser properties are temperature dependent. Not only does the bandgap shrink in energy with increasing temperature but also the carrier distributions in the bands change with temperature according to the quasi-Fermi distribution functions. Both the bandgap variation and the varying carrier distribution influence real and imaginary part of the susceptibility, i.e., the gain and refractive index of the diode laser material. With increasing temperature, the gain is generally reduced and spectrally shifted to lower energies. At the same time, the variation of the refractive index varies the optical length of the cavity and thus the spectral position of the cavity modes. Consequently, the most important laser specifications degrade with increasing temperature. The laser threshold increases and the quantum efficiency decreases due to the reduced gain and stronger non-radiative recombination processes. Thus, at higher temperature, the achievable output power is lower even if higher current is injected. Since the Ohmic heating contributes to the temperature increase, a thermal rollover may occur where the output power decreases with increasing current. Thus, it is important to provide the laser diode with an efficient heat sink and, even better, with an active cooling via a thermoelectric cooler. The increase of the laser threshold with temperature can be empirically described by a characteristic temperature T_0 according to: $I_{th}(T) = I_{th,0} \exp(T/T_0)$. The characteristic temperature T_0 is a device specific quantity and typically ranges between 50 and 300 K.

The spectral laser properties are influenced in a more complicated way due to the change of both gain and refractive index with temperature. The refractive index modification induces a change in the optical cavity length. Thus the spectral position of the laser modes shifts with temperature. Since also the spectral position of the gain maximum is temperature dependent, the mode competition is modified and different modes may become dominant for different temperature conditions. These changes may lead to so-called mode hops which are difficult to predict and to control.

23.3 Materials and Architectures

23.3.1 Semiconductor Materials

As pointed out in Sect. 23.1.1, semiconductor lasers require direct bandgap semiconductors with excellent material quality. This imposes severe restrictions to the choice of possible materials for semiconductor laser devices. Furthermore, a high material quality is crucial because defects due to dislocations or impurities induce non-radiative recombination channels and thus reduce the lasing efficiency. As a consequence, a high crystal quality is required which is achieved by growing the semiconductor devices by modern epitaxial techniques such as molecular beam epitaxy (MBE) or metal organic vapor phase epitaxy (MOVPE) onto high quality substrate crystals that define the structure of the crystal. To avoid dislocations, the lattice constant of all layers grown within the device structure should not differ too much from the lattice constant of the substrate material which imposes further restrictions to the selection of suitable semiconductor compounds.

In general, the bandgap energy of the active region roughly determines the spectral range of the emission that can be achieved with the laser. This bandgap energy can be varied in alloys as, for example, $(Ga_xIn_{1-x})(As_yP_{1-y})$, by changing the percentages of the material composition. To obtain an overview of realizable laser material combinations, it is helpful to create a diagram in which the band gap energy is plotted versus the lattice constant for the relevant materials and alloys. Then, strategies can be extracted how to achieve a defined bandgap energy with a material alloy whose lattice constant is compatible with a certain substrate (e.g., GaAs, InP, or GaN). An example of such a material map is shown in Fig. 23.6.

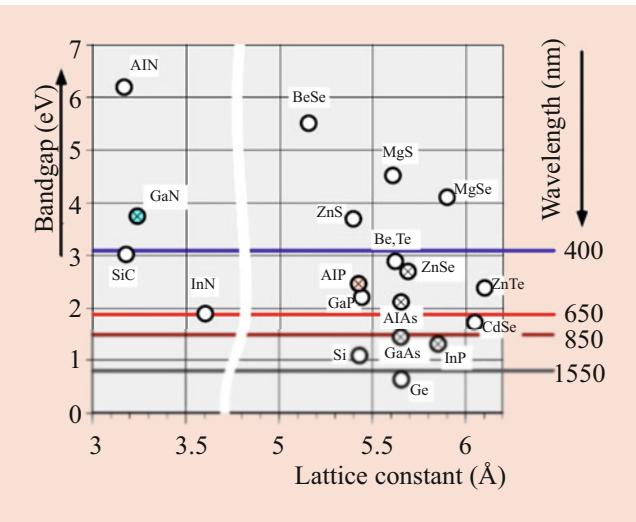

Fig. 23.6 Material map, bandgap energy as a function of lattice constant [15]

Many different material systems have been developed for specific emission wavelengths and applications. The most important examples are GaAs/$Al_xGa_{1-x}As$ heterostructures on GaAs substrates, $(Ga_xIn_{1-x})(As_yP_{1-y})$, heterostructures on InP substrates, and (AlGaIn)N heterostructures on GaN substrates, respectively. In a way, GaAs/$Al_xGa_{1-x}As$ heterostructures on a GaAs substrate serve as a model system since the first semiconductor lasers were developed using these materials. This material system is particularly attractive since the lattice constant of GaAs and AlAs is almost equal so that alloys with a lattice constant compatible with that of GaAs can be produced that cover the near infrared range around 800 nm. The only important restriction is that $Al_xGa_{1-x}As$ becomes indirect for $x > 0.4$. The material $(Ga_xIn_{1-x})(As_yP_{1-y})$ on InP substrate is the most prominent choice for lasers operating in the telecommunication range defined by the fiber windows at 1300 nm and 1550 nm. The (AlGaIn)N – based materials emit in the violet to green spectral range and were developed for blue ray DVD optical storage.

From the material map, it becomes obvious that there is a spectral range in the visible regime for which so far no diode lasers are available. Hence, the realization of yellow or orange emitting semiconductor diode lasers may be one of the major challenges for the future. An even more challenging problem is to realize diode laser structures that are compatible with Si technology, for example CMOS (complementary metal-oxide semiconductor) architectures. This is the basis of modern electronic circuits and there is a growing demand to include optical functionalities onto electronic systems. But, unfortunately, Si is an indirect semiconductor, and no direct semiconductor materials compatible with the lattice constant of Si have been available. Accordingly, the fusion of electronic and optoelectronic circuits to OEICs (optoelectronic integrated circuits) induces major technological effort. However, material research is continued and, for example, recently the direct semiconductor material Ga(NAsP) was developed [13] that may close this technological gap in the future.

23.3.2 Quantum Confinement Structures

As discussed above, semiconductor QW systems have a number of advantages for semiconductor laser applications over bulk materials. As a consequence of the carrier confinement, the threshold gain can be achieved with a much lower overall carrier density as compared to bulk material. Therefore, the threshold current is lower and the modulation speed is higher in QW lasers as compared to bulk heterostructure lasers of the same material. In addition, a certain amount of band structure engineering is possible due to the quantization effects and by introducing small controlled amount of strain to the active layer.

An additional important aspect to be considered in QW laser design is that the small QW width reduced the overlap of the active region with the optical mode and the waveguiding properties. To ensure sufficient optical waveguiding, a further larger scale band structure variation, the so-called separate confinement, has to be introduced.

Besides semiconductor QWs, also other quantum confined semiconductor configurations are used as gain media in modern semiconductor lasers. They provide even higher degrees of quantum confinement than QWs; however, they are more difficult to produce in homogeneous ensembles. Most noteworthy in this context are the so-called semiconductor quantum wire and quantum dots (QD) systems. As QDs, one commonly denotes structures where the excited carrier mobility is restricted in all three spatial dimensions. Hence, instead of the one-dimensional barriers in QWs, one imposes fully three dimensional quantum confinement leading to a particle-in-a-box, respectively particles in a sphere configuration. Quantum wires are somewhat in between QWs and QDs in the sense that they provide quantum confinement in two dimensions, leaving one unconfined degree of mobility.

One consequence of the full confinement in QDs is the discretization of the allowed energy states resembling the situation in atomic systems. Ideally, this would modify the spectrally continuous absorption/gain of usual semiconductors into a set of discrete resonances whose spectral position scales inversely with the square of the QD extension. However, in order to realize spectrally separated absorption/gain peaks in QD ensembles, on needs a high degree of size uniformity since any size variation immediately leads to pronounced inhomogeneous broadening.

Current technology allows for the growth of wire and QD structures with various degrees of precision. Lasers devices utilizing these quantum confined systems have been developed and overall desirable properties have been identified [2]. However, it remains to be seen if these systems will be able to outperform to successful commercial QW laser devices.

23.3.3 Quantum Cascade Lasers

While standard diode lasers are available for many spectral regions in the visible and near infrared regime, the realization of mid-infrared or far infrared lasers becomes challenging, in particular because the Auger losses in narrow-gap semiconductor systems are dramatically increased in comparison to, e.g., GaAs-based materials. Therefore, alternative concepts have been introduced that are based on intraband optical transitions within the conduction band instead of interband transitions between conduction and valence band. The fundamental idea is to use transitions between different quantized states in QWs. The energy splitting of these states can be well tailored by the QW geometry. However, to achieve

inversion in such structures is somewhat challenging. While the lifetime for interband transitions is of the order of a nanosecond, the lifetime in an higher QW state is only of the order of a picosecond. Thus, without further effort, it would not be possible to accumulate carriers in the upper state to achieve inversion. One fundamental achievement in the realization of quantum cascade lasers is to reduce the lower state lifetime to about 0.1 picoseconds by a resonant tunneling process into an adjacent quantum well. This may even be arranged in a way that the resonant state in the adjacent well is the upper laser level in this well. In this way, many QWs may be arranged in series and the injected electrons follow a cascade process though this series. This quantum cascade process provides multiple photons for each injected electron and increases the efficiency of quantum cascade lasers. Such quantum cascade lasers are unipolar lasers, i.e., they work with electrons injected by an applied electric field only. Their realization is challenging since practical devices contain hundreds of individual layers. After their first realization in 1994 by Capasso et al., quantum cascade lasers have been further developed to become very useful systems for spectroscopic applications like trace gas analysis in the mid infrared. The emitted power for these lasers is in the *mW* regime and they operate with moderate currents at room temperature.

Quantum cascade lasers for longer wavelengths or lower frequencies down to the THz-range are much more difficult to realize. THz quantum cascade lasers still only work at cryogenic temperatures, and it is yet unclear whether room-temperature quantum cascade lasers at 1 THz will ever be realized. For further reading about quantum cascade lasers we refer to Faist [6].

23.3.4 Microcavity Lasers

As *microcavity lasers* , one often denotes very small semiconductor laser structures with dimensions in the range of a few times the wavelength of the emitted light. Nowadays, such systems can be routinely realized by systematically utilizing the advantages of epitaxial growth. As the first microcavity device, vertical-cavity surface-emitting lasers (VCSELs) (see Fig. 23.7) have been developed in the 1990s [16].

Generically, these VCSELs are Fabry-Perot type laser systems where distributed Bragg reflectors (DBRs) serve as the cavity end-mirrors. These DBRs consist of a series of layers with different refractive index, where each layer has the optical thickness of a quarter of the emission wavelength. In VCSELs, the DBRs are epitaxially grown using semiconductor material combinations with sufficiently different refractive index such as GaAs and $Al_xGa_{1-x}As$.

During the growth process, the gain medium is deposited on top of the first DBR in the form of one or more QWs with proper barriers and spacer layers, followed by the second DBR needed to complete the Fabry-Perot cavity. The total thickness of the QWs together with the barriers and spacer layers defines the cavity length, which is on the order of a few times half the emission wavelength in typical VCSELS.

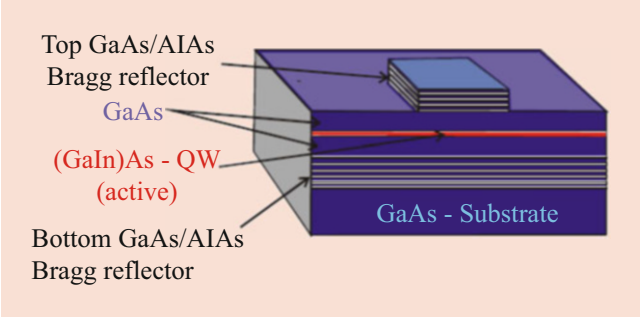

Fig. 23.7 Schematic geometry of a VCSEL

Under operation conditions, the light is emitted parallel to the growth direction such that the lasing occurs out of the surface of the epitaxial heterostructure. As a consequence of the relatively small number of QWs in the gain region, the light circulating in the cavity experiences only weak round-trip amplification. This gain has to exceed the losses in order for lasing to occur, such that very high mirror reflectivities are needed which are typically in the range of 99% or more in most configurations. Luckily, such high reflectivities can routinely be realized with semiconductor DBRs having on the order of 20 or more layer pairs.

For most practical applications of VCSELS, it is desirable to generate the needed carrier inversion in the gain QWs via electrical pumping. Thus, it is necessary to implement a p-n-junction into the overall design and to develop strategies for effectively injecting charge carriers into the active region. As a consequence, such electrically pumped VCSEL structures have an even more complex architecture than the schematic structure shown in Fig. 23.7.

Taking advantage of the small microcavity dimensions, one can design VCSEL systems such that only one longitudinal mode is amplified by the gain QWs. As a consequence, these microlasers are well suited to realize single-mode output characteristics. Another desirable feature for practical applications of VCSELS is that one can engineer a round aperture for light emission with a diameter of a few micrometers so that diffraction is weak and the beam profile is almost perfectly circular.

A further development based on the successful VCSEL concept is the so-called VECSEL (Vertical External Cavity Surface Emitting Laser) [12]. In these systems, one of the DBRs is replaced by an external outcoupling mirror. See Fig. 23.8 for an example of the schematic VECSEL design.

The single remaining DBR plus the gain QWs grown on top of it constitute the “active mirror,” i.e., the VECSEL chip.

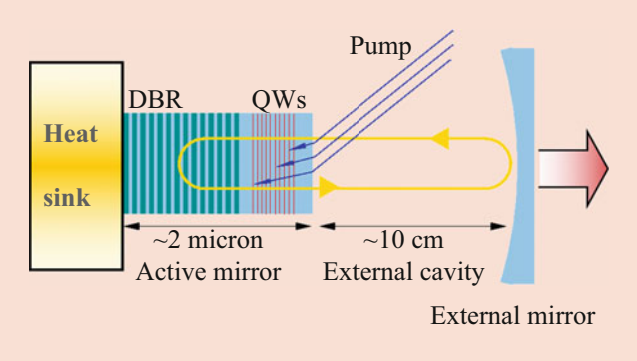

Fig. 23.8 Schematic layout of a VECSEL device showing the QW structure grown on a distributed Bragg reflector (DBR) mirror stack consisting of quarter-wave-length thick layers of alternating semiconductor materials with high and low refractive index. Together, the DBR and the quantum wells constitute an "active mirror". The spacing between the typically 8–12 quantum wells is chosen to match half the wave length of the desired laser emission, constituting the resonantly periodic gain medium. The structure is pumped using external optical sources. Lasing is achieved by using an external high-reflectivity (out coupling) mirror to form a closed cavity. The generated heat is removed by a heat sink typically consisting of a diamond heat-spreader on a copper block

The laser cavity is completed by a high-reflectivity external mirror, which is also used for the outcoupling of the laser emission. The VECSEL chip is mounted on a heat sink which typically consists of a diamond heat spreader on top of a copper block. The QWs are optically pumped using commercially available high-power pump sources. Figure 23.8 shows a simple generic VECSEL layout. Besides the depicted linear cavity arrangement, also more elaborate geometries with so-called V-cavities or even more complicated configurations are in practical use.

A wide variety of semiconductor materials can be used as the VECSEL gain medium allowing for lasing at many desirable wavelengths. Since the total VECSEL cavity can easily have an extension in the range of many centimeters, there is sufficient space to incorporate additional elements. One example are suitable nonlinear crystals that allow for intracavity frequency up-conversion which significantly extends the wavelength range of VECSEL emission, well into the visible and even UV.

Generally, in VECSELs, the emission intensity scales with the pumped area such that high-power performance is possible. For this application, one epitaxially grows the different QWs in the gain medium in a particular spatial arrangement, referred to as RPG (resonant periodic gain) configuration. Here, the center-to-center distance between the wells is precisely half the wavelength of the emitted light. Under this condition, the contributions from the individual QWs are all in phase and maximize the total output of the device for this particular wavelength. Using RPG VECSEL configurations, multi-mode output in excess of 100 W CW (continuous wave) and single mode emission of more than 20 W CW has been reported [19].

In addition to the application as bright source for CW emission, VECSELs can also be used for ultra-short pulse generation. Here, one typically utilizes the concept of passive mode locking by replacing the high-reflectivity outcoupling mirror by a SESAM (semiconductor saturable absorption mirror). The SESAM introduces an additional loss into the cavity, which is relatively large for low intensities but is gradually saturated with increasing intracavity field strength. This favors the build-up of short pulses because the high intensity at the pulse peak saturates the absorber more efficiently than its low intensity wings.

SESAM mode locking in VECSELs with RPG gain configurations has been demonstrated and ultrashort pulses with durations in the 100 fs regime have been generated. Recently, it has been realized that the spatial arrangement of the gain QWs can be optimized to achieve even shorter pulse durations [10]. Whereas first demonstrations yielded pulses with FWHM of 95 fs, the full potential of this new concept has not yet been exploited, mainly due to technical difficulties with pulse induced SESAM degradation and proper management of the group delay dispersion. Hence, this field is still an area of active current research.

23.4 Applications and Outlook

23.4.1 Applications

As already mentioned throughout this article, semiconductor lasers are attractive for numerous applications due to their specific properties including their compact dimensions, high efficiency, low price and the enormous flexibility to adapt their design for the specific application. It is almost impossible to list all semiconductor laser applications. They include, for example, laser pointers, laser printers, barcode scanners, metrology systems for measuring distance or speed, light detection and ranging (LIDAR), biomedical imaging, display technology (e.g., laser TV), optical data storage, optical data transmission, material processing, and many others. In the following, we discuss three important applications and point out the corresponding challenges for the device development.

For optical storage on compact discs (CDs) or digital versatile discs (DVDs), a good beam quality is required. To read out the tiny bits and lands on a CD or DVD, the laser spot has to be focused to a spot as small as possible. The diffraction limited spot size scales with the wavelength. Accordingly, much more date can be stored on a blue ray DVD which is read out at 405 nm than on a CD which is read out at 780 nm. This was the major driving force for the development of (AlGaIn)N lasers emitting in the blue-violet spectral range. This development was accompanied with many challenges

but has finally led to the nowadays commercially available blue lasers with extremely long lifetimes.

The internet is based on optical data transmission via glass fibers. Here, high speed modulated diode lasers are the key elements needed for sending the optical data streams. These lasers have to be adapted to the fiber properties, most importantly they should emit at the fiber window of 1550 nm. This is realized with lasers based on the $(Ga_xIn_{1-x})(As_yP_{1-y})$ material system grown on InP substrates. These lasers should emit a good beam profile to enable coupling into single mode optical fibers. This is usually realized with the help of lateral waveguiding via ridge structures.

To achieve high transmission rates, the lasers should enable fast modulation. The maximum modulation frequency is limited by the relaxation oscillation frequency to the range below 50 GHz. Material engineering is used to optimize the lasers for such high frequencies. For advanced wavelength division multiplexing, it is necessary that the lasers operate in one longitudinal mode at a well-defined wavelength. This is commonly achieved using DFB lasers.

For high power applications, completely different optimization schemes are performed. In those cases, usually the spectral quality of the emission is not crucial and multimode emission can be tolerated. The most straight forward approach to increase the output power is to scale up the emission surface in broad area lasers. Thus, power levels in the few W range become accessible. Even higher power levels are accessible with diode laser arrays. Such arrays enable output powers up to the kW range as they are required for material processing applications like, for example, laser welding.

23.4.2 Outlook

Nowadays semiconductor lasers are essential tools for our communication society. Most important, they are fundamental components for the internet data traffic. As the internet traffic is continuously growing, there is an ongoing demand for faster lasers and high modulation bandwidths. Since fundamental limits of the current technology will be reached soon, there is need for new concepts as, for example ultrafast spin lasers in which the polarization state of the light is modulated instead of the intensity [14].

Since optical communication will play a major role also for short range interconnects, potentially even between and inside chip, there is a big demand for the combination of electronic and optoelectronic devices into optoelectronic-electronic integrated circuits (OEICs). This is a challenge because electronic systems are based on silicon technology and optoelectronic systems are based on III-V-semiconductor technology. Unfortunately, common III-V laser materials have lattice constants differing strongly from that of silicon. Thus, the combination of both within OEICs is technologically challenging and primarily requires major breakthroughs in the development of semiconductor lasers compatible with silicon technology. While wafer fusion of silicon and III-V-based devices is a technologically demanding approach, new material systems as, for example, the direct semiconductor Ga(NAsP) [13], are developed that may be integrated into silicon technology due to their suitable lattice constant.

Another research field is the realization of better lasers for the visible range. While red, blue and green lasers are available, yellow and orange diode lasers still have to be developed. Such lasers would be extremely interesting for display applications, for example for compact laser television systems.

Laser diodes with higher output power are interesting for material processing applications. Due to the high efficiency of diode lasers, it is extremely attractive to replace larger solid state or CO_2 lasers in such applications, when sufficient output power is available.

A further area still awaiting a major breakthrough is the realization of room-temperature semiconductor lasers emitting in the regime of 1 THz. They would be extremely interesting for material sensing or free space THz communication systems.

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Part III

New-Generation Devices and Architectures

Heterojunction Tunnel Field-Effect Transistors

24

Paolo Paletti and Alan Seabaugh

Contents

24.1 Introduction 867
24.2 Tunnel FET Operation Principles 869
24.3 Band-to-Band Tunneling 870
24.4 Subthreshold Swing 872
24.5 ON Current 875
24.6 OFF Current 879
24.7 Output Characteristics 883
24.8 Ambipolar Conduction 885
24.9 Heterojunction Tunnel FETs 885
24.9.1 Vertical Heterojunction TFET 887
24.9.2 Lateral Heterojunction TFET 888
24.9.3 Vertical Nanowire HTFET 889
24.9.4 Layered Two-Dimensional HTFET 890
24.9.5 III-Nitride HTFETs 891
24.10 Band Tails 893
24.11 Composite TFET/MOSFET 896
24.12 Complex Gate Dielectrics 897
24.13 Technology Benchmarks 897
24.14 Summary and Concluding Remarks 899
References 899

Abstract

The tunnel field-effect transistor (TFET) relies on interband tunneling to achieve subthreshold swing below the 60 mV/dec fundamental limit at room temperature of bipolar and field-effect transistors. Since the first successful demonstration of a subthermionic TFET in 2004, research efforts have been devoted to the study and engineering of TFETs for low-power and energy-efficient integrated circuit applications. Starting from band-to-band tunneling theory, this chapter aims to give a comprehensive overview of the TFET and its principles of operation. This sets the stage for understanding electrical characteristics, design trade-offs, critical challenges, and source of nonidealities. In light of the physical challenges, the benefits of adopting a heterojunction device architecture are presented. After about 15 years of intense research and steady progress across a plethora of materials systems, spanning from group IV materials, such as Si, to III–V compounds, to two-dimensional materials and mixed-dimensional heterostructures, as well as through different device architectures, an updated benchmark of best reported TFETs is provided to benchmark the state of the art across materials systems.

Keywords

Tunnel field-effect transistors · Heterojunction · Band-to-band tunneling · Subthreshold swing · Steep-slope devices

24.1 Introduction

The relentless and persevering scaling of the silicon metal oxide semiconductor field-effect transistor (MOSFET), the building block of almost every electronic system, has been geared by an ever-increasing demand for denser, higher-performance, and more energy-efficient integrated circuits (ICs). For more than five decades, as predicted by Gordon Moore in 1965 [1, 2], semiconductor manufacturers have succeeded in exponentially increasing the number of transistors per chip at a factor of 2× every 2 years. This incredible engineering quest can be divided into two eras: the "geometrical scaling" era, spanning nearly 30 years from 1974 until the

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early 2000s, followed by the "effective scaling" era that we are now witnessing, which is around its midpoint. A third era of "hyper-scaling" is unfolding [3].

The fundamental principles of "geometrical scaling" were first laid out by Dennard in 1974 [4]. The design criteria are somewhat simple: simultaneously reduce the transistor length (L), width (W), oxide thickness (t_{OX}), and supply voltage (V_{DD}) by a factor k and increase the channel doping, N, by the same factor. With no penalty in terms of power density, the net result is constant improvement in cost (area), speed, and energy. Dennard scaling survived until the 130-nm node.

Due to limitations on oxide thickness scaling imposed by exponentially increasing leakage currents and impediments to supply voltage reduction as a consequence of nonideal electrostatics, the "effective scaling" era started around 2003 with the addition of distinct performance boosts such as strained silicon at the 90-nm node, high-κ dielectric and metal gate starting from the 45-nm node, and finally the adoption of a 3D multigate transistor architecture, the FinFET, at the 22-nm node. Despite all the technological advancements that have enabled the reduction of the minimum feature size from 50 μm, starting in 1965, to about 10 nm in today's leading technologies, Si MOSFETs operate under the same physical principle and suffer the same limitations.

In the simplest picture, an FET consists of two reservoirs of mobile charges, named source and drain, separated by the channel potential barrier whose shape and height can be modulated upon the application of a proper bias at the gate electrode. The gate is insulated from the semiconductor channel by a gate oxide. For digital applications, the MOSFET is designed to behave like an electronic switch, transitioning an insulating (OFF) state for V_{GS} below a certain threshold voltage (V_T) to a highly conductive (ON) state for V_{GS} greater than V_T. A typical semilogarithmic plot of the drain current vs. gate voltage, I_D–V_{GS}, characteristic of an n-channel MOSFET is shown in Fig. 24.1a. In the subthreshold regime, $V_{GS} < V_T$, the drain current turns off exponentially, and its inverse slope is defined as the subthreshold swing (SS). Specifically, SS refers to the gate voltage required to change the drain current by one order of magnitude. In a MOSFET, the current governing mechanism is thermionic emission over an energy barrier (Fig. 24.1b), and this sets a fundamental limit on the minimum attainable SS due to the Maxwellian tails of the source Fermi-Dirac distribution given by [5]

$$\begin{aligned} SS &= \left(\frac{d\log_{10} I_D}{dV_{GS}}\right)^{-1} = \underbrace{\frac{dV_{GS}}{d\psi_S}}_{m}\underbrace{\frac{d\psi_S}{d\left(\log_{10} I_D\right)}}_{n} \\ &\cong \left(1+\frac{C_S}{C_{OX}}\right)\ln(10)\frac{k_B T}{q}. \end{aligned} \tag{24.1}$$

In the above equation, ψ_S is the channel electrostatic potential; C_S and C_{OX} are the semiconductor and oxide capacitances, respectively; k_B is the Boltzmann constant; T is the absolute temperature; and q is the electron charge. The brackets in Eq. (24.1) highlight the two different contributions to SS: m is the transistor body factor, and n is a term that identifies the underlying transport mechanism in the channel. The SS limit at room temperature imposed by

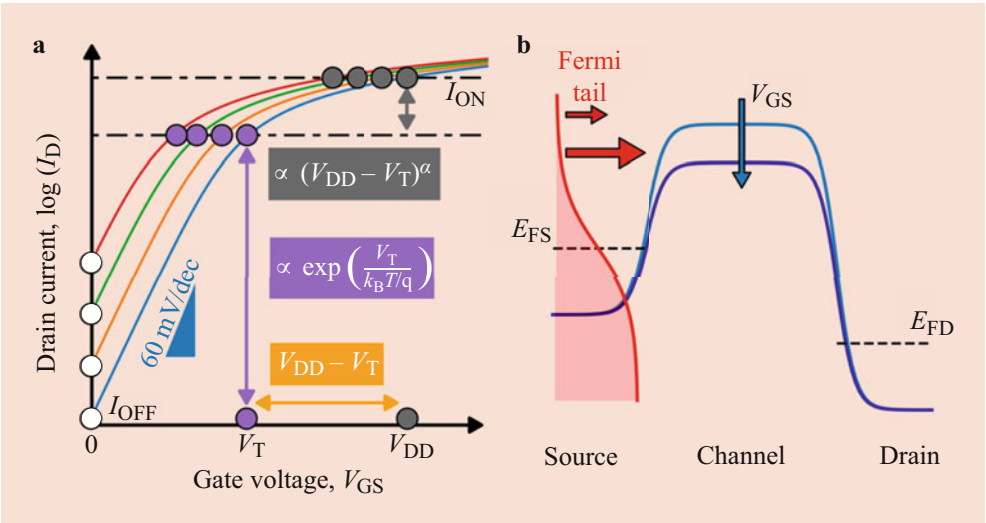

Fig. 24.1 (**a**) MOSFET transfer characteristics. The simultaneous scaling down of both the supply voltage (V_{DD}) and the threshold voltage (V_T) to meet the ON-state current requirement (I_{ON}) leads to an exponential increase in the OFF-state current (I_{OFF}). (**b**) Energy band diagram showing the conduction band with Fermi levels in the source and drain labeled E_{FS} and E_{FD}, respectively. The current governing mechanism in a MOSFET is thermionic emission over the channel potential barrier. In the subthreshold regime, the Fermi tail limits the subthreshold swing (SS) to the fundamental limit of 60 mV/dec at room temperature

thermionic emission is equal to 60 mV/dec. Figure 24.1a indicates that a reduction of V_T will translate into an exponential increase in I_{OFF}, and as a consequence, static power increases, $P_S = V_{DD}\ I_{OFF}$. Therefore, a reduction of V_{DD} at matched overdrive cannot be achieved. Because of these fundamental limits, a third era of hyper-scaling is dawning, in which new physics, materials, and devices will be essential for meeting Moore's law requirements for next-generation computing devices.

24.2 Tunnel FET Operation Principles

The tunnel FET (TFET) is a transistor concept compatible with CMOS technology and able to overcome the 60 mV/dec MOSFET limit. In contrast to MOSFETs, TFETs rely on interband tunneling through a potential barrier [5–7]. In simple terms, the TFET is a gated reverse-biased p-i-n diode. Figure 24.2a exemplifies the archetype of an n-type TFET; it consists of a p^+ source and an n^+ drain, connected with a fully gated intrinsic channel. Structurally, the peculiar feature of a TFET is the asymmetric doping of the drain and source with respect to a conventional MOSFET. The corresponding band diagrams of an nTFET transitioning from the OFF to the ON state are shown in Fig. 24.2b under positive V_{DS} bias. As in a backward diode, the interband overlap of the source and channel regions enables the conduction of carriers by means of band-to-band tunneling (BTBT) (Zener tunneling). However, in the OFF state, the band gap in the channel acts as an energy filter, cutting off the availability of states for tunneling. As a consequence, I_{OFF} in a TFET results ideally only from thermionic emission above a barrier approximately equal to the energy band gap, E_G. Other processes that contribute to the OFF-state leakage currents are associated with Shockley-Read-Hall (SRH) generation and trap-assisted tunneling (TAT) [8], Auger generation [9], and direct source-to-drain tunneling at scaled channel lengths [10].

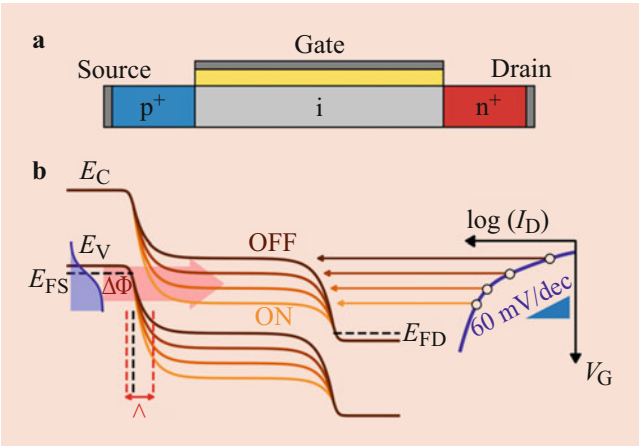

Fig. 24.2 (**a**) Schematic cross section of an n-type TFET. It consists of a p^+ source, a fully gated intrinsic channel, and an n^+ drain. (**b**) Energy band diagrams for different V_{GS} biases. Each band diagram corresponds to a specific point in the I_D–V_{GS} characteristic indicated in the right panel. The tunneling window is labeled $\Delta\Phi$, and Λ denotes the tunneling distance from source to drain; the conduction and valence band energies are E_C and E_V, respectively

Referring again to Fig. 24.2b, if a positive gate voltage is applied, the bands in the channel move to lower energies reaching a crossing point where the conduction band in the channel begins to overlap with the valence band in the source. This corresponds to the onset of BTBT where electrons tunnel from the source valence band into the channel through a tunneling width Λ. The tunneling probability is exponentially dependent on the tunneling distance. The BTBT generation processes can result either from direct transition between the maximum of the valence band and the minimum of the conduction band at the Γ-point or via a phonon-meditated indirect transition. The gate voltage plays a twofold role in the operation of a TFET. It modulates both the tunneling probability and the availability of states to tunnel into, within a tunneling window given by the interband overlap. These two contributions allow for two different mechanisms for realizing SS steeper than 60 mV/dec. Unlike the MOSFET where the slope of the I_D–V_{GS} transfer characteristic has a fixed swing in the subthreshold regime, the SS of a TFET is not constant but depends on V_{GS}. The key voltage defining the upper bound of this region is defined as V_{60}, the voltage at which the slope of the characteristic $d\log I_D/dV_{GS}$ is 60 mV/dec. The drain current at $V_{GS} = V_{60}$ is denoted I_{60}, which is a useful figure of merit, discussed in Sect. 24.4.

A short historical perspective of the discoveries that have led to the conceptualization and demonstration of the TFET begins with the theory of BTBT, i.e., "electrons passing from one band into another under the action of a constant electric field," written by Zener in 1934 [11] to explain electrical breakdown in solid dielectrics. Zener tunneling is the core transport mechanism in a TFET. It was not until 1958 with the pioneering work by Esaki [12] that BTBT manifested itself in the characteristic negative differential resistance (NDR) in the forward bias regime of a degenerately doped p^+n^+ Ge homojunction. A gated p-i-n device called the "surface channel tunnel junction," the prototype of the TFET, was reported by Quinn [13] in 1978 as a means to investigate subband splitting in quasi-2D systems. BTBT was then identified as the working principle in a trench transistor cell leading to a three-terminal planar MOS tunneling device proposed by Banerjee in 1987 [14]. In the early 2000s, several research groups highlighted that subthermal SS could be achieved in a tunneling transistor [15–18], and the first experimental demonstration of SS <60 mV/dec was demonstrated in a carbon nanotube TFET by Appenzeller [18]. The benefit of employing heterostructures in the optimization of TFETs' performance followed shortly afterward [19]. Since then,

TFETs have attracted significant research interest, and an amazing number of steep-slope devices have been proposed and reported exploiting different device architectures and materials systems [20]. The prior art leading to the TFET is further detailed by Ionescu and Riel [5] and Seabaugh and Zhang [6].

24.3 Band-to-Band Tunneling

In this section, a simple analytical theory is derived to lay out some general TFET design rules and to illustrate under what circumstances subthermal SS can be achieved. As illustrated in Fig. 24.2b, only carriers within the tunneling window $\Delta\phi = E_{V,S} - E_{C,CH}$ contribute to the transport, where $E_{V,S}$ is the valence band in the source region and $E_{C,CH}$ is the conduction band in the channel far away from the tunnel junction such that the bands can be considered flat. Using Landauer formalism [21], the drain current per unit width can be written as

$$I_D = \frac{2q}{h}\int_{E_{C,CH}}^{E_{V,S}} T_{BTBT}(E)\left[f_S(E) - f_D(E)\right] dE \tag{24.2}$$

where h is Planck's constant, $f_{S,D}(E)$ are the source and drain Fermi distribution functions, and $T_{BTBT}(E)$ is the BTBT tunneling probability. The direct BTBT probability can be evaluated analytically by means of the Wentzel-Kramers-Brillouin (WKB) approximation:

$$T_{BTBT} = \exp\left(-2\int_{x_1}^{x_2} k_X(x, E)\, dx\right) \tag{24.3}$$

where x_1 and x_2 are the classical turning points defining the tunneling path length and k_X is the imaginary wave vector obtained through the Kane two-band model [22, 23]. Assuming a triangular potential barrier at the source/channel interface, i.e., constant electric field over the tunneling path, the transmission probability can be written as [24]

$$T_{BTBT} = \exp\left(-\frac{4\Lambda\sqrt{2m^*}E_G^{3/2}}{3q\hbar(\Delta\phi + E_G)}\right) \tag{24.4}$$

In Eq. (24.4), Λ is the width of the transition region at the source/channel interface, i.e., the tunneling width, m^* is the reduced tunneling mass, $\hbar$ is the reduced Planck's constant, and E_G is the semiconductor energy gap. The reduced tunneling mass is often approximated $m^* = \left(1/m_e^* + 1/m_h^*\right)^{-1}$, which averages both the electron, m_e^*, and the hole, m_h^*, effective masses. The tunneling width is given by the sum of the depletion width in the source, W_D, and the scaling length of the gated region, λ, i.e., $\Lambda = W_D + \lambda$. The scaling length for double-gate TFETs has been discussed by Taur [25]. Equation (24.4) considers a semiconductor with a direct band gap such as InAs, where carriers tunnel from a single conduction band to a single valence band. In indirect semiconductors, e.g., Si and Ge, the WKB model breaks down due to the many interacting bands involved in the tunneling process [26]; however, the same general dependencies on Λ, m^*, and E_G are maintained. Substituting Eq. (24.4) back into Eq. (24.2), I_D can be rewritten as

$$\begin{aligned} I_D &= \frac{2q}{h}\exp\left(-\frac{4\Lambda\sqrt{2m^*}E_G^{3/2}}{3q\hbar(\Delta\phi + E_G)}\right)\int_{E_{C,CH}}^{E_{V,S}}\left[f_S(E) - f_D(E)\right] dE \\ &= \frac{2q}{h}T_{BTBT}F(\Delta\phi) \end{aligned} \tag{24.5}$$

Equation (24.5) indicates that the BTBT current is determined by both the transmission probability and the occupation functions at the two sides of the tunnel junction within the tunneling window. If we assume a drain-source bias large enough to suppress any back injection from the drain to the source, I_D simplifies to [27–29]

$$\begin{aligned} I_D &\approx \frac{2q}{h}T_{BTBT}k_BT\left[F_0\left(\frac{E_{FS} - E_{C,CH}}{k_BT}\right) - F_0\left(\frac{E_{FS} - E_{V,S}}{k_BT}\right)\right] \\ &= \frac{2q}{h}T_{BTBT}k_BT\ln\left[\frac{1 + \exp\left(\frac{E_{FS} - E_{V,S} + \Delta\phi}{k_BT}\right)}{1 + \exp\left(\frac{E_{FS} - E_{V,S}}{k_BT}\right)}\right] \end{aligned} \tag{24.6}$$

where F_0 indicates the complete Fermi-Dirac integral of order 0. Typically, T_{BTBT} <1; therefore, TFETs are not able to match the MOSFET in terms of I_{ON} at large overdrives. On the other hand, the low SS, if achieved across a range of at least three to four orders of magnitudes, makes TFET a legitimate alternative for low-voltage and low-leakage applications [30].

Thanks to their simplicity, Eqs. (24.3) and (24.4) are particularly appealing to model Zener tunneling and will be used extensively in the following sections to build an understanding of how the various design parameters affect TFET performance. It is though important to gain a grasp of the tunneling physics itself. Equation (24.3) states that BTBT occurs when an electron travels through the forbidden energy gap having a complex wave vector along the tunneling direction. Therefore, an accurate description of the evanescent modes is necessary to analyze the electron trajectory, i.e., complex band structure, and understand the interactions between the different complex branches involved in the BTBT.

Using a nearest neighbor $sp^3d^5s^*$ tight-binding method, Luisier and Klimeck [26] computed the band structures for three different nanowire channel materials of interests for

TFETs, namely, InAs, Si, and Ge, featuring both real and imaginary bands, and provided a comparison of the transfer characteristics obtained using the WKB approximation and more complex quantum transport models for 1-D nanowire TFETs. From a pedagogical point of view, the three materials investigated give a general and broad description of the different BTBT processes at play and, as examples, illustrate the transport in a wide variety of other materials systems.

Figure 24.3a shows the real and imaginary bands of an InAs nanowire having diameter $d = 3.35$ nm and $E_G = 1.175$ eV. The peculiar feature of its complex energy dispersion is the presence of a single, nondegenerate imaginary branch, highlighted in gray, connecting the highest valence subband to the lowest-lying conduction subband. Along this imaginary path, no crossing between imaginary bands is found. Transfer characteristics computed using this complex "least action for tunneling" branch, i.e., path with the smallest imaginary wave vector, within the WKB approximation, and quantum transport models, with and without phonon-assisted tunneling, showed excellent agreement from the OFF state to the full ON state of the 1-D TFET nanowire geometry [26]. More generally, these results validate the use of the WKB approach to model BTBT for a semiconductor with direct band gap at Γ, showing a single dominant imaginary branch connecting the valence band with the conduction band. Moreover, if direct tunneling is the dominant leakage mechanism at scaled channel lengths, the WKB approximation can be expected to yield a good description of the subthreshold current in the device OFF state.

A different situation is encountered in Si, as shown in Fig. 24.3b. The computed band structure refers to a Si nanowire with $d = 3$ nm and $E_G = 1.619$ eV. The imaginary dispersion highlights that multiple band crossing points are present. A description of such band mixing goes beyond the standard WKB approximation, therefore preventing the identification of a path of least action for tunneling connecting the top of the valence subband with the bottom of the conduction subband. Moreover, not all the complex branches start from a conduction subband minimum or a valence subband maximum at the Γ point, i.e., having a purely imaginary wave vector. If originated away from the Γ point, these imaginary paths have also a real wave vector component; therefore, the transition between different complex bands requires the absorption and emission of a phonon to satisfy momentum conservation. These nuances have been highlighted by Luisier and Klimeck [26], where they compared the BTBT currents obtained following the imaginary path with the smallest κ (dashed gray line in Fig. 24.3b) against the results computed via a quantum transport model accounting for phonon-assisted tunneling and found that the WKB approximation overestimated the device current by two orders of magnitude.

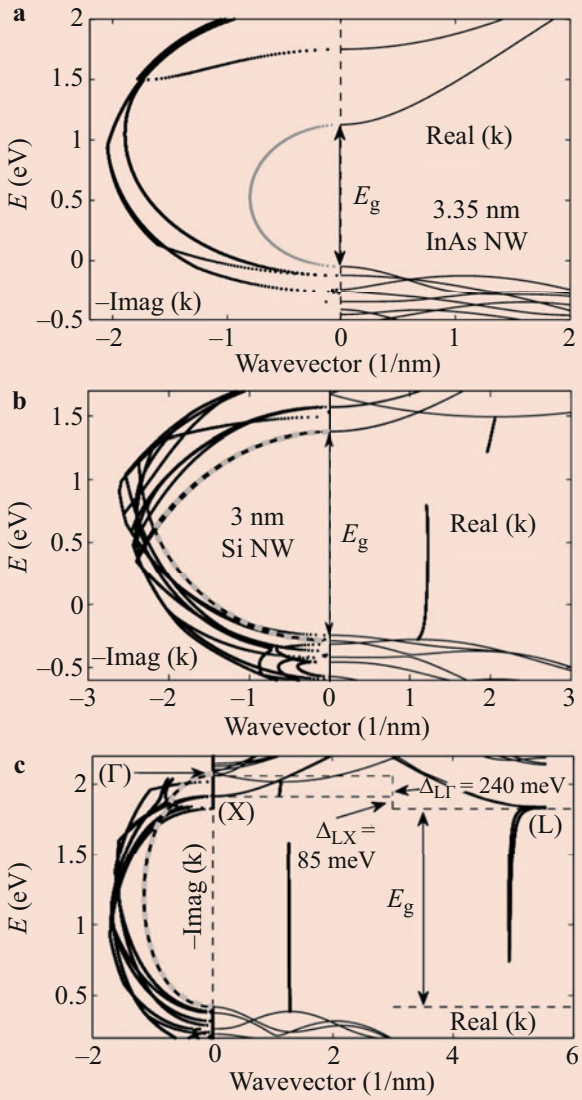

Fig. 24.3 Imaginary and real band structure of (**a**) 3.35-nm-diameter InAs nanowire, (**b**) 3-nm-diameter Si nanowire, and (**c**) 3.12-nm-diameter Ge nanowire. (Figure from Luisier and Klimeck [26])

A peculiar case emerges from the study of Ge nanowires as shown in Fig. 24.3c ($d = 3.12$ nm, and $E_G = 1.409$ eV). The lowest conduction subbands at the L point have nonzero real part, and do not have any imaginary path connecting directly to the highest valence subbands. The lowest conduction subband originates from the bulk Ge Γ valley, labeled (Γ). This subband is nondegenerate, has zero imaginary part, and is directly connected to the maximum of the valley subband. In proximity to the conduction band minimum, several band crossings are also present with four of the bulk X valleys, labeled (X), that are projected to Γ due to quantum confinement in the 1-D geometry. The least action for tunneling path is indicated by the dashed gray lines in Fig. 24.3c and the BTBT

current computed with the WKB approximation matches the quantum transport models only for the ON state, i.e., direct tunneling between the top of the valence subband and the (Γ) conduction subband dominates. However, it fails in the OFF state, where the subthreshold current is a combination of direct tunneling from the top of the valence band and the (X) subbands as well as phonon-assisted tunneling to the (L) subbands.

The analysis by Luisier and Klimeck [26] reveals that the WKB approximation represents a viable approach to the modeling of TFETs in those cases where BTBT develops along a single, nondegenerate imaginary band connecting the top of the valence band to the bottom of the conduction band. For a full analytical description of BTBT processes that can be employed for fast assessment of TFET performance and the development of compact models of tunneling devices, analytical expressions of the complex branches are needed. Unlike the MOSFET where, due to the thermal statistics, only carriers within a small range of energies around the band extrema determine current transport, therefore a parabolic effective mass description of the real band structure is sufficient; in the case of a TFET, carriers need to follow a path along the entire semiconductor band gap, and therefore it is of great importance to resolve the full range of energies with accuracy to precisely compute BTBT probabilities [31]. To this purpose, Guan [32] showed that the nonparabolic approximation of real bands works well to describe the complex band structure of common semiconductor materials within the energy gap, thus revealing the intrinsic elliptic nature of the imaginary branches. Assuming a semiconductor with direct band gap at Γ, the nonparabolic approximation prescribes that the imaginary wave vector, κ_Γ, takes the form [32]

$$\kappa_\Gamma = \begin{cases} \frac{1}{\hbar}\sqrt{2m_h^* E\left[1-E/\left(2E_q^\Gamma\right)\right]}, & 0<E<E_q^\Gamma \\ \frac{1}{\hbar}\sqrt{2m_e^*\left(E_G^\Gamma-E\right)\left[1-\left(E_G^\Gamma-E\right)/\left(2E_G^\Gamma-2E_q^\Gamma\right)\right]}, & E_q^\Gamma<E<E_G^\Gamma \end{cases} \tag{24.7}$$

where E_G^Γ is the direct energy gap at the Γ point and $E_q^\Gamma = E_G^\Gamma\, m_e^*/\left(m_c^*+m_v^*\right)$ is the branch point at which the conduction and valence branches join continuously. The elliptic and analytically integrable expression of Eq. (24.7) can then be substituted in Eq. (24.3) for an accurate calculation of the BTBT probability. From a knowledge of complex band structure and the interactions between the different branches obtained from first principle calculation, a similar expression of the complex wave vector applicable for indirect semiconductors can be obtained [32].

As a last remark, Eq. (24.3) is valid for a 1-D tunneling mode where the tunnel path starts at the valence band edge and terminates at the conduction band edge, which has zero perpendicular momentum. For a bulk direct semiconductor, we can write the total energy as the sum of two components, i.e., $E = E_X + E_\perp$, where E_X is the energy along the tunneling direction, and $E_\perp = \hbar^2\left(k_Y^2+k_Z^2\right)/2m^*$, where k_Y and k_Z are the wave vectors in the directions transverse to tunneling [6]. The transverse energy, $E_\perp$, must be conserved during the tunneling process; therefore, the net effect is that the effective tunneling gap increases and the tunneling probability diminishes. In fact, carrying out the WKB integral, one obtains that the 3D tunneling probability can be written from [6]

$$\begin{aligned} T_{WKB}^{3D} &= \exp\left(-\frac{4\sqrt{2m^*}(E_G+E_\perp)^{3/2}}{3q\hbar\xi}\right) \\ &\cong \exp\left(-\frac{4\sqrt{2m^*}E_G^{3/2}}{3q\hbar\xi}\right)\exp\left(-\frac{E_\perp}{\overline{E}}\right) \end{aligned} \tag{24.8}$$

where ξ is a (constant) junction electric field and $\overline{E} = q\hbar\xi/2\sqrt{2m^*E_G}$ is a factor that takes into account the degradation of the tunneling probability due to the transverse energy state. The larger the factor $\overline{E}$, the smaller the attenuation of the tunneling probability due to carriers having nonzero transverse energy. The simple expressions of Eq. (24.8) also indicate that in order to simultaneously engineer small $E_\perp$ and large $\overline{E}$, one has to rely on materials having elliptic band structures, with light effective mass in the tunneling direction for enhanced transmission and heavier mass in the perpendicular direction to minimize the transverse momentum.

24.4 Subthreshold Swing

It is instructive to show how sub-60 mV/dec swings arise from the simple model of Eq. (24.5). Recall the definition of SS:

$$SS = \left[\frac{d\log_{10} I_D}{dV_{GS}}\right]^{-1} = \ln(10)\left[\frac{1}{I_D}\frac{dI_D}{dV_{GS}}\right]^{-1} \tag{24.9}$$

Assuming that the channel potential varies one to one with the applied gate voltage, SS becomes [24]

$$\begin{aligned} SS &= \frac{\ln(10)}{q}\left[\frac{1}{I_D}\frac{dI_D}{d\Delta\phi}\right]^{-1} \\ &= \frac{\ln(10)}{q}\left[\frac{2q/h}{I_D}\left(\frac{dT_{BTBT}}{d\Delta\phi}F(\Delta\phi)+T_{BTBT}\frac{dF(\Delta\phi)}{d\Delta\phi}\right)\right]^{-1} \\ &= \left[\frac{1}{SS_{TUN}}+\frac{1}{SS_{DOS}}\right]^{-1} \end{aligned} \tag{24.10}$$

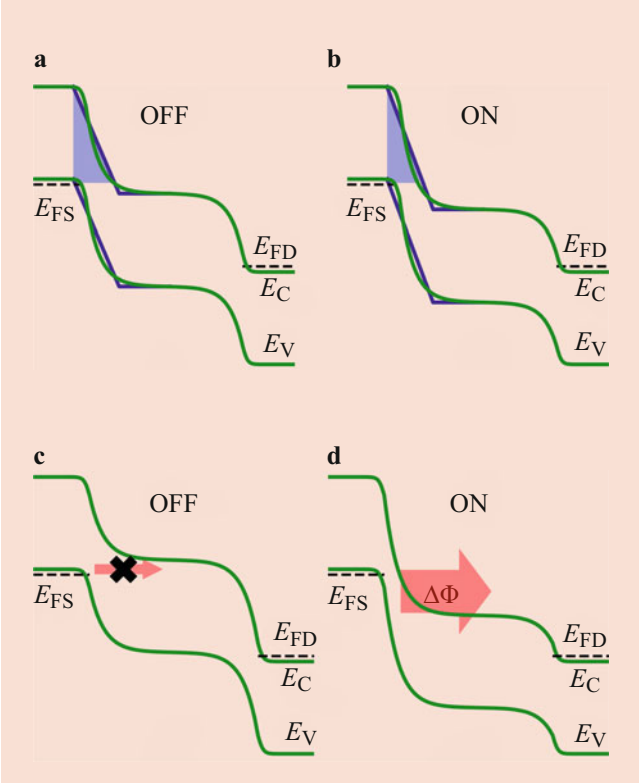

Fig. 24.4 Energy band diagram illustrating the two different methods for achieving steep swings. (**a**–**b**) Tunneling width modulation. The thickness of the tunneling barrier can be modulated by changing the gate voltage and thus the electric field across the tunneling junction. (**c**–**d**) Density-of-state modulation. The alignment of the conduction and valence band is used to cut off the available states for current flow

It can be seen in Eq. (24.10) that two distinct mechanisms contribute to the change of the drain current as a function of V_{GS}; hence, two mechanisms lead to SS <60 mV/dec. These are labeled SS_{TUN} and SS_{DOS} denoting subthreshold swing components based on tunneling width and density-of-state modulation, respectively. The first mechanism, SS_{TUN} , reflects the change of tunneling probability as a function of gate voltage (Fig. 24.4a, b), a process which dominates when T_{BTBT} is small and rapidly changing with V_{GS}:

$$\begin{aligned} SS_{TUN} &= \frac{\ln(10)}{q}\left[\frac{1}{T_{BTBT}}\frac{\partial T_{BTBT}}{\partial \Delta\phi}\right]^{-1} \\ &= \frac{\ln(10)}{q}\frac{3\hbar q(E_G+\Delta\phi)^2}{4\Lambda\sqrt{2m^*}E_G^{3/2}} \\ &= \frac{\ln(10)}{q}\left|\frac{(E_G+\Delta\phi)}{\log(T_{BTBT})}\right| \end{aligned} \tag{24.11}$$

Careful examination of Eq. (24.11) reveals that SS_{TUN} is not limited by the Boltzmann factor. By making Λ larger and for narrow tunneling windows, SS_{TUN} can be made very steep relative to (kT/q)ln(10). Equation (24.11) also indicates a quadratic dependence on $\Delta\phi$; hence, subthermal SS will only occur within a narrow range of gate voltages. It is evident that these requirements are satisfied only for extremely low drain current densities, since SS_{TUN} increases as tunneling probability tends toward unity, i.e., large current densities.

On the other hand, the second term in Eq. (24.10), the DOS switching behavior (Fig. 24.4c, d), rules SS when T_{BTBT} is close to unity, this mechanism controls ON-state current levels, and when this term dominates, SS_{TUN} varies only slightly as a function of V_{GS}. It follows from Eq. (24.10):

$$\begin{aligned} SS_{DOS} &= \frac{\ln(10)}{q}\left[\frac{1}{F(\Delta\phi)}\frac{\partial F(\Delta\phi)}{\partial\Delta\phi}\right]^{-1} \\ &\approx \frac{\ln(10)}{q}\Delta\phi \end{aligned} \tag{24.12}$$

where the integral $F(\Delta\phi)$ is expanded to first order for small $\Delta\phi$. For vanishing $\Delta\phi$, SS can be made arbitrarily small, and the linear dependence on $\Delta\phi$ implies that subthermal SS can be maintained for a wider range of current swing. This particular condition justifies the term density-of-state switching, because the energy filtering action of the conduction and valence band edges cuts off the high and low tail of the Fermi distributions. It follows that the Fermi level in the source needs to be aligned close to the valence band edge (for an nTFET, Fig. 24.5a). If the source degeneracy is too large, this hampers cutoff of the low-energy exponential tails of the Fermi distribution as shown in Fig. 24.5b, leading to a deterioration of the SS. This aspect can be highlighted by computing SS_{DOS} starting from Eq. (24.6) and using the definition of Eq. (24.12):

$$SS_{DOS} = \frac{k_BT}{q}\ln(10)\left[\frac{F_{-1}\left(\frac{E_{FS}-E_{V,S}+\Delta\phi}{k_BT}\right)}{F_0\left(\frac{E_{FS}-E_{V,S}+\Delta\phi}{k_BT}\right)-F_0\left(\frac{E_{FS}-E_{V,S}}{k_BT}\right)}\right]^{-1} \tag{24.13}$$

where we used the property of the Fermi-Dirac integrals, $F_{-1}(\eta) = \partial F_0(\eta)/\partial\eta$. By substituting the analytical solution of the Fermi-Dirac integral of order -1, $F_{-1}(\eta) = [1 + \exp(-\eta)]^{-1}$, back into Eq. (24.13), SS_{DOS} can be written as [29]

$$SS_{DOS} = \frac{k_BT}{q}\ln(10)\left[1+\exp\left(-\frac{E_{FS}-E_{V,S}+\Delta\phi}{k_BT}\right)\right] \ln\left[\frac{1+\exp\left(\frac{E_{FS}-E_{V,S}+\Delta\phi}{k_BT}\right)}{1+\exp\left(\frac{E_{FS}-E_{V,S}}{k_BT}\right)}\right] \tag{24.14}$$

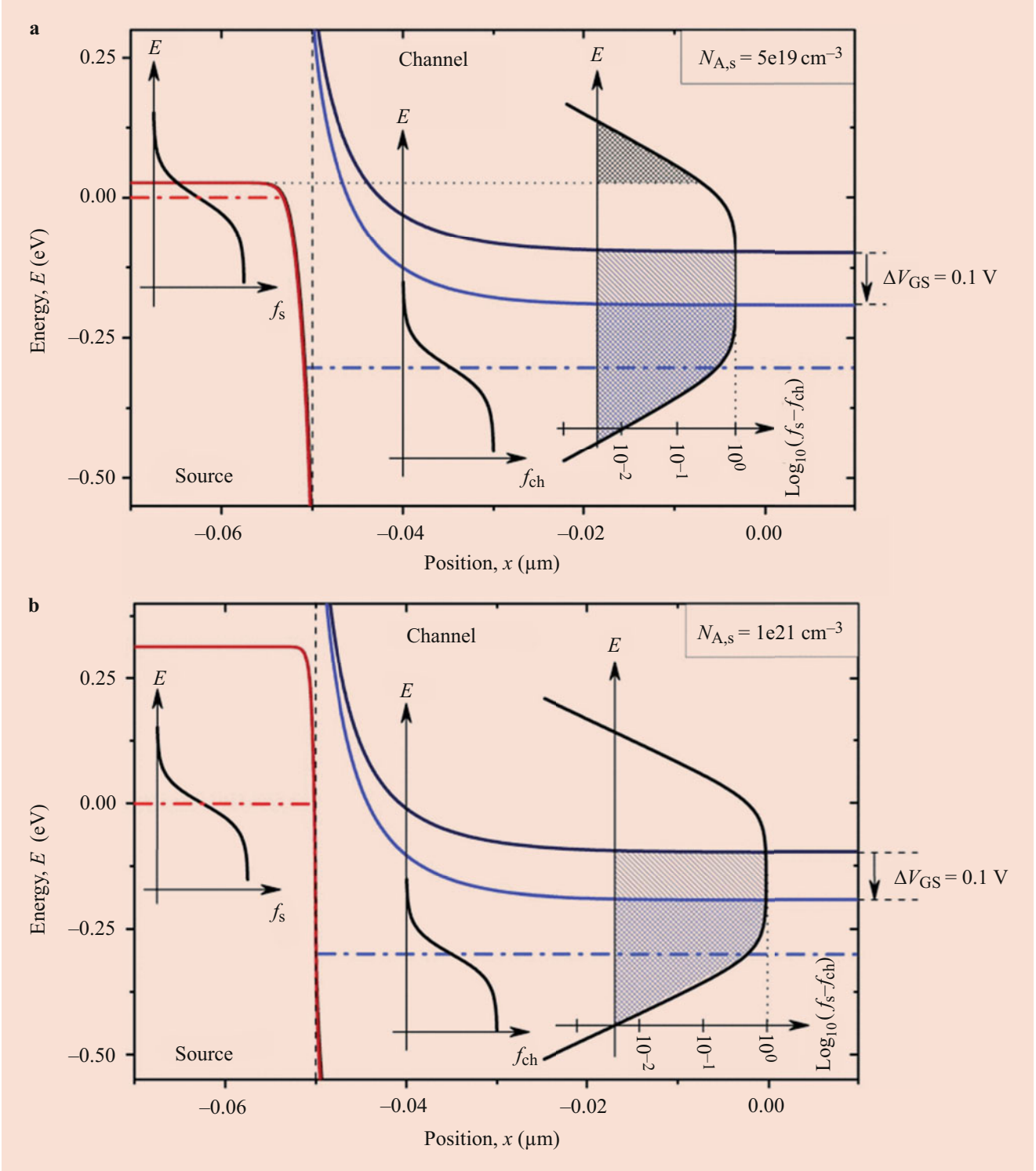

Fig. 24.5 Energy band diagrams of an n-type TFET for (**a**) weak degenerate and (**b**) highly degenerate source doping. When the Fermi level is no longer aligned to the conduction band, the low-energy exponential tails are no longer filtered by the source band gap. (Figure from De Michielis [29])

showing explicitly the dependence on the source hole degeneracy, $\xi_p = E_{V,S} - E_{Fs}$. For nondegenerate to weakly degenerate source doping levels, $\xi_p < 0$, Eq. (24.14) simplifies to $SS_{DOS} \approx \ln(10)\Delta\phi/q$, as previously shown. For a highly degenerate source, $\xi_p > 3k_BT$, SS_{DOS} still vanishes for small $\Delta\phi$. For large tunneling windows such that

$E_{Fs} - E_{C,CH} > 3k_BT$, $SS_{DOS} \approx \ln(10)(E_{FS} - E_{C,CH})/q$. Consider the case of a large source degeneracy, $\xi_p \gg 3k_BT$, where the conduction band lies above the source Fermi level such that $\Delta\phi > 3k_BT$ and $E_{C,CH} - E_{Fs} > 3k_BT$. Under these conditions, SS_{DOS} reduces to the thermionic subthreshold swing of a MOSFET, $\ln(10)k_BT/q$.

The detailed dependences of the subthreshold swing on conduction band energy and gate voltage, respectively, from Eq. (24.14), are shown in Fig. 24.6a, b. In the highly degenerate case, it is possible to distinguish three different regions as outlined above: an initial turn-on where SS is proportional to the tunneling window, a region of almost constant SS at 60 mV/dec, and a region of further increase, proportional to $E_{FS} - E_{C,CH}$. As pointed out by De Michielis [29], Fig. 24.6a, b suggests that a highly degenerate source is preferable since it allows for a wider energy window over which SS is subthermal.

Figure 24.6c shows the separate contributions of tunneling and occupation probabilities for the case of weakly degenerate (top left) and highly degenerate (top right), source doping, and their combined product (bottom). For the highly degenerate case, the larger modulation of the tunneling probability takes place in an energetic window where the combined product is small, and does not translate to an effective drain current change. This also affects the absolute tunneling current levels, because while a narrower tunneling width is expected with increasing source doping, the reduction of the occupation probability of the Fermi-Dirac thermal tails impedes drain current enhancement.

Moreover, other sources for SS degradation lie in parasitic conduction mechanisms, such as TAT, that occur in parallel to the desired BTBT processes. Due to the presence of localized traps originating from defects in the material, vacancies, or dangling bonds, either in the bulk or at the channel interfaces, carriers outside of the tunneling window may contribute to the current flow by means of direct and phonon-assisted tunneling into and out of trap levels.

Another important fact to highlight is that in Eqs. (24.11) and (24.12), the temperature dependences cancel out, meaning that in the OFF state the TFET should display an SS insensitive to temperature. In this description, temperature dependence of the band gap is not considered. When TAT processes are present, the transfer characteristics exhibit a strong temperature and field-dependent dispersion in the subthreshold region [33, 34].

Whether the switching dynamics is governed by tunneling barrier width modulation or DOS switching, SS of a TFET is not limited by k_BT/q ln (10); however, SS as described by Eqs. (24.11) and (24.12) is not constant with respect to the gate voltage. Therefore, while it is possible to obtain a steep slope smaller than 60 mV/dec for a particular V_{GS}, as is often the case for small I_D, this "point slope" is not a good metric to assess TFET performance. To enable supply voltage scaling, an average SS < 60 mV/dec has to be attained over several orders of magnitude change in drain current. Bhuwalka [35] proposed a definition of average swing, $\overline{SS}$:

$$\overline{SS} = \frac{V_T - V_{OFF}}{\log_{10}(I_T/I_{OFF})} \tag{24.15}$$

where V_T is a threshold voltage computed at a particular threshold current, I_T, and V_{OFF} is the gate voltage for which the drain current is minimum, I_{OFF}. Boucart and Ionescu [36] suggested an alternative definition for V_T, corresponding to the gate voltage for which the energy barrier narrowing starts to saturate which is characterized by a transition point between a quasi-exponential dependence and a linear dependence of drain current with respect to V_{GS}. For practical reasons, an $\overline{SS}$ over the full V_{DD} window can be written as [37]

$$\overline{SS} = \frac{V_{DD} - V_{OFF}}{\log_{10}(I_{DD}/I_{OFF})} \tag{24.16}$$

The definitions in Eqs. (24.15) and (24.16) are subject to the supply voltage, $V_{DD,}$ and OFF current, I_{OFF}, of the target application. To compare different TFET configurations independently of the device geometry or the choice of V_{DD} and I_{OFF}, Vandenberghe [38] suggested the I_{60} metric; I_{60} is defined as the current at which the SS is 60 mV/dec, i.e., the current at V_{60} . For voltages less than V_{60}, SS is less than 60 mV/dec, and the TFET has steeper swing than the ideal MOSFET. To outperform MOSFETs for low supply voltage applications, $V_{GS} = V_{60}$ should be approximately 0.1 V with I_{60} in the range 1–10 μA/μm [38]. This provides 0.1 V over which the steep TFET swing can act to provide orders of magnitude OFF-current reduction vs. the MOSFET.

24.5 ON Current

In order to be attractive for low-voltage, low-energy applications, Dehaene and Verhulst argue that TFETs should deliver current of $I_{ON} \approx 100$ μA/μm for sub-0.4 V supply voltages [30]. ON current less than 100 μA/μm will directly impact circuit delay performance since $\tau_D = CV_{DD}/I_{ON}$, where C indicates the gate-source capacitance. Equation (24.5) provides the general guidelines for increasing the tunneling probability and ON current; this can be achieved by increasing the junction electric field and reducing E_G, both of which lead to shorter tunneling paths. By using materials with lighter m^*, there is smaller attenuation of the evanescent mode with imaginary dispersion in the band gap. Small E_G and reduced m^* lead to higher tunneling current, which then points to III–V materials as promising candidates for TFETs, either in homojunction or heterojunction configurations.

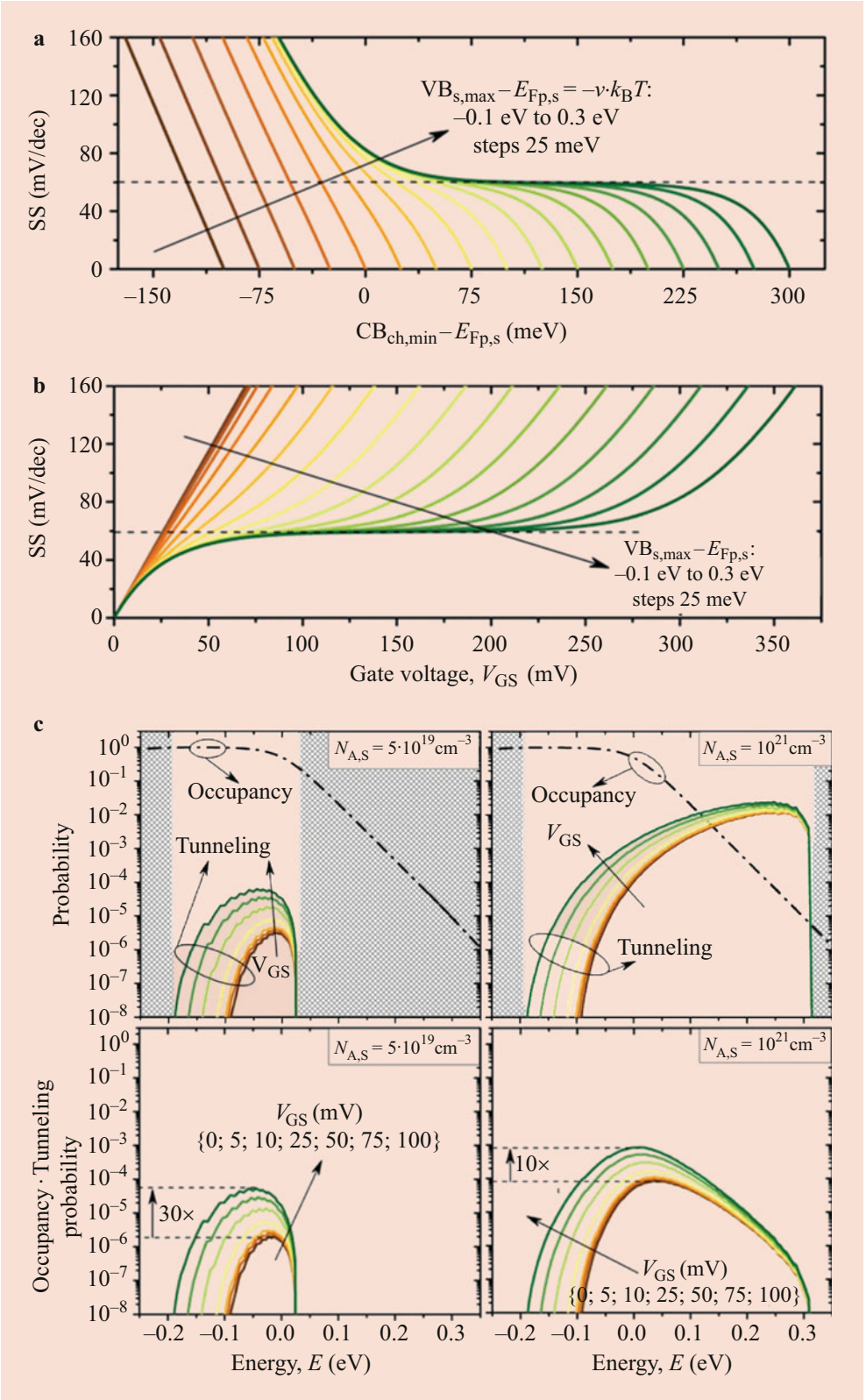

Fig. 24.6 Subthreshold swing (SS) as a function of (**a**) conduction band edge and (**b**) gate voltage evaluated from Eq. (24.14), for different source degeneracies. (**c**) Contribution of the occupancy and tunneling probabilities (top) and their combined product (bottom), for two TFETs having (left) weakly degenerate and (right) highly degenerate source doping. (Figure from De Michielis [29])

It is useful to relate the source depletion width and channel scaling lengths to the device parameters; we can approximate W_D with the Debye length in the source region:

$$W_D = \sqrt{\frac{\varepsilon_S k_B T}{q^2 N_D}} \tag{24.17}$$

where ε_S is the semiconductor permittivity and N_D is the doping in the source. The expression for the channel scaling length depends on the channel geometry [39–41]. In the case of a planar single-gate (SG) structure assuming a parabolic expansion of the vertical potential distribution, the natural length is given by

$$\lambda = \sqrt{\frac{\varepsilon_S}{\varepsilon_{OX}} t_{OX} t_S} \tag{24.18}$$

where ε_{OX} is the oxide permittivity, t_{OX} is its thickness, and t_S is the semiconductor body thickness. It follows from Eqs. (24.5) and (24.17) that I_{ON} improves if the active doping concentration in the source increases. The reason is twofold [42]: Firstly, higher doping in the source reduces W_D and thus enhances the junction electric field. Secondly, E_G is reduced due to band gap narrowing and so then is the tunneling barrier. In optimizing the source doping concentration, an SS- I_{ON} trade-off arises. As discussed in Sect. 24.4, high source doping degrades SS if the source degeneracy becomes too large. The source degeneracy in a pTFET (nTFET) is determined by the DOS in the conduction (valence) band; therefore, from a material standpoint, a large source DOS is desirable for keeping the degeneracy and SS degradation small [38, 43]. For all the common bulk semiconductors, the DOS in the conduction band is lower than in the valence band, and therefore more stringent trade-offs exist for the realization of high-performance pTFETs [44, 45]. Dopant pocket structures have been proposed to ameliorate this imbalance [45].

Equation (24.17) assumes abrupt doping profiles and therefore neglects lateral smearing of the dopant profile into the channel region due to dopant diffusion resulting in an increase of the tunneling path [46]. Materials systems which can achieve abrupt doping are clearly favored for source-channel junction formation. This points to materials system where the junctions can be grown, e.g., by molecular beam epitaxy (MBE) or chemical vapor deposition (CVD), to minimize dopant compensation within the depletion layer.

The gate control of the surface potential in the TFET must be as efficient as possible. As in a MOSFET, increasing the coupling of the gate voltage with the channel potential requires a reduction of the effective oxide thickness (EOT). Oxide thickness scaling and the introduction of high-κ dielectrics have been shown to enhance the tunneling current [47–51]. Enhanced gate control over the channel near the source junction can also be attained by going from a single gate (Fig. 24.7a) to a double gate (or multigate) (Fig. 24.7b) or to a gate-all-around configuration (Fig. 24.7c) [52, 53]. Due to the exponential dependence of the tunneling currents with respect to the dielectric properties, dielectric engineering will achieve a superlinear improvement in the TFET's I_{ON}. Furthermore, when a second gate is added or wrapped around the channel, the equipotential lines crowd toward the source in the device ON state, enhancing the junction electric field locally. This results in shorter tunneling paths and a greater I_{ON} improvement. As far as gate control, these results have also a beneficial impact on the SS favoring an abrupt transition from the device OFF state to the ON state with high tunneling probability.

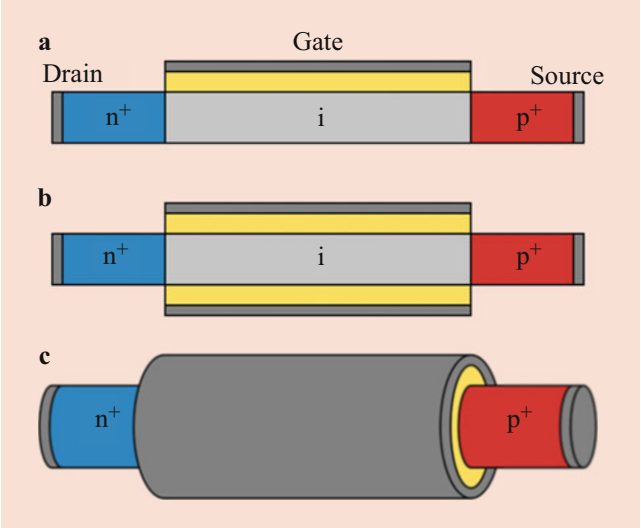

Fig. 24.7 (**a**) Single-gate (SG), (**b**) double-gate (DG), and (**c**) gate-all-around (GAA) TFET geometries

The curvature of the equipotential lines can be further strengthened with the reduction of the channel body thickness. Due to desirable low m^*, when the Bohr radius becomes comparable to the thickness or diameter of the channel t_S [54], size-induced quantum confinement effects result in global increase of the material band gap and hence an increase in tunneling path lengths. These effects are more pronounced for the GAA configuration, with the result of a smaller I_{ON} for the GAA configuration [53].

A double-gate geometry in conjunction with nanometer-scaled body thickness can further enable an additional class of TFETs, the electron-hole bilayer TFET (EHB TFET). Originally proposed by Lattanzio [55–57], a schematic representation of the EHB TFET is shown in Fig. 24.8a. It resembles a DG TFET with the addition of a slight offset between the top and the bottom gate; however, the peculiarity of this device structure consists in adopting an asymmetric configuration between the top and bottom gate to enable perpendicular BTBT in line with the gate electric field. To

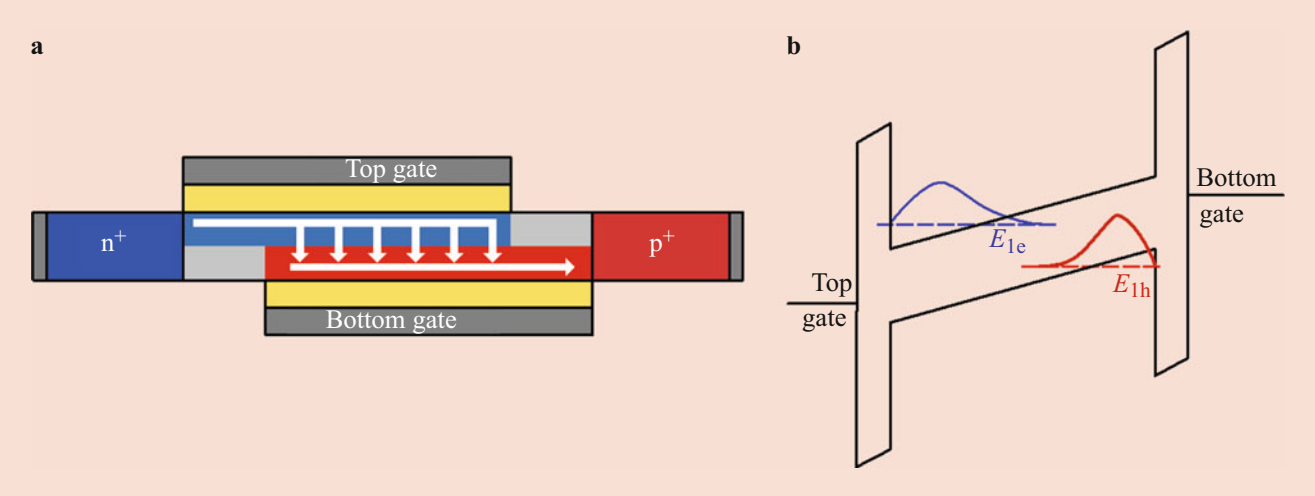

Fig. 24.8 (**a**) Schematic of the EHB TFET. (**b**) Corresponding energy band diagram along a vertical cut in the channel region. E_{1e} and E_{1h} indicate the electron and hole eigenstates

operate as an n-type TFET, the bottom gate bias is fixed in order to electrostatically p^+ dope the bottom part of the channel. On the other hand, the top gate is swept to form an electron-rich top layer. The two gates extend to fully connect the hole-rich bottom layer to the p^+ source and, conversely, the electron-rich top layer to the n^+ drain. Due to the narrow body thickness, in this highly quantized structure, tunneling will occur when a sufficient bias is applied to the top gate such that the electron eigenstate aligns in energy with the hole eigenstate, as exemplified in Fig. 24.8b. In this case, the offset between the two gates is needed to prevent parasitic lateral tunneling leakage paths that degrade SS and enhance ambipolar conduction.

One of the main advantages of this TFET structure is that BTBT takes place within the intrinsic portion of the channel, therefore minimizing the detrimental effects related to dopant-induced band-edge smearing and TAT. Since the total BTBT current depends on the spatial overlap between the electron and the hole wave function, the channel body thickness needs to be aggressively scaled in the 10-nm range. The resulting increase in quantization energies presents a major drawback since it increases the gate voltage needed to align the electron and hole eigenstates (which can only be partially recovered by tuning the work function difference between the top and the bottom gate) while also reducing the gate efficiency. A detailed analytical framework able to capture the trade-offs between ON-state performance and gate efficiency has been developed by Agarwal [58].

The dielectric in the region adjacent to the gate can also play a role in coupling the gate electric field to the tunnel junction internal field. Dielectric sidewall spacers which clad the gate metal concentrate the fringing fields of the gate, thereby setting the position of the maximum electric field and the length of the tunneling path. Chattopadhyay and Mallik [59] studied the impact of spacer dielectric constant on the extent of the source tunneling junction with the help of the contour plots of Fig. 24.9. The simulation results are for a DG TFET with (a) high-κ HfO_2 and (b) low-κ SiO_2 spacers. Fringing fields coming out of the spacer regions are more pronounced for the HfO_2 rather than the SiO_2 case, resulting in a reduction of the band bending at the tunneling junction. This has the detrimental effect of reducing the TFET's ON current. An additional effect concerns the location of the maximum electric field and minimum tunneling distance at the junction. While for the SiO_2 spacer these are located near the surface, for the HfO_2 case, the same are positioned toward the middle of the channel [59]. This leads to a degradation of device performance limited to not only the ON current but also SS. Design criteria for specifying dielectric spacers are highly dependent on the TFET geometry: single-gate, double-gate, gate-all-around, dielectric permittivity, channel permittivity, channel thickness, gate length, and gate-to-junction alignment (underlap vs. overlap) [59, 60].

Dopant pockets can be important performance boosters in TFETs, improving both I_{ON} and SS while simultaneously reducing short-channel effects and possibly providing a pathway for the optimization of pTFETs. Stemming from the proposal of Nagavarapu [61], a pocket TFET presents a localized counterdoped region at the source/channel interface. A pocket nTFET utilizes a p^+-n^+-i-n^+ doping profile (conversely an n^+-p^+-i-p^+ profile is used in a pocket pTFET), where the tunneling junction is formed between the source p^+ region and a narrow, fully depleted n^+ region underneath the gate. The gate also covers the intrinsic channel region. The dopant pocket enhances the built-in electric field, thus increasing the band bending at the junction and reducing the tunneling width, which results in higher drive currents and steeper SS, and causes a shift of the tunneling onset voltage

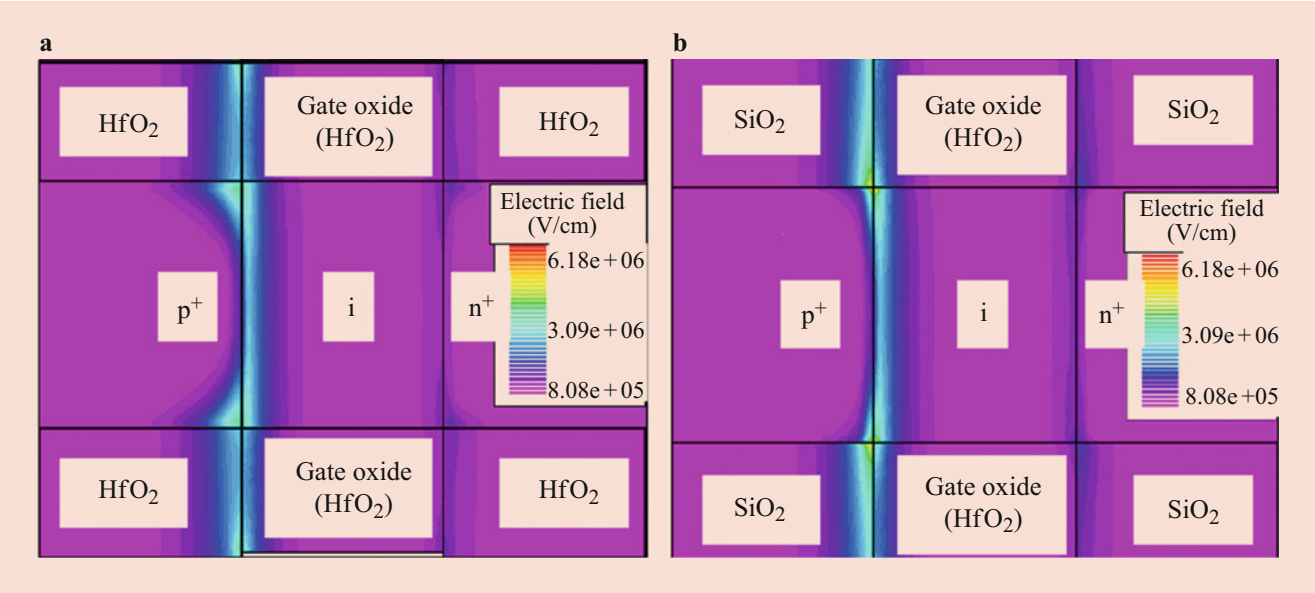

Fig. 24.9 Electric field contour plot for a DG TFET with (**a**) a high-κ HfO_2 and (**b**) low-κ SiO_2 spacers. The TFET is biased at an overdrive voltage $V_{GS} - V_T = 0.5V$ and $V_{DS} = 1V$. (Figure adapted from Chattopadhyay and Mallik [59])

to lower V_{GS} [61, 62]. Moreover, since the enhanced electric field forces the tunnel paths to be more strongly aligned longitudinally with respect to the gate, a lesser impact of field-induced quantum confinement can be anticipated [62].

A properly designed pocket must be fully depleted in order to gain these advantages; this is explained with the help of the energy band diagrams of Fig. 24.10 computed for a Si-on-insulator (SOI) pocket nTFET geometry at the onset of tunneling (simulation described by Nagavarapu [61]). For a thin pocket thickness (Fig. 24.10a), the band diagram at the tunnel junction resembles the case of a canonical p-i-n TFET, where the gate voltage controls the BTBT injection in the channel and the doping pocket serves to shorten the tunneling path. On the other hand, for a thick pocket as shown in Fig. 24.10b, the pocket region is only partially depleted, and the free carrier concentration in the pocket becomes larger than the free carrier density in the channel region at the onset of tunneling. This effect manifests itself in a dip in the band diagrams in proximity to the tunnel junction followed by a hump in the channel region, as it can be seen in Fig. 24.10b. For such a wide pocket, the gate loses control of the band bending at the tunnel junction, and the overall device operation is similar to a p^+-n^+ tunnel diode in series with an n^+-i-n^+ MOSFET; thereby, its switching abruptness is limited to 60 mV/dec at best. Therefore, for a fixed pocket doping, the pocket thickness needs to be minimized while keeping the same fully depleted; this can be attained for a pocket thickness in the range of the depletion width at the tunnel junction [61, 62].

Further optimization can be achieved with the addition of a doping or heterojunction doping pocket at the source side of the tunneling junction as proposed by Verreck [63]. This source design is an especially useful tweak for pTFETs, which typically suffer from a low conduction band DOS resulting in a large source doping degeneracy in conventional p-i-n TFET structures. In such cases, the electron Fermi level is pushed well above the conduction band edge, thereby disabling the energy filtering of the source Fermi tails and degrading SS. The pTFET doping configuration becomes n-n^+-p^+-i-p^+, where the low source doping reduces its degeneracy. This comes at the cost of an increased source resistance; the n^+ pocket retains a high electric field at the tunnel junction to promote BTBT. Also, at the source side, careful tuning of the width of the n^+ pocket is required to minimize the tunneling length and source degeneracy. This aspect is important since carrier thermalization to lower-energy states within the potential well on the source side of the tunnel junction can open a tunneling path to the channel even when the device is in the OFF state. This strategy can also be implemented employing a heterostructure by choosing a source material with a lower electron affinity than the channel (ideally also with a larger conduction band DOS) [63].

24.6 OFF Current

Equations (24.11) and (24.12) predict vanishing SS at the onset of BTBT; however, in the OFF state, other leakage contributions dominate TFET leakage current. Equation (24.5) indicates that low band gap materials are necessary to achieve BTBT transmission probability close to unity. When a low band gap material is employed, I_{ON} increases according to

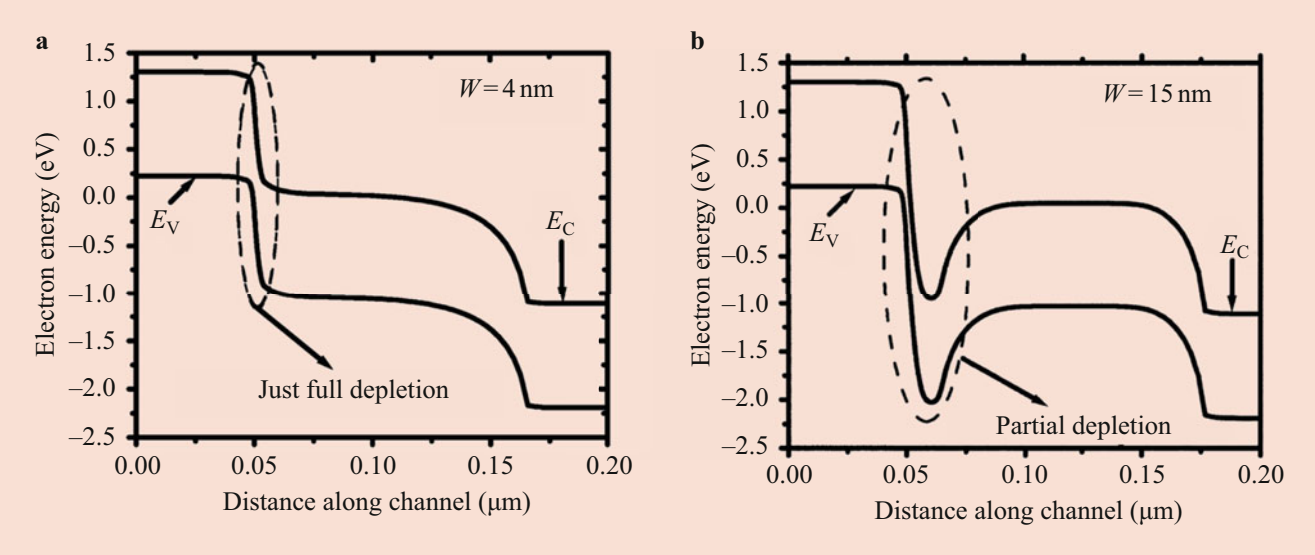

Fig. 24.10 Energy band diagrams of (**a**) a fully depleted vs. (**b**) a partially depleted pocket nTFET. (Figure from Nagavarapu [61])

Eq. (24.5), but also the thermionic current, I_{TH}, becomes significant [28]:

$$I_{TH} = \frac{2q}{h}\int_{E_{C,S}}^{+\infty} f_S(E)\mathrm{d}E \approx \frac{2q}{h}k_B T \exp\left(-\frac{E_G + E_{V,S} - E_{F,S}}{k_B T}\right) \tag{24.19}$$

for the case of an nTFET. At scaled gate lengths, L_G, direct source-drain tunneling, I_{TN}, dominates the OFF-state leakage, especially for low E_G and small m^* materials. Figure 24.11a shows the schematic band diagram for an nTFET in the ON and OFF states.

To obtain a semi-analytical expression for I_{TN}, the simplified band diagram of Fig. 24.11b is considered for the device OFF state, where a rectangular barrier of height equal to E_G and width equal to L_G ($\gg\Lambda$) is assumed for carrier tunneling and qV_{OFF} represents the energy offset between the source Fermi level and the channel conduction band. Under these assumptions, the OFF-state tunneling transmission coefficient, T_{OFF}, and I_{TN} can be computed [10]:

$$T_{OFF}(E) = \exp\left(-\frac{2\sqrt{2m^* L_G}}{\hbar}\sqrt{E\,(1 - E/E_G)}\right) \tag{24.20}$$

$$I_{TN} = \frac{q}{\pi\hbar}\int_0^{qV_{DD}} T_{OFF}\left(E + qV_{OFF}\right) dE \tag{24.21}$$

Figure 24.11c shows the computed I_{TN} versus E_G for the case of a 5-nm-diameter nanowire (NW) and a graphene nanoribbon (GNR) TFETs, for two different L_G, namely, 10 and 15 nm. Figure 24.11c indicates also two different OFF-state targets; for the low-power threshold of 5 nA/μm, the minimum $E_G \approx 0.77$ eV for a gate length of 15 nm. Below a minimum channel length, the OFF current increases sharply, and subthermal SS can no longer be achieved, and the advantages of tunnel FETs disappear [64, 65]. A reduction of I_{TN} can be achieved by increasing L_G: for a planar TFET configuration, this will come at the cost of an increase device footprint, unlike for a vertical TFET where L_G and device footprint are decoupled. The analysis of Zhang [10] shows that the gate length and supply voltage of the technology node where the TFET is inserted ultimately set the minimum band gap needed to achieve a given ON/OFF current ratio.

Trap-assisted tunneling is another important parasitic conduction mechanism often called into play to explain the deviations observed between simulated and measured TFET characteristics. Using Fig. 24.12a, Sajjad [8] depicts the basic physical mechanisms represented in TAT. First, an electron from the valence band (for nTFET) tunnels to a trap state via a heat- or light-mediated transition, followed by thermionic or thermionic-field emission to the conduction band. The latter step is greatly enhanced in the presence of the high built-in electric field of the source-to-channel tunnel junction. Therefore, any effort aimed to increase BTBT generation by boosting the local electric field will similarly increase the TFET leakage current. In general, a strong temperature dependence in the TFET OFF-state and subthreshold characteristics is a signature of TAT.

A good starting point for the modeling of TAT is represented by the SRH generation/recombination theory. The SRH formalism describes a generation process where an electron in the valence band is promoted by heat or light to a trap state in the band gap of the semiconductor, before

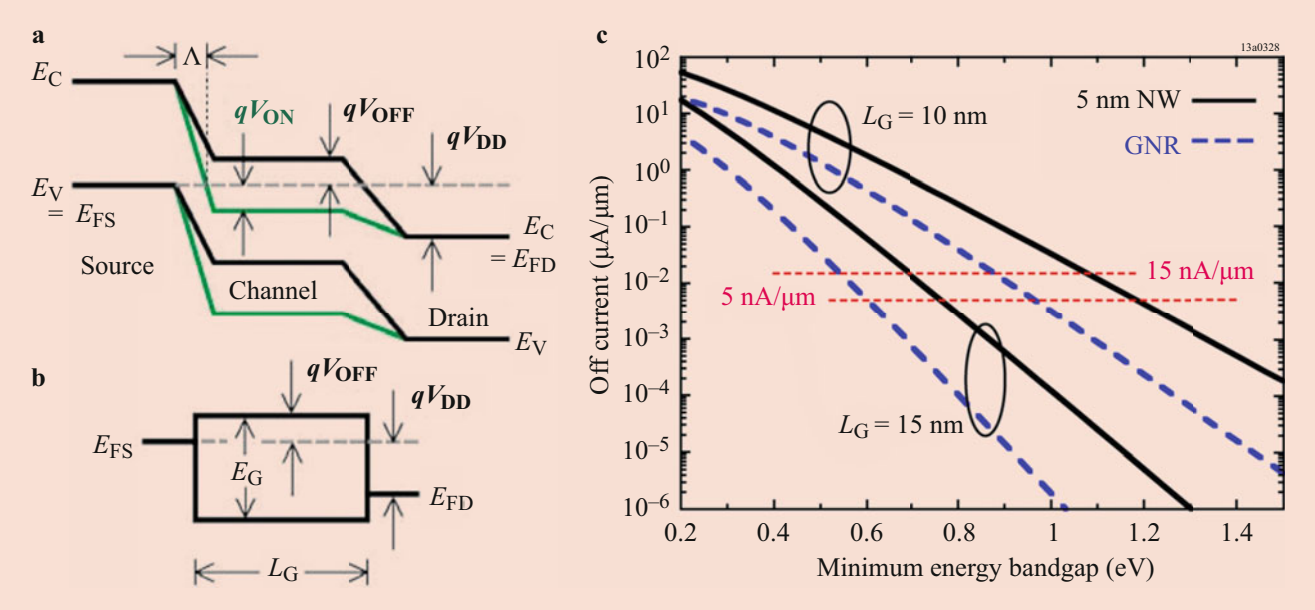

Fig. 24.11 (**a**) Schematic energy band diagram of an nTFET in the OFF (black) and ON state (green). (**b**) Simplified band diagram of the device OFF state for $\Lambda \ll L_G$. (**c**) OFF-state current, I_{TN}, vs. E_G for nanowire (NW) (solid lines) and graphene nanoribbon (GNR) TFETs. (Figure adapted from Zhang [10])

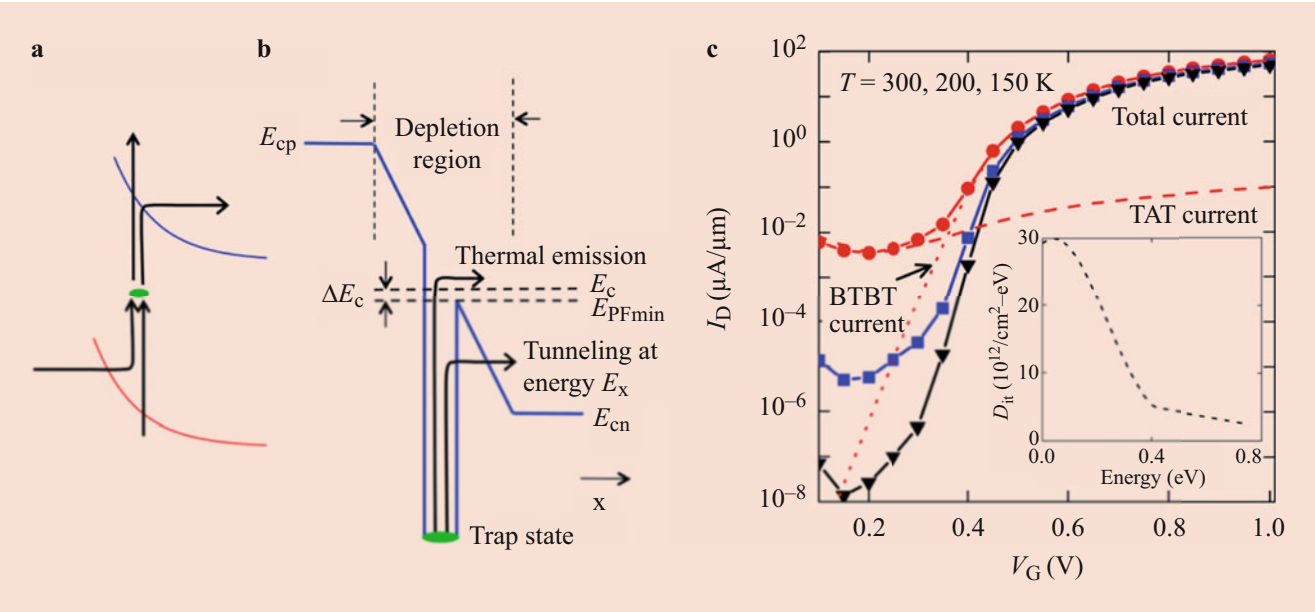

Fig. 24.12 (**a**) Schematic of the TAT process at the source-channel junction of an nTFET, which is mediated by phonon/photon absorption and tunneling. (**b**) Electron emission from the trap occurs via thermal emission, which can also be assisted by tunneling. (**c**) TAT impact on the transfer characteristic of an $In_{0.53}Ga_{0.47}As$ homojunction TFET at different temperatures. Inset: trap distribution vs. energy. (Figure adapted from Sajjad [8])

being emitted to the conduction band by similar interactions. However, in the presence of a strong electric field, defect-to-band tunneling becomes significant and can even dominate. In this case, the SRH formalism has been adapted to take into account the enhancement factor due to the high electric field at the tunneling junction. An analytical framework for the study of electric field-enhanced carrier generation via TAT has been presented by Sajjad [8]. The net generation rate per unit area can be written as [8, 66]

$$G = \int \frac{n_i^2 - np}{\tau_p \left(\frac{n+n_1}{1+\Gamma_p}\right) + \tau_n \left(\frac{p+p_1}{1+\Gamma_n}\right)} D_{it} dE \qquad (24.22)$$

In Eq. (24.22), n_i represents the intrinsic carrier concentration; n and p are the electron and hole carrier densities, respectively; and τ is the minority carrier lifetime. The parameter Γ is the tunneling enhancement factor; it accounts for the electric field dependence and acts to decrease the minority carrier lifetime. The terms $n_1 = n_i \exp\left(\frac{E_t - E_i}{k_B T}\right)$ and $p_1 = n_i \exp\left(\frac{E_i - E_t}{k_B T}\right)$ are derived from the principle of detailed balance, where E_i is the semiconductor intrinsic Fermi level and E_t is the trap state energy. Figure 24.12b depicts how, after an electron is emitted from the valence into the trap state, the same electron can then be emitted to the conduction band for energies exceeding E_{PF}, which is the activation energy for trap emission that has been lowered by the trap's presence in a high electric field, the Poole-Frenkel effect. It is also possible to emit to the conduction band by thermionic field (tunneling field) emission in the energy range between E_{Cn} and E_{PF} indicated in Fig. 24.10b. Therefore, the electron enhancement factor, Γ_n, is given by the sum of two terms, $\Gamma_n = \Gamma_{PF} + \Gamma_{TN}$, where Γ_{PF} represents the enhancement factor due to a thermal jump over a reduced barrier due to the Poole-Frenkel effect and Γ_{TN} the enhancement factor due to tunneling. As shown by Furlan [67], the electron enhancement factor can be written

$$\Gamma_n = \frac{1}{k_B T} \int \exp\left(\frac{E_C - E_X}{k_B T}\right) T(E_X)\, dE_X \qquad (24.23)$$

where E_X is the energy to which the electron is tunneling. The tunneling probability is computed with the aid of the WKB approximation for a triangular barrier:

$$T(E_X) = \exp\left(-\frac{4\sqrt{2m^*(E_{PF} - E_X)^3}}{3q\hbar F}\right).. \qquad (24.24)$$

The enhancement factor, Γ_n, can then be expressed as follows after Sajjad [8]:

$$\Gamma_n = \underbrace{\frac{1}{4}\exp\left(\frac{E_C - E_{PF}}{k_B T}\right)}_{\Gamma_{PF}} + \underbrace{\frac{\Delta E_n}{k_B T}\int_0^1 \exp\left[\frac{\Delta E_n}{k_B T}u - K_n u^{3/2}\right] du}_{\Gamma_{TN}} \qquad (24.25)$$

where $K_n = 4\sqrt{2m^*\Delta E_n^3/3q\hbar F}$, $E_C - E_{PF} = q(qF/\pi\varepsilon)^{1/2}$ is the electric field-induced lowering of the barrier due to Poole-Frenkel effects, and ΔE_n is the tunneling barrier height. ΔE_n is the difference between the top of the (reduced) barrier and the minimum energy where the electron can tunnel to, which can vary from $\Delta E_C = E_{PF} - E_t$, if $E_t > E_{Cn}$, to $\Delta E_C = E_{PF} - E_{Cn}$, if $E_t < E_{Cn}$ [66]. A similar treatment follows for Γ_p. The TAT tunneling current can be calculated, $I_{TAT} = \int G(x)dx$. Therefore, both the spatial and the energetic location of the traps determine the exact bias dependence of I_{TAT} while also affecting the device electrostatics.

Figure 24.12c shows the computed transfer characteristics for an $In_{0.53}Ga_{0.47}As$ TFET at various temperatures to reveal the signatures of TAT and how it can severely degrade both I_{OFF} and SS [8]. At all temperatures, well above the crossing of the band, the total current mainly comes from BTBT, and the ON current is shown to be only weakly dependent on temperature. However, close to the onset of BTBT, the drain current is dominated by TAT for the higher-temperature range, thus hiding the steepest part of the BTBT branch. At lower temperatures, below 200 K for this calculation, the intrinsic SS is observed, and in this case, the minimum SS is limited by the rate of change of BTBT. This is because TAT is highly dependent on temperature; therefore, the lowest achievable OFF-state current is a function of temperature (ambipolar current can further increase I_{OFF}).

Teherani [9] has shown that parasitic leakage currents can also arise due to Auger generation/recombination processes, and this can also limit TFET performance, affecting both I_{OFF} and the minimum achievable SS. Since Auger generation is an intrinsic phenomenon highly dependent on the material band structure, its effects cannot be alleviated with improved material quality or device processing. Auger generation, also known as impact ionization, consists of a three-particle process, where a high kinetic energy hole collides with an electron in the valence band. In the process, the former loses most of its kinetic energy, while the latter is excited to the conduction band, thus generating an electron-hole pair. The reverse process, Auger recombination, involves the annihilation of an electron-hole pair that either excites an electron to higher energies in the conduction band or pushes a hole deeper into the valence band. Since Auger generation is limited by the probability of finding a high-energy carrier, in conventional semiconductors, this becomes significant only at high carrier densities or very large electric fields or at lower carrier densities for narrowband gap materials.

In the context of TFET, the band gap of interest is not the actual semiconductor band gap, but rather the effective band gap separating the electron and hole eigenstates at the two sides of the tunneling junction. This situation is illustrated in the band diagrams of Fig. 24.13 for the case of a bilayer TFET. In the device OFF state, the energy separation between the two eigenstates is large (Fig. 24.13a); however, as the device transitions toward the ON state (Fig. 24.13b), the effective band gap is reduced, resembling the situation of a gate-modulated small band gap semiconductor. Before the bands uncross and the BTBT current dominates, the spatial overlap and small energy difference between the electron and hole eigenstates can promote Auger generation as well as other generation/recombination processes. Once an elec-

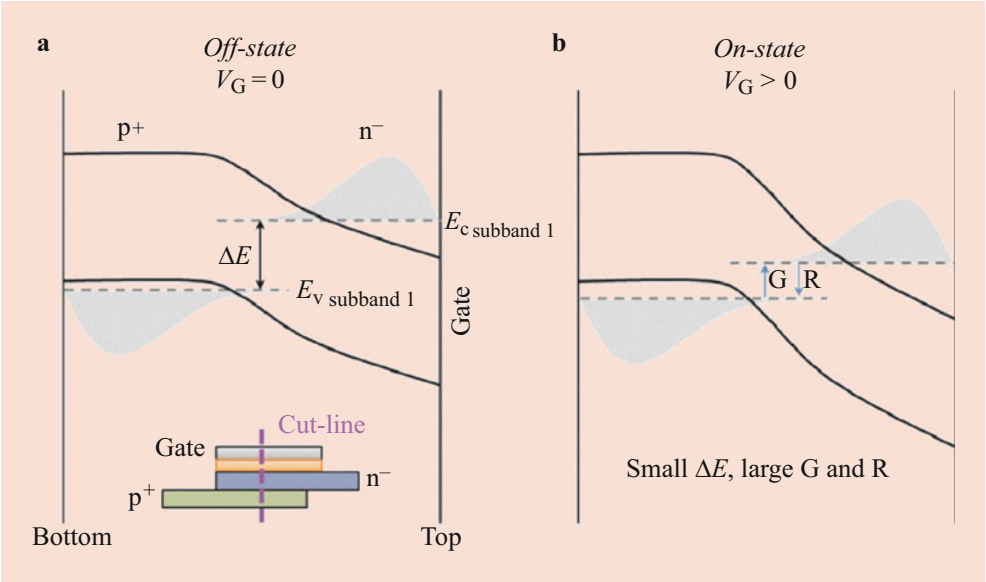

Fig. 24.13 (**a**) Energy band diagram across the tunneling region of a vertical nTFET in the OFF state and (**b**) ON state. Shaded gray areas indicate the hole and electron wave functions. (Figure from Teherani [68])

tron/hole pair is generated across the junction, due to the applied bias, the electron (hole) is swept to the drain (source). The Auger generation current, I_{AU}, across the device increases exponentially as the energy separation between the eigenstates, ΔE_{EG}, is reduced, as discussed by Teherani [9, 68]:

$$I_{AU} \propto \exp\left(-\frac{\left(2\frac{m_e^*}{m_h^*}+1\right)}{\left(\frac{m_e^*}{m_h^*}+1\right)}\frac{\Delta E_{EG}}{k_B T}\right) \tag{24.26}$$

It follows from Eq. (24.26) that if the Auger generation current dominates the device OFF state, this will also affect the minimum achievable SS. In fact, assuming perfect gate efficiency, $d\Delta E_{EG}/dV_{GS} = 1$ at room temperature SS $\approx$ 30 mV/dec when the hole mass is much heavier than the electron mass. On the other hand, if the carrier masses are comparable, SS $\approx$ 40 mV/dec.

24.7 Output Characteristics

The tunneling window in an nTFET is set by the difference between the valence band in the source and the conduction band edge in the drain. Therefore, $\Delta\phi = (E_{Fp} - E_{Fn}) + \xi_p + \xi_n$, where the difference between the hole quasi-Fermi level in the source, E_{Fp}, and the electron quasi-Fermi level in the drain, E_{Fn}, is equal to $-qV_{DS}$ and ξ_p (ξ_n) is the source (drain) degeneracy. It follows that $\Delta\phi$ is controlled by both the drain-source and the gate-source potential modulating the position of the conduction band in the channel region. For a fixed V_{GS}, sweeping V_{DS} starting from 0 V enlarges $\Delta\phi$, and as a consequence, I_D increases. When the valence band in the source is lowered below the conduction band in the channel, increasing V_{DS} does not impact the energy extent of the tunneling window, and I_D saturates. Similar to a MOSFET, a saturation voltage, $V_{DS,\,SAT}$, can be defined, and since the conduction band edge in the channel is dependent on V_{GS}, the larger V_{GS}, the more $V_{DS,\,SAT}$ is shifted to higher values.

A significant difference between MOSFETs and TFETs lies in the shape of the output characteristics for low V_{DS}. Fig. 24.14 compares the common source measurements of three III–V nanowire nTFETs [69] with different source doping, ranging from (a) unintentionally doped $10^{17} - 10^{18}$ cm^{-3}, (b) 10^{19} cm^{-3}, and (c) 4×10^{19} cm^{-3}. A superliner onset and delayed saturation is observed for the lowest doping case, as well as lower ON-state currents. As the source doping is increased, the turn-on at low V_{DS} becomes linear, and $V_{DS,\,SAT}$ is reduced. These features are generally unwanted, as they increase the switching delay. However, if properly engineered in a TFET with $V_T \approx 0$, intrinsic gain larger than unity can be attained in the superlinear region enabling TFET circuit to operate at supply voltages under 400 mV [70].

To understand the origin of the superlinear onset, it is important to understand how V_{DS} affects both the tunneling window and the device electrostatics. In a MOSFET under high drain bias, channel inversion is maintained due to source-injected carriers, i.e., the gate-source capacitance dominates the gate-channel capacitance. However, this is not true for a TFET because the source-channel tunneling barrier limits the

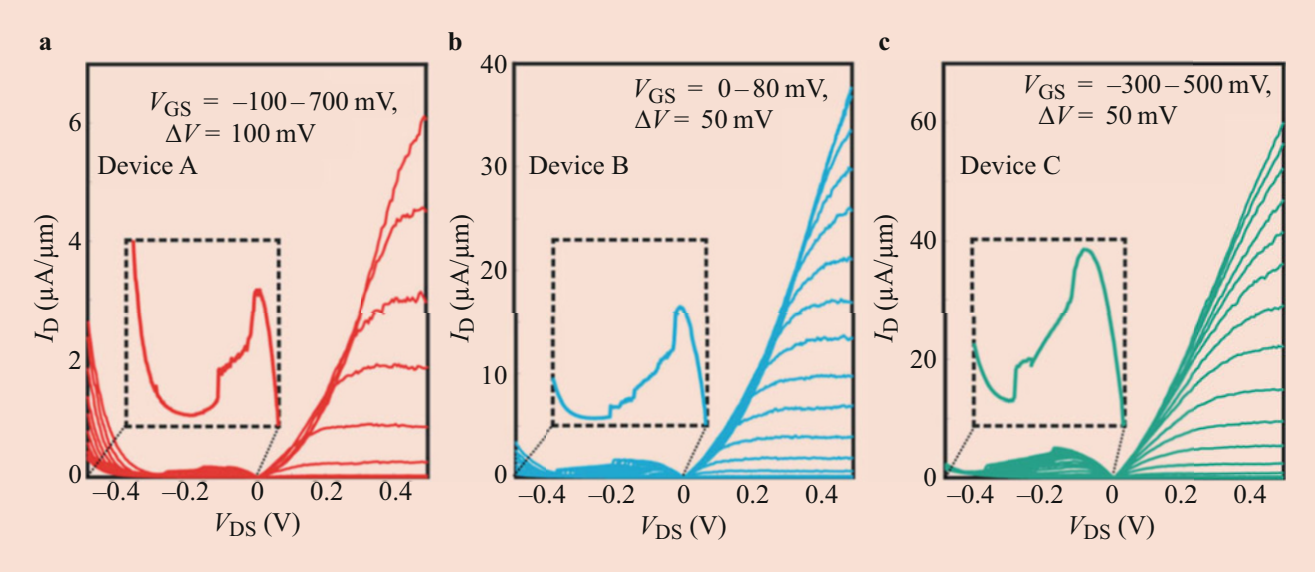

Fig. 24.14 Comparison of the measured output characteristics of InAs/InGaAsSb/GaSb NW nTFETs. From (**a**) low, (**b**) medium, and (**c**) high source doping. Device A shows the lowest ON current performance due to source depletion effects as well as the strongest pronounced superliner onset behavior. Negative differential resistance is observed for all three devices for negative V_{DS} corresponding to the Esaki tunneling branch. (Figure from Memisevic [69])

inflow of carriers; therefore, the gate-channel capacitance is dominated by the gate-drain capacitance. If V_{DS} increases, then the drain channel increases, and the channel charge reduces, resulting in an increment of the surface potential [71]. Moreover, for low V_{DS}, the majority of the applied bias drops across the tunnel junction; therefore, the drain-source bias controls both the quasi-Fermi level in the channel and its conduction band. To gain insight, Eq. (24.5) for the nTFET can be rewritten in the following way:

$$\begin{aligned} I_D &= \frac{2q}{h} T_{BTBT} \int_{E_{C,CH}}^{E_{V,S}} [f_S(E) - f_D(E)]\, dE \\ &\propto \int_{E_{C,CH}}^{E_{V,S}} [f_S(E) - f_{CH}(E)]\, dE \end{aligned} \tag{24.27}$$

where for simplicity $T_{BTBT} = 1$ and the quasi-Fermi level in the channel is aligned to the drain Fermi level. The integral of Eq. (24.27) can be expressed in closed form in terms of the Fermi integrals of order 0 as [72]

$$I_D \propto [F_0(\alpha) - F_0(\beta) - F_0(\gamma) + F_0(\delta)] \tag{24.28}$$

and the arguments of the Fermi integrals read

$$\begin{aligned} \alpha &= (E_{Fp} - E_{C,CH})/k_B T \\ \beta &= (E_{Fp} - E_{V,S})/k_B T \\ \gamma &= (E_{F,CH} - E_{C,CH})/k_B T \\ \delta &= (E_{F,CH} - E_{V,S})/k_B T \end{aligned} \tag{24.29}$$

Further, we assume that $E_{Fp} = 0$ is the energy reference and that the drain bias controls in a one-to-one fashion the $E_{F,CH}$ as well as $E_{C,CH}$ such that $\partial E_{F,CH}/q\partial V_{DS} = \partial E_{C,CH}/q\partial V_{DS} = -1$. It follows that α and δ follow a linear relation with respect to V_{DS}, β is a parameter fixed by the source degeneracy, while in γ the V_{DS} dependencies cancel out. Following the analysis by De Michielis [72], it is assumed that in the TFET ON state for $V_{DS} = 0$ V, $E_{C,CH}$ is below E_{Fp} and $E_{V,S}$ by at least $3k_BT$ and two different cases can be studied.

For a degenerately doped source, $(E_{V,S} - E_{Fp}) > 3k_BT$, in Eq. (24.28), we can approximate the Fermi integrals with $F_0(\alpha) \approx \alpha$ ($\alpha \gg 0$) and $F_0(\delta) \propto e^{\delta}$ ($\delta \ll 0$), and it follows that the drain current is linearly dependent with the drain bias, $I_D \propto -E_{C,CH}$. Therefore, the superlinear contribution in the output characteristics is evaluated by calculating the derivative of the output conductance, g_o, with respect to V_{DS}:

$$\frac{\partial g_o}{\partial V_{DS}} \propto \exp\left(\frac{E_{Fch} - E_{V,S}}{k_B T}\right) \tag{24.30}$$

On the other hand, for the nondegenerate case, i.e., $(E_{V,S} - E_{Fp}) < -3k_BT$, Eq. (24.30) becomes

$$\frac{\partial g_o}{\partial V_{DS}} \propto \frac{\exp(-\alpha)}{[1 + \exp(-\alpha)]^2} + \frac{\exp(\delta)}{[1 + \exp(\delta)]^2} \tag{24.31}$$

The derivative of the output conductance expressed as in Eq. (24.31) shows a nonmonotonic trend, exhibiting a maximum for $V_{DS} = -E_{V,S}/q$. For this case, the output char-

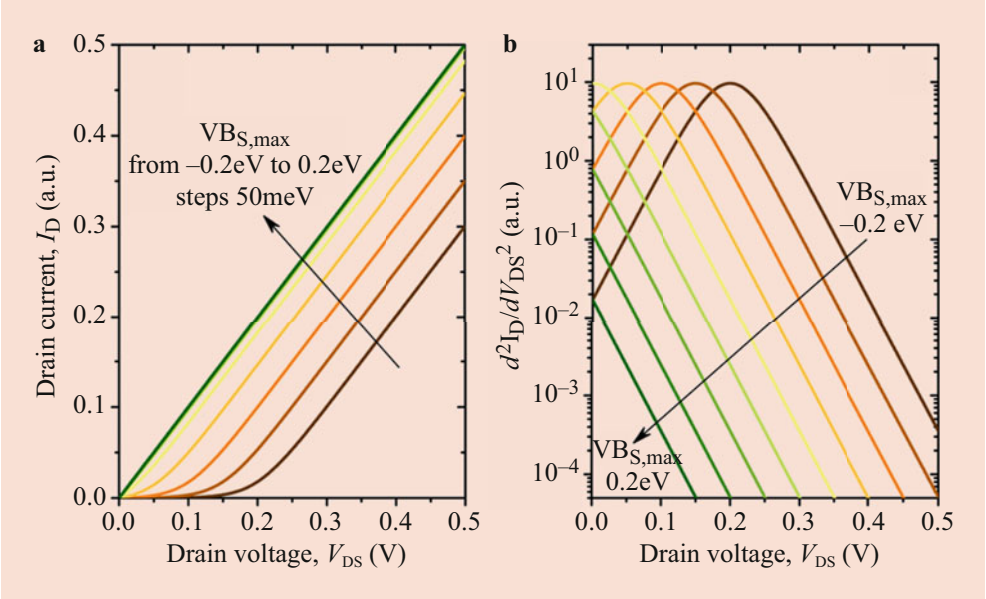

Fig. 24.15 (**a**) Output characteristics evaluated using Eq. (24.28) and (**b**) derivative of the output conductance for different source degeneracies ranging from −0.2 to 0.2 eV. (Figure from De Michielis [72])

acteristics show the detrimental superlinear onset as shown in Fig. 24.15, qualitatively in agreement with experiments with low source doping.

24.8 Ambipolar Conduction

The TFET presents two tunneling junctions, at the source-channel and at the channel-drain interfaces; thus, it exhibits ambipolar conduction , meaning that an nTFET can operate as a pTFET when a negative V_{GS} is applied. In fact, for negative V_{GS}, the crossover between the channel valence band and the drain conduction band opens up a tunneling path where holes are injected into the channel, and I_D increases for decreasing V_{GS}. Ambipolar tunneling current is, in general, undesirable since it leads to higher OFF-state leakage current especially for materials having low E_G and light m^*. Under these circumstances, the ambipolar BTBT current could be the dominant conduction mechanism in the OFF state and thus need to be abated. In the opposite manner as described in Sect. 24.5, reducing ambipolar conduction requires to weaken the gate control at the drain-channel junction and reduce the BTBT generation efficiency. Therefore, this can be achieved by reducing the drain doping, at the expense of increasing the channel resistance, using materials with higher E_G and heavier m^*. For a homojunction TFET, a wider band gap material then can directly reduce I_{ON}. A weaker gate control also results in weaker tunneling electric field which occurs when introducing a gate-drain underlap [73]. In fact, in a TFET, it is required to have a tight gate control at the source side where the desired BTBT processes take place. Adding a gate-drain underlap increases the tunneling path at the drain tunneling junction and consequently reduces BTBT efficiency. Optimization of the ungated region is necessary, such that a higher resistance near the drain region does not impact significantly I_{ON}. An alternative is represented by the introduction of a dual material gate [74] – introducing two different metals with different work functions in the gate of a TFET (biased at the same V_{GS}) permitting an independent optimization of the amount of band bending at the source-channel and drain-channel junctions to obtain a good trade-off in terms of I_{ON}, I_{OFF}, and V_T, as well as SS improvements. Similar improvements can be attained also with a heterogeneous gate dielectric [75], where a small EOT is used to control the source-channel junction and a large EOT is employed at the drain-channel junction. A larger EOT can be realized using either a thicker oxide or a dielectric with low dielectric permittivity.

From a circuit design perspective, proper design methodologies relying on controllable ambipolarity have been proposed, enabling the design of complex logic circuit with fewer components [76]. For these applications, ambipolarity must be optimized in order to obtain symmetric I_{ON} current levels for both the source-channel and drain-channel tunneling branches.

24.9 Heterojunction Tunnel FETs

The analysis conducted in the previous sections results in very stringent trade-offs for the simultaneous optimization of both I_{ON} and I_{OFF}, since the boost of the former leads

to the unwanted increase of the latter. Decoupling the two factors cannot be achieved in a homojunction TFET, i.e., in a device configuration consisting of only one material. On the other hand, a heterojunction TFET provides the extra degree of freedom, i.e., different source and channel semiconductors, to set the desired band alignment. Materials exhibiting different electron affinities and band gaps can align to form straddled, staggered, and broken gap. In such a heterostructure, the effective tunneling band gap at the source-channel junction is given by the difference between the conduction band at the channel side of the junction and the valence band at the source side of the junction.

The goal of a heterojunction TFET (HTFET) is to combine a small effective band gap at the source-channel junction, thus resulting in high I_{ON}, with a large effective band gap at the channel-drain junction to keep I_{OFF} low. In a broken gap alignment, the effective band gap is negative, meaning that there is no forbidden region to tunnel through and thus the transmission probability is unity. This is the preferable condition to boost I_{ON} performance, although careful attention has to be paid to additional phonon-assisted leakage paths in the device OFF state [77]. The associated thermal jumps are affected by the quantization effect resulting from the triangular wells at the junction due to the conduction band rising in the device OFF state and the interaction strength with the available photon. An additional flexibility is given by the choice of the source materials DOS. A large band gap material is usually associated with a large DOS [10] to limit the source degeneracy at large doping concentration. If the band alignment at the junction is highly staggered, the peak of the BTBT generation rate moves closer to the source-channel junction leading to a reduced drain-induced barrier thinning, thus improving device electrostatics [78, 79].

III–V semiconductors are well suited to realize heterojunction TFETs; by tuning the mole fraction of the constituent material in ternary compound materials, III–V materials show a wide variety of band gaps and band alignments. The same variety can be found in the effective masses. Depending on the choice of materials, heterostructures can be either lattice-matched, i.e., both materials have the same lattice constant such as $In_{0.53}Ga_{0.47}As/InP$ (straddled) and $GaAs_{0.5}Sb_{0.5}/ In_{0.53}Ga_{0.47}As$ (staggered), or lattice-mismatched, resulting in nonuniform strain. The stress has an impact in the local band structure and can be explored to improve device performance. The build-up of stress can also result in interfacial defects at the junction if relaxation sets in. Moreover, due to the splitting of light and heavy hole bands under uniaxial or biaxial strain conditions, the valence band DOS is reduced, therefore increasing the source degeneracy that could lead to a degradation of SS.

Starting from Eq. (24.2), the impact of a staggered band alignment in the performance of a 1-D TFET can be analyzed, as shown in Fig. 24.16a from Lind [80]. For weakly degenerate source doping, the source Fermi-Dirac distribution is approximately unity, $f_S(E) \approx 1$, and for a large enough drain bias such that $f_D(E) \approx 0$, Eq. (24.2) simplifies to

$$\begin{aligned} I_D &= \frac{2q}{h}\int_{E_{C,CH}}^{E_{V,S}} T_{BTBT}(E)\mathrm{d}E \\ &\approx \frac{2q}{h}\int_{0}^{qV_{ON}} T_{BTBT}(E)\mathrm{d}E \end{aligned} \tag{24.32}$$

where qV_{ON} is the allowed tunneling window. The transmission probability is computed from Eq. (24.3), and the electric field at the junction, ξ, is given by

$$\xi \approx \frac{E_G - \Delta E_V + qV_{ON}}{\lambda} \tag{24.33}$$

where the tunneling path is approximated to be equal to the geometric scaling length and ΔE_V is the valence band offset. The classical turning point for a staggered band alignment is then modified as follows:

$$\begin{aligned} x_1 &= -\frac{E_G}{2q\xi} + \frac{\Delta E_V - E}{q\xi} \\ x_2 &= \frac{E_G}{2q\xi} \end{aligned} \tag{24.34}$$

with the energy E measured with respect to the valence band edge. The integration of Eq. (24.3) yields [80]

$$T(E) = \exp\left(-\frac{\sqrt{m^*}E_G^{3/2}}{2\sqrt{2}q\xi\hbar}\left[\frac{\pi}{2} - \left(\sqrt{1-y_S^2}y_S + \arcsin(y_S)\right)\right]\right) \tag{24.35}$$

where the dimensionless parameter $y_S(E) = 2(\Delta E_V - E)/E_G - 1$, within the energy range $0 < E < \Delta E_V$, defines the enhanced transmission probability due to the staggered band alignment. For $E > \Delta E_V$, $y_S = -1$, and Eq. (24.4) is recovered. On the other hand, $y_S = 1$ corresponds to a broken gap band alignment, and the transmission probability is unity.

The ON-state current vs. ΔE_V is calculated and plotted in Fig. 24.16b for a 5-nm- and a 10-nm-diameter InAs NW, for a tunneling window $qV_{ON} = 0.3$ eV. Due to quantization effects for narrowband NWs, the relevant subband position will shift, and the NW band gap increases as diameter decreases as shown in Fig. 24.16c [80]. The bulk valence band offset is $\Delta E_V = 0.56$ eV. Zero valence band offset in Fig. 24.16b indicates the case of an InAs homojunction TFET. The lower I_{ON} for the 5 nm NW is due to the larger band gap with respect to the 10-nm case.

As can be seen in Fig. 24.16b, for small ΔE_V, I_{ON} decreases because the electric field at the junction is reduced (cfr. Eq. (24.33)); hence, this simple model reveals the condition that ΔE_V has to be a substantial fraction of E_G in order

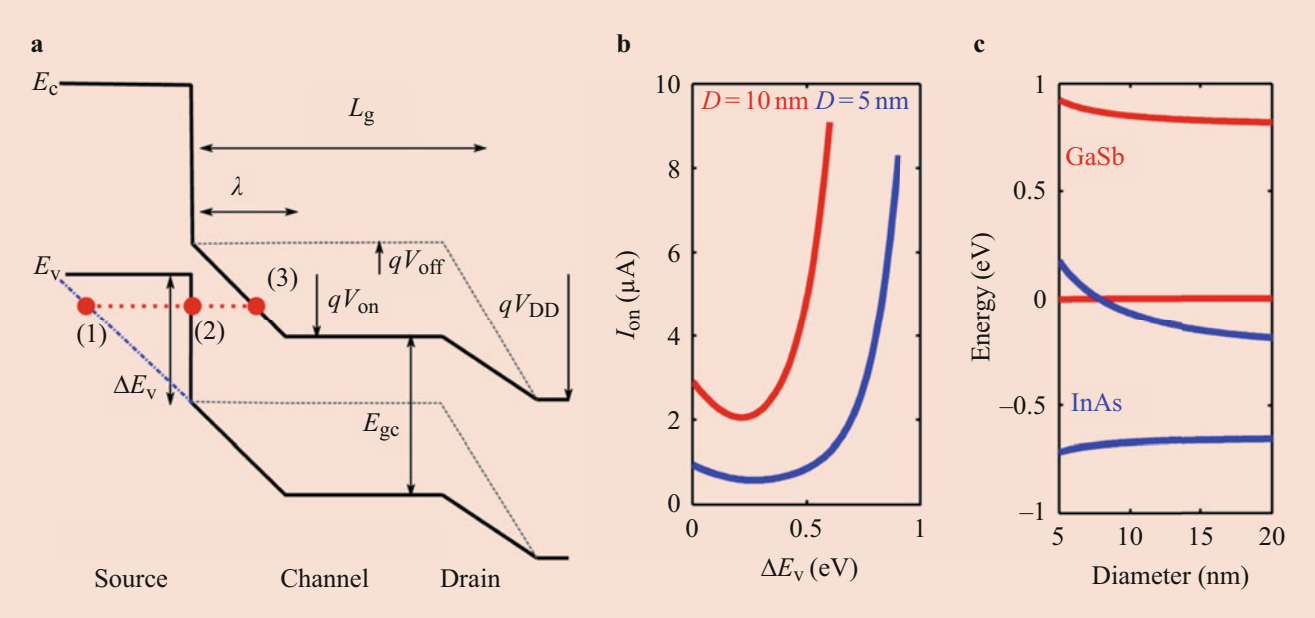

Fig. 24.16 (**a**) Schematic band diagram of a staggered band gap nTFET. Solid (dotted) lines represent the band edges for the device ON (OFF) state. The tunneling path of the heterojunction TFET occurs from point (2) to point (3), while for the homojunction TFET, the same path occurs from point (1) to point (3). (**b**) Calculated ON current vs. valence band offset, ΔE_V, for InAs nanowire having diameter $D = 10$ nm and $D = 5$ nm. (**c**) Conduction and valence subband edges for GaSb and InAs. (Figure from Lind [80])

to observe an improvement in the ON-state performance. For the InAs/GaSb materials system, for a 5-nm-diameter wire, $\Delta E_V \approx 0.18$ eV, while a broken gap band alignment is expected for NW diameters greater than 8 nm (Fig. 24.16c). The use of ternary compounds such as $In_xGa_{1-x}As$ and AlGaSb can be exploited to obtain the desired alignment. However, in a heterostructure TFET, a careful accounting of the effective tunneling gap is required in order to correctly interpret the device measurements. A calibrated simulation of a p-i-i-n $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ Esaki diode by Bizindavyi [81] highlighted how the temperature-dependent band gap narrowing of the heterojunction tunneling gap can be properly modeled using an adapted Varshni equation, whose fitting parameters are dictated by the individual compounds forming the heterojunction. As a result, despite the fact that the effective band gap is small, its temperature dependence is nevertheless consistent, introducing large temperature variations in the subthreshold regime, which then need to be decoupled from other parasitic mechanisms such as TAT.

The EHB TFET can also benefit from the use of heterojunctions to reduce the tunneling barrier and cut down voltage required to align the electron and hole eigenstates. As a result, the tunneling probability and current can significantly increase while at the same time lowering the device operating voltage. Additionally, due to the impact of quantization, one can engineer the thickness of the two materials constituting the heterojunction to modulate the electron and hole confinement energies. This is exemplified with the aid of the band diagram of Fig. 24.17 in which a narrow, trapezoidal p-

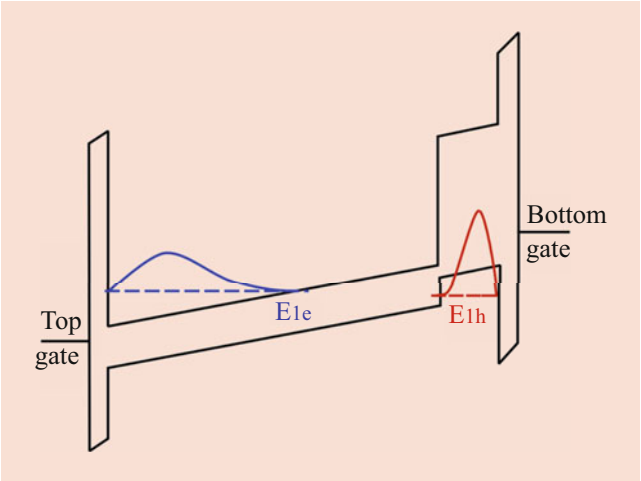

Fig. 24.17 Schematic band diagram of a heterojunction EHB TFET

quantum well defines a hole eigenstate energy that is almost "pinned" as a function of the gate bias, while the n-well width can be optimized to allow for the maximum gate efficiency [58].

24.9.1 Vertical Heterojunction TFET

Realizing high-performance HTFETs requires the growth of electronic-quality crystalline materials to minimize defect and interface trap densities and variability and create

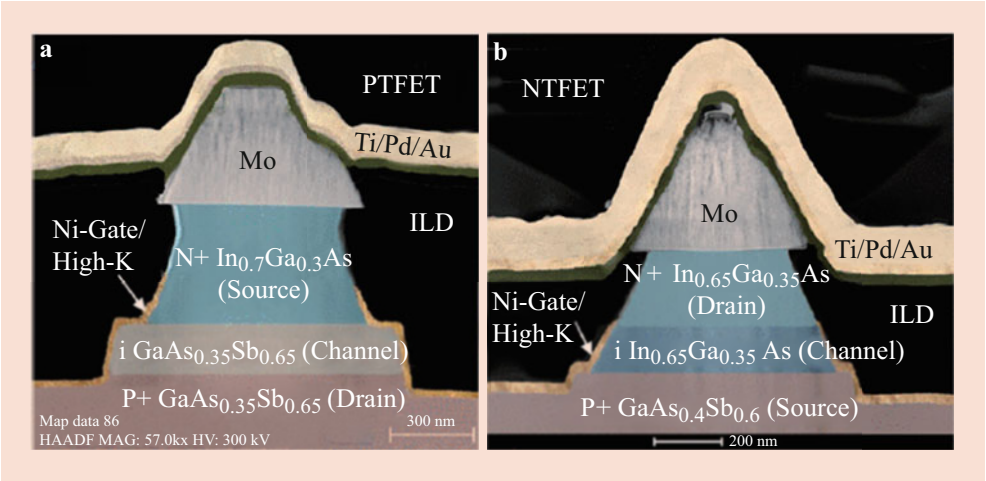

Fig. 24.18 (**a**) Cross-section transmission electron microscope images of the Sb-channel pTFE and (**b**) the As-channel nTFET. (Figure from Pandey [85])

abrupt tunnel junctions. Efficient gate control requires the deposition of low EOT gate stacks with minimal density of interface and border traps. Since the early demonstration by Baba [82], molecular beam epitaxy (MBE) has been widely utilized to achieve atomically controlled interfaces and high degenerate doping densities. In the sidewall approach, a p + in+ heterojunction is grown by MBE and then etched to form a mesa. The gate dielectric is deposited by atomic layer deposition (ALD) on the sidewalls of the etched structure [83, 84], and modulation of the channel conduction is at the sidewall of the mesa with current flowing vertically. In 2015, Pandey [85] demonstrated As-channel nTFETs and Sb-channel pTFETs for complimentary III–V TFET logic applications. The transmission electron microscope (TEM) cross sections of the $GaAs_{0.35}Sb_{0.65}$ pTFET and the $In_{0.65}Ga_{0.35}As$ nTFET are shown in Fig. 24.18a, b, respectively. This work highlighted the separate optimizations required for the deposition of high-κ dielectrics on the different III–V channel materials, which is essential for achieving both high ON currents and steep SS. For the pTFET, the process consisting of an H_2 plasma clean, for the desorption of the native oxide, followed by ALD of 3.5 nm of HfO_2 to achieve the highest accumulation capacitance on the $GaAs_{0.35}Sb_{0.65}$ channel, the gate stack on the nTFET $In_{0.65}Ga_{0.35}As$ channel used a 4-nm ZnO_2 gate dielectric with its own specialized clean.

Vertical heterojunction TFETs have also been demonstrated in alternative geometries, with the tunneling oriented in line with the gate. Li [86] and Zhou [87] demonstrated TFETs in this geometry with Zhou achieving ON current densities up to 180 μA/μm ($V_{DS} = 0.5$ V) using the InAs/GaSb heterojunction broken gap tunnel junction [87]. While the III–V materials are well suited to HTFET demonstrations, adding these to a CMOS process requires the addition of two transistors and a cost-effective approach for growing or transferring III–V to Si substrates.

24.9.2 Lateral Heterojunction TFET

Lateral HTFETs have also been explored as an approach for co-integrating TFETs in a foundry-like complementary process. The key issue is the formation of self-aligned, steep-doping, and high-quality source tunnel junctions. Utilizing group IV materials, Takagi [88] demonstrated an HTFET comprised of a Ge source and strained SOI channel. This design exploits the benefits of the staggered heterojunction between Ge, which presents a higher E_V with respect to Si and the lower E_C of strained Si, which results in a reduction of the tunneling band gap at the source for improved ON currents while maintaining the large band gap of strained Si at the drain to suppress the ambipolar current branch.

For III–V materials, much of the early work was focused on optimizing the doping processes to achieve steep tunnel junctions, mainly in a homojunction TFET configuration. In this context, studies on solid-phase Zn-diffused source junctions in InGaAs achieved p^+ doping profiles as steep as 3.5 nm/decade [88, 89]. Using this approach, an $In_xGa_{1-x}As$ quantum well TFET was proposed [90]. The quantum well is formed by tuning the In content in a $In_{0.53}Ga_{0.47}As$/ $In_xGa_{1-x}As$/ $In_{0.53}Ga_{0.47}As$ heterostructure. The higher In content results in a smaller band gap in the quantum well, thus improving the BTBT current, while the larger band gap of the Ni-InGaAs alloy present in the drain region reduces the ambipolar conduction.

IBM pioneered the development of a template-assisted selective epitaxy (TASE) technique that utilizes metal organic chemical vapor deposition (MOCVD) growth of III–V materials directly on an SOI substrate [91]. In brief, the method consisted of first defining the device region by patterning the SOI substrate. The Si body was then covered with an oxide and subsequently etched back selectively while leaving a Si seed. Selective III–V epitaxy was then carried out

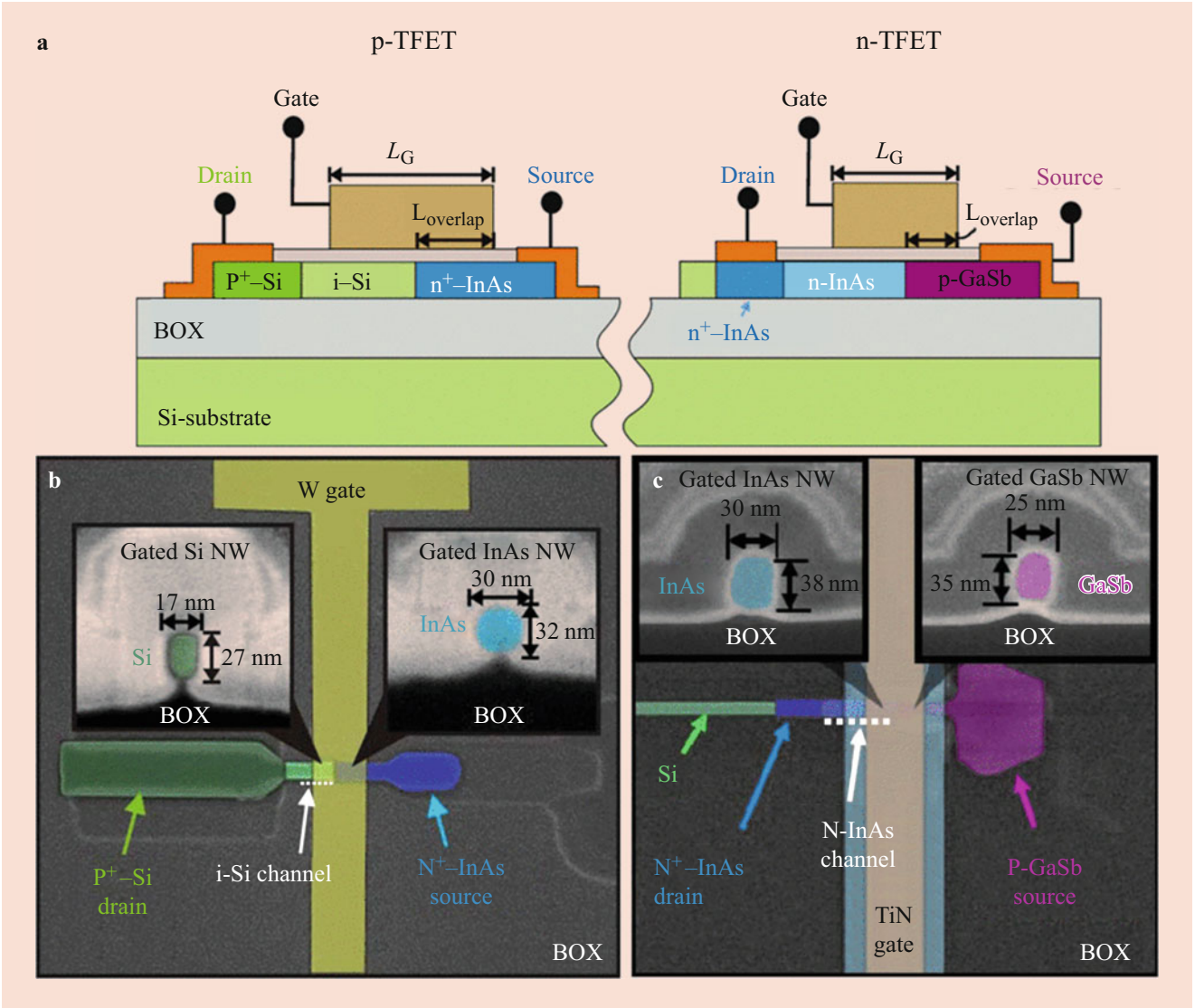

Fig. 24.19 (**a**) Schematic cross section of the pTFET and nTFET fabricated via TASE. Scanning electron microscope image of the top view of the (**b**) pTFET and (**c**) nTFET, respectively. (Figure from Cutaia [92])

inside these hollow structures starting from the Si seed. The oxide template was then removed, and the device fabrication was completed using more conventional processes. Details of TFET gate stack formation and contact deposition were reported by Cutaia [92]. Figure 24.19a shows the TFET schematic cross sections: the p-channel HTFET consisted of an n^+ InAs source, a gated i-Si channel, and a p^+ Si drain, whereas the n-channel HTFET used a p-GaSb/n-InAs/n^+-InAs heterostructure. As can be shown from the device schematics, an overlap region is present at the source side since the gate formation is not self-aligned with respect to the tunneling junction. Scanning electron microscope (SEM) images showing the top view of the fabricated HTFETs are shown in Fig. 24.19b, c for the pTFET and nTFET, respectively, and the insets elucidate the geometry of the III–V nanowire channels. The SS of the InAs/Si pTFET was approximately 70 mV/dec, with current drives of ~4 μA/μm, at $V_{GS} = V_{DS} = -0.5$ V. The InAs/GaSb nTFET exhibited ON currents reaching approximately 40 μA/μm, with much larger SS (>1 V/decade) due to an unoptimized geometry and source doping [92]. Moreover, a significant temperature dependence was observed in the subthreshold regime, suggesting TAT. This work documented an innovative approach to the monolithic integration of planar complementary HTFETs on Si.

24.9.3 Vertical Nanowire HTFET

Vertical nanowire HTFETs have achieved the best device performance for nTFETs in any materials system and in

any geometry to date, e.g., [93]. Nanowire HTFETs with wraparound gates enable superior electrostatic control, which improves both SS and I_{ON}. Suppression of ambipolar conduction through a gate underlap at the drain/channel junction has been implemented without increasing the device footprint, and the approach allows the integration of staggered or broken gap heterojunctions with large lattice mismatch and low defect density due to radial strain relaxation [69].

Best device results have been achieved through a bottom-up approach for the nanowire growth by means of metalorganic vapor phase epitaxy utilizing the vapor-liquid-solid growth starting from Au-seeds [93]. The III–V heterostructure consists of an n^{++}-InAs/n^{-}-InAs/p^{++}-GaAsSb/p^{++}-GaSb as reported by Memisevic [93] and is shown in Fig. 24.20a, where the band alignment at the heterojunction is tunable by substituting the ternary GaAsSb compound with quaternary $In_xGa_{1-x}As_ySb_{1-y}$ [69, 94, 95]. One peculiar feature of these heterostructures is represented by the larger diameter of the GaSb segment with respect to the InAs, which makes the gate metal deposition nearly self-aligned to the tunneling junction, thanks to its "shadowing" effect (Fig. 24.20b). Best $I_{60} = 0.3$ μA/μm at $V_{DD} = 0.3$ V was measured (Fig. 24.20c), and benchmarked device performance showed the performance benefits of this approach versus best TFET reports (see Sect. 24.11).

The same growth method has also been exploited to realize GaSb/InAs core-shell nanowires, where the tunneling occurs in the radial direction [96]. A core-shell nanowire TFET can increase the in-line tunneling current at fixed device footprint. Vasen [97] demonstrated a vertical GAA core-shell nanowire nTFET based on an InAs/GaSb heterostructure. The device consisted of an n^{+}InAs stem, a GaAs barrier layer, and a p^{+}GaSb source. The nanowire was clad by an undoped InAs shell that covered the whole structure. Room-temperature subthermal SS, down to 40 mV/dec, was obtained at low V_{DS} (10 mV), as well as ON currents up to 40 μA/wire at $V_{DS} = 0.3$ V, for a 50-nm-diameter device. Double sweep transfer characteristics showed low hysteresis, with distinct current steps attributed to TAT and thermal emission at the InAs/high-κ interface.

Another notable approach for the selective area growth of III–V nanowires directly on Si has been reported by Tomioka and Fukui [98]. Despite the large lattice mismatch and mismatch in thermal conductivity, HTFETs were demonstrated starting from a p^{+} (111) Si substrates covered with 20 nm of SiO_2, with 30- to 90-nm-diameter etched windows through the oxide layers to enable growth on Si. The vertical nanowire growth proceeds from the openings to yield an undoped InAs channel and a Si-doped n^{+}InAs drain to form the vertical nanowire heterostructure. Steep SS TFETs were fabricated through optimization of the nanowire geometry [99].

III–V HTFETs have also been notably realized via a top-down approach starting with an MBE III–V heterostructure [100]. Zhao demonstrated subthermal swings of 53 mV/dec and $I_{60} = 4.3$ nA/μm at $V_{DS} = 0.3$ V [101]. The tunneling heterojunction consists of a p + $In_{0.53}Ga_{0.47}As$ source, a 2-nm i-InAs/8-nm i-$In_{0.7}Ga_{0.3}As$ "notch," and an i-$In_{0.53}Ga_{0.47}As$ channel. The notch serves to reduce the tunnel barrier height and yield steeper SS and higher ON current. Careful control of the etching and passivation steps yielded highly vertical and smooth sidewalls. The process avoided the need for metal catalysts like Au.

24.9.4 Layered Two-Dimensional HTFET

The energetic abruptness of the band minima and maxima in the TFET can be degraded by atomic-scale variations in body thickness, dopant fluctuations, trap states resulting from dangling bonds, and thermal fluctuations. Two-dimensional (2D) van der Waals materials present some intriguing attributes with respect to HTFETs. They are intrinsically atomically smooth surfaces and, ignoring defects' they have no surface dangling bonds [102, 103]. 2D materials can be prepared atomically thin representing the ultimate in body thickness scaling, thus enabling best case single- or double-gate electrostatic control. Given the ability to obtain abrupt pn junctions, BTBT is possible [102, 103]. A cornucopia of layered materials is available, and there is no fundamental impediment to stacking dissimilar 2D materials to make heterojunction tunneling devices. Impediments to utilizing these materials are the difficulty in nucleating oxides on surfaces free from dangling bonds; the weak forces holding the layers together mean that they easily translated when temperature is cycled or in the presence of strain. Substitutional doping is not well established, so electrostatic doping schemes using charged surface layers are being developed and utilized.

Graphene represents the most well-studied material within this group of 2D materials; however, since it is a zero-band gap semiconductor, symmetry-breaking methods need to be adopted in order to open up a band gap. BTBT device architectures based on laterally confined graphene nanoribbons have been proposed [104] and demonstrated [105, 106]. Tuning of the transport band gap in bilayer graphene with a vertical electric field [107] has also been proposed as a control mechanism [108].

Semiconducting transition metal dichalcogenides (TMDs) have served as a first test bed for steep transistors. Layered TMDs have the form of MX_2, where M is a transition metal (e.g., Mo, W, Hf) and X is a chalcogen atom (e.g., S, Se, Te), and each layer is composed of a three-atom thick sheet where the metal atom is sandwiched in between the two chalcogenides. TMDs exhibit a wide range of band gaps that are suitable for the realization of atomically thin-body TFETs [109–114] or present favorable band alignments for HTFETs by stacking layers of different TMDs, bonded by

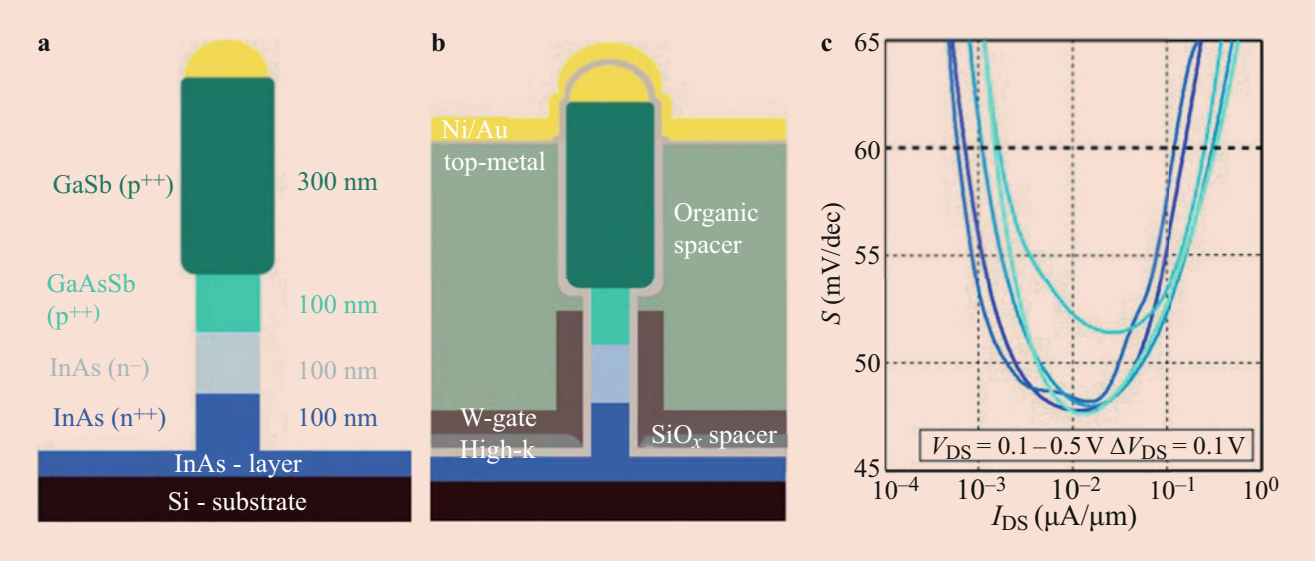

Fig. 24.20 (**a**) Schematic of the completed nanowire heterostructure growth and (**b**) cross section of the InAs/GaAsSb/GaSb HTFET. (**c**) Measured subthreshold swing vs. drain current for various V_{DS}. (Figure from Memisevic [93])

van der Waals interactions [115–118]. In striking contrast with respect to conventional heterostructures formed between epilayers of group IV or III–V semiconductors, TMD heterostructures can be formed among materials with highly mismatched crystal structures. Tunneling then occurs in the overlap region of the two layers, perpendicular to the gate. Such 2D HTFETs still maintain the advantages of conventional bulk heterostructures. Moreover, the same stacking method can also be employed to form 3D/2D heterostructures, as shown by Sarkar using bilayer MoS_2 on top of a bulk Ge source [119].

24.9.5 III-Nitride HTFETs

III-nitride materials , such as GaN and InN, present another intriguing materials system for TFET design with band gaps of 3.4 eV and 0.7 eV, respectively. The wideband gap GaN can be utilized to provide low OFF-state currents, while the narrower gap InN can be utilized in the tunnel junction. In Fig. 24.21a, Li shows the simulated energy band diagram of a GaN pn homojunction with symmetric abrupt doping of $N_D = N_A = 3 \times 10^{19}\text{cm}^{-3}$ highlighting how, despite the degenerate doping levels, the tunneling width $\Lambda \approx 15$ nm due to the large energy built-in voltage [120].

The III-nitride materials system features spontaneous and piezoelectric polarization which results in uncompensated sheet charge densities at heterointerfaces between materials exhibiting different internal polarizations. If properly engineered as in the case of GaN/InN/GaN heterostructures, the polarization-induced sheet charges can generate large built-in fields on the order of 20 MV/cm, five times higher than can be obtained using heavy doping in groups IV and III–V tunnel junctions [121]. Figure 24.21b, c illustrates this concept and shows the tunability of the effective energy gap for tunneling by adjusting the InN layer thickness. As a function of the InN interlayer thickness, the band alignment changes from staggered (Fig. 24.21b) to broken gap (Fig. 24.21b). As in conventional heterostructures, the tunneling energy gap can be tuned further by adjusting the In molar fraction of an $In_xGa_{1-x}N$ tunneling layer.

The III-nitride in-line TFET proposed by Li [120] is shown in Fig. 24.21d, together with the corresponding band diagrams of the device in the OFF (Fig. 24.21e) and ON states (Fig. 24.21f) to elucidate the operational principles. In the OFF state, the conduction band in the channel is pulled to energies that cut off available states for tunneling, and the large GaN band gap suppresses the OFF-state leakage current. In the ON state, a tunneling energy window is opened, and electrons can tunnel from the p-type source to the n-type channel, through the narrow gap of InN. In maximizing the III-nitride HTFET I_{ON}, an optimum InN thickness exists since increasing the thickness has the effect of increasing the tunneling distance which reduces the tunnel current but also shifting the band alignment from staggered to broken gap which increases tunnel current.

Several technological hurdles need to be overcome for the optimization of the GaN-based TFETs. Incomplete ionization of deep-level acceptors represents a major obstacle since a significant depletion width in the source leads to a pronounce superlinear onset in the output characteristics and a reduction of the BTBT current by widening the tunneling path. Polarization engineering of graded $In_xGa_{1-x}N$ layers in between the InN interlayer and the p-type GaN source may

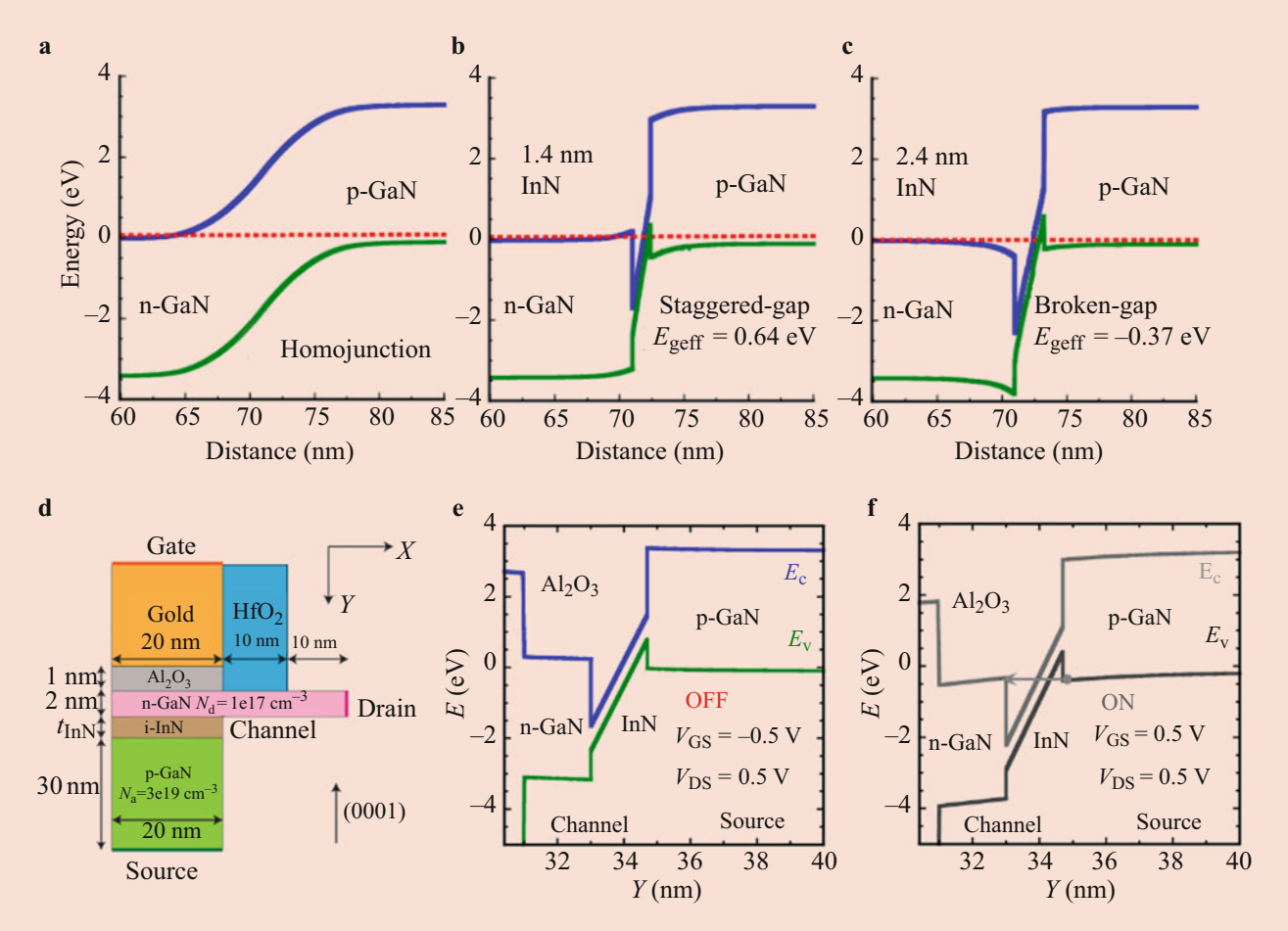

Fig. 24.21 Comparison of computed band diagrams for a (**a**) GaN pn junction and GaN/InN/GaN heterojunctions having an InN interlayer thickness of (**b**) 1.4 nm and (**c**) 2.4 nm, respectively. In a III-nitride heterojunction, the band alignment can be tuned by changing the InN interlayer thickness. (**d**) Proposed in-line III-nitride HTFET design and corresponding band diagrams of the device (**e**) OFF and (**f**) ON state. (Figure from Li [120])

mitigate this effect [122]. The epitaxial growth of GaN/InN/GaN heterostructures is challenging due to the significant difference in optimal growth temperature for the two alloys and their lattice mismatch [120]. Li [120] simulated the I_{ON} dependence on the In molar concentration for the case of a GaN/$In_xGa_{1-x}N$/graded-InGaN/GaN TFET. A reduced In molar concentration results in larger tunneling energy gap, smaller polarization charges due to a reduced piezoelectric contribution, and thus smaller electric fields leading to a significant degradation of the BTBT current.

Performance projection for GAA III-nitride nanowire TFETs by Li [123] quantified the benefits of the relatively large DOS masses ($m_E = 0.2, m_H = 1.5$), namely, a mitigation of quantization effects. The latter though starts playing a significant role in increasing the tunneling gap for sub-10 nm NW diameters. It is found that a diameter around 20–30 nm should offer a good compromise between electrostatic integrity and ON-state performance.

Through quantum simulation accounting for the different multiphysics processes at play, Ameen [124] pointed out that in order to optimize the subthreshold characteristics of III-nitride TFETs, carrier thermalization through confined state at the heterointerface must be prevented. Due to the high electric fields at the heterojunction, confined states are induced at the source, which inject hot carriers over the channel barrier in the OFF state, degrading the steepness of the TFET's turn-on. A well-designed structure is aimed to reduce the number of these confined states, i.e., shallow quantum wells, while also keeping the induced polarization intact. It is proposed that this can be achieved by adopting a 3.5-nm-thick $In_{0.9}Al_{0.1}N$ as the interlayer and an $In_{0.75}Ga_{0.25}N$ channel in spite of the InN and GaN materials [124].

Experimental demonstrations of steep III-nitride TFETs are only just emerging. Chaney [125] reported a surrounding gate GaN/$In_{0.25}Ga_{0.75}N$/GaN NW TFET, formed from a top-down approach. The extracted SS was reported to be approx-

imately 110 mV/dec and with ON current of 30 μA/μm at $V_{DS} = 1$ V. Current saturation was observed in the device output characteristics in conjunction with the suppression of the TFET ambipolar branch.

24.10 Band Tails

In TFETs, the spectral shape of the semiconductor band edge, the band-tail states, controls the steepness of the current-voltage characteristics as the tunneling window closes [126]. The spectral shape of the band edge is observed experimentally to be exponential, often called the Urbach tail [127]. Smearing of the band edge can be anticipated from lattice thermal vibrations, heavy-doping effects, dopant inhomogeneity, structural disorder, and size quantization in transistors resulting from semiconductor inversion layers and ultrathin-body transistors.

A method to investigate band-edge steepness directly from transport was proposed by Agarwal and Yablonovitch [128]. An analytical treatment was developed that correlates the joint density of states (DOS) in an Esaki/backward diode to the absolute conductance of the DC characteristics, by measuring the conductance slope in the NDR region of the I–V characteristic of a tunnel diode, and predictions about the corresponding steepness of the TFET SS were derived based on this extraction.

At the core of the method stems the observation that, for a tunnel diode, a semilog plot of absolute conductance $|G|$ vs. applied voltage, V, decreases smoothly going from negative voltages, backward diode branch, to positive voltage within the forward Esaki tunneling branch. This aspect offers the possibility of a physical interpretation in terms of the semiconductor intrinsic properties.

Considering the joint DOS, $D_J(E)$ taking into account the valence band states on the p-doped side of the junction and the conduction band states on the n-doped side, the tunneling current can be expressed as [128]

$$I \propto \int (f_C(E) - f_V(E))\, T_{BTBT} D_J(E) \mathrm{d}E \tag{24.36}$$

where $f_C(E) - f_V(E)$ represents the difference of the Fermi-Dirac occupation probabilities at two sides of the junction. A qualitative plot of $D_J(E)$ at various bias points is shown in Fig. 24.22d–f. For simplicity, the conduction and valence band tails roll off exponentially with the same slope. As the conduction and valence band edges uncross in forward bias, the band tails still overlap, and $D_J(E)$ decreases exponentially. In Fig. 24.22d–f, the area under the difference in occupation function is proportional to the applied voltage. By multiplying and dividing (24.36) by the integral $\int f_C(E) - f_V(E) \mathrm{d}E$

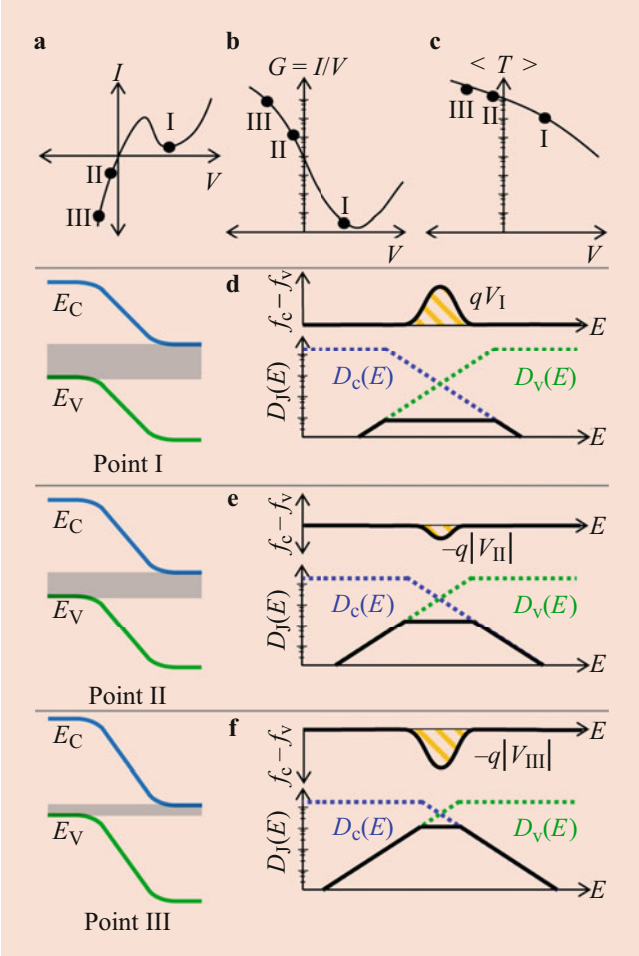

Fig. 24.22 (**a**) I–V curve, (**b**) absolute conductance G-V curve of an Esaki diode. (**c**) Tunneling probability vs. applied bias. Qualitative band diagrams, Fermi-Dirac occupation probability difference, and $D_J(E)$ corresponding to bias points (**d**) I, (**e**) II, and (**f**) III, respectively. (Figure from Agarwal and Yablonovitch [128])

$$\begin{aligned} I &\propto \int (f_C(E) - f_V(E))\, \mathrm{d}E \frac{\int (f_C(E) - f_V(E))\, T_{BTBT} D_J(E) \mathrm{d}E}{\int (f_C(E) - f_V(E))\, \mathrm{d}E} \\ &\propto qV \frac{\int (f_C(E) - f_V(E))\, T_{BTBT} D_J(E) \mathrm{d}E}{\int (f_C(E) - f_V(E))\, \mathrm{d}E} \\ &= qV \langle T_{BTBT} D_J(E) \rangle \end{aligned} \tag{24.37}$$

where the terms $\langle T_{BTBT}\, D_J(E) \rangle$ indicate a weighted average of the product $T_{BTBT} D_J(E)$ over the Fermi window. As pointed out in [128], the ratio $f_C(E) - f_V(E)/V$ barely changes for $|V| < 4k_BT$; hence, within this range, the change in conductance is governed by the change of $T_{BTBT}\ D_J(E)$ (even for the case $|V| > 4k_BT$, the exponential change of T_{BTBT} $D_J(E)$ dominates despite a correction due to the broadening of $f_C(E) - f_V(E)/V$). Therefore, the steepness of the absolute conductance is related to the steepness of D_J by

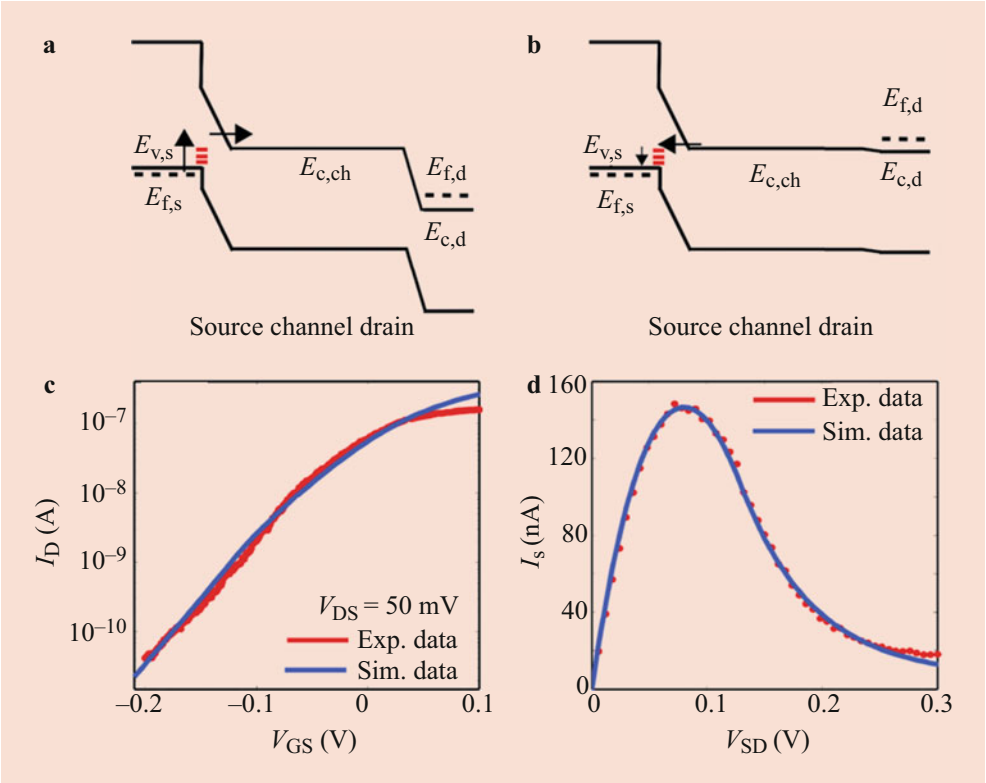

Fig. 24.23 (**a**) Schematic band diagram for a heterostructure TFET in the OFF state (**b**) and in the NDR region, respectively. (**c**) Experimental vs. model transfer characteristics. (**d**) Fitting of the output characteristic in the NDR region. (Figure from Memisevic [94])

$$SS_{T-D_J} = \left[\frac{d\log\langle T_{BTBT} D_J(E)\rangle}{dV}\right]^{-1} \approx \left[\frac{d\log(I/V)}{V}\right]^{-1} \tag{24.38}$$

expressed in mV/dec. While the voltage dependence of the conductance slope can be dominated by either the change in tunneling probability or the joint DOS, Eq. (24.11) showed that for large tunneling probabilities, i.e., large current densities, the change in tunneling probability is small, and thus the conductance slope is determined by the exponential change of D_J. While this analysis has been carried out for a two-terminal Esaki diode, a TFET is a three-terminal device, and this implies that by measuring the SS from the transfer characteristics, the impact of the DOS switching needs to be distinguished from the degradation induced by nonideal electrostatics. On the other hand, if the critical tunneling junction lies at the source-channel interface, a two-terminal-like measurement can be accomplished by fixing the $V_G - V_D$ voltage while measuring the I_D– V_S characteristics. In this manner, the drain voltage will not have an impact on the channel potential which is controlled by the gate bias.

Starting from a similar argument, Memisevic [94] proposed a simple model to link the band-edge decay parameter, i.e., Urbach energy, to the NDR current swing, instead of the conductance swing [128], and compare it with the subthreshold swing obtained from measurements of a III–V HTFET. Figure 24.23a shows the schematic band diagram of an HTFET in biased in the OFF state of the device. The conduction band in the channel, $E_{C,\,Ch}$, lies at higher energy than the source valence band edge, $E_{V,\,S}$. Despite the fact that the uncrossing of the bands suppresses BTBT, exponentially decreasing band gap states close to the valence band opens up an alternative tunneling path. This impact as well the NDR region of the HTFET for a V_{SD} bias past the peak voltage is shown in Fig. 24.23b. Assuming an energy decay parameter, E_0, the described OFF-state decay current can be expressed as

$$I_{OFF} = \frac{2q}{h}\int_{E_{C,CH}}^{+\infty} T_N(E)\,[f_S(E) - f_D(E)]\exp\left(-\frac{E}{E_0}\right)dE \tag{24.39}$$

where T_N is the tunneling transmission. In the device OFF state, it is assumed that only charges in the Fermi tails contribute to transport, such that the source Fermi-Dirac distribution can be simplified with its Boltzmann approximation, and V_{DS} is large enough such that the drain occupation function can be omitted. Additionally, T_N is considered to be energy-independent, such that Eq. (24.39) simplifies to [94]

$$I_{OFF} \propto \int_{E_{C,CH}}^{+\infty} \exp\left(-\frac{E}{E_0}\right) \exp\left(\frac{E_{FS}-E}{k_B T}\right) \propto \exp\left(-\frac{E_0 + k_B T}{E_0 k_B T} E_{C,CH}\right) \tag{24.40}$$

The conduction band in the channel is modulated by the gate voltage; however, the presence of interface traps degrades the gate efficiency:

$$-\frac{\partial E_{C,CH}}{\partial V_{GS}} = \frac{q}{1 + \frac{C_{IT}}{C_{OX}}} \tag{24.41}$$

and C_{IT} represents the interface trap capacitance. Using the definition of Eq. (24.1), SS is equal to

$$SS = \left[\frac{d \log_{10} I_D}{dV_{GS}}\right]^{-1} = \underbrace{\ln(10)\frac{k_B T}{q}}_{60\,mV/dec} \left(1 + \frac{C_{IT}}{C_{OX}}\right) \frac{E_0}{E_0 + k_B T} \tag{24.42}$$

Equation (24.42) states that subthermal slopes can be obtained in the case of exponentially decaying band tails limiting the OFF-state current. The presence of band tails results also in temperature-dependent swings. Additionally, Eq. (24.42) highlights how subthermal swing can be achieved even in the case of E_0 >60 meV. However, interface traps deteriorate the SS.

To determine E_0 independently, an expression for the current in the NDR must be evaluated. In order to observe NDR, $E_{FD} \gg E_{C,CH}$, such that degenerate conditions in the channel are met (Fig. 24.23b), assuming that the source valence band is shifted by an amount qV_S, the drain current exhibits an exponential dependence on the source voltage [94]:

$$I_S = \frac{2q}{h} T_N \int_{E_{C,CH}}^{E_{FS}} \exp\left(-\frac{E}{E_0}\right) dE \propto \exp\left(-\frac{qV_S}{E_0}\right) \tag{24.43}$$

The method laid out by Memisevic [94] consists of fitting the exponential decay in NDR region to obtain E_0, while the subthreshold swing reveals a dependence on E_0, T, and C_{IT}. The results of the analytical model are compared with experiments in Fig. 24.23c, d for the transfer and output characteristics, respectively, showing good agreement with experiments. The BTBT current is computed using Eqs. (24.32) and (24.35).

The models developed in [94] and [128] do not allow for a quantitative extraction of the band-tail DOS. Recent work by Bizindavyi [129] describes a calibration method based on semiclassical transport models of the tunneling contribution stemming from high doping induced band tails to match experimental p-i-n Esaki diode I–V data. Starting from a spherically symmetric dispersion relation, an expression of the conduction and valence band-tail DOS was derived, as shown in Fig. 24.24a. The band-tail DOS is constituted of spatially extended states within the first 100 meV from the unperturbed band edges, with an abrupt transition to strong localized states deeper into the band gap. For a p-i-n Esaki diode, only band-tail states stemming from the majority

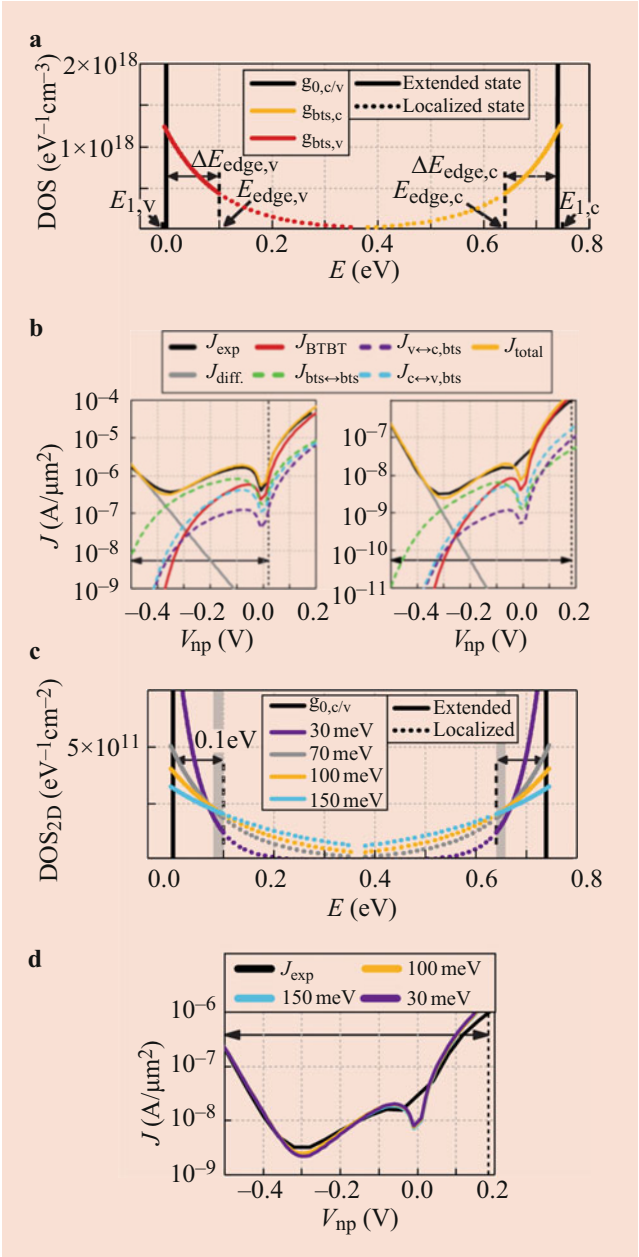

Fig. 24.24 (**a**) Conduction band tails (red), valence (gold) band tails, and (black) unperturbed DOS. (**b**) Calibrated I–V results for $In_{0.53}Ga_{0.47}As$ p-i-n Esaki diodes with (left) 9 nm and (right) 18-nm intrinsic region. (**c**) Calibrated 2D band-tail DOS for different values of the Urbach energy, E_0. Gray-shaded area represents the first 20% of the extended band-tail DOS. (**d**) Calibrated I–V simulation results for the p-i-n Esaki diodes with 18-nm intrinsic region varying the Urbach decay factor. (Figure from Bizindavyi [129])

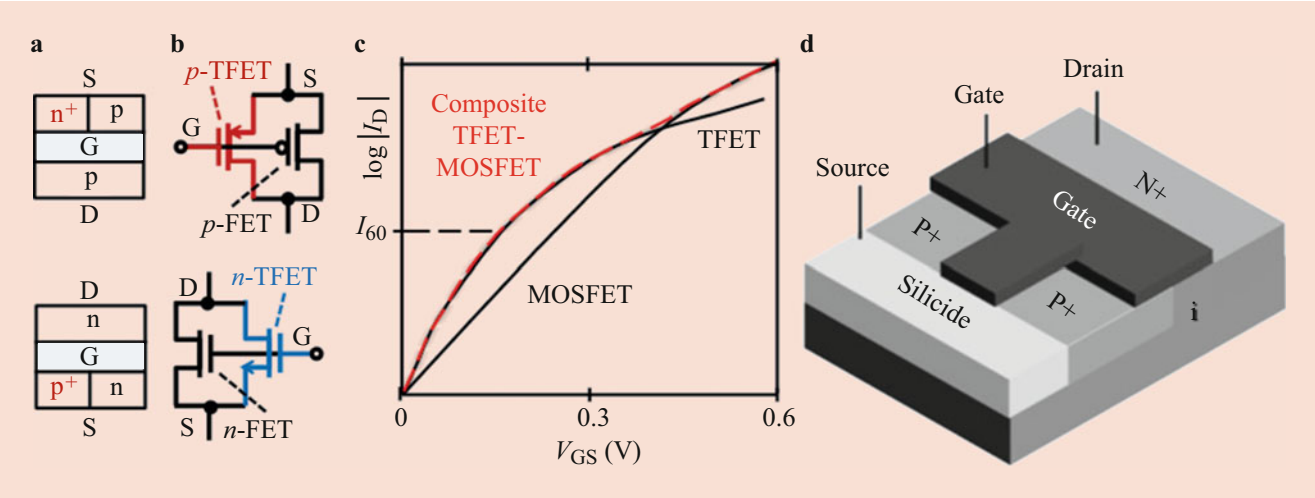

Fig. 24.25 Composite TFET-MOSFET. (**a**) Planar top view of the transistor showing how both pTFET/pMOSFET and nTFET/nMOSFET can be combined into a single transistor. (**b**) Circuit schematic showing the connection of the two transistors in parallel. (**c**) Schematic showing the two transistor currents summing to yield the composite transistor characteristic. (**d**) Refined implementation of the composite nTFET /nMOSFET after Zhan [132]

bands, valence or conduction bands on the p+ or n+ doped sides of the junction, contribute significantly to the tunneling current (Fig. 24.24b). A good match for two different Esaki diodes with the intrinsic region thickness of 9 and 18 nm, respectively, is obtained.

From a careful analysis of the current spectral contribution, it is found that it is not the Urbach energy factor, E_0, alone, but rather the integrated DOS within the first ~20% energy window close to the transition point between extended and localized band-tail states that is actually being calibrated (Fig. 24.24c). In fact, the DOS in the shaded area of Fig. 24.24c is actually comparable for multiple E_0 values. This aspect was missing in the analytical arguments presented above.

Bizindavyi [129] and coauthors also looked at these implications in a TFET configuration. Similar to the Esaki diode case, it is the integrated band-tail DOS, not E_0, that affects the SS. The effect of the band tail is to reduce the onset voltage of the device, which decrease the I_{ON}–I_{OFF} ratio for a fixed V_{DD}, and therefore a deterioration of $\overline{SS}$. However, it was found that I_{60} remains unchanged for the cases investigated.

Despite the recent efforts to include the band-tail DOS in the modeling of tunneling-based devices, the impacts of dopant concentration, dopant atom species, and corresponding activation energy on the former are still poorly understood.

24.11 Composite TFET/MOSFET

It is possible to combine the low-voltage, low-power aspects of the TFET with the high-current, high-speed capability of the MOSFET in a composite structure in which the TFET controls the subthreshold transition and a parallel MOSFET is used to boost the current at higher gate voltage. The basic concept is illustrated in Fig. 24.25, for planar p and n device configurations in both (a) layout and (b) circuit schematic representations. The n-TFET in Fig. 24.25a, lower drawing, has a p-i-n doping structure from the source to the drain, while the nMOSFET has an n-i-n arrangement. A shared ohmic contact is made to both the n and p source regions, and the gate contact over the i region is also shared. The action of the two side-by-side transistors is to provide a drain current which is the sum of the two devices in parallel. The transfer characteristic of the two transistors is shown in Fig. 24.25c, where for V_{GS} lower than approximately 0.4 V the drain current is dominated by the TFET, while for voltages exceeding 0.4 V, the MOSFET current dominates.

In a series of papers by Huang and Zhan [130–133], the transistor concept was developed and refined. One of the several versions of the composite transistor structure is shown in Fig. 24.25d from Zhan [132]. Nickel silicide was used to contact the source. A T-shaped gate was utilized to provide a three-sided source tunnel injection region to the channel to increase the tunnel injection. Since the tunnel current is largely independent of gate length, the width-dependent gate length is not detrimental to the transport. The source was made symmetric with the p + source regions for the TFET set on either side of the T-gate. At high drain and gate bias, the Schottky nMOSFET turns on providing additional current over and above the TFET drive current. Huang explains in [133] that lateral self-depletion of the source p + n junction lowers the off-state current of the Schottky MOSFET relative to a traditional Schottky MOSFET, thereby lowering the OFF current of the composite transistor.

Oliva [134, 135] demonstrated the parallel transistor combination in 2D materials by connecting a steep-slope $WSe_2/SnSe_2$ TFET with a WSe_2 MOSFET to show the benefits of the combination, which they call a dual-transport steep-slope FET. The 2D materials were exfoliated, and the transistors were wired together in parallel for the demonstration. As new processes for the TFET emerge, there appears to be value in considering ways to add the parallel MOSFET.

24.12 Complex Gate Dielectrics

The subject of complex gate dielectrics for TFETs to lower the subthreshold swing is one that is receiving considerable attention especially with regard to the use of ferroelectrics [136, 137]. Any complex dielectric innovation that boosts current and lowers SS in a MOSFET (in, for example, ferroelectrics, piezoelectrics, or phase changing material) is generally also applicable to the TFET. Complex dielectrics generally have some RC delay associated with the dynamic response of the material going through its reconfiguration. Owing to the importance of these effects, the dynamics of ferroelectric and other complex dielectrics are under investigation by many groups. Any RC delay in the gate dielectric can lead to a slew rate and direction-dependent SS which influences the measured SS [138–140]. Even a conventional MOSFET can exhibit a dynamic SS, which can be shown by simply introducing a series resistance in the gate to lower the SS [141].

24.13 Technology Benchmarks

The transfer characteristics of selected best reported nTFETs are shown in Fig. 24.26. Only TFETs sustaining subthermal swings for at least a decade of change in drain current and V_{DS} <0.5 V are considered in the comparison. Additionally, I_D–V_{GS} characteristics were shifted horizontally so that the gate voltage corresponding to the device OFF state is at the origin. Experimentally this can be achieved by engineering the work function of the gate metal. Since fewer pTFET realizations have been demonstrated [142–148], with generally worse performance with respect to the nTFET counterpart, these are not included in the benchmarking plots in Fig. 24.26. A comparison between best reported pTFETs has been given by Lu and Seabaugh [20].

Across materials systems, TFETs with subthermal SS have generally not yielded ON currents exceeding 10 μA/μm with the exception being in the III–V materials system. In agreement with theoretical predictions, Group IV materials such as Si and Ge exhibit smaller I_{ON} stemming from their indirect band gap resulting in lower tunneling probability. Performance boosters such as strain engineering or Si-Ge co-integration have been employed to improve ON-state performance [88, 146, 149]. Group III–V materials such as high-In content InGaAs alloys have higher tunneling currents due to their narrower and direct band gaps [90, 150, 151]. The use of III–V heterostructures further boosts the ON currents by shortening the tunneling distance [69, 83, 93, 152, 153]. While III–V materials can provide high-performance nTFETs, the performance of p-channel devices is limited by the low conduction band DOS. The carbon nanotube TFETs [18, 154] demonstrated to date do not show the high current drives predicted by the theory [77, 155], but these transistors do not have optimized geometries. SS steeper than 60 mV/dec was reported for a 3D Ge/2D MoS_2 heterojunction by Sarkar [119]; however, TFETs relying on 2D crystal channel still require improvements in terms of material growth quality, surface preparation and deposition of high-κ oxides, control of abrupt doping profiles, and band gap engineering.

The corresponding SS vs. I_D is shown in Fig. 24.26. Remarkably, Si-based TFETs show the steepest slopes: Knoll [146] reported ~30 mV/dec for a strained Si NW, employing a Ge source TFET embodiment, Kim [149] obtained SS_{MIN} ~33 mV/dec, and Takagi [88] achieved a point slope of ~29 mV/dec. However, the steepest SS are obtained for extremely low I_D, and I_{60} of 10 pA/μm [149], or well below it. Similar considerations apply for the Ge-MoS_2 TFET demonstrated by Sarkar [119] that is reported to maintain an averaged SS ~31 mV/dec over four decades of I_D change, yet I_{60} <50 pA/μm. The multigate CNT TFET by Lu [154] reached SS_{MIN} ~34 mV/dec and a crossover between subthermal and superthermal slope at around 1 nA/μm. The reported values of I_{60} and low I_{ON} do not meet the desired device performance metrics [30, 38] to make TFETs suitable for low-power application.

On the other hand, III–V-based TFETs do not match these extreme SS, but they are able to significantly push both I_{60} and I_{ON} to higher values, thanks to the adoption of heterostructures and nanowire geometries. Alian [152] demonstrated a pocketed vertical NW InGaAs/GaAsSb TFET using a top-down approach with SS_{MIN} ~47 mV/dec and I_{60} in the range of 5 nA/μm. Within the same materials system, InGaAs/GaAsSb, Convertino [156] showed similar performance, SS_{MIN} ~47 mV/dec, and I_{60} ~10 nA/μm at V_{DS} = 0.05 V, for a lateral HTFET directly integrated on a SOI platform. In this case, a self-aligned tunneling junction was formed, thanks to a raised GaAsSb p^+ source regrown under a SiN_X spacer, after the InGaAs channel is selectively etched. A top-down approach was employed by Zhao [153] to define a 20-nm-diameter InGaAs/InAs NWs and reported SS_{MIN} ~53 mV/dec with I_{60} ~4 nA/μm at V_{DS} = 0.3 V. A significant increase in I_{60} comes from the adoption of InAs/GaAsSb/GaSb NW heterostructures [93], where the NWs used in this study were grown by

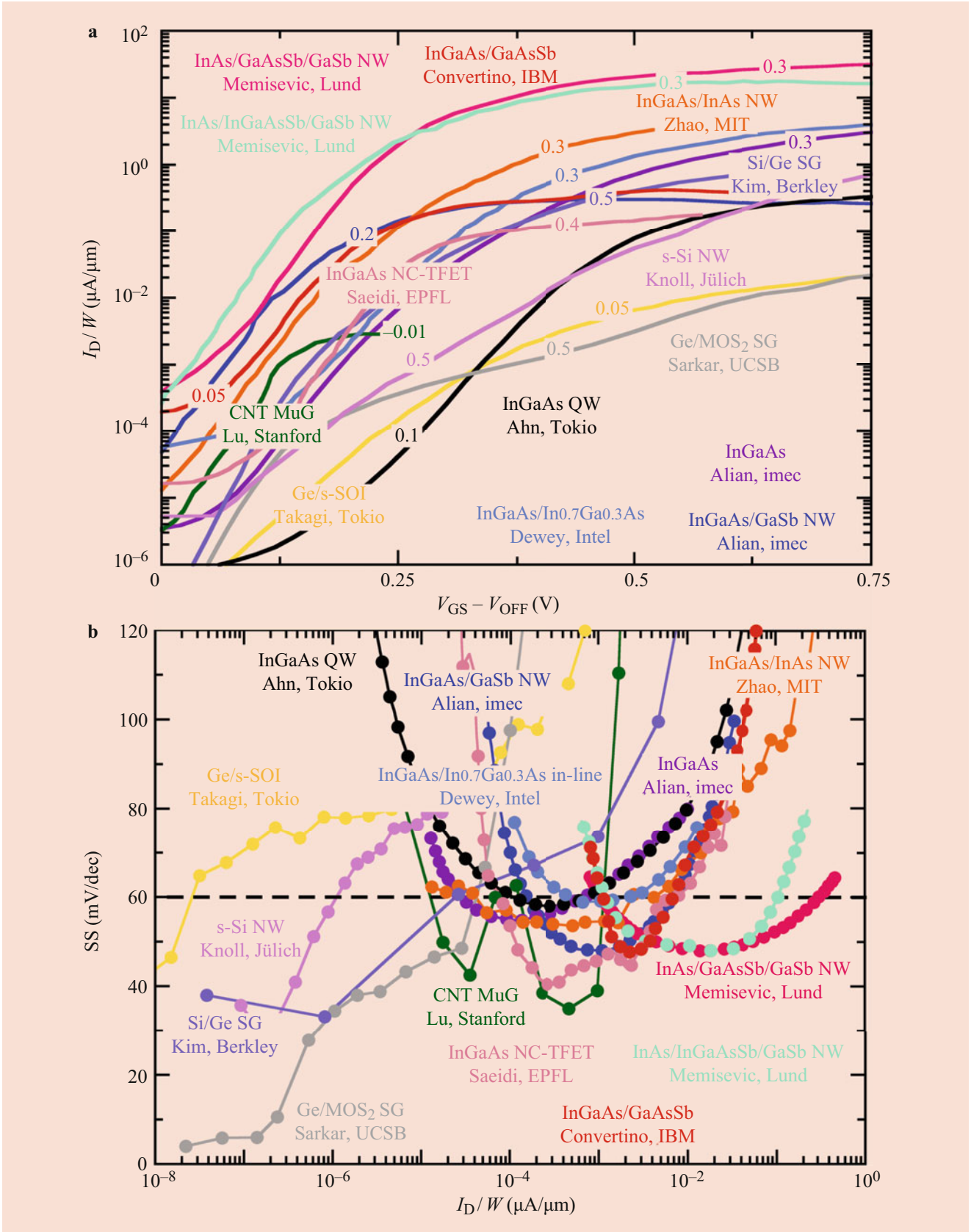

Fig. 24.26 (**a**) Comparison of published nTFET drain current per unit width versus gate-to-source voltage. (**b**) Extracted TFET SS versus drain current for the same nTFETs. Only TFETs that show SS near or below 60 mV/dec at room temperature for at least one order of magnitude change in I_D and V_{DS} <0.5 V are considered for the comparison

metalorganic vapor phase epitaxy. The devices exhibit SS_{MIN} ~48 mV/dec with I_{60} ~0.3 μA/μm at $V_{DS} = 0.3$ V, which is very close to requirements laid out by Vandenberghe [38] of SS below 60 mV/dec for current levels extending up to 1–10 μA/μm. Finally, Saeidi [151] demonstrated the coexistence of subthermal transport factor n and subunity body factor m (cfr. Eq. (24.1)) in a negative capacitance InGaAs TFET. Starting from an InGaAs TFET with SS_{MIN} ~55 mV/dec and I_{60} ~0.1 nA/μm, the addition of a PZT ferroelectric capacitor connected in series to the gate of the TFET resulted in the improvement of the abruptness of the transition from the OFF to the ON state with a reduction of SS_{MIN} down to ~40 mV/dec, a 100× I_{60} enhancement, as well as a widening of the subthermal region, internal voltage amplification, all within of minimal hysteresis window, below 10 mV.

24.14 Summary and Concluding Remarks

This chapter has sought to summarize the underlying physics and key findings in the development of the TFET, from the first discussions of a low subthreshold swing TFET (2004) to the present (2019). Some specialized advances in the wide breadth of materials systems and device geometries have been omitted to focus on the concepts that are most widely applicable. There are still many materials and process advancements that are needed before TFETs can be implemented in commercial foundries. As discussed, band tails are still not well understood, and assessment of subthreshold swing limits depends on understanding these transitions. Basic and applied materials studies are still needed to unravel the transport mechanisms at I_{60} and below and to then seed innovation and optimization. For any new materials system, the MOS heterostructure is always critical, and fundamental studies are still needed to understand the nature of interface and border traps and the processes needed for optimization.

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Carbon-Based Field-Effect Transistors

25

Zhenxing Wang, Daniel Neumaier, and Max Christian Lemme

Contents

25.1 General Properties of Graphene and Carbon Nanotubes 905

25.2 Graphene-Based Transistors 906
25.2.1 Band Structure of Graphene 906
25.2.2 Basic Device Geometry and Characterization 907
25.2.3 Contact Resistance 909
25.2.4 Radio Frequency Transistors 909
25.2.5 Flexible Transistors for High-Frequency Applications 911
25.2.6 Vertical Transistors/Hot Electron Transistors 915
25.2.7 Metal-Insulator-Graphene (MIG) Diodes 918

25.3 Carbon Nanotube-Based Transistors 921
25.3.1 Band Structure of CNT 921
25.3.2 CMOS and Integrated Digital Circuits Based on CNT 922

25.4 Summary 924

References 925

Abstract

Carbon-based nanomaterials such as graphene and carbon nanotubes (CNTs) are considered as promising candidates for various applications in electronics. This chapter provides a wide-range review of different devices and applications in this field, with a focus on high-frequency analog electronics as well as digital circuits. We start from the band structure of graphene as well as CNTs to explain why these materials may outperform conventional electronic materials in specific areas. Graphene-based field-effect transistors, hot electron transistors, and metal-insulator-graphene diodes are elaborated particularly for applications in high-frequency electronics. Graphene field-effect transistors on flexible substrates are also discussed, which could exploit the excellent mechanical properties of graphene. The scope is then expanded to digital circuits with CNTs. We describe CNT-based CMOS integrated circuits, including recent prototype microprocessors with high complexity. The purpose of this chapter is to provide readers with the basic concepts on carbon-based device physics, an understanding of typical characteristics of nanoelectronic devices, and an overview of the state of the art in the field.

Keywords

Graphene · Carbon nanotube · Transistor · Diode · Flexible electronics · Digital circuit · Radio frequency electronics · Carbon-based materials · Nanoelectronics

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25.1 General Properties of Graphene and Carbon Nanotubes

Carbon-based nanomaterials such as graphene and carbon nanotubes (CNTs) are considered as very promising materials for various applications in electronics, such as high-speed electronics, optoelectronics, sensors, and so on [1, 2].

Graphene, the two-dimensional carbon allotrope, has been intensively investigated due to its excellent properties such as extraordinarily high carrier mobility (exceeding 100,000 cm^2/Vs) at room temperature [3], high saturation

velocity of 5.5 × 10^7 cm/s [4], ultimately thin body of only one atomic plane, and high flexibility as well as mechanical stability due to the strong covalent carbon-carbon bonds. In this chapter, we will first start with the band structure of graphene, followed by the basic transistor device geometry and considerations on contact optimization. Analog radio frequency (RF) transistors will also be in the focus since the combination of high mobility and high saturation velocity makes graphene an intriguing candidate for RF electronics, despite inherent shortcomings due to the gapless band structure. In addition, the flexibility of graphene enables high-performance flexible RF electronics. Furthermore, we will introduce hot electron transistors with a with graphene base electrodes (graphene base transistors, GBTs), potentially enabling operation at >1 THz [5].

CNTs as a prominent example of one-dimensional materials also provide very high charge carrier mobility and very high saturation velocity depending on the diameter of the tube. Compared to graphene, an advantage of CNTs is that they exist also in semiconducting form depending on the chirality, so that they can be utilized for digital circuits with higher intrinsic performance than that of the state-of-the-art silicon technology [6]. In this part, we will first explain the electronic structure of CNTs. Due to the advantage of CNTs with a proper bandgap, our focus will be on digital circuits. We will discuss the way toward realizing CNT-based CMOS technology, i.e., controllable p- and n-type transistors. In the end, we will give an outlook on CNT-based microprocessors.

Both graphene and CNTs can be grown by chemical vapor deposition processes, typically on catalytic substrates like copper, nickel, or iron. The materials can then be transferred onto the desired rigid or flexible substrates or grown directly on the target substrate via templated growth. The details of these growth methods are beyond the scope of this chapter, and we therefore refer to the literature in the field [7–9]. In addition, there are hundreds of related two-dimensional materials under investigation, including semiconductors like MoS_2 (molybdenum disulfide) or WSe_2 (tungsten diselenide). These materials are also suitable for transistors, including logic gates, but a detailed discussion is beyond the scope of this chapter.

25.2 Graphene-Based Transistors

Since graphene is straightforward in terms of atomic structure, we will start to discuss it first, although the experimental investigation of graphene-based transistors started much later than CNT-based ones.

25.2.1 Band Structure of Graphene

Graphene has a two-dimensional (2D) hexagonal crystal structure as shown in Fig. 25.1. The unit cell consists of two carbon atoms, marked with A and B. The 2D crystal structure is constructed based on this unit cell according to a triangle lattice. The primitive vectors of the lattice can be written as

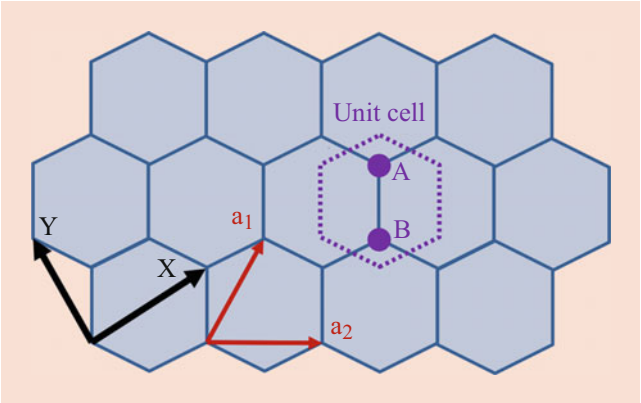


Fig. 25.1 Atomic structure of graphene. A unit cell consists of two atoms marked with A and B. The primitive vectors are defined as a_1 and a_2

$$a_1 = \frac{a}{2}\left(3, \sqrt{3}\right), a_2 = \frac{a}{2}\left(3, -\sqrt{3}\right) \tag{25.1}$$

where $a \cong 1.42$ Å is the distance between two directly neighbored carbon atoms, i.e., the distance between atoms A and B.

If we only consider the hopping between the directly neighbored atoms with tight-binding approximation (TBA), we can derive the energy dispersion of graphene [10]:

$$E_{\pm}(\mathbf{k}) = \pm t\sqrt{3 + 2\cos\left(\sqrt{3}k_y a\right) + 4\cos\left(\frac{3}{2}k_x a\right)\cos\left(\frac{\sqrt{3}}{2}k_y a\right)} \tag{25.2}$$

where $k \equiv (k_x, k_y)$ is the wave vector and $t \cong 2.8$ eV is the hopping energy between the directly neighbored carbon atoms. The signs plus and minus correspond to the conduction band and the valence band, respectively. If we plot the energy band in 3D space, it becomes apparent that the conduction band and the valence band intersect at specific points, which are called K and K' points. Their coordinates in the momentum space are

$$K = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a}\right), \quad K' = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a}\right). \tag{25.3}$$

Due to the presence of K (or K') points, the bandgap of graphene is 0, so graphene is considered as a semimetal. If we focus the band structure around K (or K') points, Eq. 25.2 can be expanded as [10]

$$E_{\pm}(\mathbf{q}) = \pm v_F |\mathbf{q}| + O\left[\left(\frac{q}{K}\right)^2\right] \tag{25.4}$$

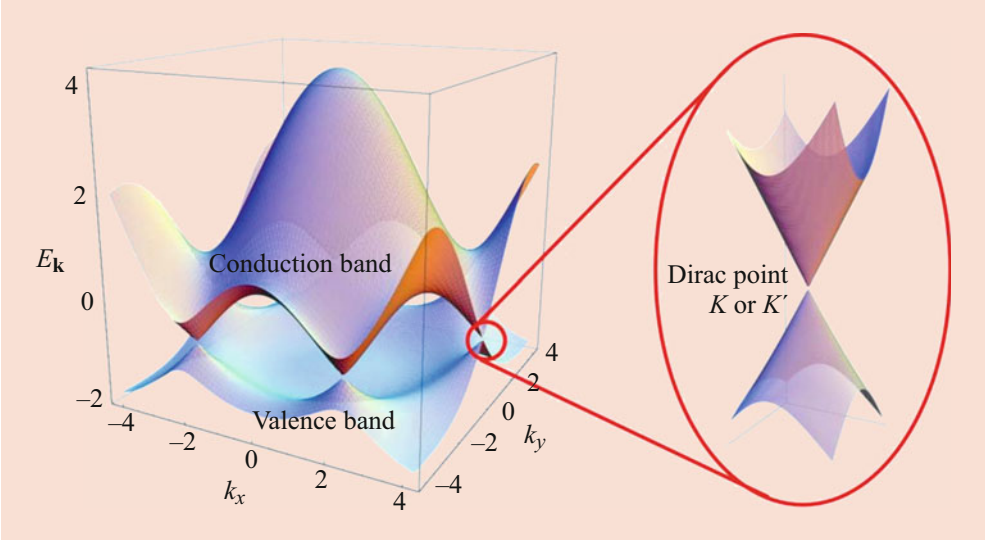


Fig. 25.2 The 2D band structure of graphene, with the Dirac cone zoomed in the band structure to K or K' points. (Reprinted figure with permission from Ref. [11]. Copyright (2009) by the American Physical Society)

where the wave vector $\mathbf{q} \equiv \mathbf{k} - \mathbf{K}$ and $v_F \cong 1 \times 10^8$ cm/s is the Fermi velocity around the K (or K') point. In the first-order approximation, the dispersion is linear around the K (or K') point, so that the effective mass of the charge carrier is 0, similar to that of photons (Fig. 25.2). The behavior of charge carriers around the K (or K') point can thus be described by the Dirac equation rather than the Schrödinger equation, and the K (or K') points are consequently also called Dirac points. The Dirac points define some of the special properties of graphene which are very interesting for fundamental research as well as engineering.

25.2.2 Basic Device Geometry and Characterization

A graphene-based field-effect transistor (GFET) consists of a layer of graphene that forms the channel, a gate dielectric, metallic contacts to the graphene, and a gate electrode [12]. The gate electrode can be used to electrostatically shift the Fermi level in graphene, as illustrated in Fig. 25.3. When the Fermi level lies at the Dirac point, the conduction band is empty, and the valence band is fully occupied. Ideally the carrier density in this situation is zero at zero temperature. However, due to thermal electron-hole pair generation as well as a finite number of negative or positive charges induced by impurities in the graphene and the surrounding dielectric layers, there are a finite number of charge carriers. The carrier concentration therefore shows a minimum value defined by the random distribution of electrons and holes across the graphene channel. The Dirac point is thus also called charge

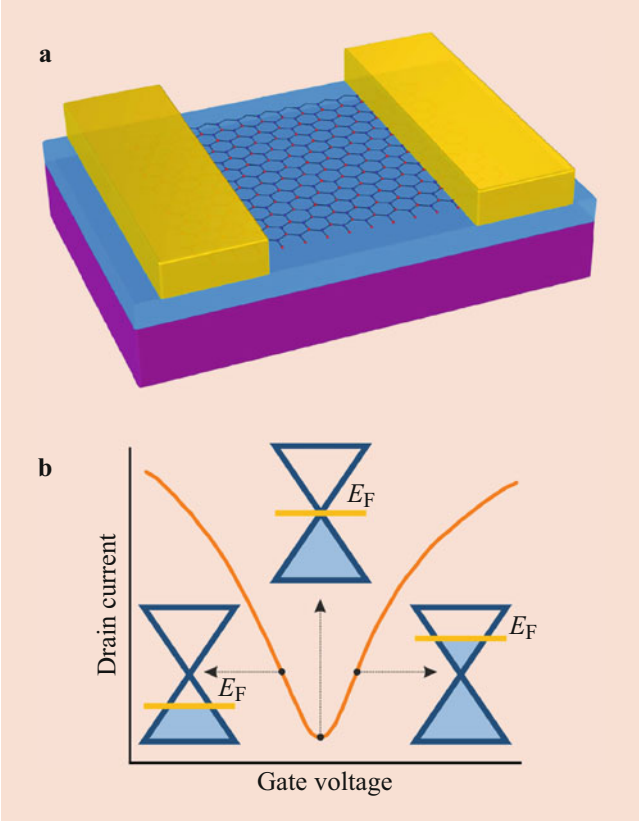


Fig. 25.3 (**a**) Basic geometry for graphene-based transistor. Graphene is contacted by metal from both ends with substrate as the gate electrode. (**b**) The field-effect ambipolar conduction due to the shift of the Fermi level. If a negative gate voltage is applied, the channel is dominated by hole conductions. While if a positive gate voltage is applied, the channel is dominated by electron conduction

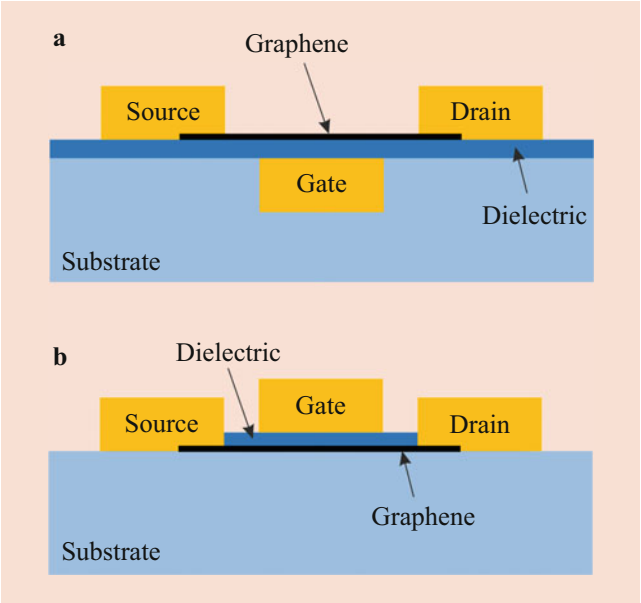


Fig. 25.4 Schematic of (**a**) top-gate and (**b**) back-gate configuration for a GFET

neutrality point [13]. When the gate voltage is changed, the Fermi level shifts upward or downward, and the electron or hole concentration starts to increase, respectively. As a consequence, GFETs typically show ambipolar conduction behavior, with minimum conduction at the Dirac point.

GFETs can be fabricated similar to thin-film transistors in either a back-gate configuration or in a top-gate configuration as shown in Fig. 25.4. The back-gate configuration has the advantage of fewer process steps after the graphene is introduced and hence is preferred in terms of process control and yield. The top-gate configuration can deliver higher performance, in particular for RF electronics, since the parasitic capacitances between gate and source/drain are minimized and the gate resistance can be minimized by T- or Gamma-shaped gate electrodes. However, the deposition of high-quality and thin dielectrics on top of graphene is still challenging.

Typical ambipolar transfer characteristics of a GFET are shown in Fig. 25.5. In principle, GFETs behave like conventional MOSFET, but because of the gapless band structure of graphene, they cannot be turned off completely. The typical current modulation in GFETs by the gate voltage results in an on-state to off-state current ratio in the range of 3–15, depending on the graphene quality and parasitic effects from electrostatic doping. It is important to note that the term "doping" is often used to describe the effect of charges near the graphene on the carrier density in graphene, which is different from the classic meaning of the term doping to describe replacing lattice atoms in bulk semiconductors. The lack of a distinct off-state makes it clear that classical CMOS logic operation cannot be addressed by GFETs, but only

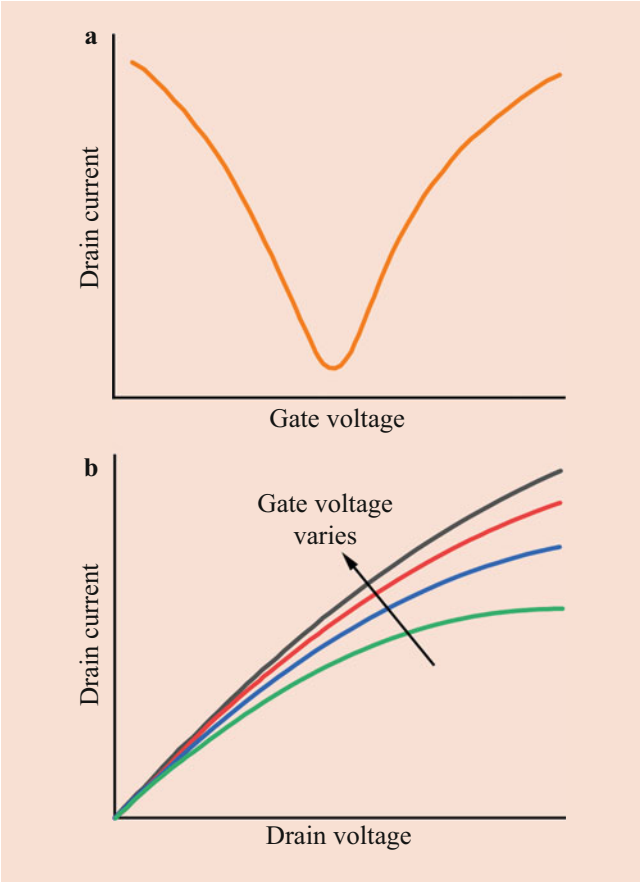


Fig. 25.5 Typical transfer (**a**) and output (**b**) curves of a GFET

analog operations are feasible, where transistors are operated in the on-state (amplifiers, mixers, oscillators, etc.). In an ideal GFET, the Dirac point should be located at zero gate voltage, but it is typically shifted due to unintentional doping of the graphene. From the slope of the transfer curve, we can derive the transconductance of the device

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{gs}}} \tag{25.5}$$

where I_{ds} is the source-drain current and V_{gs} is the gate voltage. g_{m} can be used to calculate the field-effect mobility of graphene, which is similar to the calculation for a thin-film transistor in the linear regime:

$$\mu = \frac{1}{V_{\mathrm{ds}}} \frac{1}{C_{\mathrm{g}}} \frac{L}{W} g_{\mathrm{m}} \tag{25.6}$$

where V_{ds} is the source-drain voltage bias, C_{g} is the gate capacitance per unit area, and L and W are the length and width of the channel, respectively. However, large contact resistances between graphene and metal contacts, which may further be dependent on the (back-)gate voltage, can lead to an underestimation of the mobility when extracting the mobility with this method [15–16].

The absence of a bandgap in graphene means that it is impossible to achieve proper current saturation due to a pinch-off in the output characteristics of GFETs. This is because the channel undergoes a direct transition from an n-type to a p-type variable conductor [17] and thus there cannot be a pinch-off of the channel as in long-channel semiconductor MOSFETs. Nevertheless, current saturation can be obtained through velocity saturation in a certain drain voltage window, if high-quality material is used [18]. If the drain voltage is increased further, the GFETs continue to conduct more current. Figure 25.5 shows the typical output characteristic of a GFET with standard graphene quality, which can be fabricated by CVD graphene on the wafer scale.

25.2.3 Contact Resistance

The electrical contact between metal and graphene, R_C, is determined by the limited density of states in graphene. As in any electronic device, the contact resistance should be significantly smaller than the device resistance in order to obtain high-performance GFETs. In contrast to area contacts in three-dimensional semiconductors, the contact to graphene is typically a line contact and therefore should be normalized by the channel width (R_C W), with unit Ω·μm. To characterize the contact resistance, the transfer length method (TLM) is typically used. TLM requires a set of devices with different channel length. The resistance of the device normalized by its width is then plotted against the channel length, which usually results in a linear relationship. After linear fitting of the data points, the intercept of the line with the y-axis corresponds to twice the contact resistance of the device ($2R_C$), while the slope of the fit corresponds to the sheet resistance R_{sh}. There are several pitfalls with TLM for graphene devices, since the contact resistance is gate voltage-dependent, i.e., the carrier density in graphene has an influence on both R_C and R_{sh} [19, 20]. The TLM layout and procedure are illustrated in Fig. 25.6.

There are two different configurations for graphene-metal contacts, surface contacts, and edge contacts (Fig. 25.7). The former can be subcategorized into top contacts, bottom contacts, or sandwich contacts. In this case, there is an overlapping area between the metal and the graphene surface. The carrier injection from the metal to graphene mainly occurs by tunneling between the metal and the graphene within the transfer length since there are no dangling bonds on graphene (for the ideal case of defect-free graphene). The efficiency of this process is rather low, i.e., the contact resistivity typically remains high. In contrast, edge contacts allow charge carriers to be injected into graphene via the dangling bonds at the one-dimensional edge of graphene, which form a covalent bond with the metal. Therefore, edge contacts result in lower contact resistivity, with reported values approaching 100 Ω·μm

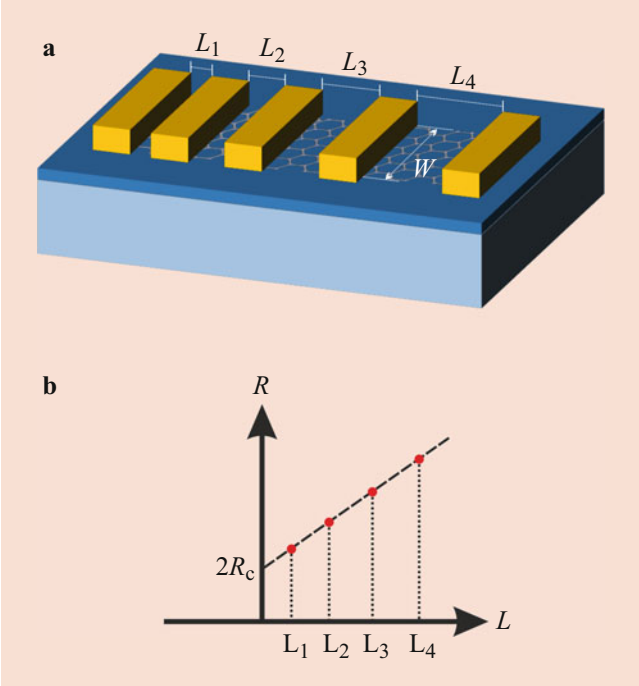


Fig. 25.6 TLM in order to extract the contact resistance of metal-graphene contact. (**a**) A set of devices need to be fabricated with the same channel width W and different channel length L_1 to L_4. (**b**) The total resistance is plotted against channel length, with a linear fitting. The channel resistance is proportional to the channel length. The slope of the line is related to the sheet resistance of graphene, and the intercept of the line with y-axis is the contact resistance from both sides ($2R_c$)

[3]. The combination of the two methods can be exploited by etching holes into graphene under the contact areas. Here, reported values are below 100 Ω·μm [21–23]. While good ohmic contacts are obviously feasible, the experimental results on contact resistance are still scattered, since the contact resistance is affected by many factors. These include metal-type, deposition method, graphene-type, contact-type, interfacial contamination, and characterization method [15, 24]. In addition, the specification for the required contact resistivity depends clearly on the device application. Hence, there is no solid conclusion today to indicate which method provides suitable and reliable results.

25.2.4 Radio Frequency Transistors

The main figures of merit for RF transistors are the cutoff frequency f_T and the maximum oscillation frequency f_{MAX}. f_T is defined as the frequency, where the current gain of a transistor reaches unity. f_{MAX} is defined as the frequency, where the power gain of a transistor reaches unity. These two quantities describe how fast a transistor can operate. It shall be noted that for most applications, f_{MAX} is more relevant, while f_T describes the intrinsic properties of the channel. For these

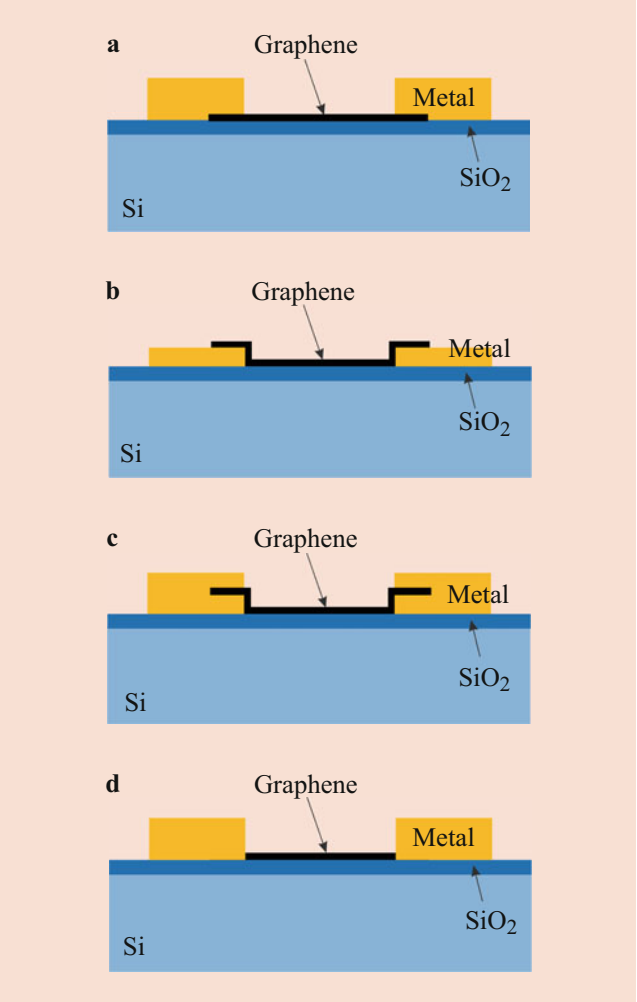


Fig. 25.7 Different contact mode between graphene and metal electrodes. (**a**) Top contact, (**b**) bottom contact, and (**c**) sandwich contact are known as surface contact. In contrast, (**d**) edge contact usually results in lower contact resistance

parameters, there are usually intrinsic and extrinsic values. Intrinsic values reflect the performance of the device itself without the parasitic effect, from, for example, substrates or testing pads. The procedure of data processing to obtain the intrinsic property is called de-embedding. In contrast, extrinsic values are those directly from the measurement without de-embedding. The intrinsic properties are only affected by the device itself, so it can be used to benchmark between devices with different substrates or layout designs. However, we have to note that the extrinsic properties are also important since it sets a performance limit that a device can deliver in such a specific process or design environment.

Based on the small-signal model of a GFET shown in Fig. 25.8, Eq. 25.7 describes the extrinsic f_T by considering the RC time constant and the time response of the charge carriers [25]:

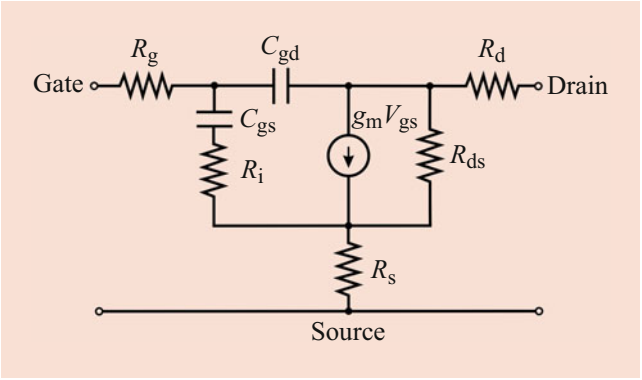


Fig. 25.8 Small-signal equivalent circuit of a GFET

$$f_T = \frac{g_m}{2\pi} \frac{1}{(R_s + R_d)\, g_m C_{gd} + \left(C_{gs} + C_{gd}\right)\left[1 + g_{ds}\left(R_s + R_d\right)\right]} \tag{25.7}$$

where R_s and R_d are the source and drain access resistance, C_{gd} and C_{gs} are the gate-drain and gate-source capacitances, and $g_{ds} = \partial I_{ds}/\partial V_{ds}$ is the differential conductance.

One critical parameter to enhance f_T of a GFET is to reduce C_{gd} or increase g_m. Scaling down the channel length of the device is a good way to reduce C_{gd} and increase g_m. In addition, reducing R_s or R_d will also have a positive impact on f_T, as in any given technology. If the device can reach the saturation regime in the output characteristics, g_{ds} will be minimized (an ideal saturation results in $g_{ds} = 0$), and therefore f_T will be increased.

If we consider the intrinsic property of the GFET, i.e., neglect the parasitic effect from R_s and R_d, we arrive at the simplified equation:

$$f_{T-int} = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)}. \tag{25.8}$$

The extrinsic f_{MAX} can generally be written as Eq. [25]

$$f_{MAX} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_{ds}\left(R_i + R_s + R_g\right) + g_m R_g C_{gd}/C_{gs}}}, \tag{25.9}$$

and the intrinsic one can be written as

$$f_{MAX-int} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_{ds} R_i}}. \tag{25.10}$$

where R_i is the resistance shown in Fig. 25.8. Early RF data of GFETs were published in 2008/2009 by Meric et al. and Moon et al., who observed f_T of 14.7 GHz and f_{MAX}/f_T of 14/4 GHz, respectively [26, 27]. Since then, there has been significant progress in terms of RF performance by reducing

the physical gate length, improving the graphene quality and reducing parasitic resistances like contact and gate resistance, with f_T values reaching several hundred GHz. This is on par with InP transistors and state-of-the-art Si transistors in terms of f_T at least for a given gate length. Since 2012, there has been no further improvement in terms of f_T in literature, which is probably due to a shift of the research focus on other properties of GFETs. In the same timeframe, f_{MAX}, which is important for applications in low-noise amplifiers (LNAs) and oscillators, has been reported up to 44 GHz [28]. Thus, while f_T increased by a factor of 100, f_{MAX} increased only by a factor of 3. This difference can be explained by parasitic effects that mainly limit f_{MAX}, but not f_T: the high resistance of the metallic gate electrodes and the high (non-saturating) output conductance g_{ds}. To increase f_{MAX}, a T-gate structure has been employed that reduces the gate resistance [29], and also the graphene quality has been improved so that in 2016 the benchmark for f_{MAX} was finally increased to 200 GHz [30], which is a value close to Si transistors at the corresponding gate length.

Numerous theoretical calculations of f_{MAX} and f_T for GFETs have been performed in order to predict the ultimate performance limits of GFET. Several publications report values for both parameters significantly above 1 THz (sometimes even up to 10 THz), which would outperform all existing transistors based on Si and III/V materials by far. However, in those simulations, one has to carefully weigh the input parameters, especially for the contact resistance and for the graphene mobility. Using still realistic, but very good values as input parameters, several simulation studies arrive at a range of 1–3 THz for both f_{MAX} and f_T [31, 32].

The noise Figure (NF) is also an important quantity for assessing the performance of an RF transistor. In this respect, only little work has been performed, mainly because the transistors often did not show gain in a 50 Ω environment typically used in RF application scenarios. In addition, most of the GFETs have relatively low extrinsic f_T due to parasitic capacitances, which also has a significant negative impact on the measured noise value. Early work reported a noise figure of 3.3 dB at 1 GHz, which is a very high value compared to Si and InP, where NF < 1 dB [33]. In 2017, a noise figure of 1.5 dB at 10 GHz was reported [34], which is close to Si CMOS transistors at these frequencies. In these GFETs, the intrinsic noise figure was estimated to be 0.8 dB at 10 GHz, which would be a competitive value.

In order to identify the main bottlenecks for GFETs, the key parameters of the best GFET in terms of f_{MAX} are compared with the best InP transistor in Table 25.1. Both transistors implement a low-resistance T-gate structure. The gate length for the InP transistor is shorter by a factor of 1.7, which translates into lower gate capacitance and faster operation. In terms of contact resistance, both transistors are similar, and hence the contact resistance is not a limiting factor for the GFET performance. A clear difference between the GFET and the InP transistor can be found for the carrier mobility and the ratio between f_{MAX} and f_T. The lower mobility for the GFET translates directly into lower transconductance, which affects both f_{MAX} and f_T. Thus, improving the material quality for GFETs will directly pay back into a significantly improved RF performance. The main limitation for the mobility in graphene is the process integration flow, with each step impacting mobility. The issues with process integration have generally been identified, and improvements can be expected as the technology matures [2, 36]. The rather low ratio between f_{MAX} and f_T of the GFET is related to poor saturation of the output conductance. Therefore, an urgent issue in order to improve the RF performance of GFETs is to engineer output current saturation, which can be achieved for high-quality graphene through velocity saturation.

Table 25.1 Comparison of key parameters of the best GFET with the best InP transistor

	InP [35]	Graphene [30]
f_T (GHz)	385	255
f_{MAX} (GHz)	1200	200
Gate length (nm)	35	60
Contact resistance (Ωμm)	50	50–100
Transconductance (S/mm)	2.3	1.1
Mobility (cm^2/vs)	15,000	3500

Hence, it can be expected that the RF performance of GFETs will be significantly improved if high-quality graphene with mobility values approaching the highest reported values (>> 10,000 cm^2/Vs) is maintained throughout the device fabrication process. This requires work especially on identifying suitable substrates and encapsulation materials like 2D hexagonal boron nitride, but on large scale, and in addition to an optimized graphene transfer process.

25.2.5 Flexible Transistors for High-Frequency Applications

Flexible electronics is a field of great promise. It is expected to provide human beings with smaller, lighter, and more comfortable electronic devices, particularly with potential applications in wearable consumer electronics, electronics for healthcare, flexible displays, flexible solar cells, tissue-like electronic devices, e-skin, etc. The thickness of the flexible substrate (typically <50 μm) is only about one-fifteenth of the thickness of 300 mm silicon wafers, which may have been beneficial for specific applications.

Graphene does not only have excellent electrical properties as discussed in the previous sections, but it also provides ultrahigh mechanical strength due to the strongest bond in nature, carbon-carbon σ covalent bonding. Free-standing single-layer graphene has a very high breaking strength of

Table 25.2 Parameter comparison for graphene-based transistors fabricated on flexible substrate

References	Gate dielectric	Hole mobility (cm^2/Vs)	Electron mobility (cm^2/Vs)	Bending radius (mm)	Max. strain (%)	Operating voltage (V)
[42]	PMMA	10,000	4000	–	–	−80 to 80
[42]	Ion gel	203	91	6	–	−4 to 2
[44]	Ion gel	1188	422	–	5	−2 to 2
[45]	Ion gel	892	628	3.1	3	−2 to 2
[46]	ALD Al_2O_3	4930	1130	–	–	0 to 6
[47]	ALD Al_2O_3	1400	–	1.3	8.7	−2.5 to 3
[48]	Natural Al_2O_3	280	190	8	0.62	−3 to 2.5
[49]	ALD Al_2O_3	3342	2813	5.5	2.7	−5 to 5
[50]	Graphene oxide	150	116	4.1	3.5	−3 to 4
[51]	YO_x	102	100	12.5	–	−4 to 3
[52]	$Al_2O_3/HfO_x/Al_2O_3$	67	67	5	–	−7 to 7
[53]	$Al_2O_3 + HfO_2$	1830	–	1	–	0 to 1
[54]	ALD HfO_2	1500	–	–	1.5	−2 to 2
[55]	hBN	2324	2307	–	–	−3 to 3
[56]	ALD Al_2O_3	2800	3900	0.7	–	−1.5 to 1.5
[57]	Natural Al_2O_3	3000	–	–	2.5	−2 to 2
[58]	ALD Al_2O_3	9214	13,000	7.9	–	−8 to 8
[59]	AlO_x + SAM	2575	3075	5	1.25	−2 to 2
[60]	PMMA	630	370	8	1.2	−60 to 60
[39]	YO_x	24,000	20,000	7.8	0.8	−0.5 to 1
[61]	hBN	10,000	–	–	1	−0.25 to −1.75
[62]	ALD HfO_2	1000	–	–	2	−2 to 2
[63]	Natural Al_2O_3	3250	–	–	–	−1 to 1
[64]	Natural Al_2O_3	2500	–	12	0.51	−2 to 1
[65]	Nanoscale PI	1100	4540	–	–	−8 to 8

Adapted from [41]

about 42 N/m, which translates to a Young's modulus of about 1 TPa and an intrinsic strength of about 130 GPa [37], which is about 200 times higher than that of steel. Graphene can withstand extreme bending conditions [38]. The outstanding mechanical properties of graphene in combination with its electrical properties (especially high carrier mobility and high saturation carrier velocity) enable its applications in flexible high-frequency electronics.

Charge carrier mobility is a crucial parameter for transistors, especially those targeted for high-frequency applications. Although the theoretical limit or mobility in graphene is extremely high, different material synthesis methods, handling, and other fabrication procedures result in graphene with different qualities, i.e., different mobility values. Table 25.2 summarizes reported graphene transistors fabricated on flexible substrates. Different gate dielectrics were utilized for flexible transistors, such as thin-film technology-based oxides (naturally oxidized Al_2O_3, ALD Al_2O_3, ALD HfO_2, thermally oxidized YO_x, etc.), flexible materials (ion gel, nanoscale PI, etc.), or other 2D materials (graphene oxide, hBN). Bending and straining experiments with up to 8.7% surface strain have shown suitability for many application scenarios. The highest mobility for graphene-based transistors on flexible substrates is higher than 20,000 cm^2/Vs, which was achieved by using thermally oxidized yttrium oxide as the gate dielectric [39]. This value is comparable to data on rigid substrate. Based on this approach, excellent high-frequency performance can be expected. In addition, it has been reported that high-quality graphene is more resistant to repeated bending, because defects in graphene usually weaken the mechanical property of graphene significantly [40].

The frequency response of graphene-based flexible transistors has been investigated through S-parameter characterization, from which the f_T and f_{MAX} can be determined. Table 25.3 summarizes literature that reports f_T and f_{MAX}. The graphene in those experiments is from chemical vapor deposition unless noted otherwise. The table clearly shows that the gate length is very critical for the performance enhancement, as is typical for conventional RF transistors. The record extrinsic f_T is 39 GHz for 100-nm gate length [64], and the record extrinsic f_{MAX} is 20 GHz for 200-nm gate length [57]. Strain up to 2.5% has been applied without significant degradation of RF performance [57].

Table 25.3 Parameter comparison for graphene-based flexible RF transistors

References	L_g (μm)	f_T ext./int (GHz)	f_{MAX} ext./int (GHz)	Bending radius or strain	Notes
[51]	0.17	2.2/8.7	0.55/–	12.5 mm	Solution-based graphene
[56]	0.5	–/25	–/2.1	0.7 mm	
[53]	0.4	3/10	–/–	1 mm	
[54]	0.5	7.2/–	2.6/–	1.5%	
[57]	0.2	32/64	20/34	2.5%	
[61]	0.375	12/29.7	10.6/15.7	1%	Exfoliated graphene
[62]	0.26	23.6/38.7	6.5/7.6	2%	f_T/f_{MAX} = 198/28.2 GHz after full de-embedding
[63]	0.1	10/11	8/–	–	
[64]	0.1	39/–	13.5/–	0.51%	
[65]	0.14	–/95	–/30	–	

Table 25.4 Benchmarking for high-performance graphene-based flexible RF transistors

References	L_g (um)	f_T ext. (GHz)	f_{MAX} ext. (GHz)	$f_T \cdot L$ ext. (GHz·μm)	f_T/f_{MAX} ext	Strain
[54]	0.5	7.2	2.6	3.6	2.7	1.5%
[57]	0.2	32	20	6.4	1.6	2.5%
[61]	0.375	12	10.6	4.5	1.1	1%
[62]	0.26	23.6	6.5	6.1	3.6	2%
[64]	0.1	39	13.5	3.9	2.8	0.51%

Gate length normalized frequency parameters, such as $f_T \cdot L_g$, can also be used as a figure of merit for benchmarking when there is only a small range of experimental data available. Moreover, there is often a lack of structural information to fully compare the de-embedding procedures, so it is often not fair to compare the values after de-embedding. For example, in reference [62], where values of 198 GHz and 28.2 GHz were reported for f_T and f_{MAX}, respectively, a full de-embedding process was used, in which the source and drain electrodes were also in the open structure. Hence, these reported values should not be compared with values from other reports, where no de-embedding procedure or a de-embedding procedure with less parasitic parameters was applied. Therefore, we use extrinsic parameters in Table 25.4 to benchmark different flexible RF transistors. The state of the art for $f_T \cdot L_g$ is 6.4 GHz·μm (extrinsic) for the device geometry as well as the frequency response characterization as shown in Fig. 25.9. The ratio between f_T and f_{MAX} approaches unity in the transistor from [61], equivalent to the best value achieved on rigid substrate [66].

There is also intensive research for different analog applications such as low-noise amplifiers (LNAs) [57], frequency doublers [39, 55], frequency mixers [57], and radio receiver [67]. LNAs operating at 5.5 GHz and featuring a noise figure of only 1.34 dB with an associated gain of 11.95 dB have been reported [57]. Ambipolar frequency doublers operate at the 10 MHz range, but there is no gain higher than unity [39, 55]. A two-tone test of a graphene mixer shows high-frequency performance which extends well into the gigahertz range [57]. In addition, a flexible graphene-based amplitude modulated radio receiver operating at 2.4 GHz has been demonstrated recently [67]. The receiver consists of a graphene transistor demodulator, graphene speaker, and graphite antenna. Albeit the interesting performance, the integration level of these circuits and systems is not yet very high. Only one transistor is typically used on chip, while all passive components are not monolithically integrated with the active device.

At higher integration level, i.e., two or more transistors, a flexible all-graphene modulator circuit with the capability of encoding a carrier signal with quaternary digital information has been reported [49]. Two types of quaternary modulation were demonstrated: quaternary amplitude-shift keying (QASK) and quadrature phase-shift keying (QPSK), with 1 and 2 all-graphene transistors, respectively. Its all-graphene design with every component (channel, interconnect, load resistor, and source/drain/gate electrodes) fabricated from graphene makes it not only flexible but also highly transparent.

The basic requirement of flexible electronic is the bendability, stretchability, or even foldability of the substrate in combination with all (di-)electric layers on top of that. The mechanical and electrical properties of these layers must be stable during the course of bending. The retention capability of all device and circuit parameters should be high over a relatively long timeframe. Figure 25.10a summarizes the carrier mobility of different materials that are compatible with thin-film flexible technology. Organic semiconductor materials such as pentacene have rather poor mobility, with the highest demonstrated values typically approximately

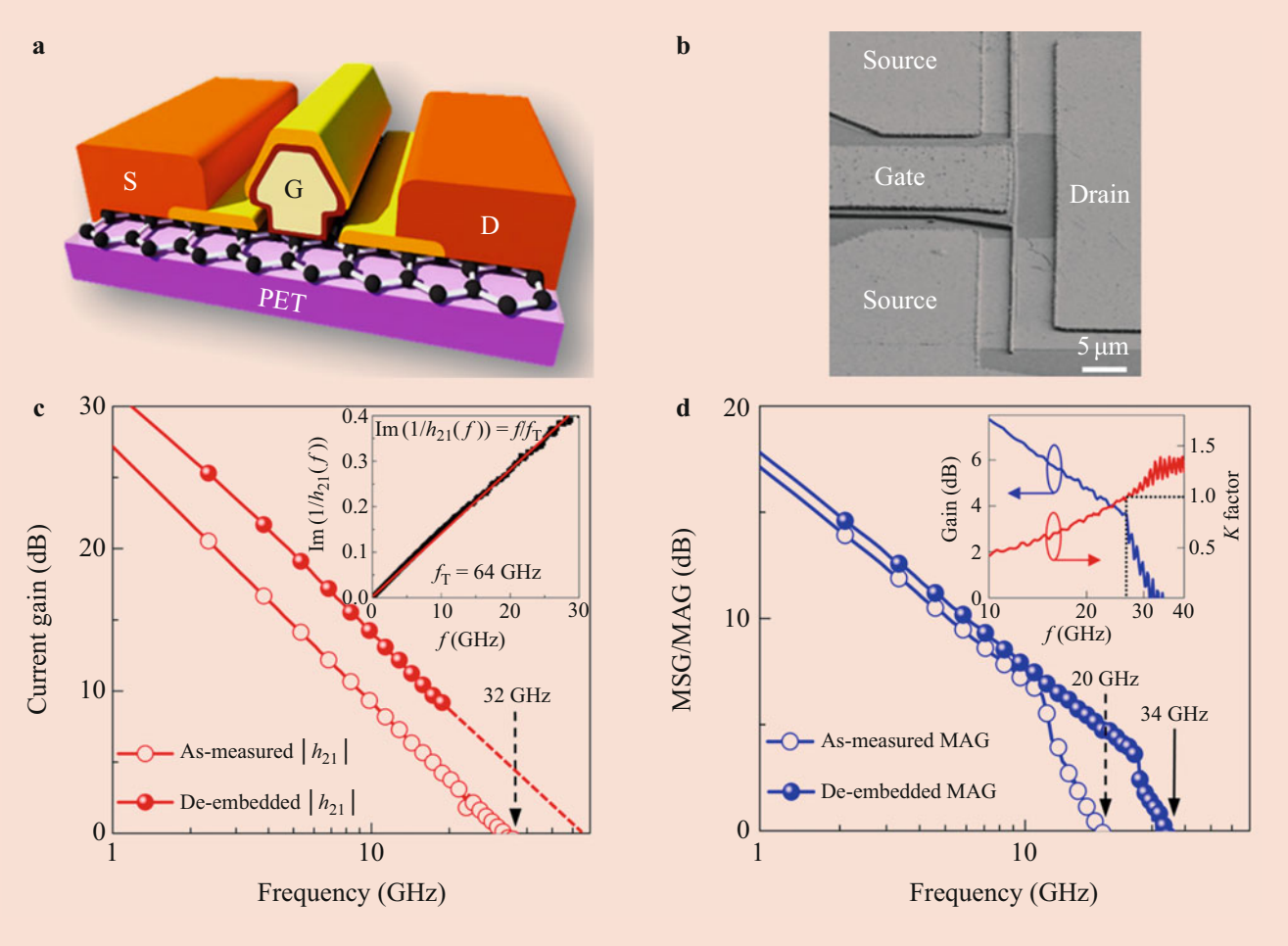


Fig. 25.9 Graphene-based flexible RF transistor. (**a**) Transistor schematic with T-gate. (**b**) The scanning electron microscopy image of the fabricated device. (**c**) The intrinsic and extrinsic current gain to determine the cutoff frequency. (**d**) The intrinsic and extrinsic power gain to determine the maximum oscillation frequency. (Adapted with permission from Ref. [57]. Copyright (2014) American Chemical Society)

10 cm^2/Vs, which largely limits the high-frequency response of the transistors [68]. Metal-based oxide semiconductors and polysilicon are very compatible with thin-film large-scale processing, but the performance is not high enough for most RF applications (mobility <100 cm^2/Vs). Nevertheless, these materials may find suitable applications in low-cost electronics. Other low-dimensional materials such as carbon nanotubes (CNT) or two-dimensional transition metal dichalcogenides (TMD) such as molybdenum disulfide may also be suitable for flexible electronics in terms of flexibility. Conventional semiconductor thin films such as silicon or III–V compound semiconductors can be applied for flexible electronics, but the flexibility of such materials is rather limited, even when thinned down considerably [69, 70]. Figure 25.10b compares different potential materials for flexible electronic in terms of f_{MAX} and maximum strain. Among all the candidates, graphene is the only material that delivers power gain in the gigahertz regime at an applied strain of more than 1%. Thus, graphene devices currently provide the best performance among the materials listed in Fig. 25.10, concerning both frequency response and strain limit capability [57].

A qualitative overview and evaluation of the different materials under consideration are shown in Table 25.5. Although the scalability and manufacturability of graphene still require further development, the outstanding performance of prototype graphene RF devices strongly underlines its potential for flexible RF electronics.

Graphene-based flexible RF electronics could find first industrial applications on flexible Wi-Fi transceivers for consumer electronic devices. This kind of technology can be used for wearable devices or smartphones in order to save the interior space. Applications in the frequency range of Wi-Fi signals (several GHz) are already attainable with graphene in terms of frequency response, with the added advantage of mechanical flexibility. Graphene-based flexible MMICs are

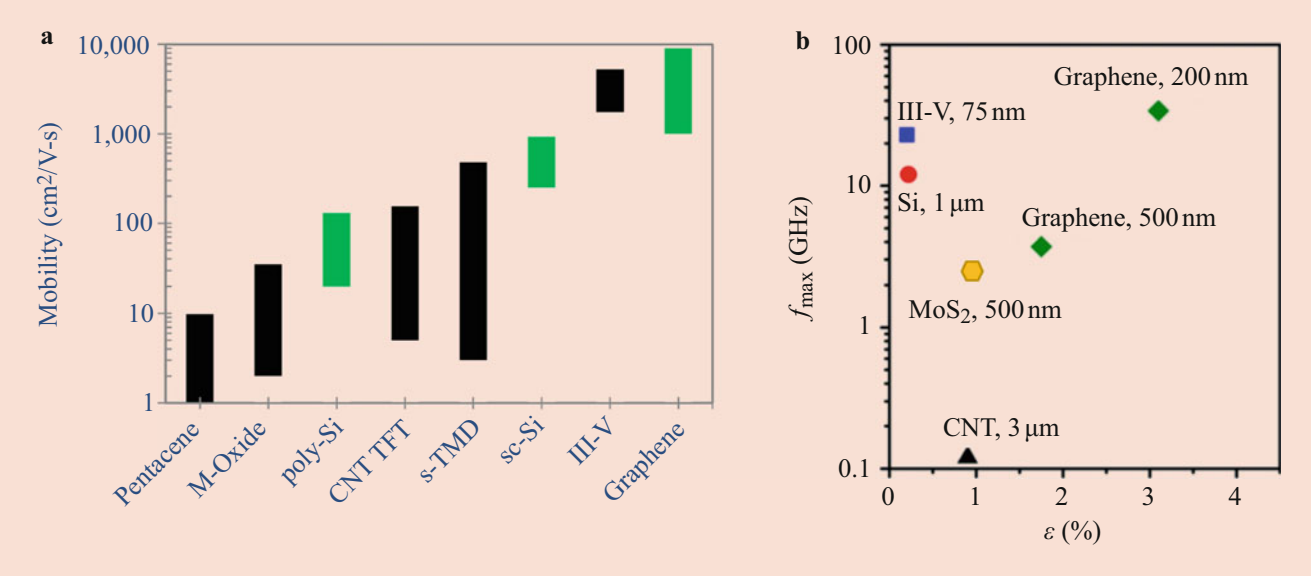


Fig. 25.10 (**a**) Mobility for different materials suitable for flexible electronics. ©2015 IEEE. (Reprinted, with permission, from [67]). (**b**) Comparison of f_{MAX} and the limit of applied strain for different materials suitable for flexible electronics, adapted from reference [54]. III–V [70], Si [69], graphene [54, 57], MoS2 [71], CNT [72]. (Adapted with permission from Ref. [54]. Copyright (2013) American Chemical Society)

Table 25.5 Comparison of thin-film technology for flexible RF electronics. Mark from best to worst noted with + +, +, O, −, − −

Material	Flexibility	Speed	Scalability
Graphene	+ +	+ +	+
Thin-film III–V	O	+ +	+ +
Thin-film Si	O	+ +	+ +
TMD such as MoS_2	+ +	+	O
CNT thin film	+ +	+	−
Poly-Si	+	O	+ +
Metal-based oxide semiconductor	+	−	+ +
Organic semiconductor	+ +	− −	O

certainly capable of providing the RF back-end circuitry. For flexible applications, the RF front end and signal processing circuits have not yet been demonstrated, but would be preferable over heterogeneously integrated solutions on rigid substrates. Applications with higher target frequency range or higher-power flexibility are not necessarily required, and graphene on rigid substrates can provide higher performance for this application space, where flexible RF electronics is not the best option.

25.2.6 Vertical Transistors/Hot Electron Transistors

Vertical hot electron transistor structures with graphene (or other 2D materials) as the material for the transistor base are investigated for their potential for high-frequency operation. These devices are similar to heterojunction bipolar transistors (HBTs) and sometimes also referred to as "graphene base transistor" (GBT) or graphene hot electron transistor. Here, we summarize the experimental and theoretical state of the art in graphene ballistic hot electron transistors, i.e., GBTs. Performance predictions indicate potential for (up to several) THz operation, even with current models that take nonidealities into account. Experimental results clearly demonstrate the basic DC functionality, with on/off current switching over several orders of magnitude and high transmission coefficient, but further developments are required to exploit the full potential of the GBT device family. In particular, interfaces between graphene and semiconductors or dielectrics are far from perfect and thus limit experimental device integrity, reliability, and performance and have prevented researchers from obtaining RF data.

Vertical electronic device concepts utilizing graphene have been proposed to overcome an intrinsic limitation of graphene, i.e., the absence of an electronic bandgap. One of these novel device concepts, introduced by Mehr et al. in 2012, is the vertical GBT [73]. The concept of the GBT is based on the metal base hot electron transistors (HETs) introduced originally by Mead in 1961 [74] and followed up by Heiblum and others in the 1980s with semiconductor heterostructures [75, 76]. HETs utilize high-energy tunneling injected electrons (hot electrons) as the main charge carrier. The first HETs were composed of metal emitters, metal bases, and metal collectors, which were isolated from each other by thin oxide barrier layers. One of the main challenges for the HETs as well as heterojunction bipolar transistors (HBTs) is that the cutoff frequency is limited by base transit

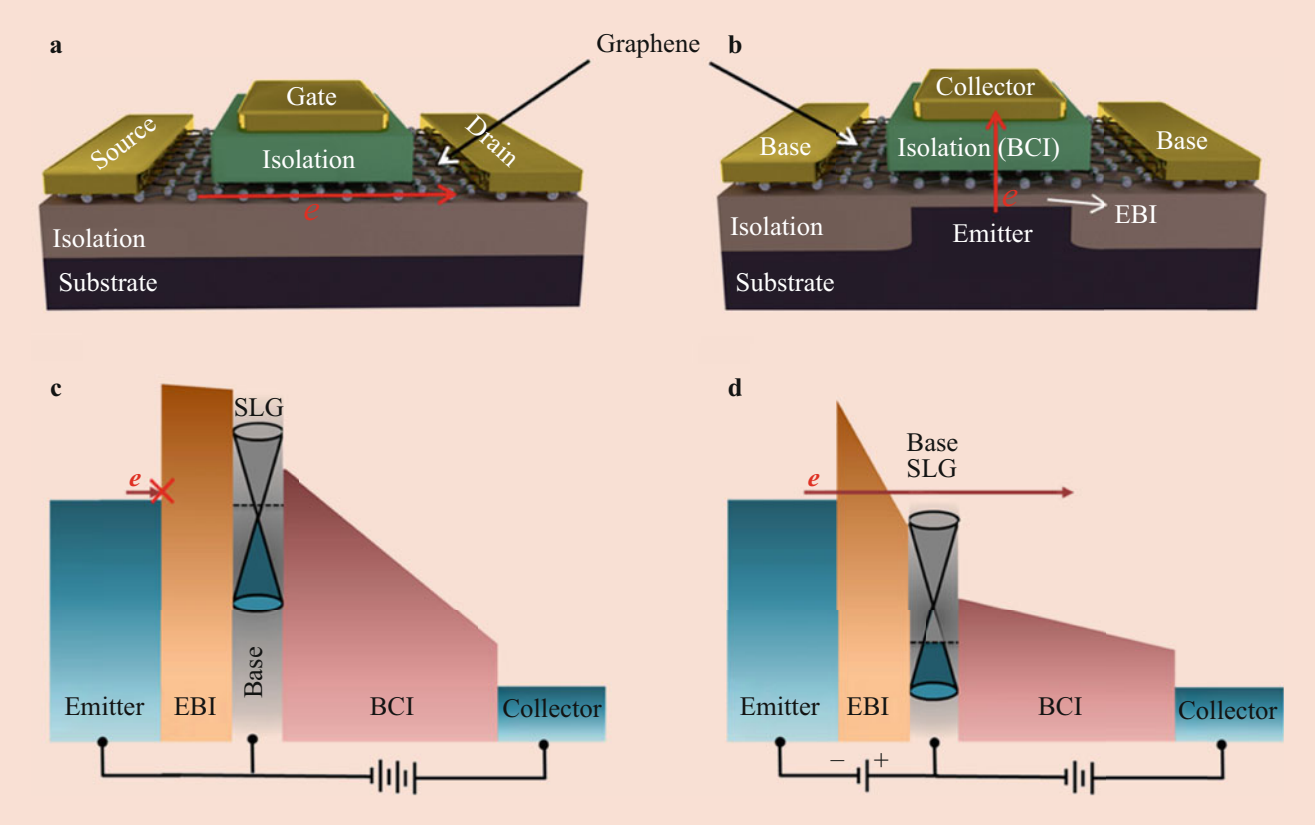


Fig. 25.11 Schematics of (**a**) GFET and (**b**) GBT. The red arrow shows the direction of electron transport in the on state of these devices. (c,d) Simplified band diagram of the GBT in the (**c**) off state and (**d**) on state in the common emitter configuration. We note that in (**c**) and (**d**), the energy difference between Fermi level and Dirac potential in graphene represents graphene's quantum capacitance effect. (Reprinted from [78], Copyright (2015), with permission from Elsevier)

time. While thinning down the base mitigates this issue, it dramatically increases the base resistance, resulting in high RC delay and self-bias crowding. The GBT addresses these issues by exploiting the high conductivity and the single atomic thinness of graphene as the base material, as it minimizes both the base transit time and the base resistance to enable high cutoff frequencies [73]. This concept is distinctly different from vertical graphene field-effect tunneling transistors as introduced by Britnell et al. [77]. While the latter functions due to the limited density of states in single-layer graphene and electrostatic gate control of the carrier transport between two isolated single-layer graphene (SLG) sheets, the GBT operates through emitter-base barrier modulation analogous to the bipolar technology (see Fig. 25.11).

In 2013, Vaziri et al. demonstrated the first experimental proof-of-concept GBT [79], where DC measurements confirmed the working principles of the devices. These first GBTs comprised of n-doped silicon emitters, 5-nm-thick thermal silicon dioxide (SiO_2) emitter-base insulator (EBI) tunneling barriers, a graphene base, 15–25-nm-thick atomic layer deposition (ALD) aluminum oxide (Al_2O_3) base-collector insulators (BCI), and metal (titanium/gold) collectors. The fabrication was done on 8-inch wafers, and the GBTs were isolated by 400-nm SiO_2 shallow trench isolation (STI) making the fabrication scheme potentially CMOS compatible. Figure 25.12a illustrates the transfer characteristics of a GBT at a base-collector voltage of $V_{BC} = 2$ V. The devices showed emitter-base threshold voltages of approximately 4.5 V, very low off-state currents and more than four orders of magnitude on/off ratio. Figure 25.12b shows temperature-dependent I–V characteristics of the emitter-base tunneling diode (input characteristics). Clearly, the dependence of the current to the temperature diminishes for high-voltage range. This fact together with the excellent linear fit of the I–V characteristics to the Fowler-Nordheim model (inset of Fig. 25.12b) confirms that the transport mechanism is dominated by tunneling. In addition, in Fig. 25.12b the onset of the emitter-base tunneling current is well matched to the onset voltage of the collector current in Fig. 25.12a. Nevertheless, the overall DC on current is not sufficient to use these poof-of-concept devices, e.g., as amplifiers.

High-frequency performance of the GBT requires high on-state collector currents I_C. In an ideal device, I_C is equal to the emitter current I_E, which consists of injected hot elec-

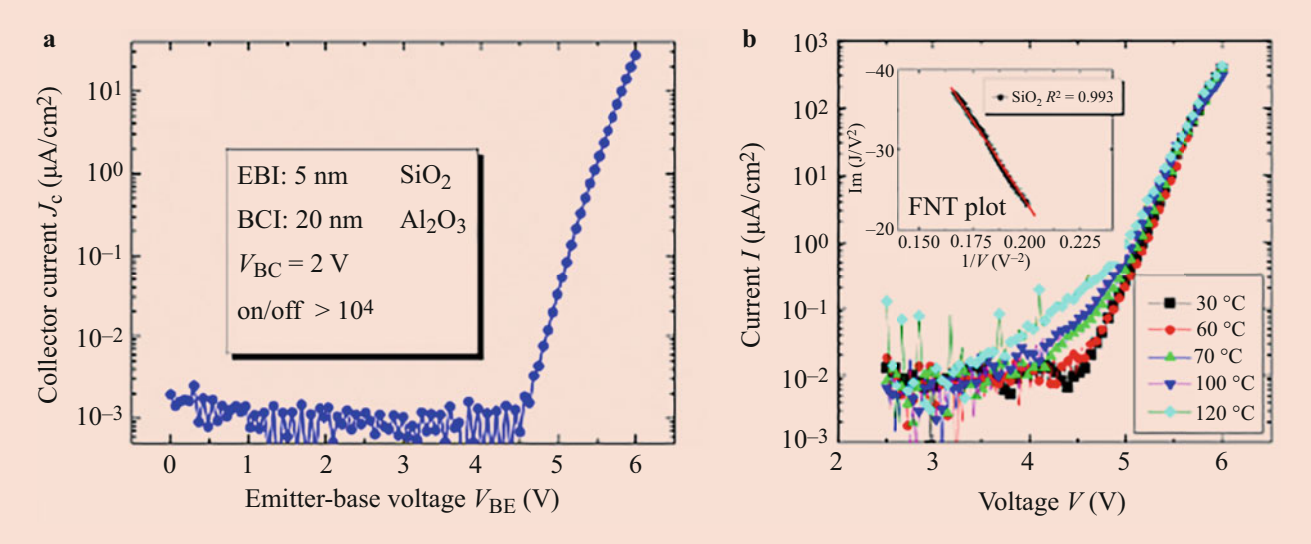


Fig. 25.12 (**a**) Transfer characteristics of a GBT with 5-nm-thick SiO_2 and 20-nm-thick Al_2O_3 as the EBI and the BCI, respectively. The transfer characteristics show an on/off ratio exceeding 10^4. (**b**) Temperature dependence I–V for the injection tunnel diode with 5-nm SiO_2 as the tunnel barrier. The inset FN plot shows an excellent linear fit. (Reprinted from [78], Copyright (2015), with permission from Elsevier)

trons, i.e., the common-base current gain or current transfer ratio $(\frac{I_C}{I_E}) = \alpha = 1$. Hence, the EBI barrier should be low and thin enough to provide a high current of hot electrons, yet block cold electron emission. For example, replacing a 5-nm SiO_2 EBI with 6-nm-thick ALD HfO_2 results in an improved threshold voltage and a higher emitter current (Fig. 25.13a). However, the choice of dielectric materials to form a low band offset barrier is limited to high-k dielectrics, which are known for reduced film and interface integrity compared to SiO_2. This means that for thin tunneling layers, defect-mediated carrier transport or unfavorable direct tunneling could become the dominant transport mechanisms. One possible solution is bilayer dielectric tunnel barriers, where a first thin layer in contact with the emitter provides a high-quality interface and material integrity, while a second layer reduces off-state leakage. Together, the bilayer dielectric minimizes defect-mediated carrier transport. This approach facilitates the application of low bandgap (high electron affinity) dielectrics to improve the emitter current by promoting Fowler-Nordheim or step tunneling [80] (Fig. 25.13b). Figure 25.13a shows a dramatic improvement in the emitter current by utilizing a novel $TmSiO/TiO_2$ (1 nm/5 nm) bilayer tunnel barrier, which is dominated by tunneling [81].

Experimental data combined with theory allows fairly accurate performance predictions. The performance of GBTs strongly depends on design parameters that should be chosen to maximize the current and minimize the loss mechanisms. Although the scattering of hot electrons in the base is minimized by using graphene, EBI parameters need to be accurately chosen to guarantee high injection current densities. Yet, the EBI needs to also prevent emission of cold electrons via defect-mediated electron transport or direct tunneling. These cold electrons are not able to surpass the base-collector barrier and lead to parasitic base current that limits α. Furthermore, the BCI needs to act as an electron filter, which allows the passage of the hot electrons and blocks cold electron emission from the base to the collector. This requires a low barrier to minimize the quantum mechanical backscattering of hot electrons at the BCI barrier and, simultaneously, suppress thermionic, tunneling, and defect-mediated electron transport from base to collector. Based on experimental data and theoretical considerations, the following requirements for the emitter current can be defined [81]:

(a) The current must be dominated by injection of hot electrons to the graphene or 2D material base (tunneling or thermionic emission). When these electrons have energies well above the Fermi level of the graphene base and the collector barrier height, they can overcome the collector barrier and contribute to the collector on current. This leads to a high current gain of the device.
(b) Emitter-base emission of cold electrons should be prevented. Electrons with energies comparable to the graphene-based Fermi level are backscattered from the base-collector barrier and contribute to the high parasitic base current. Since the emission of cold electrons is due to defects and direct tunneling (DT), high-quality barriers must be present, sufficient to prevent direct tunneling.
(c) High collector current density is required to enable high-frequency operation.
(d) High nonlinearity is essential to obtain high transconductance.
(e) A low threshold voltage is ideal for low-voltage operation.

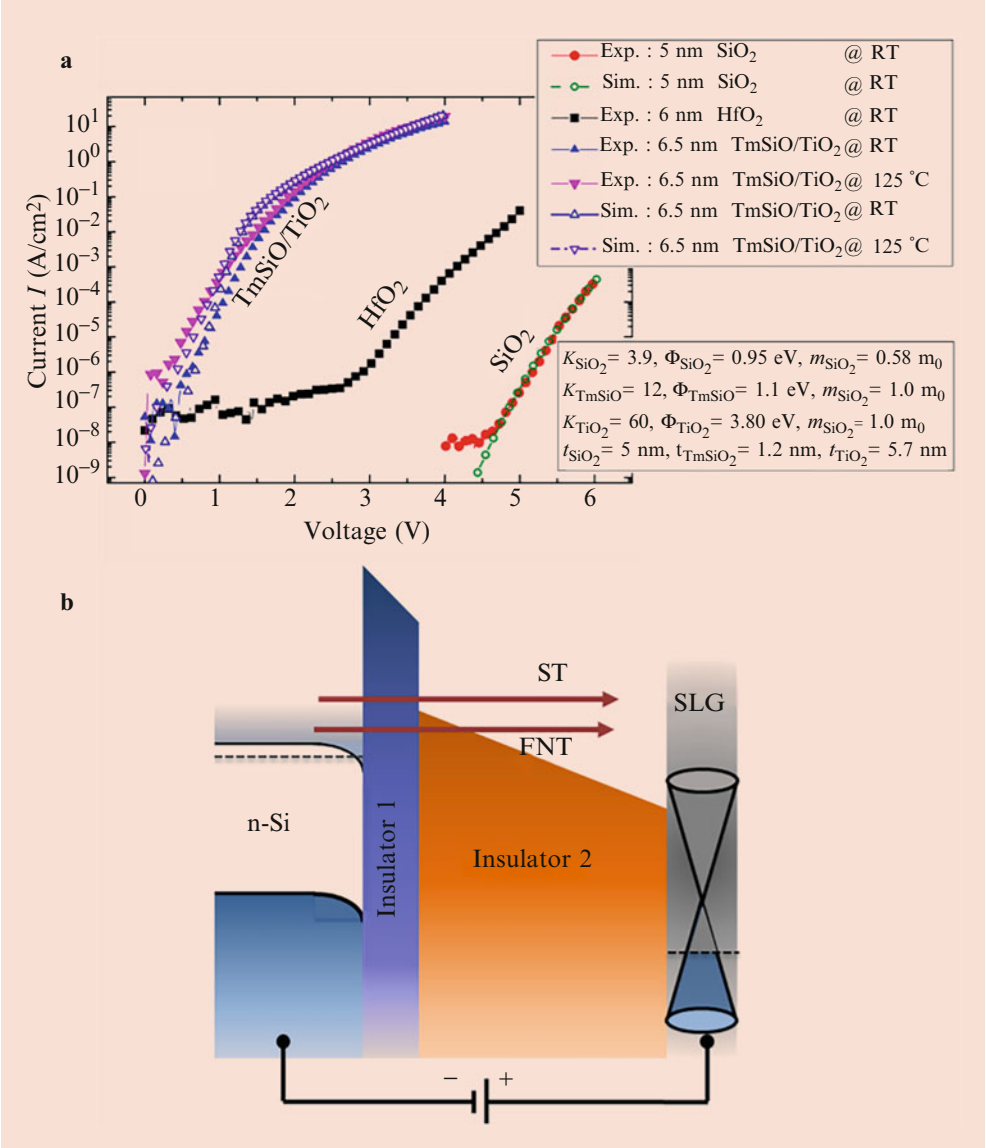


Fig. 25.13 (**a**) I–V characteristics of Si-insulator-graphene tunnel diodes with SiO_2, HfO_2, and $TmSiO/TiO_2$ tunnel barriers. The HfO_2 tunnel barrier with lower band offset with respect to Si conduction band shows improved I–V characteristics (blue triangulars) in comparison to SiO_2 (brown squares). Superior I–V characteristics have been achieved using $TmSiO/TiO_2$ bilayer tunnel barrier (red circles). The tunneling transport mechanisms in the bilayer tunnel barriers are shown in the (**b**) simplified band diagram. (Reprinted from [78], Copyright (2015), with permission from Elsevier)

So far, the entire set of conditions has not been met experimentally. Nevertheless, there are considerable efforts worldwide on GBTs or related devices. In fact, these conditions led to the theoretical prediction/invention of graphene-based heterojunction transistors (GBHTs), with low barriers made from semiconducting materials [82–84]. In addition, the RF performance potential of both GBTs and GBHTs has been predicted with multi-scale models, taking into account the limitations of process technology. Di Lecce et al. compared through numerical simulations an n-type Si GBHT with a state-of-the-art n-p-n SiGe HBT structure aggressively scaled to reach its performance limits from [85]. The study predicted that the GBHT may deliver an f_T that is two times higher compared to optimized HBTs assuming a transparent graphene/Si interface (Fig. 25.14). This is due to the monolayer thickness of the base region and the smaller emitter transit time due to the unipolar nature of the device (very few holes are present in the n-type device), another key feature which distinguishes the GBHT from the HBT.

25.2.7 Metal-Insulator-Graphene (MIG) Diodes

Metal-insulator-graphene (MIG) diodes , essentially one-half of the GBTs/GBHTs discussed in the previous section, can be

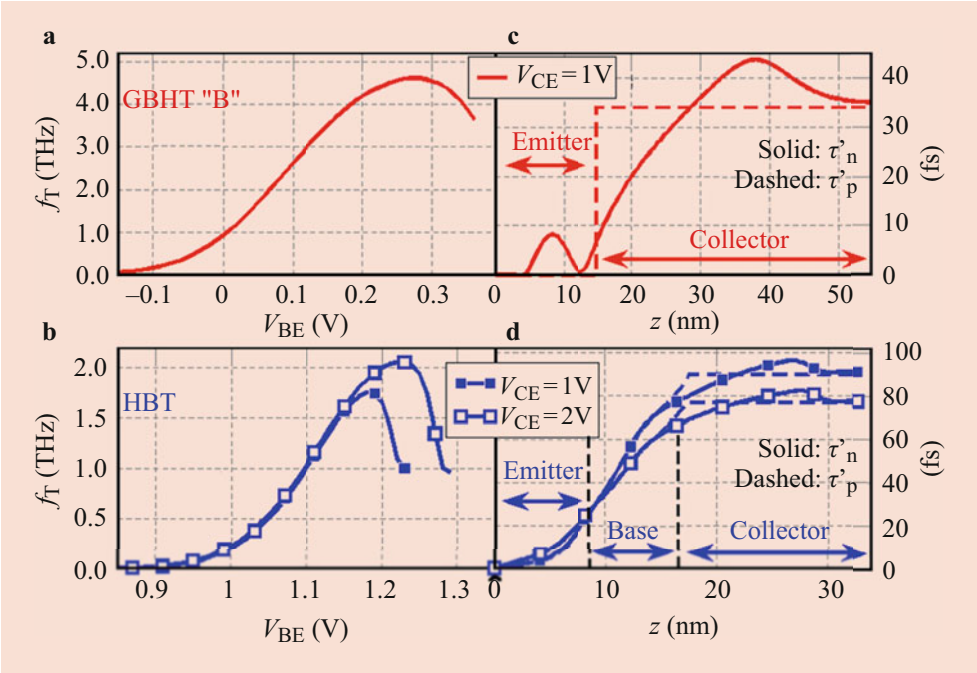
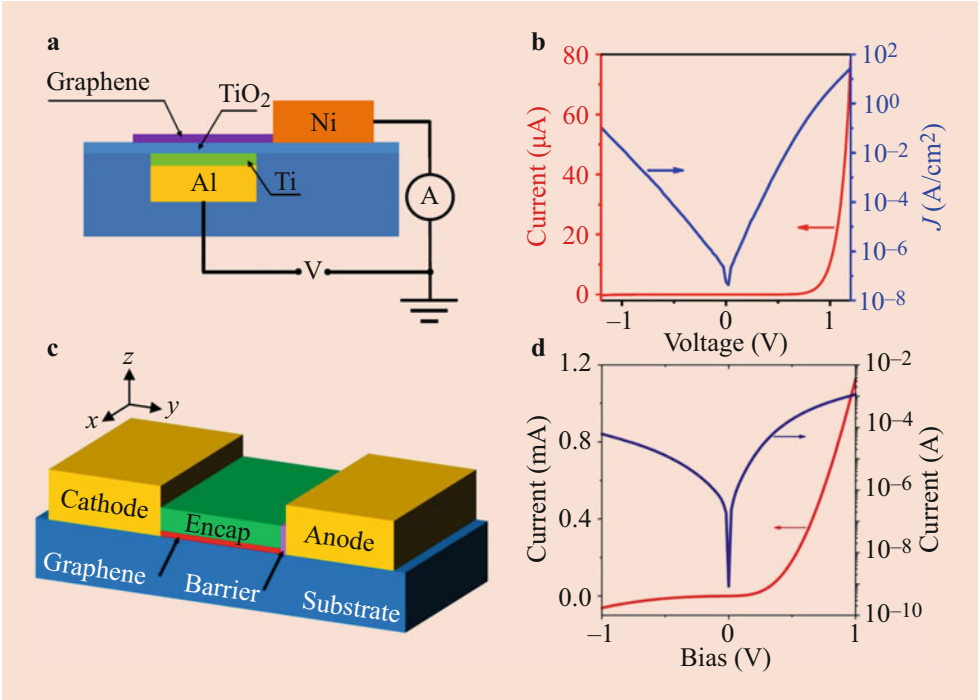


Fig. 25.14 f_T of the GBHT (**a**) and HBT (**b**), showing the capability of the former to outperform the HBT's cutoff frequency by a factor higher than 2. Accumulated transit times τ'_p and τ'_n along the devices, at the peak-f_T bias for the GBHT (**c**) and HBT (**d**). (Reprinted from [78], Copyright (2015), with permission from Elsevier)

utilized to realize different functional circuits. We therefore consider them as alternative devices for non-transistor-based electronics. The realization of p-n diodes is not possible with graphene, because of the gapless band structure and Klein tunneling, both leading to a linear IV characteristic of p-n junctions in graphene. Hence, MIG diodes have been realized and developed for several high-frequency circuit applications.

MIG diodes consist of a layer of graphene, an insulting layer, and a metal electrode similar to metal-insulator-metal (MIM) diodes. Current can flow through the insulator from the metal to the graphene either by tunneling or by thermal emission, depending on the insulator material. Due to asymmetric work functions of the metal and graphene, the IV characteristic is nonlinear. This effect is enhanced by a biased induced barrier height modulation on the graphene side, and thus the asymmetry of these diodes is higher compared to conventional MIM diodes. In 2014, a graphene/hBN/-graphene tunneling diode with a 6-nm-thick hBN barrier was experimentally demonstrated [88]. The diode showed DC rectification, with relatively low current levels of up to 10 nA. The diode was made by exfoliation of hBN and graphene, which is not a scalable process and was not characterized at RF frequencies. In 2016, an MIG based on 2-nm TiO_2 as insulator material was demonstrated [89], where thermal emission dominated the transport over tunneling. Yet again, the current levels were rather low (tens of nA), the characterization was limited to DC operation, and the fabrication process was based on graphene flakes. This MIG concept was extended with a similar layout and materials (6-nm TiO_2 as insulator) toward a fully scalable technique in 2017 [86] (Fig. 25.15a, b). The current level in these diodes was up to 100 μA, and characterization was performed at RF frequencies. The diodes showed asymmetry up to 520, nonlinearity up to 15, and responsivity up to 26 V^{-1}. The RF bandwidth defined by the RC product was about 30 GHz, with further improvements expected. The so-called one-dimensional (1D) MIG diodes, which form the junction only at the 1D edge of graphene, are expected to increase RC bandwidth to above 1 THz (Fig. 25.15c, d). Since the MIG diodes are quite reproducible compared to the current state of GFETs, there have been more complex ICs fabricated based on MIG diodes, such as power detectors [90, 91], receivers [92], mixers [93, 94], and frequency doublers [95], with examples shown in Fig. 25.16.

MIG diodes are very competitive to MIM diodes in their key DC characteristics, namely, nonlinearity, asymmetry, and responsivity (Table 25.6). The RF bandwidth is not yet competitive to silicon and III-/V-based p-n junction or Schottky diodes, which have RC bandwidth of up to or even above 1 THz; however, for many ICs, this bandwidth is not required at the moment. Theoretical calculations predict that several THz of bandwidth should be attainable with MIG diodes through design optimization. MIG diodes are thus very promising, in particular for IoT applications and for flexible electronics, because of their reasonably high performance and compatibility with thin-film processing. Applications at higher frequencies (>100 GHz) may be explored for applications like THz imaging sensors or radar, if the RC bandwidth can be improved.



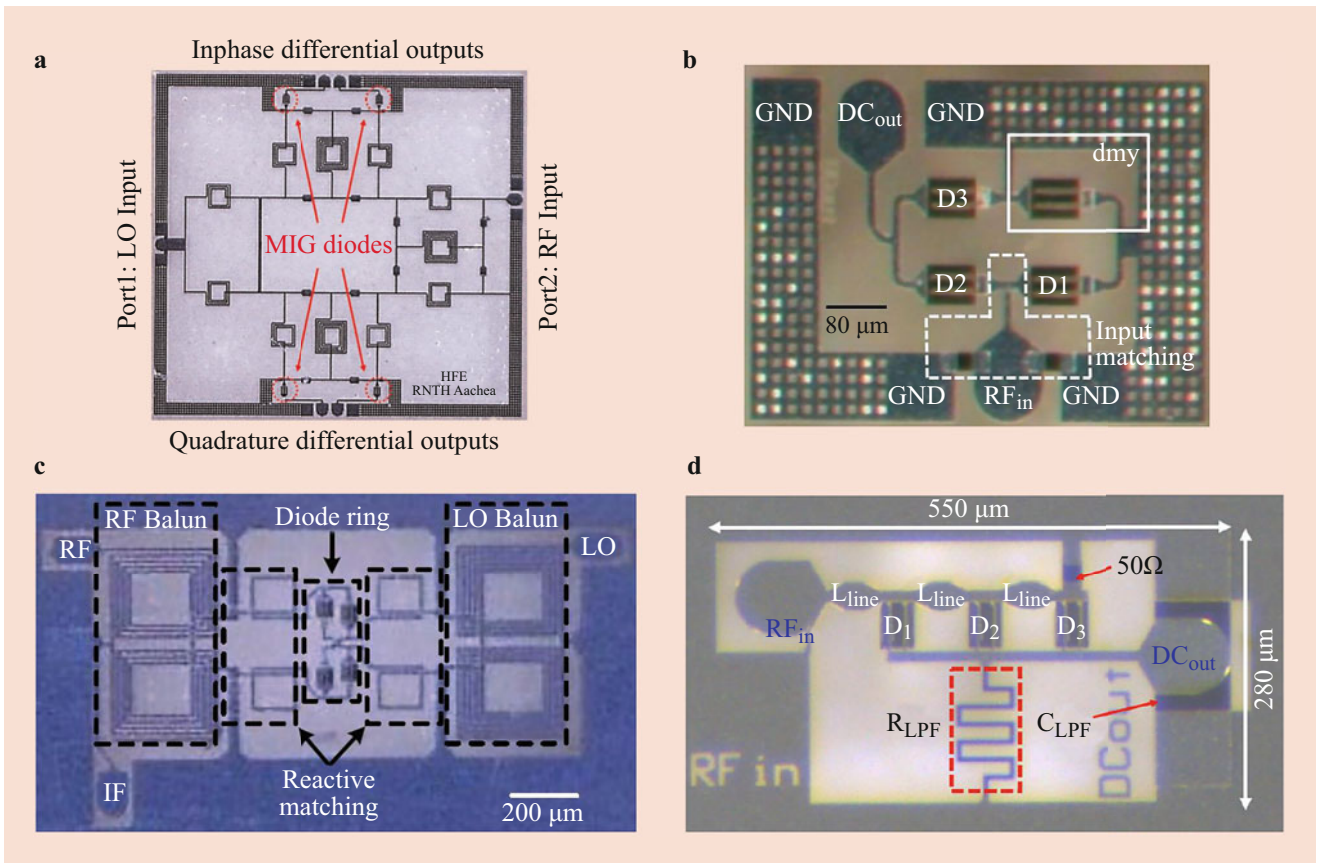


Fig. 25.15 Illustration of the MIG diodes (**a**, **b**) and 1D-MIG diodes (**c**, **d**), as well as the DC performance. (Reproduced from Ref. [86] with permission from The Royal Society of Chemistry. Reprinted with permission from Ref. [87]. Copyright (2019) American Chemical Society)

Fig. 25.16 Examples of integrated circuits based on MIG diodes. (**a**) Six-port receiver, QPSK with -10 dBm at 2.4 GHz carrier demonstrated on quartz. (Reproduced from Ref. [92] with permission from The Royal Society of Chemistry). (**b**) V-band (60 GHz) power detector, with high dynamic range of 50 dB. (**c**) Double-balanced upconversion mixer (6–12 GHz), with low conversion loss of −10 dB. (**d**) Three-stage distributed power detector (DC-70 GHz), with high dynamic range. (©2018 IEEE. Reprinted, with permission, from [90, 91, 94])

Table 25.6 Comparison of key diode parameters for MIG and MIM diodes including current density, asymmetry, nonlinearity, and responsivity

Stack material	J_{ON}(A/cm^2)	f_{ASYM}	f_{NL}	f_{RES}(V^{-1})
Nb/Nb_2O_5(5 nm)/Pt [96]	2.0	9.8	8.2	16.9
Nb/Nb_2O_5(15 nm)/Pt [97]	N/A	1500	4	20
Ti/TiO_2/bilayer graphene [89]	0.1	9000	8	10
Ti/TiO_2/graphene [86]	7.5	520	15	26

25.3 Carbon Nanotube-Based Transistors

After we have gained some insight on graphene, we will now start to discuss on CNTs, which can be considered as a one-dimensional tube rolled up from a sheet of graphene.

25.3.1 Band Structure of CNT

The structure of CNTs can be described by the circumference vector or chiral vector **C**, which represents the full circumference of the tube and is defined by

$$\mathbf{C} = n\mathbf{a}_1 + m\mathbf{a}_2 \equiv (n, m)$$

where a_1 and a_2 are the unit vectors in the two-dimensional plane and n and m are integers. This defines singe-wall CNTs, i.e., CNTs that have walls which consist of a single-graphene sheet. CNTs made up of several layers of graphene are called multiwall carbon nanotubes. They are not discussed in detail in this chapter, but are well covered in literature [98–101]. The propagation vector $\mathbf{T}_a$ is perpendicular to **C** and represents the periodicity of the tube along the tube axis (Fig. 25.17). The chiral angle θ ($0 \leq \theta \leq 30^\circ$) is defined as the angle between **C** and $\mathbf{a}_1$. As shown in Fig. 25.17, depending on different edges after rolling up, CNTs can be classified into three different groups: zigzag, armchair, and chiral types. If $n = m$, we have $\theta = 30^\circ$, and the CNT is armchair-type. If $m = 0$, we have $\theta = 0$, and the CNT is zigzag-type. For other situations with $0 < \theta < 30^\circ$, the CNTs are known as chiral-type, because they produce a mirror image of their structure upon an exchange of n and m.

For a (n, m) CNT, the circumference of the cross section L, the tube diameter d, and the chiral angle θ are defined as below, respectively [6]:

$$L = |\mathbf{C}| = \sqrt{\mathbf{C} \bullet \mathbf{C}} = a\sqrt{3\left(n^2 + nm + m^2\right)} \tag{25.11}$$

$$d = \frac{L}{\pi} = \frac{a}{\pi}\sqrt{3\left(n^2 + nm + m^2\right)} \tag{25.12}$$

$$\cos\theta = \frac{\mathbf{C} \cdot \mathbf{a}_1}{|\mathbf{C} \cdot \mathbf{a}_1|} = \frac{2n + m}{2\sqrt{n^2 + nm + m^2}} \tag{25.13}$$

Many electronic properties of CNTs are determined by the tube diameter and chiral angle, which are essentially defined by n and m.

We can derive the band structure of CNTs from that of graphene. For CNTs, a periodic boundary condition should be met along the circumference, which is

$$\mathbf{k} \cdot \mathbf{C} = 2\pi\nu \tag{25.14}$$

where ν is an integer and $\mathbf{k} = (k_x, k_y)$ is the allowed wave vector. Through the boundary condition, the allowed wave vector is now restrained to a set of lines in 2D plane. Each line with a different ν corresponds to a subband. If one of the lines intersects the K (or K') points, the resulting CNT is metallic; otherwise, they are semiconducting. Based on a geometrical analysis of Eq. 25.13, a rough conclusion can be drawn. If $n - m$ is a multiple of 3, the CNTs are metallic, while otherwise they are semiconducting with a bandgap of [6]

$$E_g \cong \frac{0.7}{d\,(\text{nm})}\text{eV}. \tag{25.15}$$

However, these considerations do not take the curvature of the tubes into account. Therefore, the conclusions are mainly valid for CNTs with relatively big diameter. For small CNTs, the curvature modifies their electronic structure. Thus, one typically observes a bandgap independent of chirality due to the quantum confinement effect [103].

Here we have two examples. In the case of an armchair tube (3,3), the periodic boundary conditions yield allowed values for the wave vector in circumferential direction according to

$$k_{y,\nu} = \frac{2\pi\nu}{3\sqrt{3a}} \tag{25.16}$$

where $\nu = 0, \pm 1, \ldots, \pm 3$. Figure 25.18a shows the projection of the allowed 1D states onto the first Brillouin

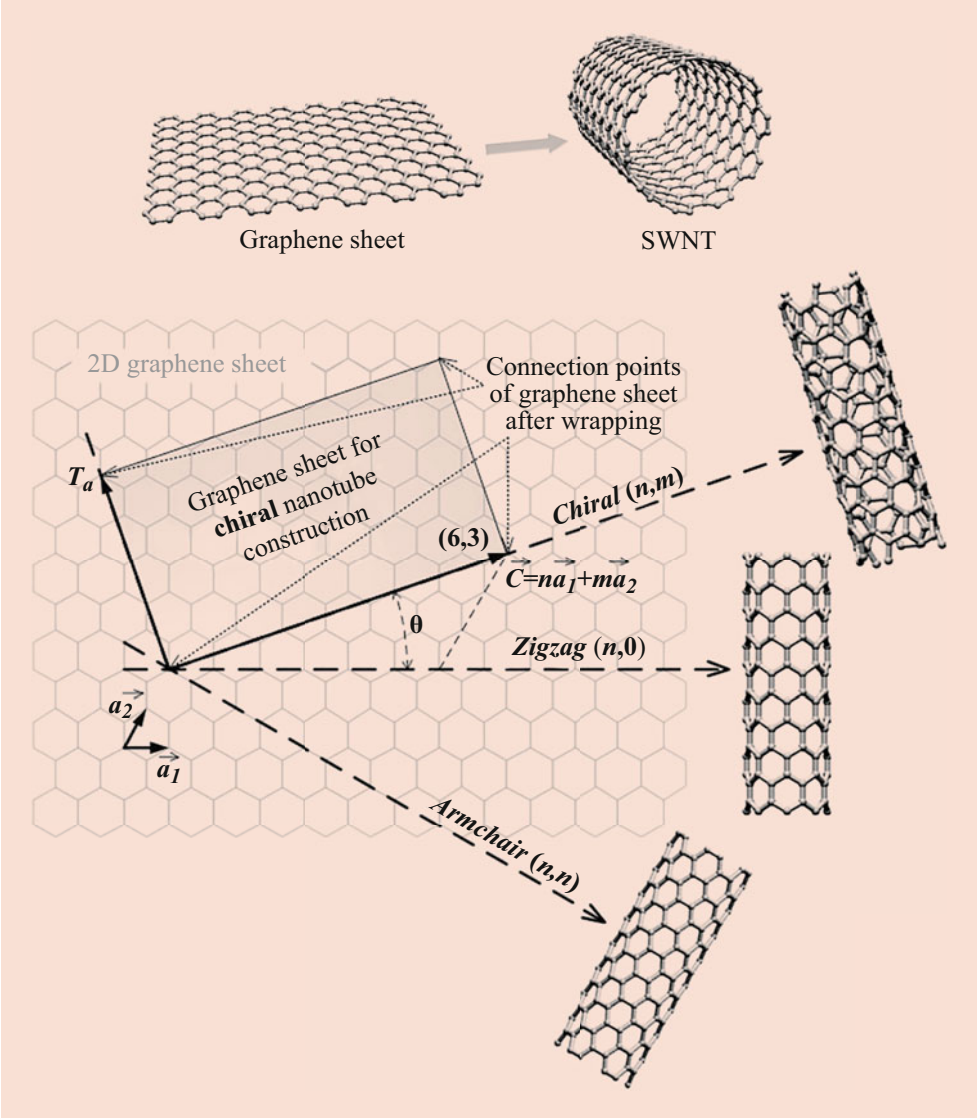


Fig. 25.17 The structure of CNT and different types of CNTs. (Republished with permission from The Royal Society of Chemistry, from [102])

zone of graphene, as well as the energy dispersion. Due to the periodic boundary condition in Eq. 25.16, the allowed states condense into lines (white lines in Fig. 25.18a). Here, there are three lines on either side of the center of the Brillouin zone and an additional line going through the center. In case of a (3,3) tube, the allowed states include the K points. The (3,3) tube and armchair tubes in general thus show metallic behavior.

As an example of a chiral tube, Fig. 25.18b shows the projection of the allowed 1D states onto the first Brillouin zone of graphene, as well as the energy dispersion for a (4,2) tube. Again, due to the periodic boundary conditions, the allowed states condense into lines (white lines in Fig. 25.18b). In contrast to the (3,3) tube, the $\mathbf{C}_h$ vector is not in parallel to the y-direction, and hence leads to a mixed quantization of k_x and k_y. The propagation of an electron along the tube axis is described by a combination of k_x and k_y components. The band structure of (4,2) tubes is determined by the fact that there are no modes which include the K points of the Brillouin zone of graphene. Therefore, a bandgap appears in the dispersion relation, and this type of tube is a semiconductor. The bandgap is of the order of a few eV.

25.3.2 CMOS and Integrated Digital Circuits Based on CNT

In order to realize simple CNT-based transistors, one approach is to place a CNT on a silicon wafer with SiO_2 as dielectric layer. After contacting two ends of the tube with appropriate metal electrodes, the device is ready to function as a back-gated transistor (Fig. 25.19). The silicon substrate

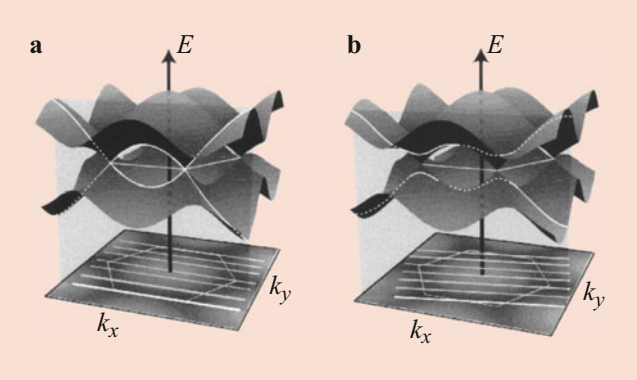


Fig. 25.18 Dispersion relation of CNTs. (**a**) A 3D illustration of the dispersion relation for graphene including the allowed states for the (3,3) CNT. The periodic boundary conditions along the circumference of the tube result in a discrete set of allowed k_y values. (**b**) A 3D illustration of the dispersion relation for graphene including the allowed states for the (4,2) CNT. The periodic boundary conditions along the circumference of the tube result in a discrete set of allowed k values. (© 2003 IEEE. Reprinted, with permission, from [104])

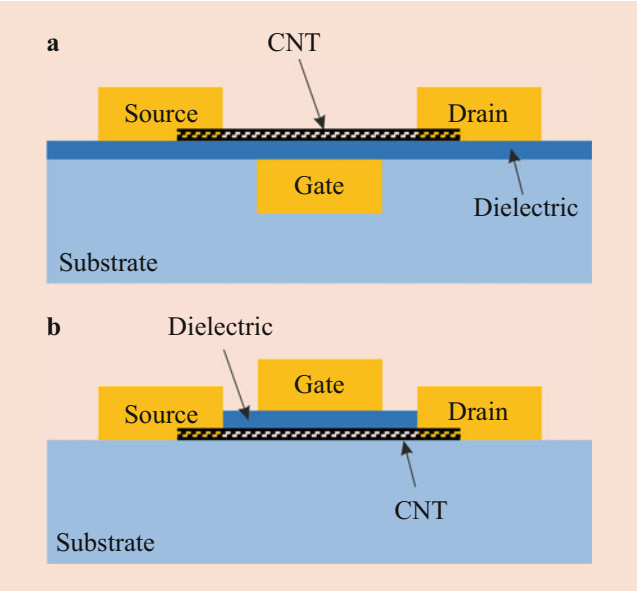


Fig. 25.19 Bottom-gate (**a**) and top-gate (**b**) CNT-based transistors

can be utilized as a gate electrode, and the contacts to the CNT serve as source and drain electrodes. Since many CNTs have a bandgap, CNT-based transistor can be switched off. In 1998, Tans et al. and Martel et al. successfully demonstrated the first back-gated CNT transistor independently by using Pt as contacting electrodes [105, 106]. These prototype transistors are not ideal due to the Schottky contact with platinum (Pt), resulting in a low on-state current. Javey et al. used palladium (Pd) contacts and obtained high-performance p-type CNT transistors [107]. This is because the contact with Pd is ohmic and the transistors showed ballistic transport. For a long time, n-type CNT transistors have been difficult to realize. In 2007, it was found that scandium can form n-type ohmic contacts with CNTs and later the same was found for yttrium [108–110]. These efforts enabled the realization of CNT CMOS circuits. A symmetrical top-gate CMOS inverter was demonstrated [111], and integrated circuits based on single CNTs have also been realized, demonstrated in Fig. 25.20 [112, 113]. Doping-free CNT transistors are of great advantage since for such an approach there is no need to modify the lattice structure of the CNTs or to use charge transfer doping at the CNT/gate dielectric interface, which typically reduces the performance of CNT transistors.

Due to the short-channel effect in traditional silicon MOSFETs, planar gates can no longer provide proper field-effect modulation for channels shorter than approximately 20 nm. Therefore, new device architectures such as FinFETs or multigate transistors were developed. CNT FETs have ultrathin channels defined by their diameter, which gives them near ideal scaling behavior. In addition, CNTs provide a nearly unperturbed inside, which allows ballistic transport over large distances and hence large potential for high on currents. CNT p- and n-type transistor with gate length of 10 nm has been demonstrated recently, with near ideal room-temperature subthreshold swing of 70 mV/dec [114].

Transistors based on a single CNT result in competing performance even compared to silicon-based technology. Yet, large-scale production is challenging since the control of the chirality and diameter of CNTs during synthesis does not yet meet semiconductor reproducibility standards. Hence, manufacturing of circuits with billions of nearly identical single CNT transistors on a wafer scale, as is the norm in silicon technology, is highly unlikely. Nevertheless, alternatives such as dense CNT arrays or CNT networks have been used for CMOS integrated circuit fabrication [115–120]. Compared to single CNTs, array- or network -based thin-film transistors can result in a fairly uniform performance over wafer scale since the CNTs can be presorted by using chemical methods [121]. Here, the device performance does not depend on single CNTs, but rather the average of many. Even in such arrays, metallic CNT components, control of CNT density, and contact resistance variations remain challenges for digital circuit applications [122].

Despite these challenges, CNT-based digital integrated circuits reached new integration levels, with a modern microprocessor with 14,000 CMOS transistors demonstrated in 2019 (Fig. 25.21) [123]. This 16-bit microprocessor is based on the RISC-V instruction set, and it runs standard 32-bit instructions on 16-bit data and addresses. In this technology demonstration, p-type and n-type transistors have

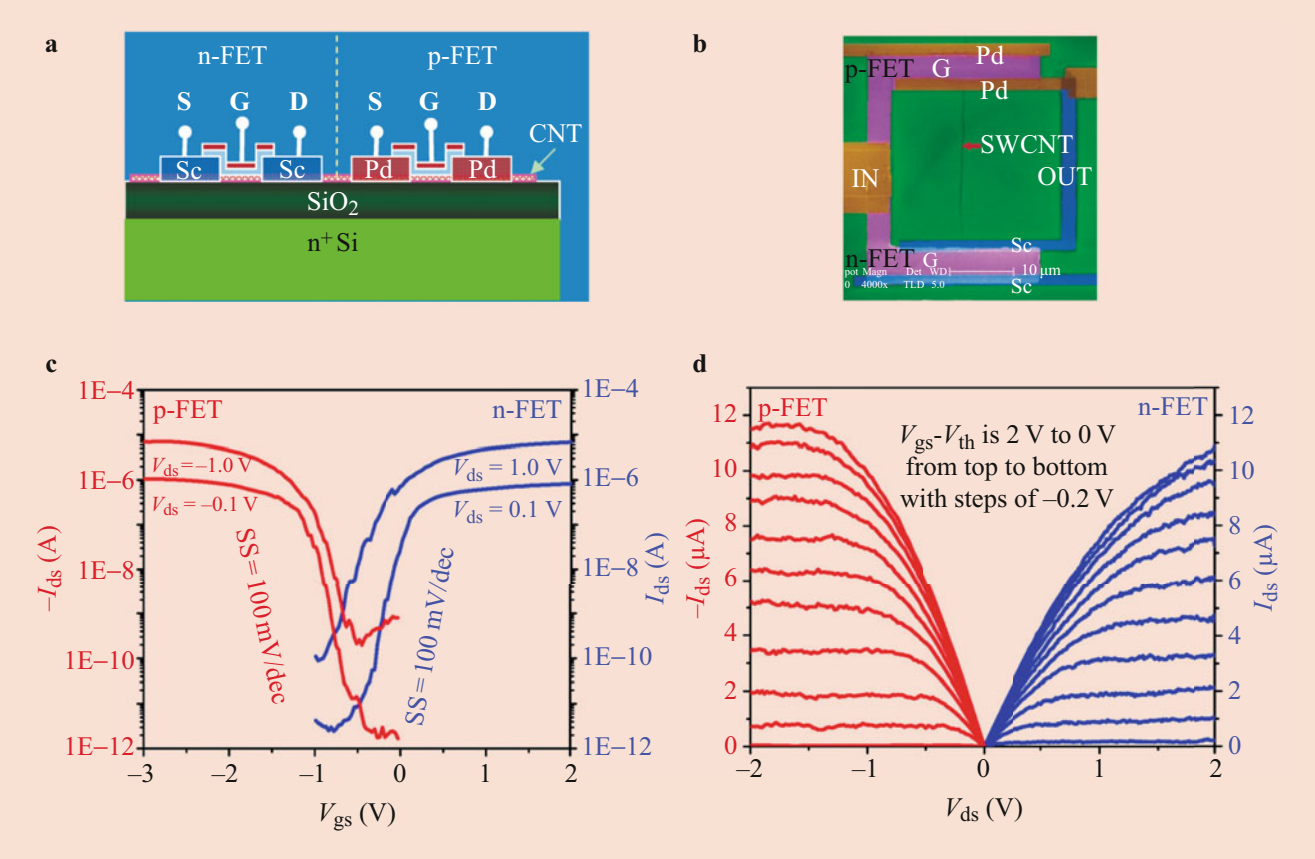


Fig. 25.20 Single CNT-based CMOS digital circuits. (**a**) The geometry of the device. (**b**) The SEM image of the CMOS inverter. (**c**) Transfer and (**d**) output characteristics of a pair of p- and n-type CNT transistor. (Reprinted with permission from Ref. [111]. Copyright (2019) American Chemical Society)

been realized through contact engineering using Pt and Ti metal contacts in combination with silicon oxide and hafnium oxide, respectively. This design and fabrication methodology for CNT technology is proposed to overcome the imperfections inherent in the materials system. This technology is also suitable for circuits made on flexible substrates [124]. Finally, a heterogeneous integration on a chiplet level may enable simple co-integration with silicon logic or memory [125].

25.4 Summary

Carbon electronics has remained a high potential candidate for future electronic applications. Although no products are on the market today, the performance and maturity of demonstrators and fabrication technologies for graphene and CNTs keep improving. At the same time, silicon technology keeps moving along at an incredible pace, driven by business demands. Hence, the investments for developing silicon technology are extraordinarily higher than for developing carbon technology. This means that carbon-based devices or circuits might become products if they found niche applications first, similar to early-stage compound semiconductor technology. Here flexible electronics may provide a suitable platform, as existing technologies cannot compete in terms of performance with carbon electronics. For example, CNT processors or graphene analog circuits can easily be manufactured on flexible substrates. In addition, 3D stacking of functional layers in conjunction with silicon CMOS may be an entry point for graphene and CNTs. This and other co-integration approaches provide further opportunities for additional functionality in silicon technology, i.e., for sensing, optoelectronics, photonics, or novel fields like neuromorphic or quantum computing. In summary, although silicon technology is still superior in integration density and overall performance, these advances show potential routes for carbon to enter the semiconductor industry.

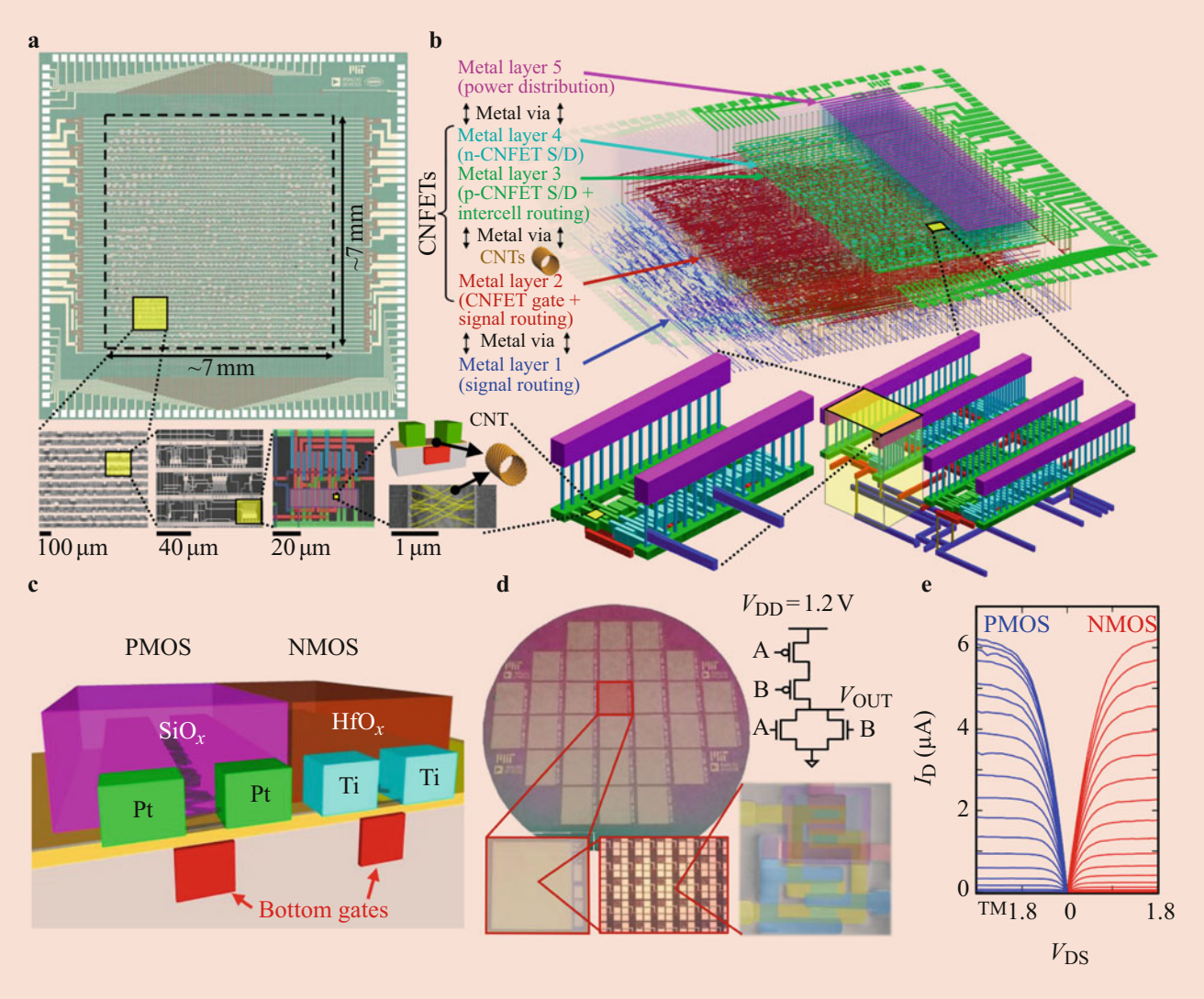


Fig. 25.21 The microprocessor based on CNT RV16X-NANO, as well as the CMOS technology which is utilized. (**a**) Image of an RV16X-NANO chip. (**b**) Three-dimensional schematic of the physical layout. (**c**) Schematic of CNFET CMOS technology. (**d**) Dies with 10,400 CNFET CMOS digital logic gates across 150-mm wafers is fabricated. (**e**) Output characteristics showing p-CNFETs and n-CNFETs. (Reprinted by permission from Nature [123] COPYRIGHT (2019))

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Negative Capacitors and Applications

26

Muhammad Ashraful Alam, Nicolò Zagni, Atanu Kumar Saha, Niharika Thakuria, Sandeep Thirumala, and Sumeet Kumar Gupta

Contents

26.1 Introduction . . . 932
26.1.1 Classification of Next-Generation Transistors . . . 932
26.1.2 Phase Transition and Landau Theory . . . 933

26.2 Device Physics of NCFETs . . . 933
26.2.1 Phenomenological Theory of NCFETs . . . 933
26.2.2 Tailoring Negative Capacitance by Energy Landscape Engineering . . . 936
26.2.3 Reliability Physics of NCFETs . . . 938
26.2.4 Advanced Issues . . . 938

26.3 Device Physics of PhaseFETs . . . 939
26.3.1 Behavioral Compact Model . . . 940
26.3.2 Physics-Based Phenomenological Model . . . 940
26.3.3 Experimental Results on PhaseFETs . . . 941

26.4 Boolean Computing with NCFETs, FeFETs, and PhaseFETs . . . 941
26.4.1 Logic Design . . . 941
26.4.2 SRAM Design . . . 944
26.4.3 Nonvolatile Memory Design . . . 945

26.5 Non-boolean Computing with NCFETs, FeFETs, and PhaseFETs . . . 948
26.5.1 Coupled Oscillator-Based Computing . . . 948
26.5.2 Neuromorphic Computing . . . 949

26.6 Summary and Conclusions . . . 953

References . . . 954

Abstract

The long-standing tug-of-war between off-state leakage power consumption and switching speed has posed severe challenges to the scaling of semiconductor devices. Deeply scaled short-channel transistors are faster but consume more off-state power. This power vs speed trade-off stems from the fundamental physical limit related to the thermionic emission that governs switching in field-effect transistors. There is a broad consensus in the semiconductor industry that future progress is impossible unless the next-generation transistors and circuits overcome the so-called Boltzmann limit associated with thermionic emission over a barrier and offer a steeper on-off switching to enable a more aggressive voltage scaling.

In this chapter, we explain the need for and suggest an intuitive classification of the emerging transistor technologies. We use two illustrative examples of next-generation transistors (i.e., negative capacitance FET (NCFET) and phase FET (PhaseFET)) to explain the relative merits of gate-controlled vs channel-controlled steep-slope switching. We explain the basic principle of device operation, summarize the experimental results reported in the literature, and highlight the speed and reliability challenges to be resolved before the devices are integrated into practical systems. In addition, the chapter includes a careful analysis of circuits based on these emerging transistor technologies with applications toward Boolean logic, memories, and non-Boolean computing. The analysis suggests relative merits of various circuit designs and application-specific opportunities for significant power-performance improvement.

Keywords

Negative capacitors · Steep-slope switching · Landau FETs · Non-Boolean computing

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26.1 Introduction

Since the early 1970s, the progress in the semiconductor industry has been dictated by the scaling of (field-effect) transistors that allow each generation of devices to have significant performance improvements over its predecessor. The tremendous growth of the computing power was driven by Moore's law from the cost/economical point of view and by Dennard scaling from the performance/physical point of view. A decisive change of course began to occur at the beginning of the twenty-first century, when transistor speed began to saturate due to self-heating and the limits of power dissipation ($\sim$100 W/cm^2) in an integrated circuit were reached.

This problem was initially solved (or circumvented) (a) from the system point of view by switching to multicore architectures and (b) from the device perspective by devising new scaling rules. These rules formed the so-called "equivalent scaling" roadmap, which relied on the introduction of new insulating materials (to limit the leakage power consumption) and of complex three-dimensional geometries (to improve electrostatic control and limit the short-channel effects). Although scaling was effectively preserved and performance could still improve, the issues brought up by new geometries in terms of self-heating (and thus temperature rise) threatened to stop transistor scaling once more. This aspect motivated researchers to focus on new device concepts with the ultimate goal of decreasing power dissipation and thus control temperature rise in transistors. The equivalent scaling rules, which are expected to be effective until around 2025 [1], will need to be replaced by next-generation transistors and computing architectures to sustain the semiconductor industry.

26.1.1 Classification of Next-Generation Transistors

It has been clear since the 1990s that next-generation transistors would have to circumvent the fundamental limits of classical Boltzmann field-effect transistors (FETs). The initial focus on tunnel FET (TFET) and resonant-tunneling transistors has now broadened to include NCFET, PhaseFET, MottFET, MEMS relay, etc. These beyond-Boltzmann FETs rely on new physical principles and device designs to overcome the fundamental limit of transistor switching. This limit is related to the energy required by electrons to overcome a potential barrier, expressed in multiples of k_BT (k_B is the Boltzmann constant, and T is the temperature), which in turn forces the minimum voltage swing required to decrease the transistor current by one order of magnitude to the value of 60 mV/dec at room temperature. This minimum voltage swing is called subthreshold swing (SS) and is expressed as follows:

$$\begin{aligned} SS &= \left(\frac{\partial \log I_D}{\partial V_{GS}}\right)^{-1} = \left(\frac{\partial \psi_s}{\partial V_{GS}} \times \frac{\partial \log I_D}{\partial \psi_s}\right)^{-1} \\ &= \left(\frac{\partial \psi_s}{\partial V_{GS}}\right)^{-1} \times \left(\frac{2.3 k_B T}{q}\right) \\ &= m \times n \approx m \times 60\ \text{mV/dec} \end{aligned} \tag{26.1}$$

where I_D is the drain current, V_{GS} is the gate-to-source bias voltage, ψ_s is the surface potential, m is the body factor (described more in detail later), n is the transport factor, and q is the elementary charge. The SS imposes a lower limit on the minimum allowable operating voltage for a target on- to off-current ratio of $V_{min} \approx SS \times \log (I_{ON}/I_{OFF})$. It is then clear than to further reduce power dissipation, SS needs to be decreased. From Eq. (26.1), it is possible to devise different strategies to reduce SS, through either m or n. The classes of transistors belonging to the family of beyond-Boltzmann devices – originating from the attempts of reducing m and/or n – can be classified as follows:

- *Non-thermionic FETs* ($m = 1$, $n < 60$) exploit physical mechanisms different from the thermionic emission to control the channel conduction. One can either reduce the electron temperature below the lattice temperature to suppress off-state conduction or use positive electrothermal feedback to enhance on-state conduction. This category includes TFETs [2, 3], impact ionization FETs (IFETs) [4], PhaseFETs [5], and MottFETs [6].
- *Landau FETs* ($m < 1$, $n = 60$) exploit the "negative capacitance" effect to lower the body factor [7, 8]. This category includes NCFET, nano-electromechanical FET (NEMFET) [9], suspended-gate FET (SGFET), etc.
- *Super FETs* ($m < 1$, $n < 60$) combine the benefits of non-thermionic FET and Landau FETs to obtain minimum subthreshold swing, such as the negative capacitance tunnel FETs (NC-TFETs) [10] or phase change tunnel FETs (PC-TFETs) (with the phase transition material (PTM) layer inserted in the gate stack [11]).

Figure 26.1 summarizes the different class of transistors in the space defined by the possible combinations of m and n, including also classical Boltzmann FETs, characterized by $m > 1$ and $n = 60$. In this chapter, we will focus on two illustrative examples of next-generation switches, namely, NCFETs and PhaseFETs. In the following, we will explain device physics, reliability limits, as well as circuit implications of these transistors.

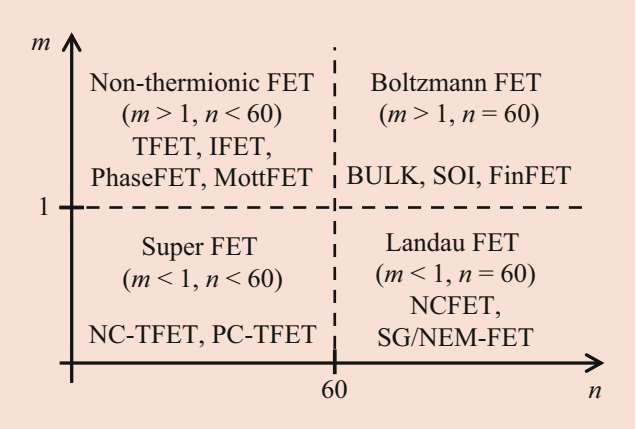

Fig. 26.1 Transistor classes in the $m \times n$ space. NCFETs belong to the Landau switch category, where m is reduced, thanks to the stabilized negative capacitance effect. PhaseFETs (and MottFETs) belong to the non-thermionic FET class as they alter the channel transport to achieve $n < 60$

26.1.2 Phase Transition and Landau Theory

We now briefly discuss some elements of phase transition and Landau theory which are at the foundation of both NCFETs and PhaseFETs operation. Phase transitions are changes occurring in a thermodynamic system when a certain order parameter of the system itself changes suddenly in response to an external stimulus. Examples of materials that undergo phase transitions are $BaTiO_3$, which experience dielectric to ferroelectric transition [12], and VO_2, which experiences insulator-to-metal transition [5]. Regardless of the physical stimulus triggering phase transition, the order of the system is disrupted from its previous state, which can be restored if the reverse process is stimulated. This interesting physical behavior is at the core of the operation of the devices discussed in this chapter.

In ferroelectric materials, the stored energy as a consequence of phase transition can trigger the so-called negative capacitance behavior [7]. This behavior occurs only if the instability associated with the negative capacitance (NC) effect can be stabilized (and this is indeed achieved by device design, as discussed in Sect. 26.2). The free energy of a ferroelectric U (in the case of uniform, mono-dimensional polarization) can be written as follows:

$$U = \alpha P^2 + \beta P^4 + \gamma P^6 - E \times P \qquad (26.2)$$

where, α, β, γ are material parameters, E is the external applied electric field, and P is the polarization of the ferroelectric. For a negative capacitor, α is always negative [7].

Although the Landau theory allows for a phenomenological interpretation of ferroelectric behavior (based on a mean-field approach [13]), it can be shown that the Gibb's free energy as written in Eq. (26.2) can be derived also starting from microscopic physics arguments [14]. In practice, this allows to connect the Landau parameters (α, β, γ) to physical properties of the ferroelectric (such as dielectric constant, temperature dependence, and so on). In Sect. 26.2, we will discuss how we can use Eq. (26.2) to deduce the NC behavior and exploit the effect for novel transistor design.

For PTMs employed in PhaseFETs, such as vanadium dioxide (VO_2), when the device temperature reaches a critical temperature (T_c), an abrupt transition occurs causing the material to switch between metal and insulator states, and vice versa. The temperature of a PhaseFET varies due to self-heating determined by the current flow as controlled by the transistor. The phase transition of VO_2 leads to the sub-thermionic switching of the transistor, as we will discuss in more details in Sect. 26.3.

26.2 Device Physics of NCFETs

In this chapter, we will describe the fundamental aspects of the physics behind NCFET operation. The discussion is built upon Landau theory introduced in Sect. 26.1.2 that allows deriving the electrostatics of the system composed by a conventional metal oxide semiconductor FET (MOSFET) and the NC layer (i.e., the ferroelectric layer).

26.2.1 Phenomenological Theory of NCFETs

Figure 26.2 shows the two typical NCFET configurations: metal-ferroelectric-insulator-semiconductor (MFIS) (Fig. 26.2a) and metal-ferroelectric-metal-insulator-semiconductor (MFMIS) (Fig. 26.2b). Regardless of the specific configuration, an appropriately designed ferroelectric layer can behave like a negative capacitor, storing energy and thus amplifying the applied gate bias [1, 7]: this phenomenon is the fundamental mechanism for the steep *SS* in NCFETs. The oxide layer between the ferroelectric and the semiconductor (either with the metal in between or not) is required in order to stabilize the ferroelectric in the NC region and to obtain sub-60 mV/dec *SS*.

Body Factor Reduction with Negative Capacitors

Before moving into the details of NCFET device physics, it is instructive to understand how the body factor m can be reduced through the negative capacitance effect. To illustrate

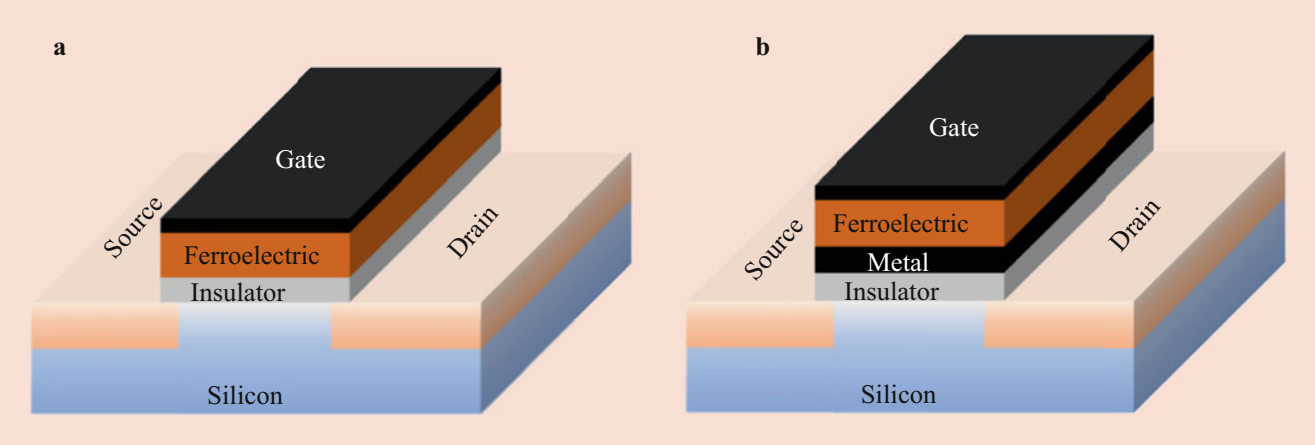

Fig. 26.2 Sketch of the NCFET configurations: (**a**) MFIS and (**b**) MFMIS. If stabilized, the ferroelectric layer in the gate stack can provide voltage amplification to reduce the subthreshold slope

the concept, we will consider a simple network of three capacitors in series, as shown in Fig. 26.3a. This network simplifies the gate stack of NCFETs composed by the NC layer, (C_{NC}), the gate oxide layer (C_{ox}) (SiO_2, normally), and the semiconductor layer (C_s). For simplicity, we will consider C_s to be a constant. Thus, the relation between ψ_s and V_{GS}, can be written as (see Fig. 26.3a)

$$m \equiv \frac{\partial V_{GS}}{\partial \psi_s} = 1 + \frac{C_s}{C} \tag{26.3}$$

where $C \equiv (C_{NC} + C_{ox})/(C_{NC}C_{ox})$. Since $C_{NC} < 0$, then $m < 1$ and $SS < 60$ mV/dec. Reducing m and SS leads to lower-power consumption, as the off-state current $I_{OFF} = I_D(V_{GS} = 0)$ is reduced. This can be simply understood from the relationship between V_{GS} and subthreshold current:

$$I_{OFF} = I_0 \times e^{\frac{q\psi_s}{kT}} \sim I_0 \times e^{\frac{-qV_T}{mkT}} \tag{26.4}$$

where V_T is the threshold voltage of the transistor and I_0 a proportionality factor (which depends on device properties). Figure 26.3b shows graphically the reduction in I_{OFF} obtained with NCFETs compared to conventional MOSFETs.

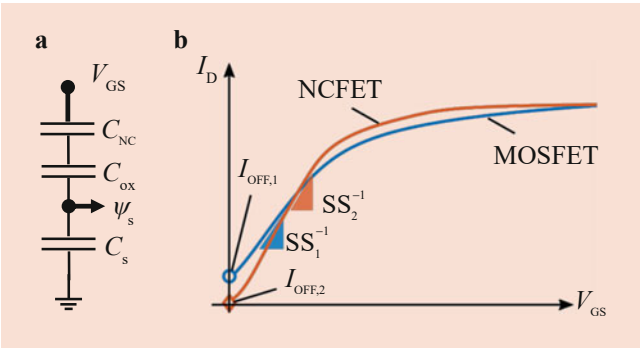

Fig. 26.3 (**a**) Simplified capacitor divider network of the gate stack to illustrate the concept of body factor m reduction. If a negative capacitance layer is used, such that $C_{NC} < 0$, then $m \equiv \partial V_{GS}/\partial \psi_s < 1$, and SS is reduced. (**b**) I_D–V_{GS} characteristics of a MOSFET (blue solid line) and NCFET (red solid line) showing that reduced SS leads to reduced I_{OFF} and thus lower-power consumption

Capacitance Matching Condition

Having clarified the role of NC in body factor reduction, we can discuss more in detail the physics of NCFETs. The discussion focuses on how to obtain effective reduction in SS by careful matching of the nonlinear C_s and C_{NC}. The NCFET analysis is presented considering a bulk MOSFET as the underlying transistor (however, it can also be adapted to encompass different kinds of transistors). The capacitance network needed to calculate the body factor reduction in an NCFET is shown in Fig. 26.4. C_{FE} is the ferroelectric (FE) layer and C_{MOS} is the MOSFET gate stack capacitance, composed by the series of the gate oxide layer, C_{ox}, and the semiconductor capacitance, C_s.

Compared to a standard MOSFET, an NCFET has an extra capacitance C_{FE} that adds an additional voltage drop, V_{FE}, to that of the gate oxide, V_{ox}. If the FE is stabilized in the NC region, then V_{FE} can become negative, thus providing voltage amplification. The constraint to guarantee the stable operation in the NC region is defined as the capacitance matching condition (CMC). We will derive the CMC starting with the ψ_s vs V_{GS} relation obtained by invoking the Kirchhoff voltage law (KVL) at the gate-to-source loop. This approach

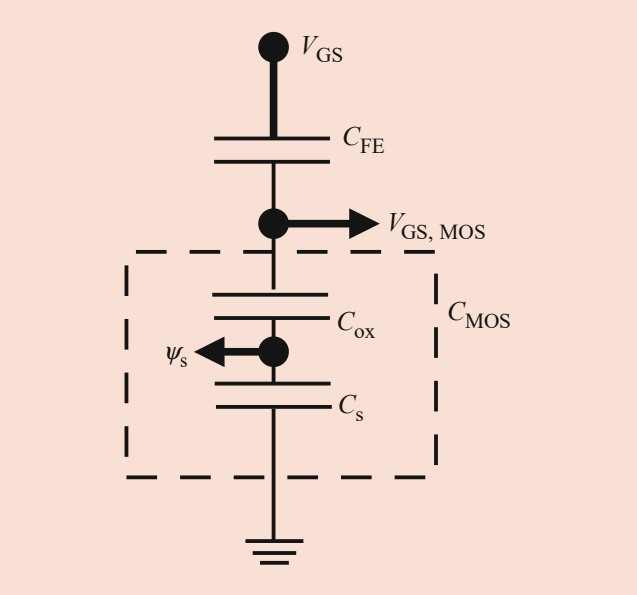

Fig. 26.4 Network capacitance for deriving the KVL at the gate-to-source loop. The voltage gain A_V between V_{GS} and $V_{GS,\,MOS}$ becomes >1 when C_{FE} is negative and with magnitude close to C_{MOS}

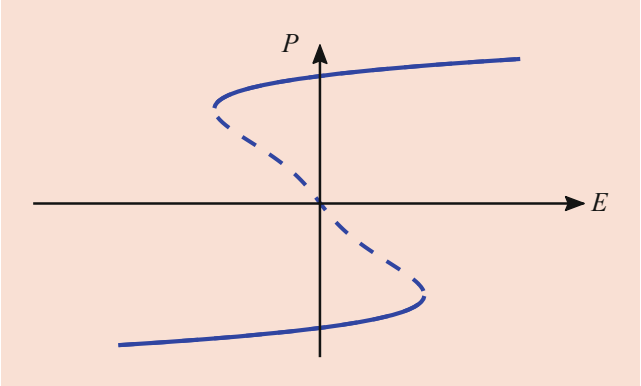

Fig. 26.5 P – E loop representing the solution of the time-independent LKE. The parameters chosen are $\alpha = -1.0 \times 10^7$ m/F, $\beta = -8.9 \times 10^8$ m^5/F/C^2, and $\gamma = 4.5 \times 10^{10}$ m^9/F/C^4 for $BaTiO_3$ [7, 17]. The dashed line represents the part of the loop for which negative capacitance occurs

is equivalent to the minimization of the Gibb's free energy of the system [15] and thus is physically sound within the limits of the validity of the theory. The KVL can be written as follows [16, 17]:

$$V_{GS} - V_{FB} = V_{FE} + V_{ox} + \psi_s \tag{26.5}$$

where V_{FB} is the flat-band voltage. V_{FE} is obtained from the phenomenological description of the FE behavior as given by the Landau-Khalatnikov equation (LKE) [7]. The LKE in the case of one-dimensional polarization component reads as follows:

$$\rho \frac{dP}{dt} + \frac{\partial U}{\partial P} = 0 \tag{26.6}$$

where U is the Gibb's free energy of the ferroelectric (see Eq. (26.2)) and ρ is the ferroelectric damping parameter (inversely related to the switching speed of the system). From Eqs. (26.2) and (26.6), it is possible to write an expression for the electric field applied to the ferroelectric as a function of the polarization, as follows:

$$E = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{dP}{dt} \tag{26.7}$$

By equating the polarization of the ferroelectric, P, to the semiconductor charge Q_s (i.e., the second term in $Q = P + \varepsilon E$ is considered to be negligible for simplicity, as the electric field in the ferroelectric is small [16]) and by focusing on the steady-state response (i.e., $\rho\, dP/dt = 0$ in Eq. (26.6)), then V_{FE} can be written as

$$V_{FE} = T_{FE}\left(2\alpha Q_s + 4\beta Q_s^3 + 6\gamma Q_s^5\right). \tag{26.8}$$

where T_{FE} is the ferroelectric layer thickness. From this equation, one can define the NC region that gives rise to body factor reduction, as shown in Fig. 26.5. The characteristic "S-shaped" curve between the two stable polarization branches (i.e., $-P$ and $+P$) represents the unstable NC region, where $(\partial^2 U/\partial P^2)^{-1} < 0$. This point will be discussed further in Sect. 26.2.2 for the whole class of NC systems, called Landau FETs. Thus, in the NC region, V_{FE} can assume negative values, so that the effective gate voltage seen by the MOSFET, $V_{GS,MOS}$, becomes larger than the applied bias. That is:

$$V_{FE} < 0 \Rightarrow V_{GS,MOS} = V_{GS} - V_{FE} > V_{GS} \tag{26.9}$$

We can define the internal voltage gain, A_V, as follows:

$$A_V \equiv \frac{dV_{GS,MOS}}{dV_{GS}}. \tag{26.10}$$

When the transistor is stabilized in the NC region (i.e., $A_V > 1$), the internal voltage amplification allows to achieve steep-slope operation. The capacitor divider network in Fig. 26.4 allows then to derive a simple equation for A_V through the expressions of C_{FE} and C_s. The former, C_{FE}, is derived by taking the inverse of $\partial V_{FE}/\partial Q_s$ [16]:

$$C_{FE} = \frac{1}{T_{FE}\left(2\alpha + 12\beta Q_s^2 + 30\gamma Q_s^4\right)} \tag{26.11}$$

Thus, simply

$$A_V = \frac{C_{FE}}{C_{FE} + C_{MOS}} = \frac{|C_{FE}|}{|C_{FE}| - C_{MOS}} \tag{26.12}$$

Clearly, A_V is maximized if $|C_{FE}| \rightarrow C_{MOS}$: this is the CMC. In the following, we discuss the design constraints necessary for CMC.

Design Constraints for Gain Maximization

To maximize A_V and reduce *SS*, it is crucial to design C_{FE} to match C_{MOS}. Since both C_{FE} and C_{MOS} are nonlinear and bias-dependent, CMC can only be obtained for a limited V_{GS}. Indeed, Fig. 26.6 shows that the ferroelectric thickness T_{FE} dictates the I_D–V_{GS} characteristics (Fig. 26.6a), the internal voltage amplification A_V–V_{GS} (Fig. 26.6b), and the corresponding *SS*–V_{GS} (Fig. 26.6c) ($T_{FE} = 0$ nm in Fig. 26.6 corresponds to a stand-alone MOSFET). Figure 26.6c confirms that *SS* is reduced significantly only over a limited range of V_{GS} because of the nonlinear, voltage-dependent C_{FE} and C_s. In general, transistors based on other semiconductor technologies (such as Ge, 2D metal transition dichalcogenides, compound semiconductors, and so on) will have different *SS* values for different V_{GS} range [18]; thus, each technology must be optimized based on their specific geometry and operating conditions. Section 26.2.4 summarizes the experimental results of NCFETs for different technologies, showing a relatively large scatter among the *SS* values due to different CMC conditions.

Subthreshold Swing and Hysteresis Trade-Off

From Fig. 26.6, we notice that although *SS* is reduced with increasing T_{FE}, at some critical value, T^*_{FE}, hysteresis in the I_D–V_{GS} characteristics appears. Thus, optimum design of NCFET must ensure that the *SS* reduction does not lead to excessive hysteresis. This undesirable feature arises when the total gate capacitance becomes negative, i.e., when $|C_{FE}|$ becomes smaller than C_{MOS}. During hysteretic operation, the ferroelectric starts switching between two stable states (indicated by the solid lines in Fig. 26.5) and skips the NC region. In this scenario, the *SS* might still be lower than 60 mV/dec but not due to the NC effect but rather to abrupt polarization switching [18]. It is important to avoid hysteresis in digital and, more importantly, in analog applications that would otherwise lead to larger power consumption and circuit overheads to manage the nonsymmetrical turn-on and turn-off characteristics. To summarize, maximization of A_V may lead to undesirable hysteresis; therefore, the design of a "well-tempered" NCFET must balance the two requirements of hysteresis-free and steep-slope operation.

Incidentally, we observe that a whole class of transistors called ferroelectric MOSFETs (FeFETs) using the same device structure as NCFETs [18] relies on hysteresis in the I_D–V_{GS} characteristics to enable a variety of applications. These include low-power and ultrafast nonvolatile memories, computing elements embedded with memory capability (suitable for the logic-in-memory paradigm), and cross-bar arrays for artificial neural networks [19]. Some of the possible circuit applications of FeFETs (as well as NCFETs) will be discussed more in detail in Sects. 26.4 and 26.5.

26.2.2 Tailoring Negative Capacitance by Energy Landscape Engineering

Let us now generalize the concept of NC operation to a wider range of devices. As discussed in the introduction, NCFETs belong to the family of devices called Landau FETs (or Landau switches) [8]. This class of devices achieves the $SS < 60$ mV/dec metric by reducing the body factor m below 1 (see Eq. (26.1)). The general behavior of Landau FETs can be understood in terms of their energy landscape, which determines the NC region as discussed in Sect. 26.2.1. The energy landscape for a NC system is expressed in Eq. (26.2), which is valid for any system that can switch between two stable states, such as a ferroelectric layer. Basically, an NCFET is a system that combines a positive capacitor with a negative capacitor so that the total energy U_{TOT} can be expressed by

$$U_{TOT} = \left(\alpha + \frac{1}{2\varepsilon}\right) P^2 + \beta P^4 + \gamma P^6 - E \times P. \tag{26.13}$$

The positive capacitor adds up the $1/(2\varepsilon) \times P^2$ term to the Gibb's free energy of the NC, making it possible to stabilize the NC region. The energy landscapes for a positive and negative capacitor are depicted in Fig. 26.8a, b, respectively. Unfortunately, the Landau coefficients are material-specific, and the higher-order terms, β and γ, make the body factor m, voltage gain A_V, and *SS* improvement bias-dependent making it more challenging, in turn, to reach the CMC condition with hysteresis-free operation for the whole V_{GS} range. In general, one could use various series combinations of NC layers in a Landau FET (such as FE, anti-ferroelectric layer (AFE), nano-electromechanical system (NEMS), each with their specific energy landscape) to tailor/flatten the total energy landscape so that CMC is reached for the entire bias range of interest [20, 21].

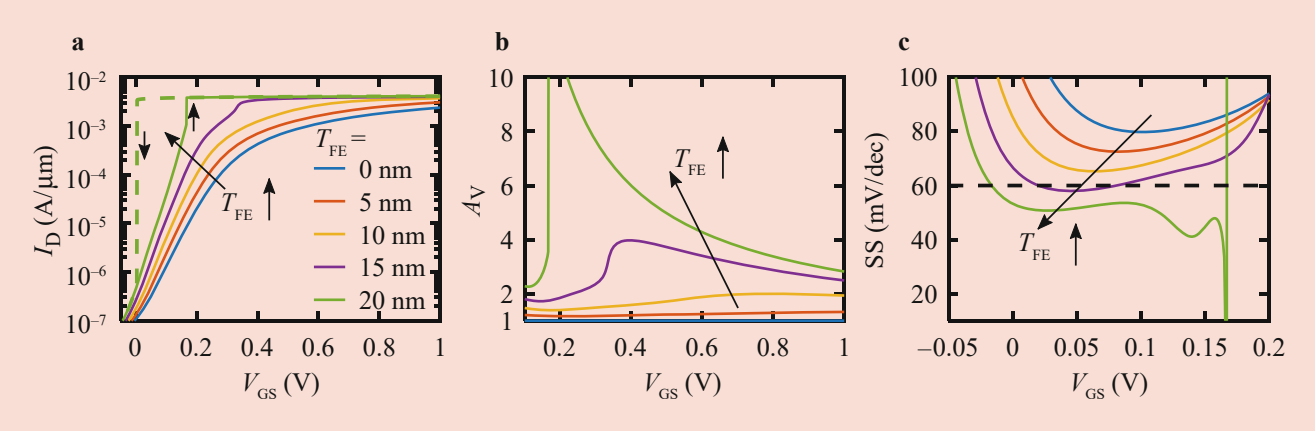

Fig. 26.6 (**a**) I_D–V_{GS} characteristic of a NCFET for different T_{FE} values (see legend). By increasing T_{FE}, (**b**) the voltage gain A_V is increased, and (**c**) at the same time the *SS* is reduced. When $|C_{FE}|$ becomes smaller than C_{MOS}, then the total gate capacitance becomes negative (i.e., unstable), and hysteresis starts to appear, as shown in panel (**a**)

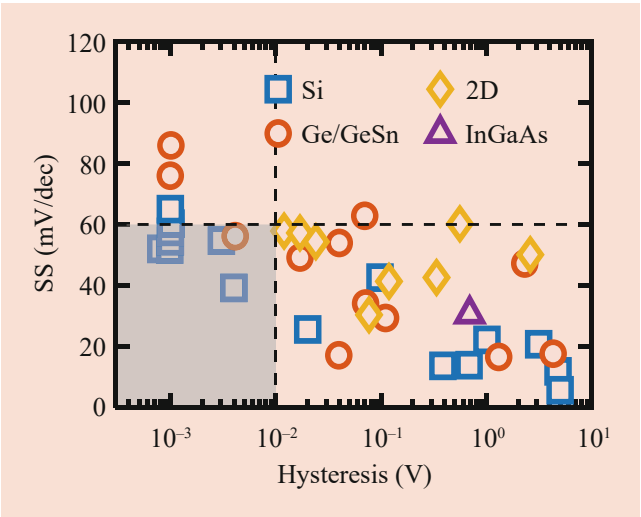

Fig. 26.7 Published experimental data of *SS* vs hysteresis for different NCFET technologies, i.e., Si, Ge/GeSn, 2D, and III–V semiconductors. The shaded area represents a "sweet spot" for an NCFET with $SS < 60$ mV/dec and moderate hysteresis. (Reproduced from [18], with permission from AIP Publishing)

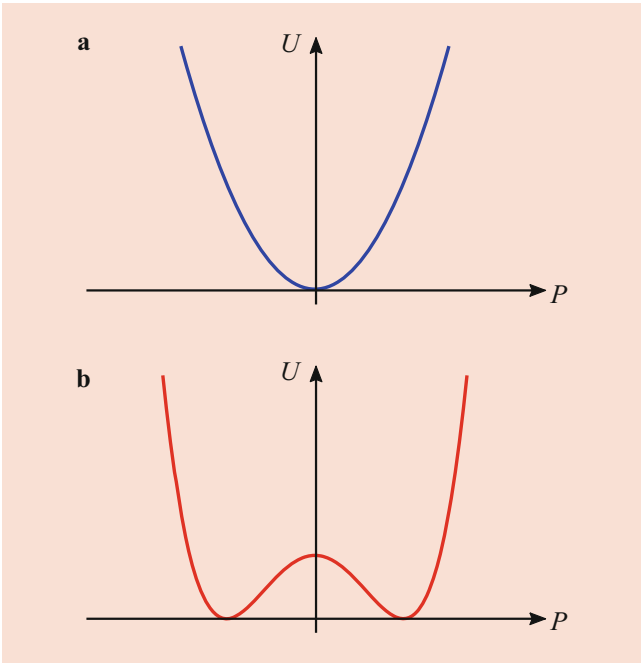

Fig. 26.8 Energy landscape plot, *U*–*P*, of (**a**) the classical positive capacitor and (**b**) the negative capacitor. The capacitance is proportional to $(\partial^2 U/\partial P^2)^{-1}$; thus, its sign is defined by the concavity (up, positive and down, negative) of the *U*–*P* plot

Prospects of Hysteresis-Free Abrupt Switching

In principle, it is possible to design Landau FETs exhibiting ideal $SS \approx 0$ mV/dec with no hysteresis [8]. This can be achieved by properly compensating for the energy barrier present in between the two wells of the energy landscape (see Fig. 26.8b). The extra energy component to compensate for the switching barrier can be provided by a nonlinear capacitor, as for example the depletion layer of a MOSFET. In this way, the intrinsic two-well energy landscape of an NC layer (be either an air gap in a SGFET or a ferroelectric in a NCFET) can be effectively flattened out, removing the switching barrier and eliminating hysteresis. In more realistic cases, however, where neither the semiconductor capacitance nor the negative capacitance is constant throughout the bias range, the *SS* cannot be arbitrarily reduced [20]. In fact, it can

be proved that depending on the particular Landau FET, there exists a minimum *SS* that is dictated by stability constraints to achieve hysteresis-free operation [20]. We conclude by observing that the theory developed in Sect. 26.2.1 can be extended to any kind of Landau FET to achieve optimum design in terms of *SS* and hysteresis.

26.2.3 Reliability Physics of NCFETs

Having discussed the general theory for NCFETs and Landau FETs, we move on with the discussion of the reliability issues of NCFETs. The reliability issues have not yet been systematically quantified [18]; thus, we will summarize the current understanding regarding the reliability issues of NCFETs in comparison with stand-alone MOSFETs:

1. Negative Bias Temperature Instability (NBTI). Negative bias temperature instability is a major reliability concern for traditional MOSFETs [22, 23]. It appears that NCFET suppresses NBTI as a consequence of two counterbalancing effects: First, the threshold voltage shift due to interface traps changes the internal potential of the transistor, thereby modifying the voltage amplification. Second, the charge balance requirement changes the range over which voltage amplification is achieved. Combined with parasitic gate-to-drain capacitance, these two effects are predicted to suppress NBTI degradation in modern Fin (or tri-gate) FETs [24].
2. Time-Dependent Dielectric Breakdown (TDDB). The amplification of internal potential induces higher fields in the oxide layer between the ferroelectric and semiconductor; thus, the TDDB reliability may be compromised if one wishes to increase drive current through voltage amplification [25]. Instead, one should design the NCFET and scale the voltage appropriately so that the interface field (and therefore I_{ON}) remains unchanged and TDDB robustness is preserved.
3. Hot Atom Damage (HAD). First analyzed for ferroelectric switching devices (such as FeFET), HAD is a novel reliability aspect of NCFETs that is associated with the polarization overshoots that might occur during switching [26]. HAD raises reliability concerns as it can lead to dielectric breakdown in FeFETs and Landau FETs. However, in NCFETs, HAD is intrinsically mitigated, thanks to the operating voltage being lower than the coercive voltage of the ferroelectric layer, which reduces the required switching energy [27].
4. Gate Leakage. The presence of a finite current discharging the negative capacitance in NCFET can destabilize the system and cause a loss of the *SS* improvement. Nevertheless, it has been suggested that for fast enough gate voltage cycles, i.e., higher than the time it takes for the leakage current to discharge all the capacitors, NCFETs can still show steep-switching operation [28].
5. Flicker Noise. Fluctuations in the number of traps and in the mobility are at the origin of the so-called flicker noise that, in turn, causes fluctuations in I_D [29]. Interestingly, NCFETs have been found to reduce flicker noise, thanks to enhanced effective gate capacitance [30], with a scaling trend of I_D power spectral density with increasing T_{FE}.

As a general remark, we observe that reliability issues in NCFETs (and Landau FETs) can be potentially mitigated by the fact that these devices reduce static and dynamic power consumption simultaneously, so that the same I_{ON} compared to a stand-alone MOSFET can be achieved at reduced V_{DD}. On the other hand, the fact that the internal potential between the ferroelectric and insulator layer has higher values than a normal MOSFET (due to voltage amplification) can lead to higher degradation in terms of TDDB, self-heating [31], and possibly also NBTI. Therefore, to ensure that NCFETs are able to meet requirements in terms of reliability, it is of paramount importance to properly design these transistors trading off the reduction of *SS* with adequate lifetime.

26.2.4 Advanced Issues

We conclude the discussion on NCFETs by outlining the advanced issues related with the technology that are yet to be fully solved or that are still debated in the community. Given the relatively recent proposal of the NCFET, it is natural that fundamental theoretical aspects and valid experimental demonstrations are still under debate. We will briefly summarize these aspects, with the goal of addressing the most pressing questions that require further investigation to consolidate the NCFET technology.

Single- vs Multi-domain Models

The analysis of NCFETs in Sect. 26.2.1 relied on the tacit assumption that the polarization is uniform across the ferroelectric layer [7]. This simplified picture derives from the adoption of the phenomenological Landau theory, neglecting the microscopic details of a ferroelectric layer. In general, a ferroelectric has multiple domains each associated with its polarization state (in the simplest case, either positive or negative) leading to an overall nonuniform polarization across the layer [32]. The models describing the spatial dependence of the polarization belong to the "multi-domain" models class compared to the "single-domain" one [18]. There are several practical implications of the nonuniform polarization. For example, it can lead to reduced [32] as well as complete loss of NC operation [33]. Further exploration of multi-domain aspects of ferroelectric layer in the NCFET is thus required to harness the negative capacitance behavior and to build

up predictive models to quantitatively characterize realistic NCFETs [34].

Quasi-Static vs Dynamic NC Operation
The steady-state analysis of NCFET in Sect. 26.2.1 neglected the dynamical effects (recall that $\rho dP/dt = 0$). However, NCFET operation (in terms of steep subthreshold switching) can also be interpreted with other models that rely on dynamic effects to explain the decrease of ferroelectric voltage with increasing applied bias. For example, in [35], the NC effect was attributed to the increase of the slope of the *P–V* characteristic near the coercive field and to the polarization lag occurring during electric field AC sweeps. Thus, in [35], the internal voltage gain was explained with the Miller theory, which did not require the ferroelectric capacitance to be negative. Besides [35], there are other works that provide alternative interpretation of the voltage amplification behavior observed in ferroelectric-dielectric (FE-DE) stacks, as summarized in [18]. In the presence of different theories for the NC effect, a single model would need to prove self-consistently a whole set of feature characteristics of these devices to convincingly explain NCFET operation.

Experimental Results on NCFETs
Ever since the seminal paper by Salahuddin and Datta in 2008 [7], researchers have come up with experimental demonstrations of the NCFET concept, either on perovskite or doped-HfO_2 ferroelectrics or on a variety of different substrates [18]. However, published data have shown hitherto a relatively broad scatter of the measured *SS* values, especially related to hysteresis. This scenario is shown in Fig. 26.7, where experimental data of NCFET realized in different device technologies (i.e., Si, Ge/GeSn, 2D, III–V semiconductors) is compared. This level of scatter is a clear indication of the relatively limited maturity of the technology and needs to be reduced in order to guarantee the adoption of NCFETs into mainstream semiconductor industry.

NCFET Models for Advanced Transistor Architectures and Technologies
While in Sect. 26.2.1 we focused the analysis on long-channel bulk MOSFETs, the NCFET concept can be applied also to other transistor technologies. Indeed, there are several attempts in the literature to couple the LKE with electrostatic and transport equations to find self-consistently the solution to advanced transistor architectures and technologies. Some examples of such modeling efforts are *(i)* dual (or double)-gate FET (DGFET) [36], *(ii)* FinFET [37], *(iii)* gate-all-around FET (GAAFET) [38, 39], and *(iv)* MoS_2 junctionless FET (JLFET) [40]. The interest in developing models for advanced transistor technologies is motivated by the scaling needs of the semiconductor industry, which require the reduction of the so-called short-channel effects as well as reduction in operating power. Indeed, NCFETs can prove instrumental in achieving these goals, provided that their distinctive features are verified in realistic devices, as discussed in the next paragraph.

Requirements to Prove the NCFET Concept
The interpretation of experimental demonstrations of NCFETs is further complicated by the debate around the theoretical aspects of the NC effect as derived from the Landau theory, as well as by the presence of other possible models explaining the observed reduction of *SS*. To unambiguously prove the NCFET concept on fabricated devices, it is not only necessary to demonstrate that *SS* is effectively reduced, but also a number of other features must be guaranteed. The necessary features to prove self-consistently the NCFET operation are [18] the following:

- Hysteresis-free steep subthreshold switching with $SS < 60$ mV/dec.
- Negative differential resistance (NDR) in the output characteristics, i.e., the reduction of I_D with increasing V_{DS}.
- Negative drain-induced barrier lowering (NDIBL), i.e., the increase in threshold voltage with increasing V_{DS}.
- Suppression of the $1/f$ flicker noise measured in I_D.

The features outlined above (e.g., NDR, NDIBL, etc.) should be proven for a combination of dielectric and ferroelectric thicknesses, for different bias sweeps, and also for a range of frequencies (to determine the speed limits of the technology). These requirements provide an operative procedure to conduct experiments to systematically prove NCFET operation.

26.3 Device Physics of PhaseFETs

In the Introduction, we mentioned that PhaseFET is a non-thermionic device that allows steep-slope switching by focusing on the channel transport and reducing channel transport factor, *n*, below 60 mV/dec. PhaseFETs are composed of the series of a MOSFET and a nonlinear variable resistor connected to the source, as sketched in Fig. 26.9a. Less commonly, some devices connect the variable resistor (also called threshold selector (TS)) to the drain, as in [41]. The variable resistor connected in series to the MOSFET is realized with a PTM that shows an abrupt switching between two stable low- and high-resistance states. Some examples of PTM are vanadium dioxide (VO_2) [5] or Ag/TiO_2 [41]. In general, the phase transition involves insulator-to-metal transition (IMT) and metal-to-insulator transition (MIT) as a response to an external stimulus (i.e., temperature, pressure, electric field), and this leads to sharp transitions in the current-voltage

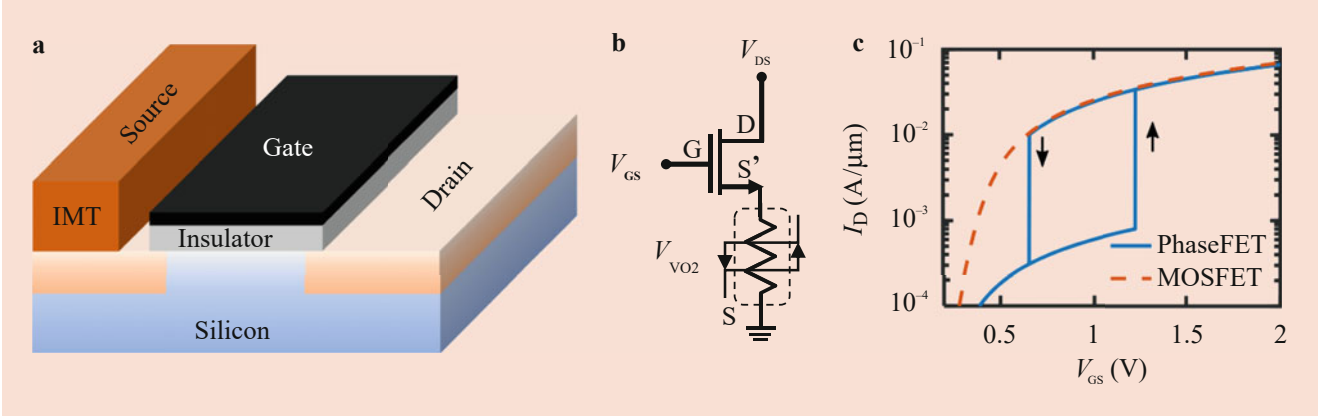

Fig. 26.9 (**a**) Sketch of the PhaseFET cross-section, which consists of an MOSFET with in series to the source a variable resistor undergoing phase transition (PTM). (**b**) Circuit schematic of the PhaseFET and (**c**) its I_D–V_{GS} characteristic (blue solid line) compared to that of the standard MOSFET (orange dashed line). The PhaseFET has much better subthreshold swing than the MOSFET though it exhibits hysteresis

characteristics of the device. The corresponding transition between on and off operation leads to steep *SS* switching.

Compared to other options (e.g., tunnel FET or MEM relay), a PhaseFET may be easier to integrate into an existing MOSFET process flow because the phase-changing element can be embedded among the interconnects within the back end. In this section, we discuss more in detail the physics of phase transition and describe the general framework of operation of the PhaseFET. The theory of PhaseFET is not as well developed as for TFETs or Landau FETs. Hence, we focus on two simple approaches (i.e., behavioral compact model and electrothermal phenomenological model) to provide a general understanding of the potential of PhaseFET-based circuits.

26.3.1 Behavioral Compact Model

To understand the operation of the PhaseFET, we can employ a simple behavioral model that captures the abrupt resistivity change in a general way and that can be coupled to a MOSFET model to obtain a self-consistent solution of the drain current vs gate-to-source voltage. The behavioral model assumes that the high- to low-resistive switching occurs at a threshold voltage, V_1, while the high-to-low switching occurs at a second threshold, V_2 [42]. Since $V_2 < V_1$, the device traces different current-voltage paths depending on the direction of voltage sweep, resulting in hysteretic switching in response to an off-on-off input pulse. This is illustrated in Fig. 26.9, where the simple circuit shown in panel (b) is simulated to obtain the I_D–V_{GS} characteristic shown in panel (c). The characteristics of PhaseFET compared to the standalone MOSFET are much steeper during turn-on and turn-off; however, hysteresis is present, as mentioned previously. In this regard, both NCFET and PhaseFET must balance clear advantage of *SS* reduction against the hysteresis inherent in the transition. We note that while an NCFET can be designed to be essentially hysteresis-free, it is difficult to completely eliminate the hysteresis in PhaseFETs. This has to do with the physics of abrupt resistive switching that inherently occurs at different thresholds depending on the previous state of the device. Nevertheless, appropriate material choice [43] can reduce the PhaseFET hysteresis to a level tolerable for a given application.

26.3.2 Physics-Based Phenomenological Model

The PhaseFET behavioral model explains device operation empirically, but it does not allow to connect the abrupt resistance change to the physical mechanism inducing phase transition (i.e., either electrical or temperature switching). An improved phenomenological PTM model should self-consistently solve for the electrical and thermal behaviors of the PhaseFET. This would allow phase transition through Joule heating in the VO_2. The abrupt resistance variation can be captured by an empirical model [44, 45]:

$$R_{PTM} = R_{LRS} + \frac{(R_{HRS} - R_{LRS})}{1 + \exp\left[(T - T_c)/T_x\right]} \tag{26.14}$$

where R_{LRS} (R_{HRS}) is the low (high)-resistance state value, T_c is the critical temperature at which transition occurs, and T_x is an empirical parameter. The temperature variation is determined by the following first-order differential equation:

$$C_{th}\frac{dT}{dt} = V_{PTM} \times I_{PTM} - \frac{T - T_0}{R_{th}} \tag{26.15}$$

where C_{th} (R_{th}) is the thermal capacitance (resistance), T_0 is the ambient temperature, and V_{PTM} (I_{PTM}) is the voltage across (current flowing in) the PTM. Notice that this equation connects the Joule heating term $V \times I$ and the thermal properties of the device, i.e., C_{th} and R_{th}.

Although this modeling approach might be good enough for circuit simulations, it is still not adequate for realistic physics-based modeling, for which the resistivity variation needs to be connected to the material properties and more fundamental theories. One possible way of to accomplish this is to rely on MottFET theory, which provides a theoretical framework to explain phase transition [6]. Materials like VO_2, in fact, belong to the class of Mott insulators, which exhibit an abrupt (but reversible) IMT when the internal temperature exceeds a critical value, T_c [6]. Although the MottFET, employing a PTM as the channel of the transistor, has not been demonstrated yet, understanding the details behind PTM in Mott insulators is instructive to harness the interesting physics associated with phase transition.

The MottFET theory allows us to model the IMT/MIT with bandgap, E_G, and thermal conductivity, κ, variations. As temperature varies in a PTM, the bandgap is modified through the following relation [6]:

$$E_G = E_{G,0} - \frac{E_{G,0}}{1 + a \exp\left[-b\left(T - T_c\right)\right]} \tag{26.16}$$

where a and b are intrinsic material parameters specific to the Mott insulator. Associated with the bandgap collapse, which determines the electrical behavior, is the variation in thermal conductivity which effectively controls the thermal behavior:

$$\kappa = \kappa_0 + \frac{(\kappa_1 - \kappa_0)}{1 + a \exp\left[-b\left(T - T_c\right)\right]} \tag{26.17}$$

where κ_0 (κ_1) is the thermal conductivity of the insulator (metal) phase, respectively. This approach of modeling bandgap and thermal conductivity variations allows for an accurate description of the observed temperature dependence of carrier concentration and resistivity, enabling predictive analysis for a variety of novel devices based on Mott insulators [6].

26.3.3 Experimental Results on PhaseFETs

Similarly to Fig. 26.7 for NCFETs, we summarize in Fig. 26.10 the data of fabricated PhaseFETs present in the literature [5, 11, 41, 46–50]. The measured data for PhaseFETs also shows a relatively broad scatter of *SS* vs hysteresis values. We note that *SS* for PhaseFET is much lower than that of NCFETs: in fact, PhaseFETs have almost ideal on-off switching, i.e., $SS \sim 0$ mV/dec. On the other hand, hysteresis is generally much larger in PhaseFETs than NCFETs (always higher than 100 mV). Thus, once again, the technology choice for a given application must be based on the trade-off between *SS* and hysteresis.

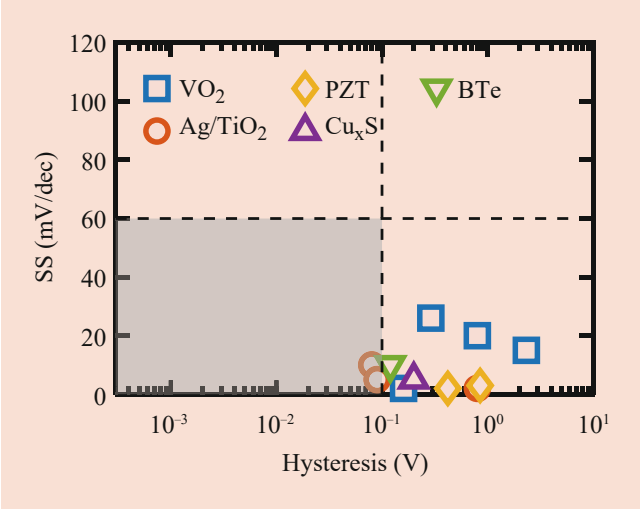

Fig. 26.10 Published data of various PhaseFET experimental data of *SS* vs hysteresis for different variable resistance materials, i.e., VO_2 [5, 11], Ag/TiO_2 [41, 46], PZT [47, 48], Cu_xS [49], and BTe [50]. The shaded area represents a "sweet spot" for a PhaseFET with $SS < 60$ mV/dec and moderate hysteresis

26.4 Boolean Computing with NCFETs, FeFETs, and PhaseFETs

With the understanding of the device operation of NCFETs and PhaseFETs, we now present their circuit implications. To complete the picture on the applications of FE-based devices, we will also discuss FeFET-based circuits which utilize the hysteretic characteristics as opposed to NCFETs that utilize steep-switching. In this section, we will focus on applications targeted toward Boolean computing in the context of both digital logic and memories. In Sect. 26.5, we will discuss the potential of using such new technologies for non-Boolean computing.

26.4.1 Logic Design

In the context of the design of digital logic primitives, NCFETs and PhaseFETs exhibit promising characteristics such as steep-switching (either due to NC effect or abrupt hysteretic switching, respectively) and therefore can potentially enable aggressive voltage scaling. The question, however, is whether or not these devices can be or should be

used as drop-in replacements of standard transistors or if new design techniques will be needed to translate the device-level benefits to optimal circuit performance. Here, we will address this question and highlight the importance of technology-circuit co-design to enable NCFET- and PhaseFET-based low-power logic. We will discuss the circuit behavior both from the perspectives of DC voltage transfer characteristics (VTC) (which dictates the gain and noise margins of the logic gates) and transient response (which determines the energy efficiency and speed).

NCFET-Based Logic

Logic gate implementation prefers non-hysteretic NCFET operation to avert polarization switching (and the associated delay/energy overheads) as well as to simplify the design of logic gates (since NCFETs can be directly used as drop-in replacements of MOSFETs). Hence, in this section, the focus of our discussion will be on logic design with non-hysteretic NCFETs.

The very NC effect that gives rise to steep-switching in NCFETs also leads to a concomitant increase in their gate capacitance [51]. Thus, for digital logic, the benefits of higher on current at iso-off current (due to steep-switching) may be offset by the increase in the fanout (gate) capacitance. Also, the viscosity coefficient of the ferroelectric, ρ, may affect circuit delay [51]. In addition, the steep-switching in NCFETs is often accompanied by NDR in the output characteristics [51, 52]. Here, we will discuss the overall effect of such unique NCFET properties on circuit behavior.

From the perspective of the DC response, steep-switching in NCFETs leads to sharper VTCs compared to complementary metal oxide semiconductor (CMOS) circuits, which implies higher gain and improved noise margins [51]. However, the story does not end here. NDR in NCFETs leads to some unique VTC attributes, especially at sufficiently large ferroelectric thickness. Specifically, the VTC becomes hysteretic due to NDR (Fig. 26.11a (see [51] for more details), even though the device is non-hysteretic. This leads to improved noise margins for Boolean applications. This unique feature can be used to design oscillators, as discussed later in Sect. 26.5.1.

Let us now come to the energy-delay analysis of NCFET-based logic. Here, we need to consider the interplay between higher on-off current ratios and larger gate capacitance (compared to CMOS) as well as the viscosity coefficient of the ferroelectric layer, ρ. While the viscosity coefficient still needs further characterization, recent experiments have indicated that ρ may be as low as 0.18 Ω.cm [53]. Nevertheless, here (in Fig. 26.11b adapted from [51]), we show the characteristics for different values of ρ to illustrate its effect. It can be observed that NCFETs show lower delay at iso-energy compared to CMOS circuits in the low-voltage regime due to higher on current. At high voltages, however, the delay associated with charging/discharging of the circuit nodes is small, and thus, the relative contribution of ρ to the overall circuit delay increases [51]. As a result, NCFET-based logic can show delay increase for large ρ. However, if ρ can be reduced, the benefits of NCFETs can be extended to a larger voltage range. In addition, NCFET circuits show higher energy-delay improvements over CMOS with the increase in the contribution of wire (back-end load) to the overall load. This is because large wire capacitance mitigates the effect of higher gate capacitance of NCFETs [51].

We will end this section by emphasizing that to maximize the benefits of NCFETs, design of devices (e.g., T_{FE} optimization) needs to be coupled with circuit design (e.g., voltage optimization, back-end and front-end fanout, etc.). With proper design, NCFET-based circuits exhibit performance benefits, especially at low voltages. Further, their unique NDR characteristics can lead to Schmitt trigger action in NCFET-based logic gates, which can be beneficial for noise immunity.

PhaseFET-Based Logic

Similar to NCFETs, PhaseFETs offer steep (in fact, abrupt) switching, which can potentially be beneficial for logic design. However, one important distinction is that unlike NCFETs, PhaseFETs cannot have non-hysteretic characteristics [43]. (The only exception to this is a very specific design point where the gate voltage associated with IMT and MIT can theoretically be matched by design; however, such a design would be impractical as a small variation can lead to the phase transition material going into the oscillatory mode [54], which is detrimental for logic operation). With hysteretic and abrupt transfer and output characteristics of PhaseFETs, logic design becomes nontrivial [55].

In order to obtain proper functionality and performance gains, the resistance ratio of the insulating and metallic state of the PTMs can neither be too high (in which case, the devices and circuits will fail to function) nor too low (in which case, PhaseFETs will not show any improvement in the on-off current ratio [43]). Moreover, the transition voltages associated with IMT and MIT need to be tailored by proper device-circuit co-design to ensure that the phase transitions in the PTM enable the required circuit functionality (for instance, complete voltage swing in the logic gates [55]).

The VTC of properly designed PhaseFET-based logic gates (obtained from DC characteristics – Fig. 26.12a) is quite unconventional, showing hysteresis in the non-transition region (which is a result of the intrinsic device hysteresis). VTCs also indicate an "apparent" reduction in the noise margins [43] due to the high insulating state

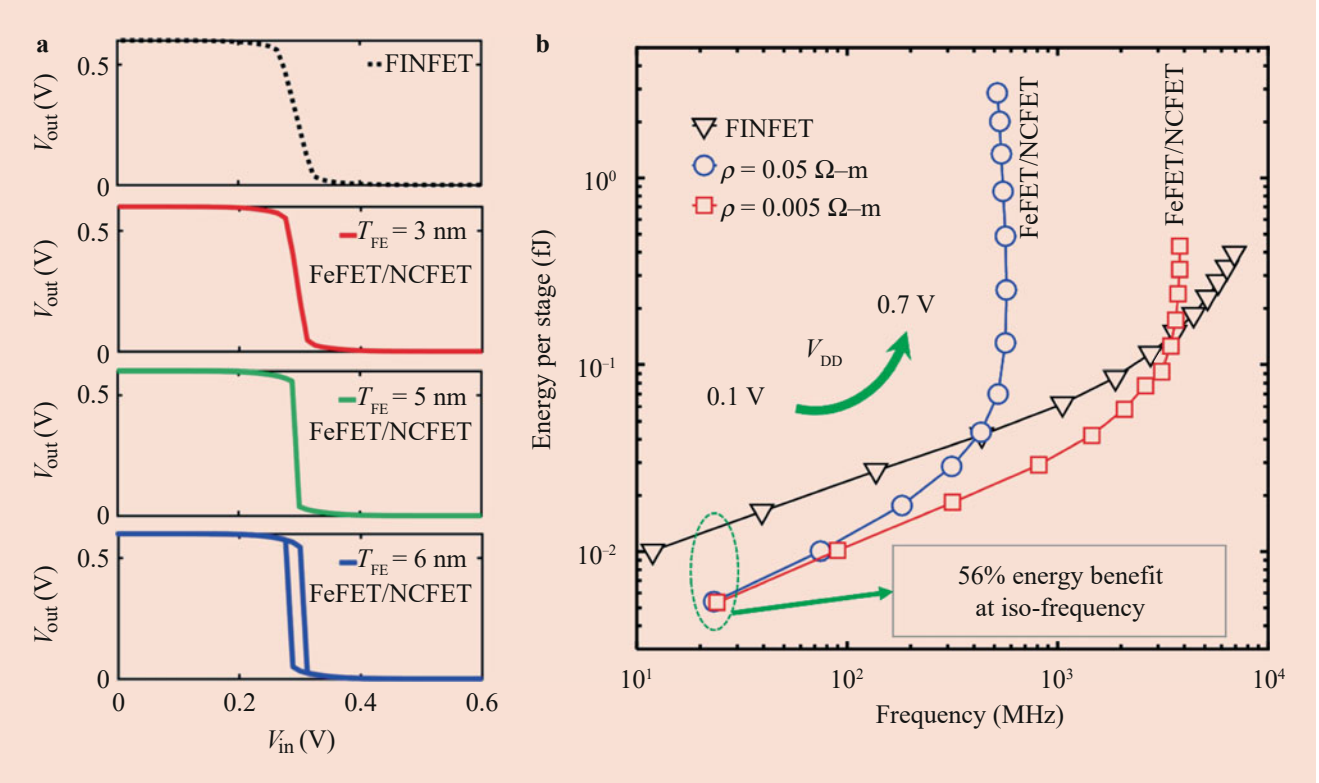

Fig. 26.11 (**a**) Voltage transfer characteristics (VTC) of NCFET inverter for different FE thickness, T_{FE}. (From [51] © 2017 IEEE). (**b**) Energy delay for NCFET-based ring oscillator for different ρ

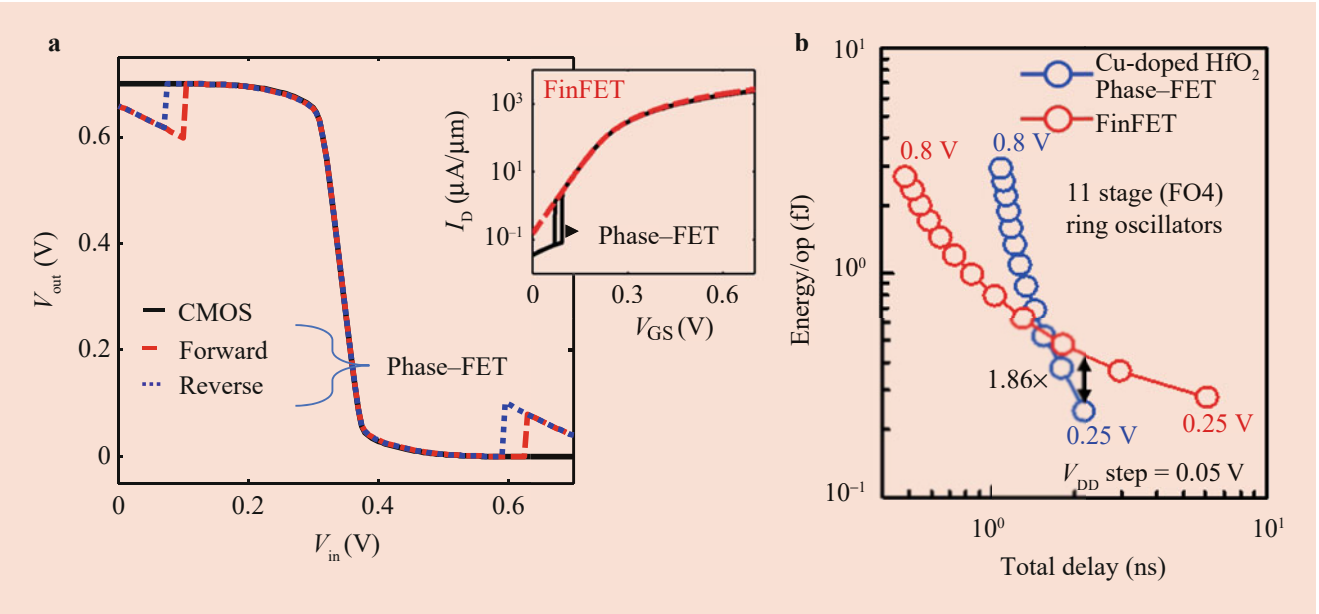

Fig. 26.12 (**a**) Voltage transfer characteristics (VTC) of PhaseFET-based inverter. (**b**) Energy delay of PhaseFET-based 11-stage ring oscillators. (From [55] © 2017 IEEE)

resistance of the PTMs in the pull-up and pull-down paths. However, this effect is not as severe as predicted by the DC characteristics, and the dynamic change in the resistance of the PTMs during the circuit operation due to IMT significantly improves the noise margins by establishing a low-resistance path to either V_{DD} or ground [55].

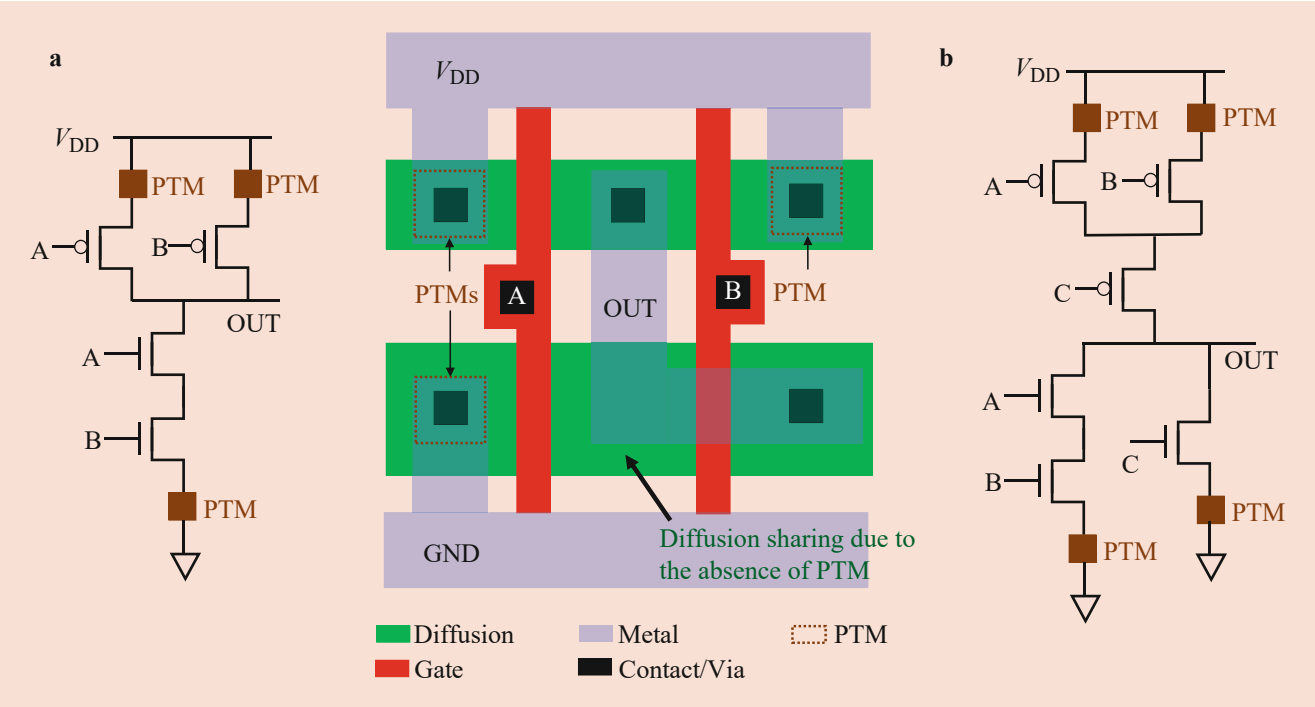

Fig. 26.13 (**a**) Schematic and layout of PhaseFET-based two-input NAND gate and (**b**) schematic of PhaseFET-based AND-OR-INVERT (AOI) gate, showing one PTM per network of series-connected transistors in the pull-up and pull-down paths

The energy-delay analysis of PhaseFETs (see Fig. 26.12b [55]) shows that PhaseFETs exhibit delay reduction at iso-energy at low voltages (similar to NCFETs) by virtue of their steep-switching and higher on-off current ratio. At high voltages, however, the transition time associated with IMT and MIT degrades the performance of PhaseFETs. Hence, novel PTMs may need to be explored that not only meet the resistance and transition voltage requirements to support the logic gate functionalities but also exhibit low transition times and high stability to enhance the benefits of PhaseFET-based logic at high operating voltages as well.

It is noteworthy that for multiple input gates, it may not be judicious to use PhaseFETs as drop-in replacements of standard MOSFETs (unlike for NCFETs). Instead, only one PTM is needed for a set of series-connected transistors in a logic gate [55]. For instance, a two-input NOT-AND (NAND) gate is shown in Fig. 26.13a. This design employs two parallel PhaseFETs in the pull-up network (PUN), but instead of using two series PhaseFETs in the pull-down network (PDN), a single PTM is placed in series with the n-type transistors. This design has the following advantages: (1) by avoiding two series PTMs, the effect of the metallic resistance of the PTM on the logic gate speed is reduced; (2) diffusion/contact-sharing between the two series n-transistors (as in standard CMOS) becomes possible, thereby averting area penalty due to PTMs (Fig. 26.13a); and (3) the regulation of IMT/MIT of a single PTM and its interactions with the network of series-connected transistors becomes easier (compared to two PTMs in series), which makes the design more robust to variations. Note, similar to an inverter, the width of the series-connected transistors and the PTM geometry need to be co-optimized, to achieve the correct functionality of the gate, sufficient noise margins, complete voltage swing, and energy-delay benefits. The idea of using a single PTM per series network of transistors can be easily extended to other complex gates. For instance, an AND-OR-INVERT (AOI) gate based on PhaseFETs is shown in Fig. 26.13b.

26.4.2 SRAM Design

Similar to the logic design, the implementation of static random access memories (SRAMs) with NCFETs and PhaseFETs requires careful co-design of devices and circuits to harness the maximum benefits. In fact, the importance of utilizing the unique attributes of the devices becomes even more critical in SRAMs because of the self-conflicting design requirements for read and write. In this section, we briefly review NCFET- and PhaseFET-based six-transistor SRAMs (6 T-SRAMs).

NCFET-Based SRAM

NCFETs, in their non-hysteretic mode, can be used as drop-in replacements of MOSFETs in a 6 T-SRAM cell (Fig. 26.14a).

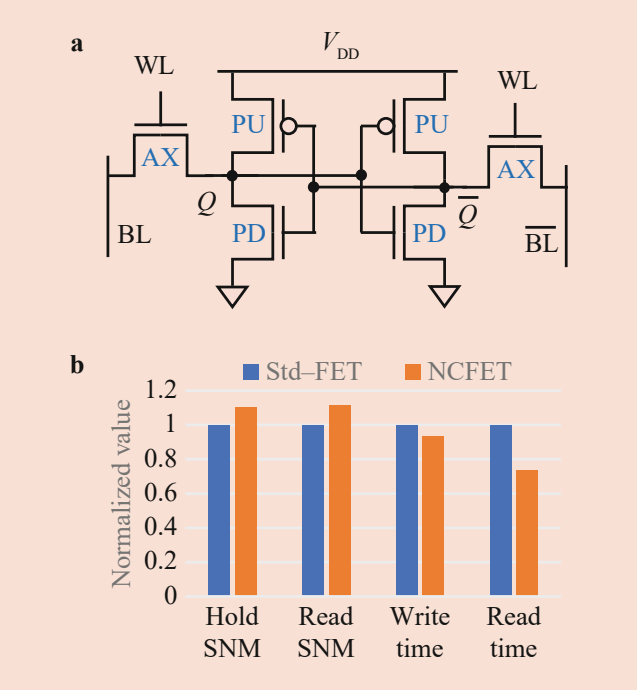

Fig. 26.14 (**a**) SRAM cell showing pull-up (PU), pull-down (PD), and access (AX) transistors. (**b**) Comparison of performances (read time and write time) and stability (hold SNM and read SNM) between Std-FET-based and NCFET-based SRAM cell. (From [56] © 2016 IEEE)

By virtue of their steep-switching, NCFETs naturally offer higher read and hold stabilities (Fig. 26.14b) [56]. However, by utilizing the NDR in their output characteristics (with proper optimization of T_{FE}), Schmitt trigger action (or hysteretic response in their DC characteristics) is achieved, which further improves the read and holds noise margins [57]. Furthermore, access time of NCFET-based SRAMs at iso-leakage and iso-area is lower due to higher I_{ON}. The overhead of higher gate capacitance in NCFETs is significantly mitigated due to the wire capacitance associated with word lines and bit lines. The write time of NCFET-based SRAMs is strongly dependent on ρ: for ρ close to 0.18 Ω.cm [53], write time improvement is observed, mainly due to higher I_{ON} in NCFETs. However, increase in ρ lessens these benefits and may even degrade write time [56]. Hence, proper device design coupled with cell optimization (including the possible use of read/write assist techniques) is needed in NCFET-based SRAMs to mitigate the design conflicts and achieve superior design solutions compared to their CMOS counterparts.

PhaseFET-Based SRAM

Unlike NCFETs, employing PhaseFETs as drop-in replacements in 6 T-SRAMs may yield a suboptimal design. As an example, the additional resistance given by the PTM in the access PhaseFET in 6 T-SRAMs may reduce the cell leakage and bit-line leakage but can lead to a significant degradation in the write-ability and read speed. Similarly, if both the pull-up and pull-down transistors of 6 T-SRAM are implemented using PhaseFETs, the stability of the cell (especially during read) may be degraded considering process variations. Therefore, it becomes important to selectively employ PhaseFETs in conjunction with standard transistors in SRAMs to utilize their unique properties (such as abrupt switching) for mitigating the read-write conflicts.

In [58], it is shown that using PhaseFETs as the pull-down transistors while using MOSFETs as pull-up and access transistors can be beneficial to simultaneously increase the read stability, hold stability, and write-ability without any increase in the area, albeit at the cost of the access time. The key idea is as follows. During read, the cell is designed to trigger IMT in the PTM of the PhaseFET driving the node storing "0" so that read current can flow. On the other hand, the other PTM remains insulating, which increases the trip point (or logic threshold voltage) of the corresponding inverter in the SRAM cell. This significantly improves the read stability. During write, two scenarios can occur depending on the design: either (1) the PTM driving node storing "0" undergoes IMT followed by MIT, while the other PTM remains insulating, or (2) both PTMs remain insulating. Irrespective of which case occurs, write-ability is significantly improved due to insulating PTMs. Thus, by triggering operation-driven phase transitions in the PTM, the read-write conflicts present in standard SRAMs can be mitigated. For the details of this design and other related aspects (such as hold stability, area, the impact on the unaccessed cells, etc.), the reader is referred to [58].

In addition to the 6 T-SRAMs, PTMs have also been shown to improve the read functionality in SRAMs and dynamic random access memory (DRAMs) with separate read-write paths at a minimal area cost [59]. Besides, PTMs have also been used as a technology assist to design nonvolatile SRAMs [60].

26.4.3 Nonvolatile Memory Design

In the following, we discuss the design of novel nonvolatile memory (NVM) technologies based on FeFET and PhaseFET and the specific constraints introduced by the integration of either the ferroelectric or PTM layer with conventional devices.

FeFET-Based NVMs

FE materials have been widely accepted as an attractive storage element for nonvolatile memories. Therefore, in addition to the applications of FE in NCFET-based logic/SRAM designs, we consider it is important to briefly review the applications of FeFETs in NVM designs.

Traditionally, NVMs based on FE capacitor RAMs (FeRAMs) have been among the most promising technologies and have been implemented in industry using their unique property of polarization retention in the absence of an external electric field [61]. They offer high endurance along with high integration densities close to DRAMs. However, they suffer from low read distinguishability. Moreover, their read operation is destructive and requires a write-back operation, leading to large energy overheads [62].

More recently, the possibility of direct integration of FE layer in the gate stack of MOSFETs, as schematically depicted in Fig. 26.15a, has led to the realization of nonvolatile FeFETs [63]. Moreover, the HfO_2-based FE enables a scalable (and CMOS-compatible) emerging NVM that keeps up the pace with the scaling demands of leading-edge logic technologies [63]. In this memory device, the binary states are encoded in the form of the FE polarization (P). The direction (and value) of P determines the resistance state, either low-resistive state (LRS) or high-resistive state (HRS), of the underlying transistor [64] (see Fig. 26.15b). For storing the memory state in the FE layer (and to switch between LRS and HRS), a V_{GS} of appropriate polarity and value greater than the coercive voltage of the FE is applied. To sense the memory state, I_D of the FeFET is used, thus separating the read and write paths. Moreover, the read operation (in FeFETs with MFIS gate stack – see Fig. 26.2a) is no longer destructive, and the distinguishability is significantly improved by virtue of the gain of the transistor coupled with polarization switching [64].

Although FeFETs are immensely promising due to their electric field-driven write, read-write path separation, and CMOS compatibility of HfO_2-based ferroelectrics, the variability associated with the domain nucleation and propagation as well as traps in FeFETs (especially with MFIS gate stack [65]) needs to be tackled. FeFETs with MFMIS mitigate these issues and other challenges related to hysteresis optimization [66]. However, gate leakage can adversely affect such devices, resulting in the need for more advanced read schemes, which may incur in energy overheads [67].

For FeFETs with dominant single-domain behavior, especially for MFMIS gate stacks [68] or those at highly scaled technology nodes, the design of NVM arrays is fairly distinct compared to FeFETs with explicit multi-domain characteristics [66]. Here, we will briefly review both.

For the former category, various designs spanning highly compact 1T NVM to a more robust 4 T NVM have been explored, as shown in Fig. 26.16 [62, 69–71]. To design the NVM arrays, selective access of the FeFET NVM cells needs to be facilitated. In the 1T design [69], this is achieved by utilizing the drain coupling with the ferroelectric layer in the FeFET. While highly compact, the design margins of this cell need further exploration. Other designs [62, 70, 71] achieve

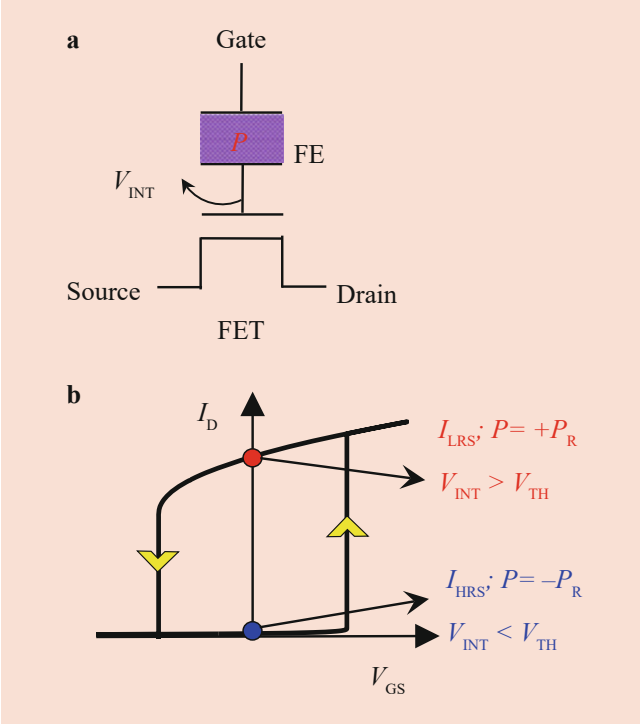

Fig. 26.15 (**a**) Schematic of FeFET with FE integrated in the gate stack of a FET. (**b**) I_D–V_{GS} characteristics of FeFET illustrating the bistability of polarization, P at $V_{GS} = 0$ V

selective access in the array by employing access transistors. In all these designs, a write access CMOS transistor is required to isolate the write paths of the unaccessed cells from that of the accessed cell. In the 2T (one MOSFET and one FeFET) design proposed in [62], an unconventional read scheme is adopted to minimize the flow of the read current through the unaccessed cell. To circumvent the overheads of the complex read scheme, 3T (two MOSFETs and one FeFET) design uses a read access transistor, albeit at the cost of area. The write operation of 1T, 2T, and 3T designs needs both positive and negative voltages [69, 62, 70]. To avert the use of negative write voltages (thereby, reducing the associated energy overheads), 4T (three MOSFETs and one FeFET) design [71] uses a third-access transistor. The other design option for all-positive write voltages is to use a two-phase write operation, as explored in [72]. The features common to all designs include (a) the application of write voltages on bit lines so that positive or negative V_{GS} greater than the coercive gate voltage appears across the FeFET of the accessed cell and (b) the application of read voltages on the sense lines to facilitate drain current flow through the accessed transistor, which can then be sensed by the sense amplifier.

Recently, multi-domain FeFETs (MD-FeFET) (with MFIS gate stack) have been explored for memory applications [66]. Their unique characteristics of polarization-

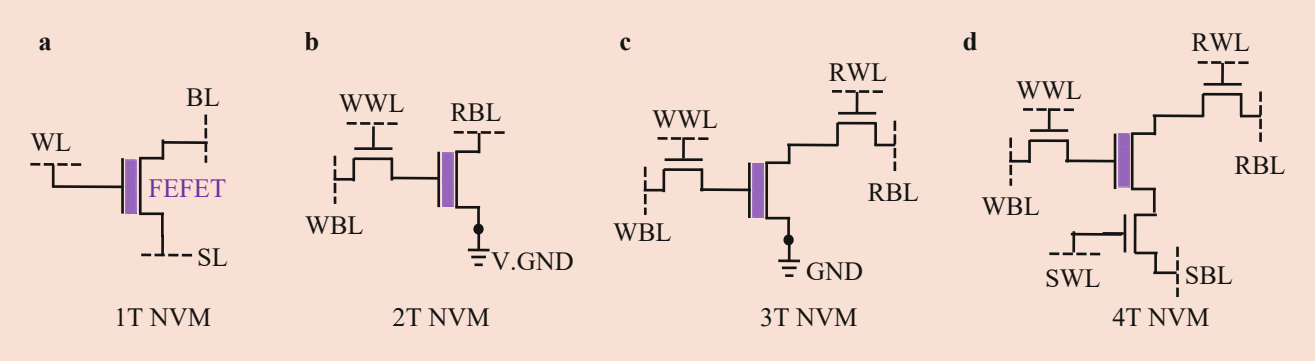

Fig. 26.16 (**a**) 1T, (**b**) 2T, (**c**) 3T, and (**d**) 4T FeFET-based nonvolatile memory (NVM) designs

dependent threshold voltage shifting (similar to NAND flash memories) have enabled the possibility of an ultrahigh-density 1T FeFET NVM [66]. Moreover, the same multi-domain characteristics have also been extensively proposed for multilevel memory cells as synapses in neuromorphic applications [73], as we will discuss later. However, the scalability of multi-domain ferroelectrics needs further exploration, and the techniques to engineer the domain sizes and distributions can potentially pave the path for MD-FeFET-based NVM designs.

In addition to standard memories, FeFETs have been utilized to design content-addressable memories (CAMs) showing promise of high-energy efficiency [74]. In addition, novel device structures such as reconfigurable FeFETs (R-FeFETs) have been proposed that dynamically change their operation between nonvolatile and volatile modes. These devices lower the power consumption of NVMs, mitigate the issues associated with gate leakage [75], and achieve differential memory designs [76]. In addition, the run-time modulation of hysteresis in R-FeFETs enables efficient logic-memory coupling for new applications such as logic in memory [76] as well as memory in logic [77].

PhaseFET-Augmented MRAMs

Unlike FEs in FeFETs, PTMs employed for the design of PhaseFETs do not offer nonvolatile characteristics. Hence, they cannot be directly utilized to design NVMs. However, by virtue of the large resistance ratio between their insulating and metallic states, PhaseFETs can be harnessed to augment the design of NVMs that inherently have low distinguishability (such as spin-based memories [78]). In [79], magnetic random access memories (MRAMs) have been designed with PhaseFETs (Fig. 26.17a, b) by coupling the nonvolatility of magnetic tunnel junction (MTJ) memories with the high ratio of insulating resistance and metallic resistance of the PTMs. The key idea behind MRAMs is to trigger operation-driven phase transitions in the PTM depending on the data stored in the MTJ. During the hold operation, the PTM remains in the insulating state. During the write operation, the PTM operates in its metallic state by design. This minimizes the adverse effect of PTM resistance on the write speed. During the read operation, PTM undergoes data-dependent selective phase transition.

First, on the assertion of the word line, IMT is triggered in the PTM. The cell is designed such that if the MTJ is in the low-resistance parallel state, cell current is high enough to keep the PTM metallic. However, if the MTJ is in the high-resistance antiparallel state, low cell current triggers MIT, thus significantly increasing the resistance of the cell. In this manner, the distinguishability of the spin memories can be enhanced by synergistically utilizing the nonvolatility of MTJs with orders of magnitude resistance difference between insulating and metallic phases of the PTMs. Results from [80] (Fig. 26.17c) show that in addition to a large increase in the sense margin, a simultaneous increase in read disturb margin and a moderate write power reduction are achieved with this technique without any area penalty but with a negligible write time increase. In [79], read improvements under process variations are also established.

In addition to this technique (with series MTJ-PTM connection), PhaseFETs can be used in spin memories with separate read-write paths such that the PTM is connected in parallel with the MTJ [81]. This design also considerably improves the read operation without affecting the write operation (due to the separation of read-write path). Moreover, instead of amplifying the distinguishability at the cell level (as in the aforementioned techniques), this design principle can be extended to the array level, wherein PhaseFETs are utilized to design compact low-power sense amplifiers, in which the core amplification occurs in the PTM (see [82] for details).

Furthermore, PTMs (without transistors) have also been explored to design cross-point NVM architectures, wherein the abrupt switching of the PTMs is utilized to design selectors with high nonlinearity [83].

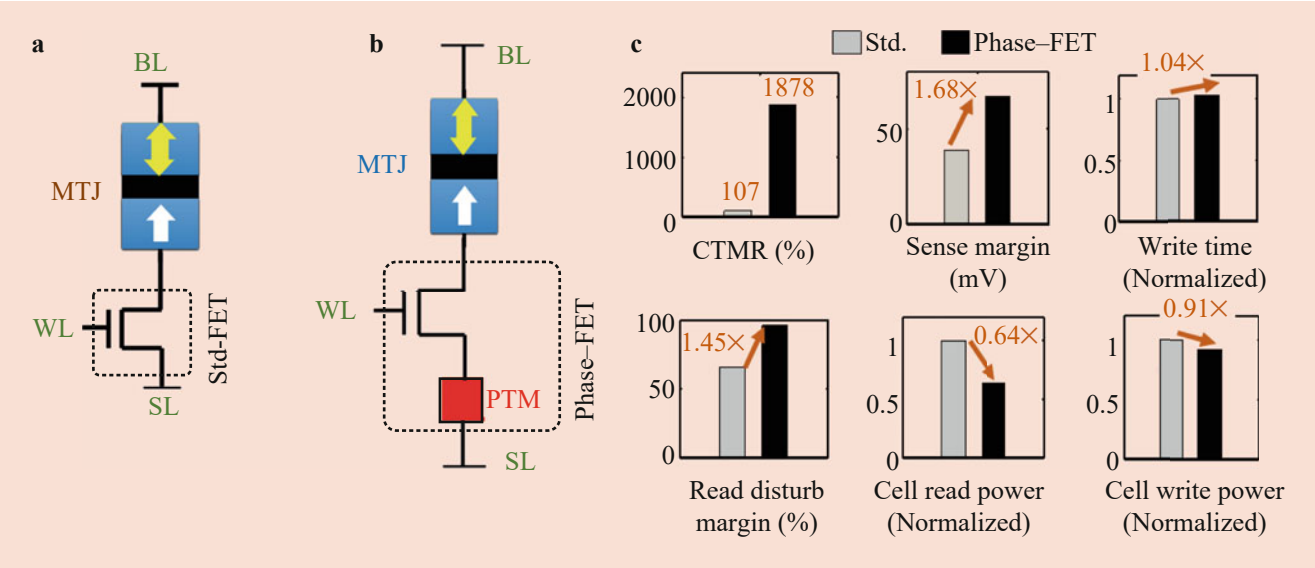

Fig. 26.17 Schematics of magnetic tunnel junction (MTJ) NVM cell based on (**a**) Std-FET and (**b**) PhaseFET. (**c**) Comparison of performances and stability between Std-FET- and PhaseFET-based MTJ NVM cell

26.5 Non-boolean Computing with NCFETs, FeFETs, and PhaseFETs

In the previous section, we presented the potential applications of NCFETs, FeFETs, and PhaseFETs for standard Boolean computing and storage. In this section, we will extend our discussion to non-Boolean computing, wherein we will highlight how the unique attributes of these technologies enable circuits that can cater to the demands of emerging applications. Before we dive into the discussion, let us understand the application perspective for non-Boolean computing. Traditional computing based on Boolean logic and von Neumann architectures has been immensely successful in the era of predominant compute-intensive tasks. However, with the advent of data-intensive applications such as recognition, machine learning, etc., the standard architectures prove to be inadequate to meet efficiency demands. Hence, new computing approaches are being explored that mitigate the limitations of Boolean computing by customizing the architectures, circuits, and technologies to meet the demands of the new applications. Here, we will focus on two non-Boolean computing approaches: (1) coupled oscillator-based computing and (2) neuromorphic computing.

26.5.1 Coupled Oscillator-Based Computing

For certain tasks involving associative computing (e.g., pattern matching) or solving optimization problems (e.g., graph coloring), coupled oscillator-based processing has emerged as a promising computing paradigm. The key idea is to couple multiple oscillators whose oscillation frequency is controlled by the inputs. If the degree of matching of the inputs is high or other interactions are strong, the oscillators get frequency- or phase-locked. Otherwise, they show asynchronous oscillations. This working principle is utilized to find the minima in optimization problems or perform recognition/matching tasks. While CMOS-based oscillators have been utilized for this purpose, it has been shown that emerging technologies can potentially offer higher-energy efficiency [84–86]. Here, we will discuss how NCFETs, FeFETs, and PhaseFETs enable the design of energy-efficient coupled oscillators.

NCFET-/FeFET-Based Coupled Oscillators

FE-based transistors, namely, (a) NCFET which shows steep-switching and NDR and (b) FeFET with hysteretic transfer characteristics, have emerged as promising candidates for compact and low-power beyond-von Neumann architectures powered by their unique device features. An example application based on these architectures is associative computing, for which oscillator-based networks have been a subject of recent study [85, 86]. By leveraging special device-circuit capabilities of NCFET/FeFET, oscillators with significantly reduced transistor count compared to their CMOS-based counterparts are realizable [85, 86].

In [85], an oscillator with one FET and one FeFET (Fig. 26.18a) was proposed. The design utilized abrupt polarization switching and hysteretic transfer characteristics of FeFETs. The key idea is illustrated in the load-line plot of Fig. 26.18c. This circuit would show stable solution if the load line (corresponding to the FET) intersected with the transfer characteristics of the FeFET. With proper design, it can be ensured that the load does not intersect in the flat (solid line) regions of the FeFET characteristics, ensuring that (as

a result of the lack of a stable DC solution) oscillations build up as shown in Fig. 26.18d. This technique is similar to the approach explored for other technologies such as PTMs that we will discuss later on. The design proposed in [85] shows relaxation-type oscillations. Synchronization between two oscillators has also been shown, which can be useful for non-Boolean applications. The oscillatory behavior has also been experimentally demonstrated in [87] utilizing a perovskite-based (e.g., $BaTiO_3$) FeFET. However, since this oscillator design relies on abruptness of polarization switching, it needs to be further explored in the context of CMOS-compatible HZO-based ferroelectrics, which are polycrystalline and hence are expected to have smoother polarization switching due to multi-domain effects [88].

In [86], NCFET-/FeFET-based oscillators (Fig. 26.19a) utilize a different mechanism to achieve oscillations. They rely on Schmitt trigger action or hysteretic VTC of inverters (see Fig. 26.11a). In contrast to the 6 T CMOS-based Schmitt trigger, NCFETs and FeFETs lead to hysteretic VTC with just two transistors by virtue of (a) NDR in NCFETs (discussed in Sect. 26.4, Fig. 26.11a) or (b) hysteretic transfer characteristics ($I_D - V_{GS}$) of FeFETs (discussed in Sect. 26.4, Fig. 26.15b). Hysteretic VTC is translated to voltage-controlled oscillations by a feedback, R_f, from output to input of the inverter. Depending on whether R_f is realized as a pass transistor (PT) or transmission gate (TG), the oscillator outputs a variety of oscillations, viz., (a) relaxation-type with PT in both NCFET (Fig. 26.19b) and FeFET (Fig. 26.19d) implementations, (b) "sinusoid-like" with TG in NCFET-based design (Fig. 26.19c), and (c) "pulse-like" with TG in FeFET design (Fig. 26.19e). Moreover, dynamic reconfiguration between relaxation and "sinusoid-/pulse-like characteristics" is achievable by tuning the bias of P-transistor in TG. Their coupled dynamics have also been analyzed, which show a promise for non-Boolean computing ([86]).

Each of the aforementioned designs has their own benefits and trade-offs. While the design in [85] offers a highly compact solution, the oscillator in [86] has been shown to achieve higher oscillator frequencies in simulations and can be implemented even if the polarization switching dynamics is not abrupt. Moreover, the latter design can be realized by both NCFETs and FeFETs.

PhaseFET-Based Oscillators

Phase transition materials (PTMs) and PhaseFETs offer intrinsic abrupt characteristics and therefore are highly suitable for the realization of relaxation oscillators. In [84], VO_2 has been used in the design of nano-oscillators (Fig. 26.18b). The working principle is based on using a series-connected resistor (or transistor) to prevent the system to stabilize in a particular phase (or find an intersection point in the load-line plot (Fig. 26.18c) by leveraging the abruptness in the current-voltage characteristics. Recall that a similar principle was used in FeFET-based oscillators [85] discussed before. Here, we describe this mechanism in a greater detail.

Let us consider in Fig. 26.18c that the PTM is in the insulating state initially. Hence, the resistor (or transistor) will charge the output node (V_0 – Fig. 26.18c). As the output voltage (or voltage across PTM) increases, IMT is triggered in the PTM. This establishes a low-resistance path from the output to ground, and the output starts discharging. As the output (and hence PTM) voltage decreases, PTM undergoes MIT. This breaks the path to ground, and the resistor (or transistor) again begins to charge the output. This keeps repeating, leading to sustained oscillations as shown in Fig. 26.18d. The gate voltage of the series transistors (not shown in Fig. 26.18b) can be used to tune the oscillation frequency, thus achieving voltage-controlled oscillations.

Further, the coupled dynamics of PTM-based oscillators have also been analyzed in [89] suggesting that the dynamics can be tuned by modulating the resistance of the series transistor, effective capacitance of PTM devices (dependent on PTM dimensions), and coupling capacitance.

26.5.2 Neuromorphic Computing

Neuromorphic computing is yet another form of non-Boolean computing that draws its inspiration from the way our brain processes data (or at least the little that we understand of it). Like for the human brain, the primitives of neuromorphic computing are neurons (or thresholding elements that fire when their weighted sums of inputs exceed a certain value) and synapses (or weights that determine the strengths between different neurons) [90]. Among the many challenges of neuromorphic computing, low-power hardware implementation of neurons and synapses remains one of the key areas of exploration.

While several existing neuromorphic architectures [91] employ CMOS technology, their energy efficiency is nowhere close to our brain. To bridge (or at least narrow) this gap, post-CMOS technologies that are intrinsically more amenable to the functionalities of the neuromorphic primitives are being actively investigated. Here, we review how FeFETs and PhaseFETs can enable low-power neurons and synapses by virtue of their unique attributes.

FeFET-Based Synapses

In FeFETs, under certain conditions [92], the FE can form multi-domains with alternating polarization directions (see Fig. 26.20a). In this multiple domain (MD) scenario, the average macroscopic polarization, $\overline{P}$, depends on the relative size of the $+P$ and $-P$ domains, which can be tuned by applying a gate voltage pulse, V_{PULSE}, as shown in Fig. 26.20b and thereby inducing a domain wall motion. Such changes in $\overline{P}$ modify the channel carrier concentrations due to the

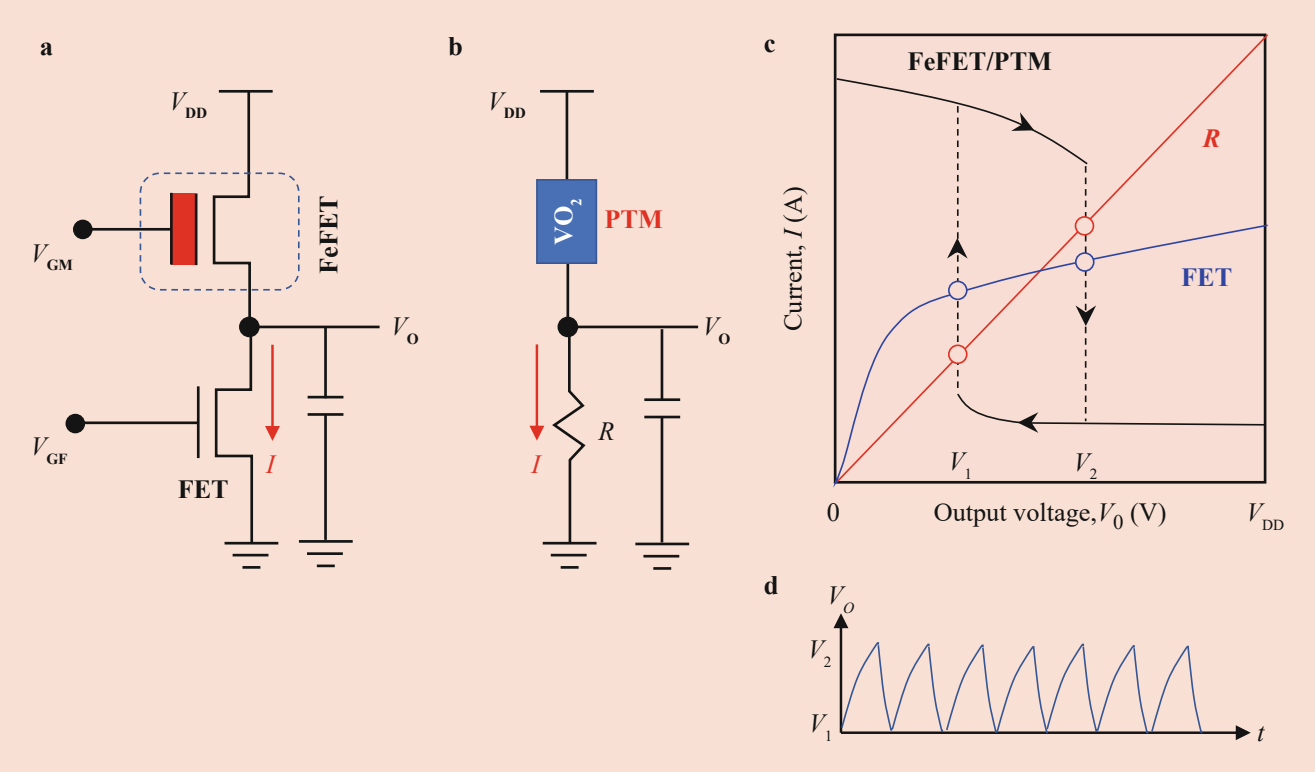

Fig. 26.18 Schematics of (**a**) FeFET-based and (**b**) PTM (or PhaseFET)-based oscillators. (**c**) Load-line plot portraying the working principle of the oscillators. (**d**) Illustration of oscillatory output waveform

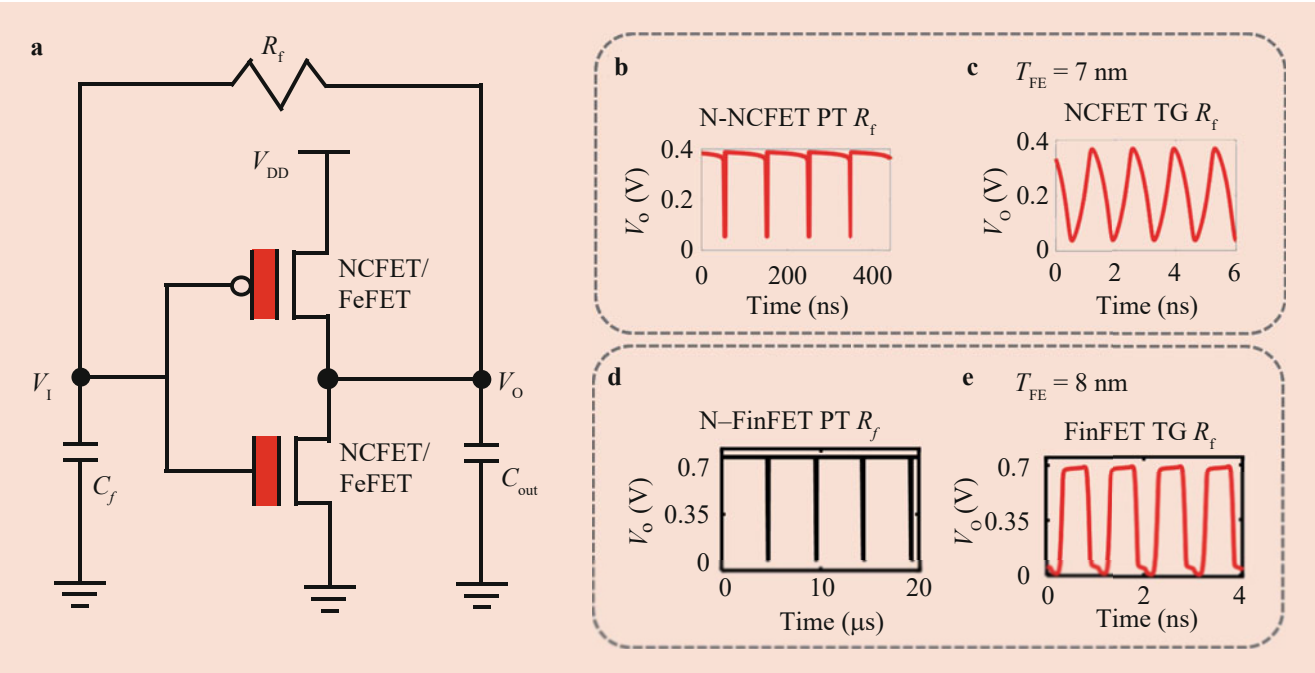

Fig. 26.19 (**a**) Schematic of NCFET/FeFET inverter-based oscillator with a feedback resistor, R_f, implemented with pass transistor (PT) or transmission gate (TG). Simulated oscillatory waveform for (**b**) NCFET oscillator with PT. (**c**) NCFET oscillator with TG. (**d**) FeFET oscillator with PT, and (**e**) FeFET oscillator with TG. (From [86] © 2019 IEEE)

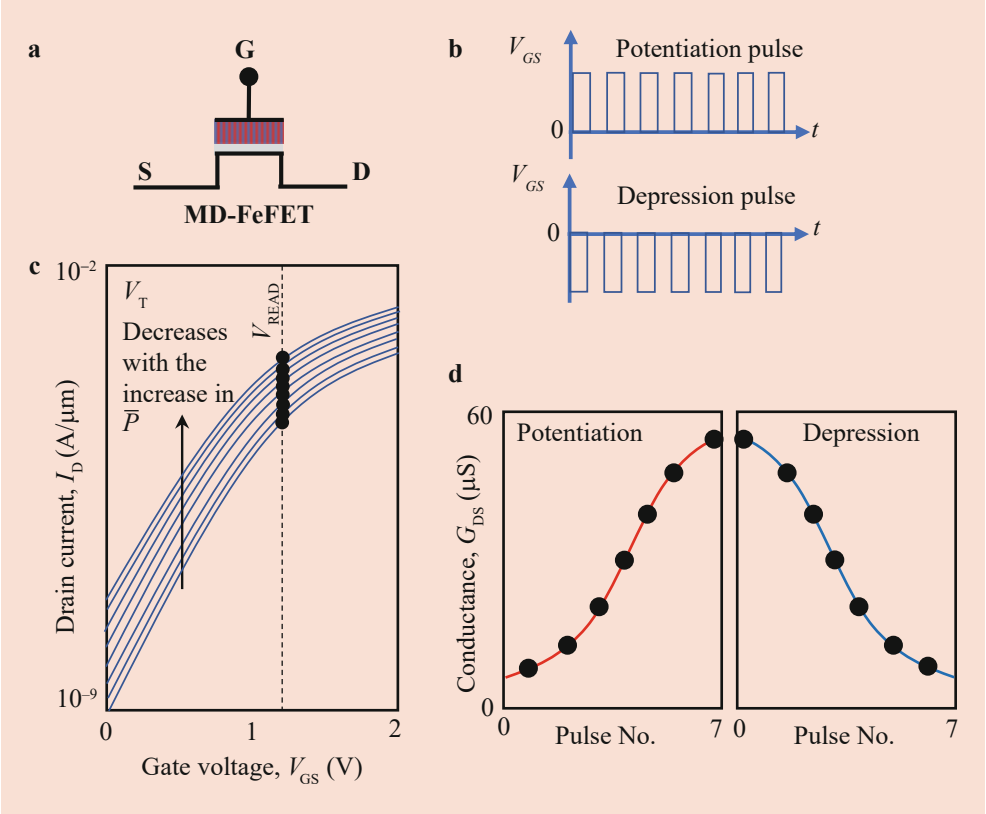

Fig. 26.20 (**a**) FeFET with multiple domains (MDs) in FE. (**b**) Voltage pulse scheme for synaptic potentiation and depression. (**c**) I_D–V_{GS} characteristics of MD-FeFET for different $\overline{P}$ that corresponds to the change in V_T. (**d**) Synaptic potentiation and depression characteristics of MD-FeFET

electrostatic coupling between the FE and the semiconductor. Alternately, the V_T of FeFET changes due to the change in $\overline{P}$ (see Fig. 26.20c), which is analogous to the dependency of V_T on the fixed oxide charge in MOSFETs. Moreover, the change in $\overline{P}$ is dependent on the magnitude and time duration of V_{PULSE} [88]. Therefore, by modulating V_{PULSE}, the V_T of the FeFET can be tuned, and thus the channel conductivity ($G_{DS} = I_D/V_{DS}$) can be modified gradually. This gradual change in G_{DS} in MD-FeFETs (see Fig. 26.20d) can readily be exploited to mimic multilevel synaptic behavior.

FeFET-based multilevel analog synaptic devices have been experimentally demonstrated in [93], where the G_{DS} potentiation and depression via a gradual V_T tuning were obtained by applying a voltage pulse at the gate terminal. However, in case of identical voltage pulses, the observed potentiation and depression characteristics are highly nonlinear and asymmetric with respect to the number of pulses. To overcome such nonidealities, different nonidentical pulsing schemes were proposed in [93]. These schemes utilize a gradual modulation of pulse amplitude or duration to improve the potentiation/depression linearity and symmetry. However, if pulses are not identical throughout the programming process, an additional step of accessing the synaptic weight (G_{DS} value) is needed every time an update takes place so that an appropriate pulse can be applied. This leads to design overheads and may increase the energy consumption of the network during training. In this regard, by using identical pulses, improved linearity and asymmetry were experimentally demonstrated in a ferroelectric germanium nanowire FET (Fe-GNWFET) [94].

In addition, an FeFET synapse featuring spike timing-dependent plasticity (STDP)-based update scheme has been demonstrated in [73] for spiking neural networks (SNNs). The proposed circuit design is shown in Fig. 26.21a, where a resistor is connected between the gate and the drain terminals of the FeFET to enable the two-terminal operation of the synapse. With this circuit design and the spiking waveform proposed in [73], the relative spike timing between the pre- and the post-neuron can be converted into a voltage drop across the FeFET. As a consequence, the closer the pre- and post-neuron spiking in the time domain, the higher is the voltage drop across the FeFET, and the larger is the change in G_{DS}. The STDP pattern considering the synaptic potentiation and depression is qualitatively depicted in Fig. 26.21b.

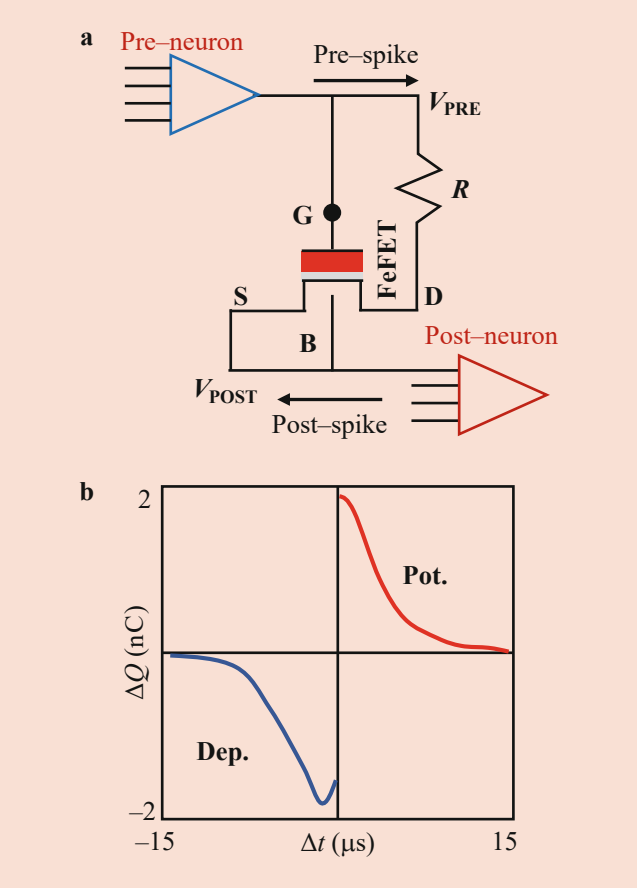

Fig. 26.21 (**a**) Schematic of FeFET-based synapse and the corresponding (**b**) spike timing-dependent plasticity (STDP) pattern

FeFET-Based Neurons

In a spiking neural network, the basic functionality of a spiking neuron is to integrate the voltage spikes fed to its excitatory input over a period of time and to generate an output spike (called fire) when the integrated quantity becomes higher than a threshold value. In addition to these integrate and fire (IF) behaviors, a neuron may also feature a leaky property while integrating spikes and is referred to as leaky integrate and fire (LIF) neuron. So far, different flavors of FeFET-based spiking neurons have been experimentally demonstrated, which we briefly discuss in this section.

The FeFET spiking neuron demonstrated in [87] comprises of 1T-1FeFET structure, where the FE layer, made out of lead zirconium titanate (PZT), is separately connected at the gate of the underline transistor with a metal (Fig. 26.22a). In this design, the "leaky" and "integration" functionalities of the neuron have been implemented in the external RC circuit, whereas the abrupt "firing" event has been mimicked through the abrupt polarization switching of FE in response to the input spikes at the gate of the FeFET (Fig. 26.22a).

The FeFET neuron demonstrated in [95] (comprising of 1R-1FeFET as shown in Fig. 26.22b) does not need an RC network and can mimic the leaky integration behavior by utilizing the inherent polarization switching dynamics of FE. In this design, an M-FE-M capacitor is connected to the gate of the underlying transistor to form the FeFET structure. A thin partially crystallized zirconium-doped hafnium oxide (HZO) layer is used so that the tunneling current can induce the leaky behavior in M-FE-M capacitor. For integration functionality, multi-domain polarization switching behavior is utilized (described earlier in the context of MD-FeFET synapse), so that the spiking inputs at the FeFET gate terminal gradually modulate the channel conductivity and hence change the output voltage of the 1R-1FeFET circuit to generate a voltage spike (Fig. 26.22b).

The FeFET-based neuronal dynamics demonstrated in [96] utilizes the polarization accumulation of FeFETs. Unlike the previous designs [95, 87], the FE layer (HZO) is directly integrated in the gate stack of FeFET. When a voltage pulse is applied to the FeFET gate for a limited time duration (typically less than the writing time of FeFET NVM), the polarization does not switch completely but merely changes incrementally. However, after a certain number of pulses are received, the FeFET abruptly switches to the LRS. Such phenomenon can be understood as the initial nucleation of nano-domains followed by an abrupt polarization reversal of the entire FE layer. Now, the applied pulses prior to the latching of the LRS can be regarded as the process of "integration" of excitatory inputs, whereas the subsequent abrupt transition from HRS to LRS can be regarded as the "firing event." To obtain the leaky behavior, a proposed option is the insertion of a negative inhibitory voltage in the intervals between consecutive excitatory pulses.

Apart from this externally emulated leaky feature (by applying an additional inhibitory signal), the possibilities for an intrinsically leaky process have been theoretically predicted in [88], which originates from the domain wall instability leading to spontaneous relaxation in average polarization. Such leaky characteristics have been experimentally demonstrated in an HZO thin film [97]. Moreover, the polarization leak rate exhibits a dependence on the initial polarization value, which is distinct from the conventional leak rate of first-order system (i.e., RC network). Utilizing such quasi-leaky (QL) behavior along with the IF characteristics, a quasi-leaky-integration-fire (QLIF)-type FeFET-based neuron was realized [97]. QLIF analysis predicted a reduction in firing rate in SNNs compared to traditional LIF neuron at iso-accuracy.

PhaseFET-Based Neurons

By virtue of their abrupt phase transitions, PTMs (and hence PhaseFETs) can potentially be ideal candidates for the implementation of the thresholding function of neurons. In

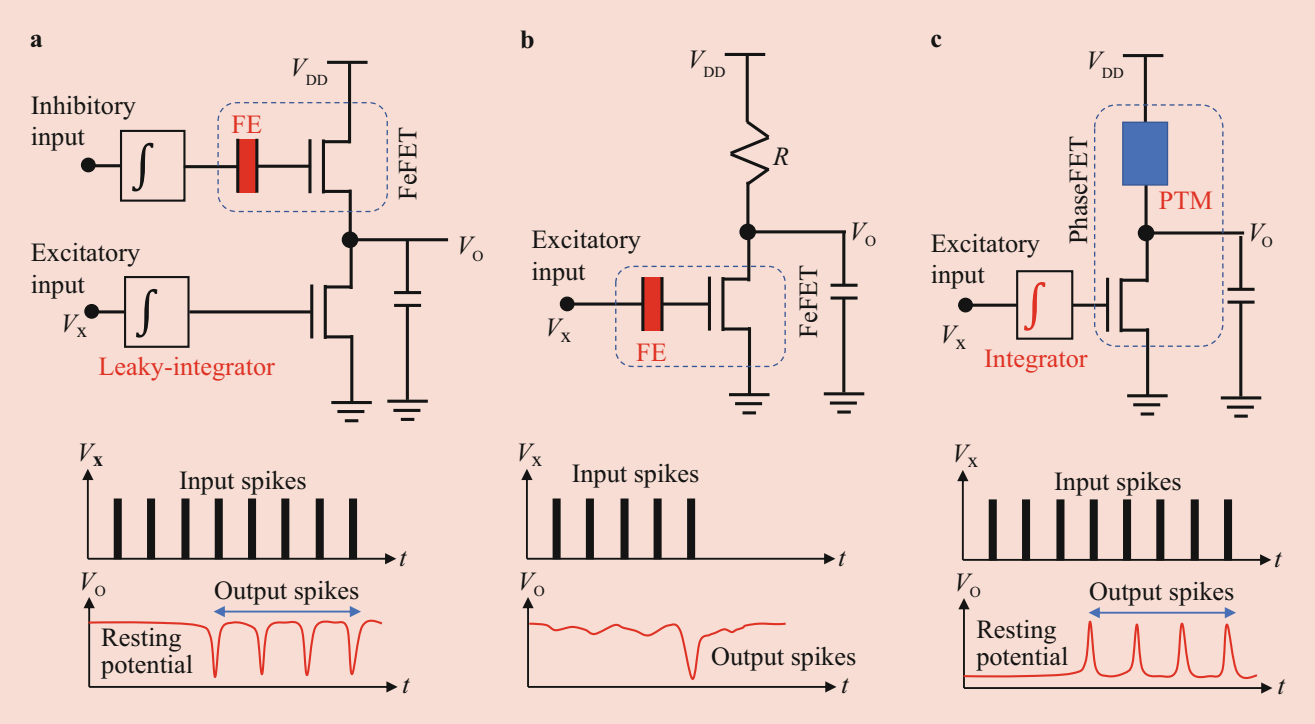

Fig. 26.22 Schematics and input-output spiking waveform for (**a**) 1T-1FeFET neuron, (**b**) 1R-1FeFET neuron, and (**c**) PhaseFET (1T-1PTM) neuron

addition, the ability of PTMs to oscillate (see Sect. 26.5.1) offers an elegant method of generating a train of output spikes where the spiking frequency can be used to encode the data. These features have been used in [54] to design a spiking neuron, as shown in Fig. 26.22c. Moreover, by biasing the neuron close to the critical voltage for IMT and leveraging the inherent randomness of the phase transition in PTMs, stochasticity in the neuron firing can be achieved. Stochastic neurons have been known to facilitate better generalization by preventing over-fitting of data during training [54]. PhaseFETs offer an ultralow-power hardware solution to design stochastic neurons. It is noteworthy that the PhaseFET only provides the thresholding (or fire) functionality; the leaky integrate functionality is obtained using additional circuitry. In contrast, FeFETs have been shown to exhibit a wide range of unique characteristics that can potentially achieve the LIF with a minimal number of transistors.

26.6 Summary and Conclusions

In this chapter, we presented a systematic overview of the fundamental device physics and the applications of NCFETs and PhaseFETs, given their immense potential to outperform MOSFETs in specific applications where low-power consumption is of paramount importance. These devices were first conceptualized to overcome the fundamental physical limits dictated by the Boltzmann tyranny that lead to the unbearable power dissipation in standard MOSFETs, especially at deeply scaled technology nodes.

We presented a theoretical analysis of NCFETs based on the phenomenological Landau theory that describes the negative capacitors as special capacitors with double-well energy landscape. Their unique properties enable a voltage step-up action in the gate stack that, in turn, leads to steep-switching. We described the conditions to achieve subthermionic switching (i.e., subthreshold swing lower than the Boltzmann limit of 60 mV/dec at room temperature) for a particular class of NCFETs employing ferroelectrics as a negative capacitance layer. We also provided a comparison of the reliability physics of NCFETs with conventional MOSFETs to outline the advantages and drawbacks of the technology. We additionally discussed the advanced issues along with open questions that need to be answered to fully harness the potential of NCFETs. Similarly, we discussed the theoretical aspects of PhaseFETs, which utilize a phase transition material in series with a conventional transistor to obtain steep-switching. We also outlined their current stage of development (presenting experimental data from the literature).

We also discussed various circuit applications of NCFETs and PhaseFETs. We began by presenting the implications of steep-switching and other unique features of NCFETs and PhaseFETs on the performance of Boolean logic and

SRAMs, showing delay reduction at iso-energy at low voltages and improvements in stability/noise immunity. In addition to steep-switching, ferroelectric-based transistors offer hysteretic characteristics, which can be highly beneficial for low-power nonvolatile memory (NVM) designs. In contrast, PhaseFETs cannot be used as NVMs; however, they can be employed to augment MRAMs to improve their read stability and distinguishability. Furthermore, the unique characteristics of FeFETs, NCFETs, and PhaseFETs enable low-power hardware for non-Boolean computing such as coupled oscillators and neuromorphic primitives. Our discussion points to the importance of understanding the unique device-circuit interactions in these technologies to translate their rich physics into useful circuit functionalities.

Every couple of years or so, new predictions about the demise (and confirmation) of Moore's law are discussed in conferences as well as in the general media. Although we cannot predict with certainty when the final chapter of this very fortunate roadmap will be written, newer devices like NCFETs and PhaseFETs provide researchers with confidence that the ability of mastering new challenges and overcoming the limits of current technology will never completely falter. In this sense, steep-switching devices belong to an exciting novel class of transistors that not only can potentially improve conventional logic switches and semiconductor memories but also offer advantages to novel applications, as for example to realize super-Nernstian nano-biosensors [98, 99]. In general, both NCFETs and PhaseFETs pave the way for a brand-new design space for a variety of applications that are yet to be explored and that we expect will continue to grow in the decades to come.

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Flexible Electronics and Bioelectronics Devices

27

Chen Jiang, Xiang Cheng, Hanbin Ma, and Arokia Nathan

Contents

27.1 Flexible Electronic Devices and Fabrication 960
27.1.1 Key Materials 960
27.1.2 Fabrication Methods 964
27.1.3 Printable and Flexible Transistors 971

27.2 Modelling of Flexible TFTs and Circuit Design Considerations 976
27.2.1 TFT Compact Modelling 976
27.2.2 Small-Signal Modelling 986
27.2.3 Subthreshold Operation for Schottky Barrier TFTs 1001

27.3 Applications of Flexible Electronics in Biological Sensing 1005
27.3.1 Current Mainstream Biosensing Technologies 1005
27.3.2 Semiconductor Technologies for Biosensing 1005
27.3.3 Fully Integrated CMOS Biosensor 1008
27.3.4 Heterogeneously Integrated Biosensor with Disposable Electrodes 1010
27.3.5 Impedance-Based Immunosensor [244] 1012
27.3.6 TFT-Based Biosensors 1014

References 1016

Abstract

Thin-film transistors (TFTs) have been successfully used as the key electronic components in today's displays in mobile electronic devices and televisions, as well as in a new realm of biomedical imagers and related applications. The requirement for mechanical flexibility and stretchability, needed in a new generation of displays and wearable devices, poses new process integration challenges for TFTs, particularly for some materials families. This chapter is focused on the flexible TFTs and their biomedical applications, in which the materials presented are drawn from several doctoral theses. We begin with a comparison of TFT technologies based on different material families in terms of their electrical performance and flexibility. The general methods for TFT fabrication are introduced, along with a special focus on printable and flexible TFTs. Subsequent discussions are focused on introducing concepts underlying modelling and simulation of flexible TFTs, addressing circuit design considerations and compensation for spatial and temporal device variations and related instabilities. Here, we review the different TFT compact models that have been reported along with small signal models and techniques for parameter extraction. Finally, we focus on the applications of flexible electronics and biomedical applications, addressing the challenges and benefits of using flexible sensors and sensor interfaces, related system design, and integration considerations, along with different use cases.

Keywords

Flexible Electronics · Thin-Film Transistors · Bioelectronic Devices

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27.1 Flexible Electronic Devices and Fabrication

27.1.1 Key Materials

Typical TFT technologies are broadly based on four types of materials and structures. These include amorphous silicon, low-temperature polycrystalline silicon, amorphous oxide

Table 27.1 Basic performance and fabrication specification comparison for TFT technologies

TFT technologies	a-Si	LTPS	IGZO	Organics
Material				
Band gap (eV)	~1.8	~1.1	>3	1–3
Density of deep states (cm^{-3} eV^{-1})	$\sim 10^{18}$	$\sim 10^{18}$	$\sim 10^{17}$	$>10^{14}$
Device				
SS[a] (V/dec)	0.5	0.2–1	0.1–0.3	0.05–1
(SS variation)	(~0.2)	(~0.1)	(~0.02)	(0.01–0.2)
V_T^b (V)	~5	~5	>1	~0
(V_T variation)	(~0.5)	(~1)	(~0.2)	(~0.1)
I_{ON}/I_{OFF}	$\sim 10^7$	$\sim 10^7$	$>10^7$	$>10^6$
Operating voltage (V)	2–20	2–20	2–5	1–10
Circuit				
Amplifier gain (V/V)	10–50	20–100	10–200	5–260
Power consumption (W)	>100n	~1μ	1n–1μ	1n–1μ
Fabrication				
Processes	Vacuum	Vacuum	Semi-printing	All-printing
Process temperature (°C)	~350	~500	>200	<130
Equipment cost ($)	>1 million	>1 million	~1 million	~40,000
Layout cost ($/$m^2$)	~400,000	~800,000	~500,000	~0
Material waste	>80%	>80%	30~80%	<1%

[a]Subthreshold slope
[a] Threshold voltage

semiconductors, and organic families, all of which have different electrical and mechanical properties [1] (Table 27.1).

Amorphous Silicon

Amorphous silicon (a-Si) is the non-crystalline form of silicon and was used in the first commercialized TFTs (Fig. 27.1). Before the 1960s, a-Si was formed by sputtering or by thermal evaporation, and the material had a very high defect density, which prevented doping, photoconductivity, and the other desirable characteristics of a useful semiconductor [2]. To reduce the defects, in 1974, Lewis et al. introduced hydrogen to the sputtering system and improved the material properties with high photoconductivity, a low defect density, and low doping [3]. A similar improvement was achieved actually 5 years earlier by Chittick et al. using radiofrequency (RF) glow discharge to deposit a-Si thin films from silane (SiH_4) gas [4], but the effect of Si-H bonds in improving material quality had not been found. Since the findings by Chittick et al. and Lewis et al., hydrogenated a-Si has been intensively developed using SiH_4 through plasma-enhanced chemical vapour deposition (PECVD) and has been widely used in solar cells and TFTs for display pixel circuits. Despite this success, a-Si TFTs demonstrate a mobility of around $1\,cm^2V^{-1}s^{-1}$, which is far lower than that of single-crystalline silicon in metal-oxide-semiconductor field-effect transistors (MOSFETs) ($1400\,cm^2V^{-1}s^{-1}$ and $450\,cm^2V^{-1}s^{-1}$ for electron and hole mobility, respectively) [5]. The main factor that limits the mobility of a-Si films is the nature of disordered

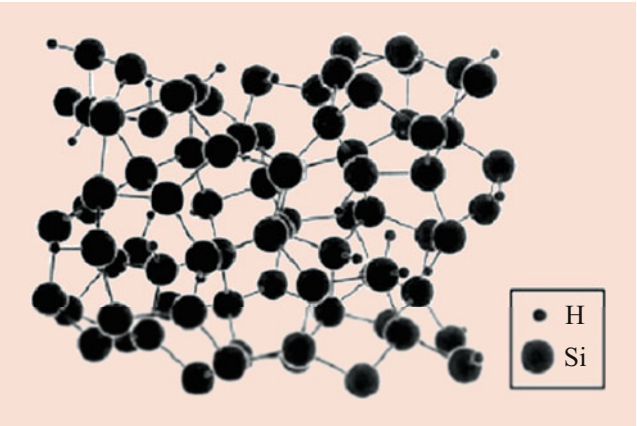

Fig. 27.1 Structure of hydrogenated amorphous silicon. (Adapted from [2])

crystalline structure that causes scattering at the grain boundaries. To reduce scattering and increase material mobility, a better ordered form of silicon is necessary, giving rise to polycrystalline silicon. In addition, a-Si TFTs are manufactured with vacuum systems, i.e. PECVD, sputtering, and reactive-ion etching. Thus, the manufacturing cost still needs to be reduced.

Low-Temperature Polycrystalline Silicon

Polycrystalline silicon (poly-Si) is a form of silicon whose crystalline order is between that of single-crystal silicon and a-Si, with grain sizes in the range of 1–100 μm. However, the

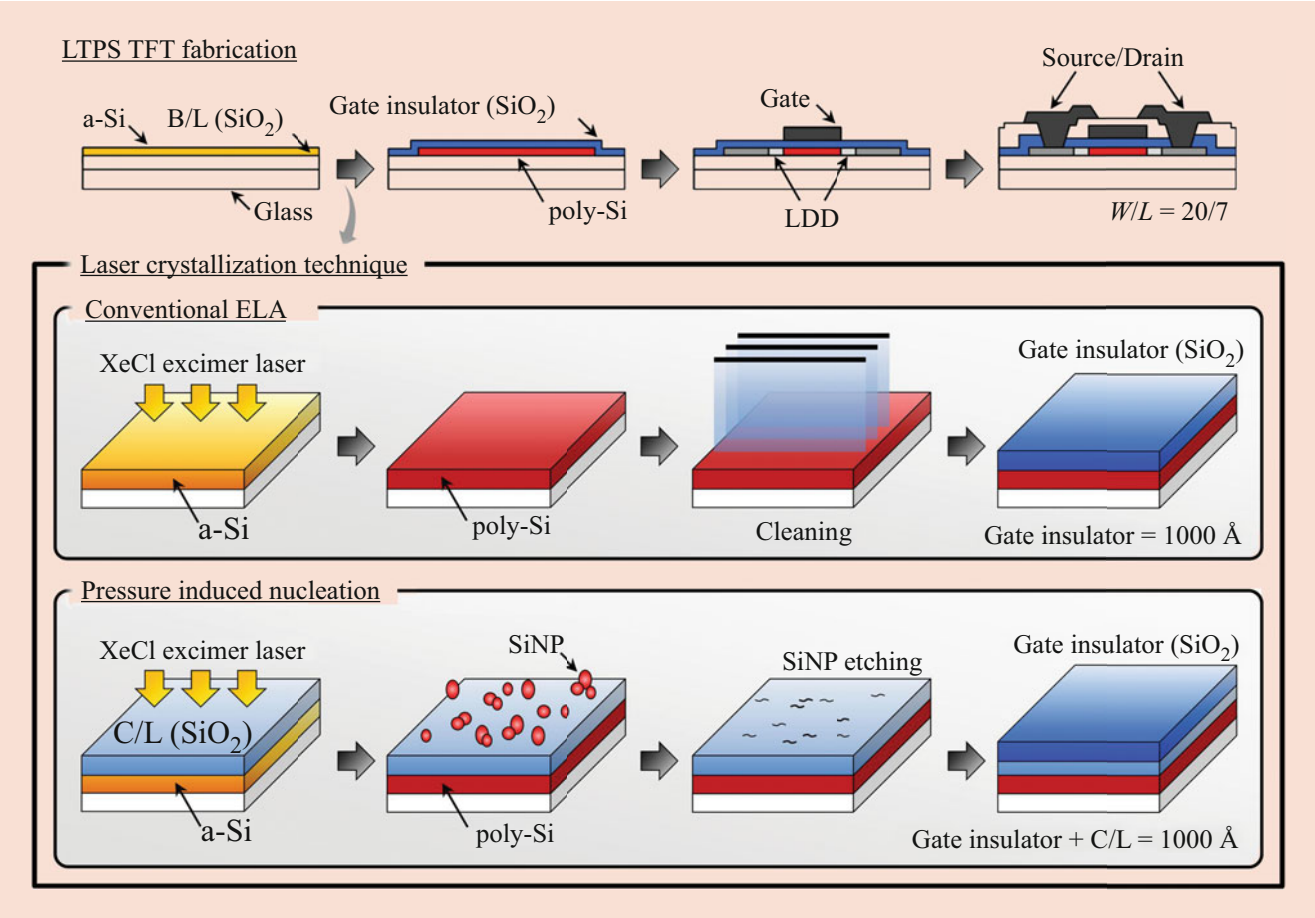

Fig. 27.2 Schematic illustration of the LTPS TFT fabrication scheme. (Adapted from [10])

conventional poly-Si process requires a high temperature of over 900 °C. Due to the requirements for display manufacturing at low temperatures on glass substrates, low-temperature polycrystalline silicon (LTPS) was invented by using XeCl excimer laser annealing (ELA) to produce poly-Si by melting a-Si material through laser irradiation (Fig. 27.2). The ELA temperature is relatively low (i.e. ~500 °C) compared to the conventional process. However, the additional poly-crystallization process from a-Si increases both process temperature and time [6]. To tackle these problems, pulsed rapid thermal annealing was developed [7, 8]. Due to larger grain sizes, LTPS TFTs generally show a high mobility of ~100 $cm^2V^{-1}s^{-1}$, and reports have demonstrated their use in logic circuits, memories, and CPUs [9]. However, there is a lack of reliable large-area production processes for LTPS TFTs with good mobilities [6], and scaling up LTPS TFTs significantly increases the cost for delicate and complex XeCl excimer lasers, therefore necessitating alternative methods for producing poly-Si.

In addition to poly-crystallization from a-Si, poly-Si films can be solution processed. Shimoda et al. reported spin-coated and inkjet-printed poly-Si TFTs through ultraviolet (UV) irradiation of cyclopentasilane (which is a liquid silicon material), demonstrating a high mobility of 108 $cm^2V^{-1}s^{-1}$ and 6.5 $cm^2V^{-1}s^{-1}$, respectively [11]. With solution-processed poly-Si, the process temperature was further reduced to 300–400 °C, compared to ELA. However, for flexible TFTs, their substrates require mechanic flexibility. Good substrate candidates are polymers, such as polyethylene terephthalate (PET), polyethylene naphthalate (PEN), and polyimide (PI), but their glass transition temperatures are <200 °C. Therefore, the process temperatures for silicon-based TFTs are still too high, and low-temperature (i.e. <200 °C) processable semiconductor alternatives are demanded.

Amorphous Oxide Semiconductors

Metal oxide semiconductors are a class of TFT materials, including binary oxides (ZnO, In_2O_3, SnO_2, Ga_2O_3) and ternary and quaternary compounds from the binary materials. In the past decade, amorphous indium gallium zinc oxide (a-IGZO) has been intensively studied, demonstrating a high mobility of >10 $cm^2V^{-1}s^{-1}$ while balancing several issues in the binary systems, including instability [12], low

mobility [13], and low current on/off ratio [14]. The reason that amorphous oxide semiconductors (AOS) possess high electron mobilities is that AOS are ionically bonded by oxygen sp^3-orbitals with metal s-orbitals, of which the shape is a sphere [15] (see Fig. 27.3). Therefore, metal s-orbitals are insensitive to bonding angles, resulting in high electron mobilities even in an amorphous phase. This is a key advantage of AOS over a-Si, in which the covalent bonds formed by silicon tetrahedral-shape sp^3-orbitals are sensitive to bonding angles, significantly degrading carrier mobility in an amorphous phase.

The high electron mobilities of AOS enable low-temperature sputtering AOS, which can greatly reduce the manufacturing cost compared to using PECVD. In addition, the wide band gaps (>3 eV) of most AOS make them suitable for transparent electronics [16] and more importantly ultra-low-power electronics [17, 18] for flexible electronics. However, ZnO-based TFTs fabricated at a low temperature lack operational stability unless annealed at 400 °C [19], since Zn-containing AOS are sensitive to moisture in the ambient environment [20]. This limitation motivated the development of Zn-free AOS TFTs. In_2O_3 is a good base material due to its wide band gap of 2.9 eV, but the issue of In_2O_3-based AOS is their stability due to excessive oxygen vacancies (V_O). Suppressing V_O can be achieved by adding gallium, as well as silicon, titanium, and tungsten, to enhance TFT operational stability [21–23]. Since the increasing usage of indium as a key material in the solar cell and display industry resulted in the shortage of indium, indium-free AOS became popular, such as gallium tin zinc oxide (GSZO) [24], tungsten-doped ZnSnO (WZTO) [25], and zinc oxynitride (ZnON) [26–28]. Despite these, a-IGZO is still the most popular material among AOS.

Apart from n-type AOS, some oxide semiconductors are p-type, such as tin oxide (SnO) [29] and copper oxide (CuO) [30]. These materials can also be deposited by sputtering. With both n-type and p-type semiconductors, complementary metal oxide semiconductor (CMOS) based on AOS was reported by Martins et al., demonstrating ultra-low-power circuits on flexible paper substrates [31, 32].

Since sputtered AOS TFTs require vacuum systems to further reduce manufacturing cost, solution-processed AOS have also been investigated. The soluble precursors are important. Common precursor solutions include acetate-, nitride-, and chloride-based precursors, among which the former two require lower process temperatures. The reactions from precursors to AOS generally take three steps: decomposition of metal ions and acetates/nitrides, hydrolysis of metal ions to form metal-OH bonding, and dehydroxylation to form metal-oxygen bonding. The maximum process temperatures are in the range of 200–300 °C. Based on soluble metal oxide precursors, AOS TFTs have been demonstrated by spin coating [33], spray coating [34], and inkjet printing [35–37], depicting high ($>10\,cm^2V^{-1}s^{-1}$) electron mobilities. In comparison to sputtered AOS, solution-processed AOS requires relatively high (>200 °C) process/annealing temperatures. There have been reports of solution-processed AOS TFTs under 200 °C [38], but the device performance is generally not as good as those annealed at higher temperatures (e.g. >250 °C) [39]. Although improvements are evident compared to the process temperatures for silicon-based solution-processable semiconductors, further developments in low-temperature AOS are required to meet the requirements of flexible plastic substrates.

Organic Semiconductors

Organic semiconductor materials are carbon-based compounds that consist of π-conjugation systems, which contribute to electron/hole charge transport. Depending on their molecular structures, organic semiconductor materials can be categorized into small molecules and polymers depending on their molecular structures. The most common small molecules include rubrene [40], pentacene (and its derivatives) [41], anthradithiophene (ADT) derivatives [42], and benzothieno[3,2-b] [1], benzothiophene (BTBT) derivatives [43]. Most polymer semiconductors are thiophene-based, such as region-regular poly-(3-hexylthiophene-2,5-diyl) (P3HT) [44] and indacenodithiophene-co-benzothiadiazole (IDT-BT) [45]. In general, small molecules can form well-ordered crystalline phases and thus demonstrate higher mobilities; however, mobilities of small molecules depend on the stacking directions of molecules [46], which are randomly distributed by most deposition methods (e.g. spin coating, inkjet printing), resulting in large variation of mobility values. In contrast, polymers are normally in amorphous phases, which yield better uniformities but lower mobilities ($<1\,cm^2V^{-1}s^{-1}$). The first organic TFT was invented by Koezuka et al. using polymer semiconductor, polythiophene in 1987, but the mobility was only $2\times10^{-5}\,cm^2V^{-1}s^{-1}$ [47]. In the past three decades, significant developments in organic semiconductors have been achieved, with a high mobility of $>10\,cm^2V^{-1}s^{-1}$ in both small molecules and polymers [48].

The most striking advantage of organics is their solution processability. Although silicon and AOS are also solution-processable, they need high process temperatures for precursors to react and form the desired materials and structures. In contrast, organics can easily dissolve in compatible organic liquids, which simplifies the processes of ink formulation and post-deposition reactions/treatments. This feature of organics enables organic TFTs and circuits printable on plastics with process temperatures of lower than 130 °C [50]. In addition, all-printed organic TFTs have been reported [51–53]. However, conventional solution-processed organic TFTs require high operating voltages of several tens of volt,

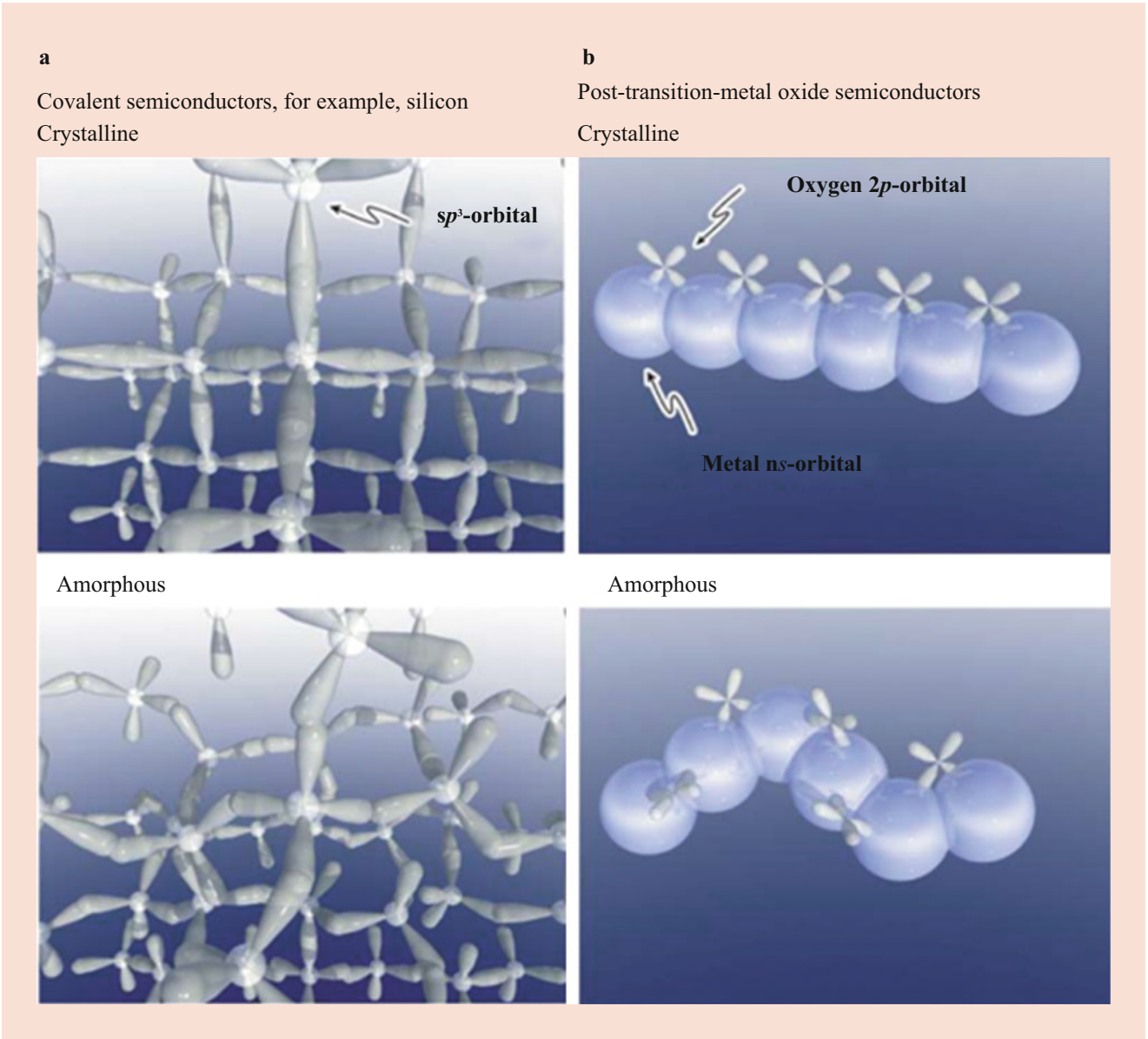

Fig. 27.3 Schematic orbital drawings for charge transport paths in the conduction band of crystalline and amorphous covalent (**a**) semiconductors (e.g. silicon) and (**b**) metal oxides. (Adapted from [15])

which contradicts the idea of low power. To tackle this issue, considerable effort has been made to lower the operating voltage of organic TFTs, and reports have demonstrated low an operating voltage of less 1 V, which has greatly reduced the power consumption for TFT operation [54–56].

Another advantage of organics is their mechanic flexibility. In contrast to silicon and metal oxides that are covalently bonded, organic molecules are van der Waals bonded and therefore can restore themselves from certain bending deformations. Someya and his coworkers have developed organic TFTs with both n-type and p-type devices and integrated them into circuits, demonstrating extreme bending stability [57, 58]. The same research group has reported ultra-flexible and ultra-lightweight organic TFTs, which are potential candidates for imperceptible electronics to be employed on the skin [59]. In recent years, intrinsically stretchable organic semiconducting materials have been achieved by Bao and her coworkers through the nanoconfinement of polymers into nanometer-scale dimensions (see Fig. 27.4), which can alter many polymer physical properties, including lowering the mechanical modulus and glass transition temperature and increasing the mechanical ductility [49, 60]. In addition to flexibility and stretchability, organic TFTs have also been developed as essential components for sensors [61], radiofrequency identification (RFID) tags [62], smart memories [63], point-of-care diagnostic systems [64], and wearable systems

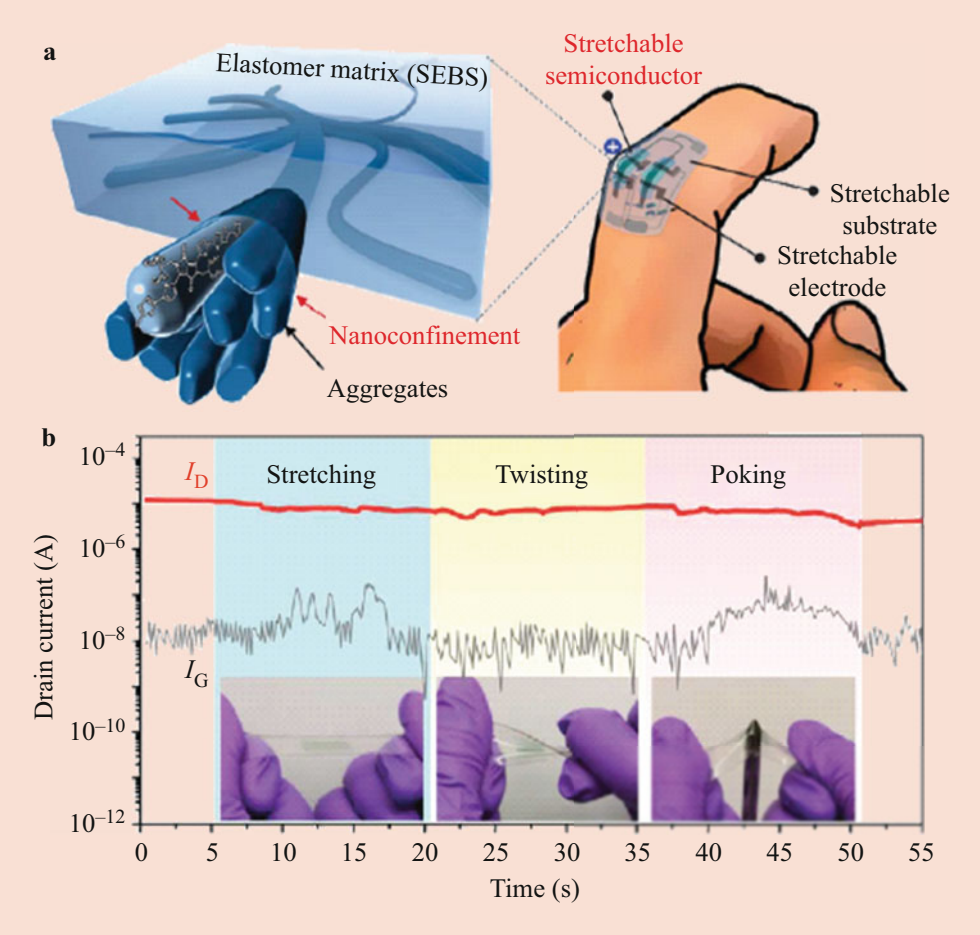

Fig. 27.4 Nanoconfinement effect for enhancing the stretchability of polymer semiconducting film and organic TFT. (**a**) A 3D schematic of the desired morphology composed of embedded nanoscale networks of polymer semiconductor to achieve high stretchability, which can be used to construct a highly stretchable and wearable TFT. (**b**) Drain current (I_D) and gate current (I_G) of a fully stretchable TFT under sequential stretching, twisting, and poking with a sharp object. (Adapted from [49])

[65]. With good compatibility to the skin, the organic TFT-based flexible e-skin has been proposed and developed [66].

27.1.2 Fabrication Methods

Vacuum Depositions

Thermal Evaporation

Thermal evaporation is a popular technique for thin metallic layer deposition such as aluminium and chrome due to their simplicity (see Fig. 27.5). It can be also used for organic semiconductor deposition. The source material is placed on a conductive carrier (normally tungsten or molybdenum with a much higher melting point), a filament, or a boat. A current is passed through the carrier to heat the source material to an evaporation point. The substrate is placed above the evaporating material, and any molecules that hit the substrate will condense. The distance between source and substrate should be large enough to grant the thin film uniformity but also small compared with the mean free path in the vacuum. The evaporation generally produces amorphous layers. The poor step edge coverage and non-uniformity over large areas are the main disadvantages of this process.

Sputtering

Sputtering employs a large source target, which is normally a block of metal [67, 68]. A bigger source metal will contribute better uniformity relative to evaporation with a point metal source see Fig. 27.6. Sputtering also provides good step coverage. However, sputtering is a more costly process to implement, as an inert gas is required to fire at the target under a vacuum. The basic principle behind sputter coating is that the inert gas ion passes its kinetic energy to the atoms at or near the target surface, allowing them to escape into the vacuum. The released atoms will condense when they hit the substrate. Argon is most commonly used for a sputtering system, but it may also be incorporated into the substrate

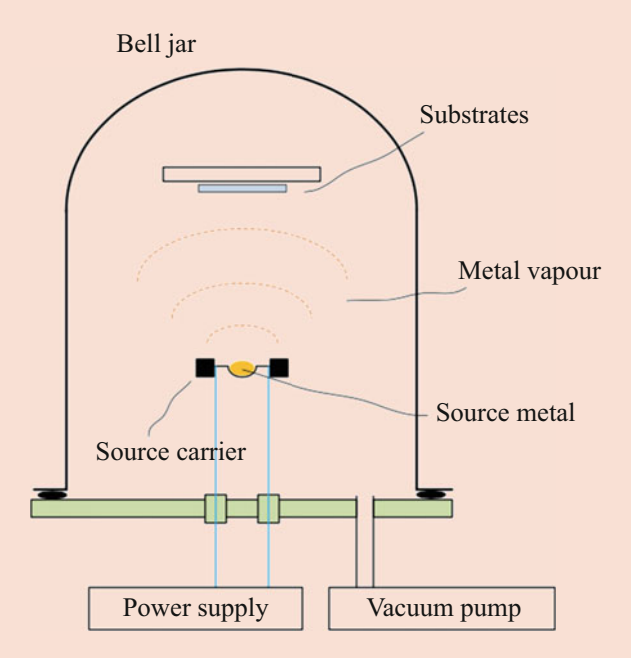

Fig. 27.5 A typical bell jar thermal evaporation system

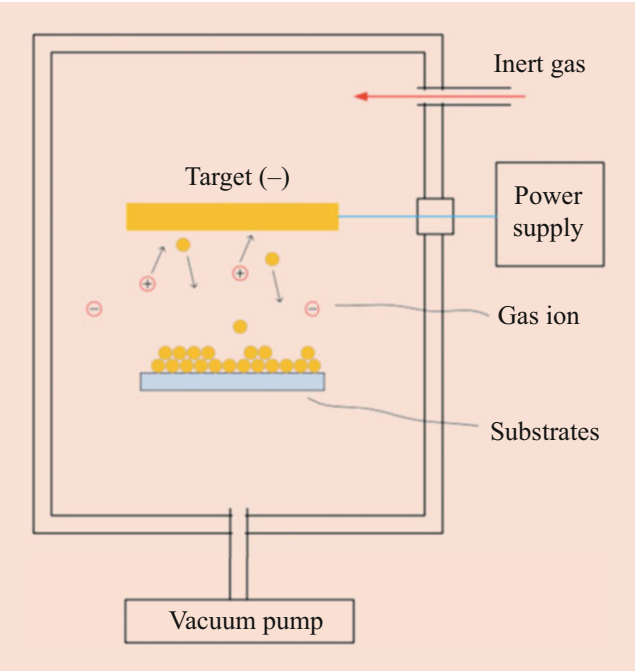

Fig. 27.6 A typical sputtering system

which is leading a porous sample. The gas used can also include some reactive gas, such as oxygen and nitrogen, and therefore sputtering can be used for amorphous metal oxide semiconductor deposition.

Chemical Vapour Deposition

Chemical vapour deposition (CVD) is a process in which films of materials are deposited from the vapour phase by the decomposition of chemicals on the surface of a substrate [69]. Contrary to thermal evaporation and sputtering, chemical vapour deposition involves chemical reactions, which can be enhanced by photo or plasma. For plasma-enhanced CVD (PECVD), the plasma is generated by radiofrequency or direct current discharge between two electrodes. The two electrodes are generally two metal plates, by which the substrate is sandwiched for material depositions. For PECVD system, it is essential that the distance between the two electrode plates is well-controlled to maintain a constant electrical field and therefore the plasma intensity. In addition, the flow rates of gases feeding into the vacuum chamber needs to be controlled by mass flow controllers to achieve a good gas environment and a constant mixture of gases if more than one gas is used. For TFTs, CVD is widely used for the deposition of several inorganic materials, such as amorphous silicon, silicon oxide, and silicon nitride.

Atomic Layer Deposition

Atomic layer deposition is a subclass of CVD. Different from conventional CVD that all the precursors are filled into the chamber simultaneously, only one gas precursor is present at each cycle of ALD to deposit materials atomically, as shown in Fig. 27.7. Generally, ALD involves at least two precursors. For example, the deposition of aluminium oxide (AlO_x), one of the most widely used materials by ALD, generally uses trimethylaluminium (TMA) and water (H_2O). During the TMA cycle, TMA gas is filled in the vacuum chamber, and some of the ethyl groups in TMA are dissociated so that the surface of substrate is covered by $Al(CH_3)_2$. During the H_2O cycle, the ethyl groups react with the H_2O molecules, leaving the surface of substrate covered by hydroxyl groups that can react with TMA for the next cycle. It is important that between each of the two gas cycles, the chamber is purged with an inert gas, such as argon, to avoid undesired reaction in the chamber and exhaustion gas line. Due to the nature of ALD, the coverage and the uniformity of deposited films are good, but the process is slow. To increase the deposition speed, a spatial ALD system with inert gas curtains was invented [70]. In this spatial ALD system, two precursors are always present in the chamber but separated by an inert gas curtain, and the substrate swings between the two spaces that contain different gases. Since the substrate can swing faster than the purge cycles in the conventional ALD systems, the deposition speed can be greatly enhanced.

Printing Techniques

In the past, printing was a method that was used to transfer a layer of ink from a stamp to a substrate [71]. In contrast to

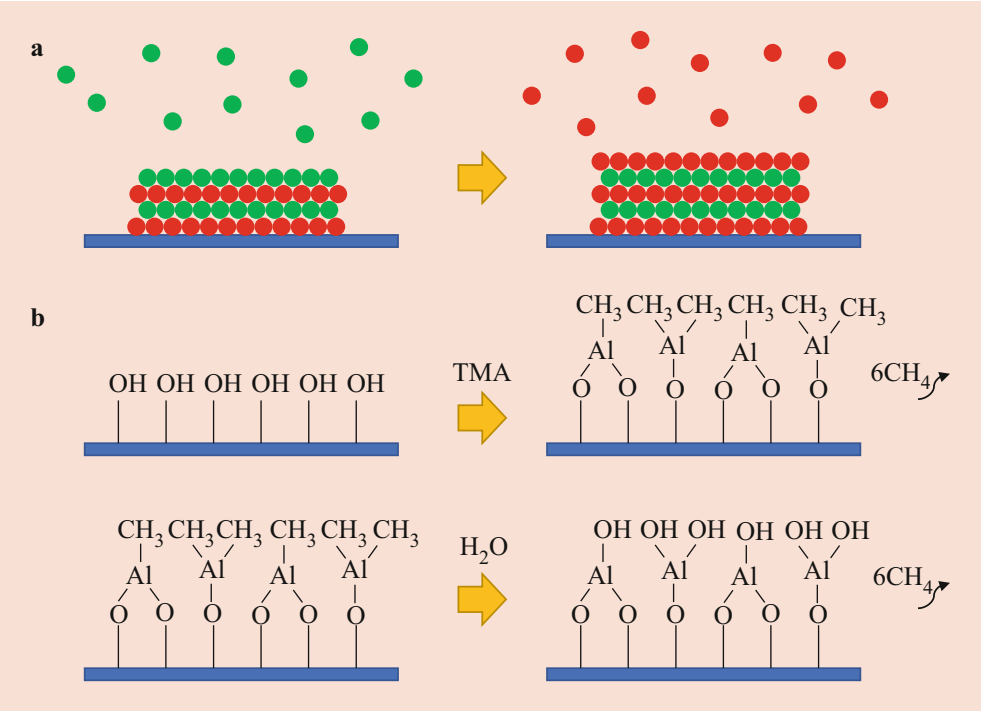

Fig. 27.7 (**a**) A schematic of ALD. (**b**) An example of the ALD of aluminium oxide

coating techniques, which simply involve pouring or casting materials over a surface, printing can provide more complex patterns (see Fig. 27.8). For the fabrication of electronic devices, patterning electronic materials is important to achieve integrated films and patterns that can function as an electronic device. For conventional fabrication of electronic devices, i.e. silicon MOSFETs, the wastage of materials is huge, since all the material deposition processes involve photolithography. In a typical photolithography process, a layer of a material is deposited and covers the whole substrate, and the unwanted areas are removed afterwards to form the desired patterns. Compared to photolithography, printing is more straightforward, and the patterning of materials can be achieved by the so-called direct patterning, i.e. depositing materials only on the wanted areas. In this way, material wastage can be greatly reduced. Therefore, printing techniques are suitable to meet the low-cost requirements of TFT fabrication for bio-applications, where low fabrication cost and negligible material waste are important criteria. Regarding TFT technologies, here we focus on printable organic TFTs, which have better compatibility with printing technologies and better mechanical flexibility as previously mentioned.

Inkjet Printing

Inkjet printing is the most promising printing technique which can produce high-resolution two-dimensional patterns. An inkjet printer consists of a cartridge and a printhead [72]. The cartridge contains ink and supplies the ink to the printhead. The printhead is a sophisticated micro-scale system which pumps the ink through nozzles to form jetted droplets, as shown in Fig. 27.9a. The printhead is designed to be resistant to organic solvents, which allows a wide range of solvents for ink formulation, and therefore the inkjet printing technique is compatible with various printable materials. Inkjet printing has several advantages, including good resolution, little material waste, the potential for customization, and no contact between the printhead and substrate [73]. These advantages are highly beneficial for printed electronics. Currently, inkjet printing for commercial electronics is still very limited, and most of the work is at the research and development or prototype level.

Screen Printing

Screen printing consists of a screen of woven material and a squeegee, as shown in Fig. 27.9b. The pattern of screen is obtained by partially filling the screen with an emulsion, which prevents ink from contacting the substrate. The open area without emulsion allows ink to go through, by which the deposited material is patterned. During printing, the screen is filled with ink, and the squeegee then forces the screen to contact the substrate to produce the pattern. Screen printing is currently widely used in industry for simple patterns, such as printing etch resists, and for complex patterns such as printing conductors for flexible electronics [71]. It can also be fully adapted to a roll-to-roll process with a rotary screen.

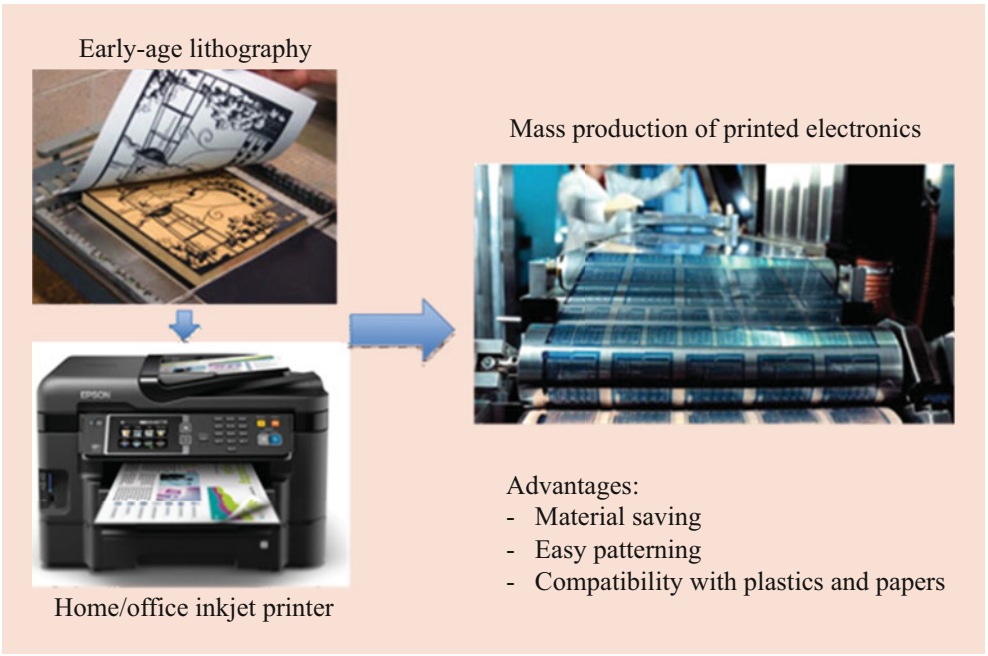

Fig. 27.8 From printing documents to printing electronics. (Adapted from [1])

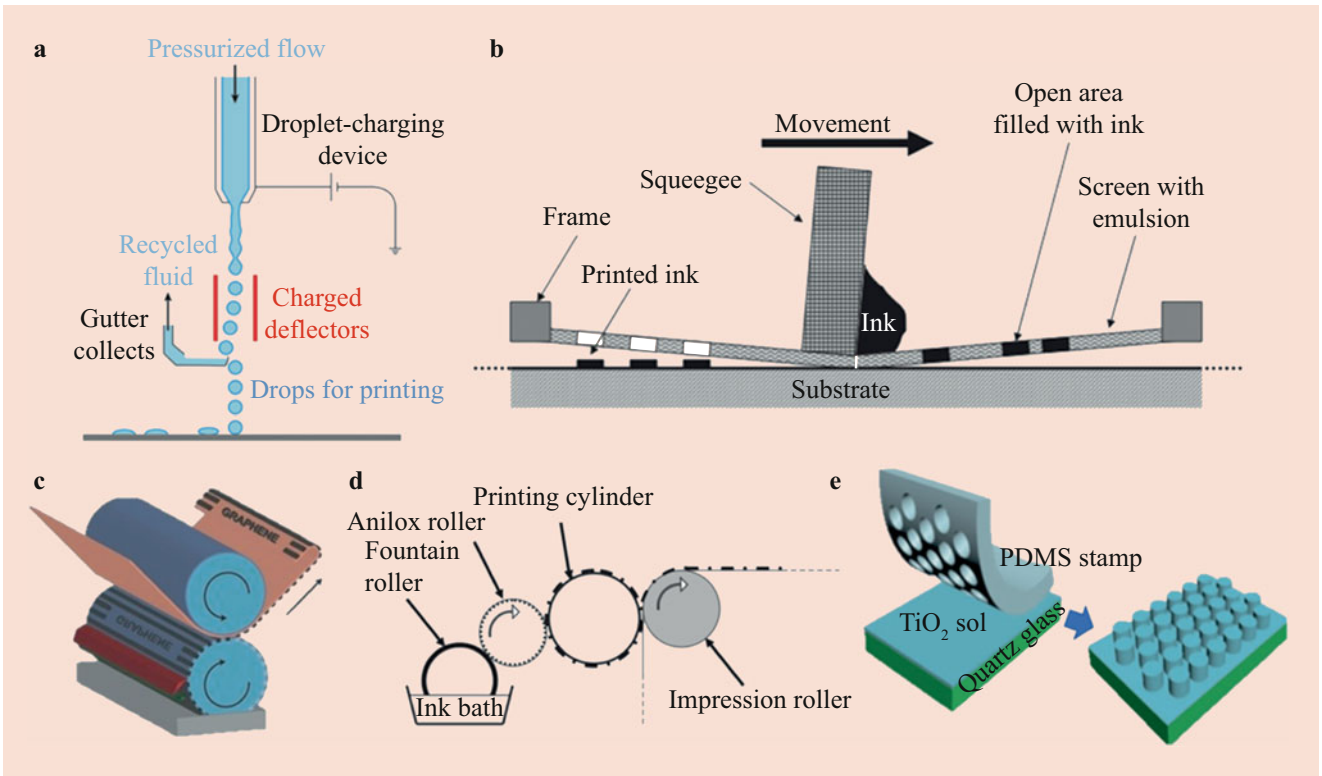

Fig. 27.9 Schematics of different printing techniques: (**a**) inkjet printing. (Adapted from [72]); (**b**) screen printing. (Adapted from [71]); (**c**) gravure printing. (Adapted from [74]); (**d**) flexographic printing. (Adapted from [71]); (**e**) nano-imprinting. (Adapted from [75])

Gravure Printing

The gravure printing technique is increasingly complex as it offers high-speed, roll-to-roll deposition of functional materials at high resolution [76]. The process consists of a two-roller system, where the printing roller has engraved patterns [74], as shown in Fig. 27.9c. The printing roller is partly immersed in the ink bath, so that the ink can be continuously refilled. The excess ink is doctored off the

printing roller to prevent accumulation in undesired areas. Since the printing roller makes strong enough contact with the rubber supporting roller, the ink in the gravure is transferred from the substrate to form patterns. The disadvantage of gravure printing is that it requires a new costly engraved roller to change new patterns. The advantage is that the web speed can be 1–10 m/s, which meets the requirement of the roll-to-roll process [71]. Gravure printing has been used in printing organic and inorganic photovoltaics [77, 78], and it has potential in conductive inks, RFID tags, and logic and memory circuits [71].

Flexographic Printing

Flexographic printing is similar to gravure printing, except that the ink is on the convex area of the printing cylinder/roller rather than in the concave area. In this case, in order to avoid excess ink, an anilox roller is used to refill a measured amount of ink into the printing cylinder, as shown in Fig. 27.9d. Therefore, a typical flexographic printing system is a four-roller system, containing a fountain roller, an anilox roller, a printing cylinder, and an impression roller. The process is simple, and the only requirement is that the inks should be less volatile. Flexographic printing has potential in smart packaging [79], transparent conductive films [80], logic circuits [81], etc.

Imprint and Nano-imprint

Imprint achieves patterning by physically deforming a deposited thin-film resist material through a micro-/nanostructured mould [75, 82]. The resist material can be thermal or UV-curable [81]. For example, as shown in Fig. 27.9e, a UV-curable material is deposited on a quartz substrate and then deformed by the mould. After UV exposure, the deformed layer is fixed with a pattern formed by the mould. Though the process is simple, it can produce patterns with good definition and high resolution, which are determined by the mould. The disadvantages of imprinting are air bubbles and ink sticking [83]. When the mould imprints the resist film, some areas make contact at the end, which can induce some air bubbles within these areas. The de-moulding process may also cause damage to the patterned layer, since the material though cured can still stick to the mould.

Comparison Among Different Printing Techniques

Due to different printing principles, these printing techniques can result in various qualities and features of printed patterns. Table 27.2 shows the comparison of the features of the printing methods. Among these printing techniques, imprint yields the highest resolution of <1 μm, which is attributed to the high-resolution mould used in imprinting. In addition, imprint does not have requirements for ink viscosity, thus allowing a wide range of choices for ink formulation.

Table 27.2 Comparison of the features of different printing methods

Printing method	Ink viscosity (mN m^{-1})	Line width (μm)	Line thickness (μm)	Speed (m min^{-1})
Screen	500–100,000	30–50	5–100	50–150
Inkjet	1–100	30–50	0.1–1	1–500
Gravure	100–1000	10–50	0.1–1	1000
Flexographic	50–500	45–100	<1	500
Imprint	–	0.01	0.1	Slow

However, the drawback of imprint is its slow printing speed. Flexographic and gravure printing techniques can provide similar feature sizes of several tens of microns and have similar requirements for ink viscosity, due to their similar printing principles. Screen printing requires very high viscosity of inks (>500 mN m^{-1}), and thus the selection of inks is limited. In addition, screen-printed features are very thick, i.e. >5 μm, which is not appropriate for printed dielectrics whose thickness is around 100 nm. As for inkjet printing, it can produce a similar resolution to most printing techniques (except imprint), and it does not require inks to be highly viscous. Therefore, inkjet printing is a good choice as a printing technique for TFT fabrication. In addition, inkjet printing has the crucial advantage that its customization capacity is high. The research and development of organic TFTs in laboratories or startups use trial and empirical patterns of devices, so it is important that the printing technique provides flexibility in pattern designs. This flexibility enabled by inkjet printing can save a considerable amount of time and money, compared to other thin-film deposition techniques which need masks, moulds, or gravures.

Ink Formulation and Printability

For inkjet printing technology, the critical part is the ink. The quality of the ink can greatly affect the reliability of the jetting droplets and the printed patterns. In this section, the chemistry and physics of inks are reviewed. Different types of ink and the compositions of ink are introduced, including the differences between different types of ink and how the composition of ink affects the properties of the inks. The fluid physical properties of ink are also reviewed, indicating how different physical parameters of ink can influence its printability.

Ink Types

In general, according to the liquid carrier medium, inks can be classified into two systems: aqueous-based inks and non-aqueous-based inks. The liquid carrier medium determines the basic properties of inks, including viscosity, density, and surface energy [84] (see Fig. 27.10). These three properties influence the printability of inks, and therefore, it is important to understand the differences between these two ink systems.

Aqueous-based or water-based inks are typically composed of 60–90% deionized water [85], which serves as the

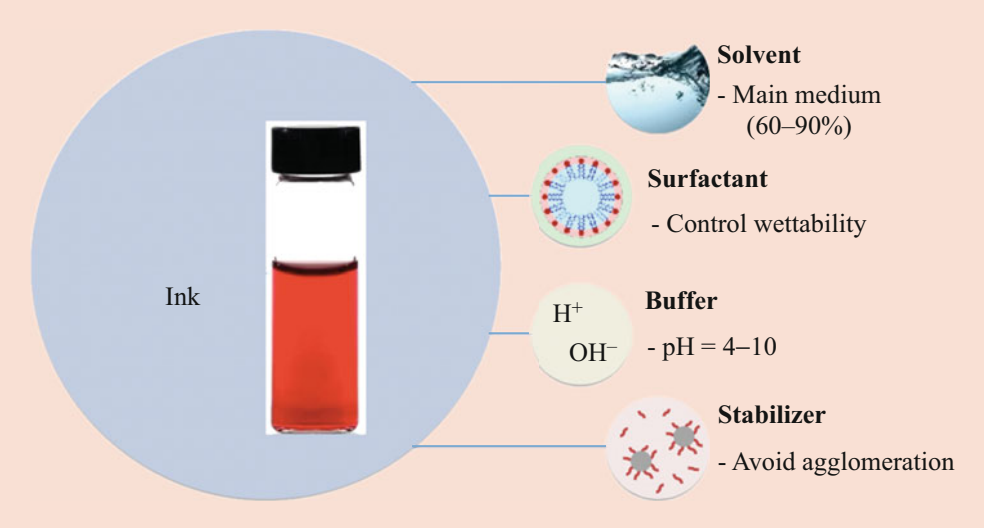

Fig. 27.10 Compositions of ink. (Adapted from [1])

carrier medium. According to the nature of water, aqueous-based inks have lower viscosities and higher surface energies compared to non-aqueous-based inks [86]. In aqueous-based inks, these properties can be engineered to meet the requirements through the addition of co-solvents, such as glycol, glycerin, and alcohols [84]. Since deionized water and co-solvents take up approximately 90% of the compositions [85], aqueous-based inks generally have many advantages, such as the use of easy-to-handle and cheaper source materials, as well as low flammability and low toxicity of the waste materials [87]. However, the drying mechanism of aqueous-based inks on non-paper substrates (e.g. glass) is based on the evaporation of water, which results in a relatively low drying rate. In addition, the high surface energies of the aqueous-based inks can cause less effective wetting on substrates.

Non-aqueous-based or solvent-based inks are based on organic solvents, which can be ketones (e.g. toluene), glycol ethers (e.g. diethylene glycol monoethyl ether acetate), and a mixture of alcohols (e.g. ethanol, isopropanol, ethylene glycol) [84,88]. These groups of organic solvents are volatile, so they can readily evaporate even at room temperature. Therefore, non-aqueous-based inks are widely used in industrial fabrication. However, although a fast drying rate is desired to obtain quick fixation of the inks and to print multilayer materials, it is somewhat undesirable that these inks evaporate so rapidly at the printheads, causing the nozzles to possibly clog [84]. Therefore, during ink formulation, organic solvents with higher boiling points may be preferred to avoid clogging of the nozzles.

Compositions of Ink

In order to improve the printability and reliability of inks, some additives are added into the inks, including humectants, viscosity modifiers, surfactants, pH buffers, stabilizers, etc. [85, 88].

Among the additives mentioned above, humectants, viscosity modifiers, and surfactants contribute to modifying the physical properties of inks. Humectants can lower the drying rate of inks; thus, inks do not dry at nozzle/air interface, and the clogging of nozzles can be avoided. The viscosity modifiers are co-solvents whose viscosities are different from the liquid carrier medium, so the viscosity of inks can be modified to meet the requirements of printing processes. Surfactants are additives that can change the surface energy of inks. The surface energy of inks not only affects the printability and the reliability of inks, but it can also influence the wetting of inks on the printed substrates [89]. In general, for a piezoelectric inkjet printer system, the surface energy and the viscosity of inks at operating temperature should be between 28–70 mN/m and 1–12 cPs, respectively [85, 90]. Buffers serve to adjust the pH of inks, which is preferred to be in a range of 4–9 to prevent printhead from corrosion and damage. These buffers can be organic or inorganic acids and bases, depending on the ink types and the pH of the original inks [88].

Stabilizers are additives that can enhance dispersion and storage time of inks. In general, for nanoparticles, stabilizers can enhance dispersion or prevent agglomeration through two approaches: electrostatic repulsion and steric repulsion [91]. Steric repulsion stems from the interaction between the capping ligands that are bound to the nanoparticles surfaces, while electrostatic repulsion results from the repulsion of charged stabilizer molecules that are chemisorbed on the surfaces of nanoparticle [91, 92]. There are different groups of stabilizers, including thiols [93, 94], citrates [95–97], carboxylic acids [98, 99], polymers [96, 97], etc. For printed

Table 27.3 Boiling point, surface energy, and viscosity of common solvents

	Boiling point (°C)	Surface energy (mN/m)	Viscosity (cPs)	Density (g/cm^3)
Deionized water	100	72.8	0.1	1.000
Ethanol	78	20.6	1.26	0.789
2-methoxyethanol	125	27.2	0.16	0.965
Glycerol	182	64	853.1	1.26
Ethylene glycol	198	48.5	1.9	1.11
Diethylene glycol	244	44.8	35.7	1.12
Toluene	110	27.9	0.06	0.867
Hexane	69	18.4	0.03	0.655
Tetradecane	253	26.6	0.22	0.765
Anisole	155	35	1.52	0.996
PGMEA	146	30.4	1.1	0.969

TFTs, however, additives may become impurities, in particular in dielectrics and semiconductors. Therefore, during ink formulation for printed TFTs, additives need to be carefully chosen and even avoided.

Fluid Physical Properties of Inks

Fluid physical properties of functional inks are essential for the stable and reliable performance of an inkjet printing system, including viscosity, density, and surface energy. Among these three parameters, viscosity and surface energy can strongly influence the fluid dynamics during jetting droplets [84]. Highly viscous inks are difficult to jet out of the nozzles, and thus the solutes of the inks may aggregate or agglomerate at the nozzles. In an advanced inkjet printer, the temperature of inks at the nozzles can be heated up to lower the working viscosity of the inks. In terms of surface energy, if it is too high, drops are more difficult to generate, and satellite droplets may form; if it is too low, droplets are easier to generate, but the tails of the droplets are long. The long tails are undesirable, since they may connect nozzles to the substrate and affect the precision of the droplet landing positions [100]. The physical properties of some commonly used solvents are shown in Table 27.3. Comparing these solvents, it can be seen that ethanol, ethylene glycol, anisole, and propylene glycol monomethyl ether acetate (PGMEA) meet the surface energy and viscosity requirements. Though these three properties influence inks differently, they have a combined effect on the printability of inks [101]. The behaviour of fluids can be evaluated by the Reynolds number (*Re*) and the Weber number (*We*), which are the ratio of inertial to viscous forces and the balance between inertial and capillary forces, respectively [102]:

$$Re = \frac{\upsilon\rho\alpha}{\eta} \tag{27.1}$$

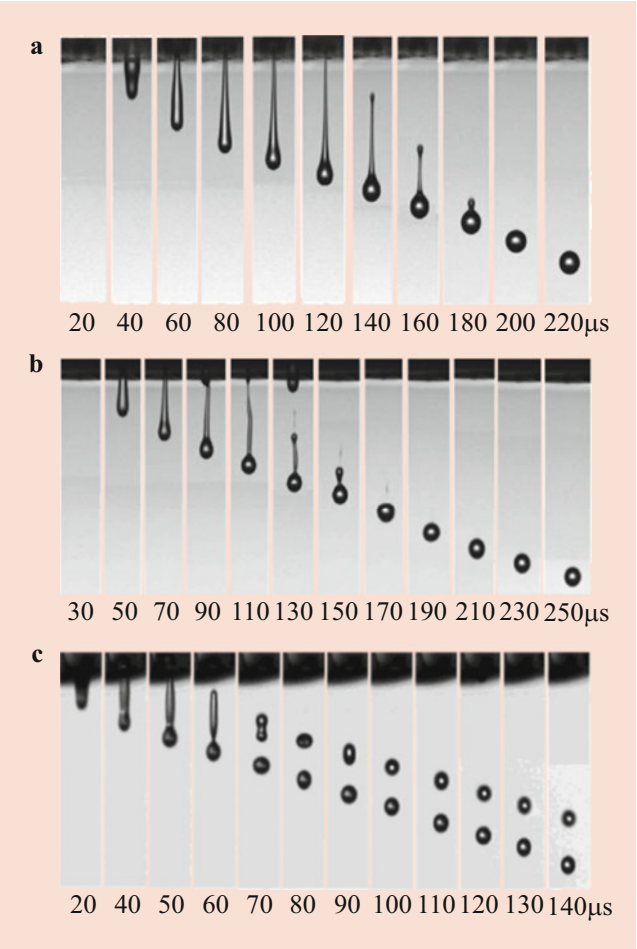

Fig. 27.11 Representative photo sequence of drop formation for fluids with values of (**a**) $Z = 2.17$, (**b**) $Z = 4.08$, and (**c**) $Z = 17.32$. (Adapted from [100])

$$We = \frac{\upsilon^2\rho\alpha}{\gamma} \tag{27.2}$$

where υ is the fluid velocity, α is the drop diameter, ρ is the drop density, γ is the surface energy of ink, and η is the viscosity of ink. The Ohnesorge number (Oh) is another useful dimensionless number to predict the printability of inks. The Ohnesorge number is independent of fluid velocity and defined as follows:

$$\mathrm{Oh} = \frac{\sqrt{We}}{Re} = \frac{\eta}{\sqrt{\gamma\rho\alpha}} \tag{27.3}$$

Therefore, the Ohnesorge number can be determined without the actual printing conditions, while the Reynolds and Weber numbers cannot be determined without the actual printing conditions.

The inverse of the Ohnesorge number, known as Z number, is widely used to evaluate the printability of inks [84]. Based on a simple model of fluid flow and numerical anal-

ysis, Fromm proposed that the requirement to form stable droplets is $Z > 2$ [103]. Reis and Derby improved this result by computational fluid dynamics simulations and pointed out that the Z value should be in a range of between 1 and 10 [104]. Later, Jang et al. experimentally defined a printable range as $4 \leqslant Z \leqslant 14$, by mixing water and different alcohols with different ratios and then characterizing the single droplet formability, positional accuracy, and maximum allowable jetting frequency of different mixtures of solvents [100].

Figure 27.11 shows the droplet formation for fluids with different Z values. As seen in the figure, when $Z < 4$, the droplet tends to generate a long tail; when $Z > 14$, the droplet tends to generate a satellite [100]. However, neither the tail nor the satellite is desirable for a droplet to be printed on the substrate, since they could distort the printed pattern in comparison to the design. Therefore, in order to achieve a printable ink, these physical properties of inks require investigation.

27.1.3 Printable and Flexible Transistors

TFT Device Architectures

In general, there are four possible TFT device architectures, including bottom-gate bottom-contact (coplanar), bottom-gate top-contact (staggered), top-gate bottom-contact (inverted staggered), and top-gate top-contact (inverted coplanar) structures, as seen in Fig. 27.12.

For flexible electronics with ultra-low-power consumption, the operating voltages of organic TFTs should be low, which can be achieved by reducing defects/traps in TFTs. For low-voltage TFTs, the semiconductors should be crystallized, and the semiconductor/dielectric interfaces should be smooth. These factors need to be taken into consideration when selecting TFT device architectures. For organic semiconductors, small molecules are much more likely to crystallize compared to polymer semiconducting materials, thereby reducing the density of defects or traps in the bulk of the semiconductor. However, the issue of using a small-molecule semiconducting material is that it tends to generate a rough surface, on which, if a gate dielectric is deposited, the semiconductor/dielectric interface trap density is significant. In contrast, polymers normally demonstrate smooth surfaces, which can be used as a base for the semiconductor/dielectric interface to reduce the interface trap density. As a result, it is preferred if the semiconductor is deposited on top of a smooth polymer gate dielectric. In other words, a bottom-gate structure is preferred. In addition, small-molecule semiconductors are more vulnerable to heat with regard to the reorganization of crystals and even evaporation. The source/drain electrodes (which need high-temperature annealing) should be deposited prior to the deposition of the semiconductor. Therefore, to achieve printable low-voltage organic TFTs, the bottom-gate bottom-contact structure is preferred, while regarding materials, small-molecule semiconductors and polymer gate insulators are preferred.

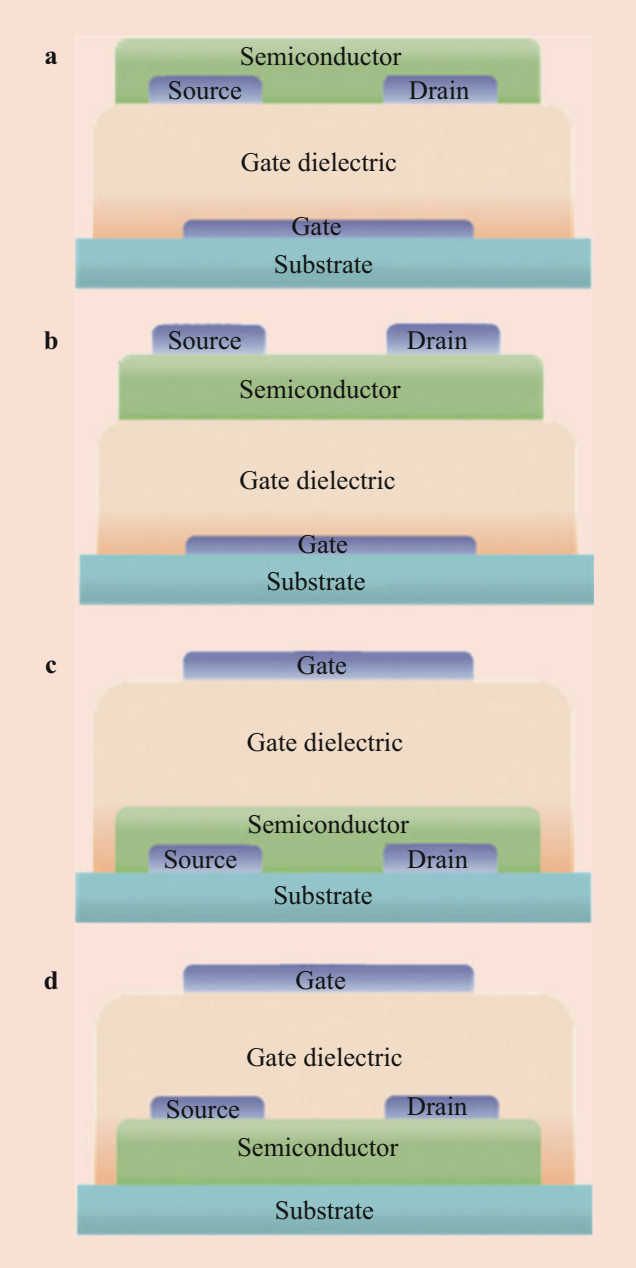

Fig. 27.12 Schematic diagram of the four TFT device architectures: (**a**) bottom-gate bottom-contact, (**b**) bottom-gate top-contact, (**c**) top-gate bottom-contact, and (**d**) top-gate top-contact. (Adapted from [1])

In fact, other device architectures also have advantages. Staggered and inverted staggered architectures can greatly reduce contact resistance between the semiconductor and source/drain electrodes [105]. In these two architectures, charge carriers are not only injected from the edge of the source electrode but also from the area of the electrode that

is overlapped with the gate electrode. Top-gate architectures allow self-aligned TFTs, which use source/drain patterns to define gate pattern [106] or vice versa [107]. In self-aligned TFTs, the overlap between source/drain electrodes and gate electrode is small, and therefore, parasitic capacitance is reduced. Noh et al. demonstrated self-aligned all-printed polymer TFTs with parasitic overlap capacitance to values as low as 0.2–0.6 pF/mm and cutoff frequencies of f_T = 1.6 MHz [106].

Issues of Printed Organic TFTs

The main issues in organic TFTs (either vacuum- or solution-processed) are the high operating voltage and poor stability, specifically short shelf-life time and significant threshold voltage shift under bias stress. The most straightforward way to lower the operating voltage is to increase unit-area gate capacitance, which can be achieved by an ultra-thin dielectric layer [59] or a high-k dielectric material [108]. However, a thin gate dielectric can result in large gate leakage in all-printed organic TFTs, while organic TFTs based on a high-k gate dielectric could suffer from the interface dipole disorder [109], inducing instability. Alternatively, operating voltages can be lowered by reducing semiconductor/dielectric interface traps. This method offers another advantage that due to the reduced traps, organic TFTs can be more stable with regard to shelf-life and bias stress [110]. However, printed thin films are not as good as vacuum-processed thin films, with regard to the defects and surface roughness of the films. These can significantly generate a considerable number of traps and are the key challenges that need to be tackled.

Instability prevails in most organic TFTs, either vacuum-processed or solution-processed. The instability of organic TFTs can be attributed to intrinsic (e.g. structural and energetic disorder in the semiconductor) and extrinsic (e.g. oxidation, presence of moisture, and chemical impurities) factors [111, 112]. These can induce degradation of device performance during storage in the ambient environment and a threshold voltage shift of the organic TFTs under electrical bias stress [113]. During bias stress, trapped charged can be created in the dielectric (which holds the high electric field) and at the semiconductor/dielectric interface (where charge carriers transport). In order to achieve highly stable all-printed organic TFTs, it is important that:

- there are few defects in the organic TFTs, in particular, in the bulk semiconductor, in the dielectric, and at the semiconductor-dielectric interface;
- organic TFTs are encapsulated to avoid material oxidation;
- materials used are water-proof but organic solvent-like, which avoid moisture while making printing possible.

Besides challenges regarding organic TFTs, there are particular issues associated with the inkjet printing technique and all-printed organic TFTs. Among all the electronic components, transistors have the most complex structure, compared to resistors, capacitors, and diodes. For a typical organic TFT, there are at least four layers stacked together, and each of these layers should be of good quality in order to form a functional device. In previously reported all-inkjet-printed organic TFTs, only one piece of work provides statistical analysis of the fabricated devices, depicting a low proportion of functional devices (34%) as compared to defective devices (Fig. 27.13) [52]. The defective organic TFTs depict atypical

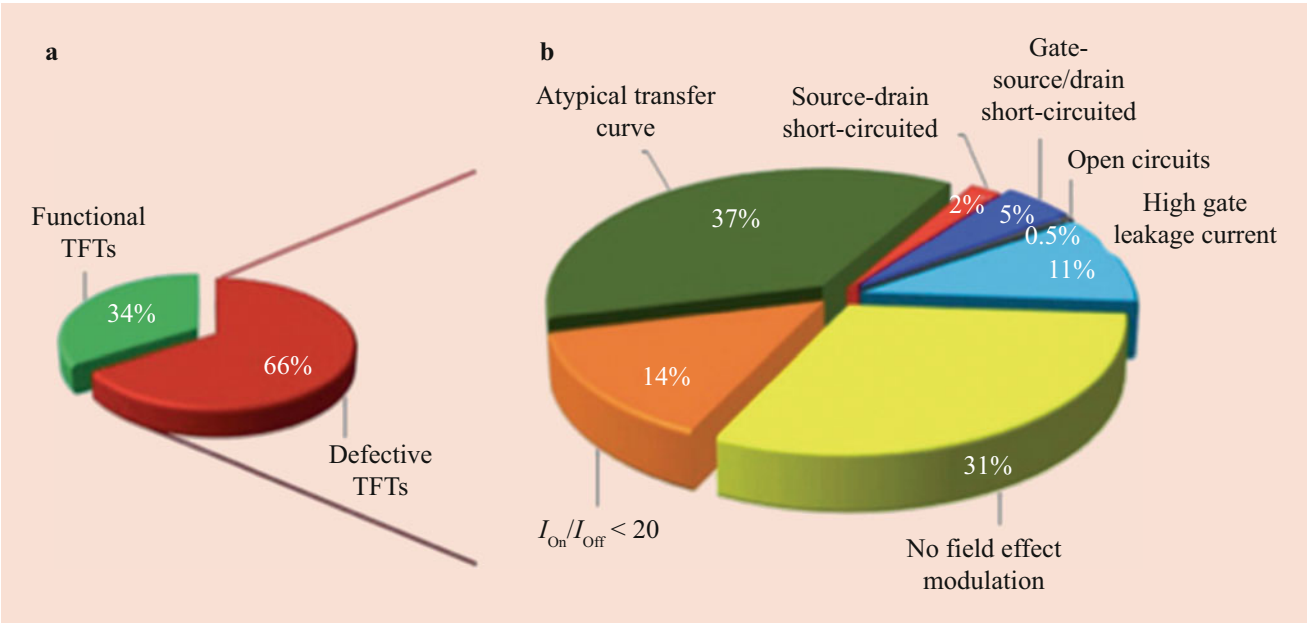

Fig. 27.13 The proportion of functional TFTs to defective OTFTs. (Adapted from [52])

transfer curves, source/drain short circuits, gate-source/drain short circuits, open circuits, high gate leakage current, no field-effect modulation, and a low on/off ratio. The reasons for the failures can be categorized into wetting, satellite drops, droplet jetting oddness, dirt and dust particles, as well as missing droplets [114]. Therefore, in order to improve the yield and device performance of all-inkjet-printed organic TFTs, it is essential to ensure that:

- the jetting properties of inks are in good condition, e.g. without satellites;
- the materials used have adequate compatibility, with regard to wetting;
- the quantities of dirt and dust are as small as possible.

Developments in Printable Organic TFTs

Methods of Organic Semiconductor Deposition

In previous work on solution-processed/printable organic TFTs, most interest has centred on semiconductor materials. In the early years (2000s) of developing solution-processed organic TFTs, most work used silicon wafers as the substrate, utilizing highly doped silicon as the conductive gate and thermally grown SiO_2 as the gate dielectric layer [115–117]. However, due to the poor interface between SiO_2 and the organic semiconductor materials, self-assembled monolayers (SAMs) were grown on the SiO_2 to facilitate charge transport at the semiconductor/dielectric interface [118], such as octadecyl-, decyl-, and butyltrichlorosilane (OTS, DTS, and BTS). At that time, typical solution-processable organic semiconductor materials were P3HT (polymer) [111, 119] and TIPS-pentacene (small molecule) [41, 120], and the mobility of the fabricated organic TFTs was low, generally less than 0.1 $cm^2V^{-1}s^{-1}$.

Since polymer semiconductor materials are amorphous, it is not easy to control the crystallization of the materials. In contrast, small-molecule materials can crystallize, and therefore, in the past decade, significant effort has been made to grow highly crystallized organic semiconductor materials, using drop casting [110, 123] and blade coating [118, 122, 124]. Optical polarized photos of TIPS-pentacene thin films deposited through these techniques are shown in Fig. 27.14. Compared to spin-coated TIPS-pentacene thin films, where crystals are randomly distributed [121], the crystallization of TIPS-pentacene in these advanced techniques is well aligned. In terms of drop casting, by using a tilted angle to guide the flow of the semiconductor solution, the crystallization direction of TIPS-pentacene also follows the flow direction, so

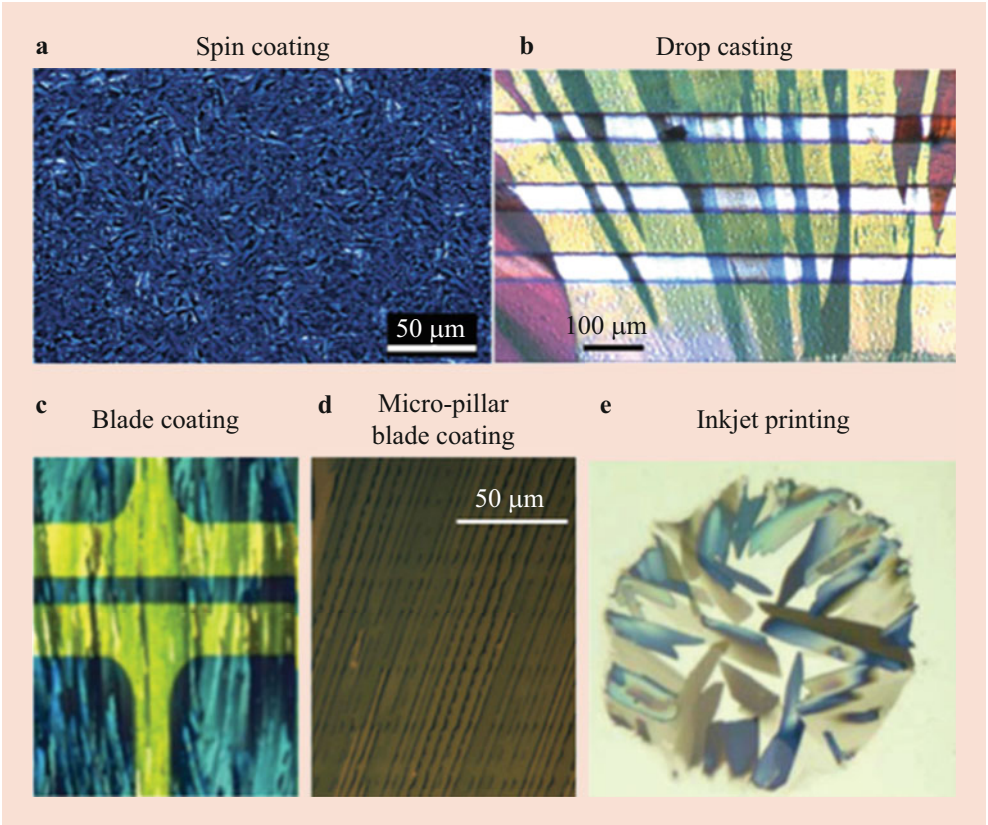

Fig. 27.14 Optical microscopy images of TIPS-pentacene thin films with various morphologies deposited by different techniques: (**a**) spin coating. (Adapted from [121]); (**b**) drop casting. (Adapted from [110]); (**c**) blade coating. (Adapted from [118]); (**d**) solution coating (micro-pillar blade coating). (Adapted from [122]); (**e**) inkjet printing. (Adapted from [117])

that the mobility of the fabricated organic TFTs is improved to around 1 $cm^2V^{-1}s^{-1}$ [125]. However, in most of cases, drop casting is a manual process, so repeatability and precise controlling of this process are the main challenges. For blade coating, the crystallization direction is also defined by the movement of the blade, and the mobility of the organic TFTs is over 3 $cm^2V^{-1}s^{-1}$ [118]. In addition, using a micropillar-patterned blade, an approach termed fluid-enhanced crystal engineering (FLUENCE), highly aligned single crystals of TIPS-pentacene can be achieved, resulting in a high mobility of 11 $cm^2V^{-1}s^{-1}$ [122]. However, the issue of blade coating is that this process does not allow patterning at the same time, so a further subtractive process is required.

In order to achieve better material usage and direct patternability, the inkjet printing of TIPS-pentacene has also been reported [53, 62, 115–117, 125–128]. Though highly crystallized TIPS-pentacene thin films can be achieved, the alignment is hard to control (Fig. 27.14e) [117]. To solve this issue, off-centre printing has been proposed [128]. Due to the better crystallinity of TIPS-pentacene at the off-centre area compared to the centre area (as seen in Fig. 27.14), the channel area can be covered by well-aligned TIPS-pentacene crystals by using the off-centre printing technique [128]. However, this technique depends on good control of the off-centre positions. To enhance the crystallinity of TIPS-pentacene thin films, polymer binders have been blended into the semiconductor ink, such as polystyrene (PS), poly(α-methyl-styrene) (PαMS), and amorphous polycarbonate (APC) [62, 116, 126]. In comparison to the work solely using TIPS-pentacene [53, 115, 117, 125, 129], the TIPS-pentacene/polymer blends facilitate TIPS-pentacene crystallization, and the fabricated organic TFTs exhibit a higher mobility, a higher on/off ratio, and a lower operating voltage.

Solution-Processable Organic Semiconductors

In addition to significant developments in semiconductor deposition processes, considerable attention has been focused on new solution-processable semiconductor materials. TIPS-pentacene is a derivative of pentacene. In the family of acenes, there are many derivatives that are solution-processable and printable, such as 6,13-bis-(triethylsilylethynyl)pentacene (TES-pentacene) [130] and 2,8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TES-ADT) [118]. These semiconductor materials, when highly crystallized and well aligned, generally exhibit a mobility of around 1 $cm^2V^{-1}s^{-1}$. In addition to the functionalized acenes, in the recent years, small-molecule thiophene-based materials have been popular, such as 2,7-alkyl [1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT) and 2,9-alkyl-dinaphtho [2,3-b:2′,3′-f]thieno[3,2-b]thiophene (C10-DNTT). Based on these advanced materials, organic TFTs with a high mobility have been achieved, with a mobility of around 10 $cm^2V^{-1}s^{-1}$ [131, 132] and even as high as 43 $cm^2V^{-1}s^{-1}$ [133]. More recently, a band-like charge transporting material has been developed, 3,11-didecyldinaphtho[2,3-d:2′,3′-d’]benzo[1,2-b:4,5-b’]dithiophene (C10-DNBDT), and nanowire-based organic TFTs exhibit a high mobility of >17 $cm^2V^{-1}s^{-1}$ [134].

Organic Dielectrics

Compared to the significant development of organic semiconductor materials, there has been less interest in advancing organic dielectric materials. In general, organic dielectric materials are polymers. Among polymer dielectrics, the most popular one used in solution-processed organic TFTs is poly(4-vinylphenol) (PVP) [53, 115, 135, 136], due to the straightforward processes of PVP deposition and annealing. CYTOP is another widely used dielectric material, due to its hydrophobicity that prevents water molecules from being polarized or trapped in the dielectric, thus enhancing the stability of organic TFTs [132, 137, 138]. Though good for stability, CYTOP is rarely used in all-solution-processed organic TFTs, since the hydrophobicity of CYTOP eliminates the possibility of depositing functional materials on top of it through solution-based processes. For all-inkjet-printed organic TFTs, all previous work used PVP as the dielectric, and the mobility of the printed devices was consistently <0.1 $cm^2V^{-1}s^{-1}$. However, PVP is not a good dielectric material for organic TFTs due to its hydrophilicity that can result in instability. Recently, monopolar dielectrics were proposed as good candidates for all-printed organic TFTs [50]. In particular, Lewis-acid monopolar dielectrics are hydrophobic, thus preventing water molecules from being trapped in the dielectrics while also allowing good wetting of most organic solvents (Fig. 27.15).

All-Printed Organic TFTs

To further reduce the cost and improve the efficiency of organic TFT manufacturing, an all-printed organic TFT device platform is needed. The pioneering work on all-printed organic TFT circuits was reported by Sirringhaus et al. using all polymer materials in 2000. However, the transistors demonstrated a low field-effect mobility of 0.02 $cm^2V^{-1}s^{-1}$ and a high operating voltage of 20 V. To improve mobility, researchers replaced the polymer semiconductor by a small-molecule semiconductor, typically TIPS-pentacene, which tended to demonstrate a higher mobility [53, 62, 115–117, 125, 126, 128, 139]. However, most works on all-printed organic TFTs based on small molecules also demonstrated low mobilities of ~0.01 $cm^2V^{-1}s^{-1}$ and high operating voltages of >20 V.

In 2016, Feng et al. controlled the printing processes to reduce semiconductor/dielectric interface trap density and achieved low-voltage all-inkjet-printed organic TFTs, with a mobility of 0.26 $cm^2V^{-1}s^{-1}$ and an operating voltage of 3 V (see Fig. 27.16) [51]. However, the organic TFTs used hy-

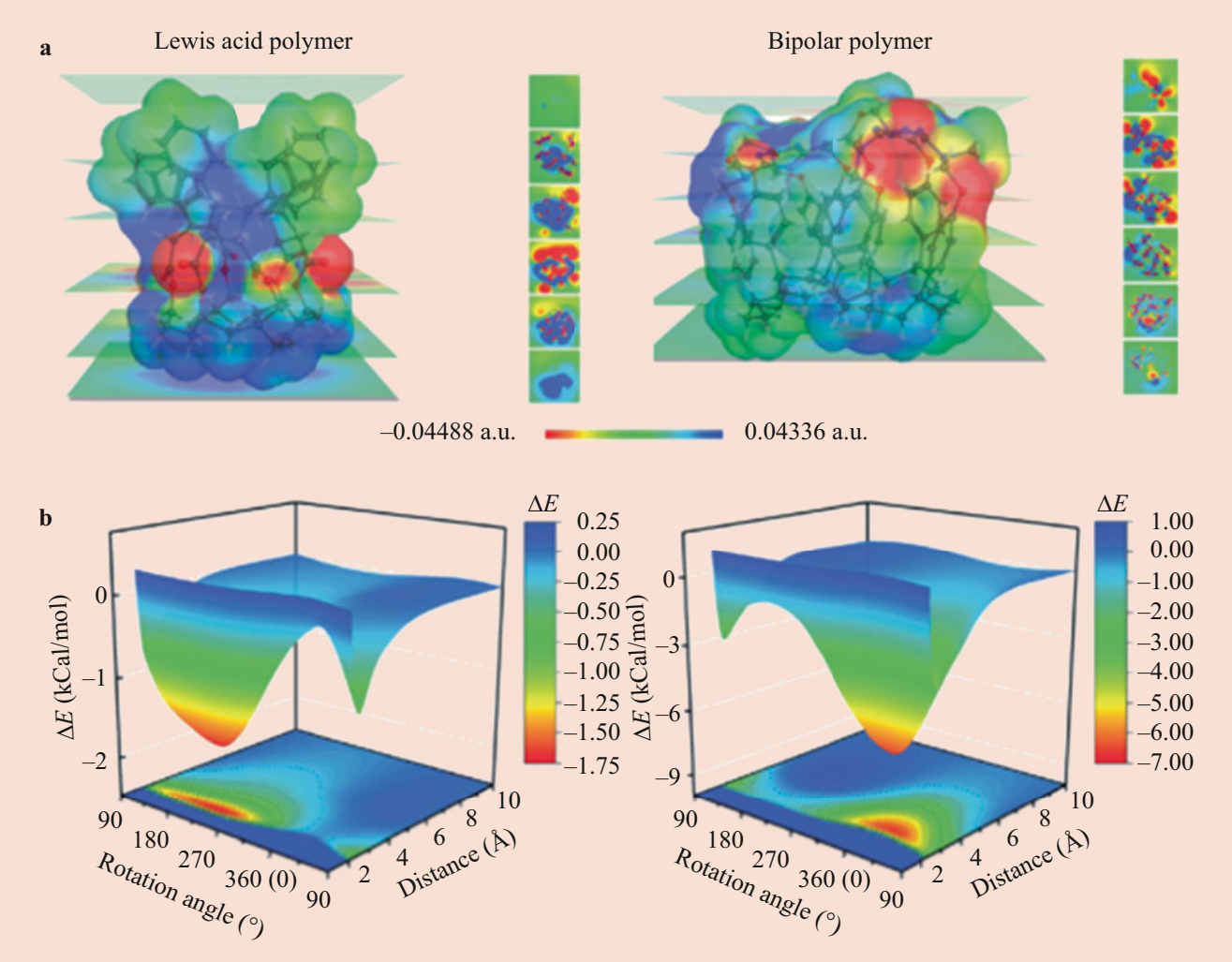

Fig. 27.15 (**a**) 3D tomographic comparison of electron densities between a Lewis-acid monopolar polymer, PVC, and a bipolar polymer, PVP. The isosurfaces and tomographic sections are coloured red (electron-rich), green (neutral), and blue (electron-poor). Different atoms in the 3D molecular structures are coloured grey (carbon), white (hydrogen), red (oxygen), and blue (nitrogen). (**b**) The interaction energy (ΔE) when a water molecule approaches PVC and PVP at different rotation angles (from 0° to 360°). (Adapted from [50])

drophilic PVP as the dielectric, which resulted in significant threshold voltage shift during bias stress [140]. To enhance all-printed organic TFT bias stress stability, Jiang et al. used a Lewis-acid monopolar dielectric, i.e. polyvinyl cinnamate (PVC), and the threshold voltage shifts were greatly reduced to 0.11 V under both positive and negative bias stress for 1 h. More recently, they used C8-BTBT as the semiconductor for all-printed organic TFTs. The printed C8-BTBT films possessed large crystals (of which grain sizes were >50 μm), and the density of states of the TFTs was reduced (i.e. deep state density was $\sim 10^{14}\,\mathrm{cm^{-3}eV^{-1}}$). Due to the large semiconductor crystals and reduced traps, the all-printed organic TFTs demonstrated a high mobility of $>1.0\,\mathrm{cm^2V^{-1}s^{-1}}$ and a low operating voltage of 1 V. In addition, the transistors exhibited good stability under ambient environment storage with threshold voltage shift of <1 mV over 3 months as well as under bias stress.

27.2 Modelling of Flexible TFTs and Circuit Design Considerations

27.2.1 TFT Compact Modelling

Computer-Aided Design

The growing maturity of thin-film transistor (TFT) technology coupled with newly emerging materials and processes is enabling integration of circuits and systems for a new family of applications ranging from biosensing systems to areas augmenting displays and imaging [28, 141–143]. The design of systems places great demand for fast computer-aided design (CAD) tools to accurately and reliably predict system behaviour [144].

CAD always requires accuracy, high speed, and reliable convergence of device models. In order to achieve high

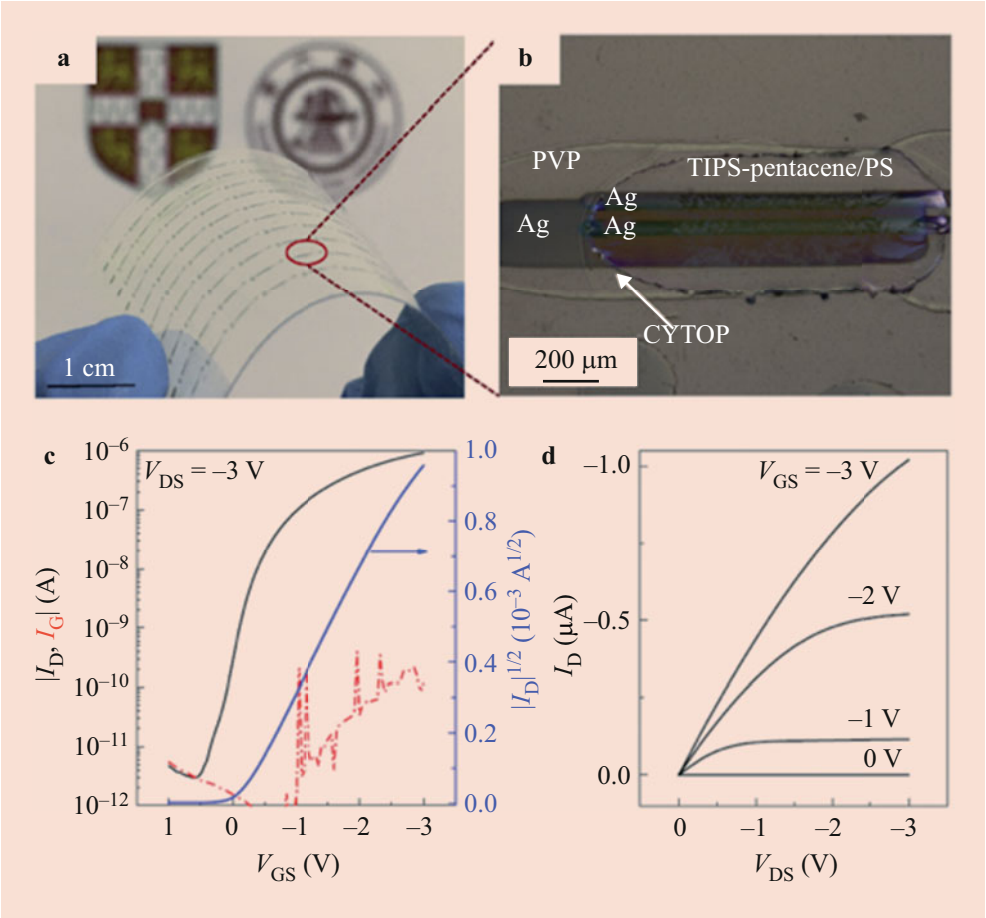

Fig. 27.16 (**a**) Photograph of the low-voltage all-inkjet-printed organic TFTs. (**b**) Polarized optical micrograph of the fabricated device. (**c**, **d**) Measured electrical characteristics of the fabricated device: (**c**) transfer characteristics (I_D–V_{GS}) and (**d**) output characteristics (I_D–V_{DS}). (Adapted from [51])

accuracy in all working regions without the use of many fitting parameters, a good understanding of device physics is needed. However, physical models are not necessarily sufficient for good CAD in the sense that the equations could be complex, which can lead to slow execution or convergence problems. Therefore, simplification of the model equations without sacrificing accuracy is one of the major requirements for a good CAD model. In addition, the model should be adaptive to a wide range of technological/process parameters through simple extraction procedures.

During the past 30 years, a great amount of effort has been made in the TFT modelling area for various semiconductor technologies, including amorphous silicon [145–151], polysilicon [150], organics [152–156], and metal oxides [157–163]. For a-Si TFTs, several SPICE models have been developed. Specifically, the model developed by Rensselaer Polytechnic Institute, also known as the RPI model [150], has become a commercial standard supported by many simulation platforms including SmartSpice, HSPICE, Spectre, etc. However, no CAD tool for organic and metal-oxide TFTs has yet become a standard due to the rapid evolution of materials and device structures.

In this chapter, we will review the major contributions to the TFT modelling area and compare the differences between Verilog-AMS and SPICE from the standpoint of compact device modelling. Finally, we present the implementation of the Cambridge TFT compact model [161] for oxide TFTs in Verilog-AMS for Spectre simulation. The major goal of this review is to give the reader guidelines for implementing device models for the CAD of circuits and systems.

Physical and Empirical Modelling

Physical and empirical modelling approaches are generally aimed at providing an accurate model for a given transistor or transistor family, which covers all working regions of the device. While the major consideration is accuracy, the developed model is not necessarily physical. In this sense, it is theoretically possible to use polynomial approximation or other empirical ways to fit any kind of transistor behaviour with acceptable accuracy. However, without a proper un-

derstanding of the underlying device physics, the resulting number of fitting parameters could be large and difficult to extract from measurements since the model should cover a wide range of different bias conditions and transistor scales. Therefore, the transistor models used in a simulator are often a combination of terms and coefficients that are physically and empirically based.

Recent efforts have primarily focused on physically based approaches in an attempt to develop simple and accurate models. The most well-studied material for TFTs is amorphous silicon (a-Si:H). Several models have been developed based on different distributions of deep states and tail states of the semiconductor to describe static and dynamic behaviour for the above and subthreshold regions [149–151]. Other properties include trap-related V_T shift [164] and the off/leakage currents [146]. The RPI model [150] captures most of the device properties leading to satisfactory simulation results and thus has been widely used.

For organic TFTs, researchers have developed models based on multiple trapping and release (i.e. trap-limited conduction) [165] and variable range hopping (VRH) [153, 166, 167]. However, due to the diverse use of materials in the TFT, the underlying physics differs, and therefore a trend has emerged to develop a model that is unified but less physical [154].

As for metal-oxide TFTs, modelling efforts are still in their infancy, although there are growing interests in the area for implementation of circuits and systems. In what follows, early efforts in compact models for CAD of oxide TFTs are reviewed.

Cambridge's TFT Model

Compared with a-Si TFTs, the oxide system has unique properties, which need to be captured. For example, localized traps or band tail states in oxides do not exist to the same extent as a-Si [160]. Their tail state density is much lower, and hence, trap-limited conduction is generally insignificant [158, 160]. In addition, more complex systems such as amorphous indium gallium zinc oxide (a-IGZO) can have compositional disorder due to the random distribution of metal constituents [158, 168]. This gives rise to potential barriers above the conduction band minima (E_m), suggesting the presence of percolation conduction [158, 160, 168].

In the following, compact models for the terminal current-voltage behaviour are presented, taking into account the different transport mechanisms in the device for the above- and subthreshold regions of TFT operation. The former is based on a mobility model that combines trap-limited conduction (TLC) with percolation conduction. The latter takes into account diffusion and drift current components [159]. A unified model is then presented that covers both regions based on a single expression that uses a reference turn-on voltage V_{on} rather than V_T [161]. Good agreement with measured terminal characteristics is obtained over the entire range of gate-source voltage (V_{GS}) > V_{on} for the test TFTs with an a-IGZO channel.

Above-Threshold Model

As illustrated in Fig. 27.17, oxide TFTs have potential barriers above E_m due to compositional disorder, suggesting percolation conduction when electrons are released into the conduction band. Moreover, there are localized tail states within the gap states, implying trap-limited conduction. In particular, oxide semiconductors can have a shallow slope of the tail states (kT_t) ~20 meV, smaller than the thermal energy (kT) at 300 K, leading to different mobility behaviour. This suggests that the field-effect mobility (μ_{FE}) model needs to be modelled based on TLC and percolation conduction, although the former is not as significant as compared to a-Si.

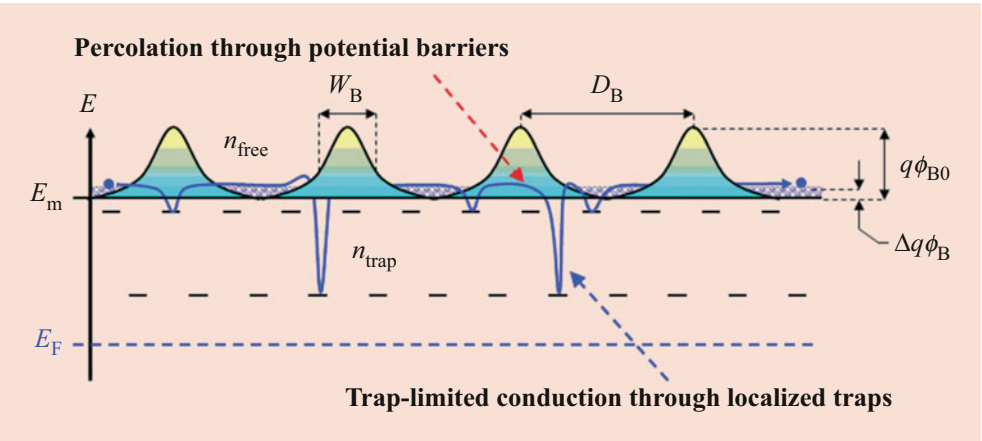

Fig. 27.17 Carrier transport combining percolation with trap-limited conduction (TLC) for oxide semiconductor TFTs (here, D_B and W_B denote spatial distance and width of potential barriers, respectively)

1. Trap-Limited Conduction (TLC)
Effect of trap-limited conduction (TLC) can be considered as μ_{FE} being proportional to ratio (γ_{TLC}) of free carrier density (n_{free}) and trapped carrier density (n_{trap}), yielding $\gamma_{TLC} = n_{free}/(n_{free} + n_{trap})$. Here, $n_{free} = N_C \exp[(E_F - E_m)/kT]$, where N_C is effective density of states in conduction band and kT the thermal energy. And the expression for n_{trap} is approximated with $kT_t < kT$ using exponential distribution of tail states. This yields $n_{trap} = N_{tc}kT_t\exp[(E_F - E_m)/kT]$, where N_{tc} is the density of trap states at conduction band edge. Now, we have γ_{TLC} as just a constant:

$$\gamma_{TLC} \equiv \frac{n_{free}}{(n_{free} + n_{tail})} \approx \frac{N_C}{N_C + N_{tc}kT_t} \tag{27.4}$$

2. Percolation Conduction
Percolation conduction associated with potential barriers above E_m can be considered as mobility scaled from band mobility (μ_0), assuming Gaussian random distribution of potential barriers with the mean (ϕ_{B0}) and the variance (σ_{B0}). This yields $\mu_0^* = \mu_0 \exp[-q\phi_{B0}/kT + (q\sigma_{B0})^2/(kT)^2]$. Here, ϕ_{B0} can be reduced by $\Delta\phi_{B0}$ due to thermally released electrons, depending on Fermi level change (ΔE_F), as described in Fig. 27.4. The thermally reduced barrier height can be expressed as $\phi_{B0}\exp(-\gamma_B \Delta E_F/kT)$, where $\gamma_B \equiv (D_B - W_B)/D_B$, which can be approximated as $\phi_{B0}(1 - \gamma_B \Delta E_F/kT)$ when $\gamma_B \Delta E_F/kT << 1$ by Taylor expansion. Thus, $\Delta\phi_{B0}$ is defined as $\gamma_B \Delta E_F/kT\phi_{B0}$. These conditions yield the percolation mobility (μ_{Per}) as follows:

$$\begin{aligned}\mu_{Per} &\equiv \mu_0 \exp\left(-\frac{q(\phi_{B0} - \Delta\phi_B)}{kT} + \frac{(q\sigma_{B0})^2}{2(kT)^2}\right) \\ &= \mu_0^* \exp\left(\frac{\gamma_B \Delta E_F}{kT}\phi_{B0}\right)\end{aligned} \tag{27.5}$$

where $\mu_0^* = \mu_0 \exp[-q\phi_{B0}/kT + (q\sigma_{B0})^2/2(kT)^2]$ considered as an effective band mobility.

3. Combined Mobility Model with V_{GS} Dependence
In Eq. (27.5), the ΔE_F is controlled by gate voltage (V_{GS}). The relationship between them can be derived by solving Poisson's equation, yielding $\Delta E_F = 2(kT/q)\ln[C_{ox}(V_{GS} - V_T)/Q_{ref}]$, where C_{ox} is gate-insulator capacitance, V_T threshold voltage, and $Q_{ref} \equiv \{2\epsilon_S N_C kT \exp[(E_{F0} - E_m)/kT]\}^{0.5}$. Combining TLC with percolation from Eqs. (27.4)–(27.5), we now have the V_{GS}-dependent mobility relation:

$$\mu_{FE} \equiv \mu_{Per}\gamma_{TLC} = \mu_0^* \left(\frac{N_C}{N_C + N_{tc}kT_t}\right)\left(\frac{C_{ox}}{Q_{ref}}\right)^{\alpha_p} (V_{GS} - V_T)^{\alpha_p} \tag{27.6}$$

As can be seen, Eq. (27.6) follows a power law. Here, $\alpha_p \equiv 2q\phi_{B0}\gamma_B/kT$, related to percolation. In Eq. (27.6), TLC affects the constant term, while the exponent is determined by percolation.

4. Current-Voltage Relation
With Eq. (27.6) and the definition of drift current, $I_{DS} = \mu_{FE}C_{ox}(V_{GS} - V_T - V_{ch})\mathrm{d}V_{ch}/\mathrm{d}x$, current-voltage relation $I_{DS}(V_{GS})$ can be derived with the integral ranges, $x = 0$ to L and channel potential $(V_{ch}) = 0$ to V_{DS}:

$$I_{DS} \equiv \mu_0^* \left(\frac{N_C}{N_C + N_{tc}kT_t}\right)\frac{W}{L'}\frac{C_{ox}^{\alpha_p+1}}{Q_{ref}^{\alpha_p}}(V_{GS} - V_T)^{\alpha_p+1}V'_{DS} \tag{27.7}$$

In Eq. (27.7), L' is defined as $L - \Delta L$, where ΔL is effective channel length reduction, and effective drain voltage $V'_{DS} = V_{DS} - 2R_C I_{DS}$, where R_C is contact resistance. For saturation region expression, Eq. (27.7) can be reformed with a saturation parameter (β_{sat}), replacing V'_{DS} by $\beta_{sat}(V_{GS} - V_T)$. Figure 27.18a shows a comparison between measured and modelled transfer characteristics

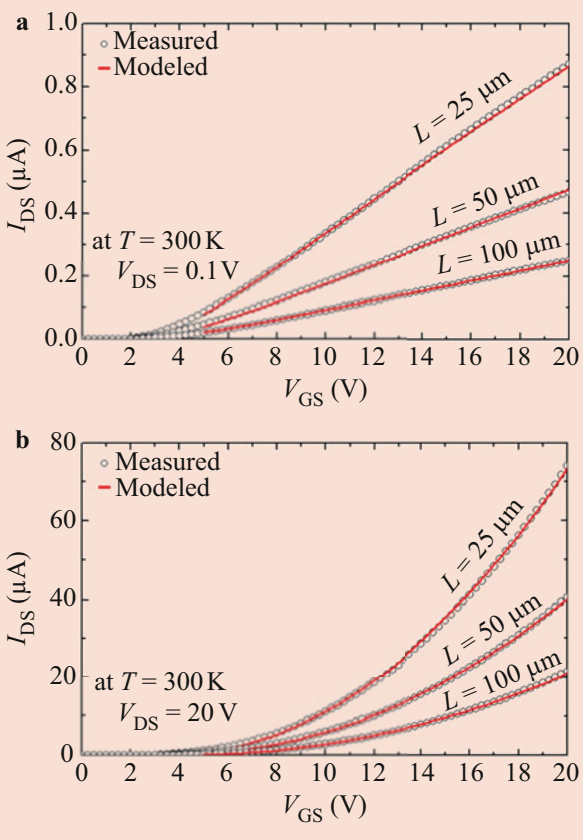

Fig. 27.18 Comparison between measured and modelled transfer characteristics (I_{DS} vs. V_{GS}) for the above-threshold region. For each region, a good agreement between measurement and modelling is achieved (**a**) Linear region with a small drain voltage (V_{DS}) of 0.1 V. (**b**) Saturation region with a high V_{DS} of 20 V

(I_{DS} vs. V_{GS}) at $V_{DS} = 0.1$ V, providing a good agreement. The measured saturation characteristics at V_{DS} =20 V is also well matched with the modelled results, as seen in Fig. 27.18b.

To check the model validity for temperature dependency, we measured and simulated the drain current as a function of gate bias for different temperatures, e.g. 100 K, 200 K, and 300 K, respectively. As seen in Fig. 27.19a, there is a good agreement between the measurements and the model (Eq. 27.7). For the purposes of validation, the modelled values of exponent (α_p) in the power law, Eq. (27.7), are compared with the extracted values from the best fit since it has a unique signature of percolation conduction, i.e. $a = \alpha_p + 1 \equiv 2q\phi_{B0} \cdot \gamma_B/kT + 1$. As seen in Fig. 27.19b, the proposed percolation model for $\phi_{B0} \cdot \gamma_B = 2.5$ meV shows better agreement compared to the conventional model (e.g. trap-limited conduction model with $a = 2kT_t/kT - 1$ for $kT_t = 30$ meV).

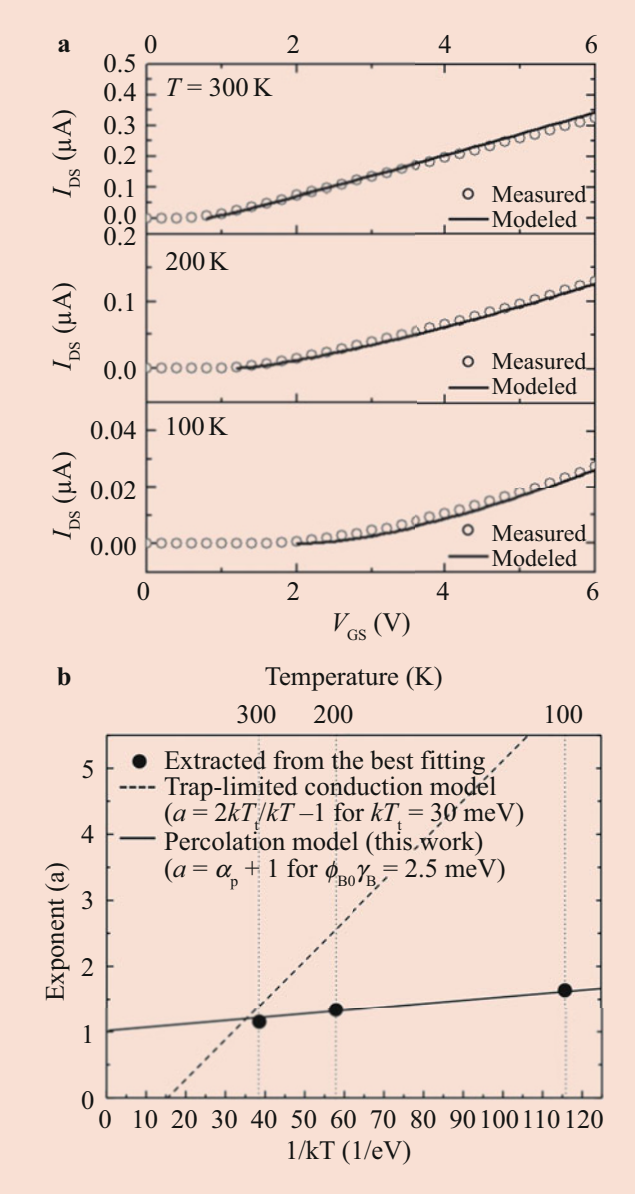

Fig. 27.19 Comparison between measured and modelled transfer characteristics at different temperatures. Here, the proposed model shows a better agreement compared to the conventional model (e.g. trap-limited conduction model) (**a**) Measured and modeled I_{DS}-V_{GS} for above-threshold region at $V_{DS} = 0.1$ V for different temperatures (100 K, 200 K, 300 K, respectively). (**b**) Retrieved exponent (**a**) vs. temperature

Subthreshold Model

The subthreshold current in the limit of low V_{GS} shows a linear dependence on V_{GS} in a semi-log plot, as illustrated in Fig. 27.22, suggesting diffusion current, as follows:

$$I_{Diff} \approx \mu_0 \frac{kT}{q} \frac{W}{L'} Q_{fi} \exp\left(\frac{q}{kT}\left(\frac{V_{GS} - V_{FB}}{1 + q^2 D_{it}/C_{ox}}\right)\right) \left(1 - \exp\left(-\frac{qV'_{DS}}{kT}\right)\right) \tag{27.8}$$

where μ_0 is the band mobility for electrons. Note that the subthreshold slope (SS) can be derived from Eq. (27.8) with the definition $dV_{GS}/d\log I_{DS}$,

$$S \equiv \ln 10 \frac{kT}{q}\left(1 + \frac{q^2 D_{it}}{C_{ox}}\right) \tag{27.9}$$

As described in Fig. 27.20, interface states are occupied first, followed by filling deep states located in the bulk at higher V_{GS}. So, as the E_F moves to the location of deep states for increasing V_{GS}, the drain current can be defined as a drift current (I_{Drift}):

$$I_{Drift} \approx \mu_0 \frac{W}{L'} \frac{C_{ox}^{\alpha_d+1}}{Q_d^{\alpha_d}} (V_{GS} - V_{FB})^{\alpha_d+1} V'_{DS} \tag{27.10}$$

where Q_d is a reference charge density associated with deep states, α_d is a power law exponent defined as $2(T_d/T - 1)$, and T_d is the characteristic temperature of deep states.

We now have the current-voltage relations for both diffusion and drift components as given by Eqs. (27.8) and (27.10). These equations can be combined as a total drain current (I_{sub}) in the subthreshold region using a harmonic average:

$$I_{sub} \equiv (I_{Diff}^{-m} + I_{Drift}^{-m})^{-1/m} \tag{27.11}$$

The examined TFT to verify this model, which is the same as that used in the previous sections, has the following geometrical and physical parameters (extracted in the previous sections): $W = 100\,\mu$m, $L = 100\,\mu$m, channel thickness $t_S = 40$ nm, channel permittivity $\epsilon_S = 11.5\epsilon_0$ (where ϵ_0

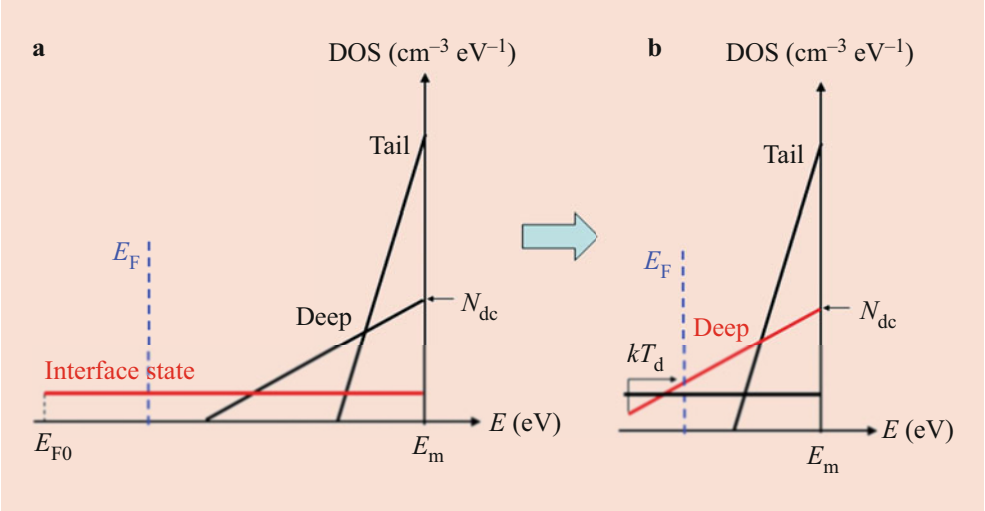

Fig. 27.20 Density of states profile with (**a**) Fermi level within interface states at low gate voltage and (**b**) the case of deep states dominant with increasing gate voltage corresponding Fermi level now within deep states

Table 27.4 Extracted subthreshold parameters at $T = 300$ K

Parameters	Value
SS	0.19 V/dec
D_{it}	1.64×10^{11} cm^{-2}eV^{-1}
I_{off}	2×10^{-14}A
Q_{fi}	7.05×10^{-14} C/cm^2
α_d	2.26
T_d	639 K
Q_d	7.8×10^{-8} C/cm^2

is vacuum permittivity), $V_{FB} \sim 0.6$ V, $V_T \sim 4$ V, $C_{ox} = 11.5$ nF/cm^2, $\mu_0 = 15$ cm^2/V · s, and $N_C = 5 \times 10^{18}$ cm^{-3} at 300 K. $2R_C \equiv R_{SD} = 9637\ \Omega$ for $W = 100\ \mu$m (equivalent to $R_{SD}W = 96.37\ \Omega \cdot$ cm), and $\Delta L = -3.5m$ ($L' = L - \Delta L = L + 3.5\ \mu$m). Other extracted model parameters are summarized in Table 27.4. Figure 27.21 shows the measured subthreshold characteristics for a different V_{DS}, providing a good agreement with each other.

To validate the subthreshold model in terms of the diffusion component in the examined transistors, we measured the drain current for small $V_{DS} = 0.01$, 0.1, and 1 V. Comparing to the model, we get good agreement as seen in Fig. 27.22. In particular, as shown in the inset of Fig. 27.22, the measured I_{DS} vs. V_{DS} at the diffusion dominant region of V_{GS} (e.g. $V_{GS} = 0.5$ V) is compared with Eq. (27.8). Here, the dependence of the drain current on V_{DS} is found to follow the law of $(1 - \exp(-qV_{DS}/kT))$ of Eq. (27.8), which is a signature of the presence of the diffusion current.

Regarding continuity and symmetry of the compact model where above- and sub-threshold models are combined, the model was subject to the Gummel symmetry test (GST)

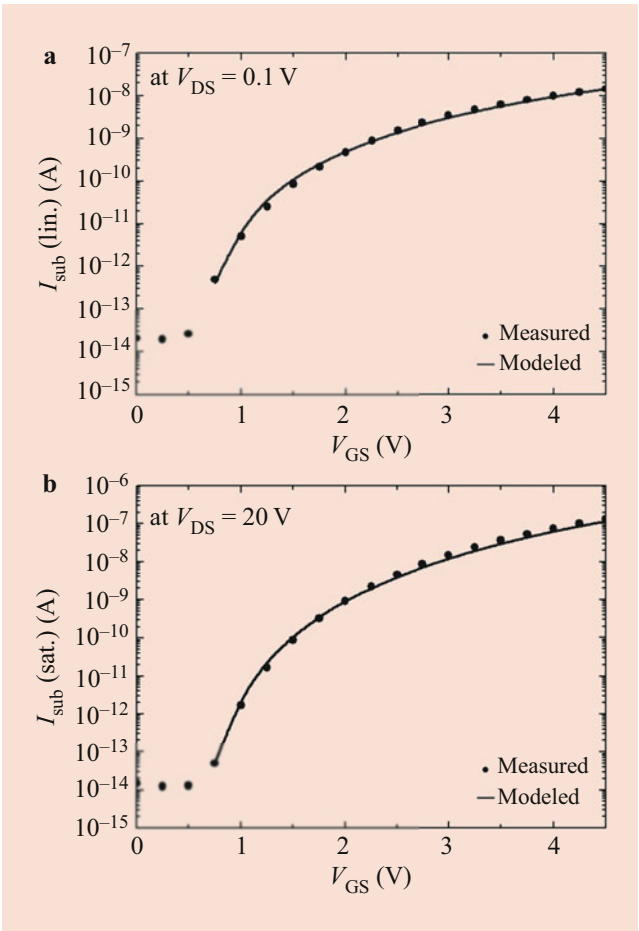

Fig. 27.21 Measured and modelled subthreshold current (I_{sub}) as a function of V_{GS}. (**a**) Linear region with $V_{DS} = 0.1$ V. (**b**) Saturation region with $V_{DS} = 20$ V

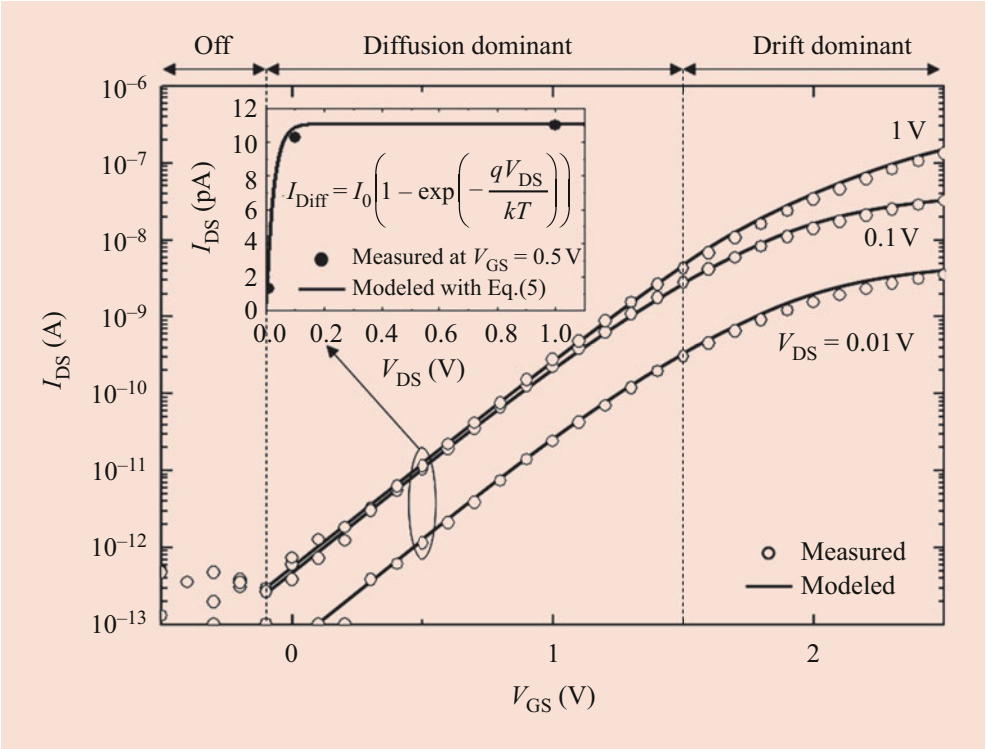

Fig. 27.22 Measured and modelled I_{DS} vs. V_{GS} at subthreshold region for a different V_{DS}. Inset: Measured and modelled I_{DS} vs. V_{DS} for $V_{GS} = 0.5$ V. Here, the equation is simplified from Eq. (27.8) introducing the pre-constant I_0 which is around 10 pA at $V_{GS} = 0.5$ V

[162, 169]. As seen in the inset of Fig. 27.23a, V_X represents a symmetrical voltage applied on source and drain sides, respectively. Figure 27.23 demonstrates perfect continuity and symmetry as a function of V_X even for the fourth derivative of I_{DS} with respect to V_X, suggesting it has successfully passed the GST. For this, we employed smoothness and continuity functions for the effective drain voltage and threshold voltage terms [170].

Off Region Model

The off current can defined according to [159] at $V_{GS} = V_{FB}$:

$$I_{off} \approx \mu_0 \frac{kT}{q} \frac{W}{L} Q_{fi} \left(1 - \exp\left(-\frac{qV'_{DS}}{kT}\right)\right) \tag{27.12}$$

Unified Model

As seen in previous Sects. 27.2.1 and 27.2.1, the current-voltage relation needs to be derived separately to describe the subthreshold and above-threshold characteristics. Here, we need separate expressions for the subthreshold and above-threshold regions, implying two different equation systems to describe total current (see Fig. 27.24). Moreover, in this case, threshold voltage (V_T) is not immediately apparent from the I-V plot and needs to be extracted from above-threshold region of the characteristic as a fitting parameter. However, the extracted value of V_T can be quite different depending on the extraction method and the I-V data range chosen for the fit. In contrast, turn-on voltage (V_{on}) is the gate voltage (V_{GS}) at which drain current (I_{DS}) starts increasing rapidly; thus, it is easy to identify V_{on} on a semi-log plot of I_{DS} vs. V_{GS}.

We can unify this to cover both subthreshold and above-threshold characteristics. The proposed unified model is a single expression with a reference voltage level V_{on} rather than V_T, providing good agreement with measured terminal characteristics over the entire range of $V_{GS} > V_{on}$ for the test TFTs with an amorphous InGaZnO (a-IGZO) channel, which is the same TFT used in the previous sections. The derived equation for this model is as follows:

$$I_{DS} = G_0 \frac{W}{L'} \exp\left(\kappa (V_{GS} - V_{on})^{\alpha}\right) V'_{DS} + I_{off} \tag{27.13}$$

where $G_0 = \mu_0 (\epsilon_S kTN_C)^{1/2}$, $\kappa = \zeta/2kT$, and ζ & α are related to trap states. To extract the values of κ and α, we can rewrite Eq. (27.13) as,

$$U \equiv \frac{I'_{DS}/V'_{DS}}{\mathrm{d}(I'_{DS}/V'_{DS})/\mathrm{d}V_{GS}} = \frac{1}{\alpha\kappa}(V_{GS} - V_{on})^{1-\alpha} \tag{27.14}$$

Here, $I'_{DS} \equiv I_{DS} - I_{off}$. Therefore, $1-\alpha$ and $1/(\alpha\kappa)$ can be extracted from the plot of $\ln U$ vs. $\ln(V_{GS} - V_{on})$ as the slope and the intercept, respectively (as illustrated in Fig. 27.25a). The extracted model parameters are summarized in Table 27.5.

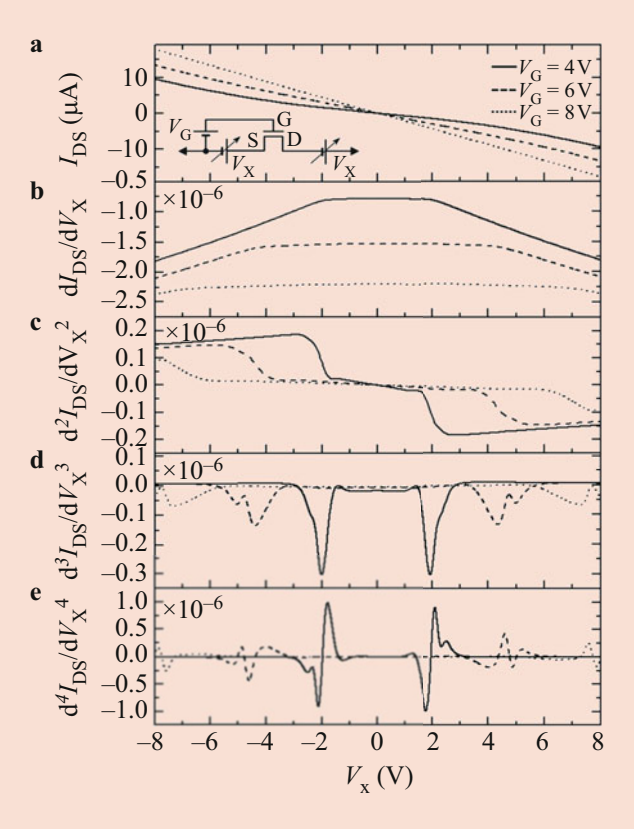

Fig. 27.23 (**a**) Calculated I_{DS} vs. V_X of the combined above- and sub-threshold model for different V_G (4, 6, 8 V). (**b**) First, (**c**) second, (**d**) third, and (**e**) fourth derivatives of I_{DS} with respect to V_X. The inset of (**a**): test circuit configuration of the GST

Figure 27.25b shows modelled results for different L (=25, 50, and 100 μm), providing good agreements with the measured characteristics. Also, they exhibit small average errors <5% over a wide range of V_{GS} from 5 to 20 V. Interestingly, the proposed model using only one equation covers both the sub- and above-threshold regions at the same time. This is mainly due to a combination of the exponential function and power law. Additional advantage of this unified model is that it just needs a few model parameters to be implemented in model code description, e.g. Verilog-A, thus providing a higher-speed simulation.

Computer Interpretation of Device Model

After having established an accurate analytical model for the TFT, computer implementation for circuit simulation is not always easy. Several considerations including speed, convergence, and even the way of translating different forms of equations into computer language should be taken into consideration in this step.

For a-Si TFTs, several SPICE models have been developed. Specifically the model developed by Rensselaer Polytechnic Institute, also known as the RPI model [150], has become a commercialized standard supported by many simulation platforms including SmartSpice, HSPICE, Spectre, etc. However, CAD of organic and metal-oxide TFTs is yet to become a standard due to the rapid and ongoing evolution in materials and device structures. In fact, and as mentioned previously, there is a quest for unifying the TFT model to meet simulation requirements of TFTs with ever-changing structures and materials.

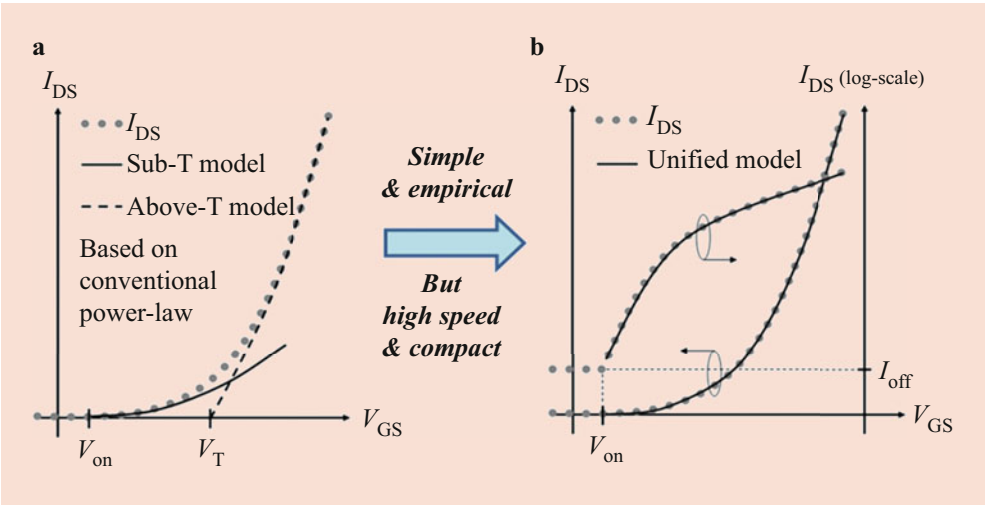

Fig. 27.24 (**a**) Schematic I_{DS} vs. V_{GS} curves (grey circles) with the conventional power law models for subthreshold (Sub-T, solid line) and above-threshold (Above-T, dot line) characteristics. In this case, we need two models for these two different operational regions. Here, V_{on} and V_T are on-voltage and threshold voltage, respectively. (**b**) Schematic I_{DS} vs. V_{GS} curves (grey circles) with only one model: unified model which can cover subthreshold as well as above-threshold regions at the same time

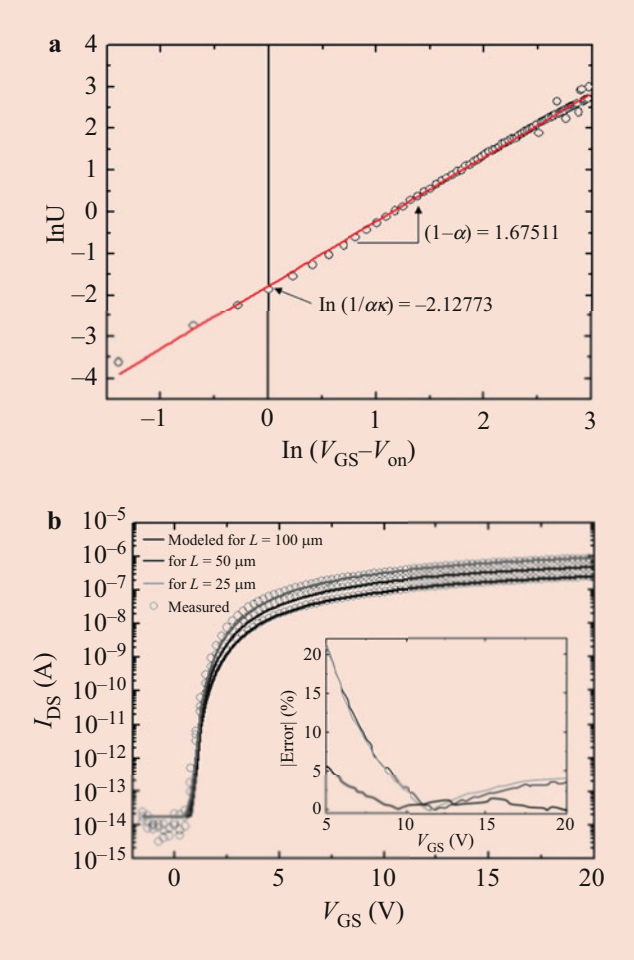

Fig. 27.25 Parameter extraction for unified model & measured and modelled transfer curve with percentage error. (**a**) Plots of ln$U$ vs. ln($V_{GS} - V_{on}$). Here, linear fitting is applied over the entire range of ln($V_{GS} - V_{on}$). (**b**) Modelled results for different L in comparison with the measured curves using a unified model, normalized error is illustrated in the inset

Table 27.5 Extracted parameters for unified model at $T = 300$ K

Parameters	Value
G_0	2.34×10^{-5}ohm^{-1}
κ	-10.812 V$^{-\alpha}$
α	-0.675

It is important to understand the benefits and drawbacks of SPICE and Verilog-A while developing a device model to be used in further circuit simulation and system design.

SPICE

SPICE is an open-source analogue circuit simulation software firstly developed at the University of California, Berkeley [171]. The first two versions of this simulator were written in Fortran. SPICE2 included several elements widely used in circuit simulation at that time, including the diode, MOSFET, JFET, BJT, etc. In 1989, a version of the simulator SPICE3 was rewritten in C. This version includes the well-known BSIM model [172].

Many commercial circuit simulators today are based on the aforementioned software, including PSPICE, HSPICE, SmartSpice, Spectre, etc. The fast simulation speed, high accuracy, and ease of use make the SPICE simulator extremely popular in the area of circuit design. However, SPICE is written in a low-level computer language (Fortran or C) and so are the models used in it. Therefore, researchers should not only have a good understanding of device physics but also need enough knowledge of the algorithms and limitations of the simulator. The procedure for developing a standalone SPICE model (not by combining existing elements) always takes time and resources. Due to the complexity of model development in SPICE, currently only well-developed and widely used devices are having SPICE models.

It is worth noting that modern circuit simulators use a heavily modified original SPICE model, but they separate as much as possible the simulation algorithm from the device model. For example, the Spectre simulator provides a Spectre Compiled Model Interface (CMI) for Spectre developers and others to use C code directly for device modelling.

Verilog

The Verilog Hardware Description Language (Verilog HDL) was designed in 1984 to meet the design demands of VLSI engineers working in the higher abstractive level to increase the number of transistors in simulating digital circuits. Subsequently adopted by Cadence Design Systems and Open Verilog International, VHDL has become an IEEE standard in 1995, i.e. IEEE Std 1364-1995 [173].

Since the original Verilog language did not support analogue systems, the extensive use of HDL languages led to a growing demand for high-level behavioural model for systems and components for use in analogue and mixed signal system design. Thus, Verilog-AMS standard was then developed by Accellera to include Verilog-A, a previously standalone behavioural language used for analogue modelling in Spectre, and extending both the digital part of the IEEE Std 1364 and the analogue part of Verilog-A [174].

In the early days of Verilog-A and Verilog-AMS, the behaviour model was limited in terms of accuracy for analogue devices. The language was first developed for design of systems, and thus the behavioural language was at that time not intended for complex physical equations at the device level. Figure 27.26 illustrates the mixed signal simulation environment in early days. In addition, device modelling often led to long execution times compared with SPICE models. Even so, the capability of behavioural modelling started to attract the attention of device modellers struggling with low-level implementation.

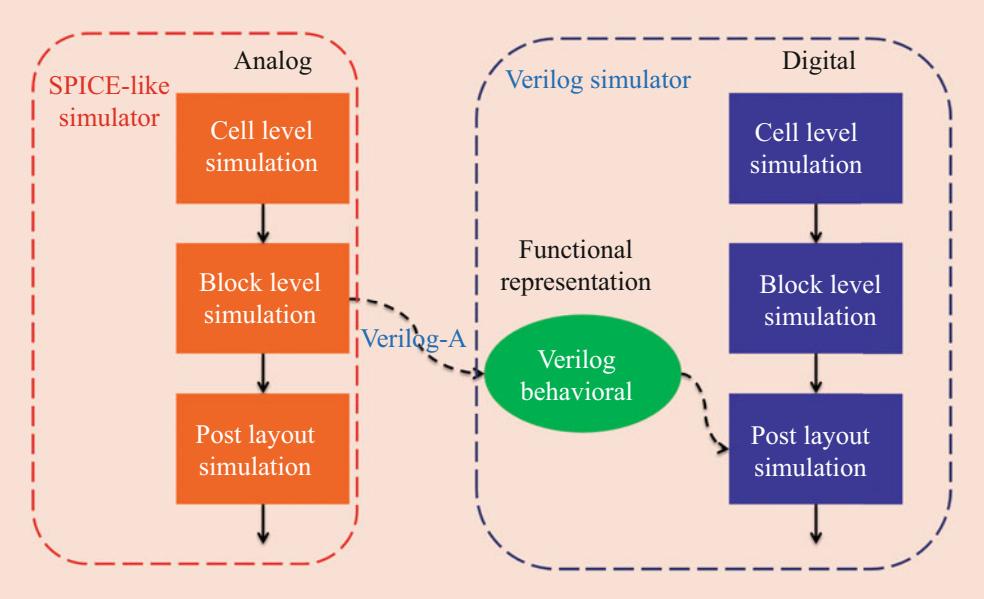

Fig. 27.26 Verilog-A behaviour model in early mixed signal simulation environment

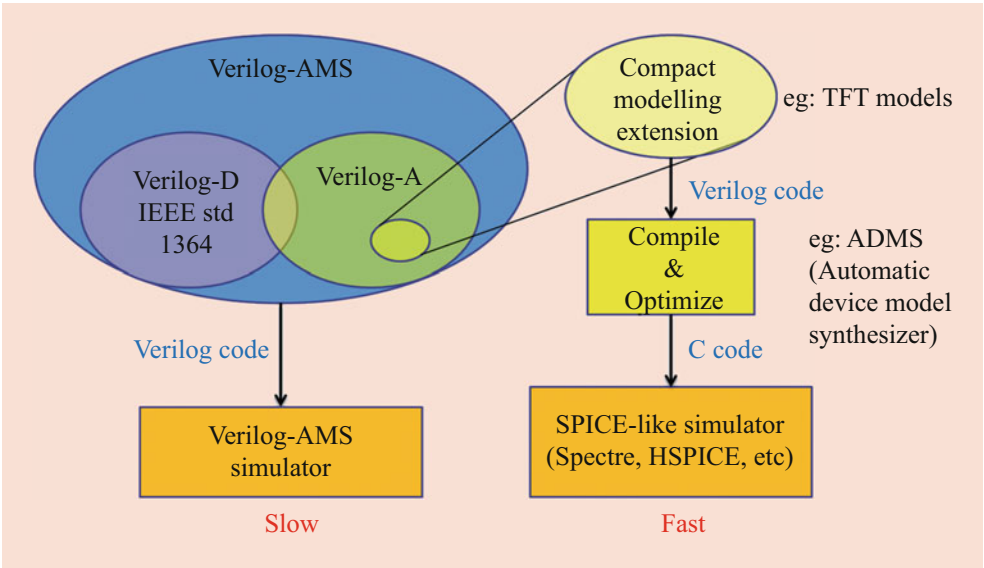

Fig. 27.27 Verilog-A(MS) extension for compact modelling with SPICE-like simulator integration

In 2002, the open-source tool supporting automatic conversion [175] of Verilog-AMS models to C codes was introduced. Since then, several proposals have been made to use Verilog-AMS to efficiently develop compact device models [176,177] to integrate with SPICE-like simulators. The report in 2010 [178] showed comparable performance of their Verilog-AMS device model against SPICE. The language has now become a major tool for device model developers. Figure 27.27 illustrates the relation between different Verilog languages and the simulation flow in two types of simulators.

Short Summary of Comparison

Table 27.6 summarizes the comparison of different model languages. The SPICE model development based on a low-level language is only used by model developers of components, which are not likely to change (due to heavy usage or technology maturity) in view of resource requirements. In the meantime, the Verilog approach is ideally suited to meet the modelling demands of ever-changing TFT or other device structures without requiring a mature physical understanding of the devices or underlying material system. The direct

implementation of physical equations in Verilog-AMS will dramatically reduce the time between development of new devices and subsequent circuit simulation.

Despite all the benefits of Verilog-AMS, the model is still slower and less efficient than a well-developed SPICE model, due to the fact that the Verilog-AMS model should be converted to a lower-level language form. The converted form although automatically optimized by the synthesizer (e.g. ADMS [175]) cannot be as efficient as a SPICE model because the latter is optimized directly in a lower-level language. Therefore, it is recommended to use SPICE for circuit simulation whenever it could offer sufficient accuracy. On the other hand, Verilog-AMS is suited for devices that are new or under development.

Table 27.6 Comparison between different model languages

	SPICE	Spectre CMI	Verilog-AMS
Language	C/Fortran	C	Verilog
Language level	Low	Low	High
Easy to use	No	No	Yes
Efficiency and speed	High	High	Low
Complexity	High	High	Low
Information needed	Algorithm and limitations	Equation limitations	None
Users	SPICE developers	CAD engineers, Cadence programmers	End users

CAMCAS Model in Simulation Environment

As discussed before, we implement the Cambridge's TFT compact model (i.e. CAMCAS model) directly into Verilog-A language for use in a Cadence Design Environment so as to focus on developing a more accurate model for circuit simulations. The simulation flow in the Cadence Design Environment is shown in Fig. 27.28.

The user extracts processing parameters based on the measurement results of their own devices and incorporates them into the CAMCAS Verilog-AMS model. In addition, the user can change the form of equations for better fitting to measurement results. Thus, circuit designers can use the usual route of circuit design by simulating their TFT circuits before fabrication analogous to using the SPICE model in Cadence Spectre.

Figure 27.29 shows an example of an IGZO TFT circuit simulated using the CAMCAS model in Cadence Spectre. The simulation results show a voltage gain of 12 dB in both transient and AC simulation as shown in Fig. 27.30a and b, respectively.

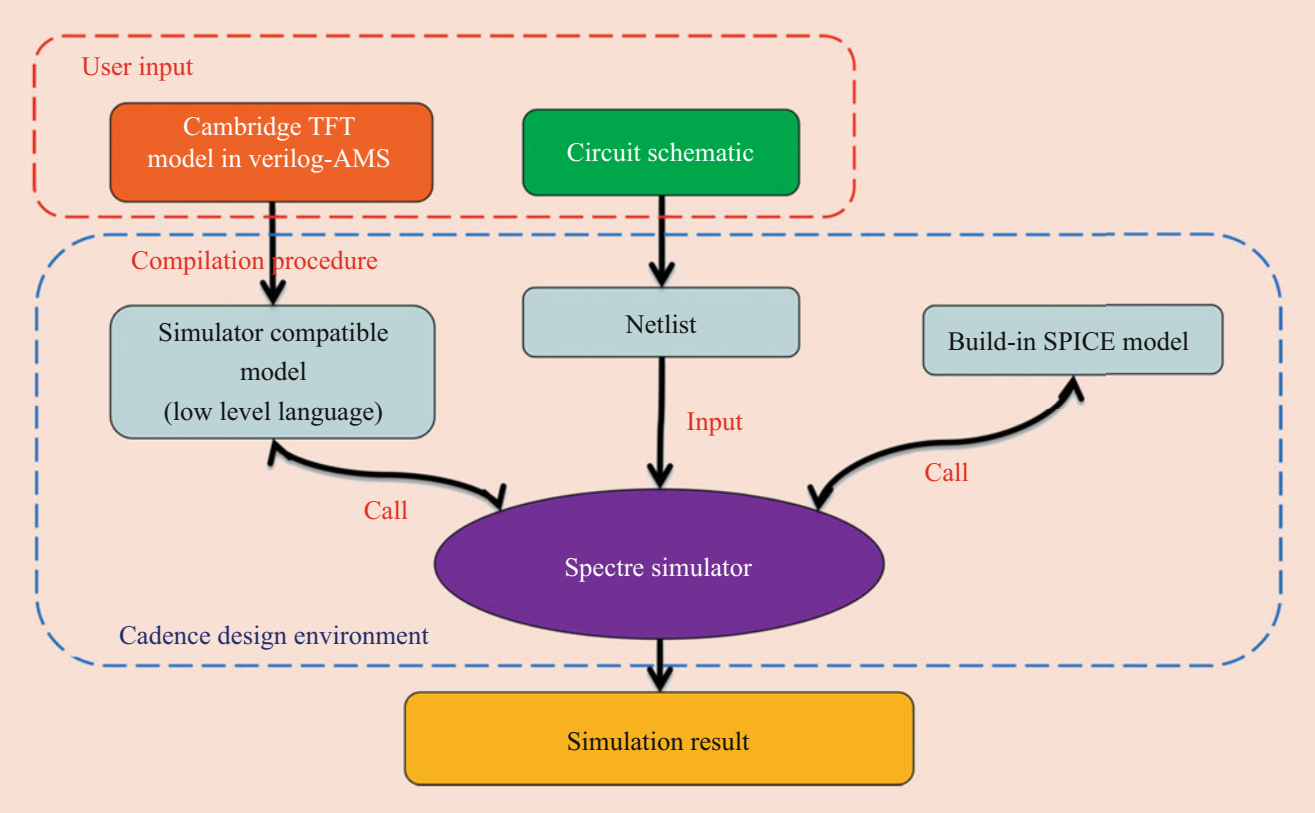

Fig. 27.28 Circuit design and simulation flow using CAMCAS model in Cadence Design Environment

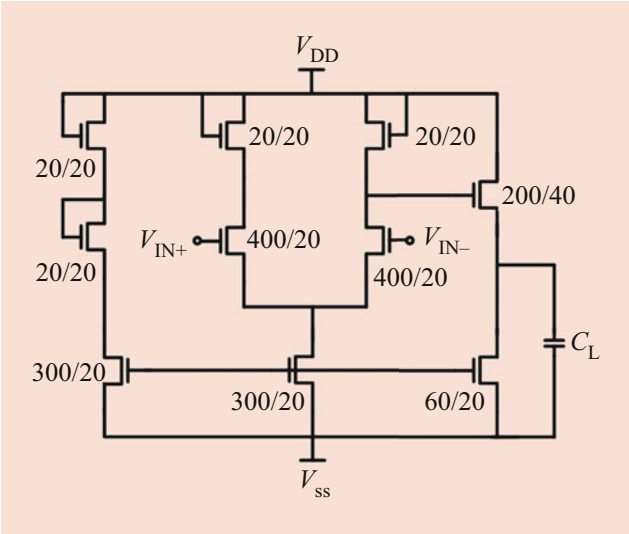

Fig. 27.29 A voltage amplifier used in simulation with CAMCAS model

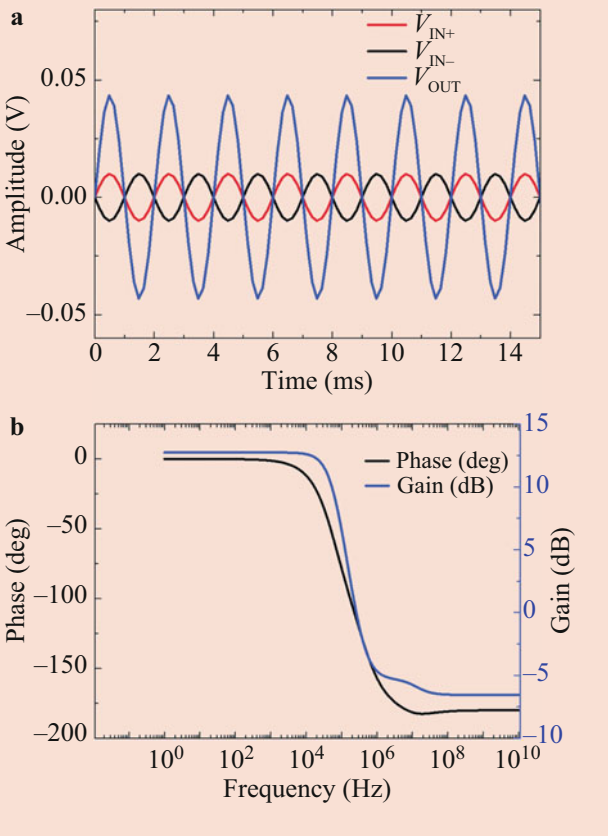

Fig. 27.30 Simulation results of the voltage amplifier. (**a**) Transient analysis for small signal amplitude at input and output. (**b**) AC analysis for gain and phase

27.2.2 Small-Signal Modelling

General Small Models

Small-signal model is used for linear approximation of many nonlinear electronic devices including diodes, MOSFET, BJT, etc. when the signal under processing is reasonably small compared with the DC bias of devices [179]. The use of small-signal model significantly simplifies the design procedure of many analogue circuits, especially amplifiers. Different small-signal models exist for different electronic devices; for example, MOSFET and BJT are having different small-signal models due to their different structure and working principles. However, researchers in the area of TFT circuit design are using the same small-signal model as MOSFET. In spite of the similarity of their structures, TFTs are having a much bigger contact resistance between different materials, more significant parasitic capacitance, and a severe instability problem. Therefore, it is helpful to re-evaluate the small-signal model specifically for TFTs.

Midband Small-Signal Model

First, we review how a midband small signal model was developed. As linear systems are to be designed out of nonlinear devices, the straightforward solution is to use a small part of the nonlinear behaviour (I-V curves) to approximate a linear response (small-signal model). Therefore, under the assumption that the signal is sufficiently small, the linear approximation would be equal to the derivative of the none linear device at the bias point. For a general three-terminal device with terminals G, S, and D (terminal names can be arbitrarily chosen; here they are chosen in consistency with TFTs), the I-V formula can be written as:

$$\begin{cases} I_D = f_1(V_{GS}, V_{DS}) \\ I_G = f_2(V_{GS}, V_{DS}) \end{cases} \tag{27.15}$$

Here, V_{GS} and V_{DS} are the voltage drops between G-S terminals and D-S terminals, respectively. As V_{GD} can be calculated from $V_{GS} - V_{DS}$ and $I_S = -I_D - I_G$, Eq. (27.15) is enough to represent the I-V of an arbitrary three-terminal device.

For small changes of V_{GS} and V_{DS}, the current differences would approximately follow the derivative of the I_D and I_G functions in Eq. (27.15).

$$\begin{cases} dI_D = \frac{\partial f_1}{\partial V_{GS}} dV_{GS} + \frac{\partial f_1}{\partial V_{DS}} dV_{DS} \\ dI_G = \frac{\partial f_2}{\partial V_{GS}} dV_{GS} + \frac{\partial f_2}{\partial V_{DS}} dV_{DS} \end{cases} \tag{27.16}$$

For sufficiently small signals and sufficiently good linearities at the bias point, the partial derivatives can be treated as a constant. The small-signal relations should follow:

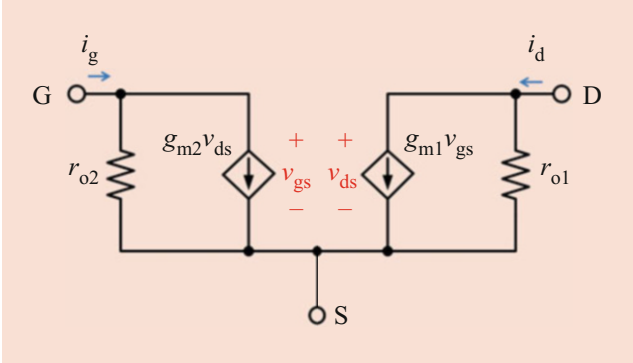

Fig. 27.31 Small signal model for a general three-terminal device

$$\begin{cases} i_d = g_{m1} v_{gs} + \frac{v_{ds}}{r_{o1}} \\ i_g = \frac{v_{gs}}{r_{o2}} + g_{m2} v_{ds} \end{cases} \tag{27.17}$$

where i and v in small cases represent the small change in current and voltage of the corresponding terminals, respectively. The coefficient of v_{ds} for i_d or v_{gs} for i_g can be represented as passive components (a resistor connection), while the coefficient of v_{gs} for i_d or v_{ds} for i_g can only be represented by active components, a voltage-controlled current source (VCCS). Therefore, resistance is used to represent passive components (i.e. r_{o1} and r_{o2}), and transconductance is used to represent active components (i.e. g_{m1} and g_{m2}).

Now, from Eq. (27.17), we have the linear approximation of the device at a fixed bias point of V_{GS} and V_{DS} (note that the coefficients in Eq. (27.17) can be a function of V_{GS} and V_{DS}, but not a function of v_{gs} and v_{ds} under the small-signal assumption.) The corresponding small-signal model of the equation can be drawn as Fig. 27.31. This is a general form of a hybrid-pi model which is consistent with both BJT and MOSFET. In the case of most transistors, V_{DS} does not affect I_G. Thus, $g_{m2} = 0$. And for the case of MOSFET, the gate resistance is huge and normally treated as open circuit. Therefore, the corresponding components can be removed.

The analysis reviewed above is a general approach for all three terminal devices. Thus, it should also be valid for TFTs at midband frequencies. However, as the parameters are derived from the derivative of I-V curves, a more physical representation of those parameters can be complicated, and some of the parameters should be represented as separate components.

High-Frequency Small-Signal Model

An accurate calculation of the circuit response at midband frequency is not enough for circuit designers as the bandwidth and phase margin should also be predicted when designing circuits. This is especially crucial for amplifiers and active filters to prevent self-oscillation. While midband

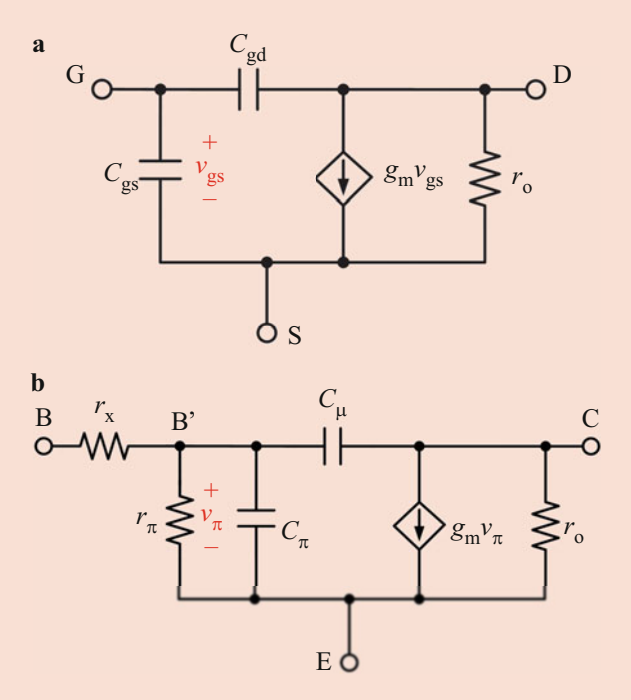

Fig. 27.32 High-frequency small-signal models for CMOS and BJT. (**a**) CMOS model. (**b**) BJT model

small-signal models can be developed through a general way from I-V curves, the high-frequency small-signal model can only be developed by considering I-V, C-V, and physical meanings of different components. This is why the high-frequency small-signal models are very different for CMOS and BJT despite the similarities on their midband models.

The comparison of CMOS and BJT models is shown in Fig. 27.32 [180]. The CMOS high-frequency model (Fig. 27.32a) is more consistent with the midband model that the parasitic capacitors are added to the midband model while keeping the original connections. In comparison, the BJT model (Fig. 27.32b) is less so as node B' is added between r_x and r_π (which are the same resistance in the midband model). The separation of r_x is due to the physical representation of a base spreading resistance, which is the resistance of the connection to the base inside the device. The contribution of this resistor becomes more significant at high frequency because of the reduced impedance of the parasitic capacitors, namely, C_μ and C_π.

The review of CMOS and BJT high-frequency small-signal models suggests that physical structure should be considered while developing high-frequency models as the connections of parasitic capacitances may vary and affect the overall performance of the model. Therefore, it is imperative to evaluate the TFT structure to include physical resistance, capacitance, and their connections correctly.

TFT Small-Signal Model

As discussed in the introduction section, an accurate TFT small-signal model needs to consider the physical representations and modelling not only for the sake of a simpler expression of each component in the midband model but also for an accurate modelling in the high-frequency model. In this section, we will discuss the concerns at the stage of model developing and report the developed models.

Midband TFT Model

As discussed in Sect. 27.2.2, the midband model can be developed using the general approach. Therefore, the small-signal behaviour can be represented by a VCCS and an output resistor in parallel. The major concern of this approach is the expression of the two components, g_m and r_o. As the two components come from the derivative of $I_{DS} - V_{GS}$ and $I_{DS} - V_{DS}$ curves, the static characteristic of TFTs should be considered first before deriving the expressions of g_m and r_o.

The major concern here comes from the big contact resistance (R_C) [161, 181–185] and the threshold voltage shift (V_T shift) [164, 186–190] in TFTs which include TFTs from different material families such as amorphous silicon, organic, and metal oxide semiconductors. Although TFTs are having a similar working principle with MOSFET, the contact resistance (R_C) is so dominant that even the static model should consider R_C as independent components. Most of the static models are developed based on a structure shown in Fig. 27.33 where the I-V characteristics are modelled for the internal transistor and the $R_C s$ (R_S and R_D here) are accounted for separately.

In this section, we will consider the effect of contact resistance and V_T shift in the midband TFT model.

The Effect of Contact Resistance

As the overall I-V expression is complicated when considering R_S, R_D, and the ideal TFT as a whole, it is more convenient to derive the small-signal model of the ideal TFT and then consider the circuit as a linear network. Therefore, by using the I-V expression, we can easily derive a small-signal model shown in Fig. 27.34a. As reviewed in Sect. 27.2.1, the general I-V expression for a TFT can be written as:

$$I_{DS} = \frac{1}{\alpha_p + 2} K \frac{W}{L'} (V_{GS'} - V_T)^{\alpha_p + 2} \tag{27.18}$$

where $K = (\alpha_p + 2)\mu_0^* (\frac{N_C}{N_C + N_{tc} kT_t}) \frac{C_{ox}^{\alpha_p + 1}}{Q_{ref}^{\alpha_p}} \beta_{sat}$. The transconductance g_{mi} in in Fig. 27.34a can then be calculated directly as:

$$g_{mi} = K \frac{W}{L'} (V_{GS'} - V_T)^{\alpha_p + 1} \tag{27.19}$$

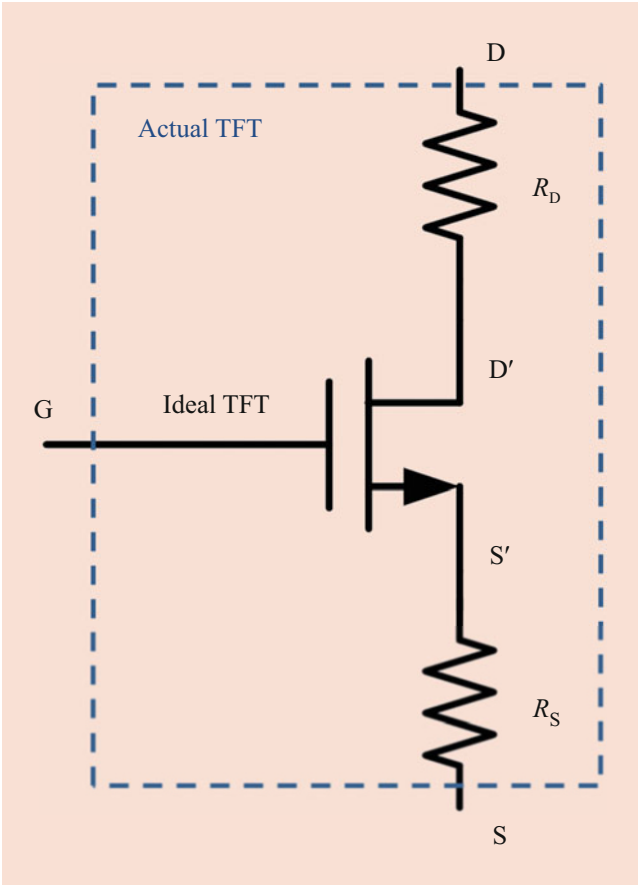

Fig. 27.33 The inner structure based on which static TFT models are developed

The r_{oi} in the figure, however, is harder to express in physical parameters. As the slope of the output characteristics are normally modeled using an empirical Early voltage (V_A), TFTs do not have the same short channel effect as CMOS does. But the output characteristics have similar trend of having an Early voltage. Thus, it is usually modeled by an empirical Early voltage. r_{oi} is then calculated using:

$$r_{oi} = \frac{V_A}{I_{DS}} \tag{27.20}$$

With the above equations, we can easily get an accurate midband small-signal model for the TFT of concern and design suitable g_{mi} and r_{oi} by choosing W/L ratio, given that the TFT technology and processing parameters are already modeled with known R_S, R_D, and V_A. However, it is not so convenient in terms of measurements as the results will be overall I-V curves directly. The derivatives of the overall I-V curves can capture the overall g_m and r_o in an equivalent midband model shown in Fig. 27.34b (the general approach).

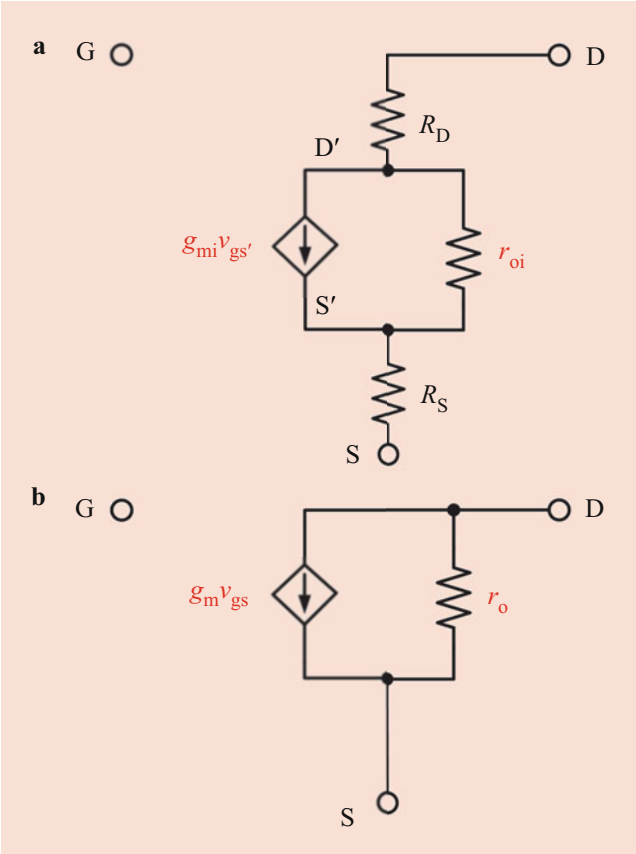

Fig. 27.34 Midband small-signal models. (**a**) R_C as separate component. (**b**) Overall midband model

It is worth finding the relations between the two models shown in Fig. 27.34.

As the circuits only consist of linear components, in this case only VCCS and resistors, the circuit in Fig. 27.34a should be equivalent to the one in Fig. 27.34b according to Thevenin' theorem [191, 192]. From Fig. 27.34a, we have:

$$\begin{cases} i_d = \frac{v_{s's}}{R_S} \\ i_d = g_{mi}(v_{gs} - v_{s's}) + \frac{v_{ds} - i_d R_D - v_{s's}}{r_{oi}} \end{cases} \tag{27.21}$$

Substituting $v_{s's}$ and considering. As the semiconductor layer and source/drain contacts are made of the same material and have identical geometries and similar properties, the contact resistances are considered to be equal at both sides for convenience. $R_S = R_D = R_C$, we get:

$$i_d = \left(\frac{g_{mi}r_{oi}}{g_{mi}r_{oi}R_C + 2R_C + r_{oi}}\right)v_{gs} + \left(\frac{1}{g_{mi}r_{oi}R_C + 2R_C + r_{oi}}\right)v_{ds} \tag{27.22}$$

Compared with Fig. 27.34b, we have:

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_o} \tag{27.23}$$

As both models should capture the same derivatives of the overall I-V curves (i.e. g_m and r_o), the relations should follow:

$$\begin{cases} g_m = \frac{g_{mi}r_{oi}}{g_{mi}r_{oi}R_C + 2R_C + r_{oi}} \\ r_o = g_{mi}r_{oi}R_C + 2R_C + r_{oi} \end{cases} \tag{27.24}$$

Here, we can derive the overall g_m and r_o out of the theoretical prediction of our transistor models. While designing real circuit applications, this will be the equations to use to estimate the circuit behavior. By solving Eq. (27.24), we can also get the values of internal components from measurement results:

$$\begin{cases} g_{mi} = \frac{g_m r_o}{r_o - g_m r_o R_C - 2R_C} \\ r_{oi} = r_o - g_m r_o R_C - 2R_C \end{cases} \tag{27.25}$$

This equation is very useful when the values of internal components are to be extracted out of measurement results. It also provides a convenient way of checking the validity of the model, which will be discussed later.

Equations (27.24) and (27.25) not only show the relation between the static model parameters and the overall parameters from measurements but also reveal some insights of the parameters:

1. The intrinsic gain $g_m r_o$ of both the overall performance and the ideal internal TFT is the same. As the overall g_m is reduced due to the contact resistance (in comparison with g_{mi}), the r_o increases at the same rate, making $g_m r_o = g_{mi} r_{oi}$. This also means that the contact properties of the semiconductor layer and the electrodes do not affect the intrinsic gain of the overall transistor. The measurement of $g_m r_o$ directly shows the maximum achievable single-stage gain of the semiconductor technology.
2. The term $g_{mi}R_C$ can be used to evaluate how different the measurement results will be from the ideal TFT in the model. As $g_{mi}r_{oi}R_C$ cannot be dominant over r_{oi}, the overall $g_m \approx \frac{1}{R_C}$ (which is impractical as there's no dependence on bias), and $R_C \ll r_{oi}$, the value of $g_{mi}R_C$ should be around 0 1 (might be a bit higher than 1 but should be around the order of magnitude).

The Effect of V_T Shift

Another property that might affect the midband model is the V_T shift under bias condition. As the implementation of TFTs in AMOLED display proves that bias-induced V_T shift must be compensated especially when the analogue properties are to be used (i.e. the output current needs to be actually controlled), the TFT small-signal model should capture the behaviour to help design and evaluate TFT analogue circuits.

The major concern of V_T shift is that it would change the bias condition in effect, as in the static models, the V_T terms always appear in $V_{GS} - V_T$. Therefore, considering V_T shift,

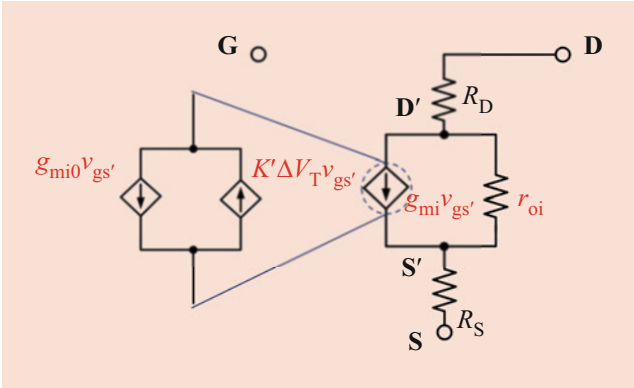

Fig. 27.35 Midband TFT model considering V_T shift

the expression of Eq. (27.19) can be rewritten as:

$$\begin{aligned} g_{mi} &= K\frac{W}{L'}(V_{GS'} - V_T - \Delta V_T)^{\alpha_p+1} \\ &= K\frac{W}{L'}(V_{GS'} - V_T)^{\alpha_p+1}\left(1 - \frac{\Delta V_T}{V_{GS'} - V_T}\right) \\ &= K\frac{W}{L'}(V_{GS'} - V_T)^{\alpha_p+1} - K\frac{W}{L'}(\alpha_p + 1) \\ &\quad \times (V_{GS'} - V_T)^{\alpha_p}\Delta V_T + O\left(\frac{\Delta V_T}{V_{GS'} - V_T}\right) \end{aligned} \tag{27.26}$$

Typically, $\Delta V_T << V_{GS'} - V_T$, as the experiments show that the V_T shift does not turn the transistor off (i.e. $\Delta V_T \sim V_{GS'} - V_T$) at least not within a reasonable time period. Hence, the higher-order terms can be omitted in the above Taylor expansion. The first-order approximation of $g_m i$ can then be written as follows:

$$g_{mi} \approx g_{mi0} - K'\Delta V_T \tag{27.27}$$

where $g_{mi0} = K\frac{W}{L'}(V_{GS'} - V_T)^{\alpha_p+1}$ is the initial value where there's no V_T shift, and $K' = K\frac{W}{L'}(\alpha_p + 1)(V_{GS'} - V_T)^{\alpha_p}$ is the coefficient of the g_{mi} change per ΔV_T change. Here, as α_p is a constant value close to zero, K' can normally be treated as a constant coefficient.

This means that the V_T shift effect can be represented by a separate component. The corresponding modification of small-signal model is shown in Fig. 27.35.

High-Frequency TFT Model

Device structure and physical meanings of all components need to be considered in high-frequency small-signal model, especially when capacitances come into the picture, as discussed in Sect. 27.2.2 of the BJT model. The connection of contact resistances in TFTs plays a similar role as the base spread resistance of BJT, which is connected in series with a parasitic capacitance. Here, as illustrated in Fig. 27.36, the contact resistance at source side (R_S) separates the overlap

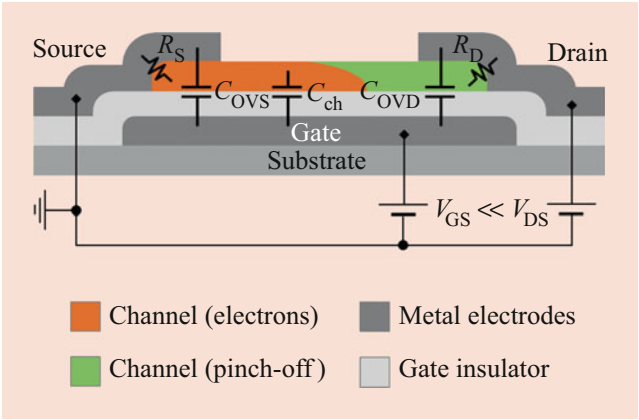

Fig. 27.36 Bottom-gate TFT structure considering passive components of the small-signal equivalent circuit. C_{OVS} and C_{OVD} are the overlap capacitance at source and drain side; C_{ch} is the channel capacitance; R_S and R_D are the contact resistances at source and drain side

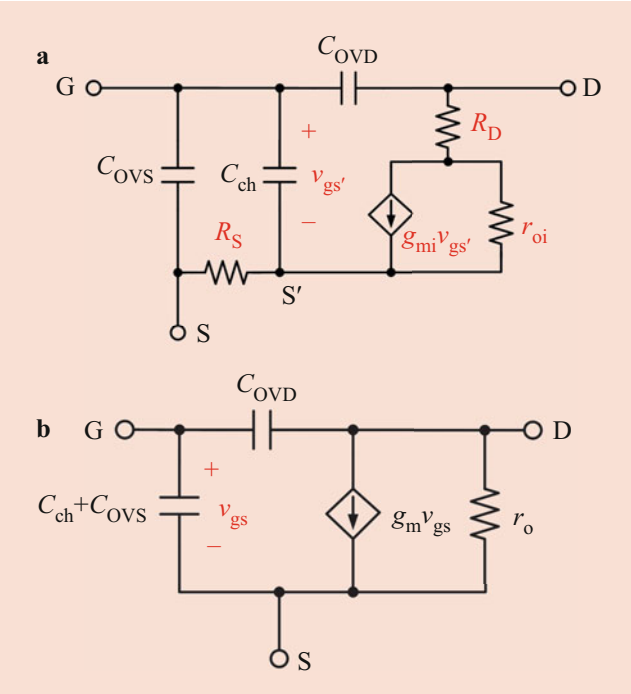

Fig. 27.37 High-frequency small-signal models. (**a**) TFT model. (**b**) CMOS model adapted to TFTs

capacitance (C_{OVS}) and channel capacitance(C_{ch}). Hence, R_S might not be negligible nor included in overall components (i.e. g_m and r_o) especially at high frequencies. Combining the analysis of the midband model, the high-frequency small-signal model for TFT can be drawn as Fig. 27.37a. In comparison, the CMOS model adapted to TFT parameters is shown in Fig. 27.37b. Here, C_{OVS} and C_{ch} are considered to be the same capacitor between source and gate terminals, and the contact resistances are included in the overall g_m and r_o.

In order to evaluate the difference between the developed model and the CMOS model, we compare the expressions of

the short-circuit current gain (A_i) and the cutoff frequency of the two different circuits.

For CMOS model, A_i can be calculated as:

$$A_i = \frac{sC_{OVD} - g_m}{s(C_{OVD} + C_{OVS} + C_{ch})} \tag{27.28}$$

which contains one pole (at 0) and one zero (at g_m/C_{OVD}). Assuming the zero is far from the point of cutoff frequency. The unit-gain cutoff frequency can be calculated as:

$$f_T = \frac{g_m}{2\pi(C_{OVD} + C_{OVS} + C_{ch})} = \frac{g_m}{2\pi C_{tot}} \tag{27.29}$$

where C_{tot} is the sum of all capacitances of the TFT.

In contrast, the current gain calculated for the TFT small-signal model seen in Fig. 27.37a is:

$$A_i = \frac{-g_{mi}r_{oi} + ((2R_C + r_{oi} + g_{mi}R_C r_{oi})C_{OVD} + C_{ch}R_C)\,s + C_{OVD}C_{ch}R_C(R_C + r_{oi})s^2}{s\,(g_{mi}C_{OV}R_C r_{oi} + (2R_C + r_{oi})(C_{OV} + C_{ch}) + C_{OV}(R_C + r_{oi})R_C C_{ch}s)} \tag{27.30}$$

where $C_{OV} = C_{OVS} + C_{OVD}$ is the total overlap capacitance. The equation shows two zeros and two poles for this model. Assuming the poles and zeros are far from the cutoff point (for linear assumption at the point in Bode plot), the cutoff frequency expression is derived as:

$$f_T = \frac{g_{mi}r_{oi}}{2\pi\,(g_{mi}C_{OV}R_C r_{oi} + (2R_C + r_{oi})(C_{OV} + C_{ch}))} = \frac{g_m}{2\pi(C_{tot} - g_m R_C C_{ch})} \tag{27.31}$$

The simplification of the above equation shows that the major difference between Fig. 27.37a, b comes from the term $g_m R_C C_{ch}$. As g_m is a term that already contains the R_C, it is preferable to consider this term as a function of independent variables. Thus, by substituting the g_m term, the expression of $g_m R_C$ is:

$$g_m R_C = \frac{g_{mi}r_{oi}R_C}{g_{mi}r_{oi}R_C + 2R_C + r_{oi}} \tag{27.32}$$

As g_{mi}, r_{oi} and R_C are independent values depending on semiconductor and interface properties with positive values, the whole term should be smaller than one. This indicates that the fraction C_{ch} is of the total capacitance that plays an important role in determining whether the two models become identical. In the case when C_{OV} is dominant over C_{ch} or when the value of R_C is very small or close to zero, the $g_m R_C C_{ch}$ term can then be omitted, and thus Eq. (27.31) becomes the same as Eq. (27.29). The CMOS model can be used despite the connection of $R_C s$ as in these cases the two high-frequency models are equivalent.

In the case when the value of C_{ch} is at least of the same order of magnitude as C_{OV} or higher, the $g_m R_C C_{ch}$ term can reduce around 50% of the total capacitance (for the case when $g_{mi}R_C \approx 1$), making the two models very different in terms of modelling of the cutoff frequency. This also indicates that the CMOS model can be inaccurate especially when the contact resistance and overlap capacitance are big and small, respectively. As the contact resistance is known to be big in TFTs (from a few kΩ to several 100 kΩ) and the reduction of overlap capacitance is preferable at the processing side for the sake of making faster TFTs, the inaccuracy of CMOS model might exist in most TFTs and may become more significant as processing technique becoming mature (e.g. for self-aligned TFTs, the overlap capacitance is close to zero).

The other point to notice is that the assumptions used to derive Eq. (27.31) is supported by calculating the actual values of zeros and poles of the transfer function. As the extra zeros and poles are at way higher frequency compared with the cutoff frequency, they are not of concern as the transistor is dominated by capacitor effects and is not working properly at the frequency range.

Model Validation

From the theoretical analysis of small-signal modelling, we know that the TFT small-signal model can be very different from CMOS model when the contact resistance and overlap capacitance are big and small, respectively. In this section, we will evaluate the amount of difference by measurement of IGZO TFTs' cutoff frequency and the dominating s-parameters.

Measurement Setup

In order to evaluate the small-signal model, we need to measure the current gain of the TFT and compare the cutoff frequency to see the model difference quantitatively. The common way of measuring the cutoff frequency of a transistor is to use a network analyser to measure the s-parameters and convert them to h-parameters. The calculated h_{21} directly reflects the short-circuit current gain of the device. Here, we use Keysight E5061B network analyser (ENA) calibrated by CS-11 calibration substrate provided by GGB Industries, Inc. The standard measurement setup is shown in Fig. 27.38. The bias-T provides DC bias to the TFT under test and separates the small signal input and output from the DC circuitry. The TFT is then connected to the ENA ports for s-parameter measurement.

The main reason for choosing the analyser is that it can provide low-frequency measurement down to 5 Hz. In contrast, most of the network analysers on the market are targeted above 100 kHz range, which is already a range close to TFT's cutoff. In the next section, we will see that even with the network analyser, low-frequency measurement is still hard, as the TFTs are more resistive at low frequencies.

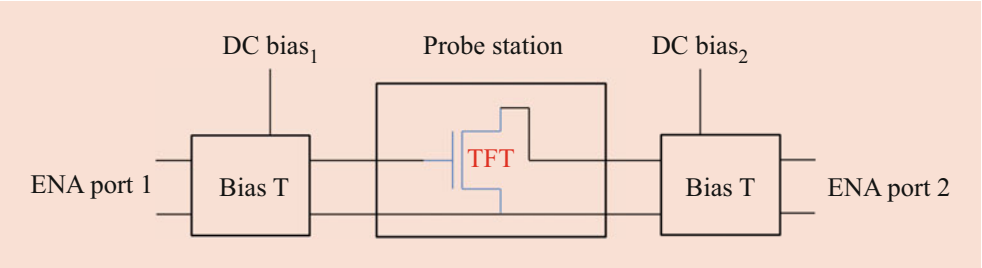

Fig. 27.38 Measurement setup for f_T and s-parameters

The ENA in use can only provide DC bias at port 1. Therefore, the bias-T at port 1 is already included inside the ENA. We still need to find a bias-T for port 2. As low frequency is important for our measurement, we choose Picosecond 5546 bias-T for this purpose. The low 3 dB frequency is 3.5 kHz, the lowest we managed to find on the market. We choose CS-11 calibration substrate and model 10 high-frequency probe (from DC to 6 GHz) from GGB Industries, Inc. for the purpose of calibration, as the parasitics on the wires and the probes, etc. should be calibrated out before s-parameter measurement.

The DC bias conditions are chosen to be $V_{GS} = 8\,V$ $V_{DS} = 15\,V$ to make sure the TFT is working in the saturation region. It is to be noted that from the output characteristic, (Fig. 27.39) the TFT saturates later than $V_{GS} - V_T$, which is the saturating point for CMOS. This is explained as the voltage drop on the contact resistance effectively reduced the $V_{D'S'}$ on the internal TFT (Fig. 27.33). The device under test has following physical and geometrical parameters: $t_s = 50\,nm$, $V_T = 1.6\,V$, $C_{ox} = 30\,nF/cm^2$, $\mu_0^* = 8.6\,cm^2/V{\cdot}s$. The device with *W/L* ratio of 100 µm/10 µm is used for model validation, and 50 µm/10 µm is used for stress measurement.

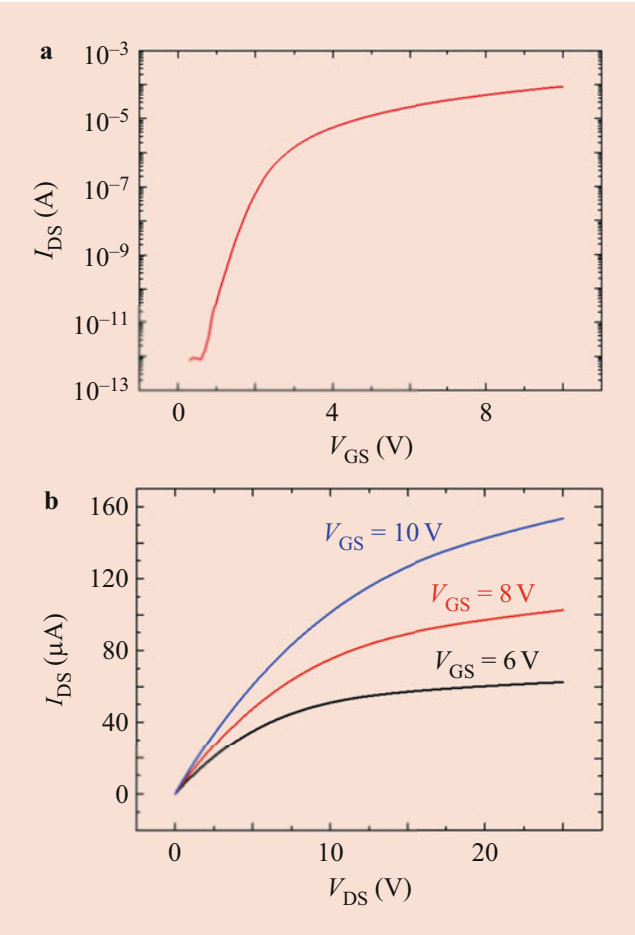

Fig. 27.39 I-V characteristic of the TFT under test. (**a**) Transfer characteristic. (**b**) Output characteristic

s-Parameters and f_T Measurement

As f_T is calculated through s-parameter measurements, it is essential to understand how it is calculated and evaluate the measurement procedure as TFTs might have specific properties which may make the measurement very different from standard CMOS.

The most significant difference for TFTs is that the devices are very resistive. As TFTs are normally biased with a few volts to 20 V level and the output current is normally around a few or a few tens µA, the corresponding resistances are around 100 kΩ or even a few MΩ level. Resistance at this level is huge, particularly in s-parameter measurement, as s-parameters are usually normalized with a characteristic resistance of 50 Ω or 75 Ω. For single-port measurement such as S_{11} and S_{22}, the relation between corresponding impedance(Z_L) and $S_{xx}(S_{11}/S_{22})$ is:

$$S_{xx} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{27.33}$$

where $Z_0 = 50\,\Omega$ is the characteristic resistance. Here, as Z_L is much larger than Z_0, the S_{11} *or* S_{22} values should be very close to 1 (or very close to 0 dB). This fact only changes at higher frequencies when the impedance of the capacitors drops significantly. As discussed before, the frequency range of concern is the range below the cutoff frequency. The

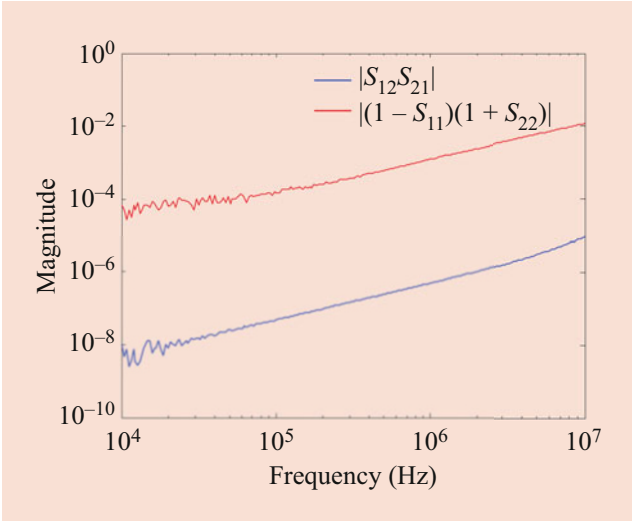

Fig. 27.40 Comparison between terms of $(1-S_{11})(1+S_{22})$ and $S_{12}S_{21}$

impedance of the capacitor at the frequency range should be comparable with the internal components; otherwise, the circuit performance will be dominated by the capacitors. Therefore, the assumption will be valid in the whole frequency range of concern.

S_{11} and S_{22} are also called reflection coefficient. It expresses the ratio of the reflected power to the incident power of an electromagnetic wave. As the reflection coefficient is close to 1, the transmission coefficients (S_{12} and S_{21}) should be small as most of the power are reflected rather than transmitted. The experiment shows these two parameters are very close to 0.

Now as we know the estimated value of the four parameters, we need to evaluate the equation of h_{21} Eq. (27.34).

$$h_{21} = -\frac{2S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21}} \tag{27.34}$$

Here, the major complexity comes from the denominator. Therefore, the next question is whether the denominator is dominated by some part of the terms or not. It is pretty hard to tell which part of the denominator is more dominant intuitively, as both terms of $(1-S_{11})(1+S_{22})$ and $S_{12}S_{21}$ are close to 0. One could estimate from the assumption that $1-S_{11}$ has a similar order of magnitude compared with S_{12} or S_{21} to conclude that $(1-S_{11})(1+S_{22})$ term dominates over $S_{12}S_{21}$. A further check from experiment based on the IGZO TFTs shows that the former term is four orders bigger than the latter term as shown in Fig. 27.40. Therefore, the $S_{12}S_{21}$ term can be omitted when calculating the current gain.

Further, as S_{22} is very close to 1, the product of $1-S_{11}$ and $1+S_{22}$ is much more sensitive to the change of S_{11} than S_{22}. The final approximation of the equation is then as follows:

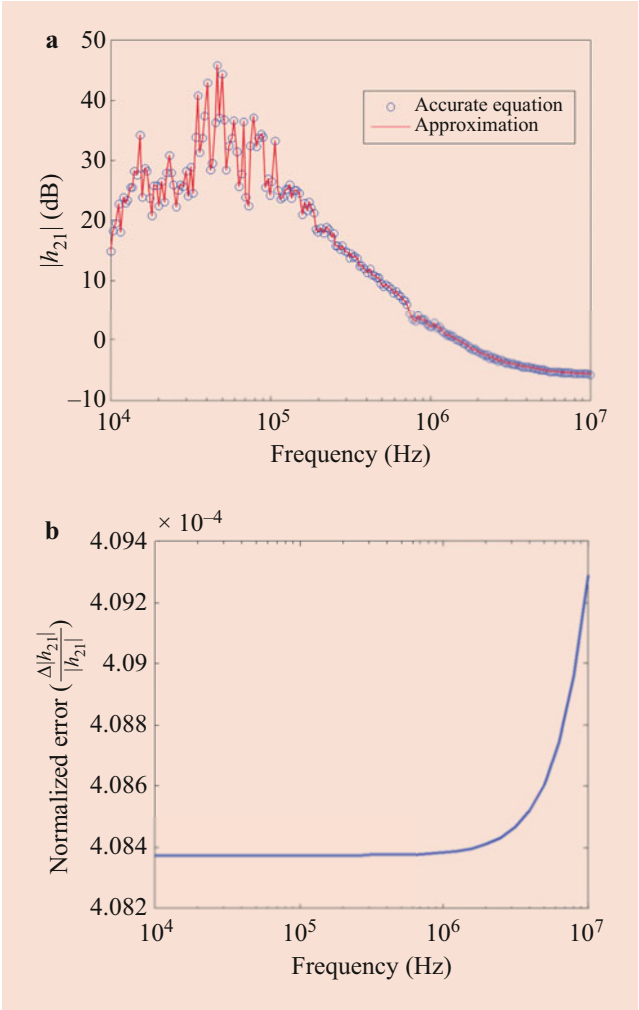

Fig. 27.41 Comparison between Eq. (27.34) and its approximation Eq. (27.35). (**a**) Calculated h_{21}. (**b**) Normalized error

$$A_i = |h_{21}| \approx |\frac{S_{21}}{S_{11}-1}| \tag{27.35}$$

Note that the approximation above is very accurate as the dominance of parameters is so significant. A comparison based on experiment result is shown in Fig. 27.41. The estimation gives 0.04% error in calculating the current gain of TFT within the frequency of concern. Therefore, Eq. (27.35) can be used in the measurement of current gain or f_T of TFTs without the measurements of S_{12} and S_{22}.

Now from the derivation and verification above, we know the dominating parameters for TFT f_T measurement are S_{11} and S_{21}. Thus, to evaluate the difference of TFT model and CMOS model, we need to evaluate and analyse the two parameters in both models. As both the two measurements need to connect a matched load at port 2 of the network, the equivalent circuit for the measurements is identical as shown in Fig. 27.42. The modelling of each parameter based

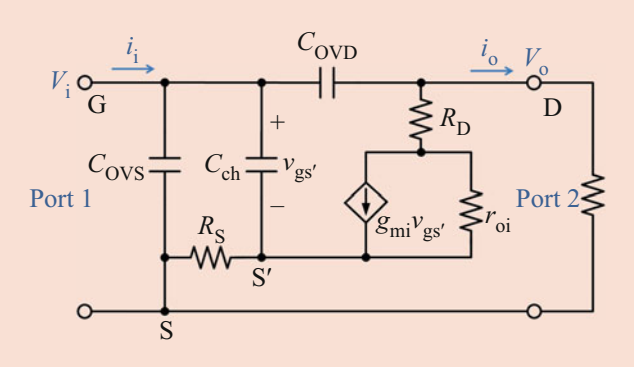

Fig. 27.42 Equivalent circuit for S_{11} and S_{21} measurement

on the equivalent circuit will be discussed in the following subsections. And the simulation will be based on the static and dynamic parameters extracted in Sect. 27.2.1.

S_{11} Measurement and Analysis

Figures 27.40 and 27.41 shows that the measurement at lower frequencies is very noisy especially when S_{11} is involved. The main reason is the contribution of the $1 - S_{11}$ term. As discussed before, the S_{11} parameter is very close to 1 due to the near open-circuit characteristic of capacitors at low frequencies. Therefore, the value of $1-S_{11}$ highly depends on the measurement accuracy of S_{11}. According to the datasheet of the network analyser E5061B, the measurement accuracy for S_{11} with different calibration kit is around 0.03 and 2 degree for magnitude and phase measurement respectively, when average factor equals to 1 and 10 Hz bandwidth is selected. However, in order to measure the parameters for the device under test (DUT), the accuracy is not enough, as the values of the S_{11} magnitude and phase are one order smaller than the corresponding accuracies.

Further, after checking the measurement results, we noticed that the major uncertainty comes from the shift of the machine property over time. As this shift is rather slow compared with one cycle of a frequency sweep, we choose to do two quick sweeps with and without the device connected to measure the S_{11} value. The open-circuit values are then subtracted from the measurement results to cancel the property shift of the machine.

The measurement and simulation results are shown in Fig. 27.43. As can be seen, TFT model fits much better compared with adapted CMOS model. The major difference comes from the magnitude measurement as the measured curve drops, which suggests that there's at least an extra pole for the S_{11} expression of TFT model higher but close to the frequency of concern. The calculation based on CMOS model gives the S_{11} model below:

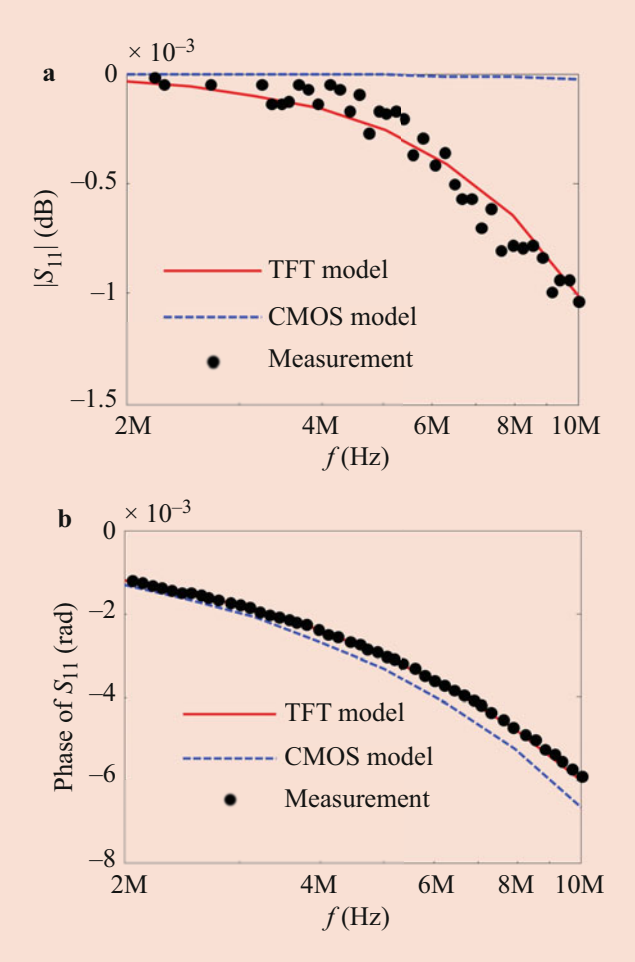

Fig. 27.43 Magnitude and phase measurement and simulation for S_{11} parameter based on TFT model and adapted CMOS model. (**a**) Magnitude. (**b**) Phase

$$S_{11_{CMOS}} \approx -\frac{-g_0^2+(C_{OVS}+C_{ch})g_0 s+C_{OVD}(C_{OVS}+C_{ch})s^2}{g_0^2+(2g_0C_{OVD}+g_0(C_{OVS}+C_{ch}))s+C_{OVD}(C_{OVS}+C_{ch})s^2} \tag{27.36}$$

where $g_x = \frac{1}{r_x}$ is the conductance of the corresponding resistor. The conductance terms are used to make the equation look simpler. An approximation is also used to simplify the equation based on the assumption that $g_0 \gg g_m$ and $g_0 \gg g_o$. This is particularly true in the case of TFT because of the high resistance of TFT devices. For example, $1/g_m$ is normally around a few kΩ to a few 100 kΩ, and r_o is around a few MΩ. However, the characteristic resistance is 50 Ω. Therefore, the conductance of the characteristic resistance g_0 should be more dominant compared with all other resistances and conductances in the small-signal model of TFT (or the

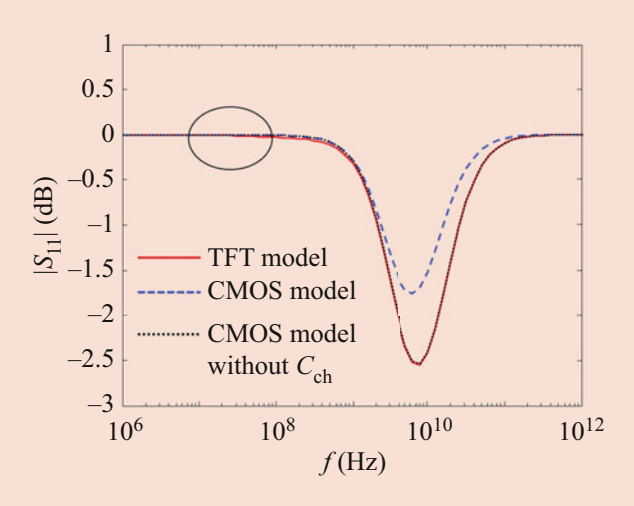

Fig. 27.44 S_{11} simulation of the TFT and CMOS models

adapted CMOS one). The assumption is also used in the derivation of S_{11} of TFT model. This model suggests that the equation has two zeros and two poles. Calculation based on Eq. (27.36) shows that the two zeros are at 3.4462 GHz and 10.853 GHz and the 2 poles at 2.4898 GHz and 15.022 GHz. As the zeros and poles are all far above the frequency of concern (i.e. below 10 MHz), the S_{11} modelled by the CMOS model would remain at 1 at the frequency range as suggested in Fig. 27.43a (which suggests a very close to open-circuit behaviour).

The calculation based on the equivalent circuit shown in Fig. 27.42 gives the S_{11} expression as follows:

$$S_{11_{\mathrm{TFT}}} = -\frac{-g_{\mathrm{tot}}g_{\mathrm{c}}g_0^2+a_1s+a_2s^2+(g_{\mathrm{c}}+g_{\mathrm{oi}})C_{\mathrm{ch}}C_{\mathrm{OVS}}C_{\mathrm{OVD}}s^3}{g_{\mathrm{tot}}g_{\mathrm{c}}g_0^2+b_1s+b_2s^2+(g_{\mathrm{c}}+g_{\mathrm{oi}})C_{\mathrm{ch}}C_{\mathrm{OVS}}C_{\mathrm{OVD}}s^3}, \tag{27.37}$$

where $g_{\mathrm{tot}} = g_{\mathrm{mi}} + g_{\mathrm{c}} + 2g_{\mathrm{oi}}$

$$a_1 = \left[g_{\mathrm{c}}g_{\mathrm{tot}}C_{\mathrm{OVS}} + g_{\mathrm{c}}(g_{\mathrm{c}}+g_{\mathrm{oi}})C_{\mathrm{ch}}\right]g_0 - (g_{\mathrm{c}}+g_{\mathrm{oi}})g_0^2C_{\mathrm{ch}},$$

$$a_2 = (g_{\mathrm{c}}+g_{\mathrm{oi}})C_{\mathrm{ch}}C_{\mathrm{OVS}}g_0,$$

$$b_1 = \left[g_{\mathrm{c}}g_{\mathrm{tot}}C_{\mathrm{OVS}} + 2g_{\mathrm{tot}}g_{\mathrm{c}}C_{\mathrm{OVD}} + (g_{\mathrm{c}}+3g_{\mathrm{oi}})g_{\mathrm{c}}C_{\mathrm{ch}}\right]g_0 + (g_{\mathrm{c}}+g_{\mathrm{oi}})C_{\mathrm{ch}}g_0^2,$$

$$b_2 = (g_{\mathrm{c}}+g_{\mathrm{oi}})g_0C_{\mathrm{ch}}(C_{\mathrm{OVS}}+2C_{\mathrm{OVD}}).$$

Here, the equation has three zeros and three poles. To further evaluate the difference between the two models, we simulated their S_{11} parameters. The simulation results are shown in Fig. 27.44. Just as the figure suggests, two zeros lie between two poles to make a valley of the magnitude curves for both models. However, these poles and zeros are at much higher frequencies compared to the cutoff of the transistor. Therefore, the simulation results only show a flat line below 10 MHz for CMOS model. As for the TFT model, the numeric calculation shows that there are three poles at 54.755 MHz, 2.8314 GHz, and 19.389 GHz. The zeros are at 54.947 MHz, 4.5660 GHz, and 11.981 GHz. The two zeros and two poles at GHz level have similar values compared with the CMOS model to make a similar shape of the curve at very high frequency. However, they would not create much difference at the low-frequency range of our concern either. The major difference we've noticed is the extra zero and pole at 54.947 MHz and 54.755 MHz, respectively. These two points are pretty close to the cutoff frequency and the frequency of concern. From further inspection of Figs. 27.43 and 27.44, we notice that it is these pole and zero that cause a slight drop of the S_{11} magnitude. As the pole is slightly smaller than the zero (although only by less than 1%), the magnitude starts to drop a little before the effect is cancelled by the zero. This drop distinguishes the two models at around 10 MHz range as the measurement in Fig. 27.43 suggests. This also suggests that the TFT model (with the contact resistance and the separation of the channel and overlap capacitance) captures an extra pole and zero, which results in better accuracy than the CMOS model.

It can be noted that $|S_{11}|$ equals to 0 dB (or 1) at both very low frequencies and very high frequencies. This can be explained by the connection of the C_{OVS} as it acts as open circuit at low frequencies ($S_{11} = 1$) and short circuit ($S_{11} = -1$) at high frequencies.

Here, as the major accuracy improvement comes from the extra zero and pole, it is worth finding the exact expression of their analytic form. The accurate expressions can be directly extracted from Eq. (27.37) by solving the cubic equations. However, the expressions become too long for the purpose of estimating the positions of the extra zero and pole. Alternatively, we discovered that by taking out the C_{ch} in CMOS model, the simulation results of the two models become very similar at high frequencies (shown in Fig. 27.44). Therefore, we could compare the coefficients of Eqs. (27.37) and (27.36) (taken out the C_{ch} term) to find the estimated expression of the extra zero and pole, assuming that the CMOS model contains all the poles and zeros except the extra ones.

Considering the matching of coefficients, we found the estimated expressions as:

$$\begin{cases} f_{\mathrm{pe}} = -\dfrac{g_{\mathrm{tot}}g_{\mathrm{c}}g_0}{2\pi(g_0+g_{\mathrm{c}})(g_{\mathrm{c}}+g_{\mathrm{oi}})C_{\mathrm{ch}}} \\ f_{\mathrm{ze}} = -\dfrac{g_{\mathrm{tot}}g_{\mathrm{c}}g_0}{2\pi(g_0-g_{\mathrm{c}})(g_{\mathrm{c}}+g_{\mathrm{oi}})C_{\mathrm{ch}}} \end{cases} \tag{27.38}$$

where f_{pe} is the frequency of the extra pole and f_{ze} is the frequency of the extra zero. Here, the expressions give a rather accurate estimation of the extra pole and zero of 54.763 MHz

and 54.946 MHz, respectively, while the numeric calculation gives 54.755 MHz and 54.947 MHz. Here, with the approximation of the extra zero and pole, one can easily draw the S_{11} curves without simulating the more complicated equivalent circuit. It also provides support for the possibility of fitting a S_{11} measurement with one pole and one zero.

S_{21} Measurement and Analysis

As for S_{21}, the simulation and measurement results are shown in Fig. 27.45. The results show that the difference of S_{21} between models is less significant compared with S_{11}. This is because the parameter varies much in a log scale axis (dB), and, therefore, the difference is not visibly prominent in comparison with that of S_{11}. For example, the measurement value at 8 MHz is $|S_{21}| = 2.85 \times 10^{-3}$. The modelled value are $|S_{21_{\text{TFT}}}| = 2.88 \times 10^{-3}$ (yielding 1.1% error) and $|S_{21_{\text{COMS}}}| = 2.69 \times 10^{-3}$ (yielding 5.6% error).

The analytic expression of S_{21} in CMOS model is shown as Eq. (27.39):

$$S_{21_{\text{CMOS}}} = \frac{2g_0(sC_{\text{OVD}} - g_{\text{m}})}{g_0^2 + (2C_{\text{OVD}} + C_{\text{OVS}} + C_{\text{ch}})g_0 s + C_{\text{OVD}}(C_{\text{OVS}} + C_{\text{ch}})s^2} \tag{27.39}$$

The equation shows that there are two poles and one zero in the model. Calculation based on the equation shows that the zero is at 6.107 MHz and the two poles are at 2.490 GHz and 15.02 GHz. Again, as the poles are all far above the frequency of concern, they would not affect the measurement results below 10 MHz. The result is that there's only one dominant zero within the frequency range. The other point that should be noticed is that at very low frequencies, Eq. (27.39) yields to:

$$S_{21_{\text{CMOS}}} = -\frac{2g_{\text{m}}}{g_0} \tag{27.40}$$

Here, the $g_0 = 1/50\,\Omega^{-1}$ is a known value. Therefore, the S_{21} measurement can directly reflect the small signal g_{m} for the CMOS model. As discussed in Sect. 27.2.2, the TFT and CMOS models are equivalent at low frequencies as the capacitances can be ignored. Therefore, this g_{m} can also be used to extract the g_{mi} for TFT model at lower frequencies.

As for TFT model, the equivalent circuit for the S_{21} calculation is the same as the one used for S_{11} as the equivalent connection for the measurements is the same (Fig. 27.42). Hence, we could derive the equation of S_{21} as below:

$$S_{21_{\text{TFT}}} = 2g_0 \frac{-g_{\text{c}}^2 g_{\text{mi}} + (g_{\text{c}} g_{\text{tot}} C_{\text{OVD}} + g_{\text{oi}} g_{\text{c}} C_{\text{ch}})s + (g_{\text{c}} + g_{\text{oi}})C_{\text{OVD}} C_{\text{ch}} s^2}{g_{\text{tot}} g_{\text{c}} g_0^2 + c_1 s + c_2 s^2 + (g_{\text{c}} + g_o)C_{\text{ch}} C_{\text{OVS}} C_{\text{OVD}} s^3}, \tag{27.41}$$

where,

$$c_1 = (g_{\text{c}} + g_{\text{oi}})C_{\text{ch}} g_0^2,$$
$$c_2 = (g_{\text{c}} + g_{\text{oi}})C_{\text{ch}}(C_{\text{OVS}} + 2C_{\text{OVD}})g_0.$$

Here, the equation shows two zeros and three poles for TFT model. Based on the parameters of the device under test, we have that the zeros are at 5.501 MHz and 60.90 MHz and that the poles are at 54.76 MHz, 2.831 GHz, and 19.39 GHz. Similar to the case for S_{11}, there's one extra zero and one extra pole at 60.90 MHz and 54.76 MHz, respectively. These extra zero and pole would also contribute a slight drop on the magnitude of S_{21} as they are very close together, just as the case for S_{11}. The difference here is that there's a dominant zero at 5.501 MHz, which is different to the 6.107 MHz zero for the CMOS model. Hence, the difference of the dominant zero contributes to the major difference between the CMOS and TFT model. And the difference caused by the extra zero and pole becomes less prominent. Here, the dominant zero for S_{21} can be expressed as:

$$f_{z0_{\text{TFT}}} = \frac{g_{\text{c}}\left(\sqrt{(g_{\text{oi}}C_{\text{ch}} + g_{\text{tot}}C_{\text{OVD}})^2 + 4g_{\text{mi}}(g_{\text{c}} + g_{\text{oi}})C_{\text{ch}}C_{\text{OVD}}} - g_{\text{oi}}C_{\text{ch}} + g_{\text{tot}}C_{\text{OVD}}\right)}{4\pi C_{\text{ch}}C_{\text{OVD}}(g_{\text{c}} + g_{\text{oi}})} \tag{27.42}$$

whereas the dominant zero for CMOS model can be express as:

$$f_{z0_{\text{CMOS}}} = \frac{g_{\text{m}}}{2\pi C_{\text{OVD}}} \tag{27.43}$$

While CMOS model gives a simpler solution for the dominant zero for the S_{21} parameter, it does not count the contribution of the channel capacitance (C_{ch}). The TFT model, however, accurately models the dominant zero with the contribution of C_{ch} but yields a much more complicated equation.

Again, at low frequencies, Eq. (27.41) yields to:

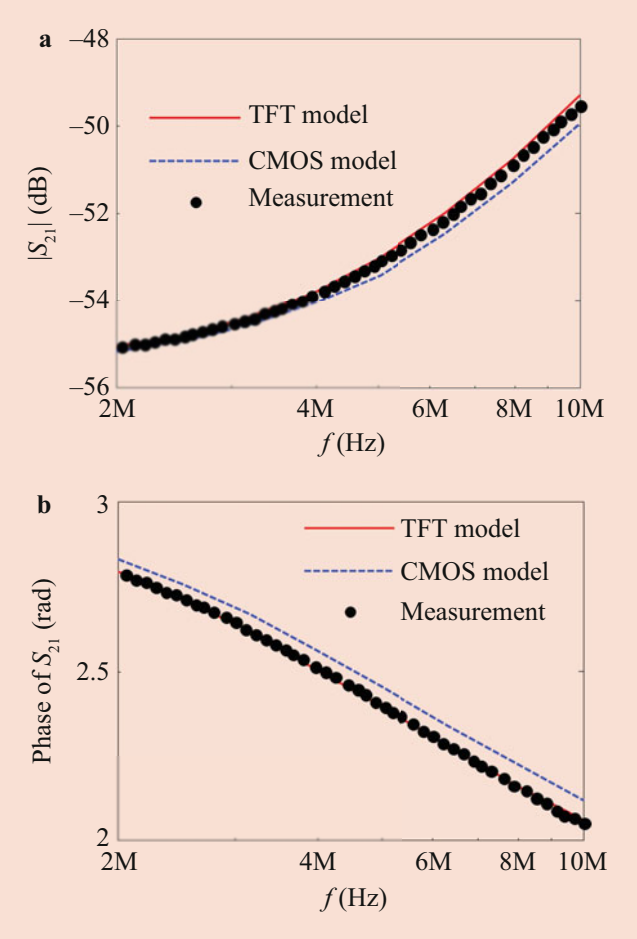

Fig. 27.45 Magnitude and phase measurement and simulation for S_{21} parameter based on TFT model and adapted CMOS model. (**a**) Magnitude. (**b**) Phase

$$S_{21_{TFT}} = \frac{-2g_c g_{mi}}{g_{tot} g_0} \tag{27.44}$$

Changing the conductance terms into resistance terms and combining Eq. (27.24), we have:

$$S_{21_{TFT}} = \frac{-2g_{mi} r_{oi}}{(g_{mi} r_{oi} R_C + 2R_C + r_{oi}) g_0} = -\frac{2g_m}{g_0} \tag{27.45}$$

This is exactly Eq. (27.40). This confirms that the CMOS and TFT model can be equivalent at low frequencies.

f_T Measurement and Analysis

As discussed, we can use Eq. (27.35) to calculate the short-circuit current gain of the TFT with enough accuracy. Therefore, we used the measured S_{11} and S_{21} to derive the current gain of the TFT under test and then use a linear fitting to get the value of the f_T.

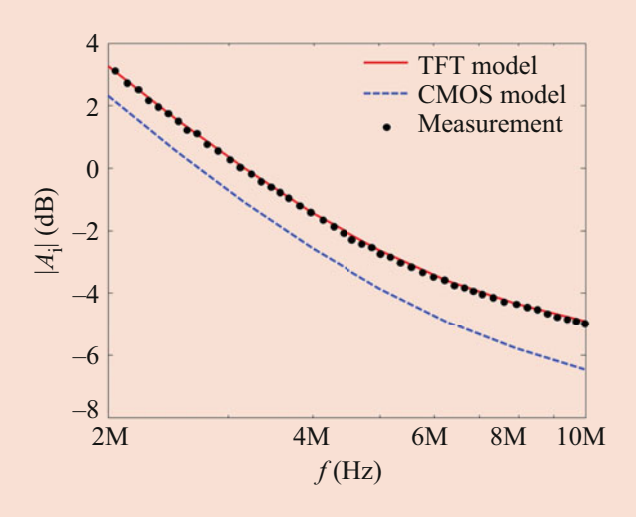

Fig. 27.46 S_{11} simulation of the TFT and CMOS models

The measurement results of f_T along with simulations based on the TFT and CMOS model are shown in Fig. 27.46. The measurement results show a cutoff frequency of 3.11 MHz, while the proposed TFT and CMOS models predict cutoff frequencies of 3.14 MHz and 2.72 MHz, respectively. This yields an error of 1% and 12.5%, respectively.

Here, we proved that the TFT model presented here is more accurate to predict the f_T compared with the CMOS counterpart. However, the measurement results of $|h_{21}|$ or $|A_i|$ only became consistent with the model at frequencies around MHz level. At lower frequencies, the measurement became very noisy as illustrated in Fig. 27.41. However, as shown in the analysis of Eq. (27.30), the $|A_i|$ curve should be a straight line at lower frequencies as it is dominated by a single pole at 0 Hz. The main reason for the discrepancy is the measurement accuracy of S_{11}, especially at low frequencies. As the value of $|S_{11}|$ is very close to, if not exactly equal to, 0 dB at very low frequencies, the noise of the measurement becomes the major contribution to its value. Therefore, as Eq. (27.35) suggested that the accuracy of $|A_i|$ depends on the subtraction of S_{11} and 1 (0 dB), the noise of the measurement at this frequency range would dominate the results of $|A_i|$ and make them unreliable. This brings a concern for the measurement of other TFTs with lower cutoff frequency, which means the frequency of concern is lower, or with smaller size, which means that the capacitances are smaller, making the gate-source port behave even closer to open circuit. Therefore, we should use a fitting method to fit the S_{11} parameter before using its value to calculate $|A_i|$ for the cases described above. More detailed discussion regarding S_{11} fitting will be discussed in the next subsection and also be used to measure the V_T shift effect in f_T measurement.

f_T and V_T Shift

In this subsection, we will discuss the effect of the V_T shift. As the accuracy of TFT model is proved in the s-parameter and f_T measurements, we would focus on the TFT model.

V_T shift is another important factor for TFTs, as this is one of the major concerns in TFT-based circuit designs, especially where TFTs' analogue properties are of concern, for example, in RFID tags. For the case of the small-signal model, the TFT is used as a voltage-controlled current source for the input of the small signal. Therefore, it is imperative to consider the impact of V_T shift on small-signal model.

In order to examine its influence on the small-signal behaviour, a constant bias stress measurement is needed to measure both f_T and V_T of the transistor. However, simultaneous measurement of the two parameters is not practical as the measurements of them need two different connections, i.e. f_T measurement needs network analyser and isolation for DC bias and small-signal input and output; however, the V_T measurement needs I-V sweep to measure the transfer characteristics (which we use KEITHLEY 4200 to measure). Therefore, we need to find an alternative way to measure both parameters other than keep switching between different measurement platforms.

Here, we decided to use two different constant bias measurements and connect the two parameters through g_m as a bridge. The basic idea is that although f_T and V_T cannot be obtained simultaneously, the g_m value can be obtained together in the measurements of both. In specific, g_m can be obtained through the derivative of transfer characteristics as discussed in Sect. 27.2.2. It can also be obtained through low-frequency S_{21} measurement as discussed in Sect. 27.2.2. Also, as V_T directly affects the value of g_m (g_{mi} is considered to be near linearly related to the overdrive voltage ($V_{GS}-V_T$)) and g_m also relates with f_T, g_m can be a perfect link between the two measurements.

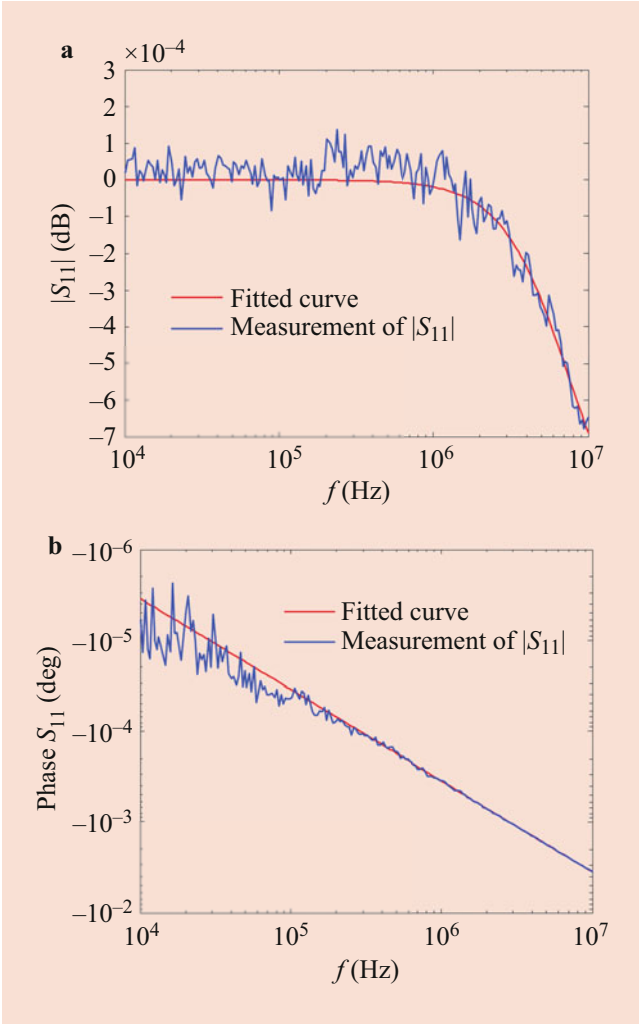

Fig. 27.47 Magnitude and phase measurement and fitting for S_{11} parameter based on single pole and zero approximation. (**a**) Magnitude. (**b**) Phase

f_T and g_m

As discussed in Sect. 27.2.2, a fitting method should be applied to the S_{11} data to obtain a better low-frequency response for the current gain result. Here, as the device under test is smaller in channel width and the cutoff frequency is lower, it is necessary to use the method for better accuracy. The measurement result of S_{11} is shown in Fig. 27.47. The results are fitted using one zero and one pole approximation following Eq. (27.46):

$$S_{11} \approx \frac{1+as}{1+bs} \tag{27.46}$$

where a and b are fitting parameters. The measurement results are fitted using MATLAB. Here, as illustrated in Fig. 27.47, the measurement results are not reliable below 1 MHz for magnitude measurement and below 100 kHz for phase measurement. The major cause of the unreliable results is that the value of $|S_{11}|$ or its phase drops below the noise level at low-frequency range. Therefore, the fitting method is imperative to obtain a reasonable low-frequency response. In addition, as the cutoff frequency for the device under test in this subsection is around 1.5 MHz, which is close to the unreliable range of $|S_{11}|$ (below 1 MHz), fitting method is even more important for a better accuracy, especially for capturing the small change of f_T caused by V_T shift.

In order to capture the f_T change under stress measurement, we kept the bias stress for 8 hours and measure the corresponding s-parameters. The converted $|h_{21}|$ with and without the fitting of S_{11} are shown in Fig. 27.48. As illustrated, the $|h_{21}|$ values without fitting are rather random at lower frequencies, which cannot reliably capture the change of the curves versus stress time. However, with fitted S_{11},

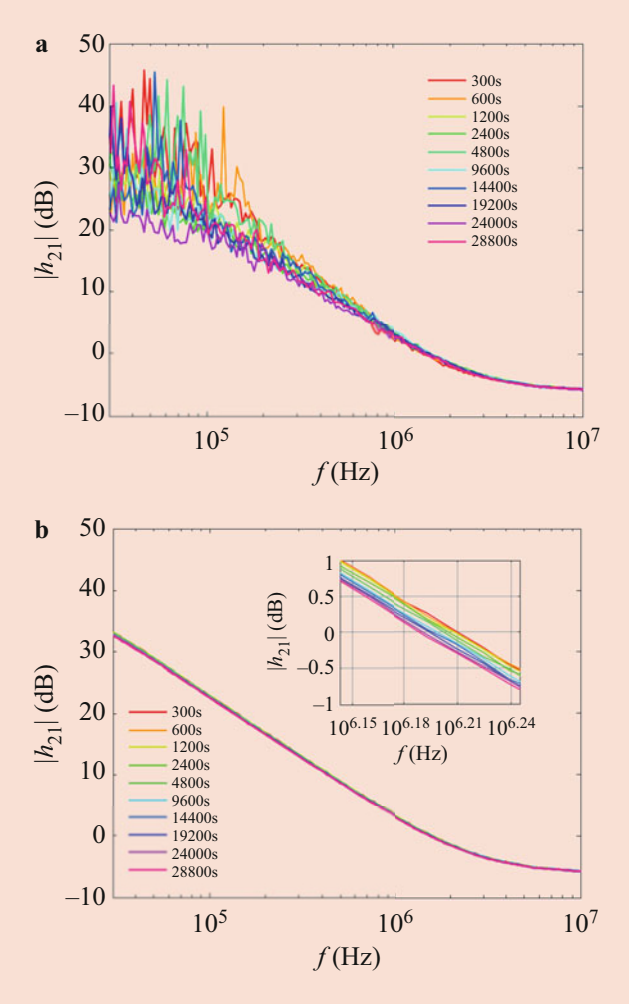

Fig. 27.48 h_{21} results with and without S_{11} fitting. (**a**) with S_{11} fitting. (**b**) without S_{11} fitting

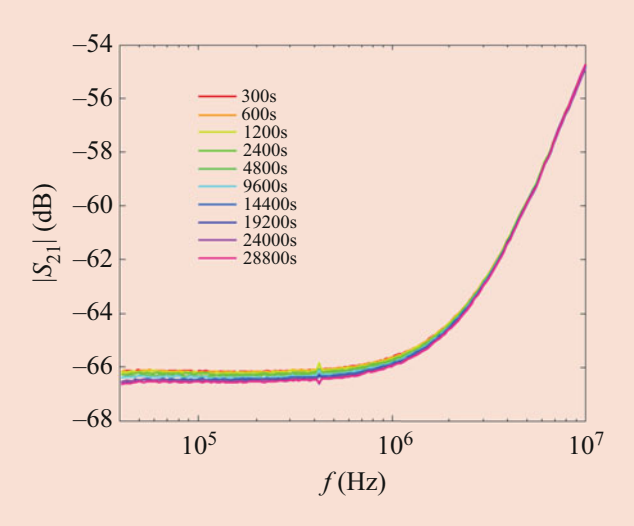

Fig. 27.49 S_{21} measurement showing low-frequency range for g_m extraction

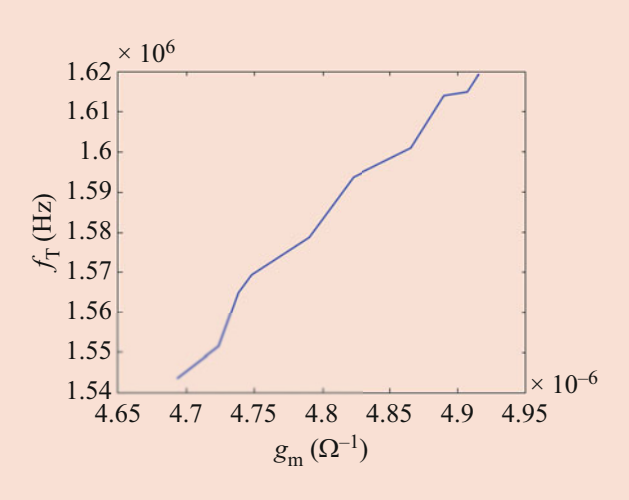

Fig. 27.50 f_T vs. g_m relation through s-parameter measurement

we can clearly capture the drop of the cutoff frequency when the stress time increases, as illustrated in the inset of Fig. 27.48b.

The low-frequency measurement of S_{21} can be used to extract g_m following a derivation from Eq. (27.45):

$$g_m = \frac{g_0|S_{21}|}{2} \tag{27.47}$$

Here, we can use the flat part of the $|S_{21}|$ measurement and calculate the average of $|S_{21}|$ as shown in Fig. 27.49. The value of $|S_{21}|$ drops when bias time increases, which is consistent with the drop of g_m caused by the V_T shift.

By extracting g_m through Fig. 27.49 and the corresponding f_T through Fig. 27.48b, we can get the f_T vs. g_m relation as shown in Fig. 27.50. The results show a linear approximation to Eq. (27.31).

g_m and V_T

The g_m vs. V_T relation can be measured through I-V measurement of the device. The TFT under test was biased at $V_{GS} = 8$ V and $V_{DS} = 15$ V, and I-V sweep was done every logarithmic time interval in order to extract the g_m and V_T. The constant stress bias is disrupted for a short time due to the measurement. However, because the sweep time (V_T measurement) is much shorter compared with the bias time, we assume that the short pause for the constant stress can be omitted. Notwithstanding this, the results showed that V_T continued rising after the sweep and the extracted value is then used to extract the relation between g_m and ΔV_T. The extracted results are illustrated in Fig. 27.51.

Combining the results of Figs. 27.50 and 27.51, we can get the f_T vs. ΔV_T relation as illustrated in Fig. 27.52. The

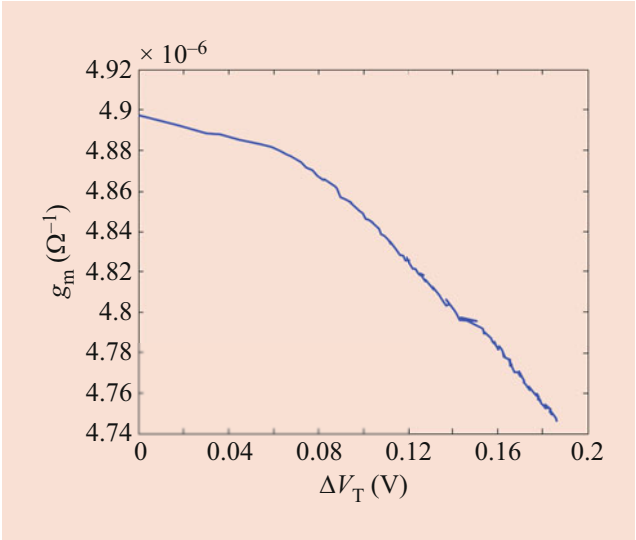

Fig. 27.51 g_m vs. V_T shift relation through stress measurement with I-V sweep

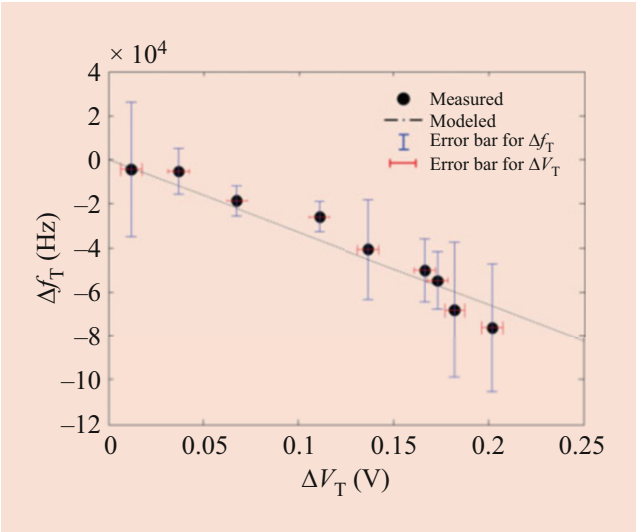

Fig. 27.52 Extracted Δf_T vs. V_T shift relation. The error bar here is the standard deviation of the fitting to obtain the corresponding result

corresponding V_T was obtained through cubic polynomial fitting of the curve in Fig. 27.51. The error bar here is the standard deviation of the fitting to obtain the corresponding result. In specific, the standard deviation of Δf_T was obtained from the linear fitting to obtain the corresponding f_T. The standard deviation of ΔV_T was obtained from the polynomial fitting of the curve in Fig. 27.51.

The ΔV_T increased to +0.2 V in total after the 10 h bias stress, and the respective Δf_T drops to 0.08 MHz almost linearly. This is due to the relatively small ΔV_T compared with V_{GS}, which leads to a first-order approximation of Eq. (27.31). From Eqs. (27.27) and (27.31), we have:

$$\Delta f_T \approx -\frac{r_{oi}(2R_C + r_{oi})(C_{OV} + C_{ch})}{2\pi\,(g_{mi}C_{OV}R_C r_{oi} + (2R_C + r_{oi})(C_{OV} + C_{ch}))}$$

$$K'\Delta V_T = \beta \Delta V_T \tag{27.48}$$

where β is the constant found to be about -3.2×106[Hz/V] for the examined TFT. Equation (27.48) allows estimating the shift in unity gain frequency with threshold voltage shift. Here, the coefficient β will be different for different material- and process-based TFTs.

27.2.3 Subthreshold Operation for Schottky Barrier TFTs

Introduction

Recent research has shown that biasing IGZO TFTs in deep-subthreshold region could improve the small-signal gain and significantly reduce the power consumption [18]. This is specifically useful in low-power applications such as sensor networks, biomedical sensing, etc. [193, 194].

While subthreshold operation in silicon-based CMOS devices had been intensively researched in the 1970s with great success in Swiss watch industry [195–198], the same in TFTs was only investigated until 2018 [1, 199].

Due to the low effective carrier mobility of TFTs (perhaps with polysilicon as an exception), TFT devices are generally working in a lower current level [57, 200]. Although this could limit the speed of the device, TFTs can be naturally suitable for low-speed and low-power applications. Biasing TFTs in subthreshold region could further reduce the power consumption to sub-nano-watt. This is particularly appealing as battery-less operation could be possible with this level of power consumption. However, as the subthreshold region is generally very narrow and current level is very sensitive to bias [201]. If a TFT has a steeper subthreshold slope (SS), a sensitivity of current variation is higher. The circuit design for this kind of devices could be challenging, although a steep SS provides a high intrinsic gain. Here, a high intrinsic gain is an important property for circuit design, so many approaches to get it have been introduced for the above-threshold operation [202–205]. For the subthreshold operation, it is known that a TFT with a Schottky contact source/drain have a steeper SS compared to an Ohmic contact TFT [18, 49, 206]; thus, a Schottky contact TFT provides a higher intrinsic gain within the subthreshold regime with a difficulty in a circuit design.

In this chapter, we will analyse several figures of merit for deep-subthreshold operating TFTs in analogue circuit design with the aim of providing a guideline of analogue circuit design capability of TFT devices using general architectures.

Subthreshold Model for IGZO TFTs

DC Model

The transfer curve of SB-TFTs in deep-subthreshold is reported to be linear in log scale, which is similar to CMOS devices. Here, we convert the model reported in [18] to a more macroscopic form to help analyse the performance. The equation for drain voltage (V_{DS}) > saturation voltage (v_{sat}) is derived as follows [18, 201]:

$$I_{ds} = I'_0 \exp\left(\frac{V_{GS} - V_T}{SS/\ln 10}\right)\left(1 + \frac{V_{DS}}{V_A}\right) \tag{27.49}$$

where I'_0 is the effective subthreshold reference current at V_T normalized by W and SS is the subthreshold slope. V_T is the threshold voltage, and V_A is the effective early voltage. The effective values can be derived as:

$$I'_0 \equiv A_J J_0 \exp\left(\frac{V_T - V_{ref}}{SS/\ln 10}\right) \tag{27.50}$$

where J_0 is the reference current density at V_{ref} and A_J is the junction area of the Schottky contact at the source and drain. In a Schottky contact TFT, A_J is proportional to the channel width (W) [18].

$$V_A \equiv n \cdot v_{th} \exp\left(\frac{v_{sat}}{n v_{th}}\right) \tag{27.51}$$

where n is the ideality factor of the junction and v_{th} is the thermal voltage.

With the above equations, we can easily connect the DC parameters to several important small-signal parameters, such as gm and ro.

Small-Signal Model

Although in previous publications [17, 18] we analysed the small-signal mode for TFTs and figured out that contact resistance can cause big errors using CMOS small-signal models, small-signal behaviour in subthreshold region can still be correctly modelled by CMOS model. This is due to the fact that channel capacitance in subthreshold is very small and normally negligible compared with overlap capacitance in TFTs.

Here, we consider C_{gs} and C_{gd} are mainly the overlap capacitance at source and drain side [17]. The tranconductance and output resistance can be calculated as:

$$\begin{aligned} g_m &= \frac{\ln 10}{SS} I'_0 \exp\left(\frac{V_{GS}-V_T}{SS/\ln 10}\right)\left(1 + \frac{V_{DS}}{V_A}\right) \\ &= \frac{\ln 10}{SS} I_{DS} \end{aligned} \tag{27.52}$$

$$r_o = \frac{I_{DS}}{V_A} \tag{27.53}$$

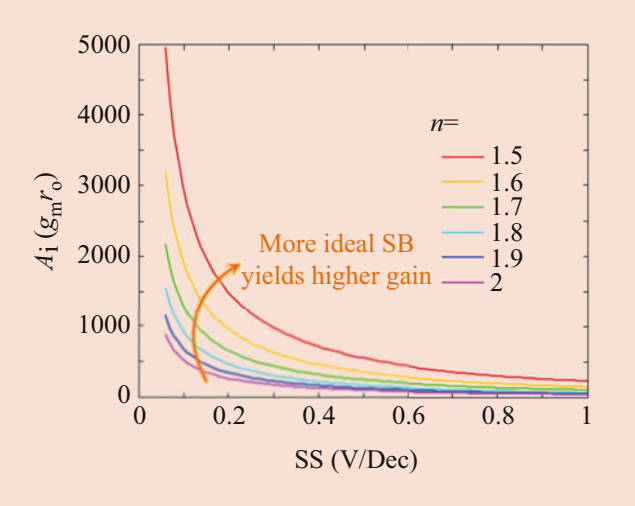

Fig. 27.53 Simulation result for the intrinsic gain (A_i) of the Schottky-Barrier IGZO TFT (SB-TFT). The parameter n is the ideality factor of the source-semiconductor junction

These equations take exactly the same form as the CMOS counterpart.

Figures of Merit

In this section, we consider several figures of merit for TFTs with emphasis in the subthreshold region. The model used for the simulation is based on the [18], and parameter values are extracted using the same samples. The W/L of the TFT under test is 50 μm/20 μm.

Intrinsic Gain

Intrinsic gain is an important figure of merit for analogue amplifier as it reflects the highest achievable single-stage gain for an amplifier. The simulation based on the model developed earlier is shown in Fig. 27.53. As seen, the intrinsic gain in subthreshold region is related with subthreshold slope and the ideality factor n of the Schottky junction.

The expression of the intrinsic gain can be approximated as:

$$A_i = g_m r_o = \frac{\ln 10}{V_A \cdot SS} \tag{27.54}$$

This suggests that intrinsic gain is reverse proportional to the SS of the TFT. By pushing the SS to its theoretical limit (60 mV), one could get over 1000 intrinsic gain with even less ideal Schottky-Barrier at source-semiconductor contact (smaller n). The expression also suggests that the value of intrinsic gain is rather independent on the bias of the transistor as long as it is working in subthreshold region.

Ideality factor n contributes to the intrinsic gain of the transistor because it controls the effective Early voltage (V_A) and thus influences the output resistance of the TFT.

Transconductance Efficiency

Transconductance efficiency (g_m/I_{DS}) is another important figure of merit for electron devices. It represents the efficiency of converting the bias current into an equivalent transconductance. For analogue TFT circuits, as the voltage bias is normally limited by the driving circuitry and the application, reducing the current bias while maintaining a high g_m also means reducing the power consumption while keeping the circuit performance.

As can be seen from Fig. 27.54, the highest g_m/I_{DS} can be obtained only at deep-subthreshold region for a TFT before it enters a transition region to above-threshold. This value remains a constant at deep-subthreshold due to the exponential nature of the TFT subthreshold behaviour. The simulation result also suggests that this value would increase if the TFT has a steeper subthreshold slope.

The expression of the g_m/I_{DS} value can be estimated as:

$$\frac{g_m}{I_{DS}} = \frac{\ln 10}{SS} \tag{27.55}$$

For above-threshold region, the g_m/I_{DS} value drops as the TFT enters above-threshold region, where the expression is:

$$\frac{g_m}{I_{DS}} = \frac{2+\alpha}{V_{GS} - V_T} \tag{27.56}$$

where α is the coefficient on the power law of TFT model and $\alpha = 0$ for the case of MOSFET [17–19]. Therefore, biasing a TFT at a high gate voltage would result in a less efficient g_m conversion and thus higher power consumption.

Cutoff Frequency

Cutoff frequency (f_T) is also considered as the current gain bandwidth product as the current gain at f_T is equal to 1 [17]. This value will limit the actual gain bandwidth product of amplifiers designed by the device. The simulation result of f_T is shown in Fig. 27.55. Here, f_T is small as the overlap capacitance of the TFT under test is quite big. The overlap length here is 50 μm, which is even bigger than the channel length of the device. Practically, this value can be reduced to a few μm or even lower with self-aligned process.

Figure 27.55 suggests that this product rolls off pretty quickly in subthreshold region. The expression of f_T can be derived as follows:

$$f_T = \frac{g_m}{2\pi C_{ov}} = \frac{I_{DS} \cdot \ln 10}{SS \cdot 2\pi C_{ov}} \tag{27.57}$$

The expression shows that the value of f_T is proportional to I_{DS}; thus, the quick roll of at subthreshold is explained by the current roll off in subthreshold region. As I_{DS} and C_{ov} are both proportional to the channel width of the TFT, f_T would be independent of channel width. In addition, by reducing the overlap length, one could further reduce the overlap capacitance (C_{ov}) to increase the frequency response.

The expression also suggests that biasing the TFT in a deeper-subthreshold region would at the same time push the frequency response lower proportionally. Therefore, it's maybe desirable to have a less steep subthreshold slope in terms of speed when considering subthreshold operation.

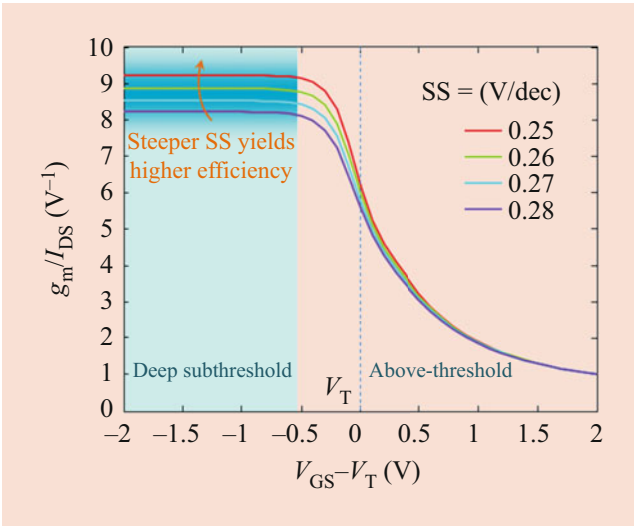

Fig. 27.54 g_m/I_{DS} from deep-subthreshold to above threshold region. The value reaches maximum at deep-subthreshold and increases with steeper SS

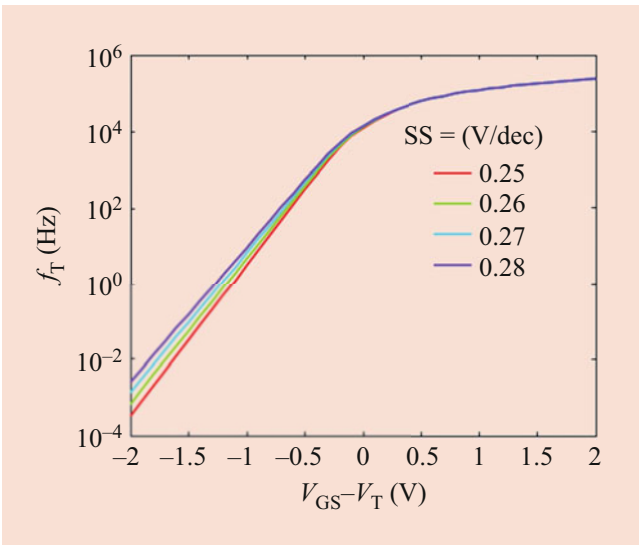

Fig. 27.55 Cutoff frequency vs. voltage bias for different SS

Sensitivity to Variations and Bias

Current Sensitivity to Variations

Here, we assume the threshold voltage shift is also a uniform shift in subthreshold. A non-uniform shift in subthreshold would mean a change in subthreshold slope, which will be discussed later. Therefore, the V_T shift at above-threshold is the same as a reference voltage shift at subthreshold, as the reference voltage shift is equivalent to a bias voltage shift. This curve can also be used for testing the sensitivity of bias voltage inaccuracy.

Figure 27.56 shows that at deep-subthreshold region, the normalized current sensitivity to V_T shift is a constant. The sensitivity becomes lower when the TFT is approaching and enters above-threshold region. As V_T shift is equivalent to bias shift, the sensitivity expression can be the same as the g_m/I_{DS} curve (as $g_m = dI_{DS}/dV_{GS}$ is also a sensitivity to bias) just with an opposite sign. For deep-subthreshold:

$$\frac{dI_{DS}}{dV_{GS}}/I_{DS} = -\frac{\ln 10}{SS} \tag{27.58}$$

For above-threshold:

$$\frac{dI_{DS}}{dV_{GS}}/I_{DS} = -\frac{2+\alpha}{V_{GS}-V_T} \tag{27.59}$$

Now we assume the change in SS would not affect V_T of the above-threshold region. Therefore, the subthreshold current of different SS would meet at around V_T. This yields the results shown in Fig. 27.57, where the normalized current sensitivity would drop when the TFT is biased closer to V_T. In above threshold region, the parameter SS do not contribute to the equation of I_{DS}. The sensitivity is therefore zero. The curve also shows that a steeper SS would increase the current sensitivity.

The expression for the current sensitivity in subthreshold is shown below:

$$\frac{dI_{DS}}{dSS}/I_{DS} = -\frac{(V_{GS}-V_T)\cdot \ln 10}{SS^2} \tag{27.60}$$

The above equation suggests that the sensitivity is reverse proportional to SS^2. Therefore, a steeper SS would yield a high current sensitivity on the variations of SS. In summary, although steeper SS would give rise to g_m/I_{DS} and potentially further reduce the power consumption, the sensitivity on process variations of SS and V_T would increase, possibly narrowing the design window for analogue circuits.

Accuracy Requirement for Biasing Circuitry

Here, we take a common source amplifier with depletion load as example (Fig. 27.58b). The load line and bias conditions are shown in Fig. 27.58a. As can be seen, bias conditions should keep both transistors working in saturated region, i.e. the V_{GS} for the green line in Fig. 27.58a. The blue lines show either of the two TFTs is working in a not saturated region.

Therefore, to maintain a high gain, V_{DS} for both TFTs should follow $V_{DS} > v_{sat}$. As the value of v_{sat} for different V_{GS} stays the same in subthreshold, the input voltage range can be calculated as:

$$V_{range} = \frac{2\cdot SS\,(V_{DD}-2v_{sat})}{V_A \ln 10} \tag{27.61}$$

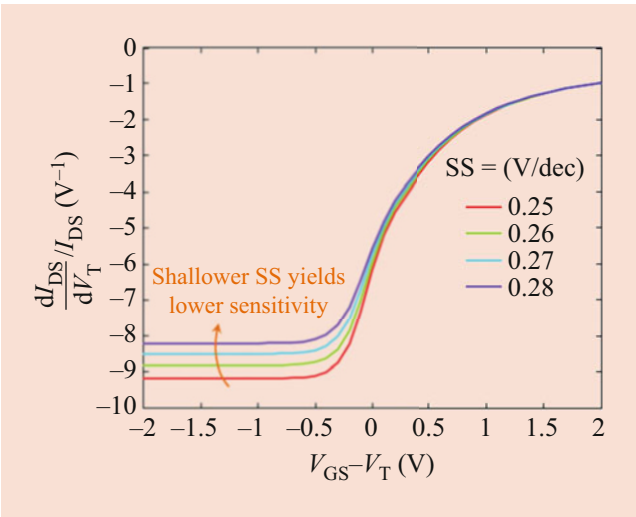

Fig. 27.56 Normalized sensitivity to VT shift for different SS

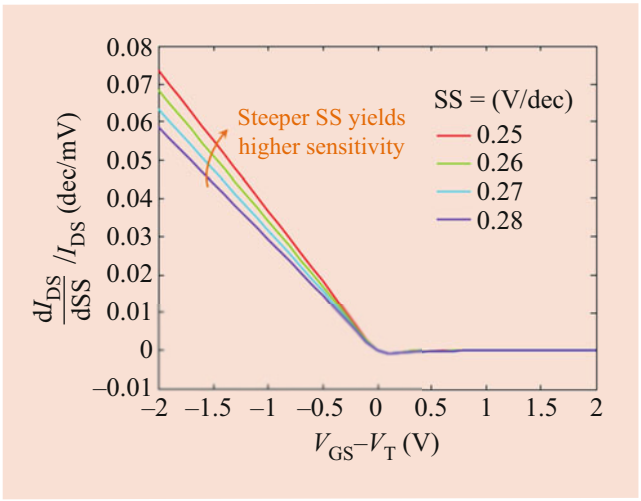

Fig. 27.57 Normalized sensitivity to SS variations for different SS mean values

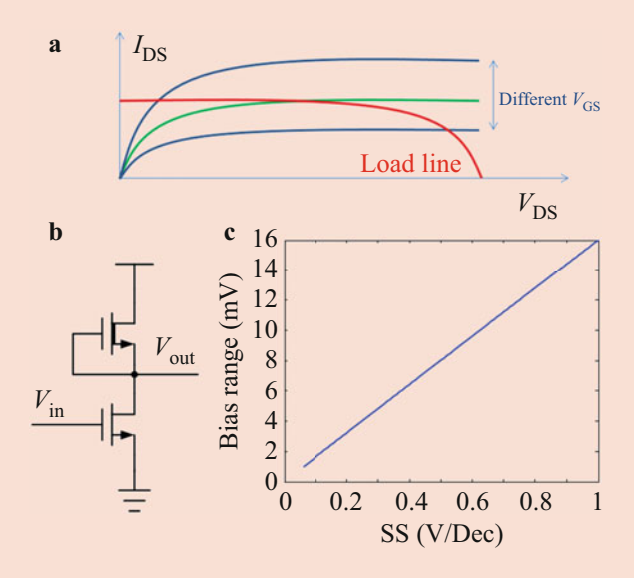

Fig. 27.58 The useful bias range for a depletion load common-source amplifier. (**a**) conceptual figure of the load line and transfer curve of the amplifier, where green curve illustrates the correct bias condition and blue curves illustrates that the amplifying TFT is biased out of useful bias range, (**b**) circuit schematic of the amplifier, (**c**) simulated useful bias range with respect to SS

27.3 Applications of Flexible Electronics in Biological Sensing

A complete biological sensing system includes samples under testing, a sensing interface, and signal processing units [207,208]. Samples (analytes) can potentially be anything biologically related, such as ions, molecules, proteins, viruses, cells, and even entire organisms. A sensing interface is a key element which offers the possibility of converting biological information into a recognizable signal. A processor is, therefore, used to amplify and process the corresponding signals. By integrating the sensing interface and signal processing unit, the analytical devices which are able to sense a certain analyte or analytes are called biological sensors or biosensors [209] and are considered the most powerful instrumentation in modern laboratories or hospitals. In this chapter, we will first introduce the current mainstream biosensing technologies, then discuss the important role of semiconductor technology in biosensing, and finally review some of the state-of-the-art flexible electronics biosensing systems.

27.3.1 Current Mainstream Biosensing Technologies

Biological sensors can be classified by the working principles, i.e. magnetic sensors, optical sensors, mechanical sensors, electrochemical sensors, etc. Figure 27.59 depicts the working mechanisms of mainstream biological sensing technologies which have been developed in recent decades.

Magnetic sensors use magnetic carriers in biological assays and molecular identification. The magnetic particles mainly perform as markers or labels to identify the analyte from the background [211].

Similar to magnetic sensors, most optical or photoabsorption-based biosensors require (fluorescent) labels to recognize the target. The optical signal (brightness) is directly related to the analyte concentration [212,213].

For biosensors which require labels, the label readout has to be converted to electrical signals and then passed to the processing unit. This has increased the system complexity and the sensor cost significantly. In order to bypass the converting step, label-free mechanical biosensors have been developed, which do not require any form of marks or label (i.e. microcantilever sensors and surface acoustic wave sensors) [210,214,215].

Electrochemical sensors could also perform label-free detection by directly converting the biosample's properties into electrical signals. A fast measurement can be carried out by a single device with a zero sample premeasured treatment. This unique advantage has made the electrochemical biosensors become one of the most successful commercial products family for in vitro diagnostics. One example is Clark's glucose sensors which was first reported in 1962 [216]. Quantitative blood glucose measurement can be performed with the glucose sensors and disposable Clark electrodes. The Clark electrode is also known as an oxygen electrode with a glucose-oxidase enzymatic membrane coating to convert the glucose concentration into electric current [217, 218]. The glucose sensor became commercially available in 1975 [219], and billions of diabetics have benefited from this technology until today.

27.3.2 Semiconductor Technologies for Biosensing

Both the sensing interface and the signal processor in a biological sensing system greatly rely on the development of semiconductor technologies. Figure 27.60 illustrates the contributions of semiconductor technologies for biological sensing, which covers materials level, single device level, and system level.

Most semiconductor materials deliver unique properties on the nanoscale. Nano-crystal quantum dots have been used to replace conventional markers to boost the biosensing performance (Fig. 27.60a). Nanowires and nanotubes are widely used for biological detection (Fig. 27.60b, d).

At device level (Fig. 27.60c), ion sensitive field-effect transistor (ISFET) is one of the major applications for biochemical sensing. A typical ISFET does not have a metal

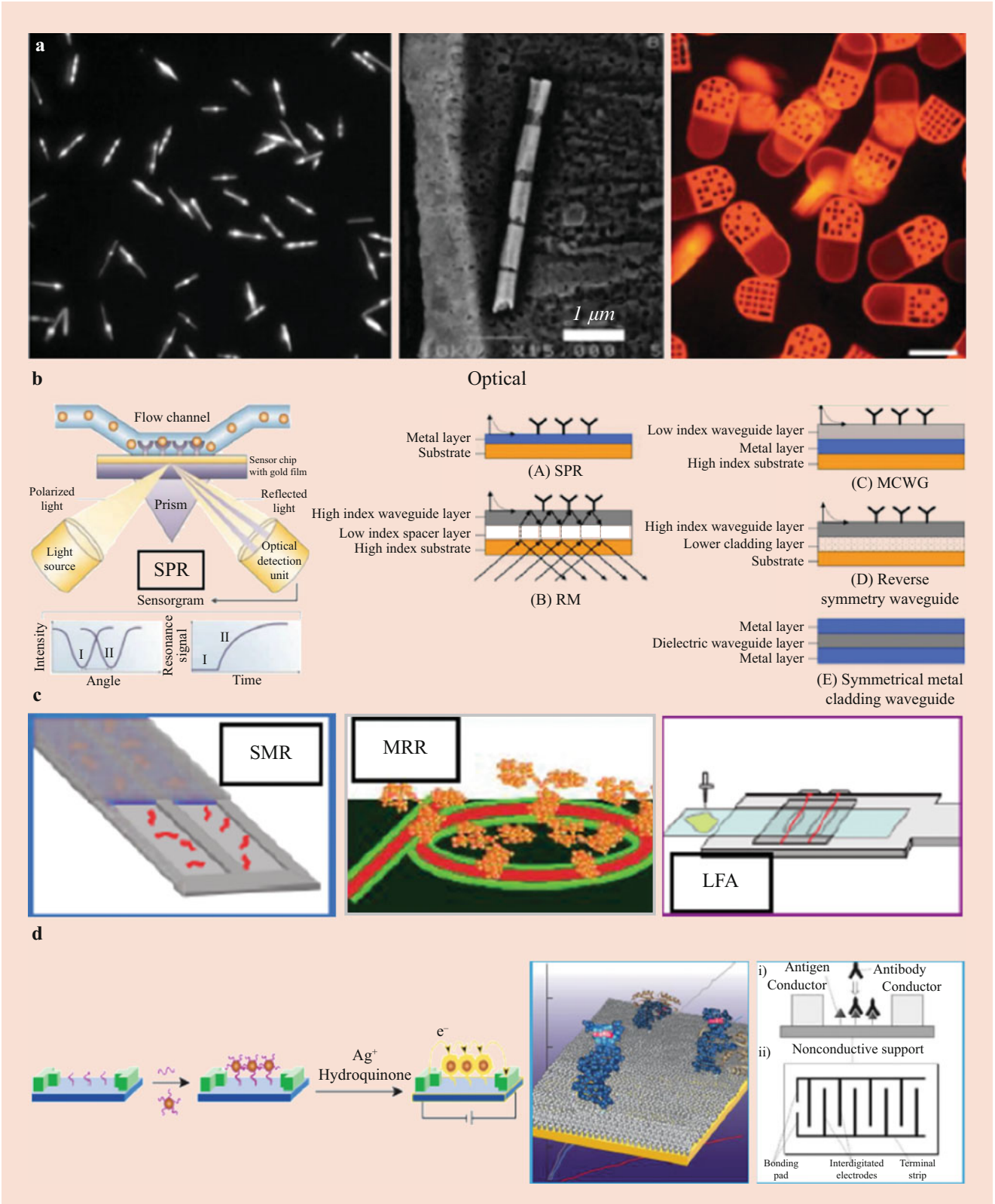

Fig. 27.59 Mainstream biological sensing technology. (**a**) Magnetic-based sensor; (**b**) optical-based sensor, including surface plasmon resonance (SPR), reflection mode (RM), micro-channel wave guide (MCWG), etc.; (**c**) mechanical sensor, including suspended micro-channel resonator (SMR), micro-ring resonator (MRR), lateral flow assay (LFA), etc.; (**d**) electrochemical-based sensor, including potentiometric sensor, voltammetric sensor, etc. (Adapted from [208, 210–213])

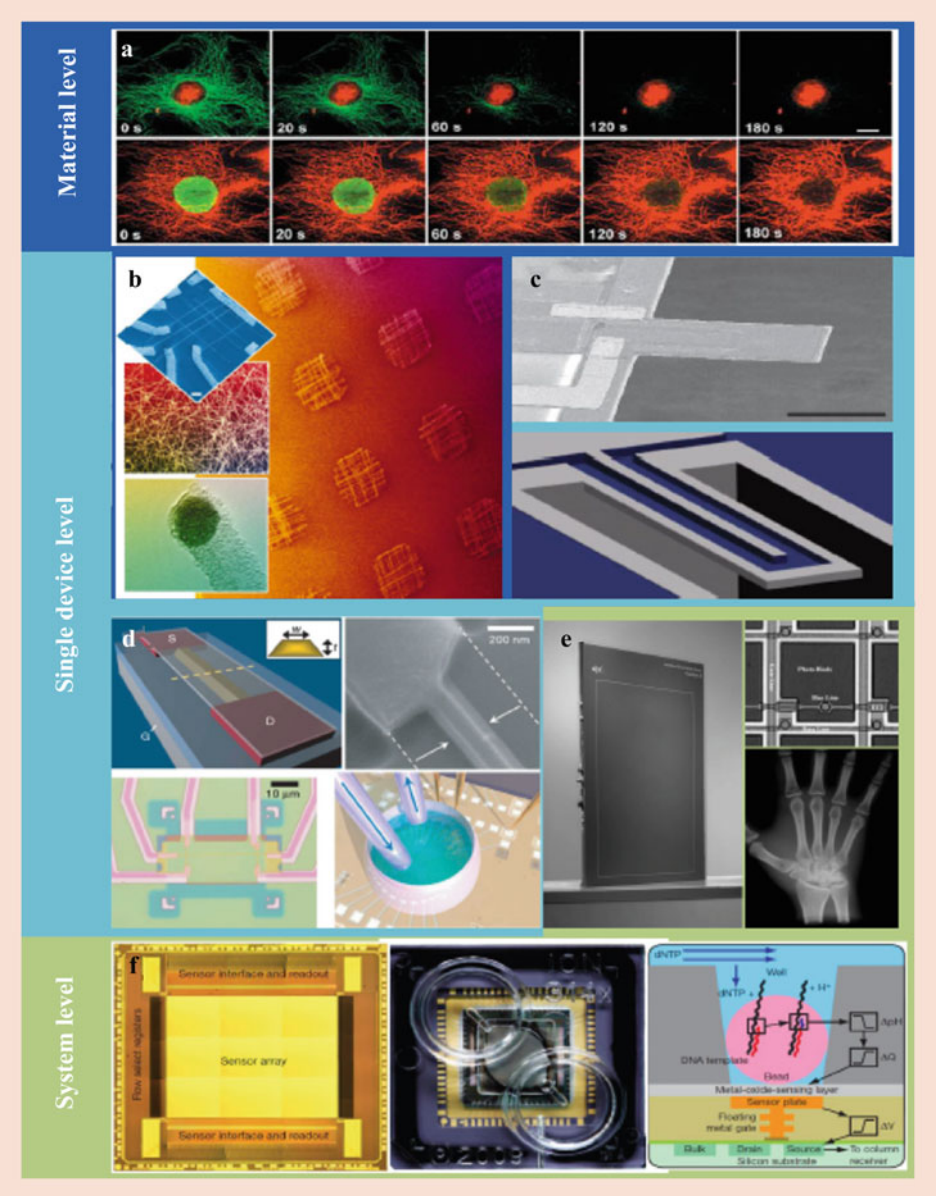

Fig. 27.60 The contribution of semiconductor technologies for biological sensing. Material level: (**a**) quantum confinement in semiconductors and new biological labels; and (**b**) nanowire arrays for biosensing; single device level, (**c**) MEMS cantilever and suspended micro-channel resonator; and (**d**) label-free immunodetection with CMOS-compatible semiconducting nanowires; system level, (**e**) an amorphous-silicon image sensor for X-ray diagnostics; and (**f**) an integrated chip for non-optical genome sequencing. (Adapted from [210, 220–224])

gate, and a special membrane directly coats on the top of dielectric layer. This artificial membrane is designed to capture certain ions, such as Na+ or K+. A fixed charge is provided to the channel after a certain amount of ions accumulate in the membrane. In addition, the performance of the field-effect transistor (FET) changes due to this fixed charge, and the result is used to estimate the ion concentration [225].

Apart from ion detection, conventional FET could be adopted to detect biological molecules, such as DNA, RNA, and proteins. Biological capture probes can be immobilized on metal gate or other electrodes that are connected to the gate, which involves a similar process to optical assays. The probe-analyte bonds will change the electrical properties of the gate or electrodes. This charge would then be amplified and output by the readout circuit. The biological detection and signal processing are fully integrated into one chip. The sample-to-result rate is increased significantly by this approach. Different electrochemical measurement methodologies have been reported for electronic biochips, such as an ISFET-based DNA sensor [226], capacitive-based dopamine sensor [227], and a DNA sensor [228], as well as a range of impedance-based sensors [229–232].

All the works presented above are achieved by complementary metal-oxide-semiconductor (CMOS) technology. At a system level (Fig. 27.60e, f), the advantages include high processing speed, low cost, high stability, and low power consumption. However, a series of common disadvantages for CMOS biosensors have been revealed as well. First of all, standard CMOS processing only support copper and aluminium as metal layers, which none of them is biocom-

patible. A bidirectional compatibility is a key consideration for a biosensing interface. The sensing interface (electrode) materials should be highly stable when immersed for a long time in a biological solution, and it should not release any toxic ions into the samples to generate any undesired interferences. Furthermore, the cost of standard CMOS technology is directly related to the area of silicon die, which makes it difficult to be scale up to be used for high-throughput applications.

27.3.3 Fully Integrated CMOS Biosensor

We presented an integrated biosensor that is capable of preforming impedance spectroscopy with biological samples [193]. By detecting the impedance, this novel system is capable of characterizing DNA samples based on their concentration and fragment length. All the label-free experiments were performed using suspended biomolecule solutions without any surface immobilization to probes or bio-functionalization. No further post-fabrication processes are required before taking biological measurements with the integrated CMOS chip. Therefore, the sensor chip system is entirely reusable, which enhances uniformity and reduces the cost of each measurement (Fig. 27.61).

Biological samples can be very precious or scarce, and thus, minimizing waste is a key consideration in biosensor design. This micro-array-based design integrates hundreds of micro electrodes and driving circuits into a 5 mm × 5 mm area. Each measurement requires only 20 μl of sample, as this volume is sufficient to cover the electrodes. Two of the major advantages of this method allow the reuse of the analyte. First, the integrated chip utilizes a noninvasive electrochemical method, dielectric spectroscopy, to analyse the samples. The typical AC stimulus of 500 mVpp is negligible compared with that of gel electrophoresis, which typically requires a supply voltage of more than 100 V DC. Second, the biochip detects the electrical properties of the biological molecules without the need for chemical reactions. The analysed biological samples are unchanged and can be reused for further analysis.

We investigated the impedances of ssDNA samples with different concentrations using the integrated biosensing system. Current applications of DNA concentration detection systems include the quantification of samples, such as libraries, prior to next-generation sequencing and quantitative PCR. Identical measurements were performed using BSA samples for comparison. Both sets of results show that the solution impedance is related to the biomolecule concentration. Concentrated solutions had lower impedance, indicating higher conductivity. This behaviour can be explained by the role of counter-ions that are attracted by the DNA backbone charges, which are in turn proportional to the concentration. More mobile counter-ions in the vicinity of the DNA result in higher solution conductivity [233]. On a log-log scale, the solution impedance showed a linear relationship with the sample concentration. This feature makes it possible to use the biochip to determine the concentrations of different samples. In general, the DNA data were clearer and more convincing than the data for the BSA samples. This difference in data quality is most likely due to the molecular structures of the samples. We used short fragments of single-stranded DNA with a length of several hundred base pairs [234]. Although ssDNA may have some secondary structure due to interactions between its own bases and interactions with other fragments, BSA, as a protein, is expected to have a considerably more complicated structure [235, 236].

Optical sensors, such as spectrophotometers, which measure the reflection or transmission properties of an analyte as a function of wavelength [237], currently dominate the DNA (and other biomolecules) detection sensor market. Most systems employ photometers to convert light signals into electrical signals for further analysis. The complex structure of the optical-electrical system results in reduced accuracy and higher costs. In this work, we report an alternative method for the quantitative analysis of biological samples. Our method significantly reduces the cost by utilizing an integrated sensor. We performed impedance spectroscopy, which measures a sample's ability to conduct electricity as a function of frequency. Furthermore, our system is purely electrical, which reduces the system's complexity and minimizes external interference.

In addition to the DNA concentration, other parameters can be measured using this impedance-based integrated biochip system. We performed a series of impedance measurements for digested ssDNA samples. DNase I was used in this experiment. This enzyme is suitable for eliminating DNA from RNA preparations prior to sensitive applications, such as RT-PCR. The DNase was able to completely digest the ssDNA into oligo- and mononucleotides in a 15-min reaction at room temperature. We divided the samples into eight groups, and the reaction time was precisely controlled. Our results showed that the reaction progress was related to the sample's impedance. The constant solution impedance after 15 min indicated that the digestion reaction had reached completion. During the DNA digestion, DNase I randomly cut the DNA strands into smaller pieces. Longer reaction times were expected to result in a shorter average DNA length. The shorter fragments act as charge carriers with higher mobility and thus provide higher solution conductivity. The solution impedance decreased as the digestion reaction progressed until the digestion reached completion at 15 min. This experiment demonstrated that the integrated biochip is capable of monitoring the progress of DNA digestion by measuring the impedance.

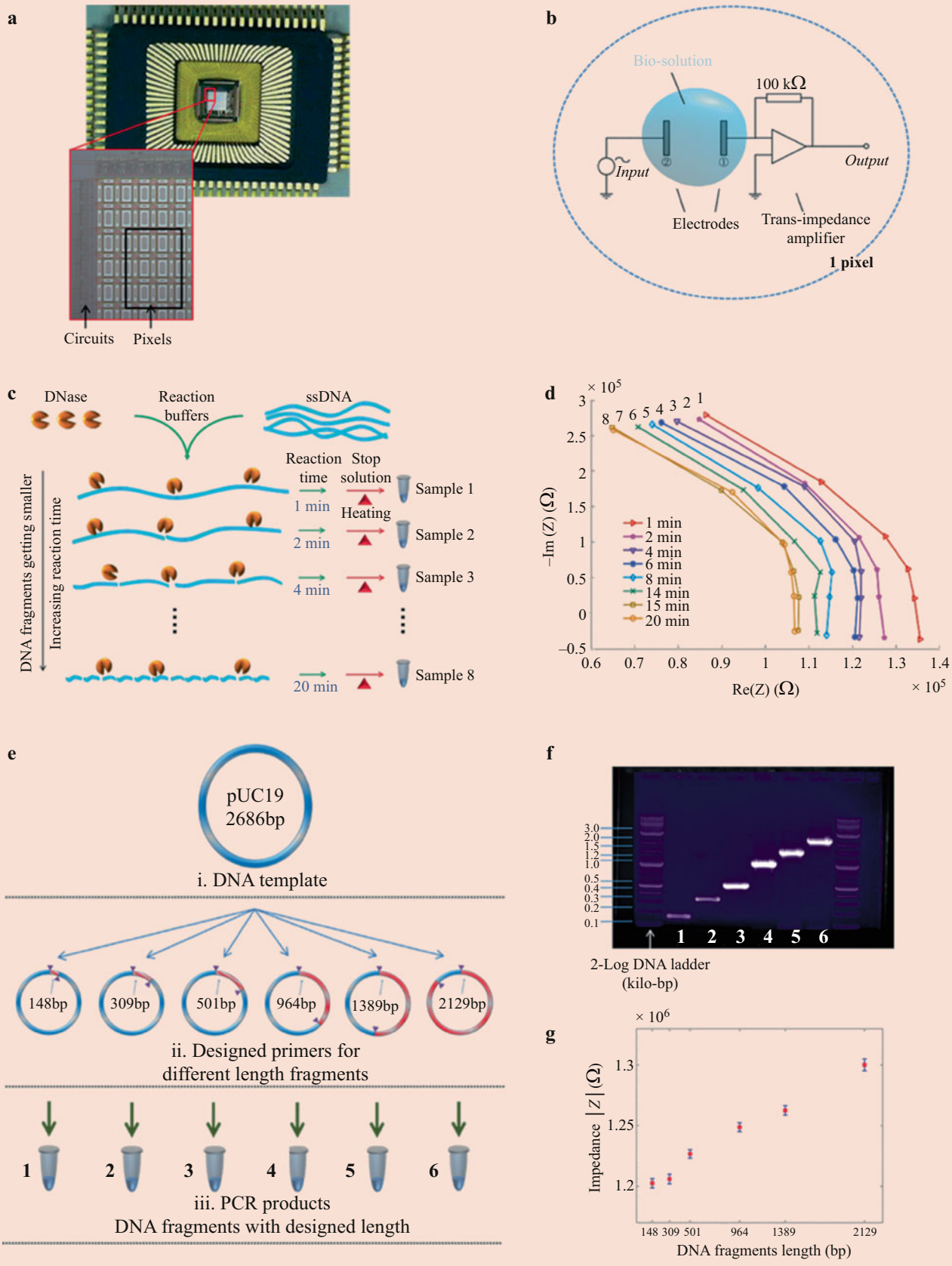

Fig. 27.61 (continued)

The DNA digestion experiment also suggested that the length of the DNA fragments is strongly correlated with the solution's conductivity. To validate this relationship, we designed an experiment that used PCR to generate various DNA fragments of known length. We amplified dsDNA, whereas the digestion test used ssDNA. Double-stranded DNA generally has less secondary structure than single-stranded DNA. In addition, the PCR products for each fragment size all had the same DNA sequence, whereas the herring ssDNA would contain a very heterogeneous mixture of DNA sequences. All of these factors minimize the interference in the impedance measurements. As expected, longer fragments were less conductive than shorter fragments. These results indicate that this system is capable of overcoming interference from other molecules in the solution, thus allowing the rapid yet precise quantitative analysis of unpurified PCR products.

The fragment length is one of the most important features of DNA for a wide range of genetic analyses [238,239]. The correlation between impedance and DNA fragment length observed in this study raises the possibility of using this purely electrical system to validate and characterize PCR products. Gel electrophoresis has dominated this area for more than 40 years. The conventional technique involves imaging the DNA using UV light after the intercalation of ethidium bromide, a highly carcinogenic compound that can also potentially damage the DNA's structure and induce mutations [240]. Our impedance system is capable of replacing this time-consuming and potentially dangerous technique. The rapid characterization of restriction fragment profiles could potentially be applied to genome assembly, in a manner similar to that of optical mapping [241]. We present a method for the label-free analysis of suspended samples, and we demonstrated that this method can detect differences in the impedance of different PCR products within a few minutes. The samples can even be reused without any further treatment.

27.3.4 Heterogeneously Integrated Biosensor with Disposable Electrodes

In this section, we developed a heterogeneous impedance measurement system with a reusable CMOS chip for signal processing and an active thin-film electrode disposable system as an electronics-biological interface (as shown in Fig. 27.62a) [242]. The disposable chip enables large-area fabrication technologies, which provide great freedom for the selection of electrode materials and electrode configurations. In addition, the design of the electrodes is separated from the CMOS chip, which can be customized for different applications. With the use of disposable electrodes, it can be used as a powerful platform for multifunctional impedance-based measurements.

The system consists of two parts, including a disposable glass chip and a reusable part. Eight Cr/Au (20 nm/80 nm) double-layer metal electrodes were fabricated by a thermal evaporator with a shadow mask on a glass substrate. Both the width of each electrode and the separation between the electrodes are 500 μm. After the metal deposition, the electrodes were then attached to connection pins by silver paste. A 5-mm-diameter metal cap was used to cover the centre part of the electrodes. The rest of the glass chip was covered by liquid PDMS to passivate and hold the connection pins. After the PDMS solidified, the cap was removed to leave a 5-mm-diameter well on top of the electrodes. This well was used to contain the sample solution during the measurement. The fabrication of the electrode chip is low-cost and highly reproducible. The glass chip is the interface between sensor and the sample, which can be disposed after each measurement.

The impedance measurement chip was designed in a Cadence analogue IC design suite, and the prototype was fabricated using AMS 0.18 um CMOS process. The design was an extended work to our previous impedance-based CMOS chip, but here sensing electrodes are extracted from the silicon chip on to a disposable glass substrate.

The DNA sample concentration tests were performed with five groups of herring sperm DNA samples at different concentrations. The measurements were carried out at frequencies from 100 Hz to 1 MHz. Figure 27.62b, c shows the results in both Cole-Cole and Bode plots. The former yields the general impedance behaviour of the samples. At low DNA concentrations (37.5 μg/ml, 75 μg/ml, and 150 μg/ml), each dataset forms a semicircle with a tail, which is a classic pattern for biosolutions [243]. The semicircle is formed by the double-layer capacitance between the electrode-electrolyte interfaces. The DNA solutions were prepared using DI water, and hence, the main charge carriers within the solution are the DNA with each base pair containing two negative charges. Higher concentration DNA meant more base pairs per volume and, hence, more charges per unit volume. Therefore, the concentrated DNA solutions were much conductive, and

Fig. 27.61 Key results of the integrated CMOS impedance sensor. (**a**) Photographs of the integrated chip, the sensing area and excitation circuits, (**b**) schematic diagram of s sensing pixel, (**c**) ssDNA fragments with different average lengths were prepared by controlling the DNase I reaction time, (**d**) Cole-Cole plot depicting the impedance of samples with different reaction times, (**e**) six different PCR products with different lengths were prepared, (**f**) the sizes of the PCR products were validated by standard gel electrophoresis, (**g**) the measured impedance values versus DNA length in base pairs at 10 kHz (Adapted from [193])

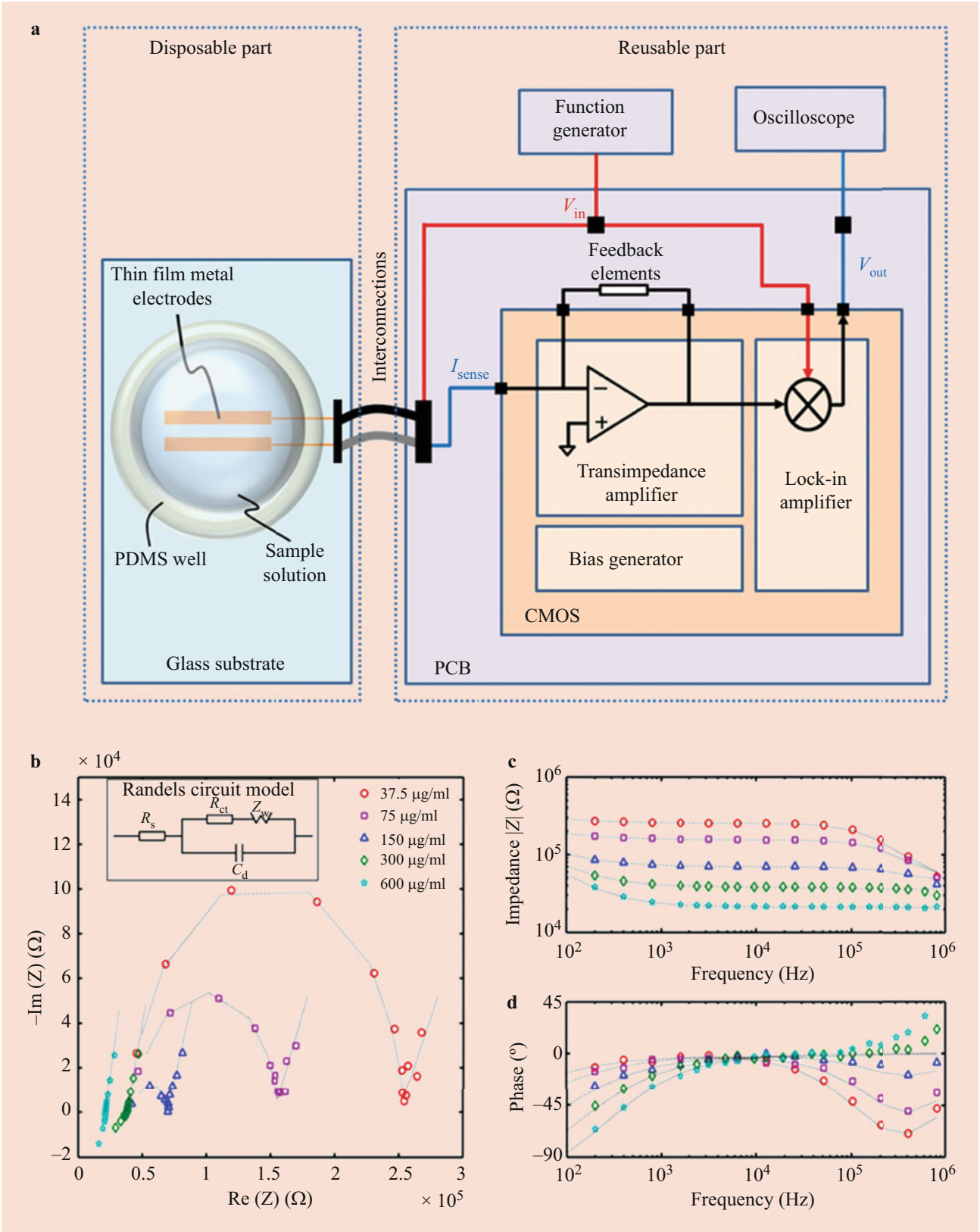

Fig. 27.62 Key results of the heterogeneously integrated biosensor. (**a**) Schematic of heterogeneously integrated impedance measurement system. The disposable part is thin-film metal electrodes on the glass substrate and reusable partincludes a function generator for stimulus, a CMOS chip for signal amplification and processing and an oscilloscope, (**b**) Cole-Cole plot of the measured and fitted results of different DNA concentrations. Inset shows a Randels circuit model used for data fitting. (**c** and **d**) Bode plot ofthe measured and fitted values from (**b**). (Adapted from [242])

as the solution concentrates, the radius of the semicircle starts to shrink. This indicates that highly conductive solutions are more resistive than capacitive. As shown in the Cole-Cole plot, a purely resistive sample manifests as a straight line parallel to the imaginary axis, which implies that the complex impedance only contains the real part. This is particularly true for the most concentrated sample (600 μg/ml), which comes up a straight line and is almost parallel to the imaginary axis.

The Bode plot shows the magnitude and the phase of the impedance for different samples. The impedance values are well spread over the frequency range from 100 Hz to 1 MHz, which indicates the clear differences in electrical properties of the samples. Each set of impedance data was fitted to a same equivalent circuit, and the results are shown in grey lines. The Randles circuit model was selected in this work, which is the classic model for depicting the electrode-electrolyte interface and the bulk solution.

From the Bode plot shown in Fig. 27.62, the magnitude of impedance for each DNA sample is relatively constant at mid-band frequencies (1 kHz–100 kHz). Higher sample concentration results lower sample impedance. This work shows almost doubled sensitivity over the previous work, where the slope of this work is 0.85 and the previous one is 0.44. The specific thin-film electrodes design in this work contributes to this sensitivity enhancement. In a DC electrolyte sensing system, cell constant κ (cm^{-1}) is defined as:

$$\kappa = \frac{R}{\rho} \tag{27.62}$$

where R represents the measured resistance and ρ is the specific resistivity. This factor also can be used to determine the performance of an impedance-based sensing system. For most biomeasurement, the solution concentration (c) is a function of the solution conductivity (reciprocal of the solution resistivity). From Eq. (27.1), we can conclude that the sensing output voltage (V_{out}) is inversely proportional to the measured impedance. We can then rewrite Eq. (27.62) as:

$$\frac{V_{out}}{c} \propto \frac{1}{\kappa} \tag{27.63}$$

where c represents the solution concentration. Equation 27.63 indicates that smaller cell constant will result better detection sensitivity; therefore, to design a small cell constant system is a key route to enhance the sensor's performance. Olthuis's work [243] suggests that the cell constant can be reduced effectively by increasing the electrodes modulus k. In a two-electrode system, k is defined as:

$$k = \frac{W}{W+S} \tag{27.64}$$

where W is the electrode width and S is the separation between the electrode pair. Thus, a better W over S ratio can give better detection sensitivity. The W over S ratio is 1:2 in previous work, and the ratio is 1:1 in this work. In the previous work, on-chip electrodes are used, and the electrode dimensions are limited by both chip area and CMOS design rules. However, by using thin-film-based electrodes, the electrode design is more flexible, and hence the sensing performance can be further enhanced. It is worth to mention that bare gold electrodes are used in this work for characterization of suspended DNA samples. This is different from the reported affinity-based sensors in which electrodes are functionalized with probes to capture target analytes. Immobilized probes are typically used to examine the presence of known analytes. However, both limit of detection and accuracy are restricted by unspecific binding and binding failure. In our work, the electrical properties of the bulk solution are measured from 100 Hz to 1 MHz. This method can be used as an effective DNA concentration sensor. It also provides the capabilities to distinguish the length of DNA fragments and can be applied to validate PCR products. Indeed, sensors without immobilization lack selectivity compared to the conventional affinity-based approaches. However, this can be solved by introducing micro-fluidic sample sorting and/or sieving technique on top of electrodes. Moreover, this heterogeneously measuring system is fully compatible with biofunctionalization on the electrodes, which can be used for different specific applications.

27.3.5 Impedance-Based Immunosensor [244]

Immunoassay is a standard technique for a wide range of applications, which is frequently applied to detect cancer biomarkers, virus, and other antigens [242, 245, 246] due to the specificity of antigen-antibody interaction. The conventional immunoassay methods include the enzyme-linked immunosorbent assay (ELISA) [247, 248], immunofluorescence techniques [249], radioimmunoassay (RIA) [250,251], mass spectrometric immunoassay [252,253], chemiluminescence assay [254, 255], immunologic colloidal gold signature (ICS) [256, 257], electrophoretic immunoassay [258], immune-polymerase chain reaction assay [259], etc. In clinical laboratories, the ELISA immunoassay method has been widely used, but the process of ELISA test is complicated, and the microplate readers are expensive and bulky, which no longer meets the current needs of immunoassays. The next-generation immunoassay techniques should have simplified operation, high specificity, and high sensitivity and should be label-free and low cost [260–262].

Compared to the complicated process of ELISA test, electrochemical sensors provide a simpler method for immunoassay [263, 264]. The electrochemical immunosensor provide the possibilities for label-free detection, detecting electrical signals instead of optical signals. They have been widely applied in biological detections at different scales, including but not limited to organs, tissues, cells, and biomolecules

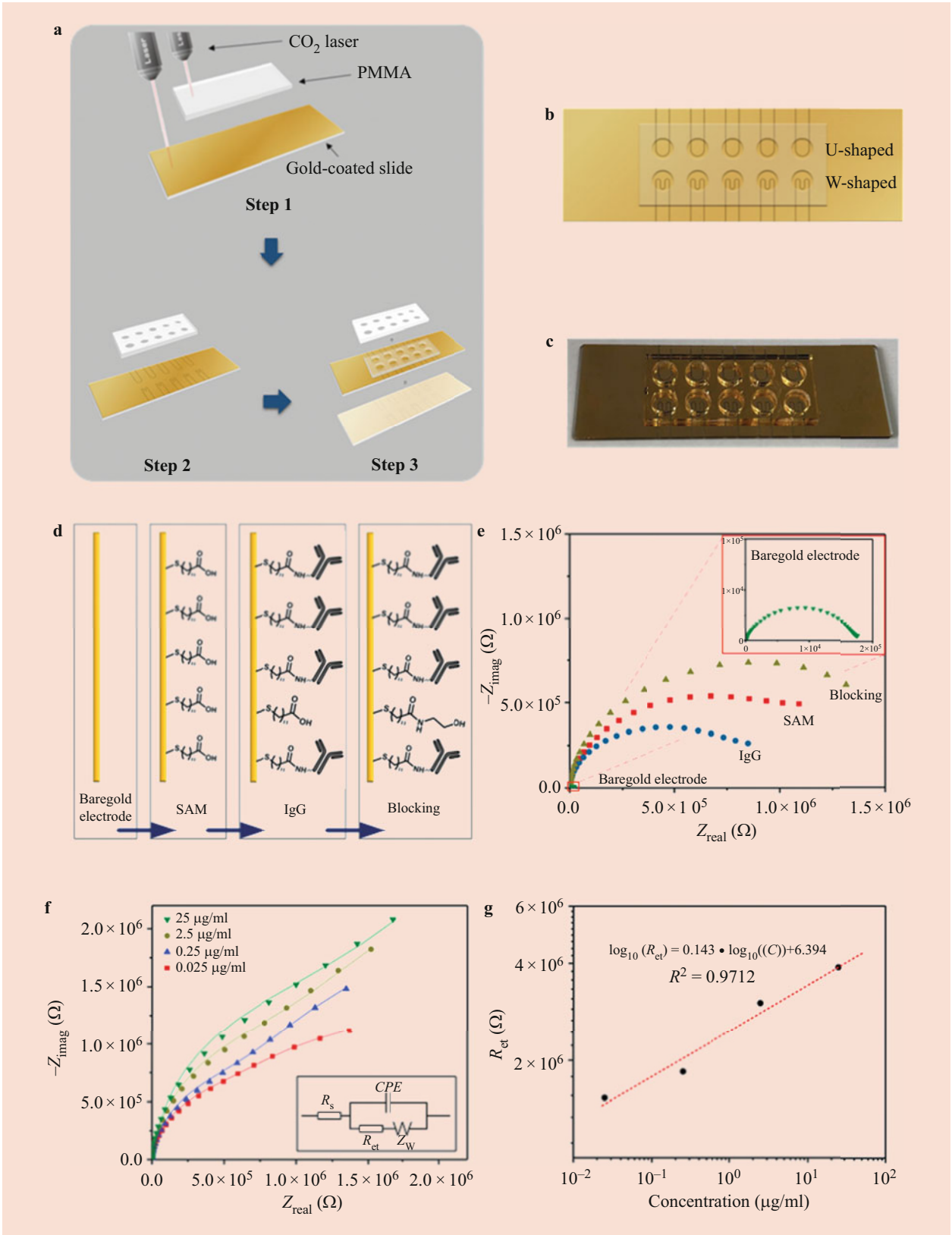

Fig. 27.63 Impedance-based disposable immunosensor. System diagrams of the disposable immunosensor. (**a**) fabrication steps for PMMA sample wells and gold electrodes with direct-writing laser: Step 1. Laser writing; Step 2, alignment; Step 3 assembling, (**b**) Top view of the sensor array model. (**c**) Real picture of the fabricated sensor. Immunosensing experiment in single sample well. (**d**) electrode functionalization procedures, (**e**) Cole-cole plot of the impedance measurements between each electrode modification steps, (**f**) Cole-cole plot of the different concentrated IgG samples, (**g**) The plot of Ret versus IgG concentration

[193]. A standard electrochemical cell [208] consists of conductive electrodes and sample under test (SUT). In the biological world, the majority of SUT is solution based, and the properties of the electrode-electrolyte interface are as important as those of the bulk sample itself in such electrochemical detection systems [243]. Impedance-based measurement, also known as electrical impedance spectroscopy, is emerging as a powerful tool for biomolecule detection. The electrical properties of the SUT can be depicted by equivalent circuits consisting of basic electrical components. The values of the components are directly linked to certain properties of the SUT. By extracting the parameters of the equivalent circuit, both the electro-electrolyte interface and the bulk solution can be characterized in one measurement. In addition, with suitable electrode functionalization techniques, the functionalized impedance electrodes can perform label-free detection for DNA [193, 224] or proteins [265] with high selectivity and sensitivity.

Figure 27.63 shows the system diagram of a disposable immunosensor platform. The system consists of a gold-coated glass slide and a plastic sheet with sample wells. After standard substrate cleaning procedures, a layer of 50 nm gold was deposited with thermal evaporation technique. Two designs were characterized in this work, U-shaped electrodes and W-shaped electrodes. The effective channel lengths of the two designs were 8.71 mm (U-shaped) and 9.36 mm (W-shaped).

Poly(methyl methacrylate) (PMMA, also known as acrylic) was chosen to create the sample wells. Acrylic is nontoxic, corrosion-resistant, and low-cost. Acrylic sheets (2 mm thick) were purchased from Mitsubishi, Japan. A 2-by-5 array was fabricated with a pitch of 9 mm, and the diameter of the sample well is 6 mm. The geometry of the wells matches the mainstream 96-well assay plate, making it compatible with all standard biochemistry liquid sample handling tools.

Laser processing is a standard material processing technique (for both metals and non-metals) by utilizing a high-power-density laser beam. Among different types of lasers, the CO_2 laser is the most commonly used, which can be used for cutting, welding, surface treatment, drilling, and micromachine [266].

Figure 27.63 shows the impedance-based immunosensing experiment which was carried out in a single sample well with U-shaped electrodes. The impedance of 5 mM $K_3Fe(CN)_6/K_4Fe(CN)_6$ redox solution was measured between each electrode bio-functionalization step. Figure 27.63 depicts the steps for IgG electrode functionalization, including 11-MUA modification (a type of self-assembled monolayer, SAM), IgG bonding, and blocking process. From the Cole-Cole plot in Fig. 27.63, the impedance characteristics have clearly shown that the electrode surface has been successfully modified. The bare gold electrode measurement is inserted as a subplot in Fig. 27.63 due to the different scales. After the electrode functionalization, different concentrated anti-IgG samples were added into the well to trigger the reactions. 0.025 μg/ml, 0.25 μg/ml, 2.5 μg/ml, and 25 μg/ml anti-IgG samples (in PBS) were added in sequence and held for one hour each. Impedance measurements were carried out with $K_3Fe(CN)_6/K_4Fe(CN)_6$ between each reaction. The Cole-Cole plots for four reactions are shown in Fig. 27.63, where the overall impedance raises up as the anti-IgG concentration increases. The dot data points are taken from the measurements, and the solid lines are the equivalent circuit model-fitted results. The equivalent circuit used here is shown in the subplot of Fig. 27.63. The Ret indicates the Faradic current strength, which is directly related to the numbers of antibody-antigen bonding. The value of Ret is also the indicator of the detected concentration of anti-IgG in this experiment. Figure 27.63 plots the model-fitted Ret versus the anti-IgG concentration, and a good linearity is observed. The linear relationship between the measured impedance and analyte concentration can be obtained from Fig. 27.63.

27.3.6 TFT-Based Biosensors

The most important functions for human-machine interfaces include pressure mapping, heartbeat monitoring, temperature capturing, electrophysiology recording, and ion detection. The following are TFT-based biosensors for these applications [1].

Pressure mapping can be implemented by using a pressure-sensitive film integrated with TFT arrays. Someya and his coworkers demonstrated an ultra-lightweight imperceptible pressure sensor array using ultra-thin flexible organic TFTs together with a resistive tactile sensing foil, as seen in Fig. 27.64a [59]. In this type of configuration, the pressure sensor array produced a current change when touched by an object, with a magnitude of ∼150 μA, which was a relatively small signal due to the low mobilities of organic TFTs. In contrast, also based on a resistive strain sensor, Wang et al. demonstrated a heartbeat monitor with an intrinsically stretchable organic TFT amplifier while using a potential divider configuration to generate voltage signals to achieve a large amplitude of >0.2 V (Fig. 27.64b) [60]. Similar to the pressure sensor array, Ren et al. demonstrated a low-operating-power and flexible active-matrix organic TFT temperature sensor array, by using a thermistor in series with a TFT (Fig. 27.64c) [267]. The temperature sensor array exhibited good mapping to a wide range of temperatures, i.e. from 20 to 100 °C, but the current change was less than 1 μA. For this small current signal, a low-noise trans-impedance amplifier (TIA) close to the sensor is needed for real application; otherwise, the small current

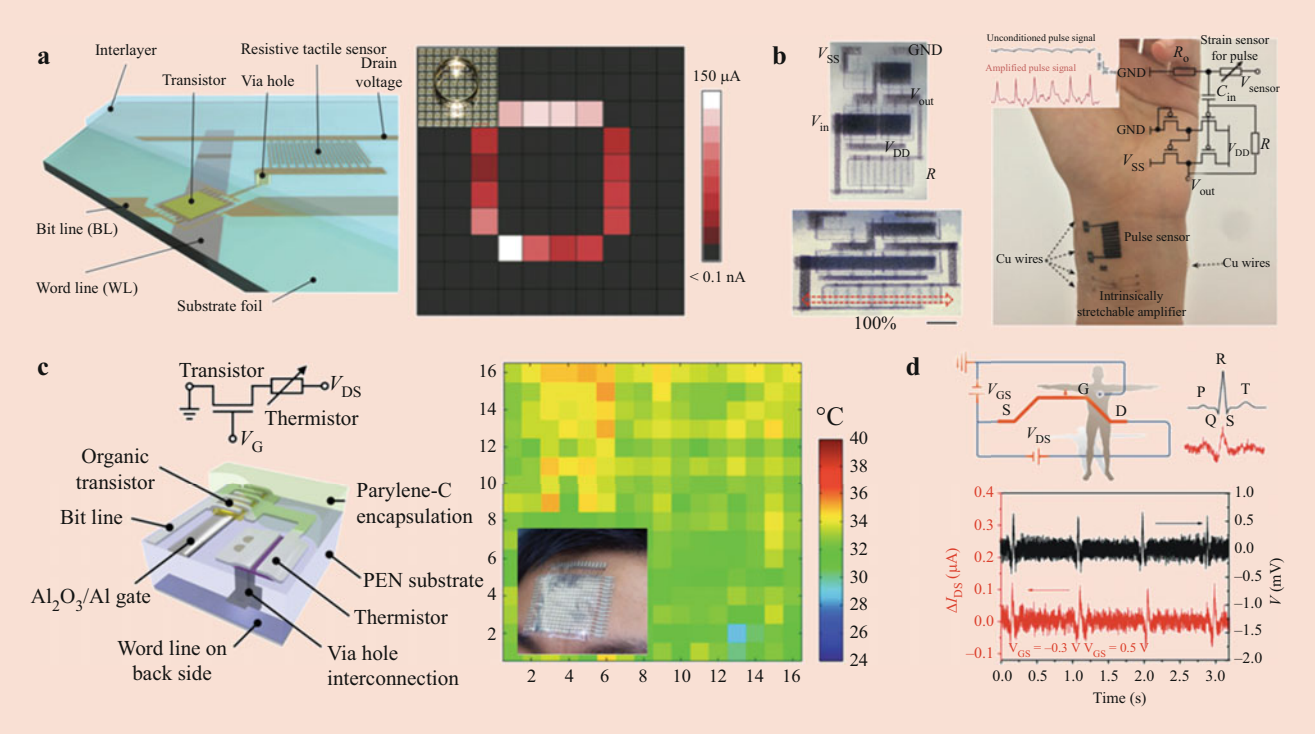

Fig. 27.64 Examples of flexible TFT-based biosensors. (**a**) An ultra-lightweight imperceptible pressure sensor array using ultra-thin flexible organic TFTs for pressure mapping. (Adapted from [59]). (**b**) An intrinsically stretchable organic TFT amplifier integrated with a resistive sensor for heartbeat monitoring. (Adapted from [60]). (**c**) A low-operating-power and flexible active-matrix organic TFT temperature sensor array with a thermistor for temperature capturing. (Adapted from [267]). (**d**) Electrocardiogram (ECG) recording using an organic electrochemical transistor. (Adapted from [268])

Table 27.7 Signal types and circuit requirements for different sensors

Sensor type	Signal type	Signal range	Frequency (Hz)	Interface circuits
Pressure	Current/ resistance	<1 mA	<10	TIA/VA
Temperature	Current	<1 μA	<1	TIA
Electrophysiology	Voltage	<1 mV	<100	VA
Ion	Voltage/ capacitance	<60 mV/dec	<1	ISFET+TIA

N.B.: *TIA* transconductance amplifier, *VA* voltage amplifier

may easily spread out and/or be affected by the noise when transmitting through a long wire (Table 27.7).

In terms of electrophysiology recording, the signals can be directly captured by thin-film amplifiers, in contrast to that of pressure mapping and temperature capturing, which require tactile sensors. Electrophysiological signals are essentially voltage signals of which the amplitudes are less than 1 mV, and therefore high-gain amplifiers are required for capturing these signals with a high sensitivity. Campana et al. used an organic electrochemical transistor that provided larger transconductance for electrocardiogram (ECG) recording (Fig. 27.64d) [268]. However, the recorded current signals were very noisy. Rather than using transconductance amplifier, Sekitani et al. demonstrated ECG recording on a rat's heart using a high-gain voltage amplifier, providing clear output signals [269]. Besides ECG to record signals from the hearts, one can also capture electrophysiological signals from the brain (electroencephalography, EEG), eyes (electrooculography, EOG), muscles (electromyography, EMG), etc., which are also very useful for e-skin or other human/humanoid applications.

Ion detection on e-skin is useful to analyse sweat compositions and their concentrations. There is a specific family of electronic devices for ion detection known as ion-sensitive field-effect transistors (ISFETs). Different from the aforementioned biosensors, ISFETs require a gate or a gate dielectric that is ion sensitive. A common example is pH sensors, which are proton sensitive. In combination with a functionalized material on the gate or gate dielectric, ISFETs can be selective towards other ions, such as sodium and potassium. The mechanism of an ISFET is that an interface potential is established by the solid/electrolyte interface ions and is modulated by the different concentrations of ions, with a theoretical maximum sensitivity of 60 mV per pH change or per decade of ion concentration change. Due to the nature of the transistor as a current device, a TIA is also required for ion detection.

For these examples of biosensors, the frequency requirement is not demanding. It is obvious that activity based on human touch, body temperature change, and ion-level change in sweat are slow, i.e. less than 10 Hz. In addition, electrophysiology signals are also in low frequencies of <100 Hz [270]. Therefore, for sensor interfaces, a relatively small bandwidth of 100 Hz is enough for most interfacing analogue front-end circuits.

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Biodegradable Electronics

28

Giovanni Antonio Salvatore, Lan Yin, and Fanqi Dai

Contents

28.1 Materials 1019
28.1.1 Terminology 1020
28.1.2 Polymeric Substrates and Encapsulations 1020
28.1.3 Metallic Conductors 1022
28.1.4 Semiconductors 1024
28.1.5 Dielectrics 1026

28.2 Devices, Circuits, and Systems 1026
28.2.1 Transistors and Circuits 1027
28.2.2 Sensors 1029
28.2.3 Optical Devices: LEDs 1032
28.2.4 Powering Devices: Batteries, Photovoltaics,and Energy Harvesters 1032

28.3 Dissolution Mechanisms 1034

28.4 Fabrication Examples 1035

28.5 Application, Grand Challenges, and Outlook 1035

References 1038

Abstract

A general goal in the development of any electronic component is to achieve high-performance operation and mechanical robustness which undergo negligible change over time. Recent advancements in materials science, thin film processing, and nanotechnology have, however, prospected the possibility of devices which can bend and stretch and provide the desired performance for a prescribed timeframe and, then, dissolve, resorb, or physically disintegrate upon the end of their functional time. Degradable or "transient" forms of electronics that disappear via hydrolysis or biochemical reactions, disintegration, and depolymerization could instill intelligence into resorbable implants, "green" environmental sensors, and biodegradable food packaging and lead to new compostable consumer electronic devices or printed boards so as to alleviate the problem of the electronic waste. Research has been driven by questions such as the following: Can we realize soft electronic implants which deliver diagnostics or therapeutic functions and then safely resorb in the body avoiding any additional surgery intervention? Can we realize compliant environmental sensors which harmlessly decompose to eliminate the need for their retrieval?

This chapter starts from reviewing the materials that have demonstrated degradable behavior in various aqueous solutions. The emphasis is on those that are key ingredients to realize active electronic devices and circuits: semiconductors, dielectrics, and conductors. Another important class of materials is the polymers which have been used mostly for encapsulation and substrates. The attention then moves to devices especially on sensors, field effect transistors, LEDs, batteries, and solar cells. The chapter also provides an insight into the dissolution mechanisms and offers some examples of the fabrication methods adopted so far to build the devices. Finally, it ends by listing some of the challenges faced by this technology.

Keywords

Thin film electronics · Biodergadable materials · Sustainable electronics · Dissolvable materials · Transient electronics

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28.1 Materials

The spectrum of degradable materials spans from polymeric substrates and encapsulations, through metallic conductors and semiconductors to dielectrics offering a complete set of

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ingredients to build electronic and optoelectronic devices. While polymers have been well studied for a long time, much less has been done on semiconductors and dielectrics. Nowadays, thanks to the progress in synthetic chemistry and materials engineering, chemical properties can be tailored to specific applications. Materials which undergo degradation by dissolution, resorption, disintegration, depolymerization, or biological processes are used for food packaging [1, 2], drug delivery [3–6], tissue engineering [3, 7–9], microfluidics [10], medical tools, and implantable devices [11–13].

28.1.1 Terminology

It is worth mentioning that terms such as "degradable," "biodegradable," and "compostable" can assume different meanings. Such ambiguity reflects the ongoing developments of insights into how biomaterials interact with living organisms. For example, a material is considered "biocompatible" if it does not produce an adverse effect when in contact with a living organism. However, since the immune response and repair function of living organisms are so complicated, it is not adequate to describe the biocompatibility of a single material in relation to a single cell type or tissue. So, ultimately, only an extensive number of tests, including analytical characterization of the material and in vivo testing, can fulfill all the requirements of the ISO definition of biocompatibility (ISO 10993). Few other definitions which are relevant are listed below.

Biodegradable: Materials break down under the action of naturally occurring microorganisms (e.g., bacteria, fungi, or algae) into low-weight and nontoxic products, but with no specific timeframe.

Compostable: Materials undergo degradation by biological processes during composting to yield carbon dioxide, water, inorganic compounds, and biomass, at a rate consistent with other known compostable materials (e.g., cellulose), and leave no visible, distinguishable, or toxic residue.

Dissolvable/Bioresorbable: Materials dissolve via hydrolysis or are absorbed in the body or in the environment.

In the chapter the terms "degradable" and "transient" are used to indicate nonspecific (bio)degradation processes but rather general decomposition with a consequent loss of functionalities (electrical and mechanical) and physical disappearance or disintegration.

28.1.2 Polymeric Substrates and Encapsulations

Polymers are the class of materials which have been studied in more details and which have been employed in a large variety of applications. The worldwide consumption of biodegradable polymers (BPs) was of about 1 million tons in 2016, and it is expected to grow up to 2.5 million tons in 2021 [14]. Target markets for BPs include packaging materials (trash bags, wrappings, loose-fill foam, food containers, film wrapping, laminated paper), disposable nonwovens (engineered fabrics) and hygiene products (diaper back sheets, cotton swabs), consumer goods (fast-food tableware, containers, egg cartons, razor handles, toys), and agricultural tools (mulch films, planters) [15]. Here, the focus is on the polymers which are more commonly used and which can be deposited in thin film to serve as substrate and encapsulation of electronic devices.

Biodegradable Natural Plastics. Starch, cellulose, and silk-based films have been used as coatings and substrates in recent studies on transient electronics. Starch is an inexpensive, annually renewable material derived from corn and other crops. Starch-based BPs can be produced by blending or mixing them with synthetic polymers. By varying the synthetic blend component and its miscibility with starch, the morphology and hence the properties can be regulated easily and efficiently. Thermoplastic starch can also be mixed with cellulose to produce rigid and mechanically stable film. Innovia Films [16], for example, provides a family of cellulose-based films (NatureFlex) which are highly transparent, highly permeable to moisture, and compostable-certified in both industrial and home composting environments. "Green" electronics using disintegrable organic semiconductors fabricated on cellulose substrates are shown in Fig. 28.1a–c. BASF produces EcoFlex® [17] which is blended from corn starch, potato, and polylactic acid. It is one of the few biodegradable plastics, which complies with the European (U Directive 2002/72/EC) and American food legislation for food contact (FCN 907). Bauer's group used EcoFlex® as substrate for the fabrication of organic transistor, while Salvatore et al. used it as substrate and encapsulation of fully biodegradable and highly flexible temperature sensors [18]. Silk is another appealing biopolymer as a temporary, soluble supporting substrate. It is optically transparent, mechanically robust, and flexible in thin-film form. Silk is biocompatible, bioresorbable, and water soluble with programmable rates of dissolution. Moreover, recent work demonstrates the ability of silk films to serve as a platform for transistors and various classes of photonic devices [13, 19]. Thin film silicon-based CMOS circuits fabricated from a foundry process transferred on silk substrates appear in Fig. 28.1d. A resorbable and implantable electronic device with silk substrate and encapsulation for in vivo infection abatement has been also reported [20]. In addition, polymers directly extracted from fruits also have the potential to be used in biodegradable electronics. A resistive switching (RS) memory based on biocompatible pectin extracted from natural orange peel exhibits

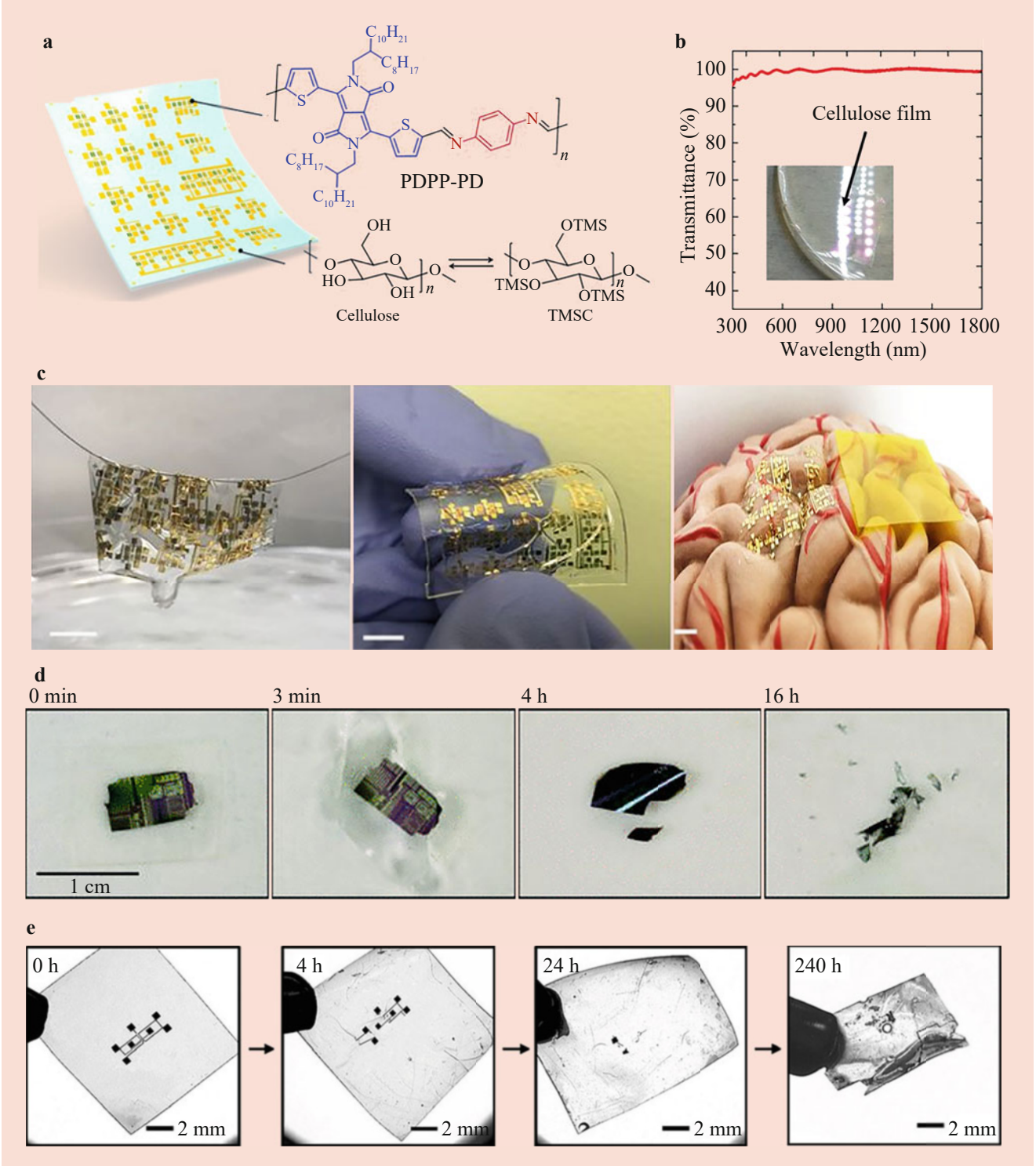

Fig. 28.1 Polymeric substrates. (**a**) Transistor and logic circuit using biodegradable polymer (PDPP−PD) semiconductor as the active material on biodegradable cellulose substrates and (**b**) optical transmittance of an 800-nm-thick cellulose film and an image of a cellulose film floating on water (inset). (**c**) Optical images of the dissolubility, flexibility, and conformability of the device. ((**a**–**c**) Reproduced with permission. [34] Copyright 2017, National Academy of Sciences) (**d**) Optical images of dissolution of an ultrathin transient CMOS device on a silk substrate. (Reproduced with permission. [35] Copyright 2015, American Institute of Physics) (**e**) Optical images at various stages of dissolution and disintegration of foundry-based transient electronics on the thin PLGA substrate. (Reproduced with permission. [36] Copyright 2017, National Academy of Sciences)

excellent RS characteristics [21]. Meanwhile, such device can dissolve in DI water within 10 min due to the good solubility introduced by the ionization of the carboxyl groups in pectin.

Biodegradable Plastics from Polyesters and Citric Acid. As early as 1973, it was shown that the polyester poly(ε-caprolactone), PLGA, degrades when disposed in bioactive environments such as soil [22]. Polyglycolic acid (PGA), polylactic acid (PLA), and their copolymers are some of the most frequently used biodegradable and bioresorbable polymer materials, in part because their properties can be tuned by changing the polymer composition within the basic PLA/PGA theme. PGA is a highly crystalline polymer and it has a high strength and modulus (7 GPa) which has promoted investigation to their use in bone internal fixation devices and sutures. PLA is often the polymer of choice for cast/extruded biomedical devices because it breaks down into L(+)-lactic acid units, which is the naturally occurring stereoisomer and is therefore excreted with minimal toxicity. Extensive research has been performed in developing a full range of PLGA polymers [23]. When the crystalline PGA is co-polymerized with PLA, the degree of crystallinity is reduced, and as a result this leads to increases in rates of hydration and hydrolysis. It can therefore be concluded that the degradation time of the copolymer is related to the ratio of monomers used in synthesis, and it ranges from 2–3 weeks to 3–4 months. Bao's group recently used PLGA (85:15) as substrate for the fabrication of organic transistors [24]. Another biodegradable polymer which is particularly important is poly(1,8-octanediol-co-citric acid), POC [9]. Rogers' group reported foundry-based microelectronics fabricated on PLGA substrates whose dissolution process is shown in Fig. 28.1e. It has shown potential to be used in tissue engineering, thanks to its nontoxic monomers, a relatively simply synthesis, an easy processing, and inherent surface affinity for various cells. Elasticity and biodegradability can be tailored by controlling the number of crosslinks. Young's modulus ranges from 1 to 16 MPa which are values comparable to those of elastin from bovine ligament. POC has been recently used as substrate for stretchable electrodes [25]. Electrospun poly(caprolactone)-poly(glycerol sebacate) (PGS-PCL) can also be utilized as substrates for engineering biodegradable electronics, in which PGS is another biodegradable elastomer widely used in cardiac tissue engineering [26].

Water-Soluble Polymers. The largest volumes of water-soluble polymers are prepared from acrylic acid, maleic anhydride, methacrylic acid, and various combinations of these monomers. With the exception of their oligomers, these polymers are not biodegradable. Conventional water-soluble polymers therefore persist in oceans, lakes, and other water depositories. To date, poly (vinyl alcohol) (PVA) is the only polymer with exclusively carbon atoms in the main chain that is regarded as biodegradable. PVA has been recently used in electronics as sacrificial layer for membrane release [27], as dielectric in organic devices [24], and as substrate for fully dissolvable IGZO transistors [28].

In all, these aforementioned polymers demonstrate desirable biocompatibility and biodegradability that can be tunable in wide timeframes. Degradation rates are closely associated with monomer structure, molecular weight, crystallinity, material processing, crosslinking, etc. [29]. Most of the biodegradable plastics based on polyesters and citric acid (PLGA, PGS, etc.) have a relatively faster degradation rate, e.g., PLGA (50:50) lost 20% of mass after 10 days in PBS [30], and PGS completely degraded in the subdermal region of SD rats within 60 days [31]; while degradation of PCL [32] and POC [9] can take more than 2 years. As for naturally derived polymers, silk can have degradation time over orders of magnitude (a few hours to a year) [13, 33], and the degradation time of BASF EcoFlex® is 11 weeks or more [17].

28.1.3 Metallic Conductors

Generally, metals serve as electrode contacts and interlayer connections for electronics due to the advantage of high conductivity and stable properties. Magnesium (Mg) is a representative biodegradable metallic material, with the combination of ease in processing, rapid rates of hydrolysis, and biocompatibility [13]. Alternative metals which share similar characteristics, such as zinc (Zn), iron (Fe), tungsten (W), and molybdenum (Mo), are also potential choices. An accurate study of the chemical dissolution of dissolvable metals has been conducted by Yin et al. [37]. The dissolution rate of different metal thin films in various solutions, which is defined as electrical dissolution rates (EDRs), was investigated by making patterned serpentine metal traces and monitoring the trend of resistance over time in DI water and salt solution under different conditions, as shown in Fig. 28.2. The dissolution rates of magnesium, tungsten, iron, molybdenum, and zinc metal thin films have been studied in deionized (DI) water and Hanks' solution at different pH and temperatures (Fig. 28.2a–f). The change in microstructure of these metals after soaking in DI water has also been investigated using transmission electron microscopy (TEM) (Fig. 28.2a–d). In general, the degradation rates in salt solution are higher than those in DI water, and changes in electrical conductions occur before the ones in the structural morphology. However, Mo demonstrates slower dissolution rates in salt solution than those in DI water. The rates also depend on how the materials have been deposited. Tungsten dissolves at a rate six times faster if deposited by sputtering rather than chemical vapor

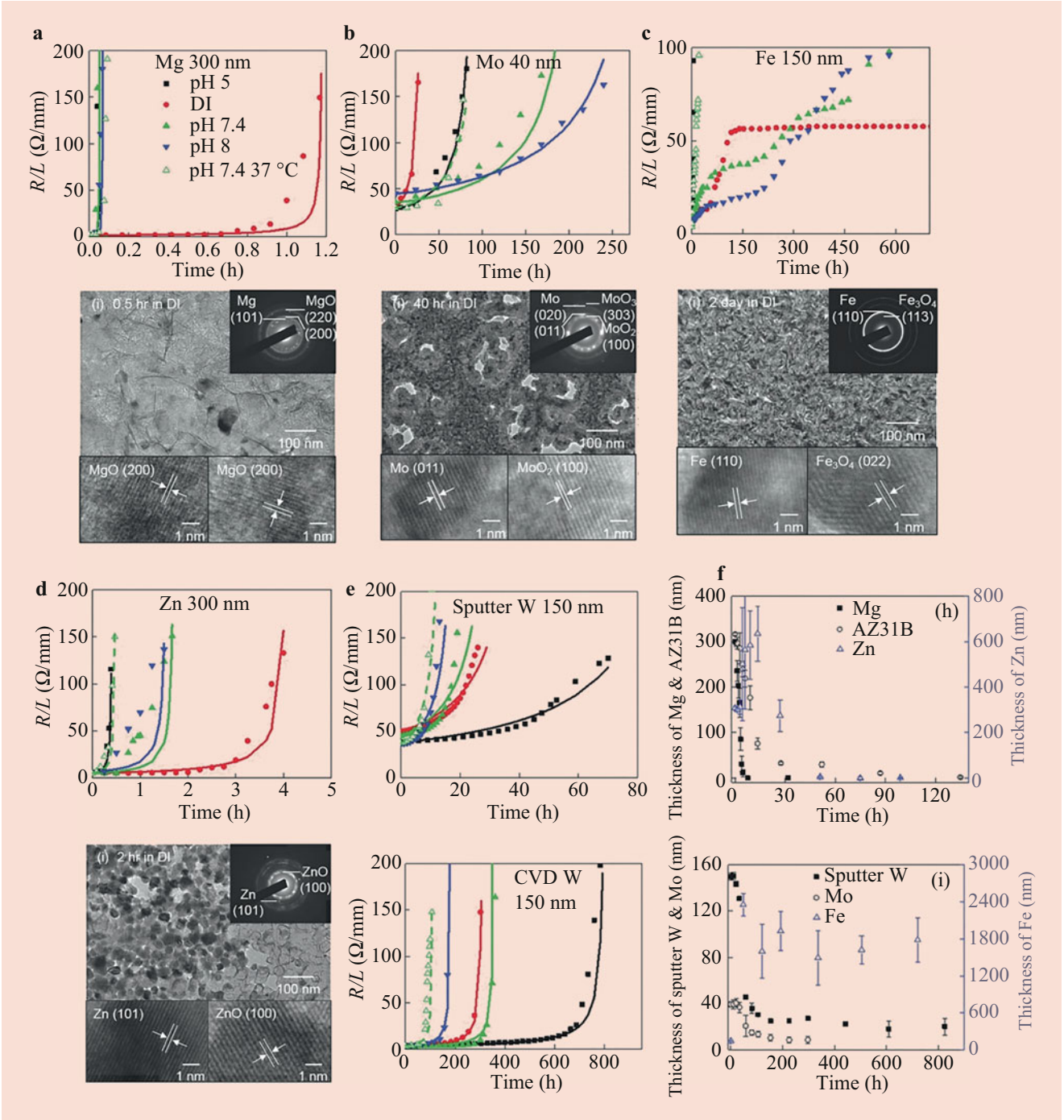

Fig. 28.2 Metals. The trend of resistance change over time during the dissolution process in Hanks' solution (pH 5, 7.4, and 8 at RT and pH 7.4 at 37 °C) and DI water at 37 °C, and TEM bright field images of the metals after dissolution: (**a**) Mg; (**b**) Mo; (**c**) Fe; (**d**) Zn. (**e**) The resistance changes over time during the dissolution process of sputter deposited W (above) and CVD W (below). (**f**) The trend of thickness over time during the dissolution process in DI water at RT: (above) Mg, AZ31B Mg alloy, and Zn; (below) Mo, Fe, and sputter deposited W. ((**a**–**e**) Reproduced with permission. [37] Copyright 2014, John Wiley and Sons)

deposition (CVD). TEM characterizations of metal thin films after dissolution in DI water show oxide formations on exposed surfaces as dissolution products. These residual oxides have much slower dissolution rates compared to those of the metals. So far, magnesium has shown excellent performance for contacting n-type silicon and oxide-based transistors [13, 38]. Table 28.1 summarizes the dissolution rates of the metals in various aqueous solutions and conditions.

Table 28.1 Metals. Dissolution rates of degradable metals in various solutions and conditions

Metals	T (°C)	Aqueous solution	pH	Dissolution rate ($\mu m\ h^{-1}$)
Mg [37, 39]	RT	DI water	–	0.3 ± 0.1
		HBBS	5, 7.4, 8	4.8 ± 2.2
		0.05 m NaCl	–	0.05–3[a]
	37	Simulated body fluid (SBF)	7.4	0.05–0.5[a]
AZ31B [40]	RT	DI water	–	0.08 ± 0.02
		HBBS	5, 7.4, 8	2.6 ± 2.1
		0.05 m NaCl	–	≈0.3[a]
		0.6 m NaCl		≈0.1[a]
	37	SBF	7.4	0.02–0.1[a]
W (S) [37, 40]	RT	DI water	–	$(4 \pm 1) \times 10^{-3}$
		HBBS	5	$(1.4 \pm 0.4) \times 10^{-3}$
			7.4–8	$(8 \pm 2) \times 10^{-3}$
		SBF	7.4	0.02–0.06[a]
	37	HBBS	7.4	≈0.02
W (C) [37, 41]	RT	DI water	–	$(7 \pm 2) \times 10^{-4}$
		HBBS	5	$\approx 2 \times 10^{-4}$
			7.4–8	$(7 \pm 2) \times 10^{-4}$
	37	HBBS	7.4	$\approx 2 \times 10^{-3}$
Zn [37, 42]	RT	DI water		0.07 ± 0.02
		HBBS		0.3 ± 0.2
		In vivo	–	$\approx 5 \times 10^{-3}$[a]
		Sea water		$\approx (2–8) \times 10^{-3}$[a]
Mo [37, 43]	RT	DI water	–	$(1 \pm 0.1) \times 10^{-3}$
		HBBS	5	$(6 \pm 2) \times 10^{-4}$
			7.4–8	$(2 \pm 0.3) \times 10^{-4}$
		Buffer solution	7	1×10^{-3}[a]
				Thin film: 2×10^{-4}[a]
	37	HBBS	7.4	$(7 \pm 4) \times 10^{-4}$
Fe [37, 40]	RT	DI water	–	$<1 \times 10^{-3}$
		HBBS	5	$\approx 9 \times 10^{-3}$
			7.4–8	$\approx 2 \times 10^{-4}$
	37	HBBS	7.4	$\approx 7 \times 10^{-3}$
		SBF		≈0.02[a]

All the dissolution rates are electrical dissolution rates (EDR) unless specified

[a] Stands for corrosion rates derived from mass loss, W (S) stands for sputter deposited W, W (C) stands for CVD W, HBBS stands for Hanks' balanced salt solution, SBF stands for simulated body fluid

28.1.4 Semiconductors

This class of materials is of great importance for the realization of high-performance electronic devices. Here the focus is mostly on inorganic materials. Table 28.2 summarizes the dissolution of the most widely studied degradable semiconductors in various aqueous solutions and conditions.

Si and III-V Semiconductors Hydrolysis of Si and SiO_2 is particularly important [13, 44–47]. Literature studies, involving basic aqueous solutions, suggest that silicon can form neutral ortho-silicic acid $Si(OH)_4$ either through an initial oxidation step to SiO_2 or through a direct equilibrium $Si + 4H_2O \rightarrow Si(OH)_4 + 2H_2$. In both cases, the silicic acid leaves the silicon surface by diffusion into the surrounding solution. The details depend not only on the crystalline form and morphology of the silicon and its doping level but also on the temperature and composition of the solution. Mechanisms for hydrolysis of silicon oxide are $SiO_2 + 2H_2O \rightarrow Si(OH)_4$. Because OH- initiates this reaction, the pH strongly influences the dissolution rates. Studies on the dissolution of alloys of silicon and germanium (SiGe) and monocrystalline Germanium have been also carried out [48].

ZnO and a-IGZO Oxide semiconductors such as zinc oxide (ZnO) and amorphous indium gallium zinc oxide (a-IGZO) are particularly attractive because they can be deposited on large scale at low temperature and exhibit properties (electric mobility, environmental stability) that

Table 28.2 Semiconductors. Dissolution rates of degradable inorganic semiconductors in various solutions and conditions

Semiconductors		T (°C)	Aqueous solution	Doping (cm^{-3})	pH	Dissolution rate (nm day^{-1})	
c-Si NMs [38, 46, 48]		20	Purified water	10^{15}(b)	5.5	<0.01	
				10^{20}(b)		<0.01	
			Tap water	10^{15}(b)	7.5	0.7	
				10^{20}(b)		0.4	
			Sea water	–		4	
		37	Bovine serum	10^{15}(b)		21	
				10^{20}(b)		0.5	
		37	Phosphate 0.05M–1M	10^{17}(p)	7.5	2.5–63	
		50				3.1–251	
		37	Chloride 0.05M–1M			1.5–63	
		50	Buffer solution 0.1M			5–398	
				10^{17}(p)		3.1	
				10^{20}(p)		0.5	
				10^{17}(b)		3.1	
				10^{20}(b)		0.2	
		37	Hanks' balanced salt solution (HBBS)	10^{15}(b)	7.6, 8.2	58, 129	
				10^{20}(b)		7, 58	
			HBBS w/Ca, Mg	10^{15}(b)	7.6, 8.2	66, 178	
				10^{20}(b)		8, 69	
Poly-Si NMs [48]		RT	Buffer solution	–	7	1	
					8	1.6	
					10	398	
		37			7	1.2	
					8	3	
					10	562	
a-Si NMs [48]		RT	Buffer solution		7	1.7	
					8	16	
					10	500	
		37		–	7	1.6	
					8	5	
					10	630	
Ge [48]		RT	Buffer solution		7	1.7	
					8	16	
				–	10	500	
		37			7	1.6	
					8	5	
a-IGZO [28]		37	Bovine serum			Zn	Ddisappear in 0.5 day
				–	–	Ga	Disappear in 0.5 day
						In	Disappear in 2 days
		60	DI water		7	Zn	Disappear in 2 days
						Ga	35 nm in 2 days
						In	Slow
			Phosphate buffer saline		7.4	Zn	Disappear in 0.3 day
						Ga	Disappear in 0.3 day
						In	Disappear in 1 day

(continued)

Table 28.2 (continued)

Semiconductors		*T* (°C)	Aqueous solution	Doping (cm^{-3})	pH	Dissolution rate (nm day^{-1})
ZnO [56, 57] (nanoparticle)	Size (nm)	RT	4-(2-hydroxyethyl)-piperazineethan-esulfonic acid (HEPES)	–	7.7–7.8	Dissolution rate (mg day^{-1})
	4					14.9 ± 0.3
	7–47					4.4–7.6
	130					3.4 ± 0.1
					4–11	Stable
Single-crystalline [49] ZnO(0001) surface		RT	Base electrolyte of $NaClO_4$	–	≤3.8	Dissolution events occur
NiO crystalline [50]		25–350	Aqueous solution	7–13		–
Poly-MoS_2 [58]		40	1M PBS	–	7.4, 12	0.01, 0.01
		85				0.27, 0.4

(p) stands for phosphorous doping, (b) stands for boron doping

outperform organic semiconductors. Recent works from Rogers' group have shown that both ZnO and a-IGZO are water soluble [28, 49]. Moreover, Ga and In are approved as alloys by the US Food and Drug Administration, and ZnO at concentration <100 μg/ml is biocompatible. Nickel oxide (NiO) is another candidate as semiconductor material [50]. Chemical studies show that NiO is water soluble: $NiO + H_2O \rightarrow Ni(OH)_2$. According to US dietary intake regulation, the tolerable upper limit of dietary nickel is 1000 μg/day, while estimated average ingestion is 69–162 μg/day [51]. Preliminary works have shown that sputtered NiO has a p-type behavior, and it can be used for the fabrication of p-n diodes [52]. Such results, however, were obtained on nonbiodegradable substrates.

Organic Semiconductors Organic materials represent a straightforward and most natural choice for the construction of degradable electronic devices because of their inherent biocompatibility [53]. Various π-conjugated molecules have been used as semiconductors including β-carotene and parylene. Among organic semiconductors for biodegradable electronics, Indigo deserves a special place. It is the most mass-produced dyestuff worldwide primarily for the coloring of the blue jeans. Indigo and its derivatives are thermally and photo-chemically stable and have been used by Bauer's group to realize field effect transistors with mobility in the order of 0.4 cm^2/Vs [54].

28.1.5 Dielectrics

Other water-soluble dielectrics include MgO and Si_3N_4 [55]. As in the case of SiO_2, such materials can be deposited on a large area and good quality and, hence, be used as insulators in thin film transistors [13]. Most of the polymers discussed in the paragraph 1.2 are dielectrics and can be used for the realization of electronics device [53]. One relevant example is PVA that can be deposited in thin film by spin coating [24]. Table 28.3 reports the dissolution rates of the most common degradable dielectrics.

28.2 Devices, Circuits, and Systems

While a lot of work has been done on the study of the dissolution dynamics of the materials, much less has been done on the fabrication of device and circuits. Most of the examples come from medicine and pharmacology. In 2003, Langer group demonstrated a PLGA-based device for multiple drugs delivery (pharmacy in a chip) [59]. A selective and controlled release of different drugs was achieved, thanks to 36 reservoirs and membranes with different molecular masses. Microneedles formed by PLA and carboxymethylcellulose have been also reported for transdermal drug delivery [5]. The dissolution of the needles, once injected into the skin, is responsible of the release. Dissolvable medical devices also include stents for angioplasty and magnesium scaffolds for tissue regeneration [60]. All these examples exhibit poor functionalities which usually consist of mechanical support and/or encapsulation. The development of transient electronics could instill "intelligence" to these systems and meanwhile keep the advantages of eliminating a second surgery for device retrieval. Biodegradable electronics would have great potential in scenarios where devices are only temporarily needed, as long as biocompatibility is not scarified for degradation. Biocompatibility therefore remains an essential consideration for building biodegradable electronics. To achieve ideal biocompatibility and functionality, both biologically benign dissolution products and mechanical/geometric properties have to be taken into account. Strategies ensuring biocompatible end products, reasonable release rates, and minimal and safe disintegrated fragments resulting from degradation would play an important role to maximize the benefits of transient electronics. Moreover,

Table 28.3 Dielectrics. Dissolution rates of degradable inorganic dielectrics in various solutions and conditions

Dielectrics	Fabrication method	T (°C)	Aqueous solution	pH	Dissolution rate (nm day^{-1})	Dissolution product
SiO_2 [55]	e-beam	37	Buffer solution	7.4	10	$Si(OH)_4$
	PECVD				0.1	
	Thermally grown				<0.01	
MgO [13]	e-beam	RT	DI water	7	1200	$Mg(OH)_2$
Spin on glass [40]	Cured at 300 °C	37	Phosphate-buffered saline (PBS)	7.4	50	$Si(OH)_4$
	Cured at 800 °C				6	
Si_3N_4[55]	LPCVD	37	Buffer solution	7.4	0.1	$Si(OH)_4 + NH_3$
				10	0.3	
				12	0.6	
	PECVD-LF			7.4	0.8	
				10	2	
				12	4	
	PECVD-HF			7.4	0.8	
				10	6	
				12	25	

various materials and device strategies have been proposed to realize soft, flexible, or stretchable electronic systems with mechanical properties close to biological systems and desirable device/tissue interfaces [61–65], which has already been involved in designing transient electronics.

28.2.1 Transistors and Circuits

The concept of "transient" or "biodegradable" electronics is very recent. In 2009, Rogers' group, at UIUC, demonstrated, for the first time, silicon transistors on silk substrate which dissolve in water [47]. One year later at Stanford University, Bao's group reported an organic biodegradable transistor on a poly(L-lactide-co-glycolide), PLGA, substrate [24]. The thin film transistors (TFTs) exhibit poor electron mobility which is about 0.253 cm^2/Vs, on/off current ratios (I_{on}/I_{off}) up to 9.4×10^3 and a threshold voltage of about −15 V. The same year, Bauer's group, at Johannes Kepler University, used natural materials like glucose, guanine, adenine, and indigo as semiconductors. The reported devices show a mobility of about 0.015 cm^2/V and an operating voltage as low as 5 V [66]. Another remarkable advancement arrived in 2012 when Rogers' group showed fully dissolvable, high-performance and scalable silicon-based components which dissolve in water at 37 °C. Here, the integration of crystalline silicon nanomembranes (NMs) on silk substrate enables operational characteristics comparable to standard consumer electronics. The resulting electrical properties for an n-channel device include mobility of 560 cm^2/Vs, on/off ratios of about 10^5, subthreshold slopes of 160 mV/dec, and width-normalized current outputs of 0.34 mA/mm.

In digital applications the main figures of merit are the threshold voltage (V_{th}), the ratio between the on and off current (I_{on}/I_{off}), and the subthreshold swing (SS). An ideal digital switch must have the V_{th} and SS as small as possible and the I_{on}/I_{off} ratio as large as possible. Analog designers are mostly interested at the transconductance (g_m) of the device and, hence, at its field effect mobility (μ). Such device-level parameters are ultimately influenced by (i) the intrinsic properties of the semiconductors-dielectrics-metals, by (ii) the combination of materials, by (iii) the interface between the gate dielectric and the semiconductor, and by (iv) the fabrication processes. The (i) has been discussed in the previous pages, while the (iv) will be described later in the chapter. It is worth highlighting the fact that the four mentioned points are interdependent. For example, the low-temperature polymeric substrates set constraints for the direct growth of crystalline materials and for their patterning and, eventually, limit the performance of the device.

Here, we will focus on some of the technological variables that must be considered to select the materials for the construction of a degradable transistor.

Dielectric Constant of the Gate Insulator In scaled transistor it is beneficial to adopt high-k gate dielectric in order to reduce the operating voltage and minimize the gate leakage. Among the inorganic and degradable dielectrics, Si_3N_4 has the highest constant (about 7) with SiO_2 and MgO that have 3.9 and 3.2, respectively. Among the organic materials, PVA has a dielectric constant in the range of 7–10 hence being suitable for the deposition of layers thinner than 50 nm. However, such thickness is hard to be achieved because of its low equivalent resistance at low voltage. Moreover, in organic transistors, the use of high-k gate dielectric layer may deteriorate the carrier transport. The energetic disorder caused by the dipoles in high-k dielectric tends to trap carriers from gate bias-induced conduction channel. The resulted localization

of charge carriers could cause not only mobility degradation but also increased hysteresis and device instabilities. It was shown that, by inserting a thin, low-*k* dielectric layer between the high-*k* one and the channel, the dipole field can be effectively screened for improved device performance [67].

Semiconductor-Dielectric Interface As the dielectric surface roughness increases, the morphology of the dielectric-semiconductor interface changes significantly, and the mobility of the transistors decreases rapidly. It is suggested that the increased lateral grain boundaries limit the transport between domains and reduce the field effect mobility. It is also found that the V_{th} shift caused by gate bias stressing was extremely sensitive to the dielectric surface roughness. The rougher dielectric surface afforded a larger V_{th} shift. The researchers suggested that the increasing amount of trap states enhanced by the rough dielectric surface is the original reason of this instable V_{th}. Other effects are the increase of the subthreshold swing and the appearance of the hysteresis in the transfer characteristic of the device [68].

In addition to the roughness, the performance of the transistors is highly affected by the surface energy of dielectric layers. Different from the dielectric roughness, the surface energy impacts the performances of organic transistors not by hindering the charges transport directly but by influencing the orientation of semiconductor molecules and the morphology of semiconductor layers. The researchers find the grain size of pentacene increased with the increase of dielectric surface energy. Consequently, depressed mobility of OFETs is observed on high surface energy dielectric layers even with larger-grain morphology [69].

In general, the above described effects are valid for both organic and inorganic materials, and they depend on the growth/deposition conditions, usually with larger effects in case of low-temperature processing on polymeric deformable substrates. The correct choice of the device structure, i.e., top or bottom gate, staggered or coplanar, may also play a role and, eventually, alleviate some of the listed issues.

Band Alignment The choice of the materials defines the band alignment. Of great importance is the alignment of the energy levels for the gate stack and for the source/drain metallization. Here, the focus is on the dielectric semiconductor bandgap, but many references are available on the other subjects [70, 71]. Figure 28.3 reports the band alignment for most of the semiconductors and dielectrics that have been chosen to build degradable transistors. Ideally the dielectric bandgap should be as large as possible and should be aligned with the semiconductor bandgap in order to minimize the gate leakage for both p- and n-type devices. The plot highlights how the shifted gap of indigo would result in higher leakage and, hence, in a smaller I_{on}/I_{off} ratio (see Table 28.4). In this regard, Si, Ge, and MoS_2 are better choices.

Anisotropy and Polarity The performance of the transistors, especially the V_{th} and the V_{on}, is to a great extent affected by the polar groups on the gate dielectric. Take p-type channel OFETs as an example; in case where the end groups at the interface are electron-withdrawing groups (e.g., -F), this means electrons from the semiconductor film will be attracted by the additional holes supplied by those groups in the channel. Thus, a more positive gate bias is needed to switch off the device [69].

The directionality of the semiconductor bonds also plays a role. For example, the excellent charge transport properties of indigoid dyes are attributed to the strong intermolecular interactions of π-stacking reinforced by hydrogen bonding. Due to the directionality of π-stacking (typically along the crystallographic b-axis for most indigoids), charge transport is highly anisotropic. In order to achieve good OFET performance, molecules must adopt a "standing-up" conformation, with π-stacking parallel to the gate dielectric. To achieve this, aliphatic dielectric materials are used, such as polyethylene or the natural oligoethylene tetratetracontane [54].

Table 28.4 contains a list of field effect transistors that have been reported over the last 20 years with the constituent materials and their main electrical properties. However, the excellent performance of inorganic transistors often comes at costs of serial and complicate fabrication process which involve multiple micro-transfer printing steps to move the silicon NMs from the native silicon on insulator (SOI) wafer to the final degradable substrate. So, while the use of organic semiconductors sets stringent constraint to the performance and stability of the transistors, the abstruse manufacturing of silicon NMs hinders the fabrication of complex circuits with only few examples limited to basic digital block-like inverter, AND, and NAND [72].

The developments of more complex circuits, both analog and digital, would be indispensable to build systems which are able to amplify, filter, digitalize the signal acquired by the sensors, and communicate the data wirelessly. These are all necessary requirements to build the next generation of resorbable medical implants and compostable deployable sensors.

Only a few examples of logic circuits have been reported, including basic logic functions like inverters, ANDs, and NANDs made of silicon nanomembranes as semiconducting layer [36, 72], ring oscillators, as well as analog amplifiers in stacked 3D assembly using foundry-based microcomponents [35, 73], a-IGZO-based ring oscillators working at 19 V and up to 57 kHz [28]. Gallium arsenide has been also used to fabricate microwave electrical components on flexible cellulose nanofibril paper proving that it is feasible to fabricate high-performance flexible electronics using ecofriendly materials.

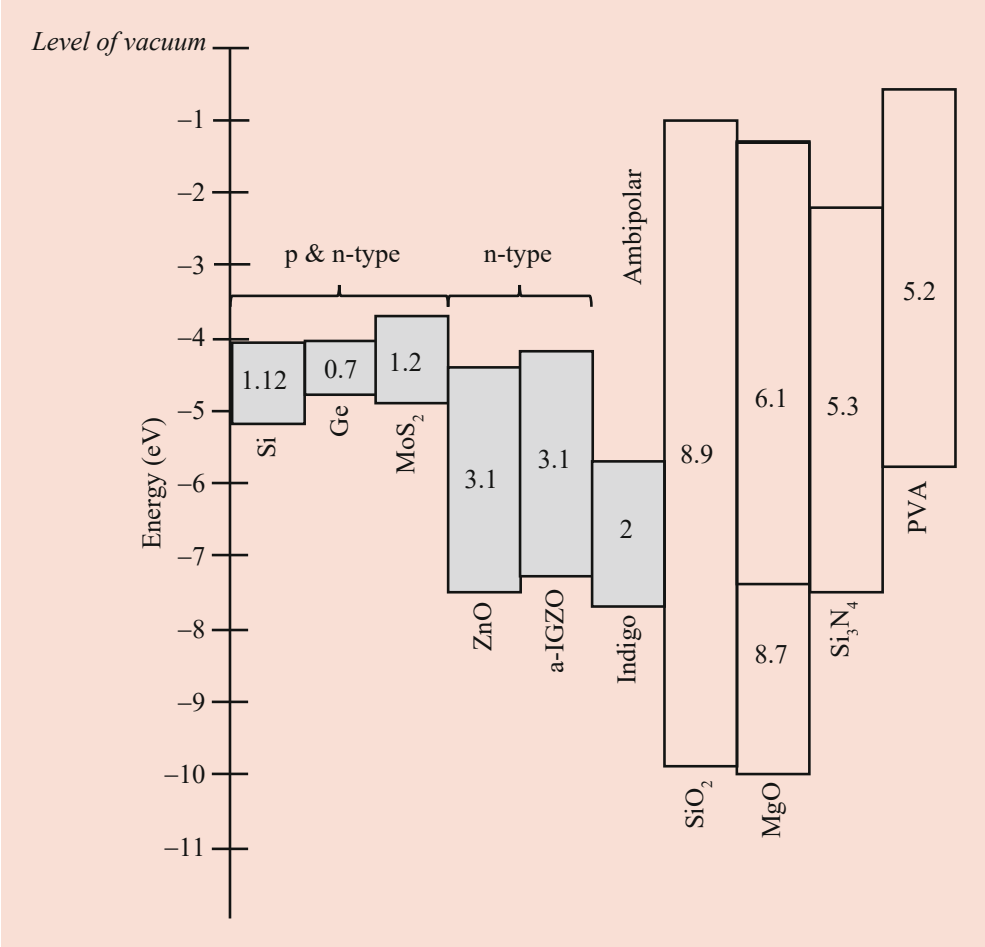

Fig. 28.3 Semiconductor-dielectric band alignment. Band alignment of most common semiconductors and dielectrics used to build biodegradable MOSFETs

Table 28.4 Transistors. Reported field effect transistors with constituent materials and electrical properties

Device	Semiconductor	Gate dielectric	Substrate	Mobility (cm^2/Vs)	Threshold voltage (V)	I_{on}/I_{off}	Year-group
n-MOSFET	c-Si	SiO_2	Silk film	500	0.2	$>10^4$	2009-Rogers'
p-MOSFET	DDFTTF	PVA	PLGA	0.25	−15	10^3	2010-Bao's
Ambipolar MOSFET	Indigo	Glucose, guanine, adenine, wax	Shellac (natural polyester resin)	0.4	5	10^3	2010-Bauer's
n and p MOSFET + basic logic circuits	c-Si	SiO_2	Silk film	500	0.2	10^5	2012-Rogers'
n-MOSFET	ZnO (sputtered)	MgO	Silk	1	1	$>10^3$	2013-Rogers'
n-MOSFET + ring oscillator	a-IGZO	SiO_2	PVA	10	2	10^5	2015-Rogers'

"c-" stands for crystalline silicon, "a-" stands for amorphous indium gallium zinc oxide

28.2.2 Sensors

Resorbable or biodegradable sensors are probably the most appealing and important class of devices which can be developed by this technology, with applications spanning from biomedical and implantable devices to environmental deployed sensors [45, 74]. Recently, Salvatore et al. reported a fully biodegradable temperature sensors made of Mg microstructures encapsulated by compostable EcoFlex® thin layers [18]. Such devices have fast dynamic response and high flexibility prospecting their use in packaging for food monitoring.

In biomedical applications, the specially designed flexible transient electronics can be closely connected with tissues

and organs; thus it can detect abnormal physiological signals sensitively and accurately, which is of great help to human disease monitoring and rehabilitation. There are various single-functional or multifunctional biodegradable sensors reported. Rogers' group utilizes MoS_2, a 2D material with unique mechanical, thermal, electrical, and optical properties, to create a multifunctional biosensor with good biocompatibility and biodegradability for accurate measurement of pressure, temperature, strain, and motion [58], as shown in Fig. 28.4a–e. Here, the CVD-grown polycrystalline MoS_2 monolayer film (grain size ~200 nm) takes about 2 months to completely dissolve at 37 °C in PBS solution. Rogers' group also developed a set of biodegradable transient electronics using doped silicon nanomembranes [25]. Figure 28.4f, g shows the device architecture of a stretchable and biodegradable pH biosensor and electrophysiology (EP) biosensor. In addition, Yu et al. reported a soft and high-resolution electrocorticography (ECoG) recording system based on Si devices which records in vivo electrophysiological signals from the cortical surface and the subgaleal space [75]. The

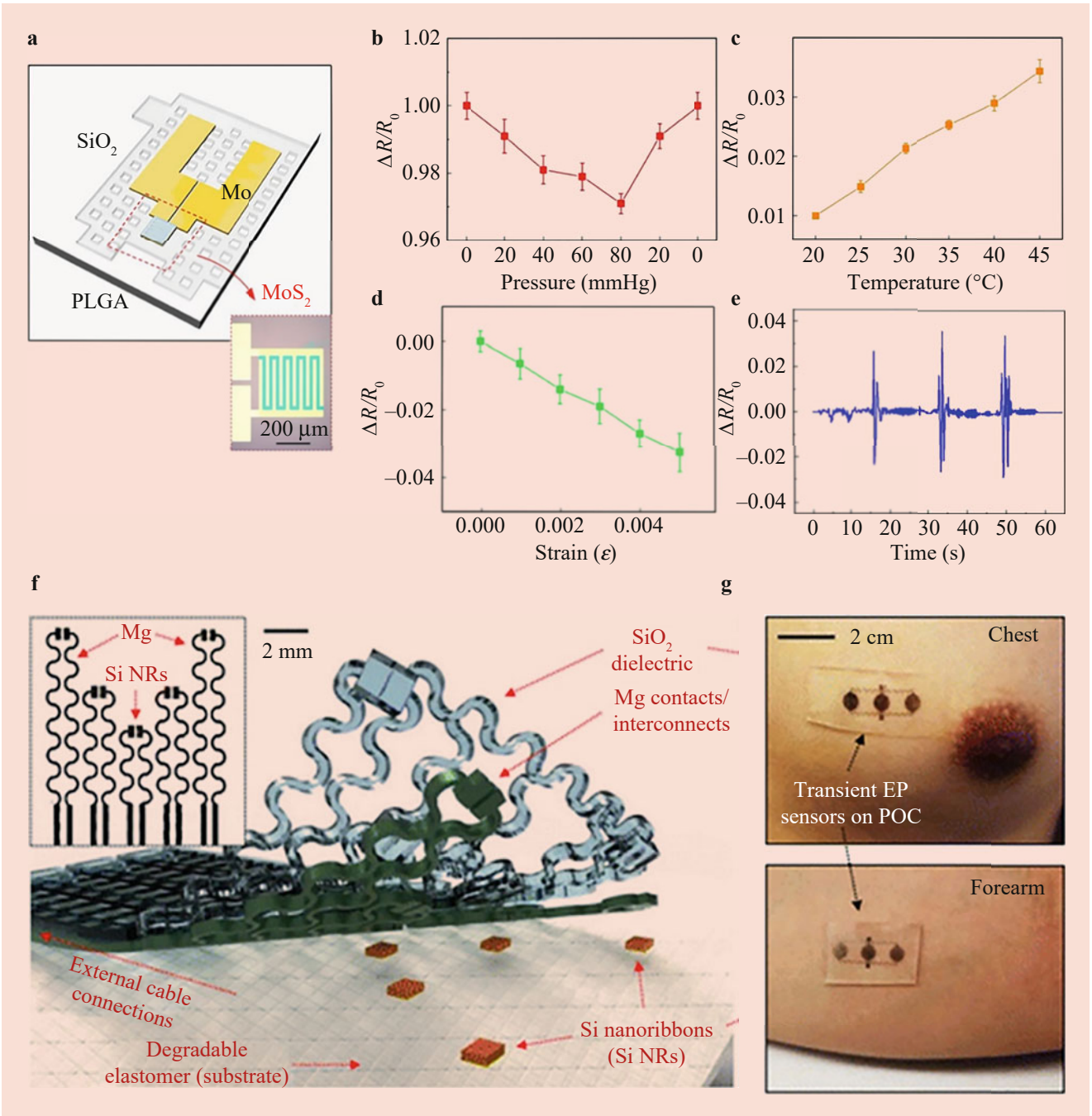

Fig. 28.4 (continued)

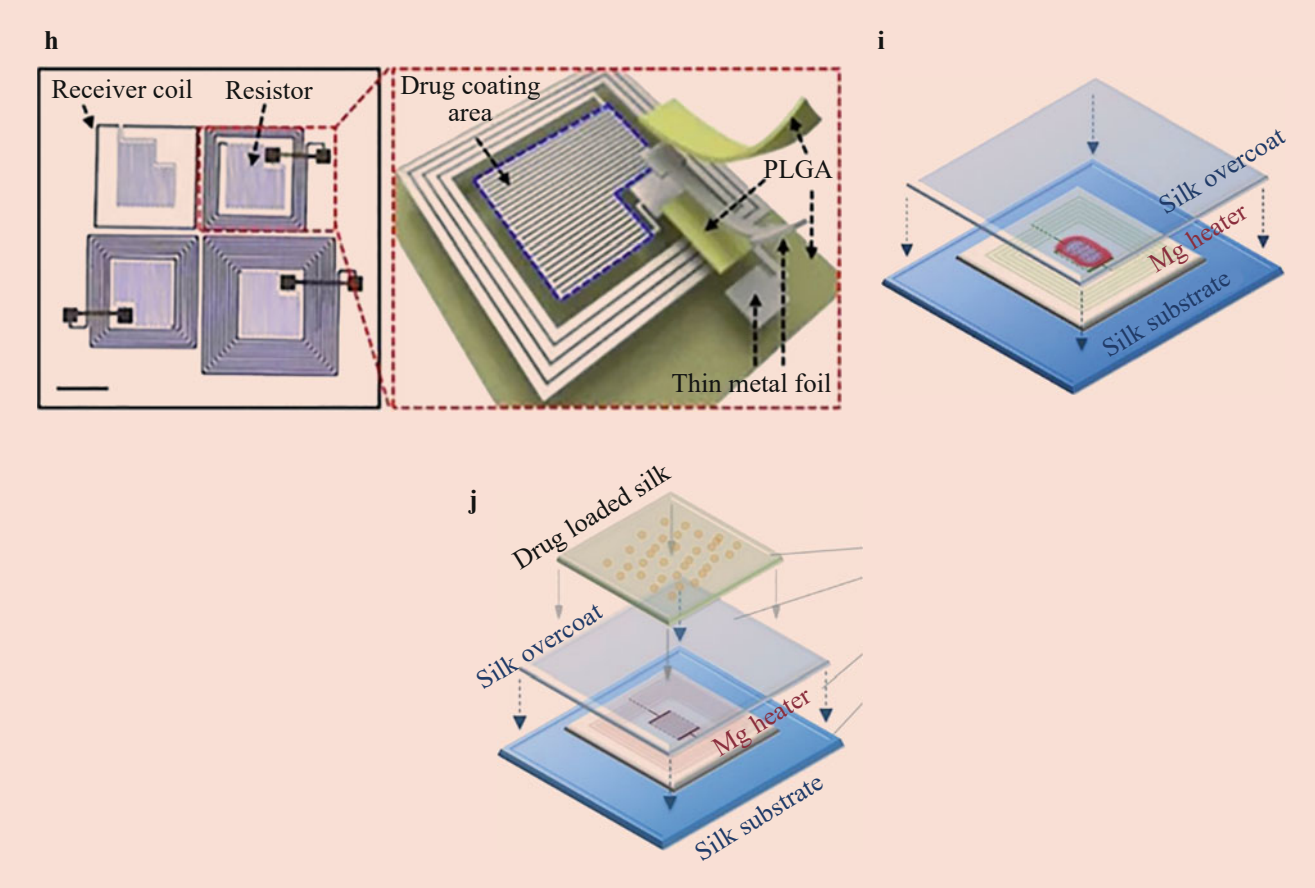

Fig. 28.4 Sensors. Biodegradable devices with different functions. (**a**) A multifunctional sensor using MoS_2. (**b**–**e**) Characteristic responses of the MoS2 sensor as a function of pressure (**b**), temperature (**c**), strain (**d**), and acceleration (**e**). ((**a**–**e**) Reproduced with permission. [58] Copyright 2018, Springer Nature) (**f**) A biodegradable, stretchable pH sensor based on doped silicon nanomembranes. (**g**) An EP sensor mounted on the chest for ECG (above) and EMG (below) detection. ((**f**) and (**g**) Reproduced with permission. [25] Copyright 2015, American Chemical Society) (**h**) Optical image of a bioresorbable drug delivery device that can be remotely activated by radio frequency, which is made up of a 2 × 2 array of inductive coupling coils and serpentine thermal actuators on a bioresorbable substrate (left); schematic exploded view illustration (right). (Reproduced with permission. [77] Copyright 2015, Springer Nature) (**i**) A silk-based bioresorbable electronic device for remotely controlled therapy. (**j**) The device in (**i**) can also be used for wirelessly activated drug release. ((**i**) and (**j**) Reproduced with permission. [20] Copyright 2014, National Academy of Sciences)

flexibility allows the device to be in close contact with the cerebral cortex, ensuring high data accuracy. Furthermore, such device can be completely degraded in PBS solutions, thus avoiding the risk of re-surgery removal to the brain. Kang et al. also reported a bioresorbable pressure and temperature Si sensor for the brain [45]. Moreover, recent studies have reported optical sensors functionalized with binding elements (such as receptors, antibodies, nucleic acids, enzymes, etc.) integrated with the device to react with target molecules [76].

Thermal therapy platforms and drug delivery systems have also gained much attention from researchers. Certain bacteria, such as *Staphylococcus aureus*, are highly sensitive to environmental changes, and their survival is reduced with an increase in the temperature. Based on this principle, it is possible to heat the specific part by implanting devices to achieve the effect of promoting wound healing. As shown in Fig. 28.4j, Tao et al. developed a transient radio-frequency (RF) device based on a Mg heater embedded between silk fibroin layers [20]. Such therapeutic device made of fully biodegradable packaging materials and electronics can be remotely activated by radio frequency after implantation. In addition to being able to heat specific sites, such thermal therapy platforms can also be used to trigger drug delivery, such as enhancing ampicillin molecular release in the silk fibroin film by an increase in temperature. Another work done by Rogers' group provides a biodegradable device that combines thermally actuated lipid membranes loaded with multiple types of drugs in a spatial array, which can be remotely activated by radio frequency [77]. Such device enables external excitation while precisely controlling drug dose. A wireless and programmable bioresorbable electrical stimulation platform has also been proposed to facilitate peripheral nerve regeneration [78].

28.2.3 Optical Devices: LEDs

Researches of biodegradable LEDs to replace commercial LEDs (high chemical stability and the risk of releasing toxic heavy metals) for use in the medical and environmental sectors expand the range of applications for such electronics. There are already some works to explore the material choices for biodegradable LEDs, such as partially biodegradable riboflavin- and peptide-based organic devices [79, 80]. Lu reports the first examples of LEDs with full biodegradability in aqueous solutions [81]. The device is demonstrated by the use of a II–VI semiconductor, ZnO, and an ultrathin (8 nm) transparent electrode of Mo, with a maximum optical power density of 0.7 mW cm^{-2} at 9 V.

Another interest in optical devices is providing intimate optical coupling to biological tissues based on the interaction of light with biological materials [19, 82]. Macromolecular materials such as silk fibroin, PLGA, and PLA are demonstrated to serve as bioresorbable waveguide materials. The main drawbacks, however, include swelling due to water absorption and limited contrast in index of refraction [83]. Recently, a silicon-based, bioresorbable photonic platform is established, in which thin filaments of monocrystalline silicon encapsulated by polymers as flexible, low loss, dimensionally stable, and bioresorbable optical waveguides provide precise optical transmission and sensing at targeted sites in biological systems [84].

28.2.4 Powering Devices: Batteries, Photovoltaics,and Energy Harvesters

Power devices are an important part of biodegradable electronics as they are essential to ensure stable operation of the electronic system in the human body. For biomedical applications, power devices need to be flexible, stretchable, and miniaturized, while the constituent materials should be highly biocompatible and fully degradable in vivo [85]. Currently, biodegradable power devices are expanded into the following categories: batteries, supercapacitors, photovoltaic devices, radio-frequency (RF) power scavengers, piezoelectric harvesters, etc.

Batteries. Biodegradable batteries providing energy for self-powered electronics in vivo have high-energy density and excellent biocompatibility. At present, researches on biodegradable batteries mainly focus on galvanic cells using biocompatible metallic electrode systems and metal-ion battery systems. For the former, Fig. 28.5a, b shows a biodegradable primary battery system consisting four Mg-Mo cells, with polyanhydride serving as spacers and packaging material [86]. Such battery system can provide a stable output voltage up to 1.6 V for 6 h at a constant current density of 0.1 mA cm^{-2}. Another fully biodegradable battery using Mg and molybdenum trioxide (MoO_3) in Fig. 28.5c provides a highly stable output voltage up to 1.6 V and capacity up to 6.5 mAh cm^{-2} while having a lifetime of 13 days [87]. For the latter, Kim et al. have reported an edible sodium ion battery with biologically derived melanin as an electrode [88]. Magnesium-iron storage devices with polycaprolactone (PCL) as a packaging and functional material have been also demonstrated [89].

Supercapacitors. Supercapacitors are an important energy source choice because of their higher power density, charge/discharge rates, and longer cycle lifetime compared to batteries. They store energy by forming an interface bilayer between the electrode and the electrolyte either through ion adsorption or redox reaction. A supercapacitor can be fabricated by a variety of different materials (metals, oxides [13, 90, 91], silicon [92], and organic polymers [93]) combined in the form of thin films. Based on such process, biodegradable supercapacitors can be developed by considering the degradation properties, biocompatibilities, and flexibilities of materials. Lee et al. provided the first fully biodegradable and edible supercapacitor using metallic electrodes (W, Fe, or Mo) and hydrogel electrolytes made of NaCl/agarose, both of which are biodegradable materials [90]. The supercapacitor provides a capacitance of 1.6 mF cm^{-2} and power density of 1 mW cm^{-2}. Studies on eumelanin have also demonstrated that this biocompatible and biodegradable material may be an effective candidate for future supercapacitor electrodes [93], as shown in Fig. 28.5d.

Photovoltaic devices. Photovoltaic (PV) power generation is a technology that directly converts light into electricity by utilizing the photovoltaic effect of the semiconductor interface. As a clean energy technology that has been developed worldwide in recent years, the light conversion efficiency of PV cells has been greatly improved, which also laid the foundation for its functional devices as implantable electronic devices. Unlike photovoltaic power generation in vitro, photovoltaic cells implanted in vivo are completely encapsulated in biological tissues (such as skin, fat, muscles, etc.) and in most cases are inefficient due to the absorption and scattering of light. Currently, biological tissue has two optically transparent windows in a specific near-infrared spectral region (NIR), 650–950 and 1000–1350 nm, respectively [88, 94]. Kang et al. have reported a fully degradable amorphous silicon (a-Si) transient thin film solar cell consisting of zinc oxide and magnesium, which can be completely degraded in a few days [48]. Lu et al. studied the first fully biodegradable silicon solar cells working in vivo [44], which appears in Fig. 28.5e, f. The fabricated PV cell array generated ≈60 μW of electrical power under 4 mm of porcine skin and fat, with an optical power density of 200 mW cm^{-2} produced by a NIR (780 nm) light-emitting diode (LED). The entire photovoltaic system coated with polylactic acid-glycolic acid (PLGA)

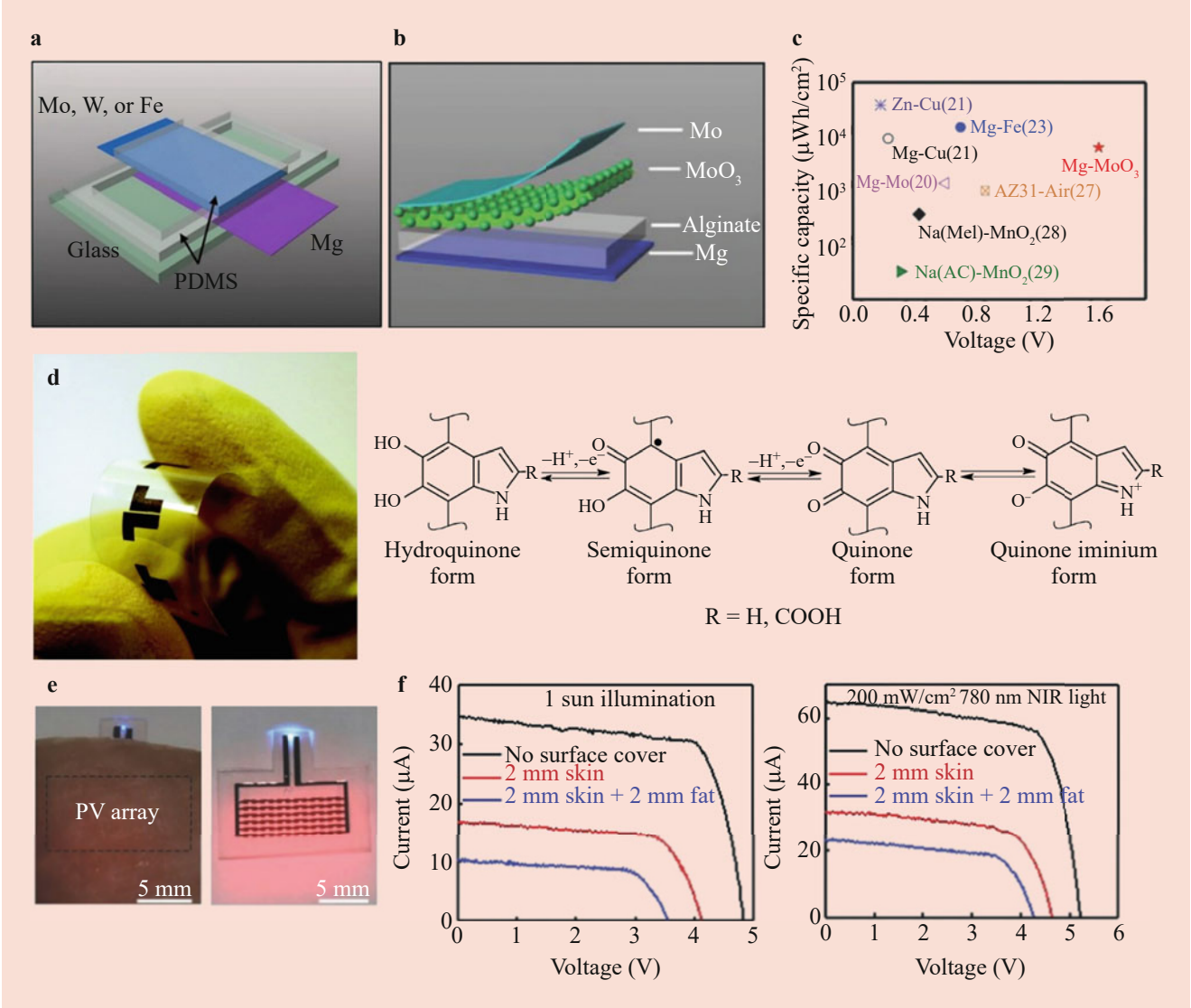

Fig. 28.5 Powering devices. Biodegradable powering devices. (**a**) A single-cell Mg-X battery (X = Mo, W, Fe). (Reproduced with permission. [86] Copyright 2014, John Wiley and Sons) (**b**) Materials and structure of a fully biodegradable Mo-MoO_3 battery. (**c**) Specific capacity versus voltage of reported biodegradable batteries. ((**b**) and (**c**) Reproduced with permission. [87] Copyright 2018, John Wiley and Sons) (**d**) Left, optical image of a melanin-based micro-supercapacitor on a flexible PET substrate; right, the redox process of melanin is the form of hydroquinone (H2Q), semiquinone (SQ), and quinone (Q). (Reproduced with permission. [93] Copyright 2016, Royal Society of Chemistry) (**e**) Optical images of an Si PV system operating blue LEDs. (**f**) Current/voltage characteristics of the PV array with no surface cover (black), with skin on its surface (red) and with skin and fat on its surface (blue), measured under 1 sun illumination (left) or under 200 mW/cm^3 780 NIR light (right). ((**e**) and (**f**) Reproduced with permission. [44] Copyright 2018, John Wiley and Sons)

matrix can be almost completely degraded by hydrolysis after 27 days, which proves the feasibility of biodegradable photovoltaic cell system. However, biodegradable photovoltaic cells currently have problems such as light source scattering, absorption, excessive depth limitation (several millimeters), and potential tissue heating [85].

Radio-frequency (RF) power scavengers. Power harvesting via radio-frequency transmission was reported by Rogers' group for the realization of resorbable implants such as the neural cuff. One of these devices demonstrated real therapeutic functionality for infection abatement [20]. After 15 days the device, constituted by a Mg planar coil, a drug reservoir, and silk layers as substrate and encapsulation, was fully resorbed by the body without any inflammatory response in the associated tissues. In addition to neurotherapy, radio frequency can also be used in offering power for thermal therapy platform [20] and drug delivery [69], as discussed in 28.2.2.

Piezoelectric energy harvesters. Piezoelectric energy harvesters (PEHs) directly generate electrical energy by con-

verting mechanical motion in the human body like heartbeat, breathing, etc. Due to the advantages of high-power density, simple structure, and good scalability, PEHs can also be potential energy supply devices in vivo. Most high-performance inorganic piezoelectric materials are inherently rigid and brittle; thus devices would require special design to be flexible and stretchable. Meanwhile, biocompatibility and biodegradability are also important indicators for selecting materials for biodegradable piezoelectric devices. Dagdeviren et al. used a variety of water-soluble materials to form a piezoelectric energy harvester: ZnO (semiconductor/piezoelectric), Mg (conductor), MgO (insulator), and silk (substrate) [49]. The voltage and current outputs of the system are 1.14 V and 0.55 nA. The entire system can completely dissolve in DI water within 60 min at room temperature.

28.3 Dissolution Mechanisms

In most of the devices that have been described in the previous paragraphs, the decomposition is controlled and tuned by designing the thickness of the encapsulation and its composition. The dynamics of degradation proceeds through hydrolysis, enzymatic degradation, or electrochemical dissolution and is governed by chemical reactions and diffusion mechanisms, and it is, hence, complicated to be accurately predicted. It depends on pH, temperature, and spatial distribution of the etchants, processing, and geometrical layout of the structure. Moreover, the desired time scale for transience depends on the application, and it ranges from days or weeks (post-surgery treatment) to weeks/months (environmental sensors) and to years (security systems and consumer electronic devices). Finally, in some cases (i.e., failure of the device), it would be important to trigger the immediate degradation process in response to external stimuli. Such requirements can be effectively addressed only if the electronics is combined with microfluidic devices in order to achieve a timely and spatially controlled dissolution. A temperature expandable polymer (Expancel 031 DU 40, AkzoNobel), which is activated by micro-machined heater, has been used to release water from a reservoir-based device [95]. Despite the difficulty in the assembly due to the heterogeneity of the components (heaters, microfluidic channels and reservoirs, electronics), this device constitutes the first example of triggered and remotely controlled dissolution. Although most on-demand degradation has so far been limited to non-biomedical application, fully degradable device capable of controlled drug release device has been achieved [69, 96]. Involving stimuli-responsive materials extensively explored as drug delivery vehicles could provide potential routes to combine triggered degradation with implantable biodegradable electronics, which will endow more versatile functionalities and further advance the technology.

Modeling of dissolution rates. In the study of the dissolution mechanisms of biodegradable electronics, the dissolution rates of materials are important parameters for judging the overall dissolution time of the devices. Considering the complexity of the actual dissolution process, a simplified one-dimensional reactive diffusion model is proposed to simulate the overall dissolution kinetics for Si and dissolvable metals [97]. The analytical solution to the model can be fitted to the measured data, and key parameters that are not existing in the literature can therefore be extracted, which could predict dissolution rates under the same conditions. The reactive diffusion model takes into account both chemical reactions and diffusion of water into the materials. The diffusivity of water in the metal film (D) and the reaction rate constant (k) are the two key parameters. With $y = 0$ as the bottom surface of the material, and $y = h_0$ as the top surface of the materials, water concentration $w(y, t)$ at time t and thickness y satisfies the reactive diffusion equation

$$D\frac{\partial^2 w}{\partial^2 y} - kw = \frac{\partial w}{\partial t} \quad (0 \le y \le h_0) \tag{28.1}$$

Conditions include a constant water concentration (w_0) at the top surface of the layer $w|_{y=h_0} = w_0$ $\left(w_0 = 1\ \mathrm{g\ cm^{-3}}\right)$ and zero water flux at the bottom surface $\partial w/\partial t|_{y=0} = 0$, as well as zero initial water concentration $w|_{y=0} = 0$ $(0 \le y < h_0)$. Thus, the analytical solution to Eq. (28.1) is as follows:

$$\frac{h}{h_0} \approx 1 - \frac{t}{t_c} \tag{28.2}$$

where h_0 represents the initial thickness and $t_c = h_0 q_\rho M_{H_2O}\left(\sqrt{kD}w_0 M\right)^{-1} \tan h^{-1}\sqrt{kh_0^2/D}$ represents the critical time when the thickness reaches zero, ρ is the mass density of the materials, and M and M_{H20} are the molar masses of the materials and water.

Dissolution mechanisms of Si nanomembranes. In Fig. 28.6a–c, Yin et al. revealed the effect of anion concentration and temperature on the hydrolysis of silicon nanomembranes at the near neutral pH and proposed an empirical model for predicting the dissolution rate of silicon [98]. The anions (chlorides and phosphates) in the solution promote surface silicon oxidation by weakening the bonding of atoms on the surface to the internal atoms. The dissolution rates can be written as

$$r^{\mathrm{model}} = k_0\left(-\frac{E_a(M)}{k_B T}\right)[H_2O]^4\left[OH^-\right]^{0.25}[M]^{0.25} \tag{28.3}$$

$$k_0 = 2480\ \mu\text{m h}^{-1}\left(\frac{\text{mol}}{\text{L}}\right)^{-4.5} \tag{28.4}$$

$$M = \text{PO}_4^{3-} \text{ or } \text{Cl}^- \tag{28.5}$$

where k_B is the Boltzmann constant, $E_a(M)$ is the activation energy for hydrolysis, $[H_2O]$ is the concentration of water and is approximately constant, and [M] represents the concentration of a specific ion (e.g., $[PO_4{}^{3-}]$, and $[Cl^-]$). Similar results were obtained by Wang et al. [99]. In Fig. 28.6d, they found that size and doping level of the silicon nanomembranes can affect the dissolution rates, and molecular dynamics simulations were used to support such conclusions. The dissolution rates can be written as the following to indicate the size effect:

$$R = r_{\text{model}}\left(1 - \text{e}^{-bx}\right) \tag{28.6}$$

where x represents the size of the silicon nanomembrane and b represents the coefficient of the size-dependent behavior.

28.4 Fabrication Examples

Constituent materials of biodegradable electronics are sensitive to temperature, solvent, or water, e.g., biodegradable metals have fast dissolution rates in water and etchants, and biodegradable polymers have low glass transition temperatures and can easily dissolve in solvents. Therefore, conventional photolithography process and thin film deposition techniques that involve harsh solvents and elevated temperatures can hardly be used for the fabrication. To address the issues, device patterning is either performed using shadow masks which constrains the spatial resolution or through a transfer printing technique by fabricating devices on stable substrates followed by a subsequent transfer onto a final biodegradable substrate which involves multistep processing. Currently, most of the demonstrated biodegradable electronics are based on mono-Si NMs due to its excellent electronic properties and fully biodegradable abilities [100]. A variety of works have been done to solve the problems in the fabrication of such biodegradable electronics. First of all, in order to harvest high-quality mono-Si NMs from a SOI source wafer onto a biodegradable substrate, researchers have developed a series of transfer printing techniques [101]. For example, Rogers' group has proposed a two-step transfer printing process to fabricate transient complementary metal-oxide-semiconductor (CMOS) on biodegradable substrates [102]. The fabrication of MOSFETs starts from silicon on insulator (SOI) wafers that are doped and HF under-etched to release the 100–300 nm nanomembrane of silicon. The silicon membrane is then transfer printed with a soft stamp (PDMS) onto a polyimide-spin-coated wafer with a sacrificial layer in between to complete the fabrication (gate oxide deposition and contact formation). A second transfer process is required to transport the devices with PI supporting layers onto the target degradable substrates. The PI layers are removed during the second transfer process to achieve the fully biodegradable devices. Foundry-based process has also been proposed as a possible method to fabricate integrated biodegradable electronics with more complexity. Water-soluble integrated circuit at the 90 nm node was produced through foundry-compatible fabrication processes, by thinning of a SOI wafer down to 1 μm and transfer-printing onto a silk fibroin substrate [35]. Tungsten acts as a bioresorbable metal for interconnects as well as vias in such electronic devices. Another work suggests to fabricate foundry-based ultrathin silicon components on SOI wafers and release the whole arrays by anisotropic etching in potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH) solutions [36], as shown in Fig. 28.7. The device is then transfer-printed onto a PLGA substrate for planarization and metallization [36].

Printing of biodegradable metallic components has also been proposed for high-speed and low-cost manufacturing of biodegradable antennas and green electronics [100]. The initial work by Huang was limited by the relatively low conductivity because of the formation of surface oxides on metal powders [103]. Further strategies have been proposed to remove surface oxides such as Ball milling and photonic sintering [104], laser sintering and printing [56], and acid treatment [57]. On the other hand, high conductivity Zn nanoparticles (Zn NPs) are used to achieve highly conductive circuits, making the devices suitable for various eco-friendly circuits [56].

Encapsulation processes of biodegradable electronics have become critical to ensure reliable operation. It is also of great interest to effectively control the operational lifetime of the devices. Transient devices generally have a two-stage operation mode (stable operation and rapid degradation under specific external stimuli) [105]. A typical device of such type suggests a N-MOSFET encapsulated by MgO and crystallized silk, which has a stable operation for ~90 h immersed in DI water, with rapid degradation after water penetration. Introduction of various encapsulation materials can extend the functional lifetime to different extent, including biodegradable polymers, plasma enhanced chemical vapor deposition (PECVD) oxides, single crystal silicon membrane, and thermally grown oxide [55, 105–107].

28.5 Application, Grand Challenges, and Outlook

Degradable and transient devices have been envisioned to find application into three main fields: (i) medical implants, (ii) green environmental sensors, and (iii) security systems.

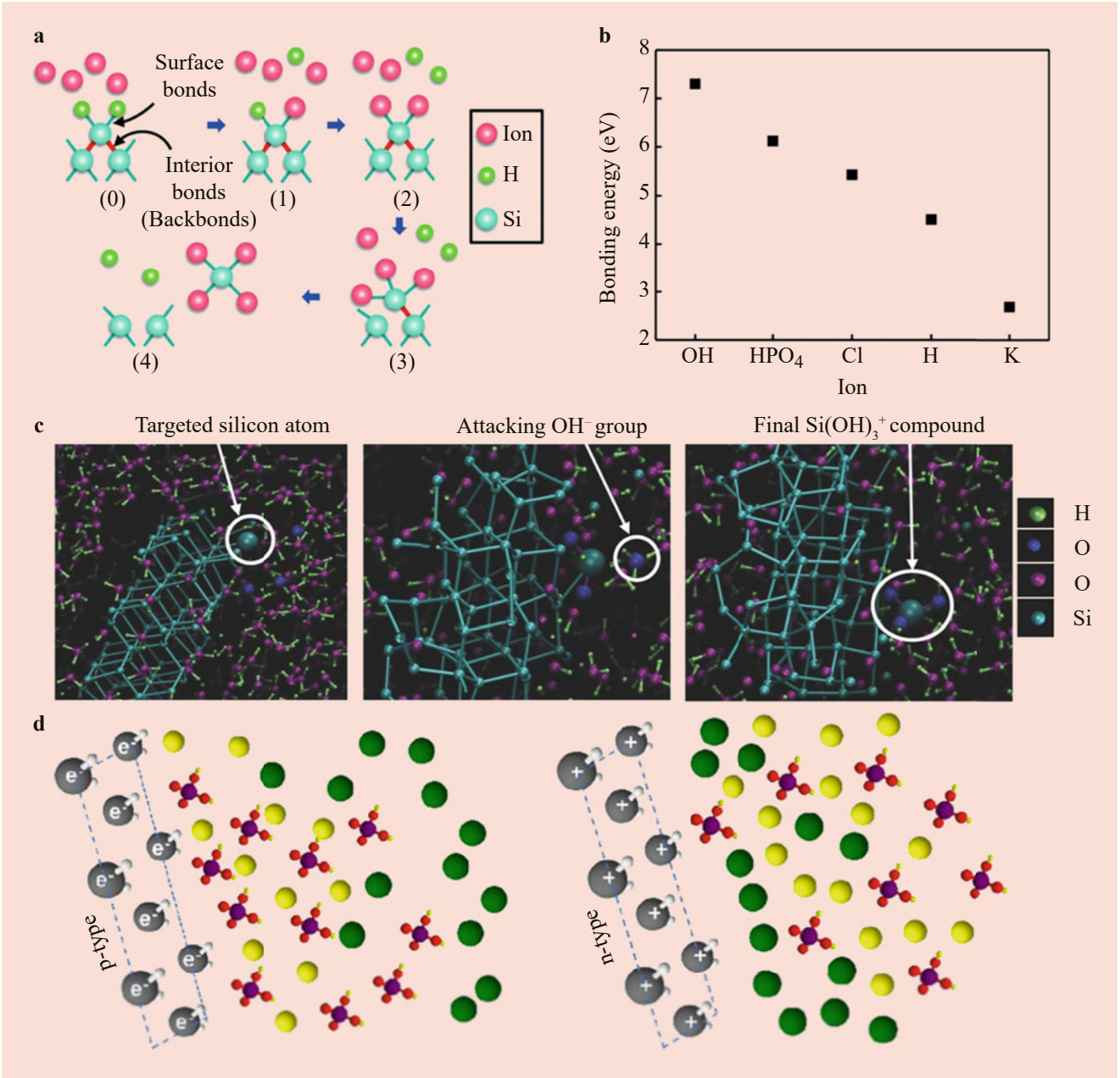

Fig. 28.6 Dissolution. Dissolution mechanisms for silicon. (**a**) Atomic configurations for each ion adsorption event in the dissolution process. (**b**) Strength of several ion-Si bonds. (**c**) Molecular dynamics images of silicon dissolution: (left) snapshot of the initiation of silicon dissociation; (middle) bonding of two OH^- groups to the targeted silicon atom; (right) bonding of the third OH^- group to the targeted silicon atom and generating $Si(OH)^{3+}$. ((**a**–**c**) Reproduced with permission. [98] Copyright 2015, John Wiley and Sons) (**d**) Schematic illustrations of different atomic configuration of each ion adsorption event for p-type (left) and n-type (right) silicon. (Reproduced with permission. [99] Copyright 2019, American Chemical Society)

Medical implants that can safely resorb in the body would be very beneficial in medical care scenarios that require the monitoring and medications of pathologies and diseases that are temporary and limited in time. A typical example consists of degradable drug release systems whose function is required only for a prescribed amount of time [59, 108]. Another example is a resorbable stent for coronary angioplasty [11, 42, 60]. Other devices may be envisioned in post-surgery treatments and care, i.e., heat delivery to accelerate healing processes. The reader would notice that such ideas are not new. However, they regained momentum, thanks to the developments in the construction of high-performance degradable electronics. The development of degradable high-performance circuits, wireless communication systems, powering devices, and actuators would generate a completely new class of medical implants. Of course, engineering efforts

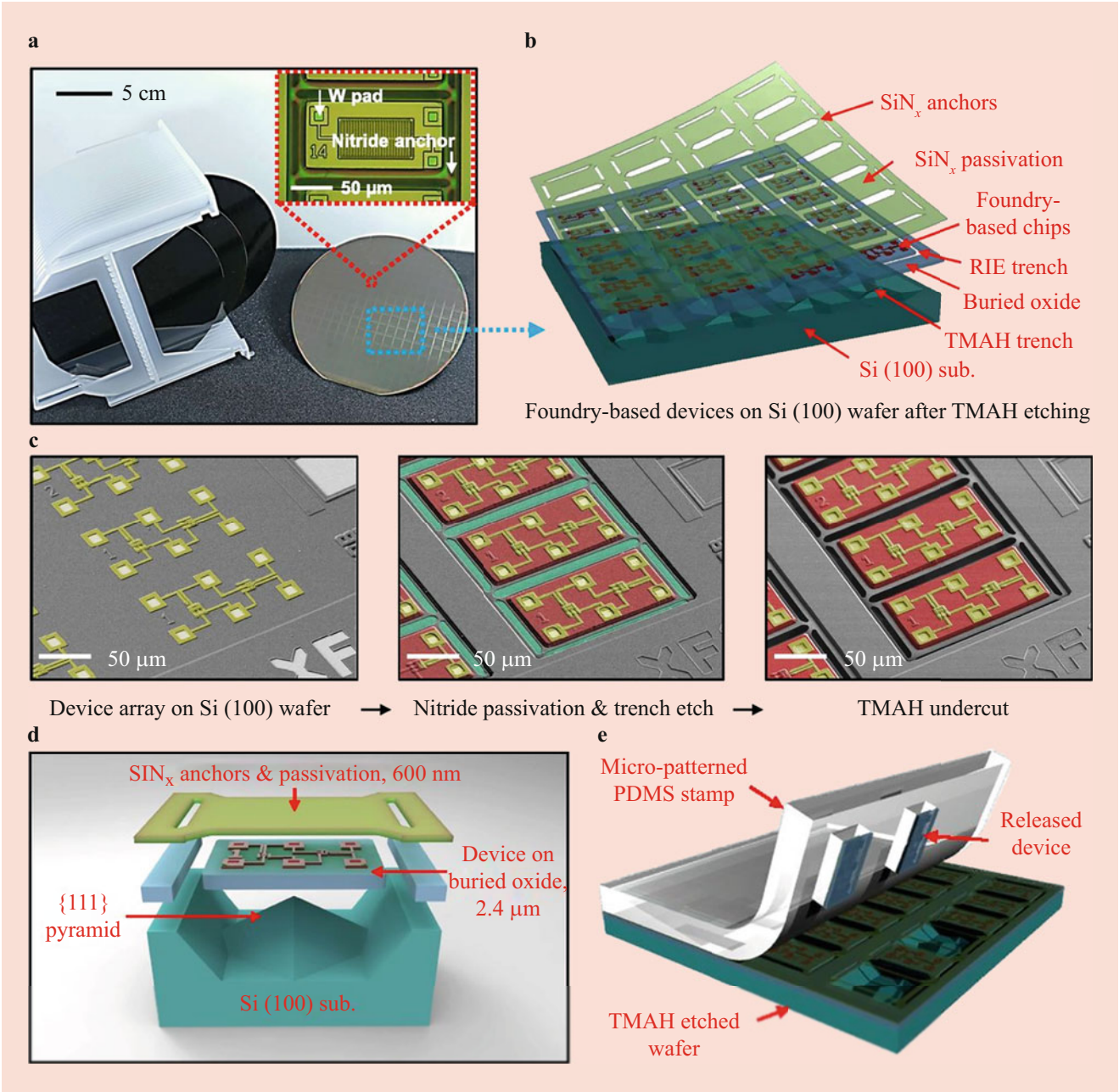

Fig. 28.7 Fabrication processes. (**a**–**c**) Device structure and wafer-scale release of foundry-based ultrathin silicon components. (**c**) SEM images of key processing steps for wafer-scale release. The individual frames correspond to the unprocessed wafer (left), the wafer after passivation and trench etching (center), and the wafer after TMAH undercut etching (right). (**d**) Schematic exploded view illustration of the device configuration of a unit cell after complete release. (**e**) Schematic illustration of the process for transfer printing with a PDMS stamp. ((**a**–**e**) Reproduced with permission. [36] Copyright 2017, National Academy of Sciences)

would need to be accompanied by more comprehensive studies of the effects on the health of the decomposition of the devices into their constituent materials and of their diffusion into the body.

Another picture that is very common in the recent engineering literature consists of realizing compostable sensors that can be deployed in the environment without any need to be retrieved and recycled. A longer-term view would even envision the fabrication of compostable printed circuit board and electronic packages to alleviate the problem of the disposal and recycling of the electronic waste. The current situation sees more than 50 million tons of waste from electrical and electronic equipment being produced per year worldwide. Developed countries have conventions, directives, and laws to regulate the disposal [109]. The European Commission has put in place two pieces of legislation: the di-

rective on waste electrical and electronic equipment (WEEE Directive) and the directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS Directive). As a result, today, European countries are able to recycle about 66% of their e-waste, but, they still deliver more than 10 million tons per year to incinerators or to the landfill, with the risk of leaching heavy metal in the ground water and with the emission of toxic fumes into the air [110]. Progress in the disposal has been hindered by the large palette of products available, where the variation in the materials and components makes e-waste one of the most complex waste streams [111]. The problem is further exacerbated by the presence of toxic and hazardous materials, such as lead and cadmium, which cannot be treated with conventional methods. The expense of proper disposal, hence, leads to the shipment of large amounts of e-waste to developing countries (i.e., China, India, Pakistan, Nigeria) where, despite the intents of national regulations, it is treated as general refuse with recovery of only a few materials of value. As dioxins, furans, and heavy metals are released, harm to the environment, workers, and area residents is inevitable.

The last application of transient devices is in the field of security systems. Here, the idea is to conceive systems that store sensitive information and that can disappear after a prescribed time or upon a remote command. In this contest, a major advancement consists in the implementation of mechanisms to trigger the dissolution process in response to external stimuli so as to ensure a spatially and timely controlled disintegration. One possible strategy to achieve such goal is to combine the degradable electronic components with microfluidic devices and functional/responsive materials. Ferromagnetic nanoparticles, UV, and thermal-responsive layers expand or rearrange their physical configuration to act as pumps or permeable membranes and release the liquid/etchants from 3D micro-reservoirs.

Transient or degradable or biodegradable electronics is an emerging technology that prospects the possibility to design new forms of devices and target applications which would be difficult to address with standard electronics. However, it inevitably faces challenges. Some of them are inherent to the nature of such technology: mechanical and functional reliability that are hard to design and predict and restricted palette of materials that may limit the performance of the devices. Here, the goal is to discuss the main ones and try to envision future research directions.

Restricted Palette of Materials The advancement in the study of materials that degrade in aqueous solution has been tremendous over the last 20 years. The list now includes organic and inorganic materials, and it is large enough to provide all key ingredients to build many optoelectronic devices. However, some of them could suffer of poor performance because of the restricted palette. Among the others, relevant examples include energy storage devices and passives for electronic circuits. Optical devices could also be challenging due to the limited choices of the semiconductors and their heterostructures.

Fabrication So far, the fabrication of degradable devices, especially those based on inorganic materials, have been achieved through multiple and tedious transfer steps from donor substrates/templates to the degradable ones. Recently, some research groups have started collaborating with industry and silicon foundries to establish transient-compatible processes. This is definitively an important step toward the realization of more complex and sophisticated devices and circuits on a large scale.

Dissolution Hard to Predict The control and prediction of the lifetime of the devices is probably the most challenging aspect of this technology. So far, the dissolution dynamics has been achieved through the design of the encapsulation layers and their thickness. Most of the time, such layers are constituted by polymers whose deposition and quality (uniformity, pinhole-free, etc.) are hard to control and reproduce. Some attempts have been also done to use higher-quality thin films that can be thermally grown or deposited by vacuum processes (PVD, ALD). However, thin film encapsulation remains challenging. Other strategies point toward the direction of combining responsive materials/devices with fluidic devices (reservoirs) that can be activated to trigger the dissolution at specific and desired point in time. Such approach could pave the way to military and security applications but would be probably even more challenging if the fluidic part should dissolve as well.

From Research Lab to Industry The technology is in its infancy, and most of the advancements have been achieved in university or research lab labs. In recent years more and more research groups have started publishing results about materials and new degradable devices. However, the involvement of industrial partners would be beneficial to both scale up the fabrication and to adopt some of the technologies/devices. Similarly, devices for biomedical applications would largely benefit from collaborations with clinicians and medical doctors both for a proper design and for in vivo tests.

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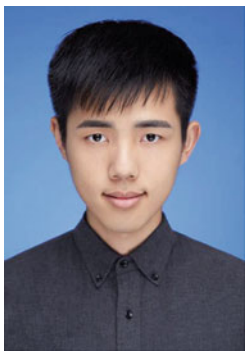

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Resistive-Switching Memories

29

Peng Huang, Yudi Zhao, and Jinfeng Kang

Contents

29.1 Introduction 1044

29.2 Physical Mechanism of Resistive Switching 1046
29.2.1 Ox-RRAM 1046
29.2.2 CBRAM 1049

29.3 Modeling and Simulation of Resistive-Switching Behaviors 1052
29.3.1 Ox-RRAM 1052
29.3.2 CBRAM 1061

29.4 Array Design and Optimization 1069
29.4.1 Crossbar Array 1069
29.4.2 Selector Devices for RRAM Array 1071
29.4.3 3D Integration 1073

29.5 Applications 1075
29.5.1 Embedded Memory 1075
29.5.2 Computing in Memory 1077
29.5.3 Brain-Inspired Computing 1082

29.6 Summary and Prospect 1086

References 1087

Abstract

In the past decades, resistive-switching random-access memory (RRAM) has been widely studied as one of the promising candidates for next-generation memory technologies. Recently, innovation research on the novel devices for new computing paradigms beyond von Neumann architecture is emerging with the rapid development of artificial intelligence (AI) technologies. With its natural features that can both store and process data, RRAM has been also extensively explored to implement for the new computing paradigms such as brain-inspired computing and in-memory computing.

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RRAM is a novel device that is based on resistive switching. It has a typical MIM structure where the resistive-switching layer is sandwiched between the top electrode (TE) and bottom electrode (BE). The resistive switching indicates that the device can be reversibly switched between high resistance state (HRS) and low resistance state (LRS). The resistive-switching process from HRS to LRS is called SET, and the reversible process from LRS to HRS is called as RESET. Two kinds of modes including unipolar and bipolar have been observed to switch RRAM. For a fresh RRAM, a so-called Forming process is usually required to achieve the reversible and repeated resistive-switching behaviors. Generally, the Forming voltage is much higher than the switching (SET and RESET) voltage. If the Forming voltage is close to the switching voltage, this RRAM is referred to as Forming-free device.

For the physical origins of resistive switching in RRAM, the filament effect has been widely accepted. In this viewpoint, the resistive switching between HRS and LRS is due to the formation and rupture of conductive filament paths inside the resistive-switching layer. According to the composition of the conductive filament (CF), RRAM can be further classified into two types: (1) oxygen vacancy-based RRAM (Ox-RRAM) and (2) metal ion-based RRAM that is also called as conductive-bridge random-access memory (CBRAM).

RRAM was initially proposed for the memory application as the next generation of nonvolatile memory candidate in the early 2000s. Especially, Samsung presented a paper at the International Electron Devices Meeting that demonstrated the highly scalable characteristics in NiO memory cells integrated with conventional complementary metal oxide semiconductor (CMOS) with a one-transistor–one-resistor (1T1R) device structure. That further intensified the research activity on RRAM. Up to now, significant technical advances have been achieved in the device performance and integration, including great scalability (<10 nm), fast speed (<1 ns), low operation

voltage (<1.5 V) and current (<1 μA), high endurance (>1012 cycles), and long retention (>10 years at room temperature). The 3D integration approaches were also proposed for the high density of RRAM integration. The testing memory chips more than 16 G-bits have been reported and demonstrated.

In 2008, HP group published a paper to establish the link between RRAM and "memristor," where the concept of "memristor" was proposed and defined by L. Chua in the 1970s. Later, RRAM or memristor was proposed and demonstrated to implement the stateful logic, in which Boolean logic states were operated and stored in resistance of RRAM. In 2012, a collaboration work from Stanford University and Peking University reported a RRAM-based electronic synapse with multilevel states (>400 states) and ultra-low spiking energy (<1 pJ/per spiking) and then further demonstrated a 3D integration approach to achieve both high uniformity and low spiking energy in 2014. This strongly stimulates the RRAM research activities that extend RRAM to much wider areas beyond memory. Especially accompanying with the development of AI, the new computing paradigms beyond von Neumann such as brain-inspired computing are highly desired to overcome the bottleneck of so-called memory wall from the traditional von Neumann architecture. Research activity has been primarily driven by the search for ideal neuromorphic devices. RRAM was paid much more attention due to the featured functions of computing in memory, which is beneficial for the brain-inspired computing systems. More recently, while a lot of research efforts still remain focused on the device level, the demonstrations of the arrays in circuit/system level are increasingly common. Various RRAM array-based chips for both memory and brain-inspired computing applications were reported.

In this chapter, we will review the latest advancements in RRAM. Firstly, the physical mechanism on resistive-switching characteristics of both Ox-RRAM and CBRAM are discussed in Sect. 29.2. Then, the physics-based models and simulation methods are presented in Sect. 29.3. In Sect. 29.4, the array design and optimization technologies are addressed and discussed. The system applications of RRAM in emerged memory and novel computing paradigms for brain-inspired neural network are explored in Sect. 29.5. Finally, the prospect of future technological trend is highlighted in Sect. 29.6.

Keywords

Resistive switching · RRAM · Conductive filament · OxRAM · CBRAM · Nonvolatile logic · Neural network

29.1 Introduction

In the past decades, resistive-switching random-access memory (RRAM) has been widely studied as one of the promising candidates for next-generation memory technologies [1–5]. Recently, innovation research on the novel devices for new computing paradigms beyond von Neumann architecture is emerging with the rapid development of artificial intelligence (AI) technologies. With its natural features that can both store and process data, RRAM has been also extensively explored to implement for the new computing paradigms such as brain-inspired computing and in-memory computing [6–10].

RRAM is a novel device that is based on resistive switching. The first report on resistive switching can be traced back to the 1960s. Hickmott published the first paper on electric field-induced hysteretic current-voltage (I-V) characteristics in thin anodic oxide films with metal-insulator-metal (MIM) structure [11]. The recent revival of interest in resistive switching began in the late 1990s originated from a report of resistive switching in $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO) by Asamitsu et al. [12]. Since that, resistive-switching (RS) phenomena have subsequently been reported in a wide variety of materials [1–7, 13–17] including metal oxides, nitrides, selenides, sulfides, and organic and low-dimensional materials. Meanwhile, the switching mechanisms [15–20] and the possible applications in the next generation of storage and computing started to be explored [21–29]. All these extensive researches were well reviewed in the published review articles [1–9].

RRAM has a typical MIM structure as shown in Fig. 29.1a, where the resistive-switching layer is sandwiched between the top electrode (TE) and bottom electrode (BE). The resistive switching indicates that the device can be reversibly switched between high resistance state (HRS) and low resistance state (LRS). The resistive-switching process from HRS to LRS is called SET, and the reversible process from LRS to HRS is called RESET. Two kinds of modes including unipolar and bipolar have been observed to switch RRAM as shown in Fig. 29.1b, c. For the unipolar switching, the same polarity of SET and RESET voltages can be used to switch the devices between HRS and LRS. In contrast to this, bipolar switching must use a pair of opposite polarity voltages to switch the device. For example, when we use a positive SET voltage to switch RRAM from HRS to LRS, a negative RESET voltage is necessary to switch the device from LRS to HRS. For a fresh RRAM, a so-called Forming process is usually required to achieve the reversible and repeated resistive-switching behaviors. Generally, the Forming voltage is much higher than the switching (SET and RESET) voltage. If the Forming voltage is close to the switching voltage, this RRAM is referred to as Forming-free device.

For the physical origins of resistive switching in RRAM, the filament effect has been widely accepted. In this view-

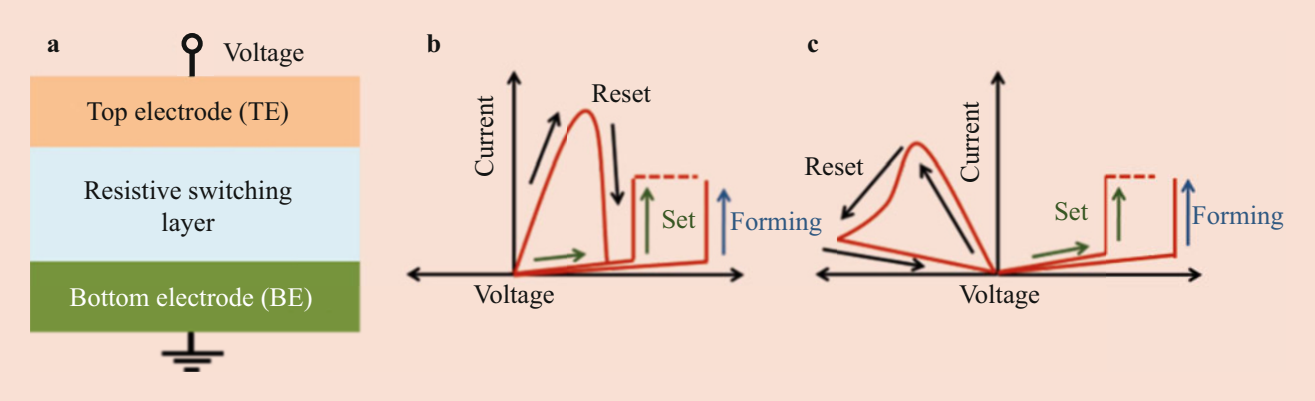


Fig. 29.1 (**a**) The MIM structure of RRAM device, (**b**) unipolar and (**c**) bipolar switching type depending on the voltage polarity

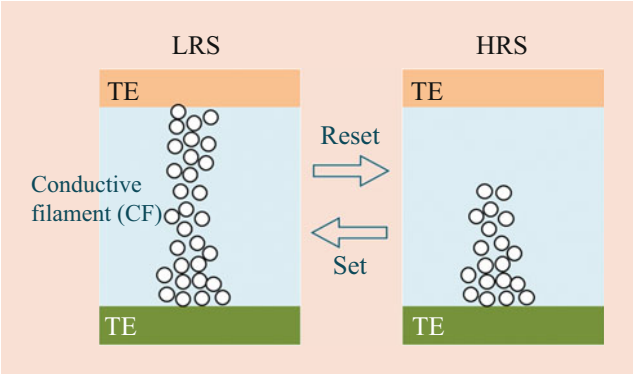


Fig. 29.2 The schematic view for the formation and rupture of a conductive filament (CF) path

point, the resistive switching between HRS and LRS is due to the formation and rupture of conductive filament paths inside the resistive-switching layer as shown in Fig. 29.2.

According to the composition of the conductive filament (CF), RRAM can be further classified into two types: (1) oxygen vacancy-based RRAM (Ox-RRAM) and (2) metal ion-based RRAM that is also called as conductive-bridge random-access memory (CBRAM).

RRAM was initially proposed for the memory application as the next generation of nonvolatile memory candidate in the early 2000s. Especially, Samsung presented a paper [30] at the International Electron Devices Meeting that demonstrated the highly scalable characteristics in NiO memory cells integrated with conventional complementary metal oxide semiconductor (CMOS) with a one-transistor–one-resistor (1T1R) device structure. That further intensified the research activity on RRAM. Up to now, significant technical advances have been achieved in the device performance and integration [31–38], including great scalability (<10 nm), fast speed (<1 ns), low operation voltage (<1.5 V) and current (<1 μA), high endurance (>10^{12} cycles), and long retention (>10 years at room temperature). The 3D integration approaches were also proposed for the high density of RRAM integration [39–41]. The testing memory chips more than 16 G-bits have been reported and demonstrated [42, 43].

In 2008, HP group published a paper [44] to establish the link between RRAM and "memristor," where the concept of "memristor" was proposed and defined by L. Chua in the 1970s [45]. Later, RRAM or memristor was proposed and demonstrated to implement the stateful logic [21], in which Boolean logic states were operated and stored in resistance of RRAM. In 2012, a collaboration work from Stanford University and Peking University reported a RRAM-based electronic synapse with multilevel states (>400 states) and ultra-low spiking energy (<1 pJ/per spiking) [22] and then further demonstrated a 3D integration approach to achieve both high uniformity and low spiking energy in 2014 [23]. This strongly stimulates the RRAM research activities that extend RRAM to much wider areas beyond memory. Especially accompanying with the development of AI, the new computing paradigms beyond von Neumann such as brain-inspired computing are highly desired to overcome the bottleneck of so-called memory wall from the traditional von Neumann architecture. Research activity has been primarily driven by the search for ideal neuromorphic devices. RRAM was paid much more attention due to the featured functions of computing in memory as demonstrated in Ref. [21–28], which is beneficial for the brain-inspired computing systems. More recently, while a lot of research efforts still remain focused on the device level, the demonstrations of the arrays in circuit/system level are increasingly common. Various RRAM array-based chips for both memory and brain-inspired computing applications were reported [46–50].

In this chapter, we will review the latest advancements in RRAM. Firstly, the physical mechanism on resistive-switching characteristics of both Ox-RRAM and CBRAM are discussed in Sect. 29.2. Then, the physics-based models and simulation methods are presented in Sect. 29.3. In Sect. 29.4, the array design and optimization technologies are addressed and discussed. The system applications of RRAM in

emerged memory and novel computing paradigms for brain-inspired neural network are explored in Sect. 29.5. Finally, the prospect of future technological trend is highlighted in Sect. 29.6.

29.2 Physical Mechanism of Resistive Switching

Since the early work in the 2000s, RRAM switching mechanisms have been attributed to the filamentary modification of conduction properties. It was possible to reveal the resistive-switching mechanism by several different techniques, including conductive atomic force microscopy (CAFM) measurements [51], area dependence of the LRS resistance [30], infrared thermal imaging of the device [52], and in situ microscopic imaging of the device during switching by transmission electron microscopy (TEM) [53]. Based on the experimental techniques, a large variety of physical mechanisms have been proposed leading to the resistive-switching effects such as the ion migration, charge trapping/de-trapping, thermal reaction, insulator-to-metal transition, charge transfer, and so on [4]. In this chapter, we will discuss the ion-based resistive-switching mechanism in detail, which can be further distinguished into two types. One type is based on the oxygen vacancies in the metal oxides, which is referred to as oxide-based RRAM (Ox-RRAM) [3, 17]. Both bipolar [54–56] and unipolar [57, 58] switching modes have been found in this kind of RRAM, and J. Kang et al. [17, 59] have proposed a unified mechanism for the bipolar and the unipolar modes, in which resistive switching is triggered by the generation and recombination of oxygen vacancies in the metal oxides. Another RRAM type is based on the bipolar electrochemical metallization mechanism, and the corresponding device is called the conductive-bridge random-access memory (CBRAM) or electrochemical metallization cell (ECM) [53]. The resistive switching of CBRAM relies on the active metal Ag or Cu penetrating (or dissolving) in the ion conducting layer which is oxide or chalcogenide to form (or rupture) a conducting path.

In this section, we will address the resistive-switching mechanisms of Ox-RRAM and CBRAM, respectively.

29.2.1 Ox-RRAM

We begin with the typical bipolar Ox-RRAM with single switching layer. The microscopic physical processes of switching in an Ox-RRAM are schematically shown in Fig. 29.3 [60]. During the SET process, the generation of oxygen vacancies (V_O) and the migration of dissociated oxygen ions (O^{2-}) to the top electrode cause the formation of CF connecting the two electrodes, which switches the cell from HRS to LRS. To specify, the excited state of ${V_O}^{2+}$ is firstly formed accompanying the generation of ${V_O}^{2+}$ and O^{2-}, and then the excited ${V_O}^{2+}$ state is relaxed to a stable V_O state. The generation probability of V_O under electric field is governed by [61].

$$P_g = f \cdot \exp\left(-\frac{E_a - \Delta\varphi}{k_B T}\right) \tag{29.1}$$

where f is the vibration frequency of oxygen atom, E_a is the average active energy of V_O, $\Delta\varphi$ is the barrier height reduction induced by electric field, and T is the local temperature. The hopping probability of the dissociated O^{2-} in the oxide layer can be described by [62].

$$P_h = f \cdot \exp\left(-\frac{E_h - \Delta\varphi}{k_B T}\right) \tag{29.2}$$

where E_h is the hopping barrier of O^{2-}.

During RESET process, firstly, the V_O state is excited to the ${V_O}^{2+}$ state, and then the O^{2-} is released by the top electrode and hop to the nearby ${V_O}^{2+}$ site and then recombine with ${V_O}^{2+}$, leading to the rupture of the CF. The probability of recombination between electron-depleted ${V_O}^{2+}$ and O^{2-} follows the equation [61].

$$P_r = f \cdot \exp\left(-\frac{\Delta E_r}{k_B T}\right) \tag{29.3}$$

where ΔE_r is the relaxation energy of recombination. The top electrode acts as an oxygen reservoir that can release O^{2-} with the probability governed by the following equation [62]:

$$P_m = f \cdot \exp\left(-\frac{E_i - \Delta\varphi}{k_B T}\right) \tag{29.4}$$

where E_i is the energy barrier of the electrode release O^{2-}.

The device uniformity and reliability of Ox-RRAM can be improved by adopting a bilayered electrolyte structure. A typical example is the widely used Ta_2O_5/TaO_X bilayer resistive-switching stack to improve the endurance characteristics [16, 63]. In the bilayer Ta_2O_5/TaO_X structure, the oxygen-deficient TaO_X layer, instead of TiN electrode in the HfO_X-RRAM, acts as the oxygen reservoir. The O^{2-} transportation in the Ta_2O_5/TaO_X stack is shown in Fig. 29.4. During SET process, the generated dissociative O^{2-} hop in Ta_2O_5 layer, and when they migrate to the Ta_2O_5/TaO_X interface, the O^{2-} can be absorbed by TaO_X layer. Within the TaO_X layer, some of the absorbed O^{2-} will continue hopping under the effect of electric field, while others get involved in the redox reaction with the oxygen-deficient TaO_X and then restored as lattice oxygen. During RESET process, the lattice oxygen in TaO_X will be thermally activated and released as

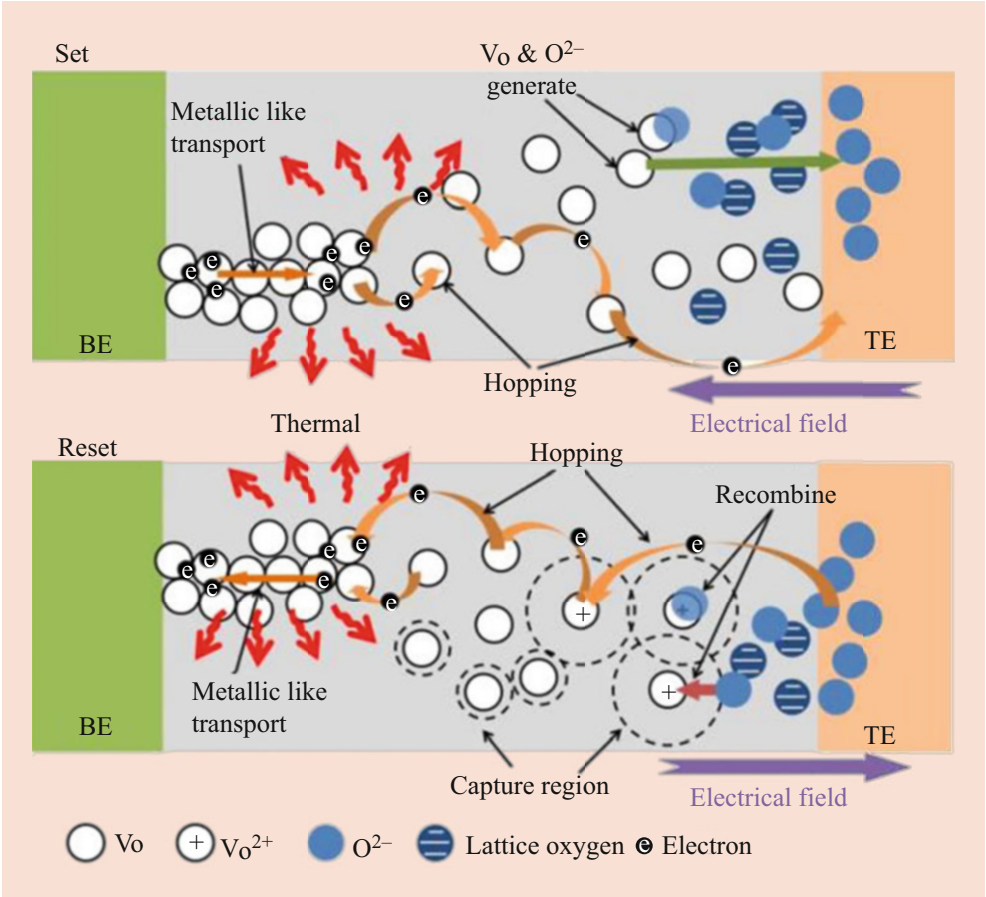


Fig. 29.3 Schematic physical processes of resistive switching in Ox-RRAM, including the generation of oxygen vacancies (V_O), hopping of oxygen ions (O^{2-}), electrode absorbing and releasing O^{2-}, recombination between V_O and O^{2-}, and increase of local temperature. (Reprinted from [60])

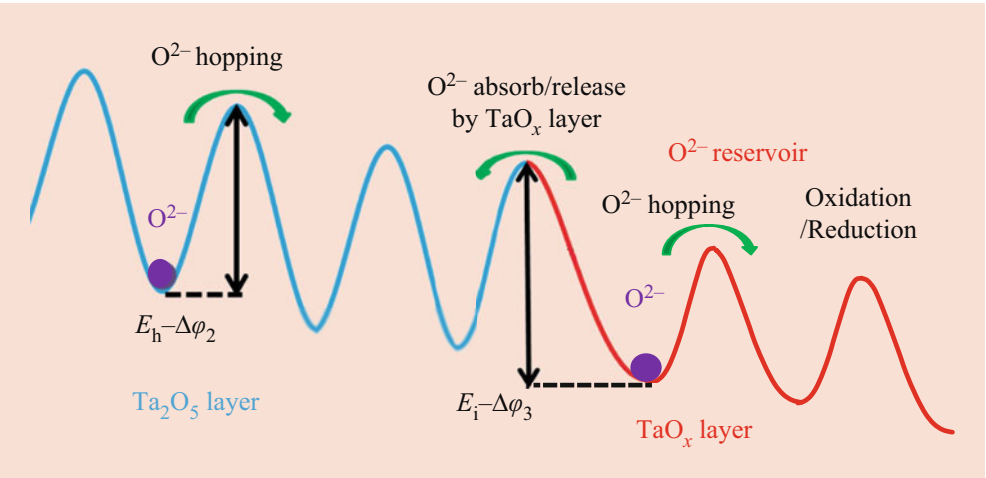


Fig. 29.4 Schematic of O^{2-} transportation in the Ta_2O_5/TaO_X stack

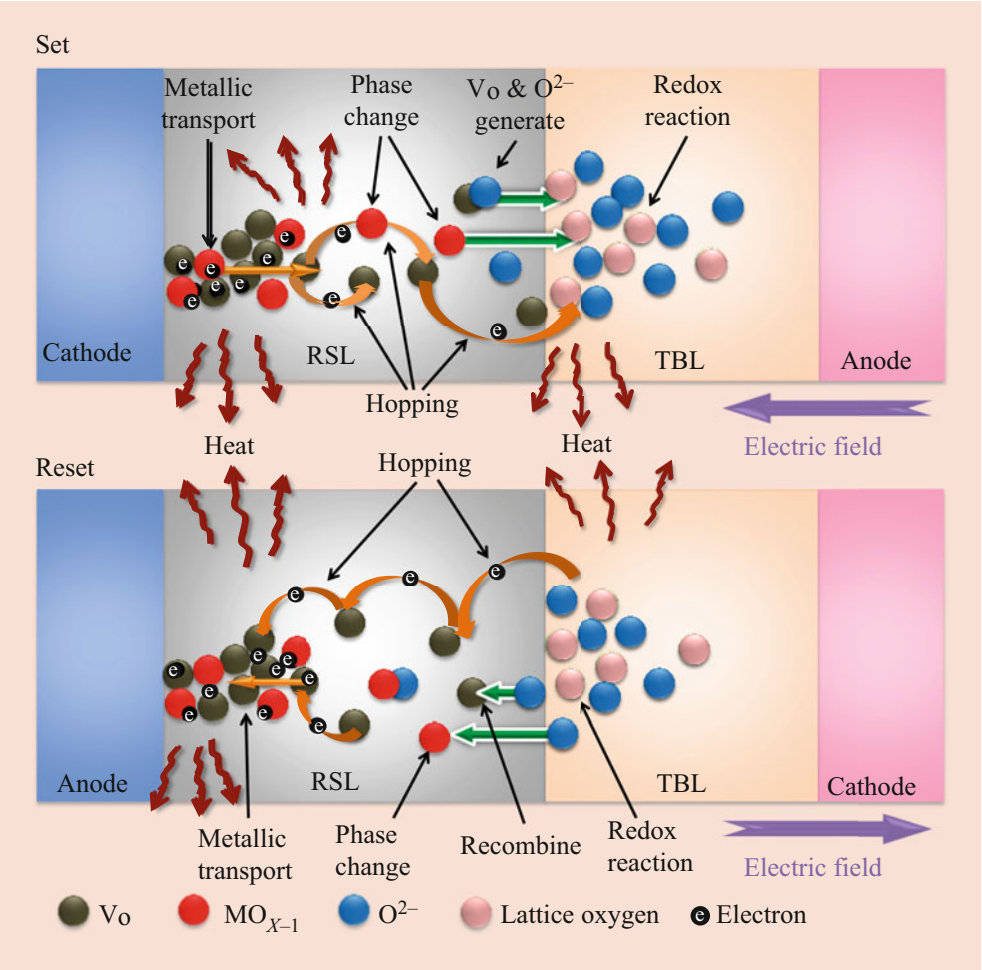


Fig. 29.5 Schematic resistive-switching model in bilayer Ta_2O_5/TaO_X RRAM. The two layers are the resistive-switching layer composed of Ta_2O_5 and TaO_X base layer. (Reprinted from [63])

dissociative O^{2-} which will migrate back to Ta_2O_5 layer to recombine with the oxygen vacancies [63].

Y. Zhao et al. have conducted ab initio calculations in the Ta-O system and found that besides the oxygen vacancy generation/recombination processes, phase transition also takes place in a Ta_2O_5-RRAM device [63]. The phase transition process takes place between Ta_2O_5 and TaO_2, which can be described by

$$Ta_2O_5 + 2e^- \leftrightarrow 2TaO_2 + O^{2-} \tag{29.5}$$

According to the ab initio calculation results, the Ta_2O_5 are semi-conductive, while the TaO_2 are metallic. The probability of the phase transition from Ta_2O_5 to TaO_2 can be described by

$$P_a = f \cdot \exp\left(-\frac{E_a}{k_B T}\right) \tag{29.6}$$

where E_a is the activation energy of Ta_2O_5 changing to TaO_2. It is a thermally controlled process. The reverse phase transition from TaO_2 to Ta_2O_5 can be described similarly. Hence the resistive switching in a bilayer Ta_2O_5/TaO_X RRAM can be depicted in Fig. 29.5. By applying a negative bias on the left electrode in Fig. 29.5, V_O is generated by ionizing O^{2-} from the Ta_2O_5 lattice. As the current increases, the phase transition between Ta_2O_5 and TaO_2 takes place, and a CF consisting of V_O and TaO_2 connects top electrode and the TaO_X base layer, switching the device from HRS to LRS. With positive bias on the left electrode, O^{2-} in the TaO_X base layer will be activated and migrate to the Ta_2O_5 layer to recombine with V_O or react with TaO_2, leading the rupture of CF, switching the device from LRS to HRS.

Next, we will discuss about the unipolar mode Ox-RRAM. The resistive-switching mechanism of unipolar Ox-RRAM is similar to the bipolar mode as shown in Fig. 29.6. It should be noted that the difference with bipolar is the storing and releasing modes of the dissociated O^{2-}. In the unipolar Ox-RRAM,

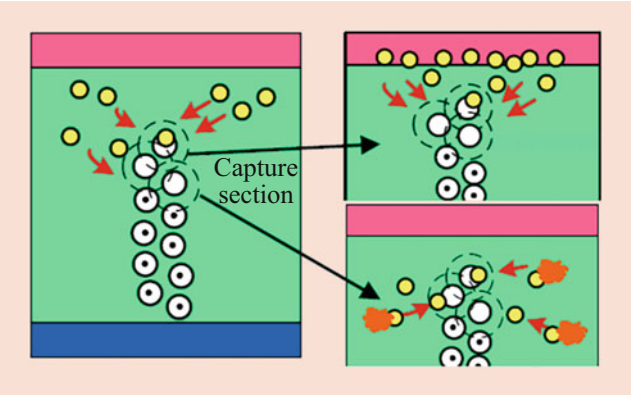


Fig. 29.6 Schematic RESET comparison between the unipolar and bipolar Ox-RRAM. For bipolar RESET, the O^{2-} is released by the O^{2-} reservoir and drifts from the interface to recombine with V_O. For unipolar RESET, the O^{2-} is released by Joule heating-induced thermal decomposition of the easily reduced oxide clusters or grains in the capture section region. (Reprinted from [59])

the dissociated O^{2-} will be absorbed and released from the easily reduced oxide clusters which are closely neighbored with the V_O-rich CF. In more details, several different phases of oxide clusters co-exist in the resistive layer [59]. One is the oxygen-rich phase. The oxygen-rich clusters can release O^{2-} mainly due to the thermal decomposition instead of electric field driving when the local temperature reaches a specific threshold [59]. The thermally released O^{2-} will then recombine with the V_O and consequently rupture the CF during RESET process. During SET process, the generation of V_O is similar with bipolar Ox-RRAM, but the dissociated O^{2-} will be absorbed by the nearby oxygen-rich phase rather than the anode.

For both bipolar and unipolar Ox-RRAM, the current conduction mechanism can be modeled as follows. For the CF region, the electron transport is metallic and the conductivity decreases with increasing temperature according to Arrhenius law [64], which can be described by

$$\sigma = \sigma_0 \exp\left(\frac{E_{AC}}{k_B T}\right) \tag{29.7}$$

where E_{AC} is the activation energy for conduction and σ_0 is the Arrhenius pre-exponential factor for conductivity. For the region without CF, the electron transport among the dispersive V_O is hopping, and the hopping rate between two V_O can be calculated by the Mott hopping model [65], which is

$$W_{m\to n} = f_{ph} \exp\left(-\frac{2\alpha R_{mn} + E_{mn}}{k_B T}\right) \tag{29.8}$$

where the f_{ph} is the vibration frequency of electron, R_{mn} is the distance between two V_O, α is the attenuation length of the electron wave function, and E_{mn} is the change of barrier height induced by the applied external field.

The local temperature plays an important role during the switching processes. The temperature distribution can be obtained by solving the Fourier heat-flow equation [66], which is

$$C\frac{\partial T}{\partial t} = \nabla (k\nabla T) + Q \tag{29.9}$$

where C is the specific heat per unit volume of the oxide layer, k is the thermal conductivity, and Q is the sum of multiple heat sources due to the inelastic electron-phonon.

29

29.2.2 CBRAM

The formation and rupture of CF are widely acknowledged as the resistive-switching effect in RRAM. Thus, understanding the dynamics of CF evolution is important to continue device research. The direct observation of CF in Ox-RRAM is difficult; however, in CBRAM, the formation of CF has been visualized in several device systems, which not only provide the origin of resistance change during switching operations but also reveal the CF evolution dynamics such as the CF geometry and CF growth direction. Figure 29.7 shows an example of CF growing from the inert electrode (IE) to the active electrode (AE) which is experimentally demonstrated by Y. Yang et al. [53]. Figure 29.7a shows the TEM image of an as-fabricated device using sputtered SiO_2 as the dielectric layer. To switch the device, a constant voltage is applied to Ag electrode. Image in Fig. 29.7b taken after the Forming process clearly revealed a well-defined CF with a typical conical shape. Detailed TEM study verified that the CFs are composed of Ag. The thinnest part of the CF is close to IE interface, with a much wider base formed near the AE. By applying a negative voltage on AE, all CFs, whether completely formed or partially formed, are found to first break at the filament/IE interface as shown in Fig. 29.7c. The dissolved parts of CF are reversely deposited on AE. The current-time characteristics during SET and RESET are shown in Fig. 29.7d, e, respectively.

However, different CF growth directions have been observed by experiments. H. Sun et al. observed the CF growth from AE to IE by SEM technique as shown in Fig. 29.8 [67]. In the Ag/SiO_2/Pt device, initially the gap between electrodes of fresh device is clean as shown in Fig. 29.8a. After constant voltage stress of 30 V with 10 μA compliance current applied on Ag electrode for 10 s, some Ag nanoparticles are generated near Ag electrode, as shown in Fig. 29.8b. After 150 s, more Ag nanoparticles are formed around Ag electrode, and

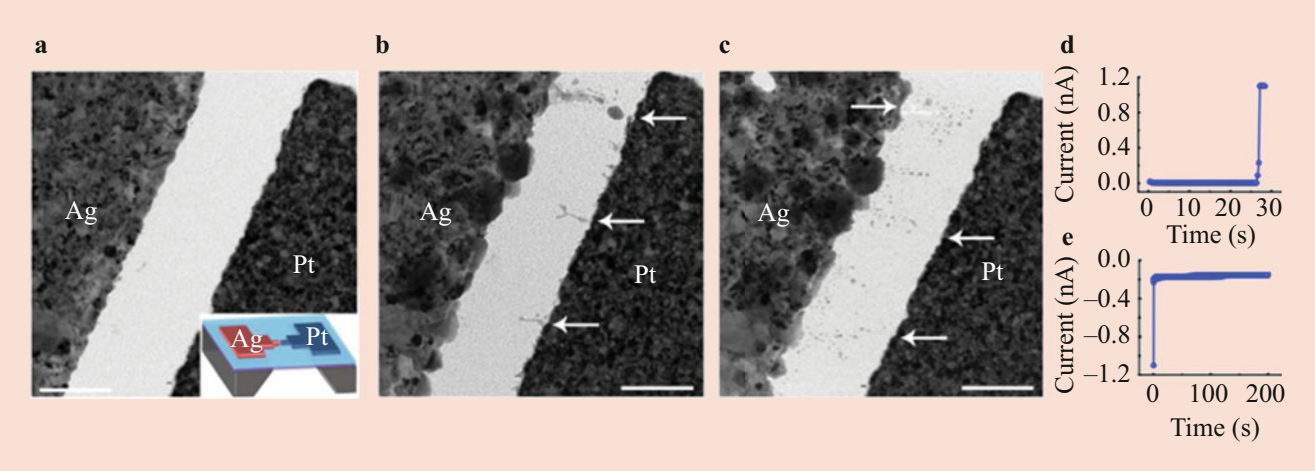


Fig. 29.7 TEM observation of conducting filament dynamics in SiO_2-based RRAM. (**a**) TEM image of an as-fabricated device, (**b**) TEM image of the same device after Forming process. Scale bar, 200 nm, (**c**) TEM image of the same device after RESET process, (**d**) corresponding I-t characteristics during Forming, (**e**) I-t characteristics during RESET. (Reprinted from [53])

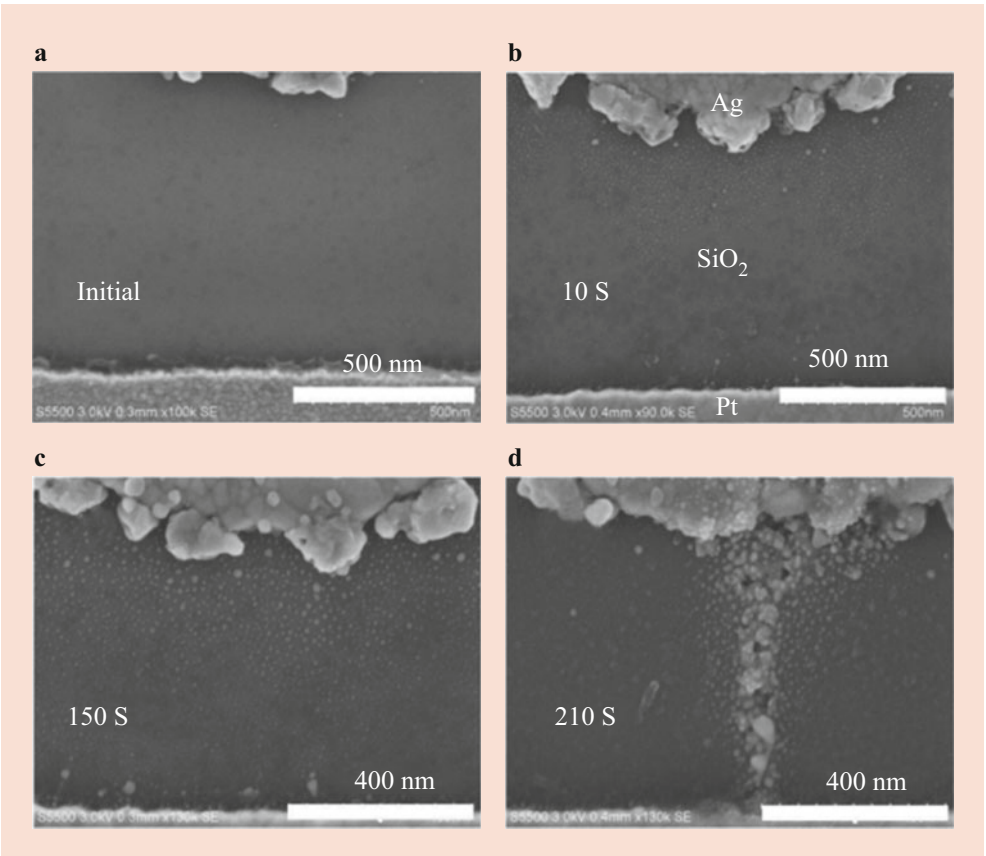


Fig. 29.8 SEM images capturing the dynamic CF growth in the Ag/SiO_2/Pt device. (**a**) Fresh device, (**b**)–(**d**) device after 10 s, 150 s, and 210 s under a 30 V constant voltage stress with 10 μA compliance current, respectively. (Reprinted from [67])

the nanoparticle chain extends toward Pt electrode, as shown in Fig. 29.8c. Finally, a continuous Ag nanoparticle chain is formed, and the device current reaches the compliance current due to the formation of Ag CF between two electrodes, as shown in Fig. 29.8d. The results clearly show that the initial Ag nanoparticle is firstly formed near the AE and then gradually extends to IE.

Based on the experimental observations, the resistive-switching mechanism in CBRAM is demonstrated as follows. Figure 29.9 shows the microscopic behaviors and

the correlated physical effects in CBRAM during resistive switching [68]. Here, the example of CF growth from IE to AE is demonstrated, while in the case of the other growth direction, the physical processes are likewise but their differences will be explained afterward. Generally, the following three physical steps would take place during resistive switching. Firstly, under the electric field of the applied voltage, the metal atoms from AE or CF may have the chance to be oxidized into cations, which can be described by

$$M \rightarrow {M_{\mathrm{ad}}}^{\mathrm{n+}} + ne^{-} \rightarrow {M_{\mathrm{ely}}}^{\mathrm{n+}} \tag{29.10}$$

where M represents the metal atoms, ${M_{\mathrm{ad}}}^{\mathrm{n+}}$ denotes the adsorbed cations on the surface of the CF or active electrode, and ${M_{\mathrm{ely}}}^{\mathrm{n+}}$ is the dissociative cations in the electrolyte. The oxidation probability of metal into cations can be described as [61].

$$P_{\mathrm{ox}} = f \cdot \exp\left(-\frac{E_{\mathrm{ox}} - \Delta\varphi}{k_{\mathrm{B}}T}\right) \tag{29.11}$$

where f is the vibration frequency of electrons, E_{ox} is the activation energy of oxidation, T is the local temperature, and $\Delta\varphi$ is the barrier height reduction induced by electric field.

After oxidation, the cations hop in the vacancy or interstitial sites of the electrolyte under electric field, with the probability of [62].

$$P_{\mathrm{h}} = f \cdot \exp\left(-\frac{E_{\mathrm{h}} - \Delta\varphi}{k_{\mathrm{B}}T}\right) \tag{29.12}$$

where E_{h} is the hopping barrier. Then when the cations collide with the electrons, the cations have the possibility to be reduced into metal atoms, which can be described by

$$M^{\mathrm{n+}} + ne^{-} \rightarrow M \tag{29.13}$$

The corresponding reduction probability is [61].

$$P_{\mathrm{red}} = f \cdot \exp\left(-\frac{E_{\mathrm{red}} - \Delta\varphi}{k_{\mathrm{B}}T}\right) \tag{29.14}$$

where E_{red} is the activation barrier of reduction. With the reduced atoms accumulated near IE, the atoms take nucleation reactions to form new nuclei on IE or within the electrolyte, depending on the particular material and experimental conditions. With application of an overpotential η_{nuc} on the atom, the Gibbs energy ΔG to form a cluster is a function of the atom number N and reaches its maximum for a critical particle number of [69].

$$N_{\mathrm{c}} = -\left(\frac{2\gamma a}{3ze_0\eta_{\mathrm{nuc}}}\right)^3 \tag{29.15}$$

where a is a constant depending on the cluster shape and the particle density and γ is the surface energy per unit area. The nucleation energy for a cluster with atom number N_{c} is

$$\Delta G_{\mathrm{c}} = \frac{4(\gamma a)^3}{27(ze_0\eta)^2} \tag{29.16}$$

Clusters with a number of particles smaller than N_{c} tend to dissolve, while larger clusters tend to grow further.

Based on these physical effects, the resistive-switching processes in CBRAM are shown in Fig. 29.9. During Forming or SET process, the positive bias is applied on AE, and the metal atoms on the surface of AE are activated into cations. Note that the oxidation barrier E_{ox} has different values according to the atom location on the AE surface. In the 2D example in Fig. 29.9, three different atom sites are considered and referred to as adatom, step, and vacancy sites. The corresponding oxidation barriers follow $E_{\mathrm{ox}}(1) < E_{\mathrm{ox}}(2) < E_{\mathrm{ox}}(3)$, where $E_{\mathrm{ox}}(1)$ is the oxidation barrier of atom in the adatom site, $E_{\mathrm{ox}}(2)$ is the barrier of step site, and $E_{\mathrm{ox}}(3)$ is the barrier of the vacancy site [65]. After oxidation, the cations migrate through electrolyte toward IE under electric field and get reduced near IE. Similar with the oxidation process, the reduction barriers also depend on the different locations of the cation being reduced. As the reduced atoms accumulate near IE, the filament gradually extends to the AE and finally forms a conduction path within the electrolyte. The device is then switched from HRS to LRS. During the RESET process as shown in Fig. 29.9b, negative bias is applied on AE, and the metal atoms in the CF are activated and migrated toward AE, finally redeposited near AE. The absence of atoms in the CF leads to the filament rupture, switching the cell back to HRS.

During resistive switching, the electrons are transferred at the metal/insulator interfaces due to the electrochemical reactions including the oxidation and reduction processes, and the electron transfer reaction can be mathematically described by the Butler-Volmer equation [70].

$$J_{\mathrm{et}} = j_{0,\mathrm{et}}\left(\exp\left(\frac{(1-\alpha)\,ze}{k_{\mathrm{B}}T}\eta_{\mathrm{et}}\right) - \exp\left(-\frac{\alpha ze}{k_{\mathrm{B}}T}\eta_{\mathrm{et}}\right)\right) \tag{29.17}$$

which exponentially relies on the electron transfer overpotential η_{et}. In the equation, z is the charge number, α is the charge transfer coefficient, and $j_{0,\mathrm{et}}$ is the exchange current density. The first and the second exponential terms describe the oxidation and the reduction processes, respectively. The cation transport within the electrolyte layer and the corresponding current density can be calculated with the Mott-Gurney law [70].

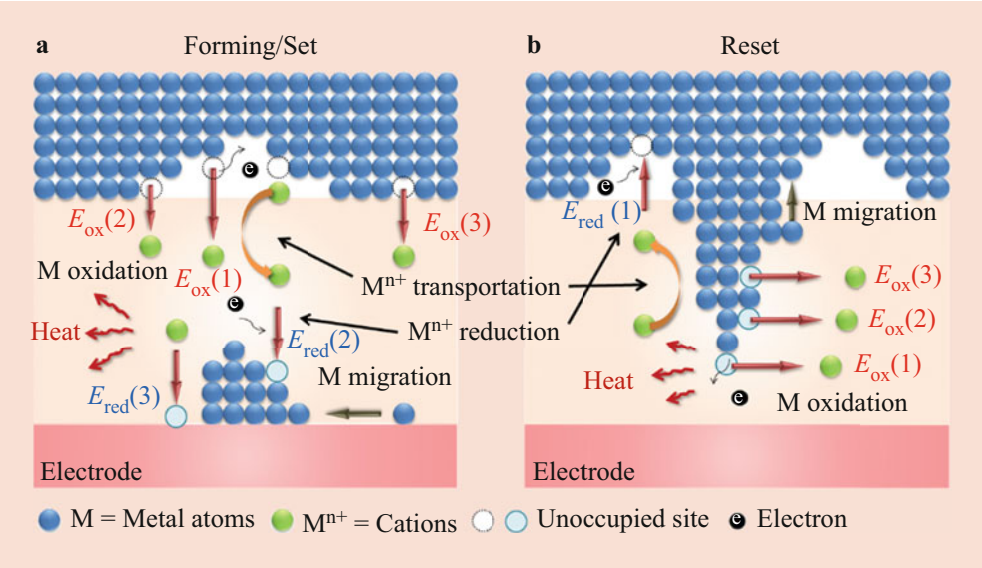


Fig. 29.9 The microscopic behaviors and the correlated physical effects in CBRAM during resistive switching. (Reprinted from [68])

$$J_{\text{hop}} = 2zecaf \exp\left(-\frac{E_{\text{h}}}{k_{\text{B}}T}\right) \sinh\left(\frac{aze}{2k_{\text{B}}T}E\right) \qquad (29.18)$$

where a is the mean cation hopping distance, E_{h} is the hopping barrier height, c is the cation concentration, and E is the applied electric field.

Under the same theoretical framework as shown in Fig. 29.9, Y. C. Yang et al. investigated the impacts of material parameters on the filament growth dynamics to explain the different filament growth modes observed experimentally [71]. According to Yang, the filament growth dynamics may fall into four different regimes depending on the kinetic factors based on the same theoretical framework as shown in Fig. 29.10. When the cation mobility μ and the redox rate Γ^{i} are high and homogeneous (case a), the cations can reach IE without agglomerating, thus avoiding nucleation within the insulating film so filament growth initiates from IE, and high Γ^{i} induced large amount of cation supply which leads to an inverted cone-shaped CF. Such CF growth dynamics are frequently observed in the conventional CBRAM in which electrolyte materials have high cation mobility. In contrast, in the case of low μ and low Γ^{i} (case b), the cations pile up and reach the critical nucleation conditions inside the dielectric, and further CF growth is fulfilled by cluster displacement. This case corresponds to electrolyte materials with very low cation mobility. If the cation mobility is low while the redox rates are high (case c), nucleation can occur inside the electrolyte, while large amounts of atoms can be deposited onto the cathode sides. This process is repeated thus again leading to an effective forward growth toward IE. Finally, if the cation mobility is high and the redox rates are low (case d), nucleation only occurs at IE, but the limited cation supply means reduction predominately occurs at the edges with high field strength, thus leading to branched CF toward AE. In general, the cation mobility determines the CF growth direction, while the redox rates determine the CF geometry.

29.3 Modeling and Simulation of Resistive-Switching Behaviors

29.3.1 Ox-RRAM

To capture the microscopic natures and the correlations with the electric and thermal properties during the switching process, numerical solutions such as the Monte Carlo methods have been developed to quantify and predict the switching, scaling, and reliability effects of RRAM. The Monte Carlo dynamic simulation is an efficient tool to study the atomic-scale evolution of a RRAM cell, which can benefit to deeply understand the underlying physics of resistive-switching behaviors and further propose optimization schemes for the RRAM cell. The Monte Carlo simulation method can be used to self-consistently simulate the microscopic processes happened during resistive switching under the external electric field and influenced by the local temperature. The general simulation algorithm flow is shown in Fig. 29.11.

For sake of simplicity, we will take 2D simulation as an example; the simulation is performed on an atomic matrix with a size of $m * n$, where m and n depend on the size of the fabricated device. Usually as the inputs of the simulation, the intrinsic defects are introduced and randomly generated when initializing simulation. After that, the potential and current distributions in the resistive-switching layer are solved by Poisson's equations or the resistor network [63], and

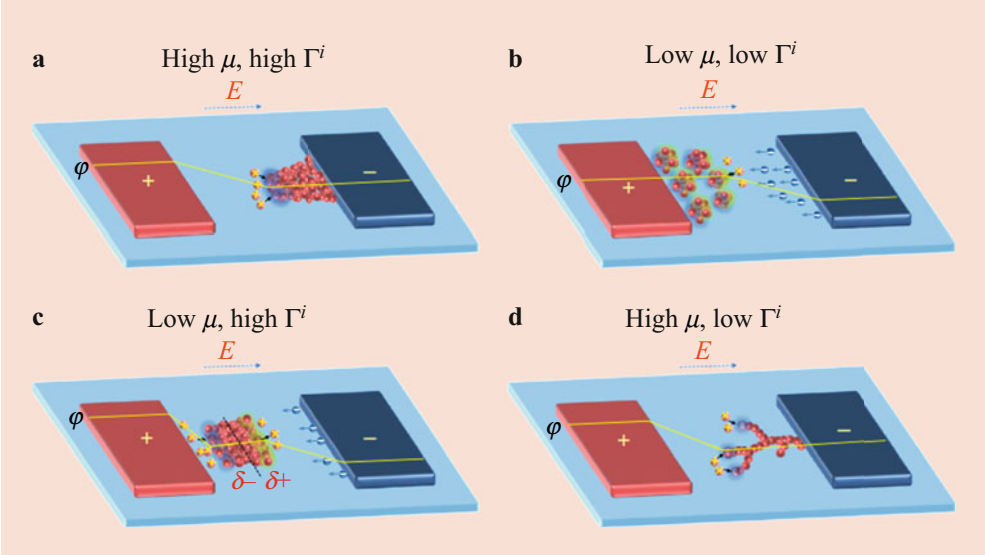


Fig. 29.10 Four different filament growth dynamics governed by kinetic parameters. (**a**) Filament growth from IE with an inverted cone shape, (**b**) filament growth from AE with discrete nanoclusters and a forward cone shape, (**c**) filament nucleation inside the dielectric and reconnection with the source, (**d**) filament growth from IE and a branched structure. (Reprinted from [71])

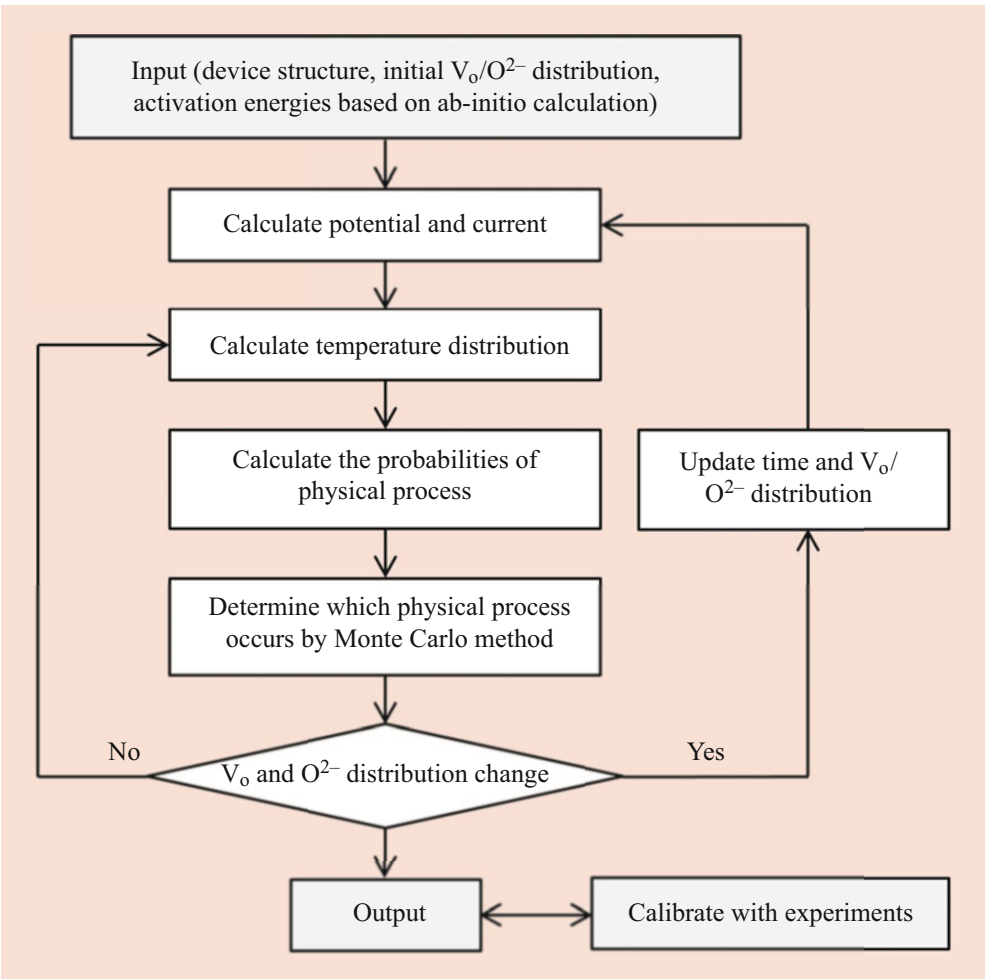


Fig. 29.11 Simulation flowchart of a typical Monte Carlo simulation algorithm for Ox-RRAM

then the local temperature distribution is calculated by the resolution pf the time-dependent heat diffusion equation [72].

$$\nabla\cdot\left[\kappa\left(\mathbf{r},T\right)\nabla T\left(\mathbf{r},t\right)\right]+g\left(\mathbf{r},t\right)=\rho C\frac{\partial T\left(\mathbf{r},t\right)}{\partial t} \quad (29.19)$$

where $T(\mathbf{r},T)$ and $g(\mathbf{r},t) = \boldsymbol{J}\cdot\boldsymbol{E}$ are the temperature and heat generation, respectively, at a given position $\mathbf{r}$ and time t, $\kappa(\mathbf{r},T)$ is the temperature-dependent thermal conductivity, ρ is the material density, and C is the specific heat capacity. Following these, the probabilities of the physical effects during resistive switching are calculated respectively. By precisely assigning different activation energies to particles according to their local structure, the probabilities of the physical processes can be calculated by Eqs. (29.1–29.4). The values of these activation energies can be either obtained through ab initio calculations or fitted with experimental results. After obtaining the probabilities, a random number uniformly distributed between [0 1] is generated and compared with these probabilities. Then a certain microscopic process is selected for each particle according to the comparison result. The time and particle distributions have to be updated in every time step. The field and temperature distributions are updated regularly, which are in turn used to update the V_O and O^{2-} configurations. For each time step, all the main physical processes are reevaluated to decide the next move. The above calculations will be repeated as the sweeping voltage changes.

Here, an example of TaO_X-RRAM is given to demonstrate the simulation results of the Monte Carlo method [63]. The simulated microscopic evolutions of CF in the Ta_2O_5 resistive-switching layer during switching are shown in Fig. 29.12. The filament configuration together with the corresponding current, temperature, and O^{2-} distributions is simulated. The simulation results indicate that the CF ruptures from the interface between the Ta_2O_5 layer and TaO_X layer and then reconnects to TaO_X layer gradually, revealing that the resistive switching is attributed to the rupture and formation of CF. More specifically, for RESET operation, the whole filament firstly disconnects at the Ta_2O_5/TaO_X interface and then extends to the interior as the sweeping voltage increases. For SET, a fine filament forms firstly in the rupture region and then gradually extends along the radius direction as current increases.

The simulated I-V characteristics of the $Pt/Ta_2O_5/TaO_X/Ta$ RRAM device are compared with measurements as shown in Fig. 29.13. The simulated results are in excellent accordance with experimental data. Points A–H in Fig. 29.12 represent each stage. The abrupt SET process and gradual RESET process can be reproduced by the simulations. From the simulation results, the 2D Monte Carlo simulation can capture the essential switching characteristics of RRAM with acceptable computation resources.

To more precisely gain the insights into the dynamics of the filament evolution, 3D simulation can be performed by Monte Carlo technique. Figure 29.14a–c shows the simulated

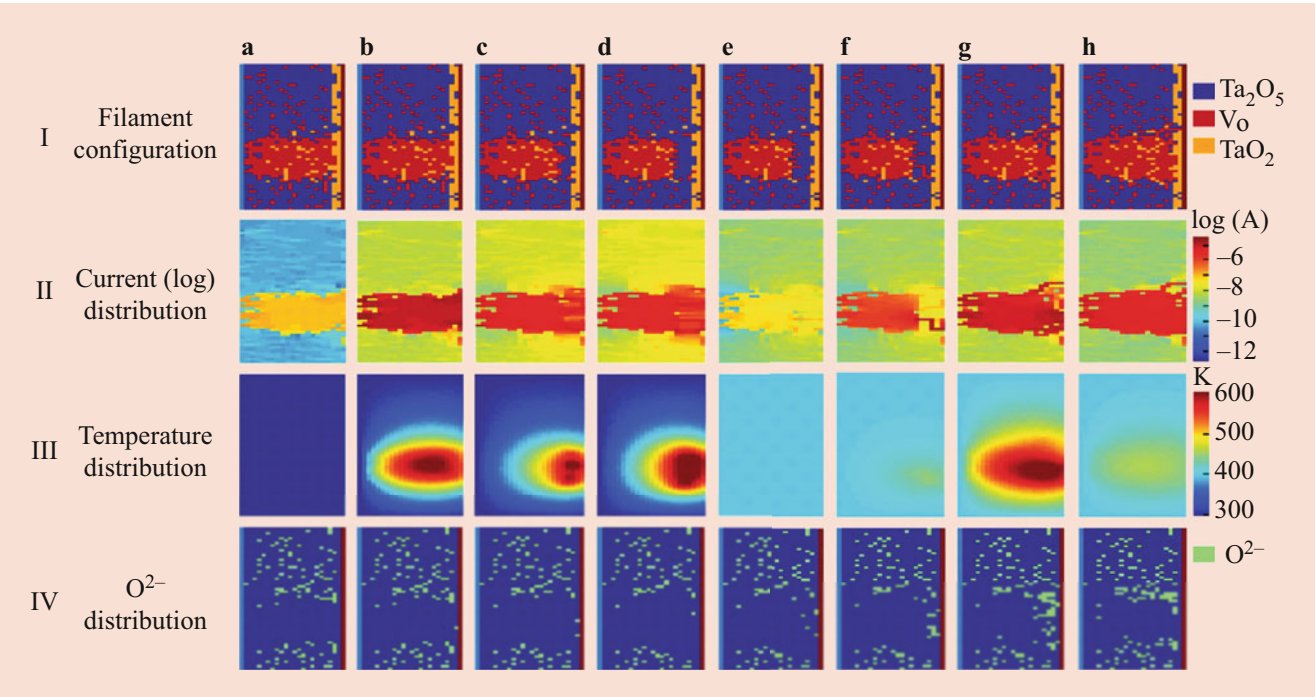


Fig. 29.12 Simulated microscopic evolutions of TaO_X-RRAM in the Ta_2O_5 resistive-switching layer during RESET and SET process. I, CF configuration; II–IV, the corresponding logarithmic current, temperature, and O^{2-} distributions. (Reprinted from [63])

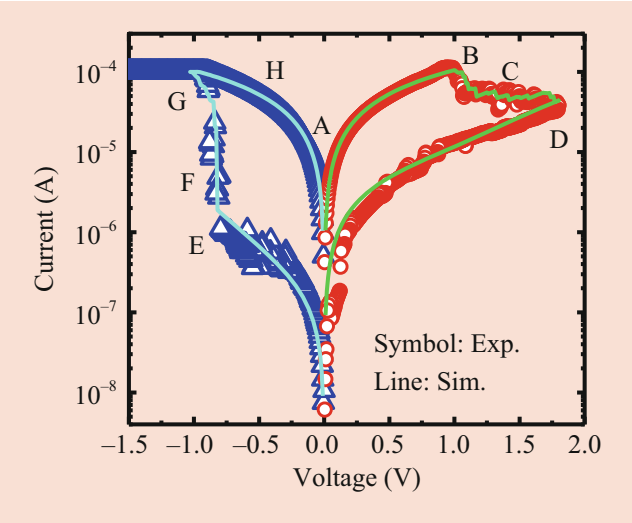


Fig. 29.13 Simulated and measured I-V characteristics of the $Pt/Ta_2O_5/TaO_X/Ta$ RRAM during the SET and RESET processes. A–H correspond to each stage in Fig. 29.12. (Reprinted from [63])

3D evolutions of V_O and O^{2-} distributions during Forming process [73]. During the initial part of the forming voltage ramp, only few native defects exist, and the device is in HRS as shown in Fig. 29.14a. Since the current is small, the power dissipation is limited, and the local temperature is uniform and equal to the ambient one, as shown in Fig. 29.14d. As the sweeping voltage approaches a critical value, the higher electric field lowers the energy needed to break the Hf-O bond, thus increasing the defect generation probability, leading to a small increase of the local temperature as shown in Fig. 29.14b, e. At the third stage, a relevant change in the Forming process occurs when the generated V_O defects create a CF as shown in Fig. 29.14c, which strongly enhances the current and the local temperature as shown in Fig. 29.14f. Compared to 2D simulation, the 3D simulation can reproduce the particle reactions and evolutions more vividly, which would benefit the understanding of the underlying physics of RRAM.

The Monte Carlo simulation method can also be used to investigate the reliability issues of Ox-RRAM. Figure 29.15 plots the simulated CF evolution processes in endurance test and the corresponding resistance varying with switching cycle under different operation Schemes [74]. The experimentally observed typical endurance degradation can be reproduced by the simulations. Based on the simulation results, the over-SET and over-RESET will result in endurance degradation. The over SET endurance degradation is attributed to the extra V_O generation during SET process, which causes the extra growth of CF size, accompanying with the reduced R_{HRS} and R_{LRS}. The over-RESET originates from extra recombination between V_O and O^{2-}, which causes the widening of electron tunneling gap. This may cause SET failure due to the weakening of electric field in gap region, resulting in the reduced V_O generation. Results reveal that CF gap distance increases during over-RESET degradation, while the radius of CF increases during over-SET degradation. The results also reveal that the operation scheme will influence the endurance degradation. Retention is another important reliability aspect. Figure 29.16 shows the LRS retention degradation and the corresponding CF geometry evolution processes [75]. The migration of V_O from CF region results in the dissolution of CF, and therefore the conduction transforms from metallic to hopping. Additionally, the O^{2-} released by the electrode and sidewall oxide can recombine the V_O which reduces the amount of V_O and leads to the rupture of the CF. Therefore, the current decreases as the time goes on.

Besides the Monte Carlo simulation including the detailed microscopic information, the compact model of RRAM is also very important, which provides fast calculations of the device electrical characteristics for circuit design and evaluations. Among various compact models, the physics-based compact model can provide accurate results capturing the dependence on the material parameters and operation parameters, through which the critical parameters during switching can be extracted from the physical view, making the device optimization and device-circuit co-design possible. The physics-based compact model can bridge the resistive-switching behaviors with the evolution of CF geometry. Based on the simulated CF geometry evolution processes during the switching process as shown in Fig. 29.12, P. Huang et al. developed a physics-based compact model for RRAM operation in which the 3D CF evolution process is modeled as shown in Fig. 29.17 [60]. Initially, there is a cylindrical CF with a diameter w_0 bridging two electrodes. The RESET process is modeled as the changing of gap distance x between the CF tip and the top electrode. Thus the gap distance x determines the HRS resistance during RESET process. Hence, x and dx/dt are key factors for RESET process. The value of dx/dt is determined by three physical processes: (1) electrode release O^{2-}, (2) O^{2-} hopping in the oxide layer, and (3) recombination between O^{2-} and V_O. The reduction of x is determined by the slowest process among the above three processes.

When O^{2-} hopping is the dominant process, the O^{2-} flow rate of $J_{O^{2-}}$, which is the amount of O^{2-} flowing through unit area of cross section per unit time, can be written as

$$J_{O^{2-}} = 1/2\,(P_h\,(E, T, dt) - P_h\,(-E, T, dt)) / \left(a^2 dt\right) \quad (29.20)$$

where a is the distance between two V_O and the coefficient 1/2 results from two different directions of O^{2-} hopping. Thus the amount of O^{2-} hopping to V_O during dt is

$$N_{O^{2-}} = J_{O^{2-}} \pi\,(w_0/2)^2 dt \quad (29.21)$$

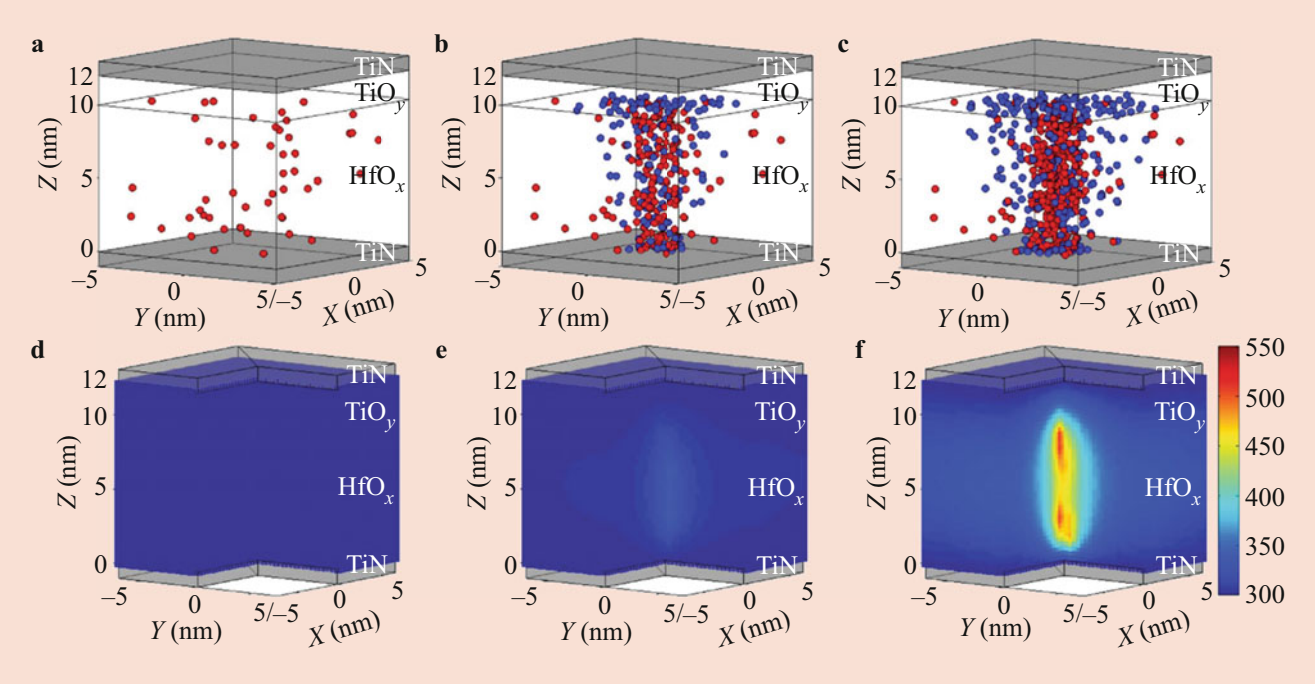


Fig. 29.14 Simulated (**a**)–(**c**) 3D V_O (red spheres) and O^{2-} (blue spheres) distributions, (**d**)–(**f**) the corresponding 3D temperature profiles. (Reprinted from [73])

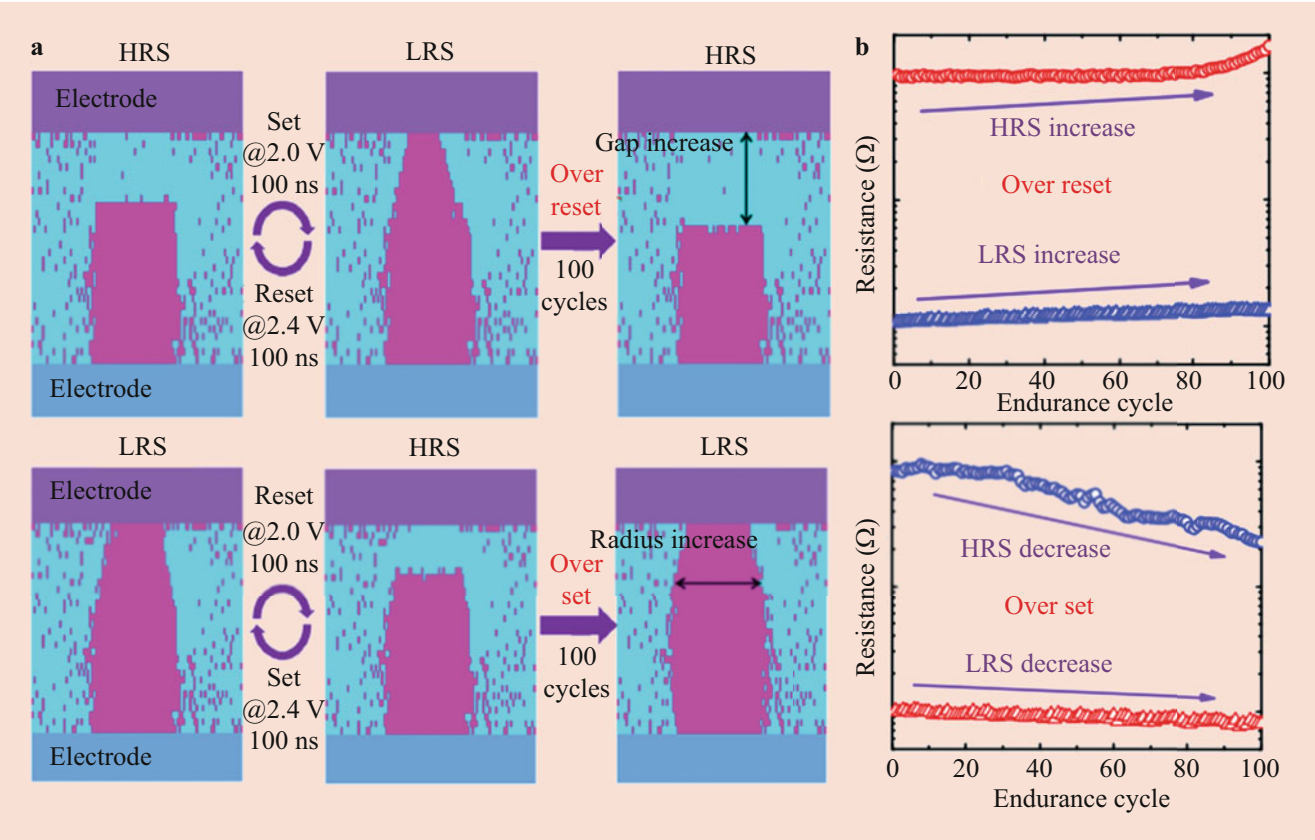


Fig. 29.15 (**a**) Simulated CF evolution in endurance test and (**b**) the corresponding resistance varying with switching cycle under different operation schemes. (Reprinted from [74])

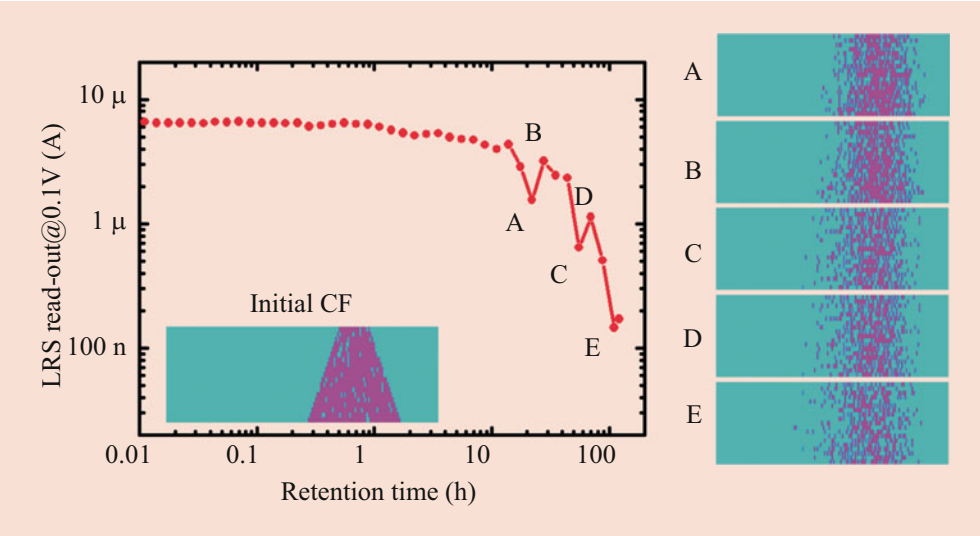


Fig. 29.16 Simulated LRS retention degradation of Ox-RRAM. The migration of V_O from CF region and the recombination of the V_O with O^{2-} released by the electrode/sidewall oxide will lead to the rupture of CF. (Reprinted from [74])

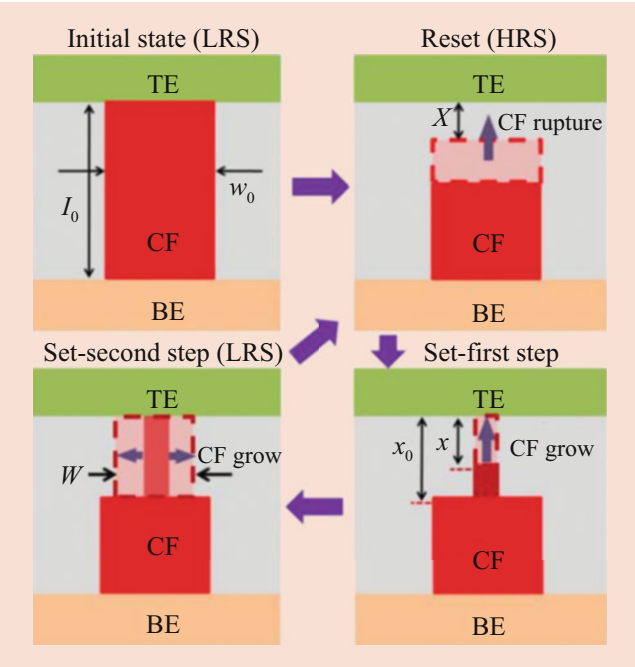


Fig. 29.17 Schematic of the CF evolution model during RESET and SET process. In RESET process, the gap distance x changes with applied voltage. The SET process is divided into two steps: CF growth from the rupture CF tip to the electrode and CF expanding along the radius direction of the formed CF. (Reprinted from [60])

and meanwhile the amount of V_O recombined with O^{2-} is

$$N_{V_O} = \pi (w_0/2)^2 \mathrm{d}x/a^3 \tag{29.22}$$

Combining (29.21, 29.22), dx/dt can be obtained as

$$\frac{\mathrm{d}x}{\mathrm{d}t} = af \exp\left(-\frac{E_h}{k_B T}\right) \sinh\left(\frac{\alpha_h Z e E}{k_B T}\right) \tag{29.23}$$

where E_h is the hopping barrier of O^{2-}, E is the electric field, α_h is the enhancement factor of the electric field for the lowering of E_h, and Z is the charge number of oxygen ion.

Similarly, when the process of electrode releasing O^{2-} is dominant, dx/dt can be written as

$$\frac{\mathrm{d}x}{\mathrm{d}t} = af \exp\left(-\frac{E_i - \gamma Z e E}{k_B T}\right) \tag{29.24}$$

where E_i is the energy barrier between the electrode and oxide and γ is the enhancement factor of the electric field. When the process of recombination between O^{2-} and V_O is the slowest, dx/dt is written as

$$\frac{\mathrm{d}x}{\mathrm{d}t} = af \exp\left(-\frac{\Delta E_r}{k_B T}\right) \tag{29.25}$$

where ΔE_r is the relaxation energy during the recombination process.

After RESET operation, x is fixed to x_0. During SET, the CF evolution is modeled by two steps: (1) a thin CF grows from the residual CF tip to the top electrode, and (2) the newly grown CF expands along the radius direction of the previously formed CF. The resistance change during SET operation is determined by the x_0 and w of the newly formed CF. Thus dx/dt and dw/dt are the key factors to model the SET operation. The key physical process during the SET process is the generation of V_O. The amount of V_O generated in the

rupture region during dt in the first step of SET process is as follows:

$$N_{V_{Og}1} = N_{sum} P_g\,(E, T, \mathrm{d}t) = P_g\,(E, T, \mathrm{d}t)\, a\pi r^2/a^3 \quad (29.26)$$

where r is the radius of newly grown thin CF. The absolute value of dx equals to the gap distance variation of the newly grown CF, which is

$$\mathrm{d}x = -\frac{N_{V_{Og}1} a^3}{\pi r^2} = -af \exp\left(-\frac{E_a - \alpha_a ZeE}{k_B T}\right) \mathrm{d}t \quad (29.27)$$

where E_a is the average activation energy of V_O. In the second step, the generation of V_O mainly occurs in the extended region along the radius direction. The changing rate of the width of CF is given as

$$\frac{\mathrm{d}w}{\mathrm{d}t} = \left(\Delta w + \frac{\Delta w^2}{2w}\right) f \exp\left(-\frac{E_a - \alpha_a ZeE}{k_B T}\right) \quad (29.28)$$

where Δw is the effective expanding width of CF.

Based on the CF evolution model, the conduction of the RRAM cell is modeled as shown in Fig. 29.18. Two major kinds of electron transport are identified in RRAM: the conduction in the CF region is considered as metallic, while the conduction in the gap region is hopping. The metallic current in the CF can be derived from Eq. (29.7) and Ohm's law. The hopping current is correlated with the voltage and gap distance by [76].

$$I = I_0 \exp(-x/x_T) \sinh(V/V_T) \quad (29.29)$$

where I_0 is 10 μA/nm^2 and x_T and V_T are the characteristic length and voltage. The LRS is modeled by the conduction of CF with a width of w parallel with a nonlinear hopping current as shown in Fig. 29.18a. Under ultralow current condition, w is small and the nonlinear I-V characteristics at LRS can be reproduced as shown in Fig. 29.18b. On the other hand, conduction in HRS can be equivalently modeled as two parallel nonlinear hopping currents with different x and the I-V characteristics of HRS are shown in Fig. 29.16c.

During resistive switching, the formation and rupture of CF are very sensitive to local temperature, and therefore it should be properly considered. For simplicity, we assume uniform temperature in the electrolyte layer. An analytic model for temperature at LRS can be adopted, which is [66].

$$T = T_0 + IVR_{th} \quad (29.30)$$

where T_0 is the ambient temperature and R_{th} is the effective thermal resistance. It should be noted that this temperature model is based on a quasi-static approach, which means

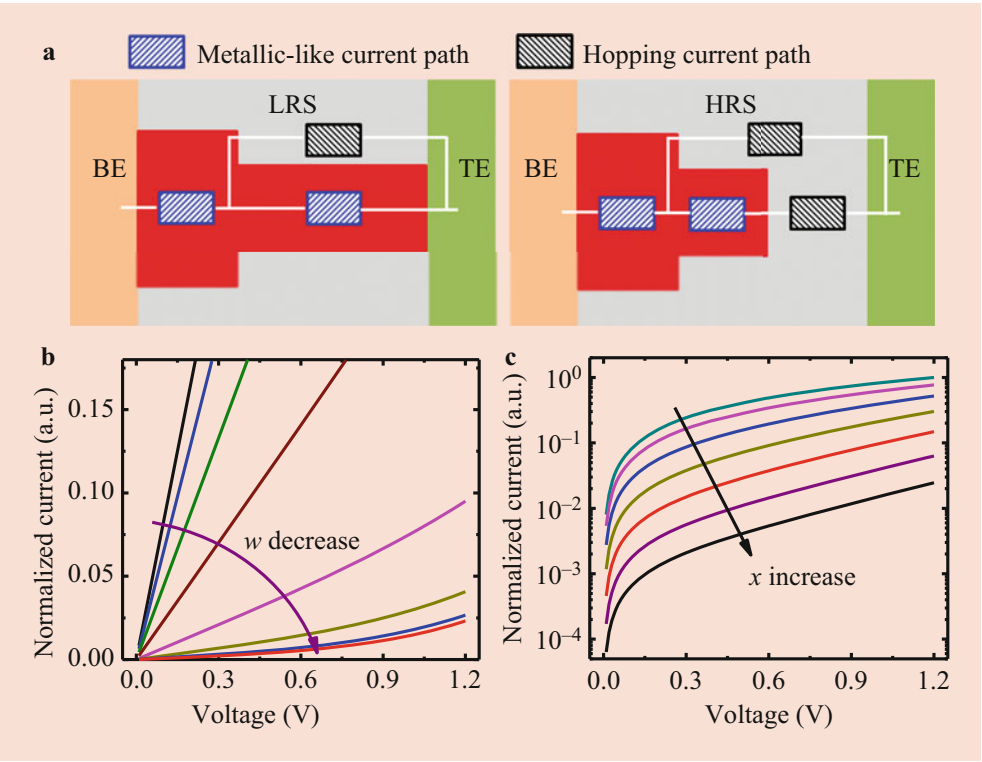


Fig. 29.18 (**a**) Equivalent circuit of conduction in LRS and HRS. (**b**) LRS and (**c**) HRS I-V curves reproduced by the conduction model. (Reprinted from [60])

the thermal equilibrium is assumed to be reached once the operation voltage is applied on the cell.

The equivalent circuit of the Ox-RRAM cell is shown in Fig. 29.19. It consists of a parallel capacitance (C_p), a large parallel resistance (R_p), and contact resistance (R_c) together with the resistive-switching elements (R_s). C_p results from the intrinsic MIM structure. R_p includes the conduction associated with the leakage current between two electrodes. R_c represents the total resistance of the electrodes itself and the contact resistance between CF and electrodes.

Utilizing the above model, the electrical characteristics of Ox-RRAM can be reproduced. Figure 29.20a shows the measured and calculated DC I-V curves during RESET and SET processes of the TiN/HfO$_X$/Pt/AlO$_X$/Pt bilayer devices. The compact model can successfully reproduce the gradual RESET and the abrupt SET processes that match perfectly with the measured data. It can be also found that the HRS resistance is high with large stop voltage during RESET process and will cause high SET voltage in the following SET process. Figure 29.20b shows the calculated and measured transient response current waveforms for the two RESET programming schemes in the TiN/HfO$_X$/Pt/AlO$_X$/Pt bilayer device. Excellent agreements between the modeling and measured data show the validity and universality of this compact model to capture the main features of the Ox-RRAM under both DC and AC operations.

Besides the physics-based model, S. Kim et al. propose a numerical electro-thermal model using the finite element method to quantitatively describe the electrical characteristics of Ox-RRAM [77]. The model is based on a V_O migration mechanism in a bilayer Ta_2O_5/TaO$_X$ device. During the Forming process, the charged V_O is attracted from the TaO$_X$ layer to the TE, where the TaO$_X$ layer only serves as the role of the V_O reservoir. The CF is described as a doped region where V_O acts as dopants and thus contributes to local electrical and thermal conductivity values. The migration of V_O is simulated by the local temperature and electric field derived from carrier continuity and heat equations fully coupled in a 3D geometry, which considers a complete bilayered structure that includes the top and bottom electrodes as shown in Fig. 29.21a. After the Forming process, the SET and RESET processes are described through V_O migration induced by the local electric field and temperature due to Joule heating. Thus, simulation of SET and RESET requires the self-consistent solution of three partial differential equations:

(1) A drift/diffusion continuity equation for V_O transport, which is

$$\frac{\partial n_D}{\partial t} = \nabla \cdot (D\nabla n_D - \nu n_D) + G \qquad (29.31)$$

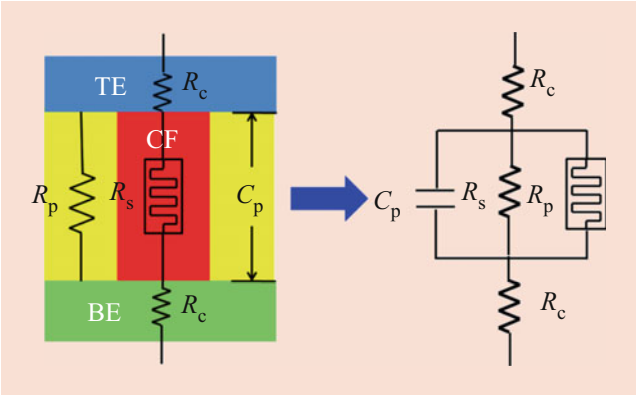


Fig. 29.19 Equivalent circuit of the Ox-RRAM cell with parasitic resistance and capacitance. (Reprinted from [60])

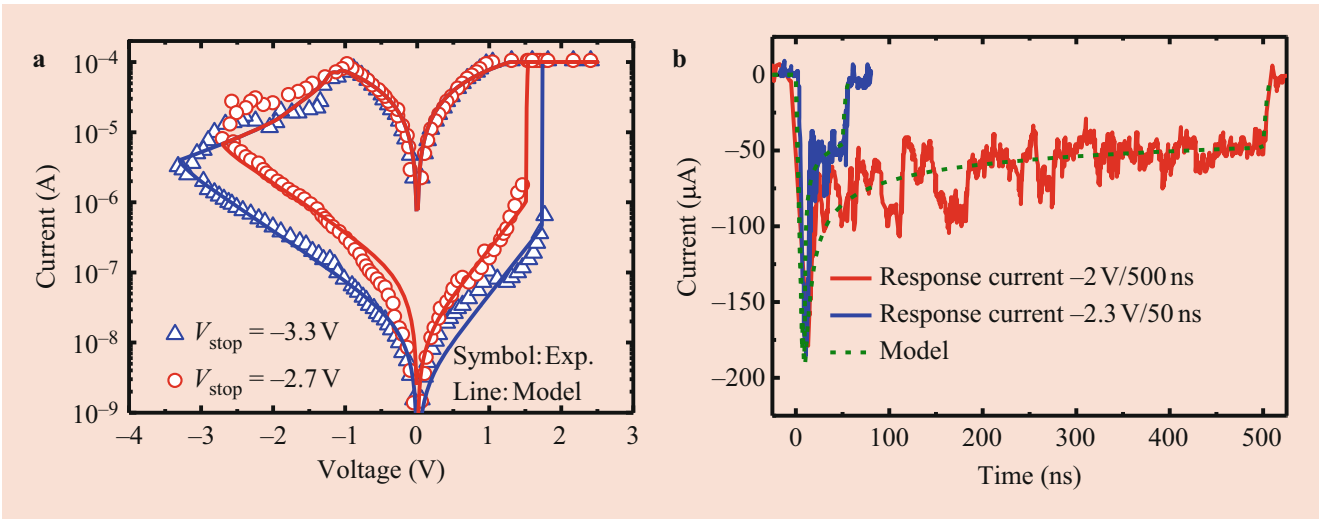


Fig. 29.20 (**a**) Measured and model calculated DC I-V characteristics of the TiN/HfO$_X$/Pt/AlO$_X$/Pt bilayer devices. (**b**) Measured and model calculated transient response current waveforms for the two RESET programming schemes. (Reprinted from [60])

where n_D is the concentration of V_O and D is the diffusivity of V_O, which can be described by

$$D = \frac{1}{2}a^2 f \exp\left(-\frac{E_a}{kT}\right) \tag{29.32}$$

where a is the V_O hopping distance and E_a is the diffusion barrier. v is the drift velocity of V_O, which is

$$v = af \exp\left(-\frac{E_a}{kT}\right) \sinh\left(\frac{qaE}{kT}\right) \tag{29.33}$$

and G is the generation rate of V_O, which is

$$G = A \exp\left(-\frac{E_b - q\beta E}{kT}\right) \tag{29.34}$$

where A is the coefficient of generation rate and β is the mesh size.

(2) A current continuity equation for electrical conduction

$$\nabla \cdot \sigma \nabla \psi = 0 \tag{29.35}$$

where ψ is the potential.

(3) A Fourier equation for Joule heating

$$-\nabla \cdot k_{th} \nabla T = J \cdot E = \sigma |\nabla \psi|^2 \tag{29.36}$$

Figure 29.21b shows the simulated region. In the calculations, the axisymmetric geometry allowed the 3D problem to be reduced to a 2D solution with a radial coordinate and a vertical coordinate. Figure 29.21c shows the measured and calculated I-V characteristics during the SET and RESET processes. The SET and RESET transition points show good consistency with the measured data.

The similar modeling method can be used for the reliability projection of Ox-RRAM and the crossbar array. P. Huang et al. have developed an analytic model for the endurance degradation of Ox-RRAM [74]. The endurance degradation behaviors under various operation modes can be predicted by the model and verified by the measurements. Based on the simulation results in Fig. 29.15, the analytic model including over-SET and over-RESET effects is proposed as shown in Fig. 29.22. An over-rupture region and an over-grow region during the switching process are introduced to model the endurance degradation. The parameters to characterize those regions are Δx and Δr. Δx and Δr are the difference of gap distance and CF radius between two consecutive cycles, respectively. $\Delta x/\Delta r$ is determined by the intrinsic effects, and the interaction effect between Δx and Δr. Δx can be described by

$$\Delta x_{n-1} = (1 - 1/\gamma_r)\, t\, v_x|_{x=x_{n-1}} - \eta \left(r_{n-1}^2/r_{n-2}^2 - 1\right) x_{n-1} \tag{29.37}$$

where x_n is the gap distance in HRS after n switching cycles, r_n is the radius of CF in LRS after n switching cycles, t^* is the time of residual CF tip growing to connecting the two electrodes, γ_r is the over rupture factor, and v_x is the x

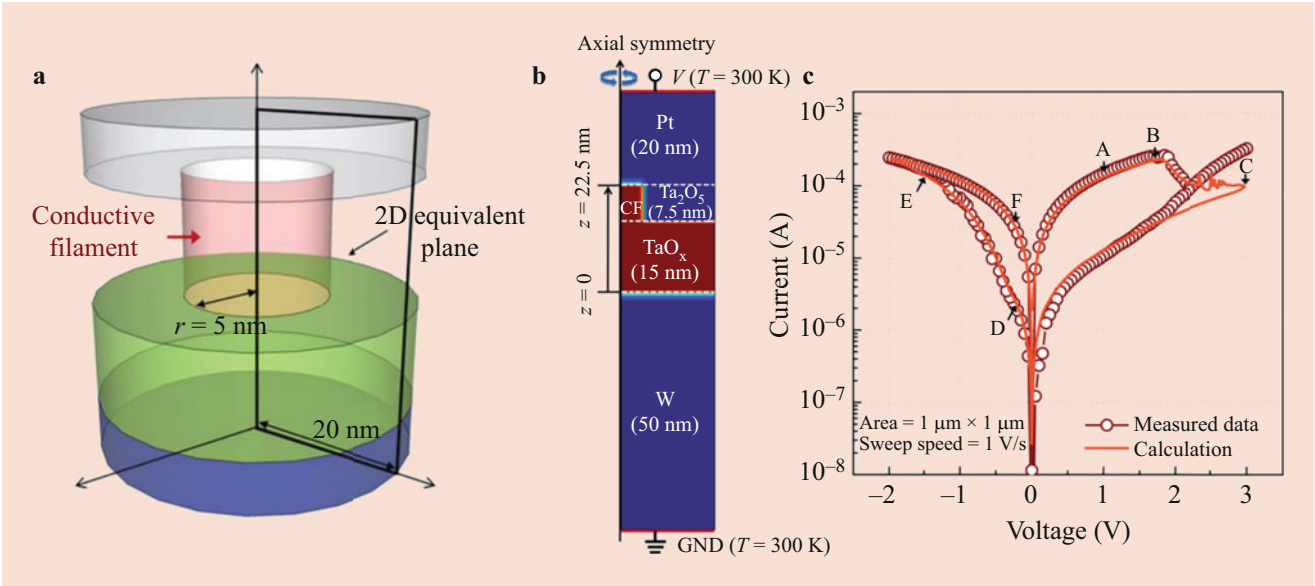


Fig. 29.21 (**a**) Simulated geometry used in calculation of the Pt/Ta_2O_5/TaO_X/W RRAM, (**b**) simulated boundary conditions, (**c**) measured and calculated I-V characteristics. (Reprinted from [77])

changing rate during RESET process. Δr can be deduced as

$$\Delta r_{n-1} = (\gamma_s - 1)\left(t^* v_r|_{r=r_{n-1}} + r_{n-1} - 2a\right) - \left[\Delta x / \left(v_x|_{x=x_n}\right) + (\gamma_r - 1)\, t^*\right] v_r|_{r=r_{n-1}} \quad (29.38)$$

where γ_r is the over-grow factor and v_r is the rate of CF growth.

By combining the endurance degradation model with the compact model of RRAM transient operations described by Eqs. (29.23)–(29.28), the endurance degradation can then be investigated. The model calculated and measured dependence of ratio degradation of over-SET on SET voltage and RESET voltage in TiN/Ti:HfO_X/Pt RRAM structure are shown in Fig. 29.23. The results imply that proper high RESET voltage and low SET voltage can suppress the ratio degradation caused by over-SET. This is because low SET voltage and high RESET voltage are not beneficial for the accumulation of extra O^{2-} during the switching cycle.

29.3.2 CBRAM

The device characteristics of CBRAM can be modeled and simulated similarly with Ox-RRAM, and the main difference is the resistive-switching mechanism. In this section, we will introduce some examples of various modeling and simulation methods to better illustrate the characteristics of CBRAM.

As mentioned previously, for CBRAM, various CF geometries, growth directions, and CF dissolution positions in different materials have been observed by experiments. Simulations can help to clarify the critical issues such as the impacts of the materials on the CF properties, which will help to understand the underlying physics in the CBRAM cell. Based on the physical effects, Y. Zhao et al. have developed a Monte Carlo simulation platform to capture the essential features during switching and the correlated microcosmic properties of the CBRAM device [68]. Figure 29.24a shows the simulated I-V characteristics of the Cu/Al_2O_3/TiN cell, in good agreement with the experimental data from [78]. The corresponding CF geometry can also be simulated by the simulation platform as shown in Fig. 29.24b, which is consistent with the experimental observation after SET by AFM in [78]. Based on the simulation results, in the case of Cu/Al_2O_3/TiN, the CF dissolves at the thinnest part due to the thermal-electric effect near IE.

Using the Monte Carlo simulation platform, by adjusting the material parameters and operation schemes, different CF geometries and growth directions can be simulated, which are summarized in Table 29.1 [79]. The simulation results reveal that the CF geometry is associated with the probabilities of oxidation, hopping, and reduction processes which are represented by P_o, P_h, and P_r. These probabilities highly rely on the activation energy (which varies with different materials) and the electric field (which depends on the operating schemes according to Eqs. (29.11, 29.12, and 29.14)). When choosing the electrolyte material with high cation mobility, P_o is usually less than P_h. In this case, the CF grows from IE to AE during Forming process. By contrast, if the cation mobility in the electrolyte is low, the CF grows from AE to IE during the Forming process. The CF geometry is determined by the competition between P_h and P_r: when P_r is larger than P_h, the CF is a converted cone; when P_r is smaller than P_h, the CF is a forward cone. The simulated CF geometry is consistent with the experimental observations in Refs. [67, 80, 81]. As shown in Table 29.1, the CF evolution is summarized as three modes labeled as Modes I–III according to the CF growth direction and geometry.

The simulation results show that the CF evolutions in the three different modes are quite similar. During RESET process, the CF first laterally narrows at the thin end, and then it shortens vertically once it ruptures. During SET process, the CF first grows vertically to connect two electrodes, and then it laterally expands near the thin end. The simulated DC I-V characteristics in Table 29.1 shows that the switching voltage and the resistance window are small in Mode II compared with Modes I and III.

The mechanical response of the electrolyte layer can also be investigated by simulations [82]. In liquid, the CF growth can take place in any direction. However, in a solid ion conducting layer, the filament growth induces mechanical stress in the host matrix, which would constrain the CF to some finite small size in general. To model the mechanical stress, a radial two-spring model is proposed in Fig. 29.25a. The small spring (I) model relaxation processes within the nanotemplate and yields a nonlinear Young's modulus that changes from a lower value $E_{1,0} = 500$ MPa to a $E_{1,max} = 1$ TPa within the first $l_1 = 5$ nm according to

$$E_1 = E_{1,0} \exp\left(\frac{r}{l_1} \ln\left(\frac{E_{1,max}}{E_{1,0}}\right)\right) \quad (29.39)$$

Spring (II) describes the mechanical properties of the electrolyte, and a constant Young's modulus E_2 is assumed. The young's modulus is related to the spring constant k according to $k = EA_k/L$, where A_k denotes the cross section on which the force works, i.e., the grid size is a^2, and L is the cell thickness. The overall radial spring constant is then calculated using $k_{ser} = k_1\, k_2/(k_1 + k_2)$. The mechanical work ΔW_{mech} that is stored when the spring is compressed by r results from the integration of Hooke's law, which is

$$\Delta W_{mech} = e \int_0^d r k_{12}\left(d'\right) \mathrm{d}d' \quad (29.40)$$

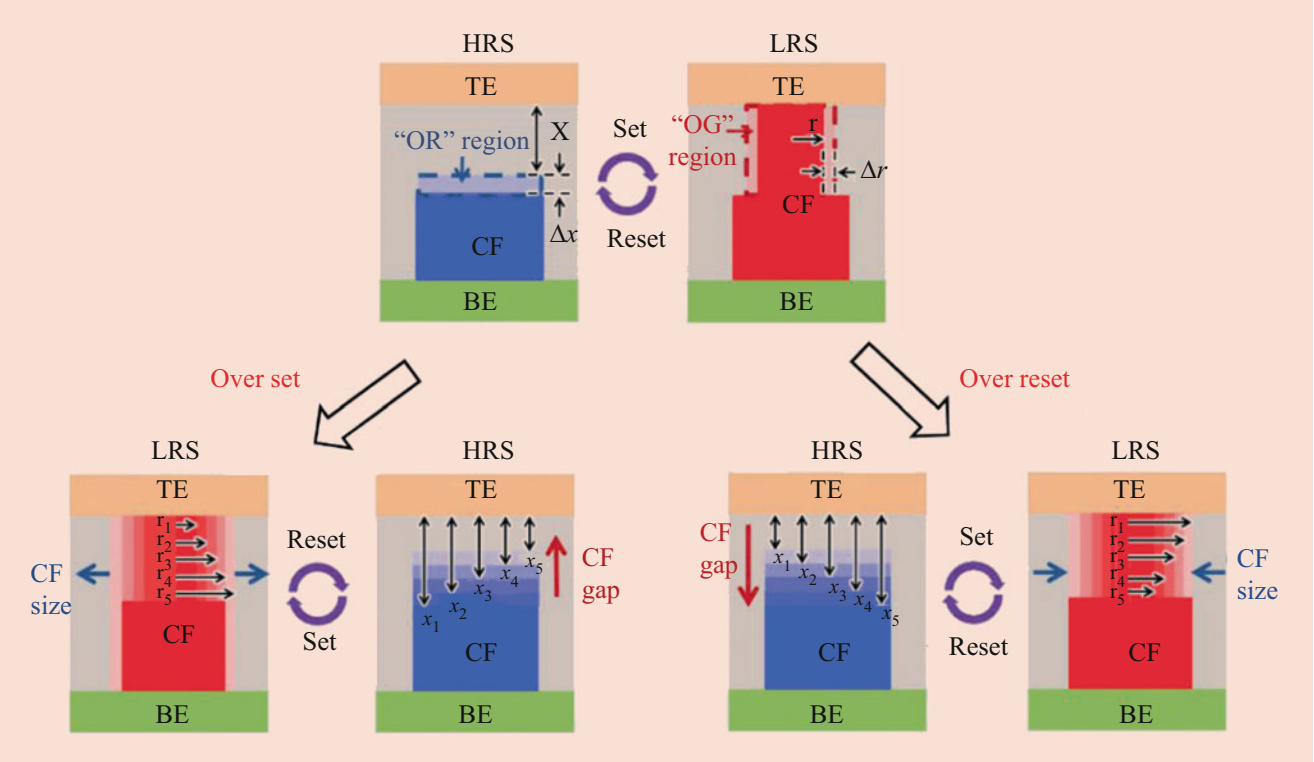


Fig. 29.22 Schematic of the endurance degradation model. (Reprinted from [74])

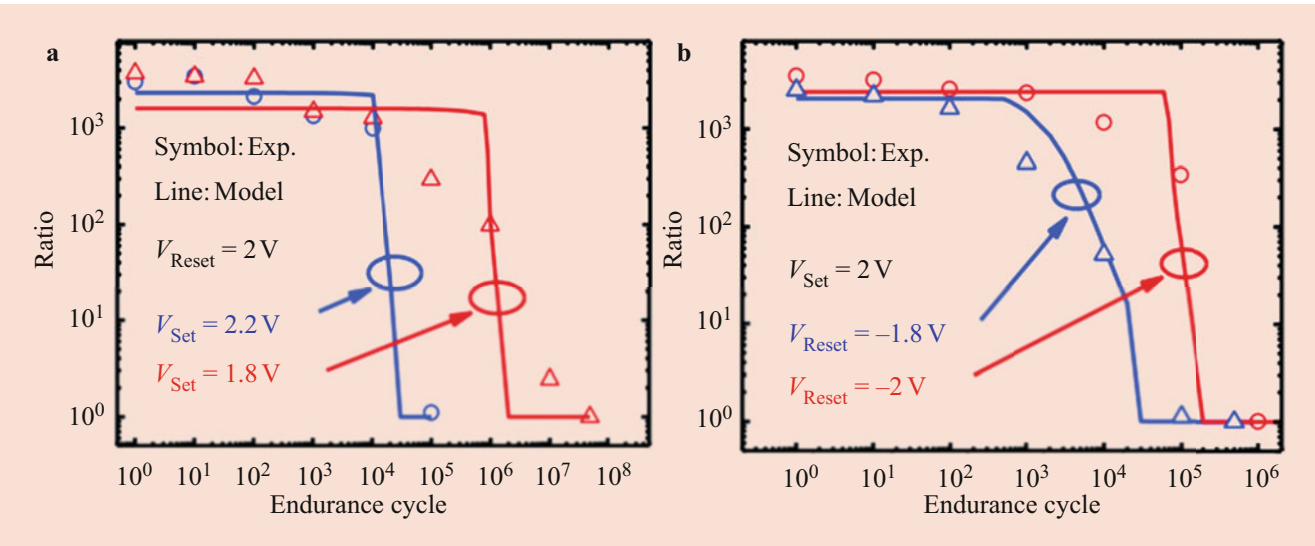


Fig. 29.23 Calculated and measured dependence of ratio degradation of over-SET on (**a**) SET voltage and (**b**) RESET voltage in TiN/Ti:HfO_X/Pt RRAM. (Reprinted from [74])

where d equals the CF diameter along the vertical axis. Figure 29.25a shows the mechanical work as a function of CF diameter for $E_2 = 10$ GPa and 500 MPa. The mechanical work is added to the reduction rate which is

$$\Delta W_{\mathrm{red,eff}} = \Delta W_{\mathrm{red}} + \Delta W_{\mathrm{mech}} \tag{29.41}$$

SET simulations were performed as shown in Fig. 29.25b, c. The diameter of the grown CF depends on Young's modulus of the electrolyte. If the Young's modulus is high, the mechanical stress applied on the filament is big resulting in a small CF diameter.

Simulations can also help to reveal the role of electrode work functions (Φ) in the switching kinetics [83]. For both

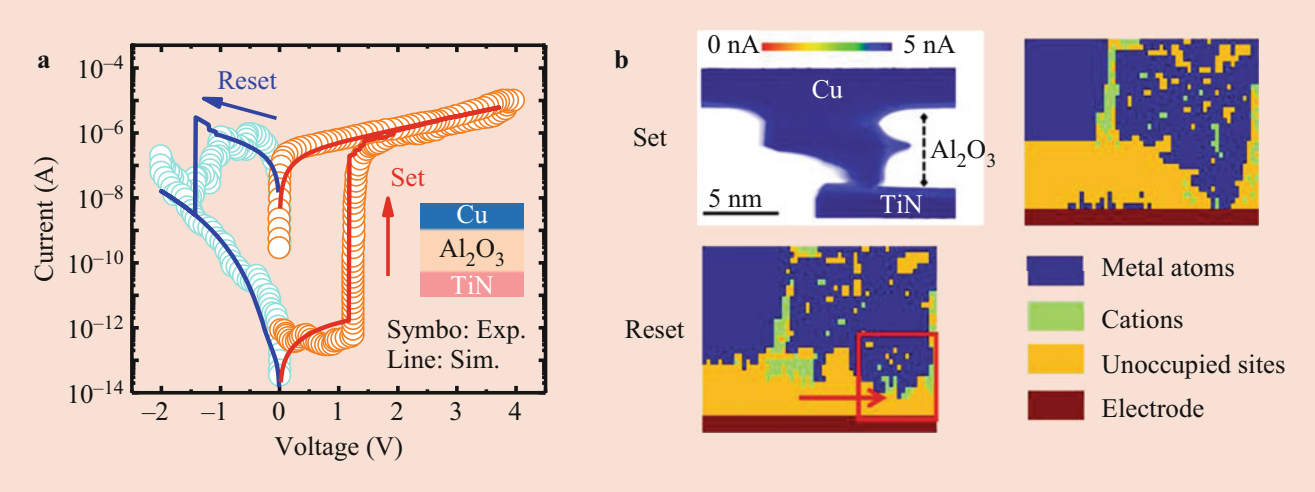


Fig. 29.24 (**a**) Comparison between simulated I-V characteristics in Cu/Al_2O_3/TiN cell and experimental data. (**b**) The comparison of simulated CF with experimental observation by AFM after SET and the simulated CF configuration after RESET. (Reprinted from [68])

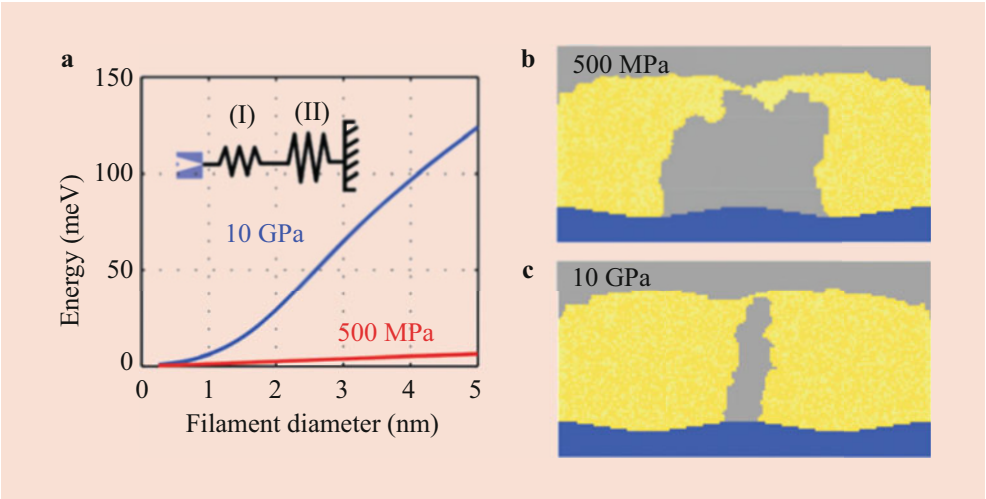
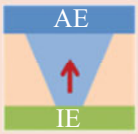
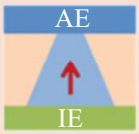
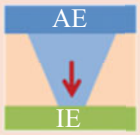
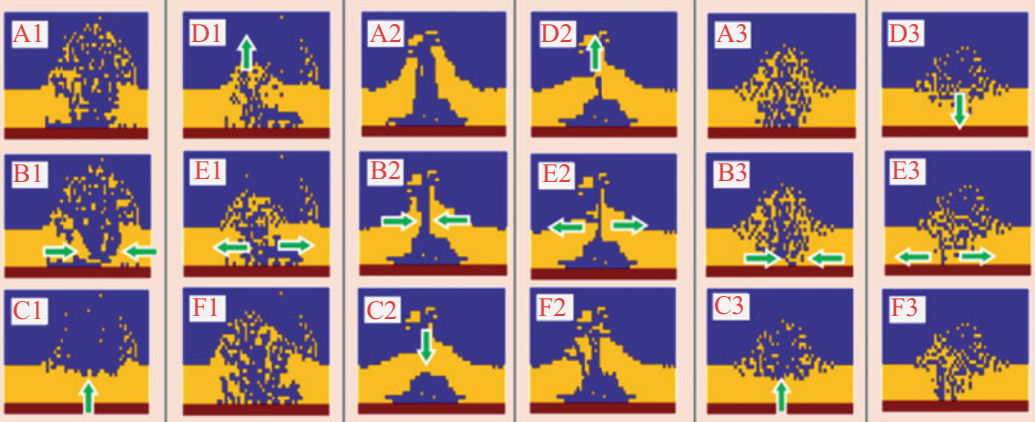
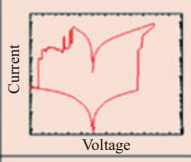
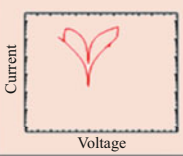
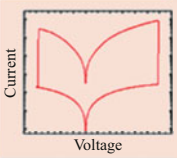
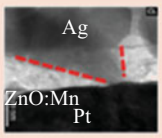
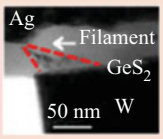
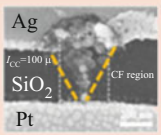


Fig. 29.25 (**a**) 1D model of the mechanical stress inside the electrolyte layer depending on the filament diameter. (**b**) The simulated CF shape when Young's modulus of $E_2 = 500$ MPa and (**c**)$E_2 = 10$ GPa. (Reprinted from [82])

electrodes, an increase of Φ leads to a reduction of Forming time as shown in Fig. 29.26. Φ induces a flat band voltage shift but also affects the chemical reactions: increasing Φ_{TE} (or Φ_{BE}) reduces the effective oxidation (or reduction) energy barrier. While in the case of the TE, the reduction of Forming voltage is essentially due to the oxidation barrier decrease. For the BE, the reduction of Forming voltage results from the variation of the flat band voltage (neglecting the reduction barrier change). The schematic illustration of the TE case is shown in Fig. 29.26a. In terms of the relationship between the pulse voltage and Forming time, the increase of Φ_{TE} shows a shift of the characteristics, favorable to low-voltage operation but with a stronger effect for Φ_{TE} as shown in Fig. 29.26b.

The Monte Carlo simulation is also employed to investigate the HRS and LRS retention behaviors [83]. The same physical properties and parameters as for the switching are used; the only difference resides in the main accelerating factor, being the voltage for Forming/SET and the temperature for data retention. Figure 29.25 shows the measured and simulated retention characteristics under 100 °C for both the HRS and the LRS. The results indicate that the higher the compliance current, the lower the initial resistance, and the better the retention. This can be explained by the fact that the core of CF remains intact longer for a thick filament, which enhances its retention capabilities. HRS is described by the presence of a residual filament. HRS resistance decreases over time as the dissolution of the CF tends to recreate a conducting path in the electrolyte. The reformed conductive path can be simulated in Fig. 29.27a showing only little differences with the final LRS. Figure 29.27b shows the temperature impacts on the retention with the corresponding simulated final states. An increase of resistance value with

Table 29.1 The summary of the different CF evolution modes

	I	II	III
Material property & operation scheme	$P_o < P_h$ Low E_h: Electrolyte of high cations mobility		$P_o > P_h$ High E_h: Low cations mobility
	$P_r > P_h$	$P_r <= P_h$	$P_r > P_h$
CF growth during forming	 Growth direction	 Growth direction	 Growth direction
CF evolution	RESET: I: CF lateral narrowing II: CF vertical shortening		SET: I: CF vertical growth II: CF lateral expanding
	Reset / Set	Reset / Set	Reset / Set
			
DC I-V	 Relatively large operation voltage & resistance window	 Small operation voltage & resistance window	 Large operation voltage & resistance window
CF geometry in Ref.	 Mode I	 Mode II	 Mode III

Reprinted from [79]

the time spent at high temperature is found. The resistance increase corresponds to the loss of data over time and is due to the CF dissolution. The higher the temperature, the more dissolved the CF, and the worst the retention.

Another method to simulate retention characteristics of CBRAM is to use a 2D numerical method [84]. The rectangular CF is assumed to be composed of metal atoms regularly distributed and each atom being treated independently. During bake, each metal atom starts to migrate following a random diffusion vector, which is

$$\overrightarrow{d_{x,y}} = \sqrt{2D} \cdot \text{Rand}\left(\overrightarrow{x}, \overrightarrow{y}\right) \tag{29.42}$$

where Rand is a randomly generated value following a normal distribution and D the diffusion coefficient in agreement with Fick's law

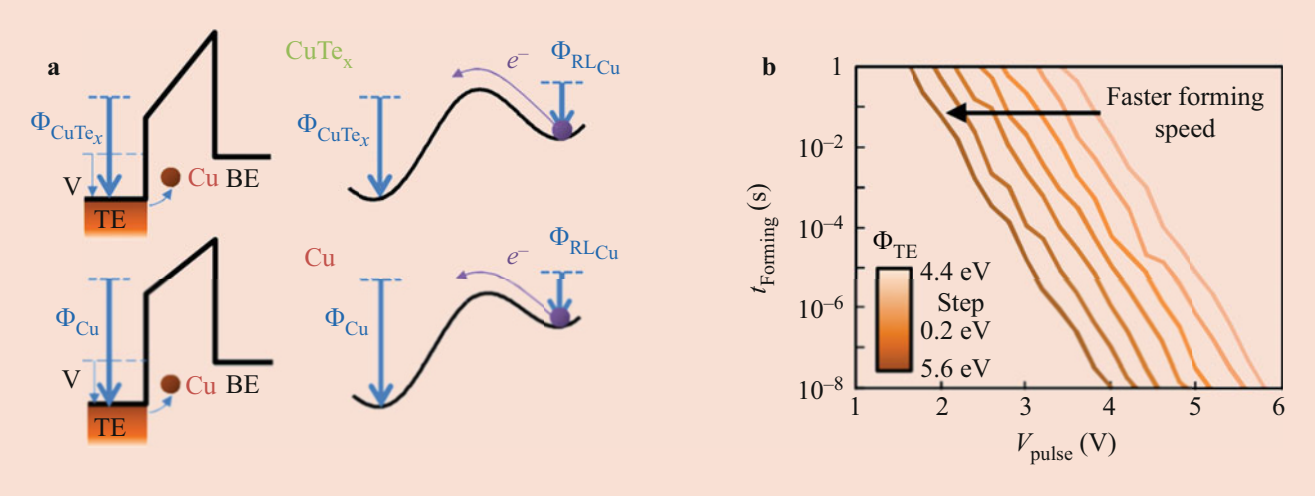


Fig. 29.26 (**a**) The schematic illustration of the impact of Φ_{TE} on the electric field in the electrolyte layer and on the oxidation-reduction reaction. (**b**) Simulated forming time as a function of the applied pulse voltage for various TE work functions. (Reprinted from [83])

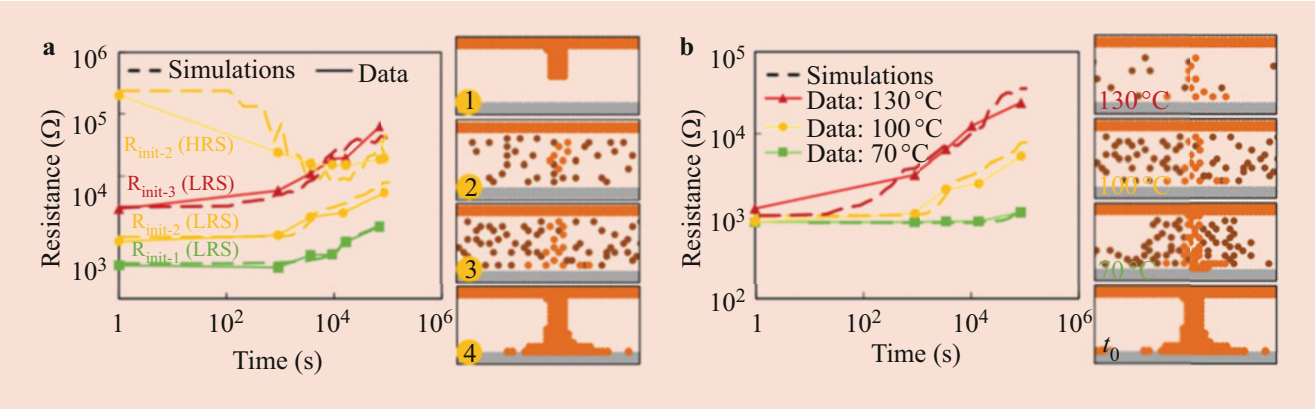


Fig. 29.27 (**a**) LRS and HRS retention degradation simulations and experimental data. (**b**) LRS retention experimental results and simulations. (Reprinted from [83])

$$D = D_0 \cdot \exp\left(-\frac{E_A}{kT}\right) \tag{29.43}$$

where D_0 is the diffusivity pre-factor, E_A is the activation energy, and T is the temperature. The cell resistance is then computed with a percolation model in a resistance network as shown in Fig. 29.28a. Figure 29.28b illustrates typical simulated LRS and HRS retention curves with the corresponding evolution of the CF morphology.

For the quick evaluation of the CBRAM characteristics in the array and circuit level, the detailed particle evolution can be neglected by highlighting the essential electrical characteristics. One way to model the switching kinetics of CBRAM is to use the electrochemical method proposed by S. Menzel et al. [70]. Depending on the electrode and electrolyte materials and also the thermodynamic conditions, the rate-limiting steps in the switching kinetics are (1) the nucleation process prior to CF growth, (2) the electron-transfer reaction at the metal/insulator interfaces, and (3) the cation transport within the electrolyte material. To model the switching kinetics, these processes can be divided into two steps: nucleation and the CF growth. For the first nucleation step, the nucleation time t_{nuc} can be written as [70]

$$t_{nuc} = t_{0,nuc} \cdot \exp\left(\frac{\Delta G_c}{k_B T}\right) \cdot \exp\left(-\frac{(N_c + \alpha)\, ze}{k_B T} \eta_{nuc}\right) \tag{29.44}$$

where $t_{0,nuc}$ is a leading factor, and here $\eta_{nuc} = V_{app}$. At time t_{nuc} the CF starts to grow. During the CF growth procedure, the equivalent circuit can be depicted as shown in Fig. 29.29a. The CF growth is modeled by the change in the tunneling gap between the filament and AE. The cylindrical CF has a cross-sectional area A_{fil} and a resistance R_{fil}. The dynamic evolution of the gap is assumed to be one dimensional and can be expressed using Faraday's law

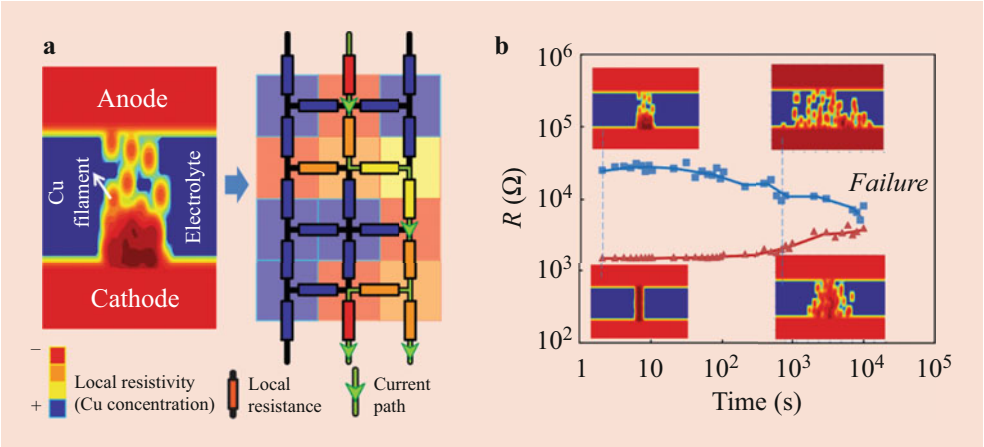


Fig. 29.28 (**a**) The resistance network used to compute the cell resistance during bake for a given metal atom distribution in the electrolyte. (**b**) Simulations of typical HRS and LRS retention characteristics at 100 °C with the CF morphologies at 2 s and 1000s. (Reprinted from [84])

$$\frac{\partial x}{\partial t} = -\frac{M_{\mathrm{Me}}}{ze\rho_{\mathrm{m,Me}}} J_{\mathrm{ion}} \tag{29.45}$$

Here, M_{Me} is the atomic mass of the deposited metal and $\rho_{\mathrm{m,Me}}$ is its density. The current density J_{ion} can be obtained by Eq. (29.18) for hopping current or Eq. (29.17) which is the Butler-Volmer equation. The electron tunneling current in the gap region can be expressed by

$$I_{\mathrm{Tu}} = C\frac{3\sqrt{2m_{\mathrm{eff}}\Delta W_0}}{2x}\left(\frac{e}{h}\right)^2 \exp \left(-\frac{4\pi x}{h}\sqrt{2m_{\mathrm{eff}}\Delta W}\right) A_{\mathrm{fil}} V_{\mathrm{Tu}}. \tag{29.46}$$

where m_{eff} is the electron effective mass, ΔW_0 is the effective tunneling barrier, h is Planck's constant, and V_{Tu} is the tunneling voltage. According to the equivalent circuit in Fig. 29.29a, the overall cell current is calculated by the sum of the ionic current and the tunneling current

$$I_{\mathrm{cell}} = I_{\mathrm{Tu}} + I_{\mathrm{ion}} \tag{29.47}$$

which is only a function of the overpotential η_{fil} and the gap distance x. Applying Kirchhoff's law, the cell voltage is

$$V_{\mathrm{cell}} = I_{\mathrm{cell}}\left(\mathrm{R_{el}} + R_{\mathrm{s}} + \rho_{\mathrm{fil}}\left(L - x\right)/A_{\mathrm{fil}}\right) + V_{\mathrm{Tu}} \tag{29.48}$$

which is also only a function of the overpotential η_{fil} and the gap distance x. The set of Eqs. (29.45–29.48) describes the dynamic behavior of the CF growth. The ordinary differential Eq. (29.45) can be solved numerically using an advanced Euler method. In each time step, the overpotential η_{fil} is calculated numerically using Eqs. (29.47 and 29.48) under different operation conditions.

Using this model, the simulations of switching kinetics have been conducted. During the simulation, first the nucleation time is calculated, and afterward the filament growth is simulated starting at the nucleation time. Figure 29.29b shows the simulated switching times as a function of the applied voltage for different temperatures and compared with experimental data. The model fits perfectly to the experimental data.

In order to bridge the electrical characteristics with the microscopic behaviors of CBRAM, a physics-based compact model is developed by Y. Zhao et al., which can clarify the impacts of CF evolution on electrical behaviors step by step based on the underlying physics. Due to the various CF growth modes, the modeling process of CBRAM would be different with that of Ox-RRAM. According to the simulated microscopic configurations of CF evolutions of the three modes in Table 29.1, The CF evolution can be modeled in Figs. 29.30 and 29.31 [79].

During the three CF evolution modes of RESET, the CF first narrows at the thin end and then dissolves from the weakest part toward the interior of the electrode along the direction of electric field as shown in Fig. 29.30. The CF geometry can be described by the following parameters: the small radius r_{t}, the wide radius r_{w}, and the filament height h, which determines the resistance of LRS. The gap distance x determines the resistance of HRS, which is modeled by the CF reduction length dh and the increase of the effective AE thickness dl. CF height reduction rate dh/dt is controlled by the slower process between oxidation and hopping. If oxidation is the dominant process, the CF height reduction rate is described by

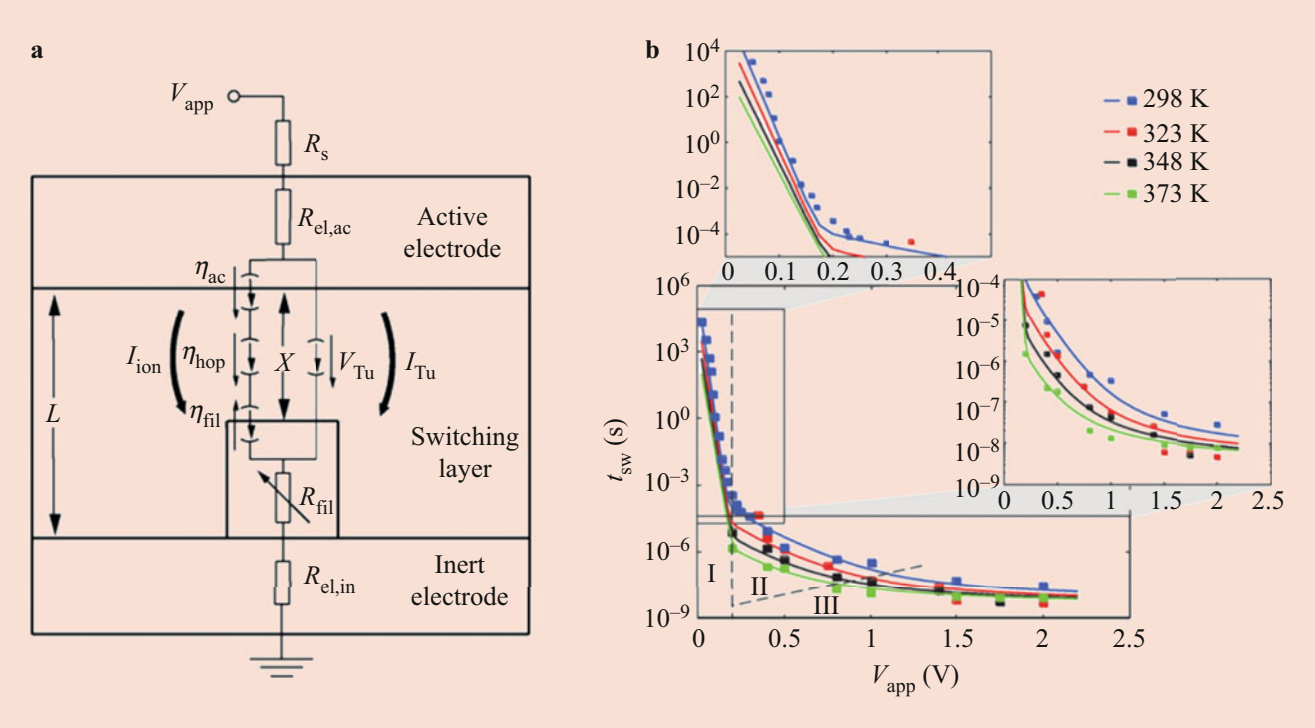


Fig. 29.29 (**a**) The equivalent circuit in the switching model, (**b**) transient SET switching kinetics of the AgI-based CBRAM for different ambient temperatures. (Reprinted from [70])

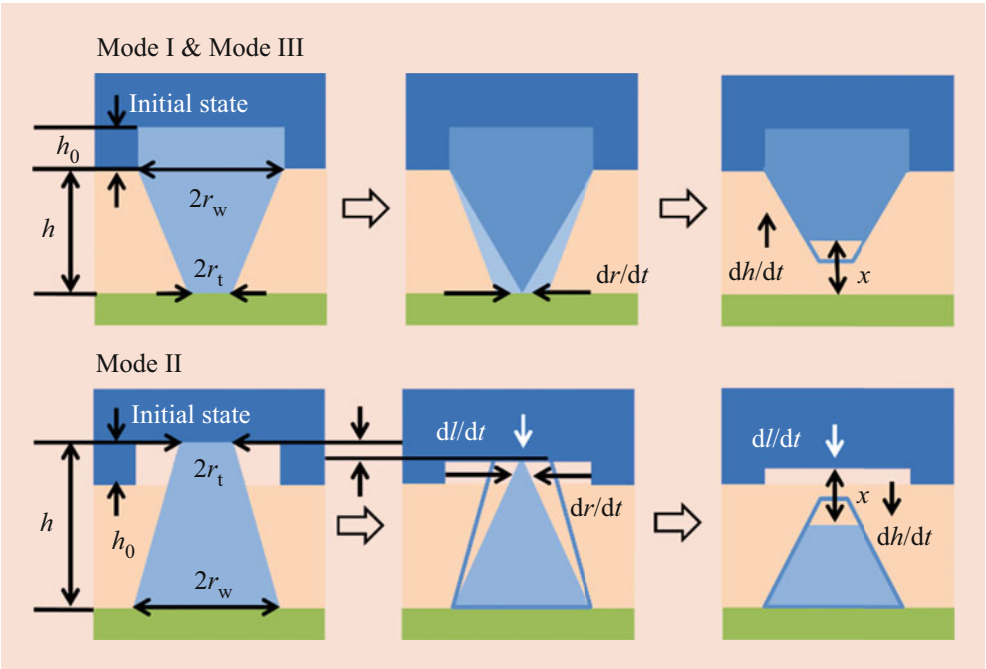


Fig. 29.30 Schematic of CF evolution model during RESET in different CF evolution modes. (Reprinted from [79])

$$\frac{\mathrm{d}h}{\mathrm{d}t} = af \exp\left(-\frac{E_{\mathrm{ox}} - \alpha_{\mathrm{o}} ZeE}{k_{\mathrm{B}} T}\right) \tag{29.49}$$

while when hopping is the dominant process, dh/dt follows

$$\frac{\mathrm{d}h}{\mathrm{d}t} = af \exp\left(-\frac{E_{\mathrm{h}}}{k_{\mathrm{B}} T}\right) \sinh\left(\frac{\alpha_{\mathrm{h}} ZeE}{k_{\mathrm{B}} T}\right) \tag{29.50}$$

and the variable dl/dt is decided by the competition between the reduction and hopping processes. The increased rate of effective AE thickness dl/dt is governed by

$$\frac{\mathrm{d}l}{\mathrm{d}t} = af \exp\left(-\frac{E_{\mathrm{red}} - \alpha_{\mathrm{r}} ZeE}{k_{\mathrm{B}} T}\right) \tag{29.51}$$

The narrowing rate of thin radius dr/dt which determines the RESET speed is modeled by the slower process between oxidation and hopping. When oxidation is the dominant process, dr/dt is described by

$$\frac{\mathrm{d}r}{\mathrm{d}t} = \frac{3f\Delta h}{h\,(2r_{\mathrm{t}} + r_{\mathrm{w}})} \sum_{i=0}^{h} \left(r_1(i)\Delta r + r_2(i)\Delta r - \Delta r^2\right) \exp\left(-\frac{E_{\mathrm{ox}} - \alpha_{\mathrm{o}} ZeE(i)}{k_{\mathrm{B}} T(i)}\right) \tag{29.52}$$

where Δh and Δr are parameters in the integrating process, r_1 and r_2 are the radii of the integrating cone, $E(i)$ is the local electric field, and $T(i)$ is the local temperature. When hopping is the dominant process, dr/dt is described by

$$\frac{\mathrm{d}r}{\mathrm{d}t} = \frac{3af}{h\,(2r_{\mathrm{t}} + r_{\mathrm{w}})} \sum_{i=r_{\mathrm{t}}}^{r_{\mathrm{w}}} \pi \left(r_2(i)^2 - r_1(i)^2\right) \exp\left(-\frac{E_{\mathrm{h}}}{k_{\mathrm{B}} T(i)}\right) \sinh\left(\frac{\alpha_{\mathrm{h}} ZeE(i)}{k_{\mathrm{B}} T(i)}\right) \tag{29.53}$$

where a is the distance between two atoms.

During SET process, a thin filament first connects AE and IE and then expands in the thin end as shown in Fig. 29.31, which is a reverse process of RESET. Compared with RESET, the dr/dt and dh/dt in SET operation are controlled by the slower process between reduction and hopping, and dl/dt is governed by the slower process between oxidation and hopping. When using the model, there is no need to presume in which mode the device is operating. Taking the material parameters and operation schemes as inputs, the model can automatically decide the CF evolution mode.

The compact model can reproduce the electrical characteristics in DC and AC operations, which are verified by experimental results with various material stacks. Figure 29.32a shows the measured and calculated DC I-V curves of the Cu/SiO_2/W during RESET and SET processes [79], where the abrupt switching can be accurately reproduced. By considering the parasitic effects such as the parasitic resistances and capacitance, the AC characteristics can be calculated by the model. Figure 29.32b is the calculated relationship between switching time and ambient temperature, which is in good agreement with experimental data from [85]. The physics-based compact model would benefit for the co-design of the device and circuit, serving as a powerful tool for the performance evaluation and optimization of the large-scale CBRAM array.

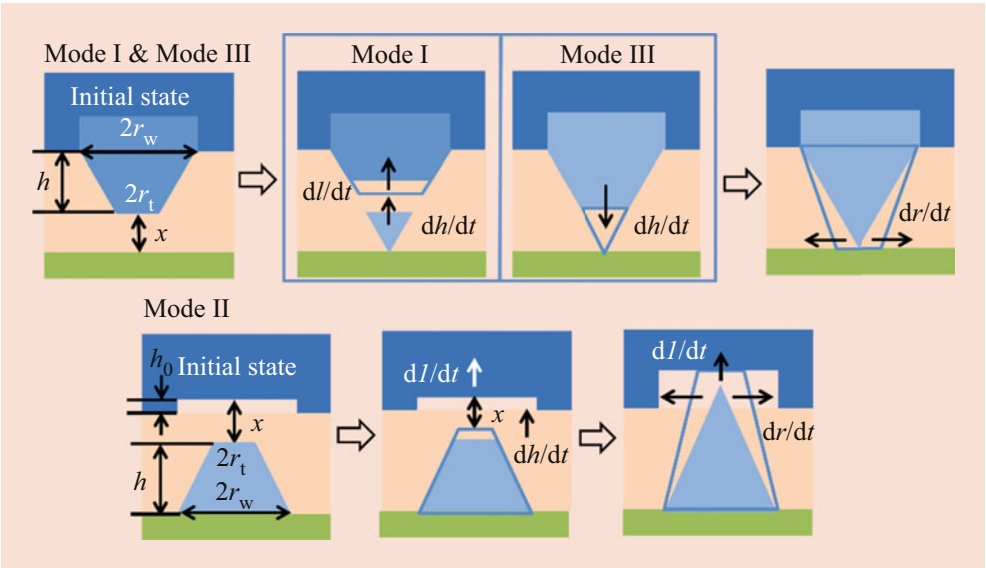


Fig. 29.31 Schematic of CF evolution model during SET in different CF evolution modes. (Reprinted from [79])

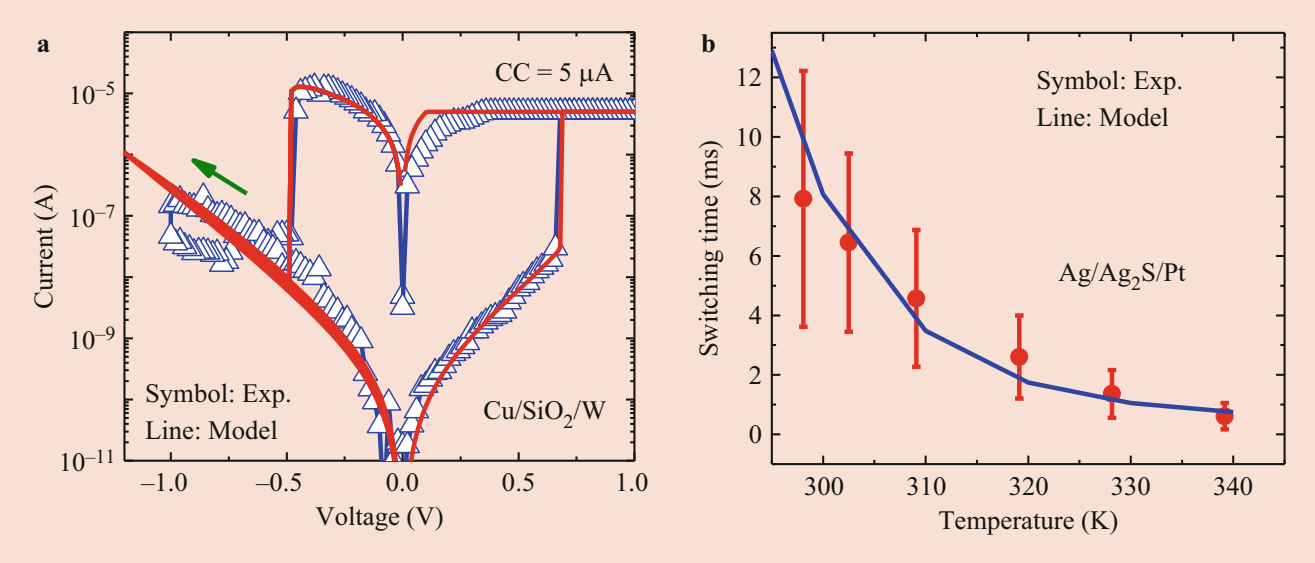


Fig. 29.32 (**a**) Comparison between the calculated DC I-V characteristics and measured data, (**b**) the model calculated dependence of switching time on temperature with the experimental data. (Reprinted from [39])

29.4 Array Design and Optimization

29.4.1 Crossbar Array

Unlike front-end-of-line (FEOL) eFlash/EEPROM, RRAM is a back-end-of-line (BEOL) memory and does not require revalidation of the existing circuit IPs due to its lower temperature integration process. Moreover, RRAM can achieve high-density integration due to its simple structure. Figure 29.33 shows the crossbar RRAM array with high-density integration. The array is composed of bit lines (BL) and word lines (WL), and every cross point of BL and WL is positioned with a RRAM device. To perform the read operation, a small voltage, such as 0.2 V, is applied on the WL of the selected cell, and the BL of the selected cell is grounded. Meanwhile the other BL and WL are floated, and the state of the cell is read out according to the current through the BL of the selected cell. Current difference (ΔI), which is obtained by reading R_{LRS} and R_{HRS}, is then sensed by connected sense amplifiers (SAs), which act as current-to-voltage converters, and thus, the resistance states can be detected in this way. An example of an SA is a simple current mirror or an operational amplifier with a feedback resistor to sense the current. The design of SAs is not a part of this chapter, and thus the peripheral sensing circuits are not introduced in detail. The BL of N cells can be simultaneously connected to CMOS sense circuits to increase the read speed. The voltage difference sensed by the CMOS circuit is defined as readout margin, which is one of the key parameters to characterize the read performance. To write the RRAM cell, the operation voltage is applied on the WL of selected cell, and the BL of selected cell is grounded. Meanwhile all other WL and BL are floated. The write operation of RRAM can also be performed in parallel like NAND flash.

Generally, the bias schemes for read and write operation are not workable due to the sneak current path as illustrated in Fig. 29.33. The sneak path causes the degradation of the readout margin and the misreading of the selected cell [86]. For write operation, the RRAM cell can't be switched and the unselected cell may be miswriting due to the sneak path. What's worse, these issues will be aggravated with the increase of array size. To mitigate the sneak current path, different bias schemes are proposed [87]. The most popular bias scheme is the "V/2" bias scheme for write and grounding bias scheme for read as illustrated in Fig. 29.34a, b. For "V/2" bias scheme, half of write voltage is applied on the BL and WL of the unselected devices to avoid the miswriting of unselected devices. However, the write disturbance is still not solved because about half of write voltage is applied on half self-selected cells. For grounding bias scheme, the BL and WL of the unselected cells are grounded to increase the readout margin. However, the energy consumption will increase for the read operation with grounding bias scheme. There are some other bias schemes for write operation, such as "V/3" bias scheme, in which 2/3 of the operation voltage is applied on the BL of unselected cells and 1/3 of operation voltage is applied on the WL of unselected cells. Consequently, the write disturbance can be effectively migrated because the voltage across the unselected cell decreases from V/2 to V/3.

Under the proposed bias scheme, the RRAM cells can be correctly read and wrote if the interconnect resistance is neglected. However, the interconnect resistance is usually comparable to the resistance of RRAM device, and it sharply

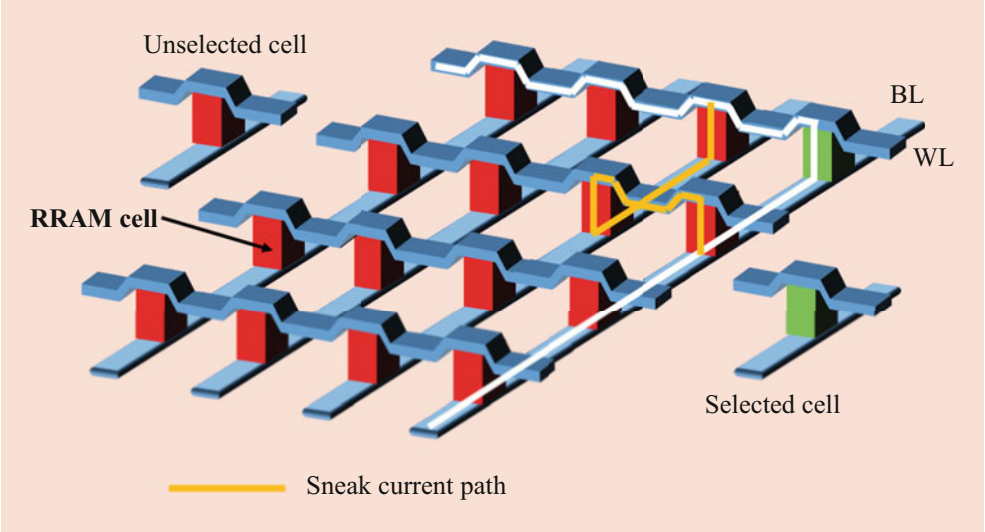


Fig. 29.33 Schematic show of the crosspoint RRAM array and the sneak current path

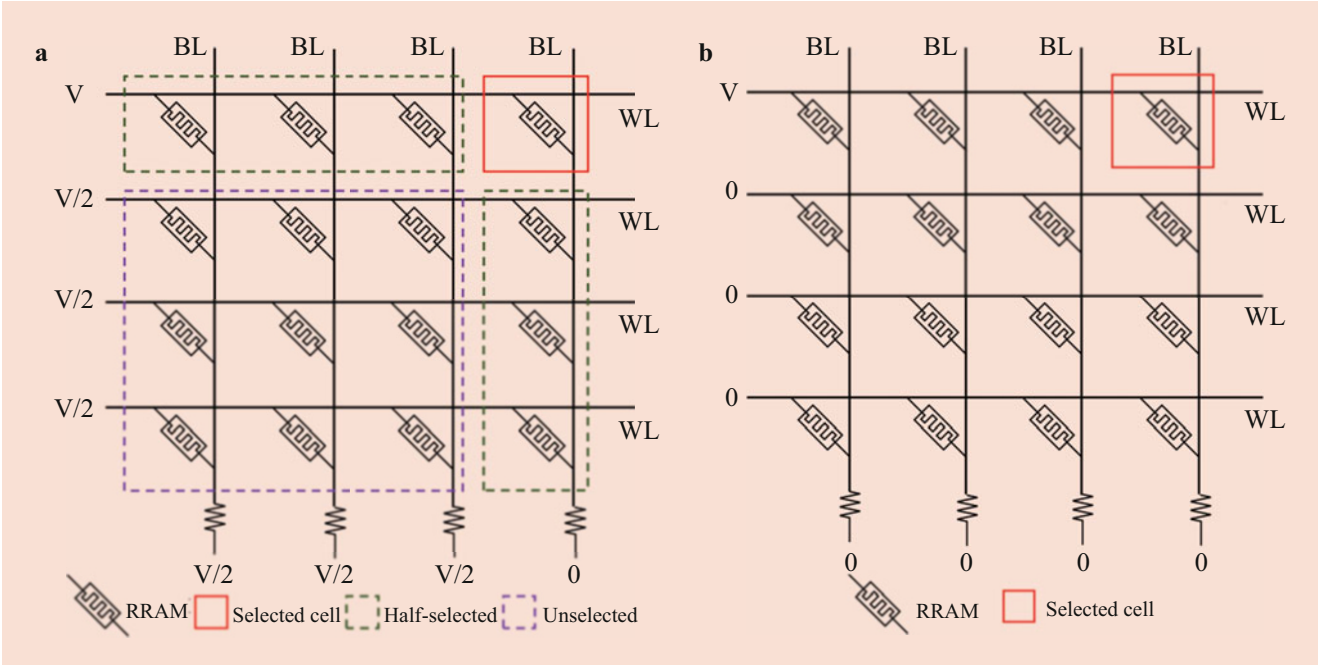


Fig. 29.34 Schematic illustration of (**a**) "V/2" and (**b**) grounding bias schemes

increases with the scaling down [88]. Therefore a selector device or highly nonlinear I-V characteristic for RRAM is required for the integration of crossbar RRAM array. Diode is the most common selector device, but it is useful only for unipolar. Unfortunately, the performance of unipolar RRAM is much worse than that of bipolar device; thus bipolar RRAM devices are widely used for the array integration. Transistor is another candidate for selector of RRAM. Up to now, most demonstrations of RRAM arrays are based on the 1T1R structure due to the nature of CMOS transistor process and the excellent behaviors as a selector without considering the scalability. A common 1T1R array structure is shown in Fig. 29.35. Generally, the RRAM cell is integrated with the drain terminal of transistor by bottom electrode. The gates of transistor in the same column are connected to the same WL, the source terminals of transistor in the same row are connected to the same source line (SL), and the top electrodes of RRAM in the same row are connected to the same BL. To read the selected cell, the high voltage is applied to the selected WL to turn on the selected transistor. Meanwhile, a small read voltage is applied to the selected BL, and the selected SL is grounded. The state of the selected cell is read

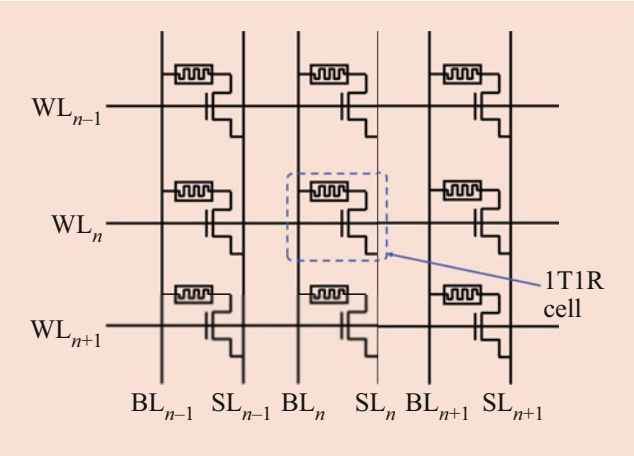


Fig. 29.35 Schematic diagram of the 1T1R RRAM array structure

out according to the current of selected SL. The sneak path is shut down since the transistors with unselected WL are all in turn-off state. To write the selected cell, the selected transistor is turned on by applying a high voltage on the selected WL. To SET the cell, the SET voltage is applied on the selected BL, and the selected SL is grounded. On the other hand, RESET voltage is applied on the selected SL, and the selected BL is grounded for the RESET operation. The transistor not only mitigates the sneak current path but also served as current compliance for SET operation. It seems that 1T1R array is a good choice for the integration of RRAM array. However, due to the intrinsic drawback of more than $8F^2$ cell size, the 1T1R structure cannot be scaled down to an ideal size. What's worse, 3D integration with 1T1R structure is hard. Therefore, a highly compact two-terminal bidirectional selector device is required for the high-density integration of RRAM array, which is discussed in the next section.

29.4.2 Selector Devices for RRAM Array

For the integration of RRAM array, the selector device should satisfy various technical requirements from both the array level and the individual RRAM cell. Firstly, the on-state current should be large enough to switch the RRAM cell, and the off-state current should be low enough to shut down the sneak path. Moreover, the fabrication process of the selector should be compatible with CMOS. It is better to be compatible with the BEOL process so that the RRAM array can be stacked three dimensionally [5]. Other specifications, such as cycling endurance, switching voltage, speed, etc., should also match with the RRAM cell.

Various attempts have been done to propose selector with different mechanisms and optimize its performance to reach the requirements. According to their IV characteristics and physical mechanisms, the proposed selectors can be roughly categorized into ovonic threshold switching (OTS) [89, 90], insulator-metal transition (IMT) [91, 92], mixed ionic-electronic conduction (MIEC) [93, 94], field-assisted superlinear threshold (FAST) [95, 96], tunneling [97], and Cu/Ag ionic selector [98]. The IV characteristics of OTS-, IMT-, MIEC-, and FAST-type selector are similar, where an abrupt increase of current can be observed at the threshold voltage (V_{th}) and abrupt decrease of current occurs when the voltage is smaller than the hold voltage (V_{hold}). Generally, the V_{th} is larger than the V_{hold}, and abs(V_{th}-V_{hold}) should be large enough to guarantee the switching of the RRAM cell. The mechanisms and material stacks of these four type selectors are different. The OTS depends on the phase change assisted by the joule heat or electrical field. The IMT relies on the insulator-metal transition of material, such as NiOx. MIEC and FAST as well as Cu/Ag ionic selectors are correlated with the movement of fast metal ion, such as Cu. However their details have some differences which are still under debate. The tunnel selector is utilized the Schottky barrier to achieve the rectifying effect. Table 29.2 summarizes the representative development for each type of selector together with their key characteristics. It can be found that all on/off ratio for the selectors is larger than 10^6, which is enough to build a crossbar RRAM array with size >10 M [86]. The on-state current of most selector is above 1 MA/cm^2, which can switch RRAM with 100 μA operation current when the feature size is 100 nm. Moreover, the operation voltage is optimized within a reasonable range. Other features such as off-state current, switching speed, and endurance also match with the mainstream RRAM cell.

Among these selectors, the FAST selector seems to be one of the most promising candidates and has been demonstrated by different groups [99, 100]. So we will introduce the FAST selector in detail next. In 2014, S. H. Jo et al. proposed a superlinear threshold layer-based selector, in which a conduction path is formed at the threshold electric field and the conduction path is dissolved when the electric field is below a value. Figure 29.36 shows its I-V curve with extremely sharp switching slope <5 mV/Dec, which is beneficial to the read and write operation of RRAM array. Moreover, the on/off ratio is larger than 10^7, which can shut down the sneak path. The threshold voltage of FAST selector is about 1 V and can be tuned by controlling either the STL thickness or device structure as discussed in [95, 96]. Additionally, the variability of threshold voltage is about 0.075 V, which is very important for integration of 1S1R RRAM array. The cycle-to-cycle performance of the selector exhibits good uniformity. The selector can reliably switch over 100 M cycles as shown in Fig. 29.37a. The selector can't switch under a disturbance of constant DC at half of threshold voltage for 2 h. Once the voltage applied on the FAST selector exceeds the threshold voltage, the FAST selector will turn on in 30 ns. The FAST selector can recover to the off state in 5 ns after removing the

Table 29.2 Various types of selectors with their key characteristics

Selector type	OTS [90]	IMT [91]	MEC [93]	FAST [95]	Tunneling [97]	Cu/Ag ionic [98]
Stack	TiN/AsTeGeSiN/TiN	TiN/NbOx/W	Cu:TE/$CuSGeSe_6$/Cu:BE	TE/FAST/BE	Pt/TaO_X/TiOx/TaO_X/Pt	Cu/Cu:HfO_2/HfO_2/Pt
On/Off ratio	10^4	10^3	10^7	10^7	10^4	10^7
V_{on}	2–3	~1.2	~0.8	~1	~0.8	~0.4
J_{on}(MA/cm^2)	11	10	50	5	10	4
V_{hold}	NA	~0.2	NA	~0.2	NA	~0.2
I_{off}(A)	10^{-6}	10^{-5}	10^{-8}	10^{-11}	10^{-10}	10^{-12}
Speed(ns)	1000	50	15	30	NA	50
Endurance	10^8	10^6	10^8	10^8	10^{10}	10^{10}

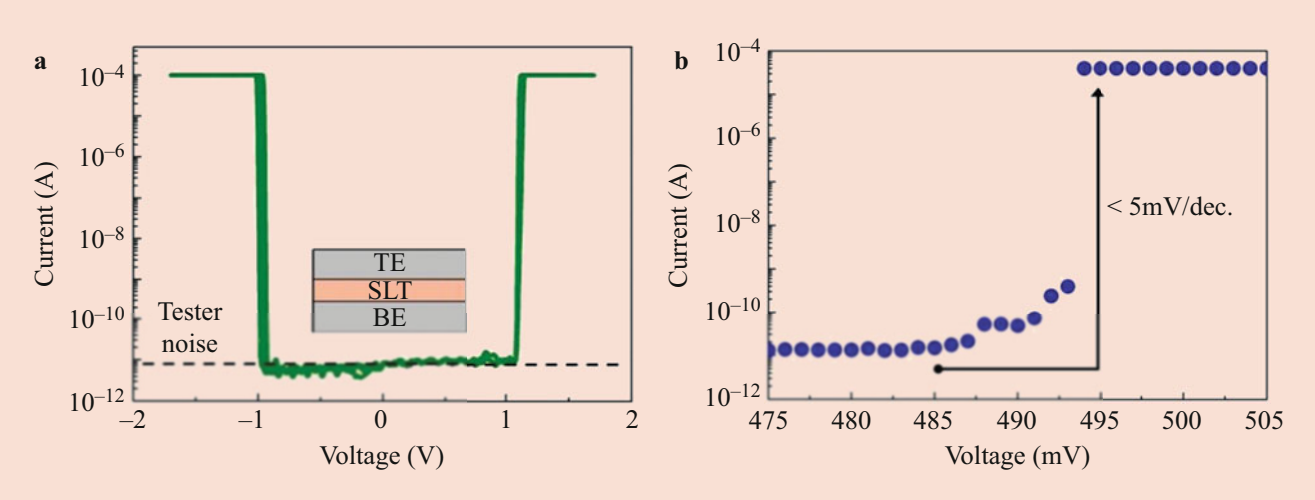


Fig. 29.36 (**a**) I-V characteristics of FAST selectors (100 nm × 100 nm). The device shows bidirectional threshold switching with larger than 10^7 on/off ratio. (**b**) Zoomed-in plot showing the turn on slope of the FAST selector. (Reprinted from [95])

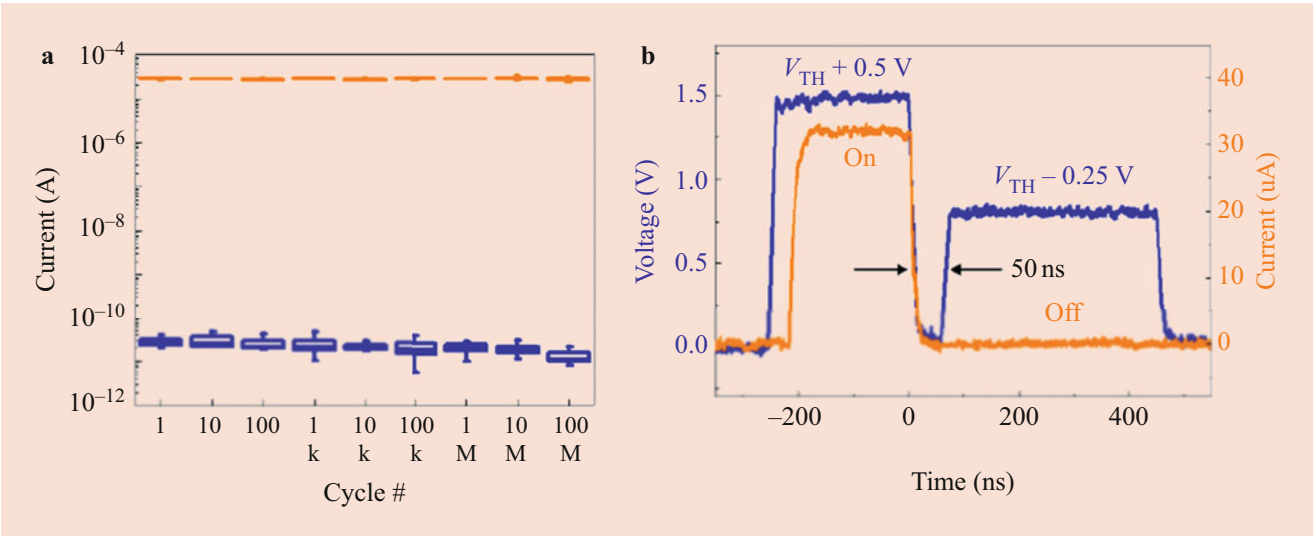


Fig. 29.37 (**a**) Cycling test of FAST selectors. The selectors can be reliably cycled over 100 M cycles which is limited by the test. (**b**) Switching speed of a FAST selector. The selector can be turned on within 30 ns in response to a 2 V pulse. Off-to-on transition time is about 5 ns for over 300 μA of passing current through the selector. (Reprinted from [95])

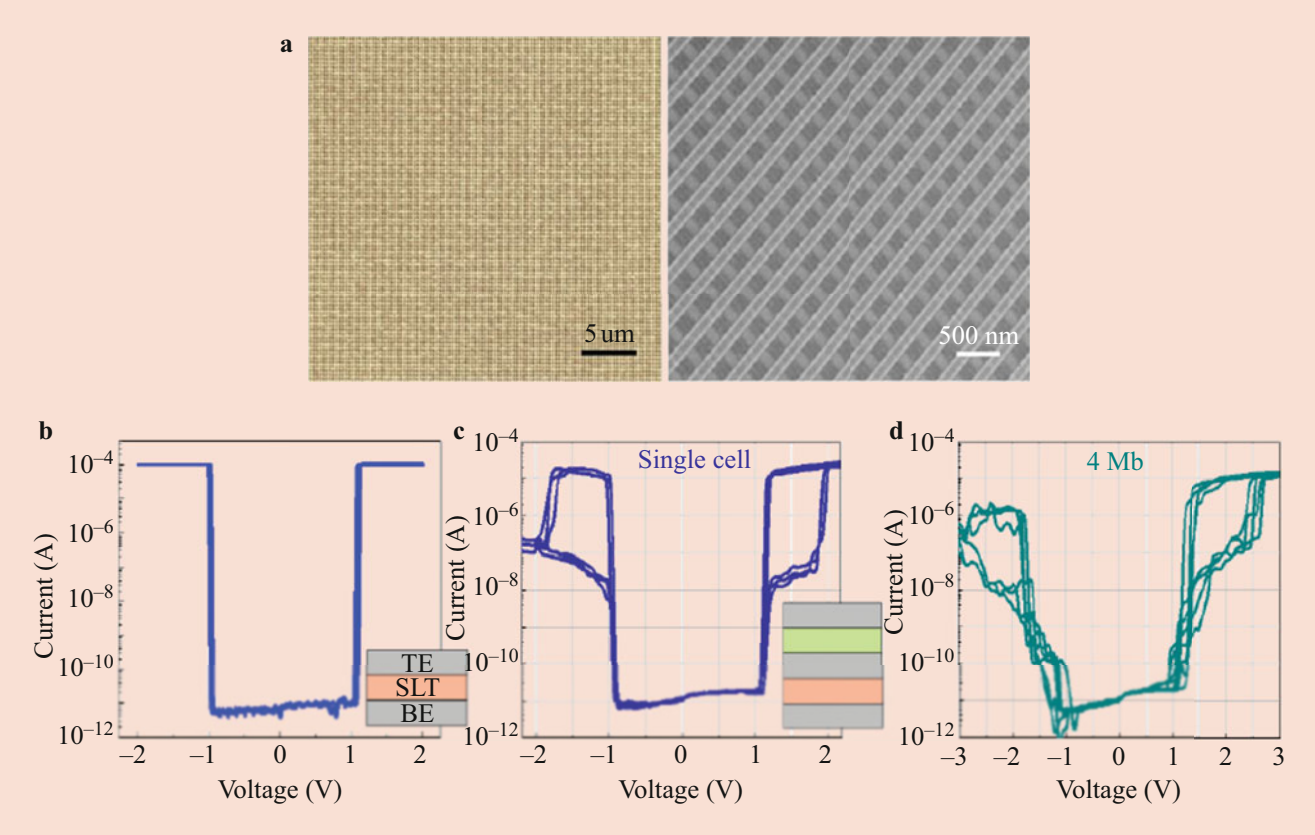


Fig. 29.38 Passive crossbar array integration of FAST selectors. (**a**) Images of the fabricated selectors. I-V characteristics of (**b**) selector, and (**c**) integrated 1S1R device. (**d**) I-V characteristics of 1S1R device in 4 Mb passive crossbar array. (Reprinted from [95])

applied voltage. Hence, the switching speed of FAST selector is less than 50 ns as shown Fig. 29.37b. The hold voltage of the FAST selector is smaller than 0.3 V for 300 uA on-state current, and it decreases with the on-state current.

S. H. Jo et al. also integrated the FAST selectors with RRAM for a 4 Mb passive crossbar array as shown in Fig. 29.38. The sneak current of single FAST selector is below 0.1 nA at both 25 °C and 125 °C with high device yield. In addition, the integrated RRAM is Forming-free with a low switching current. Hence, the IR drop of voltage and power consumption will decrease. The threshold voltage of the fabricated selectors is larger than half of RESET and SET voltage but smaller than RESET and SET voltage as shown in Fig. 29.38b. Such the sneak path can be suppressed during both the read and write operations. The integrated single 1S1R device shows $>10^2$ memory on/off ratio and $>10^6$ selectivity as shown in Fig. 29.38c. The 1S1R device in the 4 Mb crossbar array can also correctly switch as shown in Fig. 29.38d. In addition, it can reliably switch more than 100 K cycles with pulse operation. The designed and fabricated FAST selector shows a promising prospect of high-density RRAM array integration.

29.4.3 3D Integration

Although current RRAM is hard to replace 3D NAND flash in terms of existing technology, it is still one of the most promising candidates for the 3D high-density-integrated storage class memory to fill the speed and capacity gap between the DRAM and NAND flash memory in the current memory hierarchy [5]. Three possible approaches were proposed for 3D integration of RRAM. One is the 3D horizontal stacking RRAM array (HRRAM) architecture [101], in which 2D crossbar array is vertically stacked layer by layer as shown in Fig. 29.39a. This architecture has many attractive advantages in lateral scaling, and its process is more mature. Unity demonstrated a 64 Mb HRRAM test chip built with 0.13 μm technology [102]. SanDisk demonstrated a two-layer 32 Gb crossbar chip by 24 nm process, in which the memory cell is 1D1R structure [42]. However, the lithography steps will linearly increase with the number of layers as shown in Fig. 29.39b, which means a linearly increasing cost of fabrication [40].

To further decrease the cost, 3D vertical RRAM (VRRAM_1) architecture is proposed as shown in Fig. 29.39c

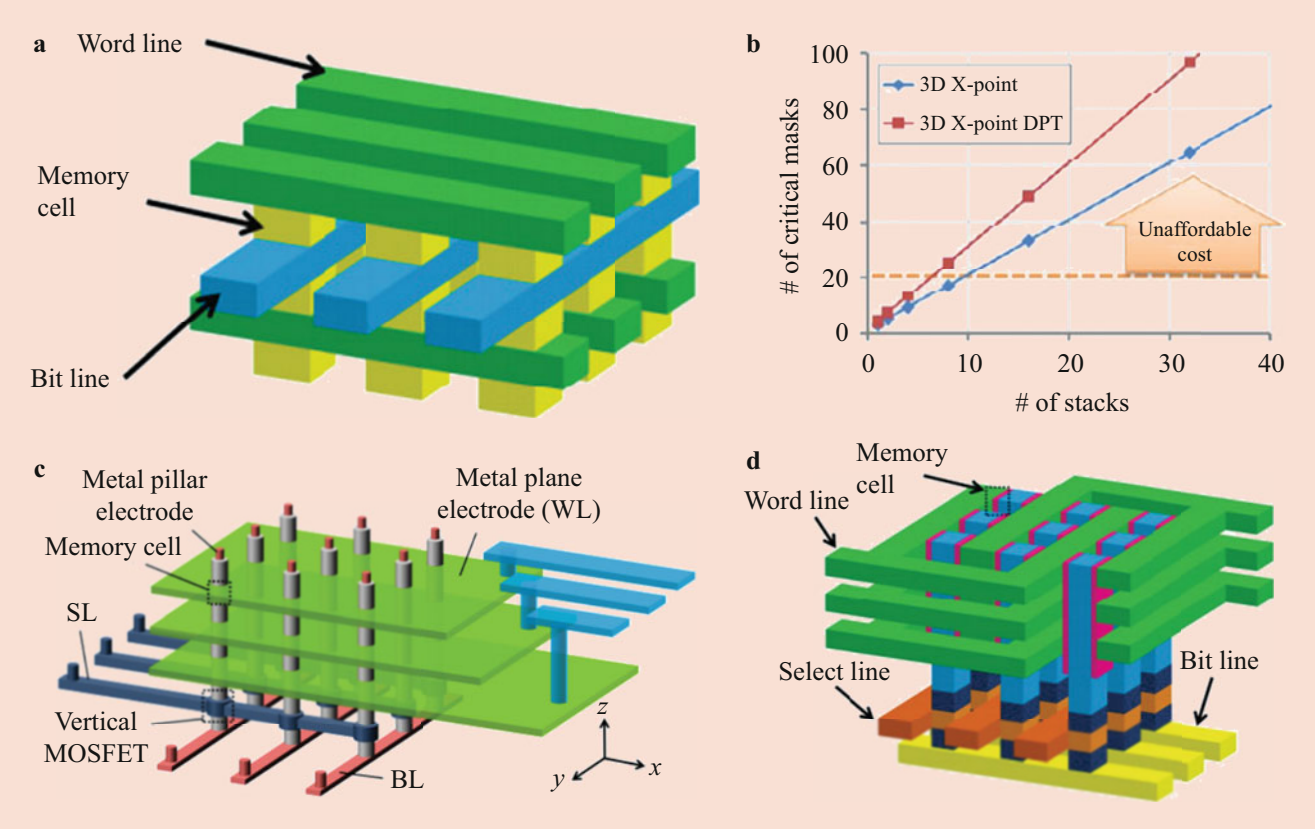


Fig. 29.39 (**a**) The schematic of 3D horizontal stacking RRAM array (HRRAM). The memory cell is located at the intersection between bit line and word line. (**b**) Minimum number of critical masks necessary for 3D horizontal stacking arrays as a function of stacked layer number. (**c**) The schematic of 3D vertical RRAM array (VRRAM_1). The RRAM cell is located at the intersection between pillar electrode and metal plane electrode. (**d**) The schematic of 3D vertical RRAM array (VRRAM_2). (Reprinted from [39, 40, 103])

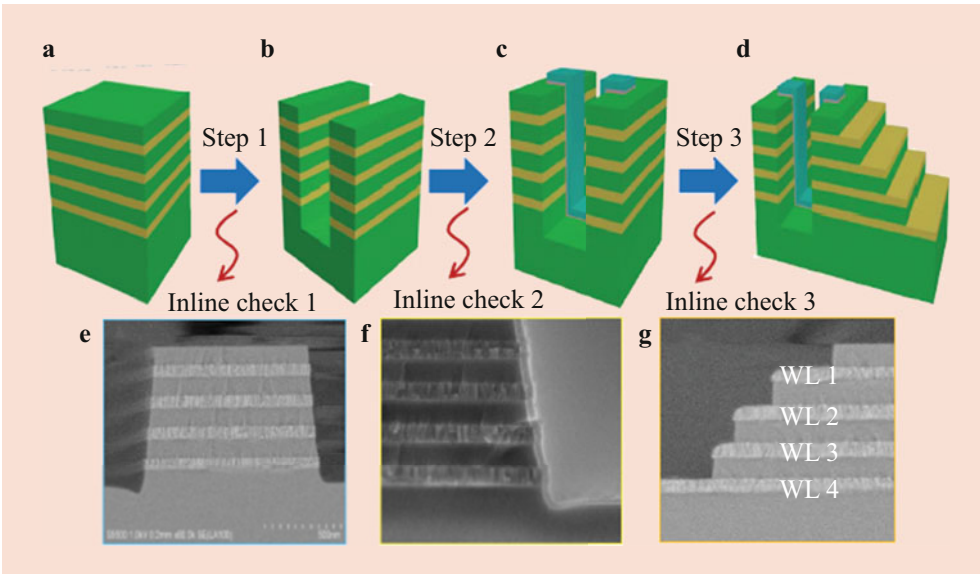


Fig. 29.40 (**a**)–(**d**) The integration process flow of 3D integration of VRRAM_2. (**e**)–(**g**) The inline check at each step of the process flow. (Reprinted from [105])

[39]. The memory cell is located between the plane electrode and the vertical pillar, which is similar to bit-cost-scalable 3D NAND. Thanks to simple one-step pillar fabrication process, this vertical 3D structure only requires one to three critical lithography steps regardless of the layer number. In addition, the IR drop will decrease due to the ultralow interconnect resistances of the metal plane and vertical metal pillar with core-shell structure. To further increase the density, another

vertical RRAM (VRRAM_2) structure is proposed by dividing the plane electrode into line electrodes with a single additional etch step as shown in Fig. 29.39d [104]. The memory cell is located between the horizontal odd/even metal word line and vertical pillar. Comparing with VRRAM_1, the leakage current path of VRRAM_2 is decreased. Therefore the energy consumption of write or read operation will decrease.

If the selector is required for these two structures, the array density may decrease due to thickness of selector. Therefore thin selector or RRAM cell with self-rectifying characteristics is more suitable for these structures. As feature size scaling down to <20 nm, the intermediate electrode would shorten the cells in the same pillar, leaving behind the self-rectifying as the only choice to prohibit the sneaking current. Luo et al. proposed a four-layer VRRAM_2 structure array by combining HfO_x resistive layer and MIEC selector layer [105]. The fabricated process of the four-layered VRRAM_2 is schematically shown in Fig. 29.40a–d. Firstly, TiN (60 nm)/SiO_2 (100 nm) layers were deposited layer by layer by PVD and PECVD. Then one-step etching was applied to form the WL after the patterning. Following is the deposition of resistive switching and selector layer HfO_2/CuGeS along the sidewall. Lastly, the top electrode was deposited on the sidewall by magnetron sputtering at room temperature, followed by lift-off process to form BL. The SEM images of inline checks for each step are shown in Fig. 29.40e–g. It can be found that profile of the sidewall is smooth, which can avoid the coverage issue and point discharge problem during write operation. Figure 29.41a shows the transmission electron microscopy (TEM) image and the spectrum of EDX line scan over the cross section of the device. Well-distinguishable layers with interface can be clearly observed. The EDX shows small amount of O signal overlap with the TiN layer, which implies that a thin TiON has formed between the TiN top electrode and HfOx layer. Figure 29.41b shows the I-V characteristic of 1S1R cell, which shows stable resistive-switching behavior and high selectivity. The SET voltage is about −3.5 V, and the RESET voltage is 6 V, which decreases with the thickness of CuGeS as shown in the set of Fig. 29.41b. The nonlinearity of LRS is larger than 10^3 with 1 V selective voltage due to the threshold switching characteristics of CuGeS layer. In addition, the operation current of the device is sub-nA with self-compliance characteristics, which is beneficial to increase the access voltage during the write operation. Figure 29.42a shows the typical.

I-V characteristics of the 1S1R cells of different layers in the VRRAM_2 array. The cells of each layer device exhibit similar stable and self-selective switching behavior. The distributions of the program (SET) and selective voltages are shown in Fig. 29.42b. The average voltage window is about 1 V, which can guarantee the correction of the read operation. The fabricated 1S1R cell can switch for more than 10^7 cycles with sub-μs pulse operation as shown in Fig. 29.42c. Figure 29.42d is the retention behaviors of LRS/HRS at different read voltages, which is stable for more than 10^4 s at 85 °C. Although four layers of the 1S1R RRAM array have been demonstrated with accepted performance, it is still far from replacing the 3D VNAND as the standalone memory.

29.5 Applications

29.5.1 Embedded Memory

Although RRAM is difficult to replace the 3D VNAND in the standalone storage case, it may be suitable for embedded memory due to its CMOS compatibility, low operation voltage, satisfactory endurance, and retention. Unlike FEOL eFlash/EEPROM, RRAM can be easily integrated into the CMOS process with limited additional masks. H. W. Pan et al. have proposed and demonstrated 1Kb FinFET RRAM in pure 16 nm FinFET CMOS logic process by utilizing the dielectric as the resistive-switching layer in 2015 [106]. The operation voltage of RRAM is smaller than 3 V, which means the charge pumps circuit can be simplified. In addition, sub-nm RRAM has been demonstrated, indicating the high scalability of RRAM [38].

A lot of effort has been done to develop various BEOL integration schemes by different researchers. In 2008, Z. Wei et al. fabricated an 8 kbit 1T1R memory array with long retention and high endurance using the standard 0.18 μm CMOS process [16]. RRAM is integrated between M2 and M3 by reactive RF magnetron sputtering using a Ta target in the oxygen environment. In 2012, S.-S. Sheu proposed an embedded mega-bit scale (4 Mb) TiN/TiOx/HfOx/TiN RRAM macro with sub-8 ns read-write random access time using 0.18 μm CMOS technology [107]. The RRAM can operate with sub-8 ns read-write speed in binary and 160 ns write speed for multilevel storage, respectively. In the same year, W. C. Shen et al. developed a high-density RRAM cell with a very small 35 nm × 35 nm contact hole realized in pure high-k metal gate 28 nm CMOS logic process [108]. No extra mask or process step is required for the fabrication of the RRAM cell by depositing in the patterned drain contact hole. Therefore, it is the most economical way to integrate the RRAM into CMOS circuit. The fabricated device can switch more than 1 M cycles together with the stable data retention. In 2015, M. Ueki et al. developed a high-speed and low-power 2 Mb ReRAM with macro-practical memory window for 10 years ranging from −40 to 85 °C in 90 nm CMOS platform [109]. The thin RRAM cell structure is integrated between M1 and M2 by the plasma oxidation of Ta with Ru as the BE. In 2016, C. H. Ho et al. fabricated 1 Mb HfO_2-RRAM between the M1 and M2 only with two extra masks between

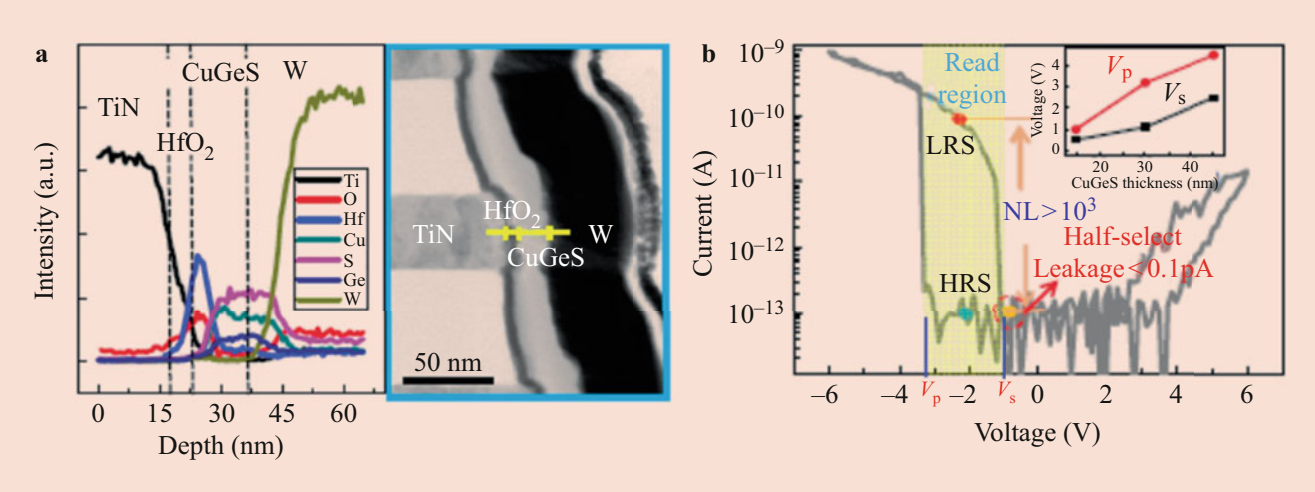


Fig. 29.41 (**a**) TEM image and EDX line scan over the TiN/HfO_2/CuGeS/W cross section of the 1S1R cell. (**b**) Typical I-V curve of the fabricated 1S1R cell. (Reprinted from [105])

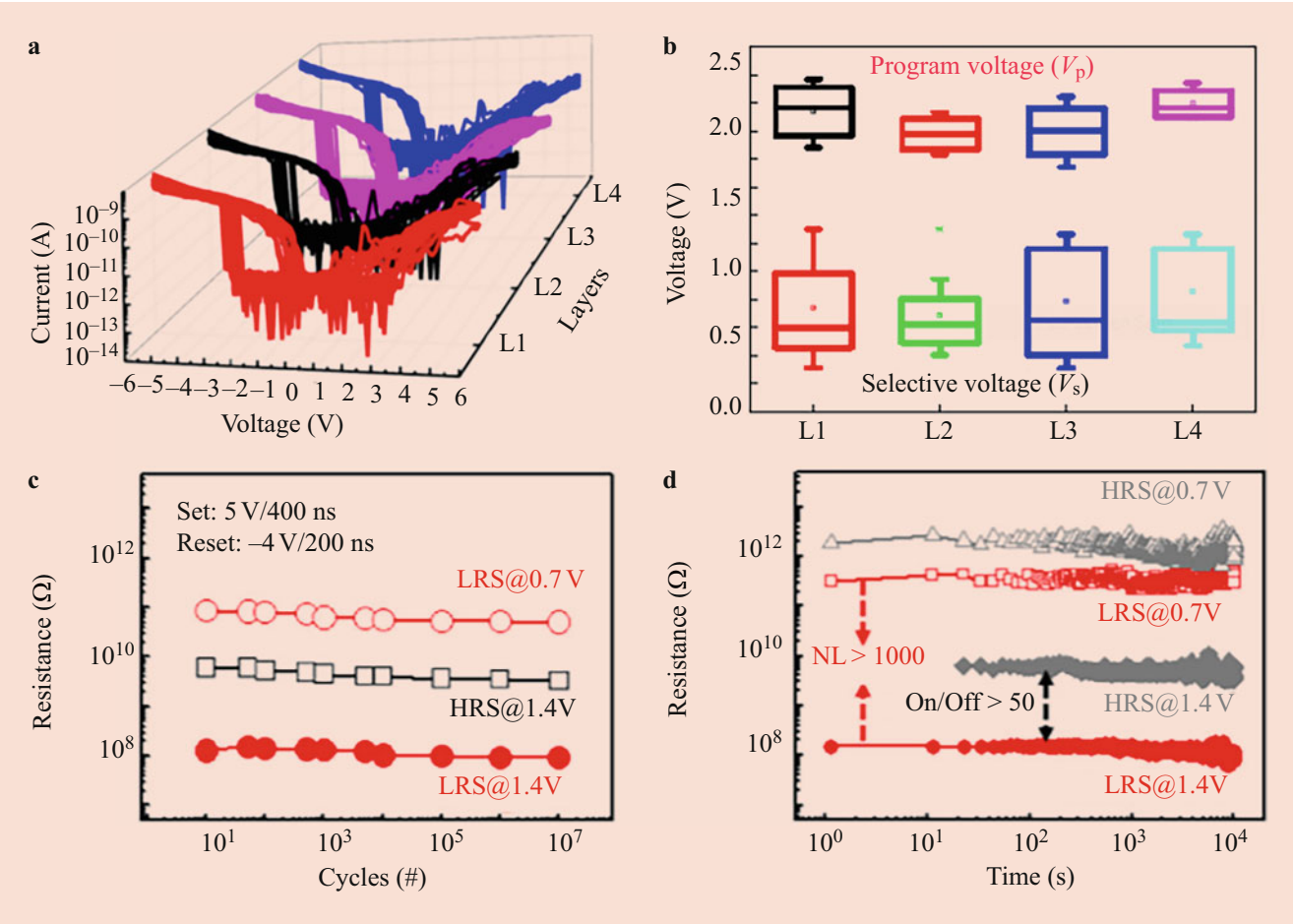


Fig. 29.42 (**a**) The I-V curves and (**b**) program (SET) voltage distributions of 1S1R cell in different layers. (**c**) The endurance and (**d**) retention behaviors of the 1S1R cell. (Reprinted from [103, 105])

metals for BEOL thermal stress immunity by 90 nm CMOS fully compatible process [110]. The resistive-switching layer is deposited by atomic layer deposition (ALD), and other layers are deposited by standard PVD processes. Reliable 20 k endurance and 85 °C 10-year retention are achieved by the stoichiometric engineering. The array offers potential applications of embedded IoT systems due to energy consumption reduction (80%) and cost-effective benefit (50% area) compared with eFlash.

In 2014, D. C. Sekar et al. proposed a low-power and robust 256 kb TiN/conductive TaO_X/HfO_2/TiN RRAM chip by controlling the capacitive surge currents during write operation. Generally, the SET and Forming process of RRAM is abrupt due to current overshoot even though the current is limited by the integrated transistor. The current overshoot mainly results from the discharge of the capacitive current as shown in Fig. 29.43a. When the applied voltage on the top electrode decreases from SET voltage to zero, the charge stored on the capacitance of RRAM will discharge via the CF and lead to the over-growth of the CF and high RESET current. To mitigate the overshoot current, a conductive metal oxide electrode (TaO_X) is introduced with optimized bulk resistivity of the TaO_X layer. It can achieve ~33% lower worst-case RESET current and 23× less fail bit count. Since the TaO_X layer can prevent heat flow and increase the temperature of CF as shown in Fig. 29.43b, the RESET voltage does not increase much despite the increase of IR drop due to the TaO_X layer. In addition, a write scheme is proposed and designed as shown in Fig. 29.43c, and the gate voltage of the selected transistor is biased near threshold voltage to limit the overshoot current. To overcome the mismatch between T1 and T2, transistor T3 and T4 are added to form the overshoot current for the current mirror. Forty percent reduction in RESET current is obtained by implementing the proposed circuit to the 256 kb RRAM array as shown in Fig. 29.43d.

The current available industrial solutions of RRAM for production mainly focus on the embedded memory application. The Panasonic Ox-RRAM processes are already available to be embedded with CMOS logic technology. In 2017, Panasonic introduced TaO_X-RRAM integrated into its 130 nm MCU product line and cooperated with foundry United Microelectronics Corporation to develop a 40 nm process, which is the first to start mass production in the industry [111]. In 2020, Panasonic announced a multifunctional secure IC that protects critical data on IoT and industrial devices by using 256 K 40 nm embedded RRAM as the memory which is highly resistant to radiation [112]. TSMC is also developing embedded RRAM for mass production. 40 nm ULP embedded RRAM has begun risk production at the end of 2017 and has completed consumer-grade qualification test for 10,000 cycles of endurance in 2018 [113]. The TSMC embedded RRAM technology is fully CMOS compatible for PDK and IP reuse for applications such as wireless MCU, IoT, and wearable devices. The CrossBar company developed the 40 nm RRAM process, both as a standalone memory and as an embedded memory. In 2018, CrossBar announced collaboration with Microsemi Corporation to integrate CrossBar's embedded RRAM in Microsemi products manufactured at the 1× nm node [114]. The Adesto company brought commercial RRAM devices to market with its trademarked CBRAM technology, and in 2018, European Solid-State Device Research Conference indicated the RRAM potential as embedded NVM for high-reliability applications such as automotive [115]. Adesto estimated that, compared to existing commercial-grade embedded NVM at 55 nm, the product using a 55 nm automotive-grade CBRAM macro could save 5–20% cost per die. In 2019 Symposia on VLSI Technology and Circuits conference, Intel announced an industry-leading combination of RRAM-based embedded NVM and 22FFL FinFET technology [116]. 22FFL is an ultra-low power and high performance technology for mobile and RF applications. It provides extensive high-voltage, high design flexibility, analog support, and low manufacturing costs. Embedded RRAM achieves 10^4 cycle endurance, 85 °C 10-year retention, and high die yield on 7.2 Mbit arrays and full 300 mm wafers.

29.5.2 Computing in Memory

In the conventional computing system, the computing unit and memory unit are separated. It leads to the huge energy-hungry and time-consuming data movement, called von Neumann bottleneck. To meet the requirement of future information evolution, developing energy-efficient parallel information processing systems beyond von Neumann architecture is highly desirable. RRAM can execute the logic operation and store the logical output in the same physical location [21, 117], which is a promising solution to overcome the von Neumann bottleneck.

The first proposal of computing based on RRAM is in 2010 by HP Inc., called stateful logic [21]. The basic logic operation demonstrated by HP Inc. is the implication (IMP), which is a university logic operation. The sub-circuit to execute the IMP logic operation is composed of two RRAM devices, P and Q, and one resistor (R_G), as shown in Fig. 29.44a. The bottom electrodes of device P and Q are connected by a common line, which is grounded via a resistor. The resistance state stored in the RRAM devices is the logical value. Two voltage pulses, V_{COND} and V_{SET}, are simultaneously applied to the top electrodes of P and Q, respectively, to trigger the logic operation. The output of logic operation is stored in the RRAM device Q after the operation. The magnitude of V_{SET} is little larger than the SET voltage, and the V_{COND} is half of V_{SET}. The resistance of R_G is chosen such that

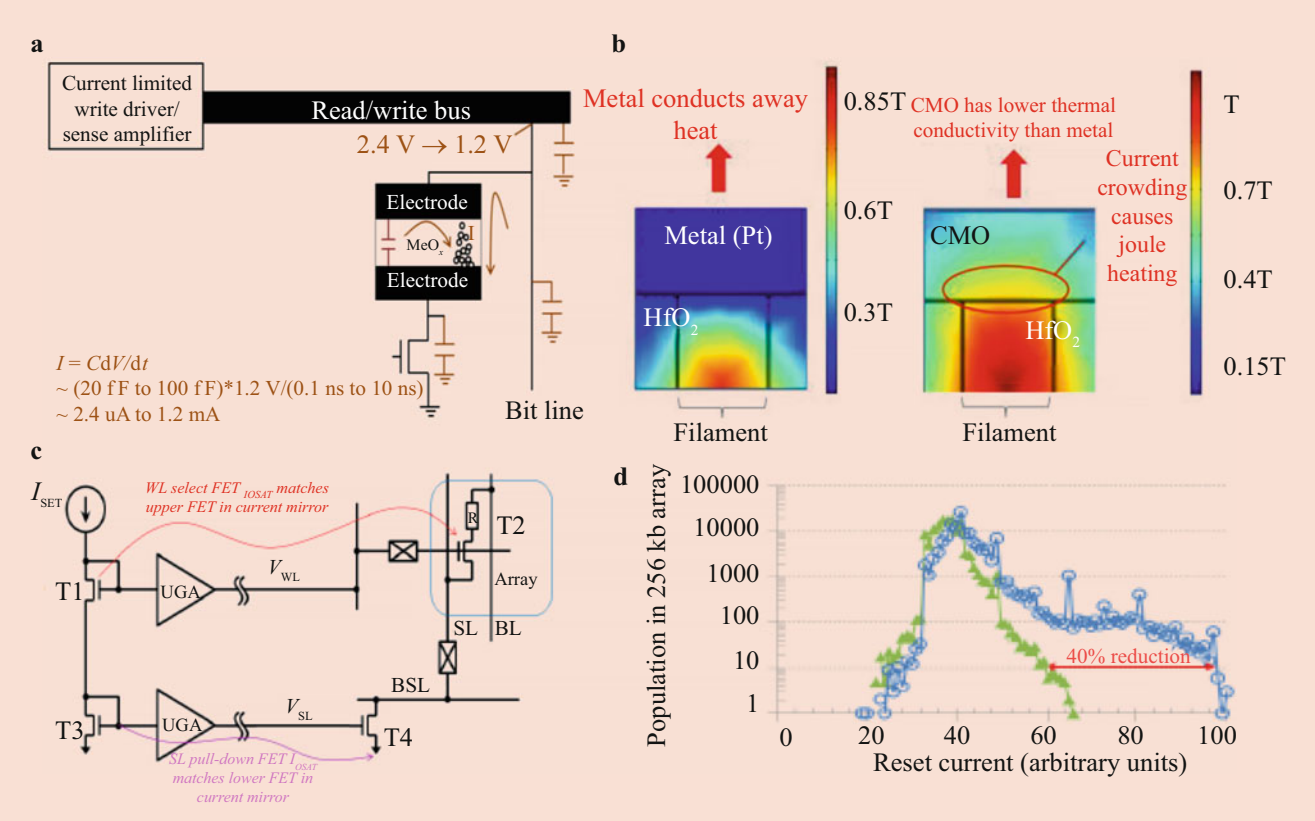


Fig. 29.43 (**a**) Overshoot current in 1T1R cell. (**b**) Simulation of the temperature distribution in the device with/without TaO_X layer for the same write current. (**c**) Proposed peripheral circuit for mitigating the overshoot current. (**d**) RESET current distributions for a 256 kb RRAM array. (Reprinted from [117])

$R_{LRS} < R_G < R_{HRS}$. If the initial state of Q (q) is LRS, it will not be switched regardless of the state of P (p). Q will be switched according to the p when the q is HRS. If p is HRS, it has little influence on the voltage divider formed by Q and R_G, and thus Q is SET to LRS. But if p is LRS, the V_{COND} pulse on P "shorts out" the voltage divider, and Q remains unchanged. During the operation process, the voltage across the P is not enough to change the state regardless of states of Q and P. We define the HRS as logical value "1" and LRS as logical value "0." The logical relation between the Q and P is summarized in Fig. 29.44b. It can be found that the IMP logical operation is performed, which can be experimentally demonstrated [21]. Other arbitrary logic computations can be performed based on the proposed logic operation. For example, NAND logic operation can be executed in three sequential steps by a circuit with three RRAM devices. However, the initial state of Q is covered during the logic operation, which hinders the logic cascading. Moreover, if the initial of Q is useful in the subsequent operation, a copy operation is required [118], which increases the computational time.

P. Huang et al. proposed a method to execute NAND and AND logic operations via resistance state interaction in one step without covering the input values in [26]. Figure 29.45a shows the sub-circuit to execute the NAND operation, where TE of the RRAM devices is connected by a common WL. A large voltage pulse is applied to the WL via a reference resistor (R_G), and a small voltage pulse is applied to the BL of devices A and B. The BL of device Y is grounded. Inputs are the resistance states of devices A and B, and the output logic

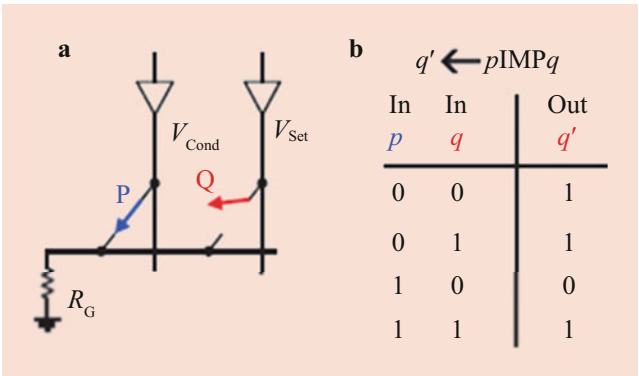


Fig. 29.44 Illustration of the IMP logic operation based on the RRAM. (**a**) IMP is performed by two simultaneous voltage pulses, V_{COND} and V_{SET}, applied to switches P and Q, respectively, to execute conditional toggling on Q depending on the state of switch P and Q. (**b**) The truth table for the IMP operation. (Reprinted from [21])

state will be stored into device Y after logic operation. The output device Y is initialized to HRS before the operation. Here we defined the HRS as logical "1" and the LRS as logical "0." If the input devices A and B are both logical "1," the potential of common WL is more close to V_{DD}, and the output device Y will be programmed to logical "0" after logic operation. If any input devices are logical "0," the potential of common WL is more close to V_R; thus the output device will still be in logical "1" after the logic operation. In this case, a NAND logic operation is performed. To guarantee the validation of the NAND logic operation , the V_R, V_{DD}, and R_G should be carefully selected. The magnitude of V_{DD} should be larger than the SET voltage to compensate the voltage drop across the R_G. Because the voltage across the input device can be close to V_{DD}-V_R, V_R should be large enough to not switch logic inputs. Meanwhile, the V_R should be small enough not switch the device Y. Therefore, the V_R is chosen to $V_{DD}/2$. Roughly, R_G can be selected as the $(R_{LRS}R_{HRS}/2)^{0.5}$. More detailed discussion about the selection of R_G can be found in [26].

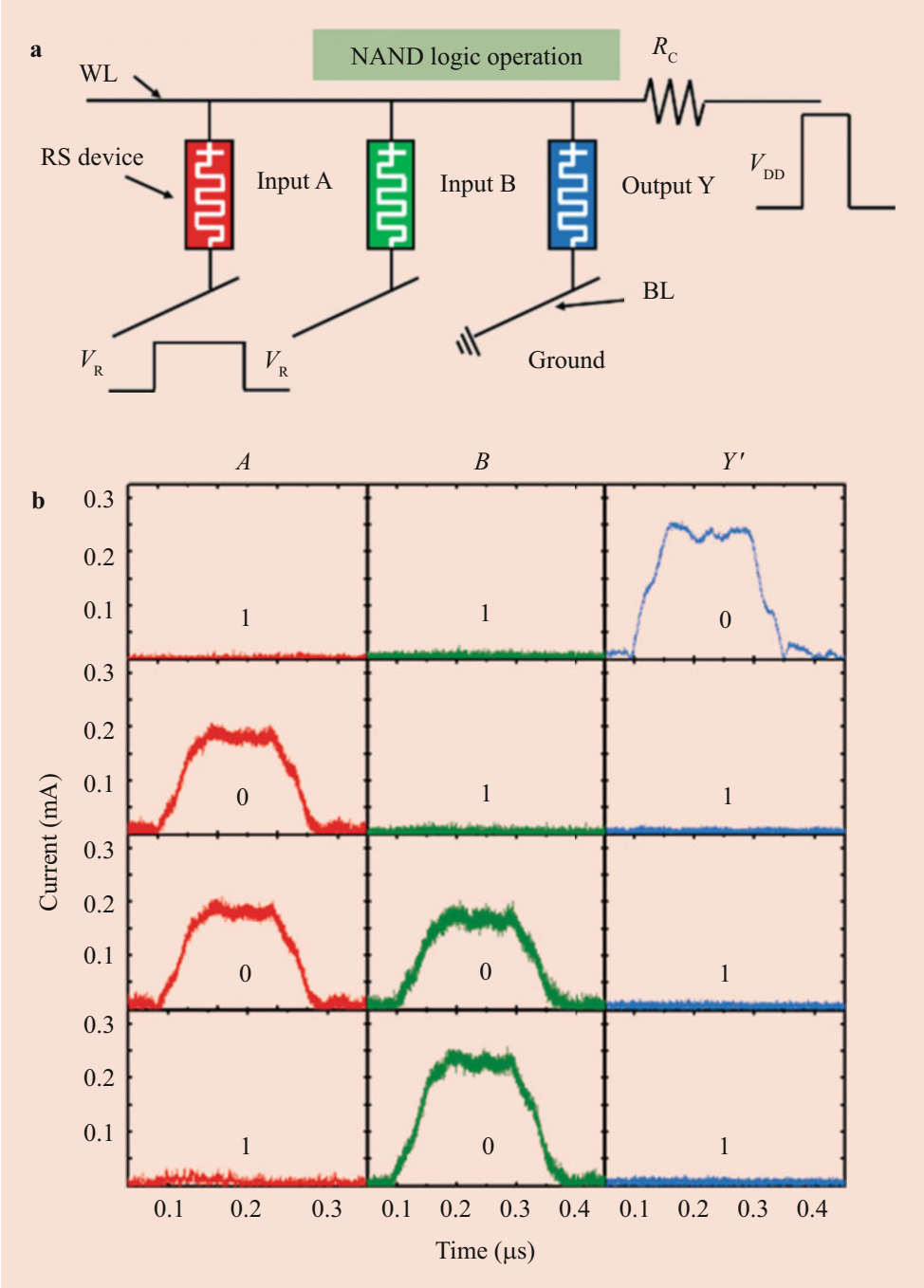
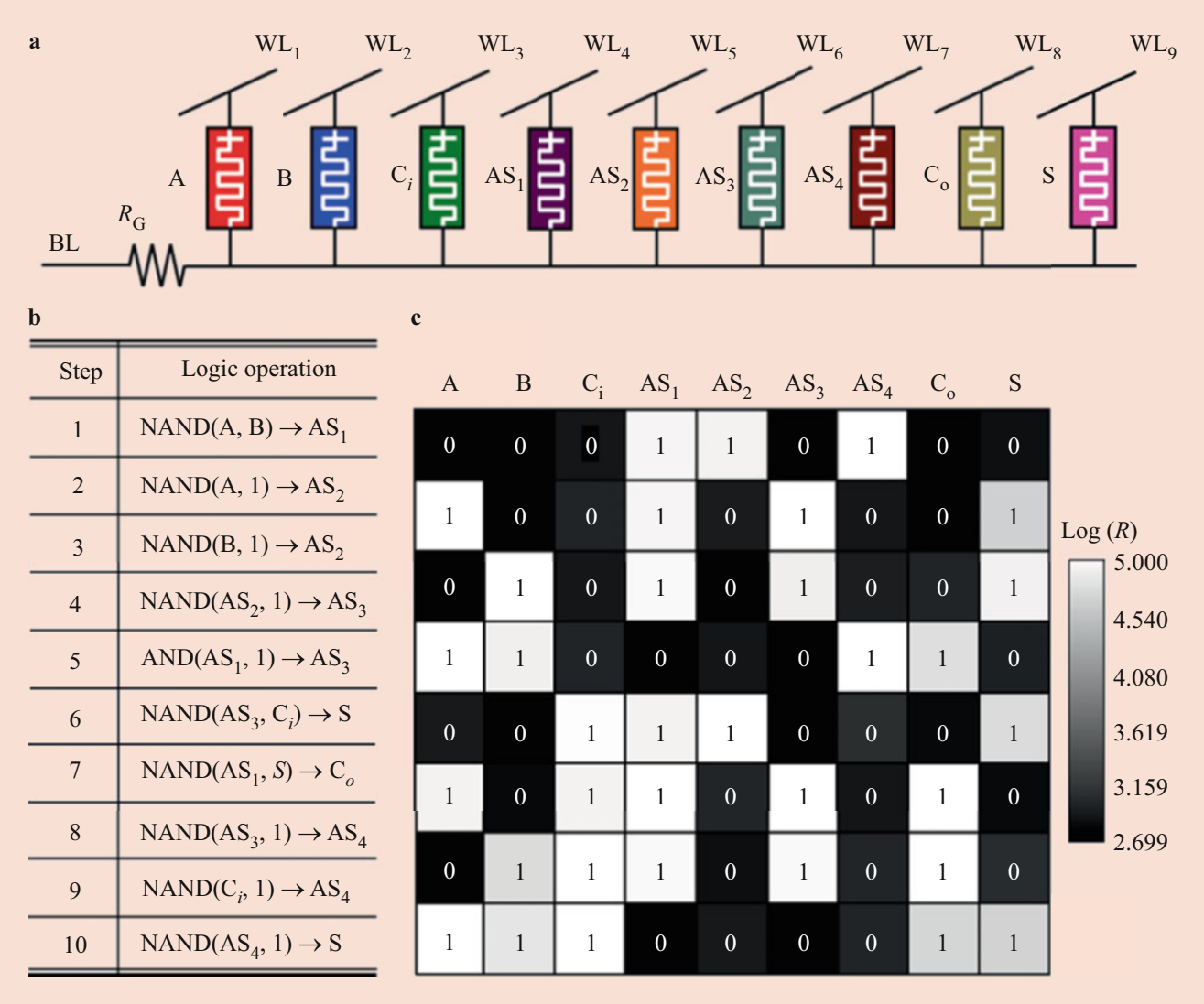


Fig. 29.45 (**a**) Sub-circuit of NAND logic operations executed by three RRAM devices with common WL. Logic inputs are stored in devices A and B, and Y will store the logic output depending on the states of devices A and B. Voltage pulses V_{DD} and V_R are applied to trigger logic operation. (**b**) The measured result of the NAND logic operation. (Reprinted from [26])



Step	Logic operation
1	NAND(A, B) → AS_1
2	NAND(A, 1) → AS_2
3	NAND(B, 1) → AS_2
4	NAND(AS_2, 1) → AS_3
5	AND(AS_1, 1) → AS_3
6	NAND(AS_3, C_i) → S
7	NAND(AS_1, S) → C_o
8	NAND(AS_3, 1) → AS_4
9	NAND(C_i, 1) → AS_4
10	NAND(AS_4, 1) → S

A	B	C_i	AS_1	AS_2	AS_3	AS_4	C_o	S
0	0	0	1	1	0	1	0	0
1	0	0	1	0	1	0	0	1
0	1	0	1	0	1	0	0	1
1	1	0	0	0	0	1	1	0
0	0	1	1	1	0	0	0	1
1	0	1	1	0	1	0	1	0
0	1	1	1	0	1	0	1	0
1	1	1	0	0	0	0	1	1

Fig. 29.46 (**a**) Array configuration of one-bit full adder circuits. (**b**) Computation procedure of one-bit full adder. Here formula "NAND(A, B) → Y" is used to represent that states of devices A and B executed the NAND logic operation and the logic output is stored into device Y. (**c**) Experimental result of logic operation of full adder for all eight input combinations. (Reprinted from [26])

To demonstrate the proposed logic executing method, a 16 × 8 array is fabricated and the measured result is shown in Fig. 29.45b. It can be found that NAND logic is successfully performed. By exchanging the V_{DD} and V_R, another frequently used logic operation AND can be executed by the same sub-circuit. It means that the logic function of the sub-circuit can be reconfigured at run-time by altering the applied voltage pulses. If the output device Y is LRS before the logic execution, its logical value will not be changed after the operation. Therefore the logic function should be revised as $Y' = \overline{AB}Y$ and $Y' = ABY$, respectively, if the logical value of Y is treated as an input. By cascading along the time dimension, any other logic functions can be realized using a finite number of NAND logic operations. Figure 29.46 shows the sub-circuit and computation procedure to perform the full adder, which is an example to show how to execute the compound logic operation with latching NAND logic operation. The sub-circuit is composed of nine RRAM cells including three input cells (addend A, summand B, and carry-in C_i), two out cells (summary S and carry-out C_o), and four assisted cells (AS_1–AS_4). The full adder logic operation requires ten sequential steps as shown in Fig. 29.46b. The logical states of input cells before operation and assisted devices and output devices after operation are read out by small voltage and are pictured as grayscale maps as shown in Fig. 29.46c. The measured results show that all eight possible input combinations correctly yielded the logical values of C_o and S that corresponded to the truth table for a full adder operation.

To execute logic operation between the states of devices in arbitrary positions of RRAM array, the previous discussed

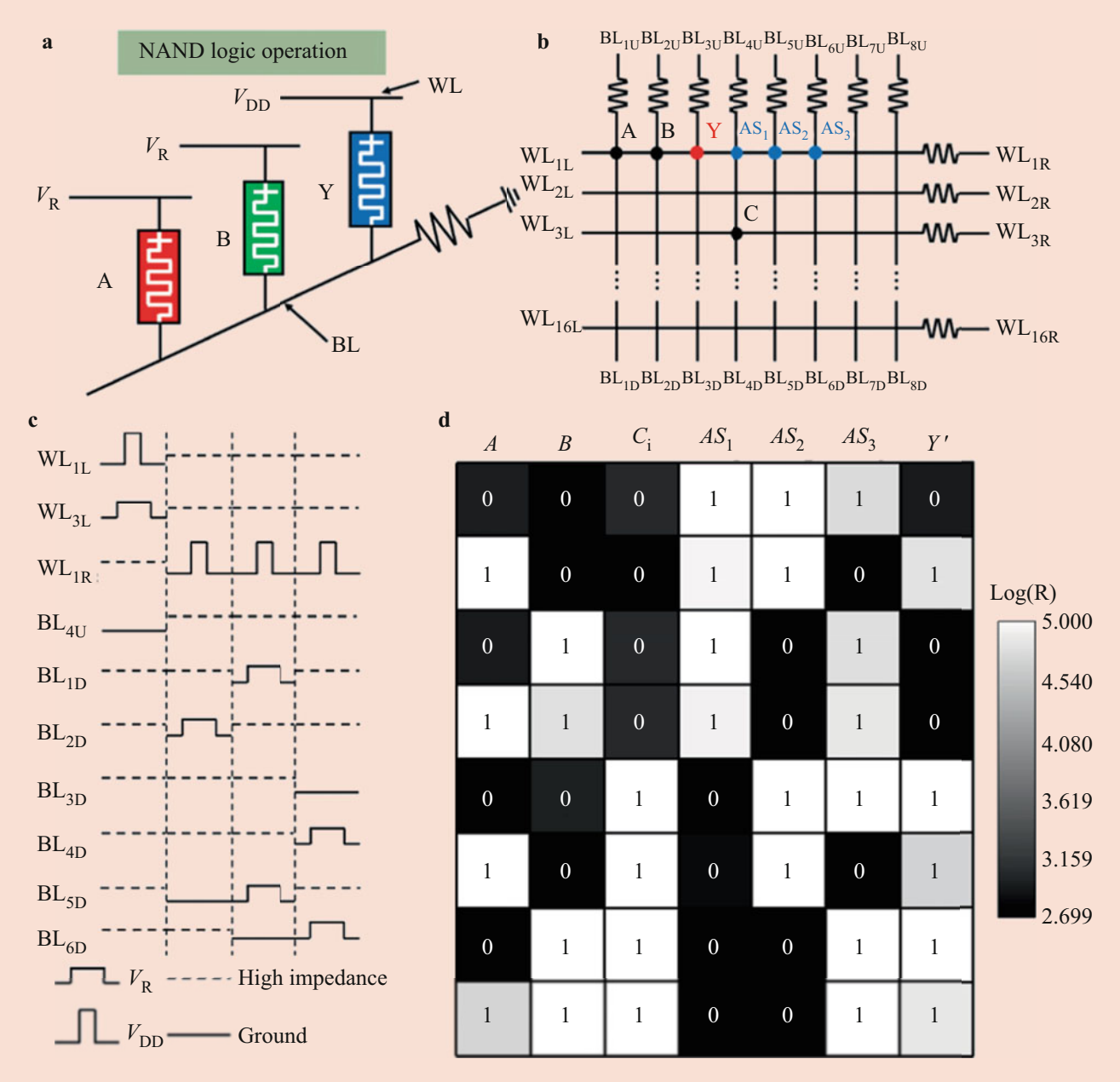


Fig. 29.47 (**a**) The array configurations of NAND logic operation executed by RRAM devices with common BL. (**b**) Location of input device in RRAM array to execute the logic operation $Y' = A\overline{B} + C$. (**c**) Time sequence of voltage pulses applied to the ports of RRAM array to perform $Y' = A\overline{B} + C$ logic operation. (**d**) Measured truth table. (Reprinted from [26])

method is not enough because the circuit structure of cells with the same BL (Fig. 29.47a) is different from the sub-circuit discussed in Fig. 29.45a. To execute the logic operation in the cell with the common BL, voltage pulses V_{DD} and V_R are applied to the TE of cell Y and A&B, respectively. Meanwhile, the common BL is grounded via the R_G. The validation of this method can be experimentally demonstrated as discussed in [26]. Figure 29.47b–d show an example how to perform arbitrary logic operations with the states of devices in different columns and rows of RRAM array. The time sequence of voltage pulses assigned to each port of RRAM array is illustrated in Fig. 29.47c. The measured results are pictured as grayscale map as shown in Fig. 29.47d, which means the defined computing task is correctly performed. Cells in different rows or columns of RRAM array can perform the same computing task in parallel by simultaneously applying the voltage pulses to the corresponding ports of BL and WL [25].

Besides the stateful logic, there are two other methods to execute Boolean logic with RRAM. In 2012, R. Rosezin et al.

used single RRAM cell as finite-state machines to perform the IMP logic operation in three steps [119]. The input of logic operation is transferred to the magnitude of voltage pulse applied to the BE or TE, and the output of the logic operation is stored in the device. The input and output physical variables of this method are different, which is difficult to cascade. Another way is using the RRAM as switch to build a reconfigurable logic array, which is proposed by B. Chen et al. in 2015. The logic operation is executed by readout based on the data matching method, which is similar to the content-addressable memory function [120]. In 2017, W.-H. Chen et al. fabricated 16 Mb ReRAM concept chip to achieve sub-14 ns computing speed with this method [121]. The variability of resistance is mitigated by the self-write termination scheme, which enhances the robustness of logic operation.

Compared with other new computing paradigms such as brain-inspired computing and quantum computing, Boolean logic computing is more close to the off-the-shelf system, which does not require developing new algorithms or software. However, the development of this field is very slow due to limited interest compared with other new computing paradigms. It still lacks the demonstration of complete computing and memory unit with input and output.

29.5.3 Brain-Inspired Computing

Another promising solution to overcome the von Neumann bottleneck is brain-inspired computing. Generally, there are two approaches for brain-inspired computing depending on the hardware used to compute. The first approach is mapping the algorithm of brain-inspired computing to the conventional CPU/GPU-SRAM/DRAM system or CMOS-based application-specific integrated circuit. This solution is still based on von Neumann architecture. Another solution is exploiting the unique properties of emerging nonvolatile memory (NVM) technologies to better emulate the analog synapses and utilize its crossbar structure for the hardware acceleration in the neural networks. The NVM uses its resistance or conductance to represent the weight of synapse. Among all emerged NVM, RRAM is one of most promising candidates due to its fast switching speed, high-density integration, low power, and COMS compatibility [24, 49, 122].

Neural network is composed of neurons and synapses. The neurons are connected by synapses with different weights. A two-layer neural network can be directly mapped to a RRAM crossbar array as shown in Fig. 29.48. The WL of the RRAM array is connected to the pre-neurons, while the BL of the array is connected to the post-neurons. The signals sent by the post-neurons are transmitted to the post-neurons via the RRAM-based synapse. The weights in the neural network are mapped to the conductance of the resistive synaptic devices. According to Kirchhoff's laws, the output current I_j at the j_{th} column can be written as

$$I_j = \sum_{i=1}^{m} V_i G_{i,j} \tag{29.54}$$

where V_i is the voltage pulse applied to the i_{th} row of WL from the pre-neurons and $G_{i,j}$ is the conductance of RRAM in the intersection of the i_{th} row and j_{th} column. Therefore, the weighted sum, which is the most time-consuming computing step for brain-inspired computing based on conventional computing system, can be performed by this crossbar RRAM array in one step. Generally, the integrated current at each column will be converted to voltage pulse by the neuron circuit and sent to the post-neuron.

The weights of RRAM-based synapses can be tuned row by row. There are two mainstream principles of weight update. One is the working mechanism of biological neural networks, in which the weight can be updated based on certain rules, such as spike time-dependent plasticity (STDP) and spike rate-dependent plasticity (SRDP) [122–126]. Such the goal is to emulate the synapse function of biological neural networks. For a STDP synapse, the weight update direction depends on the time difference Δt of the voltage pulses or spikes from the pre-neuron and post-neuron. When spikes from the pre-neuron before (after) the post-neuron, the RRAM-based synaptic weight increases (decreases). In 2010, S. H. Jo et al. fabricated a nanoscale RRAM device exhibiting the STDP synapse function as shown in Fig. 29.49a [126]. It can be found that the relation between the change in the synaptic weight and the Δt can be well fitted with exponential decay functions, which is similar to the STDP characteristics of biological synaptic systems as shown in Fig. 29.49b. In addition, this synapse can be repeated potentiating and depressing for more than 10^8 cycle. In 2017, N. Panwar et al. fabricated a PCMO-based RRAM, which shows a quasilinear relationship between analog conductance change and applied programming pulse voltage magnitude [127]. Arbitrary STDP behaviors, such as anti-STDP, symmetric STDP, and STDP with sin decay function, are achieved by leveraging this feature. In the same year, Z. Wang proposed a Ag:SiO_XN_Y-based RRAM to emulate the diffusive dynamic of biological synapse [28]. By utilizing the metal atom diffusion and spontaneous nanoparticle formation, multiple synaptic functions for both short-term and long-term plasticity, such as PPF, PPD, PPD following PPF, SRDP, and STDP, are successfully emulated. Besides the analog STDP function, binary STDP protocol was also experimentally demonstrated in the fabricated RRAM array [128]. Although various functions of biological synapse have been achieved by the RRAM, large neural network based on such synapse update rule is still lacking due to the fact

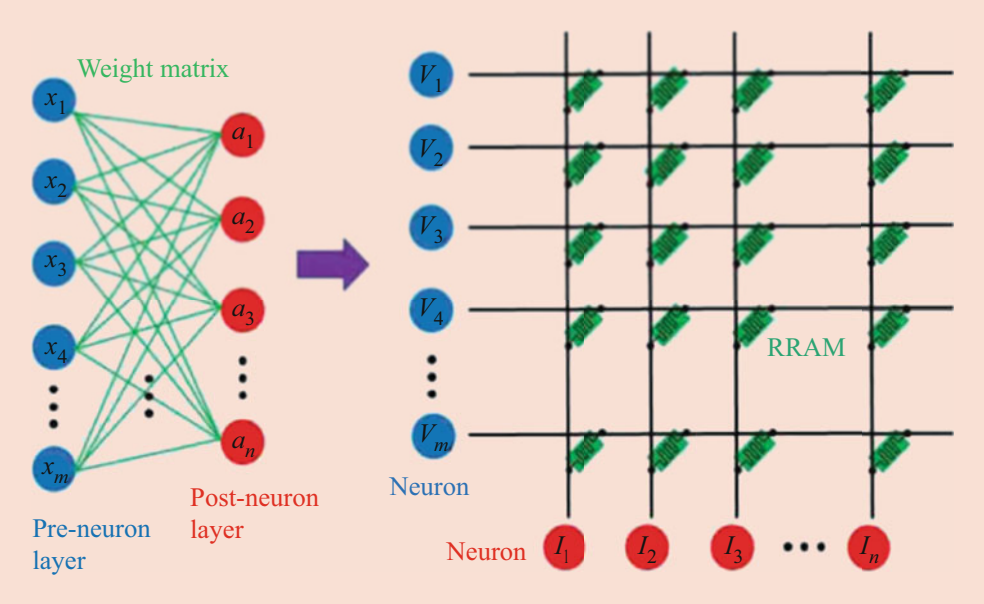


Fig. 29.48 Illustration of mapping a two-layer neural network to a RRAM array. (Reprinted from [5])

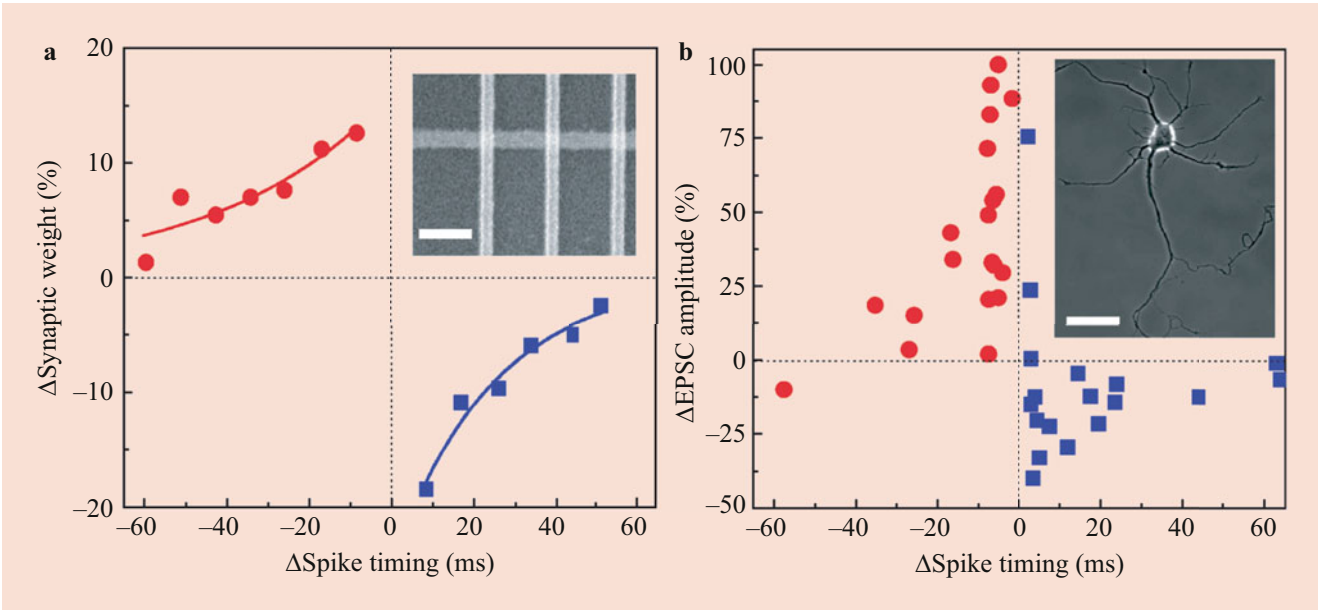


Fig. 29.49 Demonstration of STDP in the RRAM-based synapse. (**a**) The measured change of the memristor synaptic weight vs the relative timing Δt of the neuron spikes. Inset: scanning-electron microscope image of a fabricated memristor crossbar array. Scale bar: 300 nm. (**b**) The measured change in excitatory postsynaptic current (EPSC) of rat hippocampal neurons after repetitive correlated spiking (60 pulses at 1 Hz) vs relative spike timing. (Reprinted from [126])

that the working mechanism of brain is not clear. However, these achievements are helpful to the researcher of biological neural network and will significantly enhance the intelligence of neuromorphic hardware once a suitable algorithm is developed.

Another principle to update the weight is backpropagation (BP) learning rule, which has shown its advance in pattern and speech recognitions. The desirable characteristic of RRAM synapse for BP learning rule is multilevel (states > 64) and low-power (<0.1 pJ/spiking) switching, linear for update and good uniformity. In 2012, S. Yu et al. fabricated an HfOx-based RRAM synaptic device with sub-pJ energy to build a neuromorphic visual system as shown in Fig. 29.50a [76]. Z. Chen demonstrated the RRAM-based synaptic device with more than a hundred states in crosspoint array as shown in Fig. 29.50b, which can be utilized to recognize

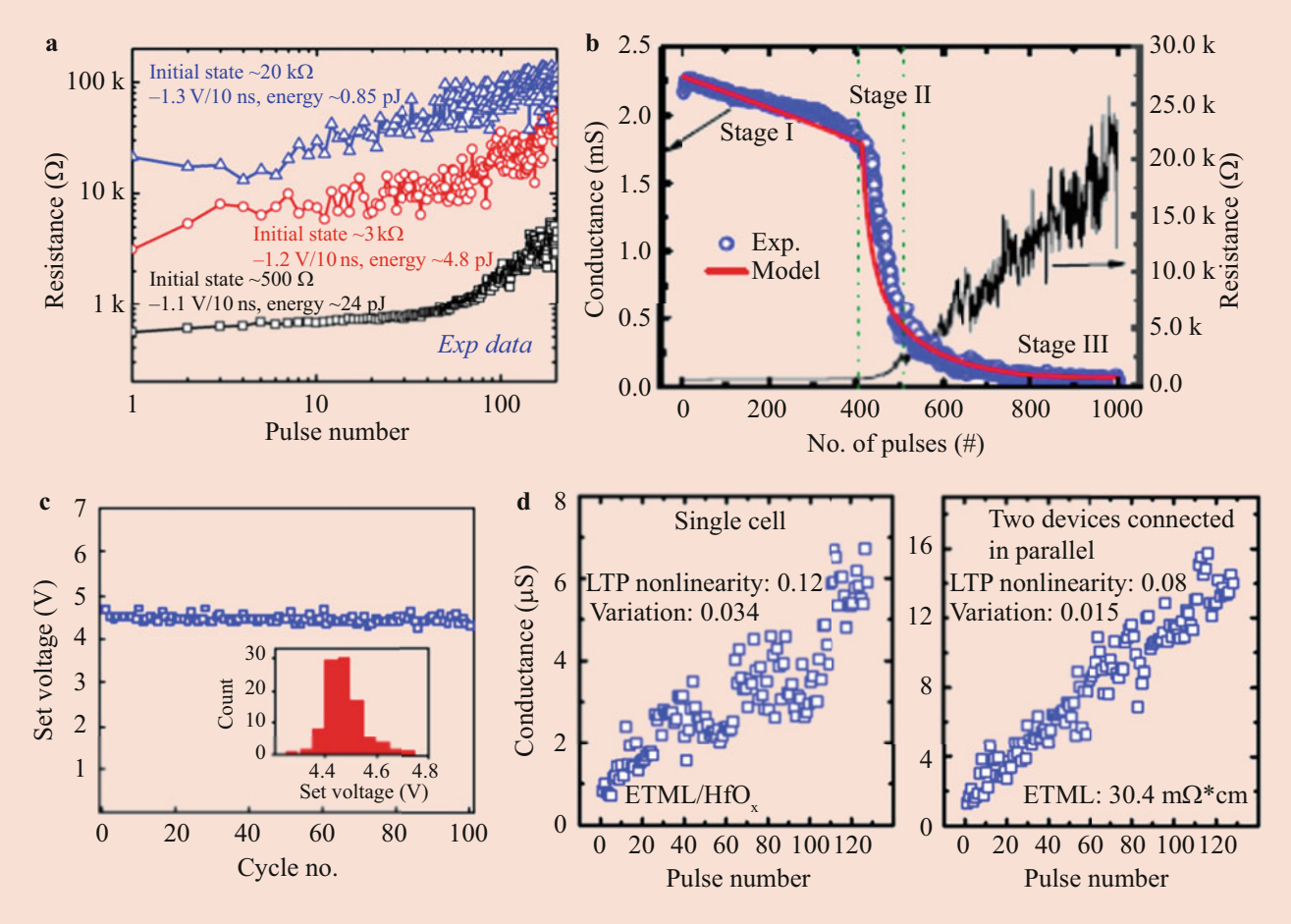


Fig. 29.50 (**a**) Dependence of energy per spike on the initial resistance states for the training process. (**b**) Measured gradual training process of resistive-switching device under consecutive identical pulses. (**c**) SET voltage with minimal temporal variations. (**d**) RRAM devices with good linearity, which is improved by introducing an electro-thermal modulation layer. (Reprinted from [76, 128, 130, 131])

the grayscale image [129]. S. Choi proposed an RRAM synaptic device with minimal spatial/temporal variations by confining the CF into widened dislocations in SiGe as shown in Fig. 29.50c [130]. By inserting an electro-thermal modulation layer between the TE and resistive layer to control the distribution of electric field and temperature in the filament region, conductance tuning linearity of RRAM synaptic device is improved by W. Wu et al. in [131]. However, the dynamic range decreases as shown in Fig. 29.50d. Z. Zhou et al. proposed a new hardware implementation approach to utilize the nonlinear synaptic cells to achieve high efficient online training [132]. Based on the presented implementation approach, the conductance tuning nonlinearity has little impact on the recognition accuracy of neural network.

Up to now, there are also a few experimental implementations of small-scale neural network based on RRAM array. In 2015, M. Prezioso et al. reported the experimental implementation of transistor-free Al_2O_3/TiO_{2-x} crosspoint array with low variability to allow operation of integrated neural networks for the linear classification [24]. The fabricated 12×12 crosspoint array was used to implement a single-layer perceptron with 10 inputs and 3 outputs, fully connected with 30 synapses. The neural network is used to classify three black-and-white images with 3×3-pixel, which corresponds to the nine inputs $V_1 \sim V_9$ as shown in Fig. 29.51a. V_{10} is the constant bias of nonlinear activation function. Thirty patterns, including three stylized letters ("z," "v," and "n") and three sets of nine noisy versions of each letter, are used to train and test this small-scale neural network. Each input signal was represented by a voltage V_j equal to either $+0.1$ V or -0.1 V according to the color of the pixel. The bias input V_{10} was equal to -0.1 V for the balance of the input. Each synaptic weight was implemented with a pair of memristors, so that $w_{ij} = G+ ij - G- ij$, enabling negative weights values. The network was trained with the Manhattan update rule in situ. The weights are updated in parallel for each column using two sequential voltage pulses. After 23 training epoch, the neural network can classify the 3 different letters by initializing the RRAM cell in the middle of their conductance (Fig. 29.51b). P. Yao et al. built a single-

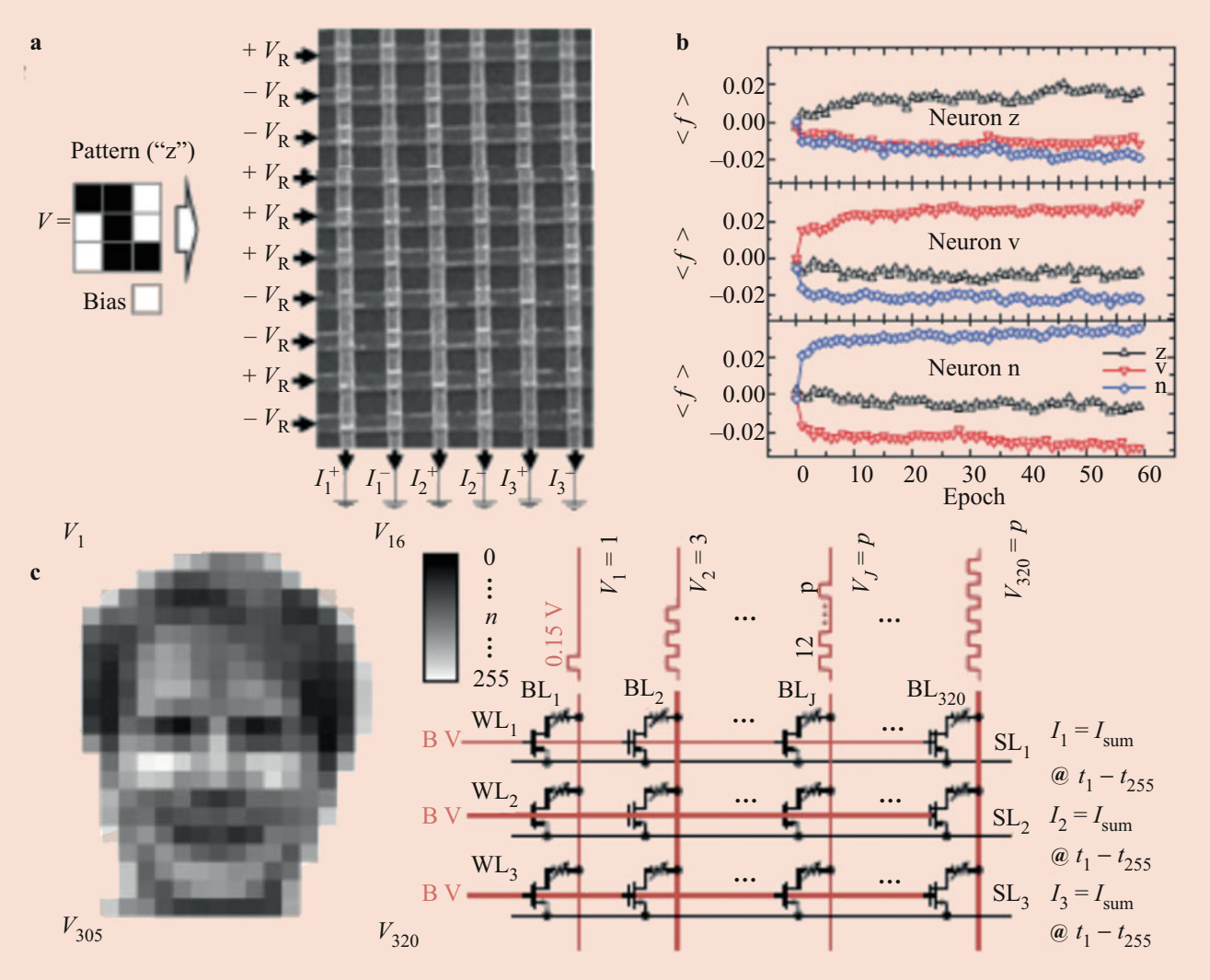


Fig. 29.51 (**a**) An example of the classification operation for a specific input pattern (stylized letter "z"), with the crossbar input signals equal to $+V_R$ or $-V_R$, depending on the pixel color. (**b**) The evolution of output signals, averaged over all patterns of a specific class. (**c**) The schematic of parallel read operation and how a pattern is mapped to the input. (Reprinted from [24, 49])

layer perceptron for grayscale face classification with 1T1R crosspoint array capable of bidirectional continuous weight modulation [49]. The fabricated $TaO_X/HfAl_yO_x$ RRAM array is 128 × 8, which is used to train the face pattern with 20 × 16-pixel as shown in Fig. 29.51c. In the training of neural network, two update rules were adopted: (1) without write-verify which only points out the switching direction depending on the errors sign, following the Manhattan rule, and (2) with write-verify which implements both direction and amplitude based on the errors sign and value, following the delta rule. There is a tradeoff between these two schemes. The scheme without write-verify can simplify the control circuitry since it is not necessary to calculate the specific analog value of the error between the targeted weight and the current weight, but it may slow down the converging speed due to the programming stochasticity, and the recognition rate is relatively low compared with the scheme with verify. The activation function of the output neurons is realized by measuring the total currents on SL to obtain the weighted sum and applying the sum to a nonlinear activation function. Nine images are chosen from the Yale Face Database and cropped down to 320 pixels to train and test this small-scale neural network. The image is in grayscale ranging from 0 to 255, which was converted to the number of voltage pulse applied to the BL (Fig. 29.51c). The average recognition rate on the total 9000 augmented noisy test patterns is 88.08% and 85.04% for the write-verify and without write-verify scheme, respectively.

Although some small-scale neural networks based on RRAM array have been demonstrated, it is still far from being applied. Challenges such as material optimization, variation suppressing, neuron circuit design, and algorithm

modification according to the practical device are needed to be solved.

29.6 Summary and Prospect

The RRAM has achieved remarkable progresses in the past decades. The significant advances include the following:

1. Physics understanding of the underlying mechanisms on resistive-switching behaviors. Various mechanisms have been proposed to clarify the physical origins of resistive switching in RRAM.
2. Physics-based models and simulation methods and platforms have been developed to quantify the device characteristics for the design and optimization of devices and circuits.
3. A variety of technical approaches for the integration and design of RRAM arrays and circuits were presented to achieve high performance with high-density integration and low-cost manufacturing.
4. The fabrication processes of RRAM-CMOS hybrid circuits were investigated.
5. The comprehensive visions of RRAM have been explored for future information processing technologies such as emerged memory and brain-inspired computing. RRAM testing chips for memory and brain-inspired computing have been demonstrated, indicating the feasibility of RRAM technologies for data storage such as embedded memory and brain-inspired computing systems.

These achievements highly promote the advances of RRAM technologies both in research and commercial activity.

Facing the research and application requirements, RRAM technologies still have some key challenges.

1. Physical mechanism: The development and application of RRAM technology demands a deep and predictive understanding of its underlying mechanisms. Even if the filament effect has been widely accepted for resistive switching, the physical origins of the conductive filament evolution during switching processes are still debated on, especially for Ox-RRAM. The main reason is due to the lack of direct experiment evidences in microscopic characterizations to identify the proposed mechanisms. Therefore, the final solution is to have the aid of breakthrough in atomic-level characterization technologies in the future.
2. Device optimization: The significant advances on device performance improvements have been achieved in Ox-RRAM. However, some key issues have to be addressed such as device variability from switching cycle to cycle and from device to device, peak switching current, forming voltage, and multilevel resistance states. Further optimization on these characteristics is desired to meet the requirements of the circuits and systems. The effective solutions may depend on the design and optimization of structures, materials, and operation schemes in device level by means of the deeply physical understanding and innovative device-engineering methods.
3. Selector: In the implementation of RRAM arrays, the array cell, in which a select device or selector is connected with a RRAM in series, is required to avoid or suppress the sneak path current issue in the crossbar arrays. It is key to develop a high-performance selector that can be easily stacked with RRAM and fabricated by CMOS-compatible process. For a selector, the required characteristics should include high on-current, high on/off-ratio, bipolar switch with high endurance, matching switch voltage with RRAM, and robust reliability. The optional selectors may be a transistor or a nonlinear device. From the viewpoint of high-density integration, a two-terminal selector is preferential for RRAM array. For this kind of selector, high nonlinearity, bipolar switch with high on-current, robust switching capacity with high endurance and anti-breakdown is highly desired. However, to develop the available selector for RRAM technology is still one of the major challenges.
4. Array cell: RRAM arrays usually utilize a crossbar structure, in which a basic cell includes a select device and a RRAM. Three types of optional cell structures have been proposed for RRAM arrays: (1) 1T1R, (2) 1R, and (3) 1S1R. For the 1T1R cell, a transistor is used as the selector at each cell. A transistor may be an ideal selector from the functions, but it limits the footprint of each cell and three-dimensional integration capability. 1R structure may be a plausible solution for ultrahigh density of crossbar array, in which the I–V nonlinearity of RRAM devices is utilized. In this structure, high I–V nonlinearity is needed. Additionally, the hard breakdown of RRAM cells during operation process is a key factor, which may cause unrecoverable damage to the array performance and reliable operation. The best solution is to use 1S1R structure, in which a two-terminal nonlinear device is stacked with RRAM to achieve small footprint of each cell and three-dimensional integration capability. However, 1S1R cell solution is stuck by selector technology. In this case, 1T1R or 2T2R cells with complementary structure will be the available solution for high volume of array integration in the near future.
5. Hardware architecture implementation: For brain-inspired neural networks, hardware implementation is emerging as one of the key challenges. In deep neural networks (DNNs), the key technical challenges are from two aspects. One is associated with the acceleration computing

using RRAM array, in which the design and fabrication of high performance RRAM arrays are key factors. Another is about the nonlinearity/symmetry and variability of RRAM-based synapses. According to the BP algorithm, the linear and symmetric responses of synapses to electric pulses are required for training process. However, that is a quite difficult task for RRAM-based synapse. Regarding this issue, the possible solutions may be from the interaction and optimization between devices and algorithm or architectures. For example, incorporating with recently proposed binarized neural networks (BNNs) based on modified BP algorithm, the impact of nonlinearity in RRAM-based synapses on system performance can be effectively eliminated.

In addition, programmable and reconfigurable physical fabrics using the intrinsic natures of RRAM are highly demanded.

As we look forward to the future, RRAM has emerged its great potential as one of most promising candidates for future information processing technologies past the von Neumann and Moore's law era. When the information processing technologies come to the data-centric era, it is necessary to develop the brain-inspired neural networks. While RRAM has the potential to be a nonvolatile memory technology both in standalone and embedded cases, it may be even more suitable for brain-inspired computing, especially considering its computing capacity beyond data storage. RRAM-based computing paradigms might provide a promising solution for the hardware implementation of brain-inspired neural networks. Specifically, RRAM arrays in crossbar structure can provide a native solution to implement massively parallel and power-efficient vector-matrix operations that form the basis of the core-computation in brain-inspired neural networks such as DNNs.

For the brain-inspired computing, RRAM devices are widely studied not only as function cells to mimic the dynamic behaviors of the basic cells-synapses and neurons in artificial neural networks (ANNs) but also as the data processing cells to perform the complex computing function such as convolution computing in deep learning convolution neuron networks. In DNNs, the backpropagation algorithms and corresponding architectures have been successfully developed and implemented for various application systems including image/speech recognition and natural language processing. The state-of-the-art DNN networks require a large memory capacity and high memory bandwidth. The massively parallel and power-efficient vector-matrix operations featured in a RRAM crossbar structure may provide an effective solution to DNN with high-performance acceleration for convolution computing. In the spiking neural networks (SNNs), the typical biological characteristics of spike timing-dependent plasticity (STDP) have been demonstrated, and a STDP-based learning rule is studied. However, the corresponding architectures and algorithms that can be utilized to construct a power-efficiency and operable SNN computing systems are still being developed. It is highly desired to develop the applicable algorithms or architectures based on the biological behaviors such as STDP. That will require persistent and creative research for RRAM technologies but must include insights from neuroscience, physics, chemistry, computer science, and electrical and computer engineering beyond any single discipline.

RRAM-based low-power embedded chips may be promising for edge-computing such as Internet of Things. Further advances in device technology and algorithm/architecture developments may lead to large-scale implementation of RRAM-based brain-inspired computing systems. This will drive RRAM into new research upsurges in the near future beyond memory.

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Phase-Change Memories

30

Enrico Piccinini and Carlo Jacoboni

Contents

30.1 Introduction 1093

30.2 PCM Development 1094
30.2.1 A Historical Overview 1094
30.2.2 PCM Placement in the Non-volatile Memory Market 1095

30.3 Basics of the PCM Technology 1096
30.3.1 Optical and Electrical Properties of Chalcogenide Materials 1097
30.3.2 Device Operation 1099
30.3.3 The Ovonic Threshold Switching 1101
30.3.4 Memory Switching and the Physics of Phase Change 1103

30.4 Materials and Devices 1105
30.4.1 Materials and PCM Performances 1105
30.4.2 PCM Device Architectures 1106

30.5 Reliability and Perspectives 1112
30.5.1 PCM Reliability 1112
30.5.2 Performance Improvements and Perspectives 1116

References 1117

Abstract

This chapter is devoted to phase-change memories that have entered the market of non-volatile memories at the verge of the new millennium as a possible replacement for ultra-scaled flash memories. Rather than replacing conventional flash memories, the phase-change memory technology is now paving the way to the new market segment of storage-class memories.

Phase-change memories rely on chalcogenide alloys, which have been studied for more than a century now. After revisiting the most important historical and technological achievements of the last 50 years, the second part of the chapter summarizes the most relevant fundamental physical properties of chalcogenide alloys that influence their exploitation by the semiconductor industry. Besides pure phase-changing alloys for data storage, Ovonic materials for selectors are also considered.

The last two sections are more focused on the real-device performances. At first, the properties of chalcogenide alloys are reviewed in view of their influence on the performances of devices, and the most common device architectures are presented. Emerging cross-point arrays are also described. Finally, the most relevant reliability issues affecting phase-change memories are analyzed. New perspectives that are being pursued to achieve faster and more reliable phase-change memories are briefly outlined in the concluding paragraph.

Keywords

Properties of chalcogenide alloys · Ovonic threshold switching · Memory switching · Phase-change memory architectures · Selectors and cross-point arrays · Reliability issues

30.1 Introduction

Phase-change materials have historically received great interest from the community of optical and electronic engineers. At first, they were exploited for optical data storage; then, more recently, in the last couple of decades, they experienced a kind of second life as electronic non-volatile memories (NVM). Such an interest is based on their speed, data retention, endurance, and scalability, mainly due to the physical properties of the chalcogenides, the main materials they are made of.

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A vast literature has been published in 50 years by research centers and, partially, by semiconductor industries. The present chapter contains a general, broad presentation of the physics and the technology of phase-change memories (PCM), as a detailed, exhaustive description would largely go beyond the scope of this chapter. Thus, in the following pages, only the main ideas on which these devices are based will be considered and illustrated. Readers willing to enter more deeply into the physics, material properties, and technology of PCM can find more detailed information in many good books specifically devoted to these topics [1–3], in review papers (e.g., [4–8]), and in the references therein.

30.2 PCM Development

30.2.1 A Historical Overview

In 1917 A.T. Waterman [9] published a paper entitled "*On the positive ionization from certain hot salts, together with some observations on the electrical properties of molybdenite at high temperatures*." Such observations sound, today, very peculiar, and it is worth reporting some of the original wording. They refer to the fact that "*With small applied potential differences the resistance of the strips is very high, but diminishes rapidly with increasing potential differences. No doubt this alteration in conductivity is partly due to the rise in temperature caused by the electric current*." Furthermore, "*The diminution of resistance with increasing potential difference continues uniformly up to a certain potential difference, […] at this point, which will be referred to as – 'the break', the resistance diminishes suddenly […] Before the voltage has been raised sufficiently for the break to occur the resistance diminishes […] with increasing voltage, whereas after the break the resistance diminishes with diminishing voltage. This difference may be regarded as characteristic of two states, α and β, of the material […] The phenomenon of the break is reversible […] The substance also tends to persist in the state in which it was when the current was turned off*." Figure 30.1, taken from the original paper of 1917, shows the results reported above. Waterman returned to the subject a few years later [10]. The new, more detailed, results confirmed the idea of the two forms of the molybdenite, α and β. The first form is characterized by a much higher conductivity than the second one. Part of these results, whose general aspects are very familiar to the present-day researchers in the field of PCM, are reported in [11].

The results of Waterman did not contain, of course, any indications of possible applications, and there were no relevant follow-ups.

The topic was investigated again many years later, in the sixties of the last century [12–15]. In his PRL paper of 1968, Ovshinsky reported "*a rapid and reversible transition between a highly resistive and a conductive state effected by an electric field … observed in various types of disordered materials, particularly amorphous semiconductors*." Despite not being the very first paper on this topic, this PRL paper is universally considered the first milestone of the PCM technology. In fact, this work had a particular impact on the scientific and technological literature, also because the analysis was soon extended to the optical properties of the same materials [16]. Since then Ovshinsky has been considered the founder of the applications of such materials, generally called *Ovonic* materials. He himself proposed this adjective to advertise his business, as for his previous important invention, which he called Ovitron switch [17].

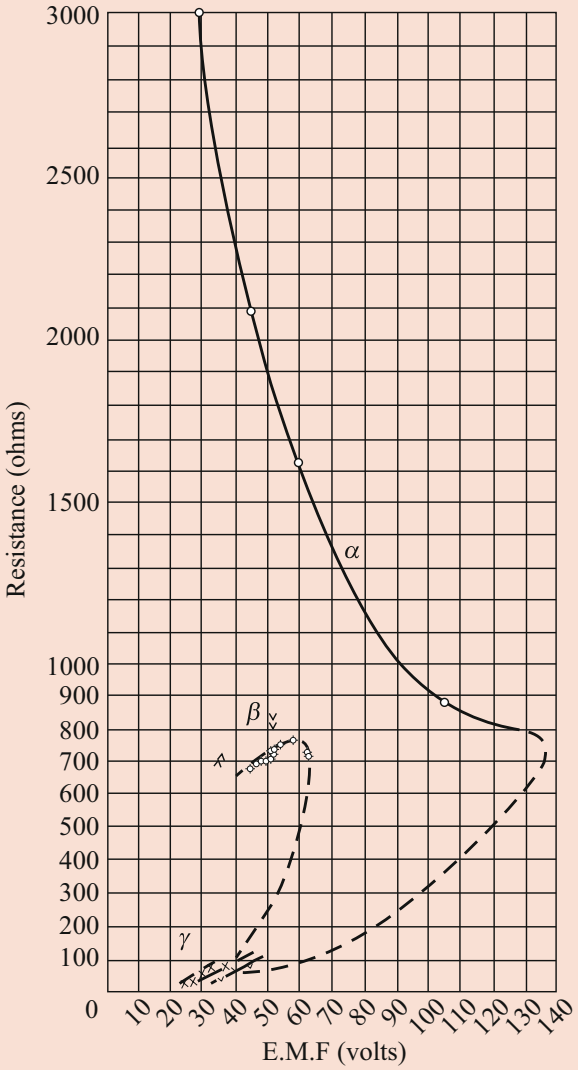

Fig. 30.1 Resistance of a sample of molybdenite as a function of the applied potential. (Reprinted, with permission, from [9] © Taylor & Francis Ltd., http://www.tandfonline.com)

In 1964 Eaton suggested that "*the transformation from one resistance state to another is due to a thermal breakdown of the dielectric during which melting occurs. Subsequently, either a high-resistance, glassy state, or low-resistance, crystalline state develops depending on the rate of cooling of the specimen*" [13]. In 1969 Pearson and Miller [18] mention "*well known semiconducting glass diodes […] which can exhibit negative resistance, […] undergo reversible electrical switching, and display a memory function*." They also report on "*the formation of a liquid phase and what appear to be conducting filaments […] with current densities* $> 10^4$ *A* cm^{-2}." Such filaments had been already suggested [13] and were coherent with the general theory of Ridley [19], according to which semiconductors with current controlled negative resistance might be expected to show filamentary current paths as a consequence the principle of least entropy production. The technological importance of fast and reversible variations of physical properties of such materials was already very clear to the above authors as evidenced by the fact that the publication of their results took place only after the request of patent registration [11]. In fact, several attempts to produce electronic memory chips of PCM have been made by some electronic industries in the following years. Such attempts, however, did not succeed mainly because of the large energy required to realize the phase change at each switch. Furthermore, chalcogenide-based memory prototypes were bigger and slower than conventional memories.

In addition to these objective difficulties, at that time there was also a certain *ideological* opposition from the establishment to Ovshinsky's new proposals: on the one hand, Ovshinsky was an outsider, without any academic credit, and this gave him little credibility; on the other hand, at that time scientific and technological activities were concentrated on the physics of crystals, and it did not seem possible that amorphous materials could be fruitfully exploited for the development of electronic devices owing to their intrinsic disorder [17].

Electronic PCM acquired a renewed interest and popularity at the turn of the millennium. On the one side, the reduction of the dimensions of the single devices drastically cut the power necessary to their working; on the other side, new chalcogenide alloys with fast crystallization times, high endurance, and long data retention were synthesized and studied. In addition, PCM proved to be less vulnerable to radiation, which makes them suitable for space and military applications. These reasons paved the way for making PCM competitive as replacements for conventional NVM, and in 2002 a 4Mb demonstrator array at the 180-nm technology node was presented by Ovonics and Intel [20].

Since then, most of the main semiconductor industries revealed their interest in PCM, and mass production was initiated by Numonyx (now Micron) [21] and Samsung [22, 23] with denser chips that reached 1 Gb at the 45-nm technology node in 2009, and 8 Gb after scaling down to the 20-nm technology node in 2012. Moreover, manufacturers investigated the exploitation of Ovonic materials also for new selectors, and Intel announced in 2009 a prototype of a stackable cross-point PCM [24].

Finally, in 2015 Intel and Micron unveiled the 3D XPoint™ technology, a commercial non-volatile 3D memory solution entirely based on chalcogenide materials for both the selector and the storage element [25, 26].

Optical memory devices had a better and faster success. The Ovshinsky group, in the same years of the research on the electrical properties of amorphous semiconductors, performed an analogous research on their optical properties [16]. They reported "*a high-speed crystallization of amorphous semiconductor films and the reversal of this crystallization back to the amorphous state using short pulses of laser light and evidenced by a sharp change in optical transmission and reflection. This optical switching behavior is analogous to the memory-type electrical switching effect in these materials*."

The first attempts to manufacture optical memories date back to the early 1970s; in the 1980s, write-once optical disks were released to the mass market. Owing to the possibility of being programmed with a suitable flashlamp exposure, phase-change materials, and chalcogenides in particular, became in the late 1990s key enablers for rewritable CDs and DVDs, under the impulse of Panasonic as leading industry. In 2003, high-capacity Blu-ray disks were also introduced into the market [27].

In recent years, new perspectives have opened up for the application of PCM (as well as other memories based on a controllable resistance change like RRAM) in the field of neuromorphic computation, a form of non-von Neumann, brain-inspired, computing where the same device acts both as memory element and processing unit. This subject is treated in details in Chap. ▶ 32. It must be said that also in this field Ovshinsky was a far-sighted anticipator. In fact, already in 1955 he was strongly interested in neurons and in the possibility of duplicating their functioning with electronic devices. There is little written testimony of his old proposals [17], while, more recently, one devoted to cognitive computing, developed in cooperation with Pashmakov, can be found in [28].

30.2.2 PCM Placement in the Non-volatile Memory Market

When PCM commercialization began in the late 2000s, a lot of expectations arose around this technology. The initial product development aimed at replacing NOR flash memories, targeting cellular phones as the driving application. According to Fantini [29], millions and millions of PCM

Table 30.1 Taxonomy of memory technologies on the basis of their key attributes

	PCM	NOR-flash	NAND-flash	DRAM
Non-volatility	Yes	Yes	Yes	No
Scaling	1× nm	45 nm	1× nm	1× nm
Granularity	Small/byte	Large	Large	Small/byte
Power	∼ Flash	Flash	Flash	> Flash
Write bandwidth	1–>15 MB/s	0.5–2 MB/s	>10 MB/s	>100 MB/s
Read latency	50–100 ns	70–100 ns	15–50 µs	20–80 ns
Endurance	$>10^6$	10^5	10^4–10^5	Unlimited

Adapted from [32]

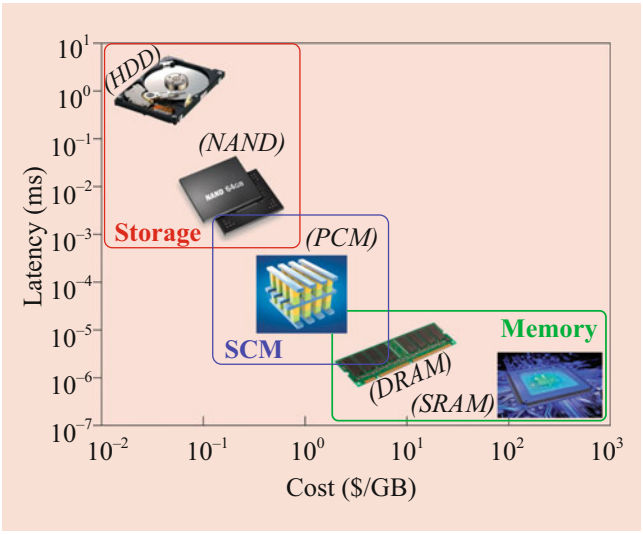

Fig. 30.2 Access time and cost for various memory technologies

cells were used, representing "*the largest volume of bits ever shipped on a non-charge based solid state memory physics*." The advent of smartphones turned the tables on the mobile phone scenario, and at that time it was clear that the huge demand of memory elements favored the transition to the NAND architecture. The use of PCM was then discontinued; PCM devices would turn competitive again only if they could be aggressively scaled down to reach data densities superior to those achieved by 3D-NANDs and justify the large investment costs to implement a new technology option.

Nevertheless, PCM still represent a viable choice for the embedded non-volatile memory technology, taking also into account their potential for computation. Currently, when these notes are being written, the integration of a conventional embedded non-volatile memory (e-NVM) at the 28-nm node is challenging, whereas PCM have already demonstrated the feasibility of such a solution at the production stage. Embedded PCM have the potential to quickly become the mainstream solution for automotive applications thanks to their single-bit alterability, which is a key enabler for a much simpler data handling with respect to flash-based memories, and to their reliability properties [30].

Besides the interest for automotive applications, manufacturers are seeking new market opportunities for PCM. During the early stages of development, the promising features of PCM devices led to envisaging PCM as a potential *universal* memory able to replace on one side flash memories and on the other side DRAMs. As knowledge progressed, neither of these two options became viable: PCM proved slower and with a worse endurance than DRAM and with a higher cost per bit than NAND flash. However, as reported in Table 30.1 and in the memory hierarchy of Fig. 30.2, a large gap in terms of latency (access time) and cost per bit exists between DRAM and NAND flash. Filling this gap is a clear opportunity for PCM, which can enter the memory market as a new complementary system usually referred to as storage class memory (SCM) [31], featuring an access time <10 µs and a moderate cost < 1 $/GB. PCM can thus compete as a faster, higher endurance NAND flash in the form of a storage-type SCM, where cost is the primary driver, and also as a non-volatile, though slightly slower, DRAM in the alternative form of a memory-type SCM, whose main focus is on write speed and read latency. At present, the main limitation for a storage-type PCM-based SCM is represented by the cost per bit, which can be reduced with the significant enhancement of the density offered by cross-point stacked 3D architectures.

30.3 Basics of the PCM Technology

A class of alloys including elements of the VI-A group, called chalcogenides, can easily and reversibly be switched between the amorphous and the crystalline phase upon the application of a heat source, like a laser spot or an electric current. Despite the intrinsic thermodynamic instability common to all glasses, the amorphous phase requires up to some years to spontaneously recrystallize at room temperature so that the amorphous state is considered stable as well in any practical application. On the contrary, crystallization becomes very rapid when the material is heated above the crystallization (or the glass transition) temperature.

Moreover, the amorphous and the crystalline phases exhibit in general a very large contrast in reflectivity and resistivity. These features make chalcogenide layers as the key component of a non-volatile phase-change memory, which is basically a thin-film resistor whose low-field resistance varies by at least two orders of magnitude depending on the phase state of the active region.

A ternary diagram of common chalcogenide alloys used by the semiconductor industry is shown in Fig. 30.3; among them, the most exploited compositions lie along the GeTe-Sb_2Te_3 tie line or are derived from it by doping and stoichiometry alteration [27].

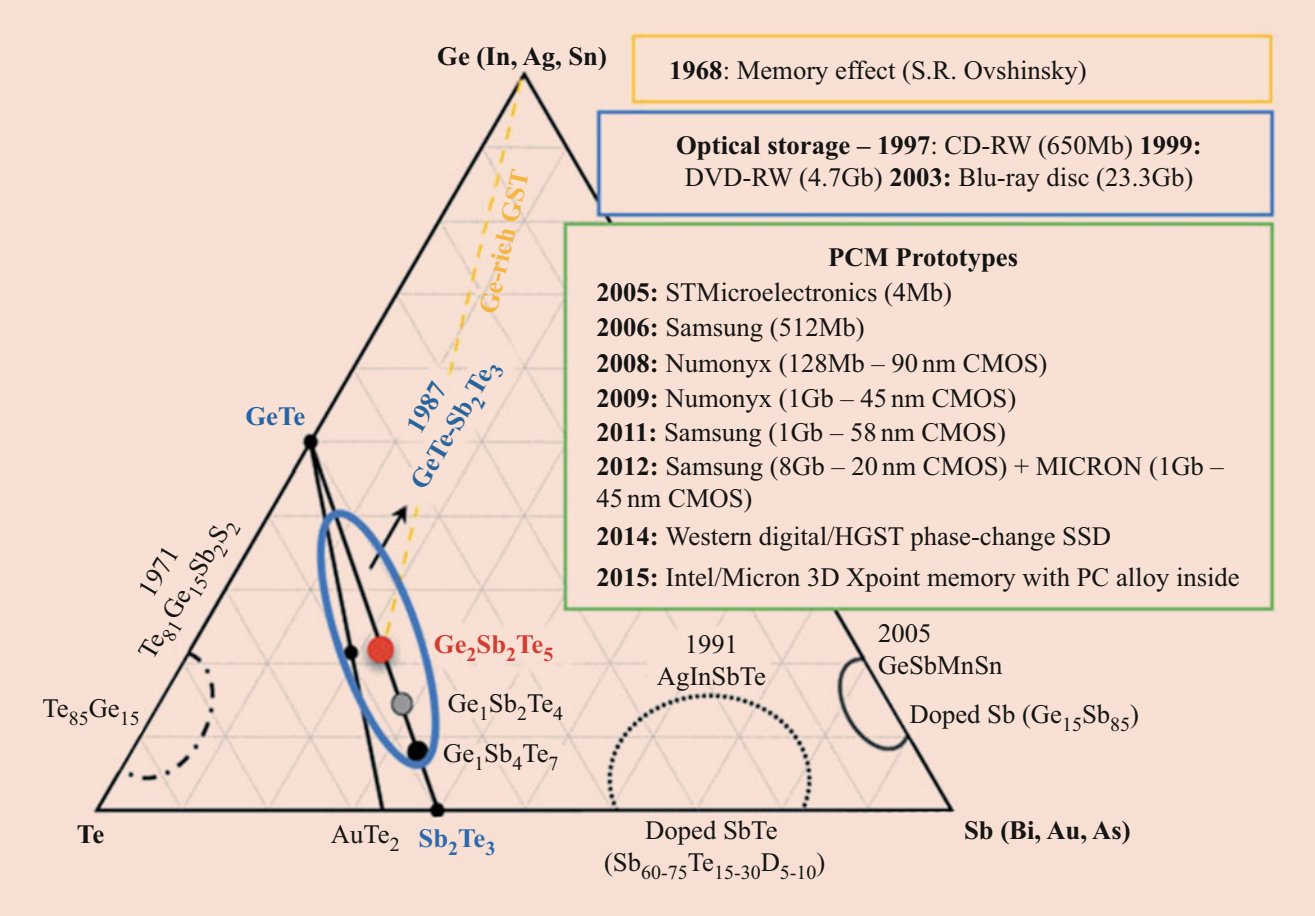

Fig. 30.3 Ternary phase diagram of most common chalcogenide alloys. The insets list the most important technological achievements reported also in Sect. 30.2.1. (After [33])

30.3.1 Optical and Electrical Properties of Chalcogenide Materials

The knowledge of the optical and electrical properties of chalcogenide materialsis of the utmost importance for unraveling the physics of the switching and their behavior in an NVM device. Some of these properties are often derived, either directly or indirectly, from optical experiments on thin films, which make them dependent also on the deposition parameters and the film microstructure. As a consequence, data published in the literature regarding, e.g., the optical bandgap, may be scattered (the interested reader can compare data cited in [33]), though they all lead to the same common interpretation and to the same trends. Most of the results disclosed in the literature have been determined for the $Ge_2Sb_2Te_5$ (also known as GST-225) and for the GeTe alloys, which are prototypical chalcogenides.

The amorphous GST-225 crystallizes into a rock-salt-like cubic phase, where one site is occupied by Te and the other site is occupied by Sb, Ge, and a 20% of stoichiometric vacancies [34], which are useful to stabilize the structure. This phase is metastable and transforms at about 600 K into a stable hexagonal phase. The sharp transition of the electrical resistivity between the amorphous and crystalline states is shown in Fig. 30.4a, where an initially fully amorphous layer of GST-225 (GeTe) is slowly heated up to the melting temperature. The abrupt changes highlight the amorphous-to-crystalline transition; a smaller drop is also present for GST-225 at higher temperature, coinciding with the transformation to the hexagonal phase. After the amorphous-to-crystalline transition has occurred, the material preserves the high-temperature resistivity also during cooling.

Analogous diagrams can be obtained also for the optical reflectivity (Fig. 30.4b), with a very pronounced increase in correspondence of the amorphous-to-crystalline transition, as for the resistivity. On the contrary, the cubic-to-hexagonal transition has limited effect on the optical reflectivity. The refractive index n and the extinction coefficient k for the two crystalline structures are, in fact, quite similar with small to

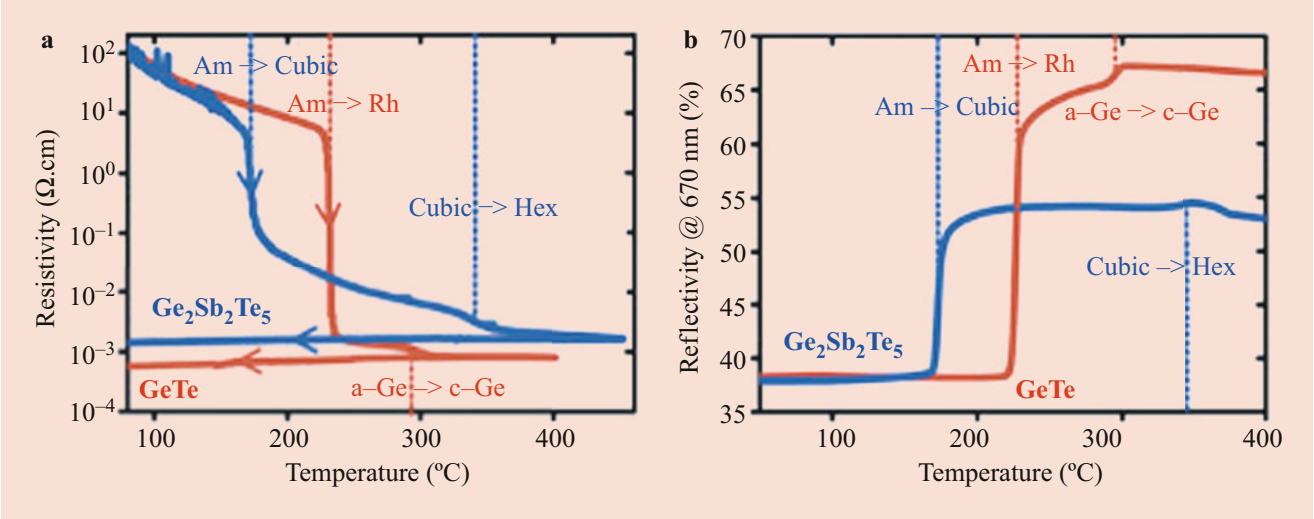

Fig. 30.4 Resistivity (**a**) and reflectivity (**b**) of GST-225 and GeTe during phase transitions as a function of temperature. (Adapted from [33])

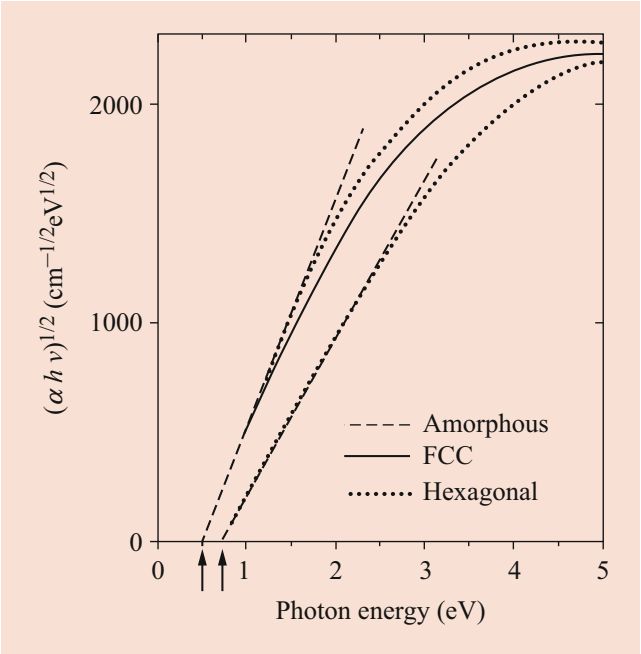

Fig. 30.5 The two arrows point at the optical bandgaps obtained as extrapolations to zero of the absorption coefficients, as from the Tauc equation 30.1. Values of 0.5 eV and 0.7 eV are obtained for crystalline and amorphous GST-225, respectively. (Reprinted from [35], with the permission of AIP Publishing)

negligible differences, but a significant change is found if they are compared to the amorphous phase [35].

The same applies also to the absorption coefficient α (Fig. 30.5), whose steep drop at the lowest energies indicates the band edge. By using the Tauc equation

$$\alpha h\nu \propto \left(h\nu - E_{\mathrm{g}}^{\mathrm{opt}}\right)^{r}, \tag{30.1}$$

with $r = 2$ (indirect bandgap), and extrapolating to the abscissa, an optical bandgap about 0.5 eV is found. Similarly, an optical bandgap about 0.7 eV is found for the amorphous phase; however, in this latter case, a deviation from linearity occurs at energies lower than 0.9 eV [35], which is the typical signature of an exponentially decaying Urbach tail connected to a high density of localized states.

Two sketches of the band diagrams (with associated densities of states, DoS) for the two phases of these prototypical chalcogenide semiconductors are shown in Fig. 30.6. Besides the larger gap of the amorphous phase, there are two more main differences. First, the amorphous phase features a large concentration of localized states spanning the entire gap, which are instead absent in the crystalline counterparts. These localized states significantly modify the density of states, which can be approximated by a continuous function joining the band states, the Urbach tails, and the midgap, deep, localized states. As long as carriers occupy states far from the band edges, their mobility decreases exponentially, thus giving origin to a mobility gap, i.e., an energy region where the mobility of carriers is negligible.

Next, the position of the Fermi level is different. Due to the large number of localized states, the Fermi level in amorphous chalcogenides is pinned close to midgap [36], i.e., amorphous chalcogenides behave like an intrinsic semiconductor with an activation energy for conduction about half of the mobility gap. On the contrary, crystalline chalcogenides are p-type semiconductors with a Fermi level lying close to the top of the valence band, which enables a thermal activation energy for conduction, compatible with a self-doping behavior that can be associated to the large number of stoichiometric vacancies of the crystalline structure. This picture is also confirmed by the hard X-ray photoemission spectroscopy (HXPES) spectra shown in Fig. 30.7 for GST-

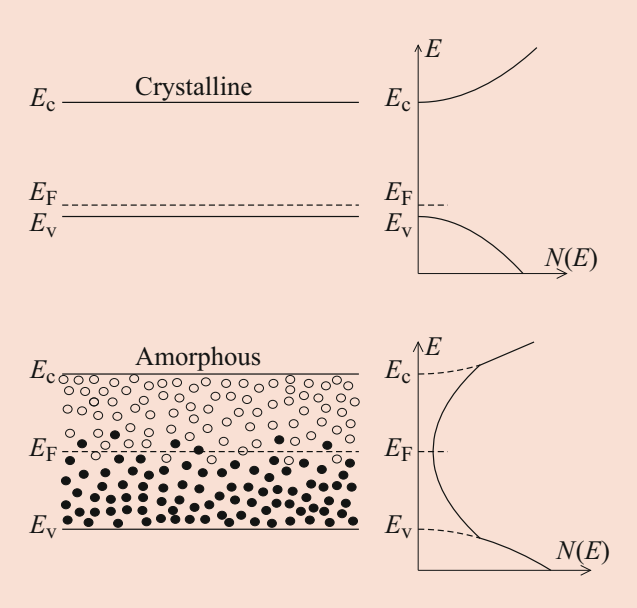

Fig. 30.6 Schematic band structure and DoS of crystalline and amorphous chalcogenide alloys at room temperature. White and solid circles represent empty and filled traps, respectively; the large number of traps originates a continuous DoS within the band gap. The band edges and the position of the Fermi level are also shown

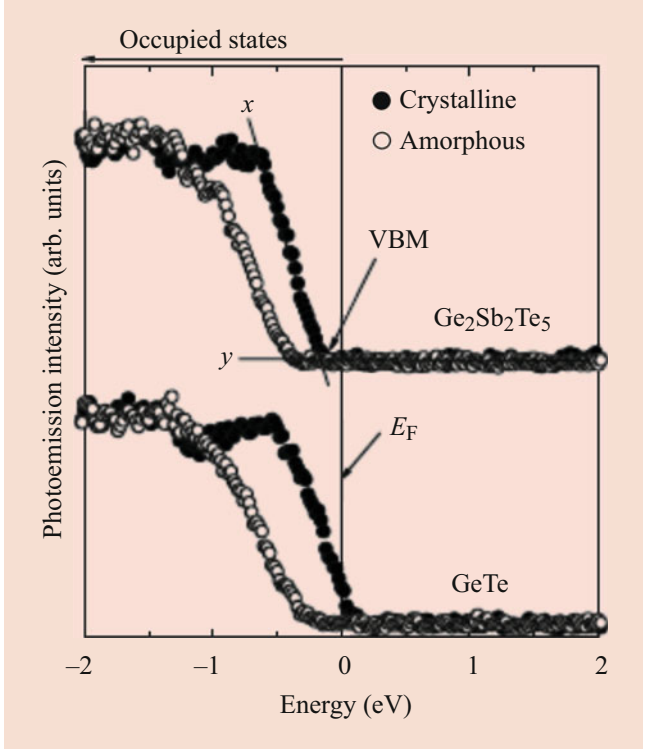

Fig. 30.7 Photoemission spectra near the valence-band maximum of amorphous and crystalline GeTe and GST-225. (Reprinted with permission from [37] © (2007) by the American Physical Society)

225 and GeTe, showing the occupation of the valence band with respect to the Fermi level [37].

The p-type conduction of crystalline GST-225 is further confirmed by Hall mobility measurements [38] and is also claimed for amorphous GST-225 via Seebeck analysis [39]. However, as a result of the strong Fermi-level pinning, the intrinsic semiconductor behavior of the amorphous phase still seems more appropriate due to the negligible carrier concentration in the extended states.

30.3.2 Device Operation

At the end of the fabrication stage, the deposited chalcogenide layer is brought into the low-resistance crystalline, or SET, state. The RESET operation, i.e., the amorphization of the programming region (which usually corresponds only to a portion of the chalcogenide layer), is obtained by heating the material to more than 1000 K, largely above the melting temperature T_m, with a very short electric-pulse of suitable intensity and then rapidly cooling it down. The entire amorphization process can be as fast as few tens of picoseconds [40,41]. This procedure destroys the periodic atomic arrangement typical of the crystalline phase and freezes the atoms in a disordered configuration, because the very fast quenching hinders the atomic mobility and prevents the system from reaching an energy minimum. As a result, a high-resistive amorphous state, also known as RESET state, is reached.

To switch back the material into the SET state, an electric pulse bringing the system into the fast crystallization regime is required. If the temperature is kept between the crystallization temperature T_x and the melting temperature T_m for a sufficient long time, atoms are allowed to move, and the ordered crystalline state is progressively recovered. It is thus evident that the SET operation takes place at temperatures lower than the melting temperature, in the 500–600 K range, but needs a significantly longer time to complete, from some tens to a few hundreds of nanoseconds [40,41].

In order to READ the state of the programmed region, a low voltage, small current pulse that does not alter the actual state of the memory is applied, and the resistance of the cell is determined by a current sense amplifier. A schematic of the READ, SET, and RESET pulses is shown in Fig. 30.8. Note that the two terms SET and RESET are commonly used for both states and programming operations; in order to avoid ambiguity, we shall use SET/RESET state or SET/RESET operation wherever necessary.

Depending on the phase of the chalcogenide layer, two distinct current vs. voltage characteristics are found (Fig. 30.9a). The crystalline phase is basically a simple resistor, and the slope of the $I(V)$ curve is determined by the series of the low-resistive chalcogenide layer and the resistance of the circuit necessary to the memory operation.

The amorphous phase features, instead, a highly non-linear, S-shaped characteristic, in which a high-resistive branch at the lowest voltages and a low-resistive branch at high bias—the latter merging with the characteristic of the crystalline phase—are connected through a negative differential resistance (NDR) branch. The latter is quite unstable, and it is often identified, under current controlled measurements, only by the two portions very close to the switching points.

By deeply analyzing the $I(V)$ characteristic of the amorphous phase, two switching processes can be identified (Fig. 30.9b). In the so-called subthreshold, or amorphous OFF, regime, the current exhibits an Ohmic, an exponential, and a super-exponential regime as a function of the increasing voltage. At a given voltage V_{th}, or threshold switching voltage, the conductivity of the chalcogenide layer rapidly increases. This state is usually addressed as amorphous ON, since no phase transformation has occurred yet. The amorphous ON state corresponds to the NDR branch of the current-driven $I(V)$ characteristic (voltage snapback), whose slope is determined by the load resistance, or to a dramatic steep rise in the current level if the measurement is voltage-driven, as it happens in memory arrays. If the bias is removed with the material in the amorphous ON state, the amorphous OFF state is recovered.

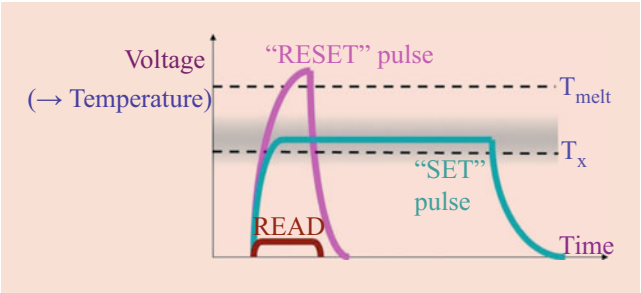

Fig. 30.8 Schematic voltage pulses, with the corresponding temperatures reached in the chalcogenide alloy, required for the operations in a typical PCM cell. (Reprinted with permission from [5] © (2010) American Vacuum Society)

This phenomenon is known as Ovonic threshold switching (OTS) and often triggers a second switching event, the memory switching. The strong increase in the current due to the threshold switching leads, in fact, to a high Joule heating of the chalcogenide layer which, in turn, activates the phase transition to the crystalline state, if the bias persists for a sufficient time.

Yet, OTS does not occur as soon as the bias is applied, and a certain delay time can be measured between the application of an electrical pulse and the beginning of the switching event. The delay time ranges from few nanoseconds to milliseconds, with an exponential dependence on the applied voltage, as shown in Fig. 30.10; in principle, if the applied voltage coincided exactly with the very threshold voltage, the delay time would be infinite, as reported also in [43].

While OTS is reversible, memory switching (MS) is permanent and is responsible for the non-volatile behavior of the PCM. The volume of the amorphous region depends on the temperature field achieved in the chalcogenide layer, whose distribution and maximum value can be tailored by applying electrical pulses of calibrated power. A typical programming curve, i.e., the mapping between the memory resistance and

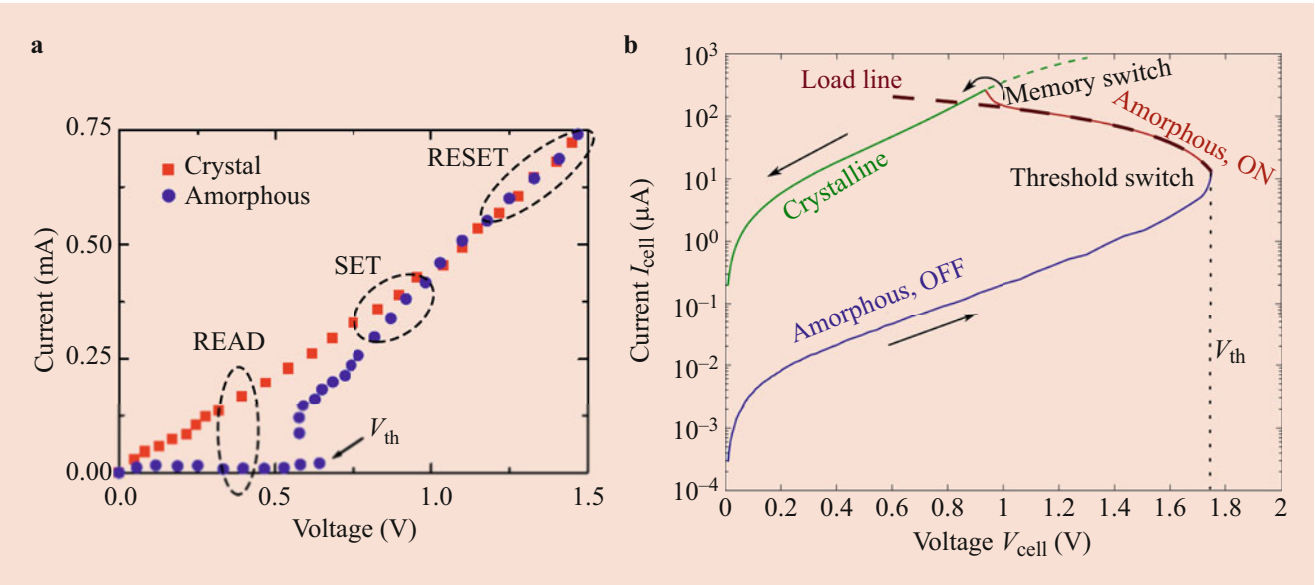

Fig. 30.9 (**a**) Current vs. voltage characteristic of an amorphous and a crystalline GST-225 PCM cell showing the Ovonic threshold voltage V_{th}, and the three conditions for SET, RESET, and READ. (Reprinted from [42], © (2006) with permission from Elsevier). (**b**) Quasi-static current vs. voltage characteristic of a PCM device in a semilog scale. (Adapted from [8], © CC-BY 4.0)

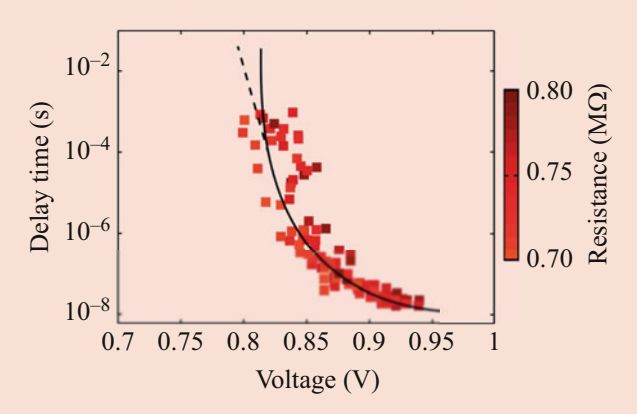

Fig. 30.10 Delay time for threshold switching as a function of the applied voltage. Colors indicate the initial cell resistances. (After [44], © CC-BY 3.0)

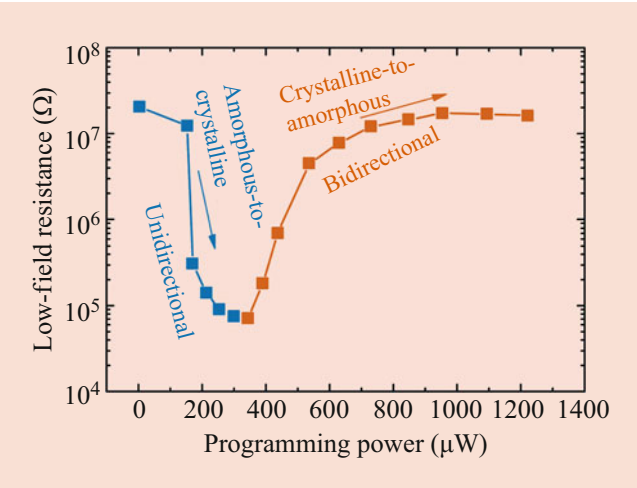

Fig. 30.11 Typical low-field resistance vs. programming power. The same behavior is reported for a large number of alloys, though figures appreciably vary with composition. See text for full details. (After [8], © CC-BY 4.0)

the programming power, is reported in Fig. 30.11. This curve is obtained by setting the amplitude of the programming pulse, reading the PCM resistance and then reverting the PCM to its initial state for a higher programming pulse. The left half of the programming curve describes the sharp transition from a fully amorphized to a fully crystalline layer: after a threshold current is reached, the amorphous region is rapidly converted into a crystalline region with a small-to-negligible modulation of the crystalline volume. Once the SET process is completed, the PCM cannot be switched back to the high-resistive state with a pulse of the same amplitude, irrespectively of the pulse duration. The right half of the programming curve describes the opposite transition, from a fully crystalline to a fully amorphous layer. Such a transition is much broader and is dominated by the timescale of the melt-quench process: the higher the RESET pulse, the bigger the amorphous region, the more resistive the chalcogenide layer. Differently from the left half of the programming curve, the amorphous region can be transformed back to crystalline through a proper calibration of the falling edge of the electrical pulse. More interestingly, the possibility of modulating the PCM resistance in accordance to the programming current paves the way to multiple-level cells (MLC), and reliable solutions up to 4 bits per cell have been demonstrated [45, 46].

Though memory switching is common to all chalcogenides, for certain compositions the melting temperature is so high that in practice it is never reached, or the kinetics of the phase change is slower than the typical pulse duration so that the phase change does not immediately follow the threshold switching event. The material remains in the amorphous ON state even at voltages larger than the threshold switching voltage. If the voltage is progressively reduced, the amorphous ON state is kept down to the so-called holding voltage $V_h < V_{th}$, which is the minimum voltage that sustains the ON state, and then the current falls down to the amorphous OFF level. These chalcogenide materials are not used for storage but have a strong potential for selector devices.

While the physics of MS is well determined by the thermodynamics and the kinetic of the crystallization, that of OTS is still far from being completely understood, though it has been studied for more than 50 years now, and a number of models have been proposed. These models, in fact, are able to properly describe some features of OTS, but none of them provides the full picture yet.

30.3.3 The Ovonic Threshold Switching

The Ovonic threshold switching is undoubtedly the key enabling mechanism of phase-change memories, as it provides the high current necessary for the amorphous phase to switch to its crystalline counterpart. Ridley pointed out in 1963 that S-shaped $I(V)$ characteristics lead to filamentary conduction [19], which is the formation of low-resistance filaments connecting the electrodes within a high-resistance matrix. Most of the models developed up-to-date to interpret OTS are still coherent with such an observation, either by creating unstable crystalline filaments, or by thermal filaments, or by identifying preferred pathways where some kinds of enhanced tunneling/hopping among defective states occur. These models can be classified into three main categories: thermal, electronic, or structural. In the following, we shall summarize the main features of some of them; further information is reported in Chap. ▸ 40. The interested reader can also read more detailed reviews in [7, 8].

Thermal Models

The very first mechanism proposed to explain the threshold switching in phase-change materials is an electro-thermal instability that triggers the switching event [13]. In the thermal models, Joule heating boosts the conductivity, being the latter proportional to the thermal activation of the carriers: $\sigma \propto \exp[-E_a/(k_B T)]$. A positive feedback is established: the higher the current, the more the power dissipation, the higher the conductivity, and so on. If one assumes that Joule heating is predominant along a filament (whose origin basically depends on local non uniformities of the amorphous matrix that induce the initial current concentration), the threshold temperature T_{th} is approximately given by [8]:

$$T_{th} = \frac{E_a}{2k_B}\left(1 - \sqrt{1 - \frac{4k_B T_0}{E_a}}\right), \tag{30.2}$$

where E_a is the activation energy for conduction and T_0 is the ambient temperature. The relationship above requires $E_a > 4k_B T_0$, which is the minimum condition for obtaining a negative differential region in the $I(V)$curve. Interestingly, the same conclusion was also found in [47] for a pure electronic model. Thermal models were abandoned in the 1980s in favor of purely electronic switching mechanisms. Adler [48] observed that the switching event is triggered by a specific value of the electric field, not of a voltage, and for such a reason, the switching event occurs in an extremely small timescale, much lower than the time required for heating the lattice. However, an electro-thermal interpretation of the OTS was proposed again by Bogoslovskyi and Tsendin in 2011 [49] by combining thermal excitation to tunneling from ionized negative U-centers.

Electronic Models

Double-injection electronic models were initially proposed by Henish [50] and Mott [51] but were later abandoned in favor of the generation-recombination model proposed by Adler [52]. This model relies on the idea that valence alternation pairs (VAPs), i.e., pairs of three-fold coordinated, positively charged C_3^+ and one-fold coordinated negatively charged C_1^- chalcogen atoms, enhance the carrier generation and recombination rates, with different time constants for the two processes. Some years later, Pirovano [53] showed that a similar model can be applied to any kind of defects, and not only to VAPs.

In order to obtain the threshold switching condition, it must be assumed that the rates are proportional to the carrier concentration, as happens for impact ionization, the generation term is dependent on the electric field through the Okuto-Crowell equation [54], and the recombination time is modulated by trap filling. The switching point represents the limit condition where recombination is able to balance generation by simply filling traps. In the subthreshold regime, the recombination process is favored by the presence of empty traps, and an equilibrium is established with a generation process that is exponentially dependent on the current. At higher currents, when a vast majority of traps is already filled, the only way to let recombination balance generation is reducing the voltage, so that the generation rate is reduced as well. In order to sustain a high current, a large carrier concentration, as the one produced by impact ionization, must be considered.

The model consists of the standard drift-diffusion equations for electrons and holes, coupled to kinetic equations for trap filling, and to the Poisson and Fourier heat equations, which is also one of its main advantages in view of a possible implementation in TCAD simulators.

Two main shortcomings of generation-recombination models have been evidenced [55]. According to the original work by Adler, the mechanism above takes place in a micrometer-wide filament, which raises a natural skepticism about its applicability to much smaller devices as those made available by the semiconductor industry in the 2000s. Moreover, the model relies on impact ionization, which does not seem compatible in amorphous chalcogenides, as the typical mean free path for carriers is quite small and does not allow them to reach the energy required to ionize neutral defects.

Still bound to the idea of filamentary conduction, Karpov and coworkers proposed in 2007 a unified model for OTS and MS [56]. Their model assumes a field-enhanced nucleation rate that, in turn, decreases the energy barrier for crystallization so that a rod-like embryo of a crystalline filament is formed in the vicinity of the bottom electrode (BE). The very high contrast in the resistivity of the filament with respect to the surrounding amorphous matrix is such that the current is largely gathered by the embryo, thus concentrating the electric field at its edges, and the crystalline filament progressively grows until it connects the electrodes. Once the full filament is created and the field is removed, the filament can either be stable or dissolve according to its radius: if the latter is larger than the minimum thermodynamically stable radius, the filament is stable and MS is achieved, otherwise it dissolves and OTS takes place.

This model presents two strong points: the unified vision encompassing both OTS and MS, and the description of the delay time necessary for OTS to occur, including its dependencies on voltage and temperature. However, it is affected also by two important weaknesses: on the one side, an unstable filament should dissolve at a rather lower field (corresponding to the holding voltage) than the one required for its creation (corresponding to the threshold voltage); on the other side, parameters used to model crystallization do not fully cope with those stemming from its pure thermodynamical description.

Also in 2007, Ielmini proposed a model based on hopping from deep to shallow traps and the non-uniformity of the electric field [57]. At present, this model represents undoubtedly the most credited and used model for OTS nowadays. The model was later reworked by Ielmini himself [58] and mostly by Piccinini at al. [59,60], Buscemi et al. [47,61], Jacoboni et al. [43], and Brunetti et al. [62], who introduced also the self-consistent coupling to the Poisson equation and ended up in a hydrodynamic formalism. Interestingly, Buscemi et al. [47] found the same constraint for the activation energy holding for thermal models, once the carrier temperature replaces the lattice temperature. Cappelli et al. [63] developed also a 3D discrete version of the hydrodynamic model, by which they demonstrated the occurrence of filamentary conduction also with their model. All of these models share the same physical explanation and take into consideration a different level of complexity. Detailed descriptions are reported in Chap. ▶ 40; generally speaking, they can be referred to as hot-carrier models.

In essence, these models consider the co-existence of low-energy, thus low-mobility, states (e.g., deep traps) and states at higher energy, with a higher mobility (e.g., shallow traps and extended band states). In the subthreshold regimes, either Ohmic or exponential, carriers move according to trap-limited conduction, hopping from a low-mobility state to another by tunneling or thermal emission; the carrier distribution is close to the equilibrium distribution. In the super-exponential region, carriers are partially promoted to high-mobility states as a result of the action of the high electric field close to the BE. An out-of-equilibrium carrier distribution featuring a carrier temperature replaces the equilibrium distribution. Since the mobility of carriers in high-energy states is exponentially higher than the one of carriers in deep states, high currents can be sustained with a high field close to the BE and with a much smaller field far from the BE, as long as the carrier concentration in these states is large enough. This originates the positive feedback for OTS: the higher the field close to the BE, the larger the amount of carriers in mobile states, the higher the current that can be sustained with a low field far from the BE, and so on.

While hot-carrier models provide a good to excellent fitting of the $I(V)$ characteristics and of the threshold conditions, they all fail in explaining the measured switching delay time, which is much longer than the one predicted by the models [44].

Structural Models

Besides thermal and electronic models, a new interpretation of OTS was provided in 2020 by Noé et al. [64], who connected the switching mechanism to the presence of the metavalent bonding proposed by Wuttig, Raty, and coworkers [65,66].

Metavalent bonds have been introduced on the basis of many physical parameters, such as hybridization and ionicity, whose values are between those typical of covalent and metallic bonds, as shown in Fig. 30.12. Materials featuring metavalent bonds are also called incipient metals, since their conduction properties can progressively reach values close to those of metals upon the application of a proper driving force.

According to the proposed model, the change of the bonding configuration in chalcogenide glasses is triggered by a high electric field, which has a significant impact on the electronic properties of the OTS materials by increasing the degree of bond alignment. More specifically, states around the Fermi level delocalize and transform from low-conductivity defect states to high-conductivity delocalized channels. The latter are responsible for a dramatic change in the electronic DoS and, in turn, to a huge increase in the electronic conductivity. These changes are metastable and are mostly recovered after the removal of the excitation; however, since the mechanism involves structural modifications, part of them are irreversible and the amorphous structure is unable to recover the full pristine state. This behavior could thus explain the so-called forming (or first firing) of Ovonic materials, according to which the very first switching events occur at higher voltages than the subsequent ones.

30.3.4 Memory Switching and the Physics of Phase Change

The physics at the basis of the phase change in chalcogenide materials is nothing but the physics of a phase transition in a solid system, as described by Avrami in the late 1930s and early 1940s [67–69]. The driving force for crystallization is the difference in Gibbs free energy that exists between the amorphous (or the liquid) and the crystalline phase. At first, a crystalline nucleus is created. This can happen either in the bulk (homogenous nucleation) or close to a surface, an interface or an impurity (heterogeneous nucleation), but since heterogeneous-nucleation rates dominate over homogenous-nucleation rates, the crystallization process begins quite often at an interface between two materials [70].

According to classical nucleation theory, clusters of crystallites are created as a result of two competing phenomena: the addition of a new crystallite to an existing crystallite and the detachment of a crystallite from a formed cluster. The process of cluster formation is governed by the reversible work of formation, which is the result of two components: the energy gained by forming the crystal phase and the energy required by the surface formation between the crystalline and the amorphous phase. The critical quantity is the variation of the Gibbs free energy $\Delta G = G_{\text{crystal}} - G_{\text{liquid}}$ [70]:

$$\Delta G = -\Delta g V + \gamma S, \tag{30.3}$$

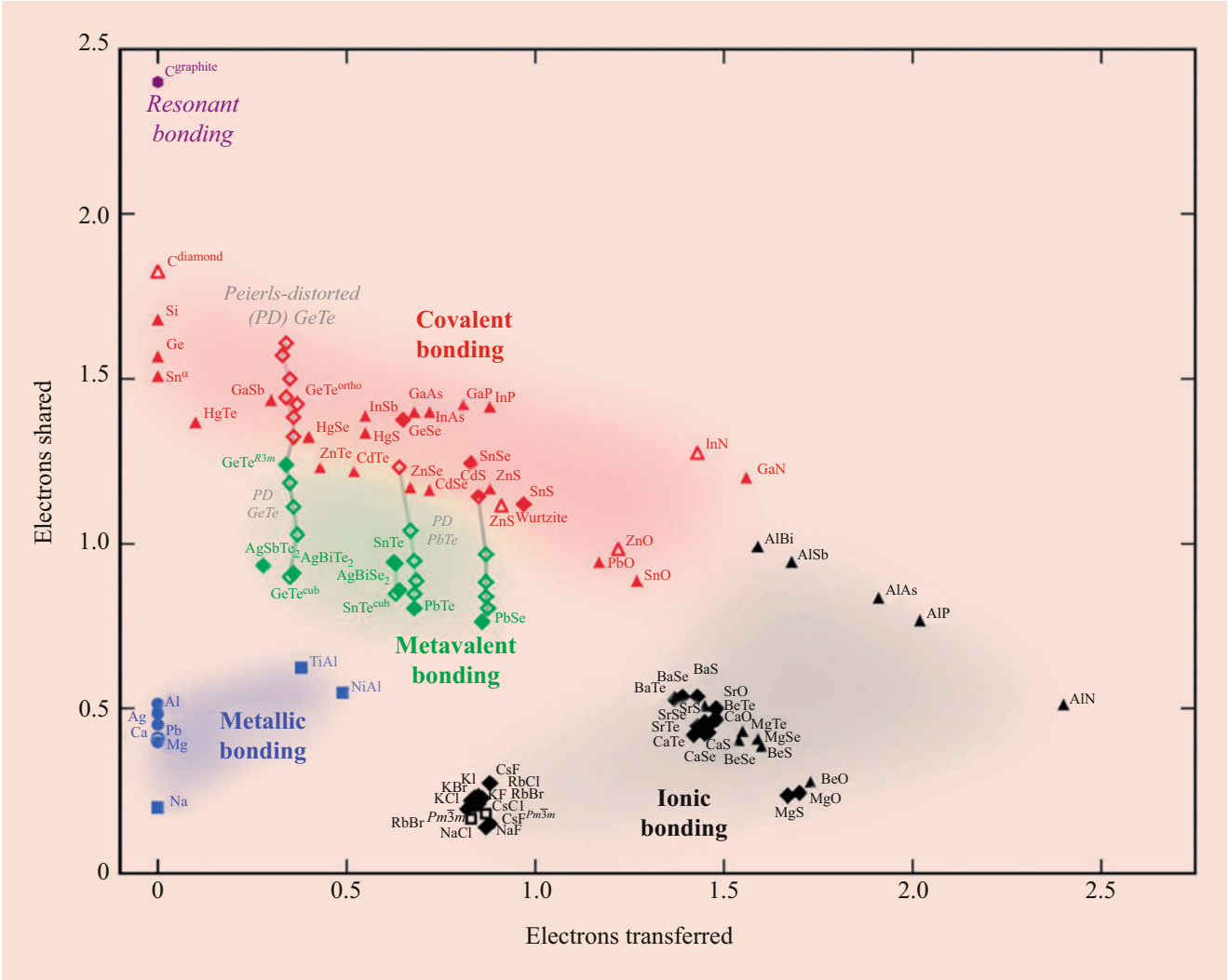

Fig. 30.12 Map of electronic interactions and bonding of many materials. The amount of electrons transferred between neighboring basins is a measure of the ionicity of the bond, while the amount of electrons shared is a measure of its covalent character. Metavalent bonding is collocated between covalent and metallic bondings. Adapted from [66], with permission from John Wiley & Sons Inc.

where $\Delta g = g_{\text{liquid}} - g_{\text{crystal}}$ and γ are the bulk-specific free energy difference between the amorphous and the crystalline phase and the surface-specific free energy, respectively, and V and S are the volume and the surface of the crystallite. Note that $\Delta g < 0$ above the melting temperature T_{m}, and γ is positive, thus unfavorable to crystallization. For spherical crystallites at $T < T_{\text{m}}$, ΔG has a maximum at the critical radius $r_{\text{c}} = 2\gamma/\Delta g$, which represents the minimum size for clusters to be stable. The nucleation rate reads [71]:

$$I = K \exp\left(-\frac{\Delta E_{\text{a}}}{k_{\text{B}}T}\right) \exp\left[\frac{-16\pi\gamma^3}{3(\Delta g)^2 k_{\text{B}}T}\right], \qquad (30.4)$$

ΔE_{a} being an activation energy at the surface, and the bulk free energy difference being expressed as $\Delta g = \Delta h_{\text{f}} f(T_{\text{m}}, T)$, with Δh_{f} the specific enthalpy of fusion. Several empirical approximations have been proposed for $f(T_{\text{m}}, T)$; among them, many authors agree on that by Singh and Holtz [72].

After nucleation has occurred, a stable cluster can grow. New atoms from the amorphous phase hit the cluster with frequency ω and can attach to the cluster if they are able to overcome the energy barrier $\Delta E'_{\text{a}}$, which may differ from the activation energy ΔE_{a} above. Similarly, some atoms can detach from the cluster if they overcome the same energy barrier $\Delta E'_{\text{a}}$ modulated by the difference in the Gibbs free energies of the clusters before and after detachment $\Delta G_n - \Delta G_{n-1}$. The cluster growth velocity can thus be expressed as [6]:

$$v = \beta\lambda\omega \exp\left(-\frac{\Delta E'_{\text{a}}}{k_{\text{B}}T}\right)\left\{1 - \exp\left[-\frac{\Delta g V}{k_{\text{B}}T}\left(1 - \frac{r_{\text{c}}}{r}\right)\right]\right\}, \qquad (30.5)$$

where λ is the typical crystallite size, β is a geometrical factor, and r is the cluster radius. When $r \gg r_c$, the growth velocity depends only on the temperature and has a maximum close to the melting temperature.

A phase-change alloy can be classified as growth-dominated if it features long incubation times, low nucleation rates, and high growth velocities. On the contrary, when relatively short incubation times, high nucleation rates, and moderate growth velocities prevail, the alloy is nucleation-dominated. As is evident from the formulas above, nucleation rates and growth velocity are functions of the temperature, so that the same compound can behave as a nucleation-dominated material at low temperatures and as growth-dominated material at high temperature. Typical activation energies for nucleation of chalcogenides along the GeTe-Sb_2Te_3 tie line lie in the range 2.5–4.0 eV, whereas slightly lower values have been derived for the growth process, according to growth velocities in the range tens of nm/s to few pm/s [6].

In order to account for memory switching, the thermodynamical model above must be coupled to any of the transport models summarized in the previous paragraph and to the Fourier heat equation. The full model is tackled only numerically, due to the strong non-linearity affecting the constitutive equations. While many numerical schemes can be applied to solve the transport equations, the thermodynamics of the phase change is mostly solved by means of Monte Carlo techniques that provide a very accurate description of nucleation, crystal growth, and dissociation [73, 74] and also take into account the intrinsic stochasticity of the process [71, 75].

30.4 Materials and Devices

30.4.1 Materials and PCM Performances

The key requirements for a PCM device may vary significantly upon the specific application the memory is designed for. Generally speaking, the PCM must have a fast SET speed (<100 ns), a limited RESET current (values lower than 200 μA whenever possible), a high endurance (typically $>10^8$ cycles), and a long data retention (more than 10 years at 85 °C; stricter requirements apply instead to embedded-PCM for automotive applications). Besides these properties that are mostly linked to the chalcogenide composition, a good scalability and a low intra- and intercell-variability of the threshold condition and of the ON and the OFF resistance are also a plus from the technological standpoint [8].

Demonstrators of PCM cells have been designed to largely overcome one or a few of these constraints, but none of these prototypes meets the entire set of requirements altogether, or can easily be moved to the fabrication stage at the industrial level.

Table 30.2 Most relevant phase-change material parameters and their influence on the PCM performances

Phase-change material parameter	Influence on PCM performances
Crystallization temperature and thermal stability of the amorphous phase	Data retention and memory lifetime
Melting temperature	RESET power
Resistivity in amorphous and crystalline phases	ON/OFF ratio SET and RESET current
Threshold voltage	SET and READ voltages
Thermal conductivity	SET and RESET power
Crystallization speed	SET pulse duration (power) Data rate
Melt-quenching speed	RESET pulse duration (power)

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The most important material parameters that influence the performance of a PCM are listed in Table 30.2.

The crystallization temperature T_x is defined as the lowest temperature at which the crystallization takes place in a time scale compliant with the technological needs. The crystallization temperature represents the upper bound for data retention in the amorphous state, though it does not give any precise measure of data loss at lower temperatures after a sufficient long time from the programming operation. In other words, it is a measure of how hot a PCM cell can become before immediately losing the stored information. The crystallization temperature is strongly dependent on the material composition, the layer thickness, the presence of defects in the bulk of the alloy, or on the metallization lines at the boundary of the chalcogenide layer. Raoux et al. [76] reported that some chalcogenides are able to crystallize films as thin as 1.3 nm or in nanoparticles about 2 nm in diameter in a longer time with respect to their thicker counterparts, which is a key enabler for the extreme scalability of the PCM technology.

The melting temperature is also dependent on the composition, and to a lesser extent, on the size in ultra-thin films, nanowires, and nanoparticles. As a rule of thumb, the lower the melting temperature, the better the PCM. As a matter of fact, the melting temperature dominates the power required for the RESET operation, which is the most energy-demanding programming operation, and the reduction of the high energy consumption per bit is one of the most challenging open issues for the PCM technology.

The difference in resistivity between the amorphous and the crystalline phases contributes to defining the memory window of PCM, which is determined through the ON/OFF ratio, i.e., the ratio between the current in the SET and RESET states upon the application of a READ pulse. The best alloys for phase-change memories exhibit a very large theoretical contrast up to five orders of magnitude, even

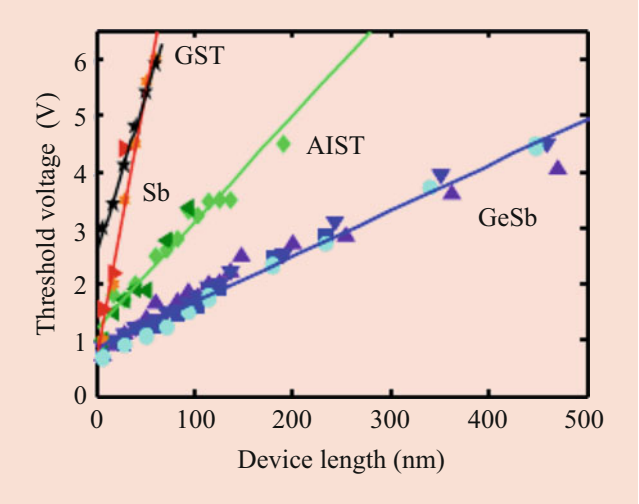

Fig. 30.13 Experimental threshold voltage vs. device length for various phase-change materials. The intersection with the *Y*-axis are attributed to the contact resistances. (Reprinted from [77], with the permission of AIP Publishing)

though, in practice, the ON/OFF ratio never exceeds two orders of magnitude due to technological constraints. In fact, from the one side, the series of the contact resistance and the circuitry resistance is higher than the resistance of the crystalline chalcogenide, thus becoming the dominant factor; from the other side, the resistivity of the amorphous phase is determined by the kinetics of the melt-quench process, yielding a different value than an as-deposited layer. A large ON/OFF ratio is a fundamental condition for designing multiple level (or multibit) cells, so that also intermediate resistances can be exploited for data storage. Moreover, the resistivity slightly increases for both phases with scaling: this is beneficial also in the reduction of the programming currents, as higher voltages drop across the chalcogenide layer and higher Joule heating is present.

Another parameter that has a strong influence on the programming currents is the threshold voltage or, more appropriately, the threshold field. Studies and theoretical models have in fact shown that the threshold voltage scales linearly with the thickness of the amorphous layer, and no deviations have been observed down to 10 nm (Fig. 30.13). The ideal value for the threshold voltage is about 1 V (corresponding to a threshold field about 10–100 MV/m), which is considerably higher than the typical reading voltage (few hundreds of mV to ensure a proper separation far beyond noise between the SET and RESET states of the $I(V)$ characteristic), sufficiently lower than the SET voltage, and compatible with the integration with an access device.

The thermal conductivity impacts the thermal response of a PCM cell to the programming conditions. In practice, the lower thermal conductivity, the lower the energy required for the RESET operation, and this is achieved by scaling rather than acting on the composition of the chalcogenide alloy [5].

Among these parameters, the crystallization speed and the melt-quenching speed are probably the most critical ones, as they define whether a material is suitable for being exploited in the PCM technology or not. In order to be competitive, PCM must be fast, with a crystallization time in the nanosecond time scale. The entire PCM technology relies on the possibility to modulate electrical pulses with *fast* or *slow* falling edges. The difference between what should be considered fast and what should be considered slow is given by the crystallization speed: pulses whose thermal effects are faster than the crystallization speed will amorphize the material, provided that a temperature higher than the melting temperature is reached, whereas slower pulses will lead to recrystallize the bit. Generally speaking, the melt-quenching speed should be at least one order of magnitude faster than the crystallization speed, which determines the achievable data transfer rate. Downscaling is beneficial for both the crystallization and the melt-quenching speed, as the transient components in the Fourier heat equation are shorter.

The elemental crystallization processes (nucleation, crystal growth, and dissociation) typically follow the Arrhenius law for activated processes. Due to activation energies in the 2–4 eV range [6], differences have been observed up to 15–20 orders of magnitude in the crystallization time between room temperature and the melting temperature. Such a large difference prevents the spontaneous recrystallization and leaves the amorphous phase unchanged for years after RESET (retention time), even though a continuous relaxation of the amorphous phase occurs leading to resistance drift. The latter is evidenced by a continuous decrease of the conductivity of the amorphous layer with time, whose effects are of null interest for single-bit cells, but can be extremely detrimental for a MLC where the information is encoded by means of intermediate and narrow resistance windows. As shown in Fig. 30.14, resistance drift is negligible in the crystalline phase. A more detailed explanation of resistance drift can be found in Chap. ▸ 40.

30.4.2 PCM Device Architectures

As reported above, the most serious concern for the PCM technology is given by the large current required for the RESET operation, whose average density has been estimated as $J_{\mathrm{RESET}} \sim 40$ MA/cm^2, which projects the energy consumption for the RESET operation at about 20 pJ/bit [79]. As shown in Fig. 30.15, with advanced prototypes of PCM obtained with carbon nanotube electrodes, it is possible to reduce the energy consumption down to ∼100 fJ/bit, and a theoretical limit as low as 100 aJ/bit has been estimated [80, 81].

The high current density required by the RESET operation is not only a challenge per se but strongly limits the compatibility with standard selector devices like FETs used in a memory array to address the single bits, unless very large transistors are used to drive the current. Alternatively, the dimensions of the phase-change volume are decreased sub-lithographically.

According to the way sub-lithographic features are implemented, PCM cell structures can be classified as [5]:

- *Contact-minimized* cells (Fig. 30.16a), where the sub-lithographic element is represented by a narrow BE, usually made of TiN, on top of which a chalcogenide layer is deposited. The reduced cross-section of the BE determines the high current density required to heat up the chalcogenide, so that the BE also acts as an external source of heat. This configuration is known also as mushroom cell, since the amorphized dome on top of the heater resembles the cap of a mushroom.
- *Volume-minimized* cells (Fig. 30.16b), where the sub-lithographic element is given by a confined chalcogenide volume. Contrarily to contact-minimized cells, the phase change in volume-minimized cells is guaranteed primarily by the power dissipated in the confined chalcogenide volume via Joule heating, so that these cells are also referred to as confined, self-heating cells.

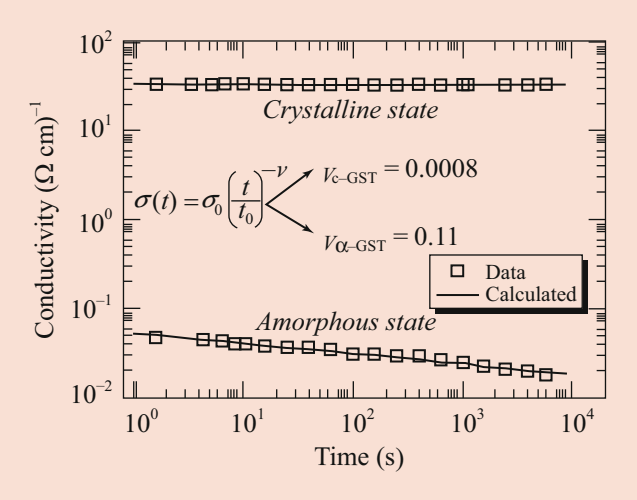

Fig. 30.14 Conductivity as a function of time for the amorphous and crystalline states for GST-225. The trend with time is described by the power law $\sigma = \sigma_0(t/t_0)^{-\nu}$. (Reprinted from [78], with the permission of AIP Publishing)

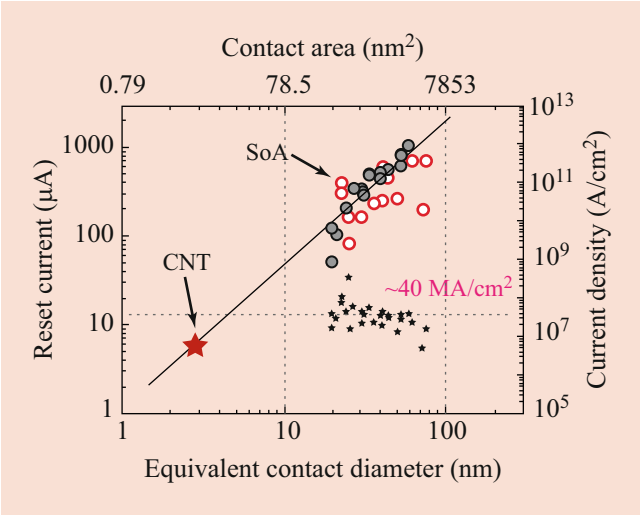

Fig. 30.15 Trend of RESET current as a function of contact diameter in PCM. Experiments performed using carbon-nanotube electrodes (CNT) demonstrate a potential for further reduction with respect to the state of the art (SoA) of about two orders of magnitude. Small stars correspond to SoA current densities and refer to the right *y*-axis. (Reprinted, with permission, from [80] © (2011) AAAS)

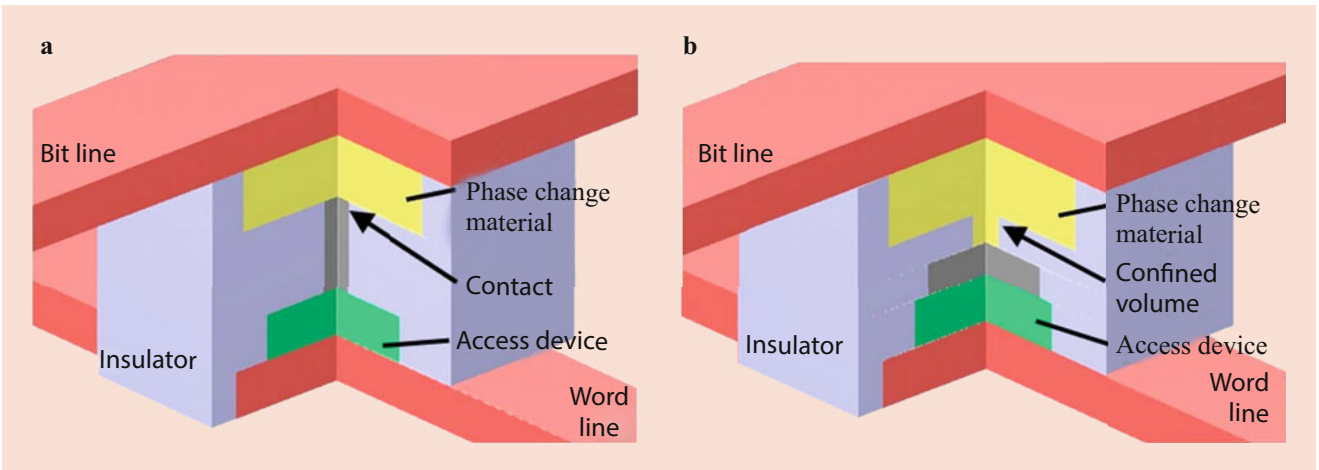

Fig. 30.16 (**a**) Schematics of a contact-minimized cell and (**b**) volume-minimized cell. (After [82]; courtesy of IBM Corporation, © (2008) IBM Corporation)

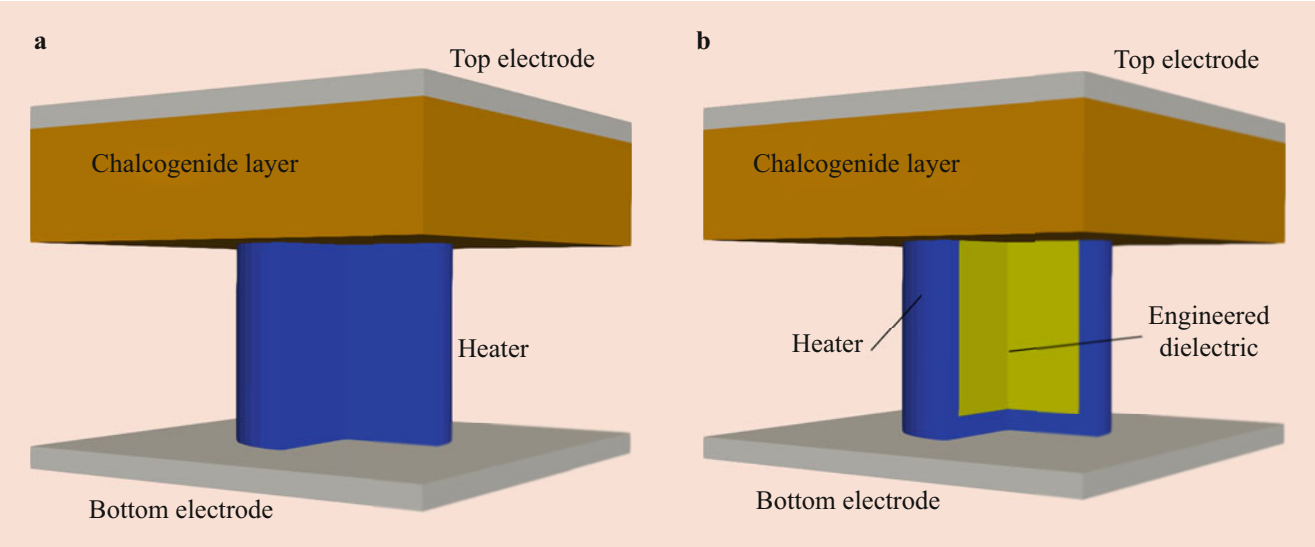

Fig. 30.17 (**a**) Matchstick and (**b**) ring architectures. A quarter of the heater has been removed to show the internal structure of the pillar; the surrounding oxide is not represented

Contact-Minimized Cells

In mushroom cells, the main thermal contribution to the phase change is generated outside the chalcogenide volume along the heater, owing to its purely resistive nature. The hottest spot has been estimated inside the chalcogenide material close to the BE, where self-heating adds to the thermal power flowing across the interface. Moreover, due to inefficient phonon scattering at the heater/chalcogenide interface, a thermal boundary resistance (TBR) also sets in, locally increasing the temperature. The presence of this additional element makes the cell more complex to manufacture and opens new challenges on the material side, as the heater must ensure good compatibility with the phase-change alloys both for mechanical adhesion and absence of cross-contamination. Furthermore, it must provide a good resistivity to induce the phase change and an endurance with cycling similar to that of the chalcogenide alloy.

The first developed PCM cell with a heater is the matchstick structure, where the heater is a simple pillar grown within a surrounding oxide, with a large chalcogenide layer on top (Fig. 30.17a). In order to engineer the heater/chalcogenide resistance and/or adhesion, or to hinder undesired species diffusion activated by the hot temperature, functionalized interfacial layers can be deposited in between.

Rather than filling the entire pillar of the matchstick structure, in the ring structure (Fig. 30.17b), the heater is made of an outer TiN layer and of an inner part filled by a dielectric material engineered to achieve the optimal thermal performance [83]. Using this architecture, an about 10% reduction of the RESET current is achieved.

The μ-trench architecture (Fig. 30.18) represents an effective alternative way to reduce the contact area [84]. Instead of depositing a planar chalcogenide on top of the heater, a dielectric layer is deposited first, and part of it is etched away in correspondence with the heater, so that the chalcogenide layer can fill the gap. The μ-trench geometry allowed an optimized RESET current about 300 μA at the 90 nm technology node. The most advanced contact-minimized PCM structure

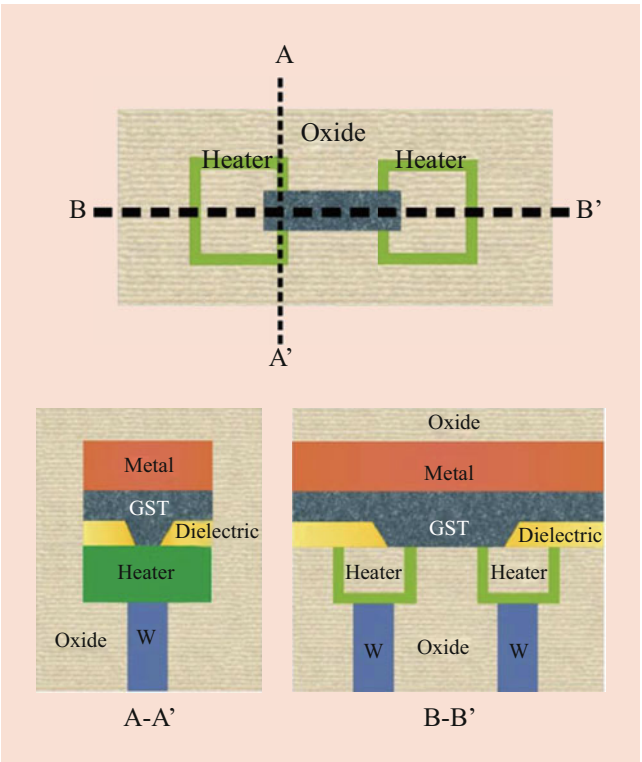

Fig. 30.18 Top view and cross-sections on planes AA′ and BB′ for a μ-trench cell. (Reprinted from [42], © (2006) with permission from Elsevier)

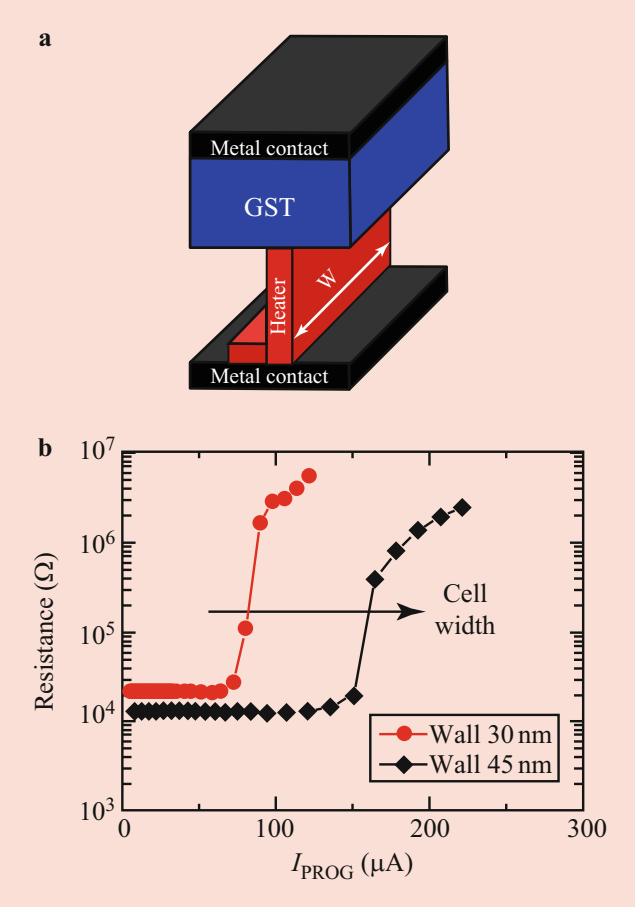

Fig. 30.19 3D sketch of the heater-based wall structure (**a**) and $R(I)$ programming curves (**b**) measured for two different widths W. (Reprinted, with permission, from [85] © (2014) IEEE)

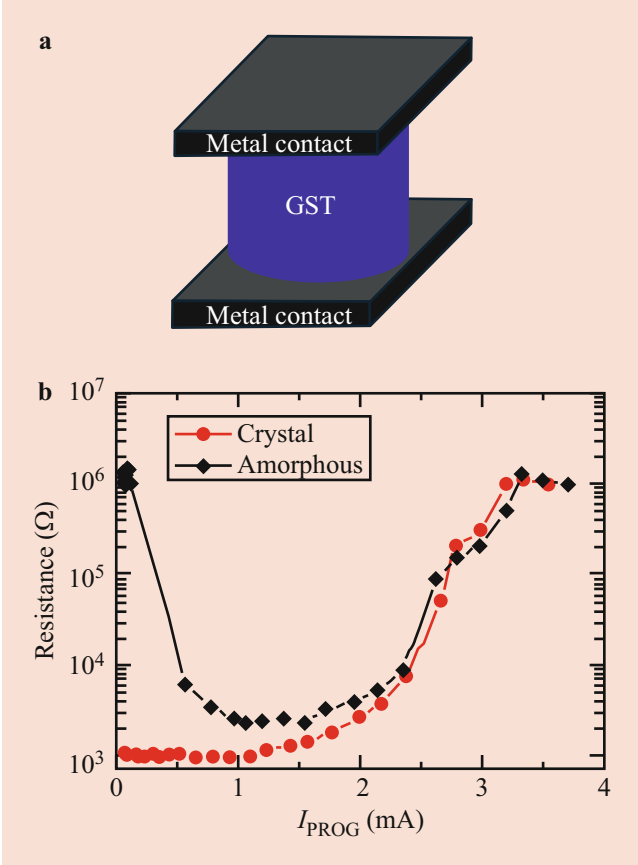

Fig. 30.20 3D sketch of the self-heating pillar structure (**a**) and $R(I)$ programming curves (**b**) for the initially crystalline and initially amorphous states. (Reprinted, with permission, from [85] © (2014) IEEE)

that has been adopted so far by PCM manufacturers is the wall geometry (Fig. 30.19). In this case, an L-shaped heater connects the metallization to the chalcogenide layer on top of its thin vertical wall. With a wall structure, a RESET current of about 200 μA has been obtained at the 45-nm technology node [85].

Volume-Minimized Cells

Self-heating PCM devices rely only on the heat generated by the current flowing through the chalcogenide layer. The main advantage of this solution is given by the simplified layout, which gets rid of all the wear-out mechanisms related to the heater; however, these cells may require extremely high current densities to initiate the phase change, which always occurs in the middle of the chalcogenide layer. The maximal efficiency is pursued by means of a geometrical optimization.

The simplest volume-minimized cell is the so-called pillar structure (Fig. 30.20), where a prismatic volume of chalcogenide material is sandwiched between two metal contacts and is sealed on the sidewalls by an oxide. The high programming current (about 3 mA for a 45 nm wide chalcogenide [85]) limits the application of the pillar structure, unless a very high aspect ratio for the chalcogenide prism is considered.

In order to mitigate the impact of resistance drift and improve the reliability of the cell, preventing also void formation upon cycling, some manufacturers introduced a metallic liner to surround the chalcogenide volume [86].

A step further from the pillar structure is represented by the self-heating vertical wall structure (Fig. 30.21), where the chalcogenide material is deposited according to an L-shaped geometry, whose largest base is connected directly to the BE. The programming current can be reduced significantly by controlling the width of the chalcogenide wall. The limiting factor attaining the wall structure is the strict geometrical alignment to be achieved with a complex deposition of the chalcogenide and of the surrounding oxides.

Line and bridge cells (Fig. 30.22) are created by patterning a thin layer of chalcogenide on top of a dielectric substrate. In line cells, this layer grows wider far from the active region and is directly contacted by metal pads, whereas in bridge

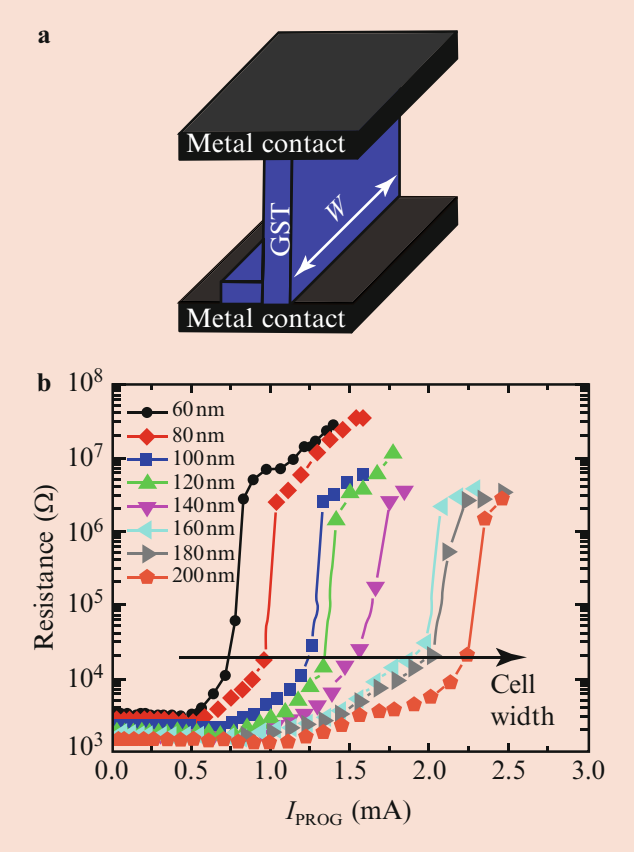

Fig. 30.21 (**a**) 3D sketch of the self-heating wall architecture and (**b**) $R(I)$ programming curves with different wall widths W. (Reprinted, with permission, from [85] © (2014) IEEE)

cells also the contacts are buried in the substrate under the chalcogenide thin layer. These cells do not allow for the creation of a dense array but are quite useful for material testing and early prototyping [85].

In Fig. 30.23 several figures of merit (high-density, efficiency, optimizations, easiness of integration, and manufacturing complexity) are pictorially evaluated in a radar plot. Self-heating cells slightly outperform heater-based solutions in terms of efficiency but introduce some manufacturing issues at the process, integration, and optimization levels. The wall structures, either self-heating or heater-based, allow for a high density due to their shape factor. The optimal trade-off is thus represented by the heater-based wall structure. On the one side, this architecture benefits from its aspect ratio, which is particularly interesting for dense packing, and on the other sides from multiple optimization knobs and a high integration level, suffering only from a limited lower efficiency and higher process complexity due to the larger number of manufacturing steps.

Cross-Point Arrays

Being two-terminal devices, PCM cells are arrangeable in cross-point arrays (i.e., arrays where orthogonal bit-lines and word-lines are created on two parallel planes, with the memory elements in between) with a footprint on the order of $4F^2$, provided that they can be addressed individually. As sketched in Fig. 30.24, even denser arrays can be reached when multiple layers are stacked on top of each other, further reducing the footprint to $4F^2/L$ where L is the number of layers considered, though this solution is limited by the wear-out connected to the necessary circuitry. In order to select single-memory cells, an access device, or selector, must be connected in series to the storage element so that, ideally, no disturb occurs in the neighboring cells when any operation (either READ, SET, or RESET) is performed on a *selected* cell. The selector acts then as a normally OFF switch, and it is temporarily activated only when its storage element in series is read or programmed. A selector must be capable to supply, in the ON state, the high current density required by the most critical programming operation, which means a current density on the order of several MA/cm^2. On the contrary, the OFF-state leakage current must be as low as possible, and a good selector should provide a very large ON/OFF current ratio, ideally as high as 10^5–10^6, though in real devices it is limited to 10^2–10^4. In order to satisfy these two constraints, the $I(V)$ characteristic of an access device should be highly non-linear with a steep rise of the current above a given voltage threshold.

Furthermore, the selector must match the voltage requirements of the memory element it is paired to. In particular, the voltage drop across *half-selected cells*, sharing the same word-line or the same bit-line with the selected cell, should always guarantee a low leakage current not to degrade the selectivity of the access device. The threshold voltage of the selector has to be stable and repeatable to minimize cell-to-cell variability and noise effects. Usually, this is achieved by finding a selector whose resistivity is much higher than the memory resistivity in the RESET state. Furthermore, the selector threshold voltage should also be sufficiently higher than the switching voltage of the partner memory and with a small stability window on the order of 0.3 V or less. It is also important that the holding condition, that defines the minimum current and/or bias to sustain the ON state, be significantly lower than the operation condition, in order to avoid undesired oscillations between the ON and the OFF states.

Finally, the access device should not limit the memory performance, i.e., the properties of the selector should outperform those of the companion memory cell in terms of switching speed, cycling endurance, and reliability.

As reported in [4], several memory-cell selectors have been tested to be paired to PCM cells. As it regards conventional devices, such as diodes or transistors, the large RESET current density points at diodes/BJTs or large-sized MOSFETs. The latter makes integration quite challenging due to the huge dimensions of the access device with respect to the small storage elements, nearly preventing dense arrays.

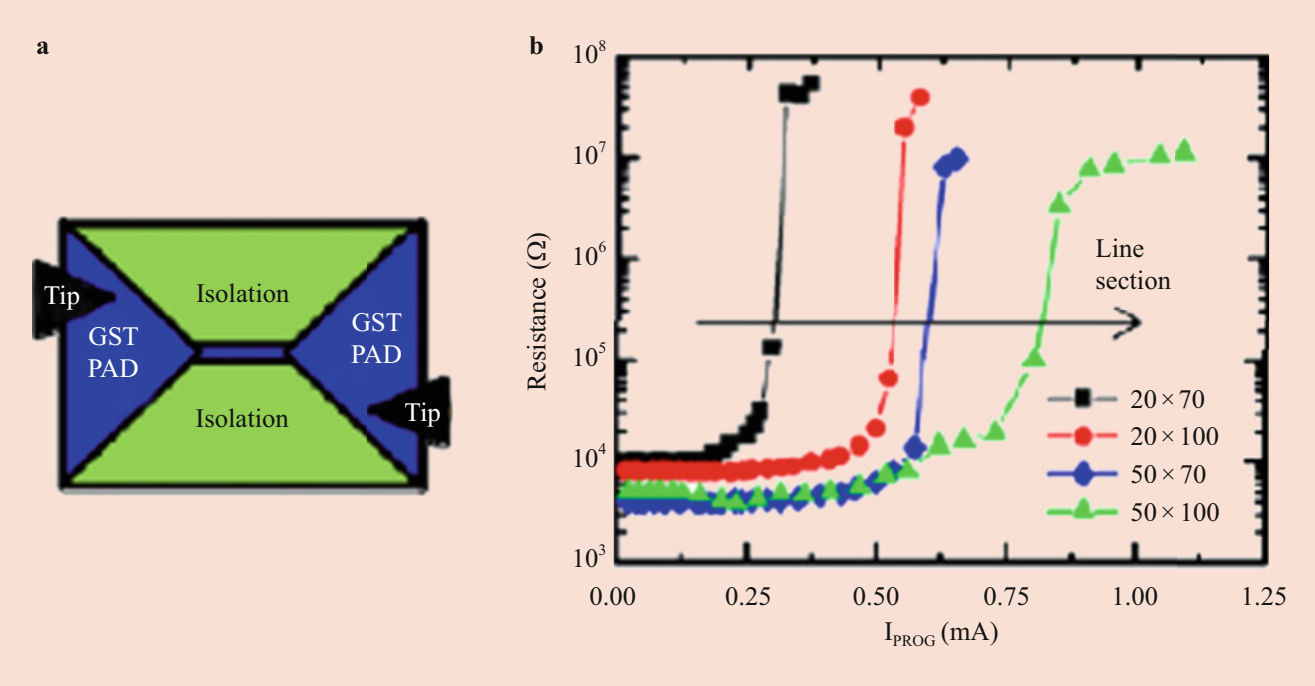

Fig. 30.22 (**a**) Top view of the planar line/bridge architecture and (**b**) $R(I)$ programming curves for different cells with different line sections. (Reprinted, with permission, from [85] © (2014) IEEE)

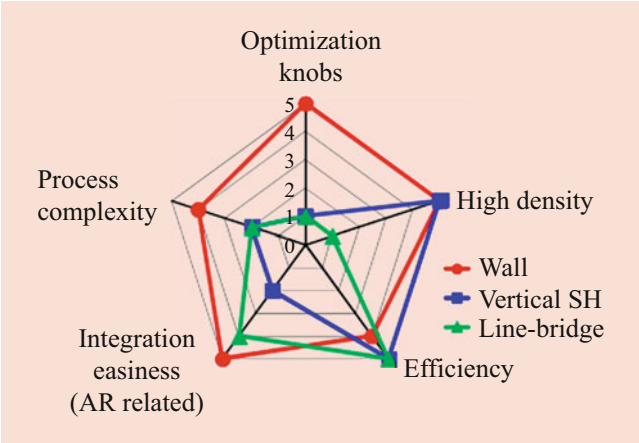

Fig. 30.23 Comparison of strengths and weaknesses for heater-based wall, vertical self-heating, and line/bridge cells. (Reprinted, with permission, from [85] © (2014) IEEE)

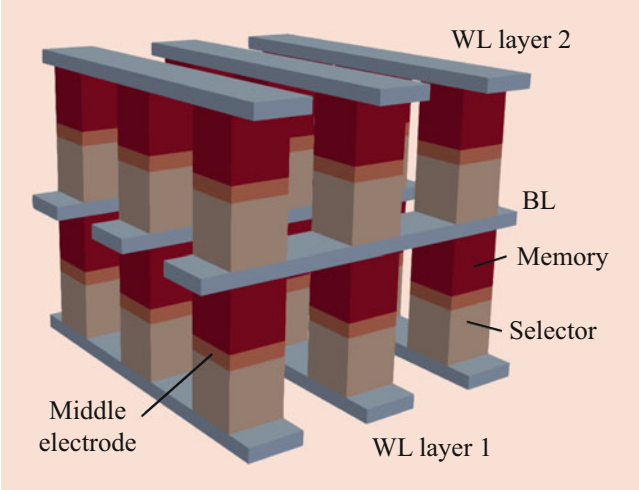

Fig. 30.24 Schematic of a cross-point array with two layers stacked one on top of the other. Each cell is composed of a selector and a partner memory, separated by a metal line to prevent the interdiffusion of the chalcogenide alloys

New configurations and new materials have been investigated to increase the bit density. Among them, Ovonic materials can be tailored to match many of the requirements above (Table 30.3), and in the last 10 years, they have intensively been studied as the most promising candidate for pairing a PCM device, after Intel revealed the integration of an OTS access device on top of a PCM cell in a stackable cross-point architecture [24]. In 2015 Micron and Intel jointly announced their 3D XPoint™ memory, a cross-point array with a vertically stacked double layer of GST-based PCM cells and As-doped Se-Ge-Si OTS selectors [26], and a similar announcement was made also by SKHynix 3 years later [87].

When an OTS selector is connected in series to a PCM, the two $I(V)$ characteristics merge. In Fig. 30.25, these $I(V)$ curves are reported when the PCM is either in the SET or

in the RESET state. When the PCM is in the SET state, the threshold voltage $V_{th,S}$ is close to the OTS threshold voltage, since the PCM is merely a low loading resistance; on the contrary, with the PCM in the RESET state, the overall threshold voltage $V_{th,R}$ is significantly higher than the OTS threshold voltage alone, as the voltage drop across the PCM must be sufficient *per se* to turn the memory to its ON state. By applying a voltage pulse between $V_{th,S}$ and $V_{th,R}$, the selector is always in the low-resistance state, and the PCM state is thus read; pulses larger than $V_{th,R}$ are instead used for programming the PCM. In practice, in order to prevent disturbances, the OTS material should be engineered to have a threshold voltage higher than half of the voltage required by the RESET operation, including the variability window of the threshold voltage itself.

The interested reader can find a comprehensive review about access devices, their figures of merit, and requirements in [89] and on the state of the art of cross-point PCM arrays in [88, 90].

Table 30.3 Main properties of a few cutting-edge selectors for PCM cross-point arrays

	OTS	MIEC	Doped α-Si
Material	AsTeGeSiN	Cu-based	As-SiO_2
I_{off}	10 nA@ 0.5 V_{th}	10 pA@ 0.5 V_{th}	20 nA@ 0.7 V_{th}
I_{on}	100 μA	10 nA	>100 μA
V_{th} adjustability	Good	No	Limited
Endurance	$>10^8$	$>10^5$	$>10^5$

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30.5 Reliability and Perspectives

30.5.1 PCM Reliability

The superior performances of PCM devices in terms of speed and scalability reviewed in Sect. 30.4.1 must be accompanied by a high degree of reliability. Reliability primarily depends on the inherent instability of the amorphous phase, which spontaneously tends to recrystallize, and on the changes in the local alloy composition over time owing to component segregation induced by the electric field or temperature. Failure mechanisms can be classified according to the usage specifications that are impacted: data retention, read disturb, and thermal disturb, all connected to the nature of the amorphous phase, and cycling endurance, linked instead to the local composition and to the response of the whole device.

Data Retention

A data retention failure may occur when the resistance of a programmed bit shifts with time and affects only the RESET state, since the SET state is thermodynamically stable. After being programmed, the resistance of the cell initially increases with time (resistance drift), then, when spontaneous recrystallization begins, it progressively drops to low values. When the threshold that separates the SET and RESET states is crossed, the information is lost. While resistance drift is a concern only for phase-change MLCs, recrystallization is observed sooner or later for all chalcogenide alloys and impacts all kind of devices. The typical criterion adopted for data retention requires fewer than 1 ppb failures at the array

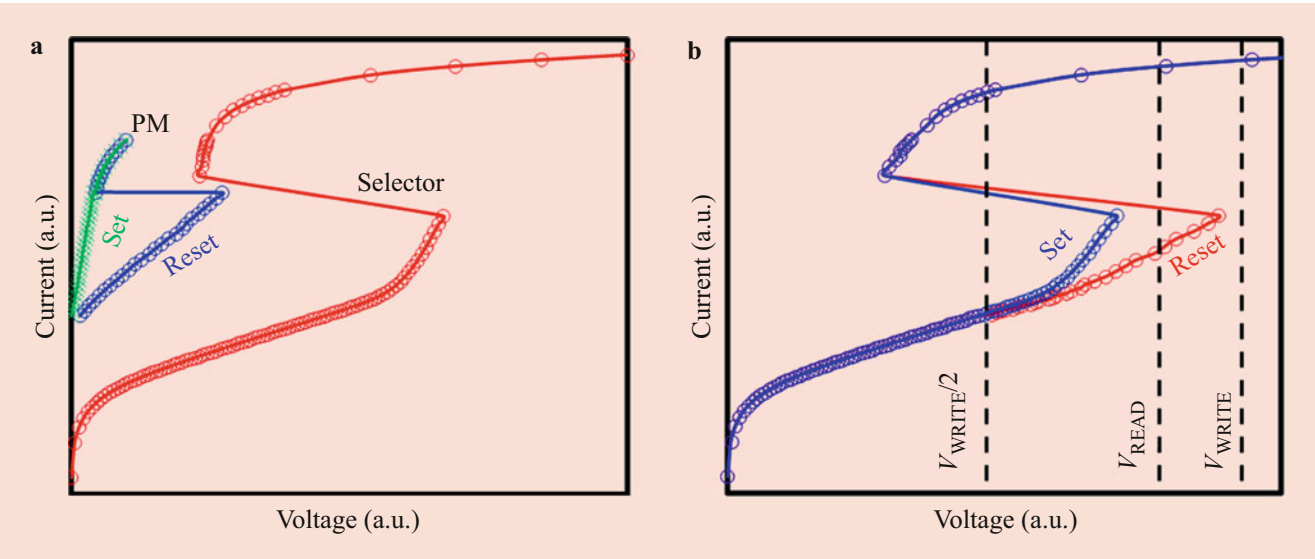

Fig. 30.25 (**a**) Current vs. voltage characteristics of stand-alone and (**b**) of the series of an OTS selector and a PCM cell; the vertical lines show the operating voltages for the READ and the PROGRAM operations. (Reprinted, with permission, from [88] © (2020) IEEE)

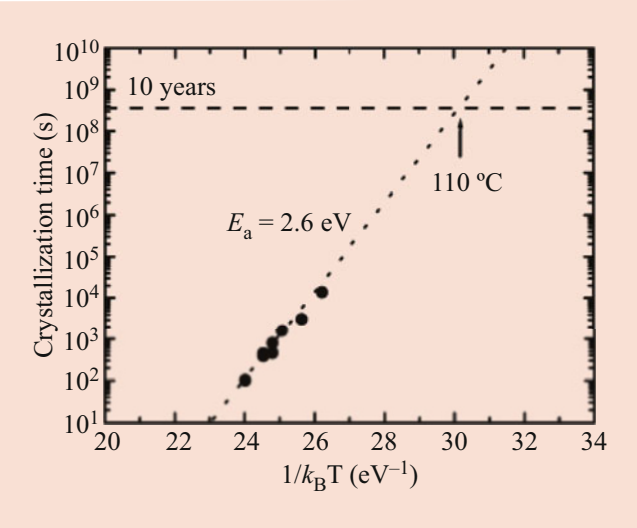

Fig. 30.26 Arrhenius plot for data retention of a GST-225 cell and extrapolation to 110 °C. (Reprinted, with permission, from [92] © (2003) IEEE)

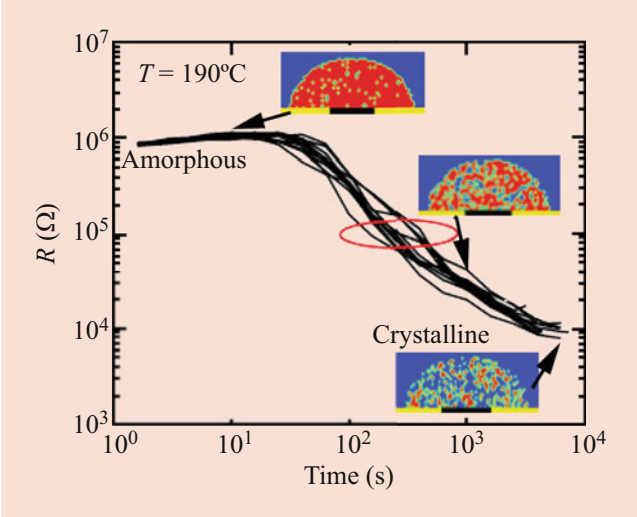

Fig. 30.27 Repeated measurements of resistance of the same PCM cell. The cartoons show the creation of the percolative paths that lead to the loss of the stored information. (Reprinted, with permission, from [93] © (2005) IEEE)

level after 10 years at 85 °C, independently of the previous stress history [5].

Data retention is strictly connected to the write speed, since both of them involve the crystallization process and its activation energy. To achieve a low write latency, the alloy must be able to crystallize in hundreds of nanoseconds when heated above the crystallization temperature; on the opposite side, crystallization must not occur in years at the operation temperature. In general, a high activation energy is a key property to ensure a good data retention over time, as long as it allows a fast SET operation within technologically-compliant temperatures.

To estimate the data retention capability, measurements are typically performed at multiple high temperatures (>150 °C), and data are fairly well extrapolated at lower temperatures assuming a reasonable Arrhenius activation model (Fig. 30.26). Pirovano et al. [91] measured in GST-225 samples a halving of the cell resistance in 10^2–10^4 s for temperatures ranging between 150 °C and 200 °C, with an activation energy about 2.6 eV. This leads to a data retention longer than 10 years for temperatures below 110 °C.

Repeated measurements on the same cell result in a large distribution of retention times according to a Weibull distribution [93], and the same occurs also across an array of cells. These evidences demonstrate the existence of a dominating stochastic component to crystallization. Redaelli et al. [93–95] interpreted the loss of data retention by means of a percolation model, where crystalline grains are stochastically nucleated in the amorphous dome and grow, until a percolation path finally crosses the whole amorphous dome, thus dramatically reducing the overall device resistance (Fig. 30.27).

Gleixner et al. [96] also observed an early failure of a tiny fraction of bits, irrespectively of the applied stress condition; this behavior was attributed to an insufficient RESET operation by which some of the nucleation sites require a limited growth to induce the resistance drop.

Cycling Endurance

Cycling endurance has long been recognized as one of the strengths of PCM devices, as from early studies on single cells, 10^{12} cycles have been demonstrated without a significant degradation of the resistance contrast [97]. Pirovano et al. [91] compared the endurance of a single optimized cell to the statistical behavior at the array level on a large dataset, finding that even at $\pm 4\sigma$ a sufficient separation between SET and RESET is still present after 10^6 cycles (Fig. 30.28). Cycling issues are common to both PCM cells and OTS selectors.

Two different failure modes have been observed: the *stuck-set* and the *stuck-reset*. In the former case, the RESET pulse is progressively less effective in amorphizing the chalcogenide layer until it fails to induce the resistance change, and the memory is left in the SET state; in the latter case, instead, the resistance remains very high, irrespectively of the SET pulse due to permanent local damages at the chalcogenide-electrode interface, like void formation and delamination.

In order to understand the degradation induced by cycling, it must be recalled that the PCM operation exposes the chalcogenide alloy at relatively high temperatures under the influence of high current densities. Both these two conditions favor atomic mobility and electromigration. Experiments

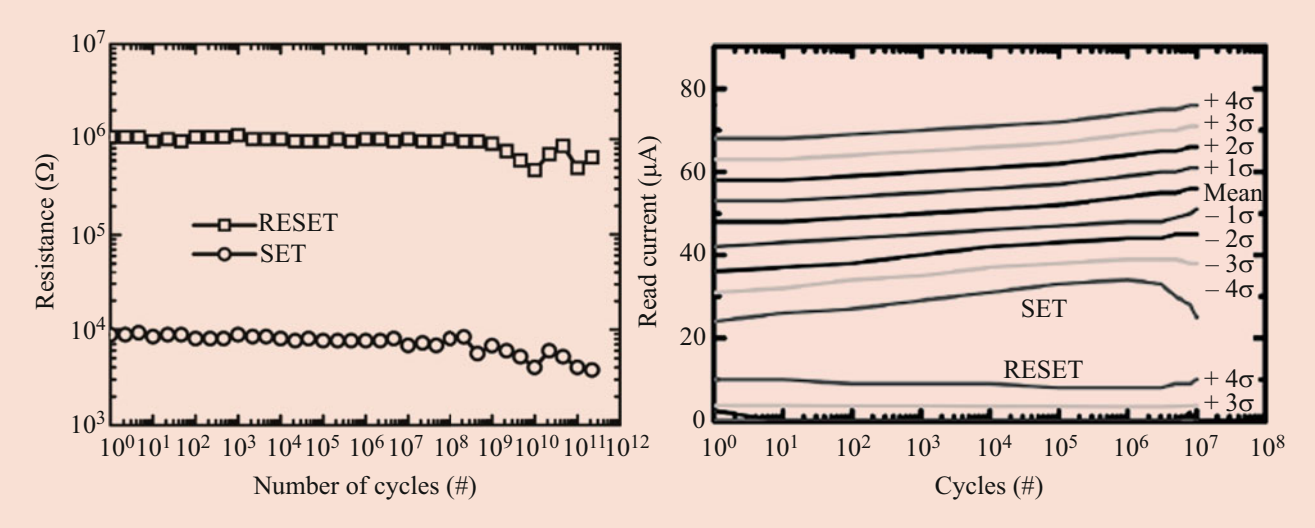

Fig. 30.28 Cycling endurance for the SET and RESET states and associated statistical distribution of the READ current at the array level. (Reprinted, with permission, from [91] © (2004) IEEE)

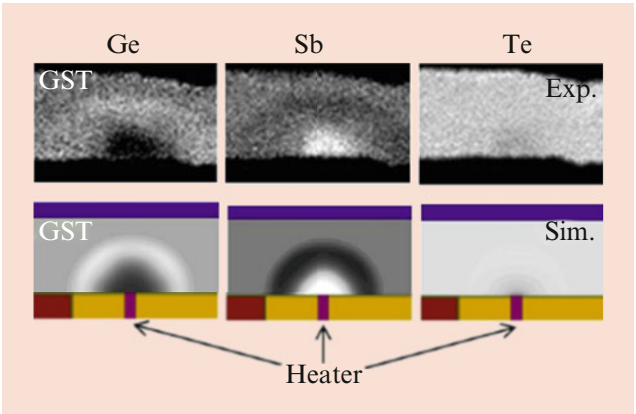

Fig. 30.29 Experimental and simulated concentrations of Ge, Sb and Te after a trapezoidal pulse with a falling edge about 1 μs on the central cut plane for a 45-nm wall cell. (Reprinted, with permission, from [99] © (2013) IEEE)

performed on test line cells showed that, once the molten state is reached, Te takes the form of an anion, and Sb and Ge that of a cation, moving in opposite directions [98]. Energy dispersive X-ray spectroscopy (EDX) analyses and electromigration simulations in a 45-nm wall cell evidenced Sb-richer and Ge-depleted volume in the cell core and a nearly invariant Te concentration (Fig. 30.29) [99]. This form of compositional segregation limits the ability of amorphizing the programmed region, and the cell is finally left stuck-set. On the other side, material depletion induced by temperature-accelerated, current-driven elemental migration results in void formation or delamination of the chalcogenide-electrode interface, and the cell becomes stuck-reset. Endurance measurements have found that the endurance increases when the time spent for melting is shortened [100].

To expand the life cycle of a PCM device, several protocols have been proposed to heal, either thermally or electrically, the damage produced by write cycling before reaching an irreversible condition. These protocols detect the accumulation of the damage by, e.g., monitoring a shift to higher values of the programming characteristic; after a given threshold value is crossed, a recovery operation is activated in order to bring the device back to its pristine state [101].

Read Disturb

The read disturb consists in an undesired recrystallization accelerated by the current flowing in the cell during READ pulses. It does not represent a severe issue for the PCM technology, as it can be controlled by modulating the READ current. As a matter of fact, READ operations, in general, are not able to increase significantly and uniformly the overall temperature of the cell and induce the phase change. However, Pirovano et al. [91] hypothesized that extremely confined local heating may occur, and in those portions of the amorphous dome the crystallization rates are larger than expected. Thus, there is a small, but non-negligible crystallization probability, whose magnitude depends on the time spent for reading. Since the READ pulse is fast, the event of crystallization during reading is unlikely, but sometimes it may happen. It is clear that a single event in a very confined volume would not appreciably alter the overall resistance of the amorphous dome, and it does not constitute any concern. However, multiple READs on the same cell without an intermediate programming pulse increase the possibility of local recrystallizations, as the cumulative time spent under biased conditions is much longer, and eventually the cell may fail (Fig. 30.30). The operating temperature may further accelerate the process.

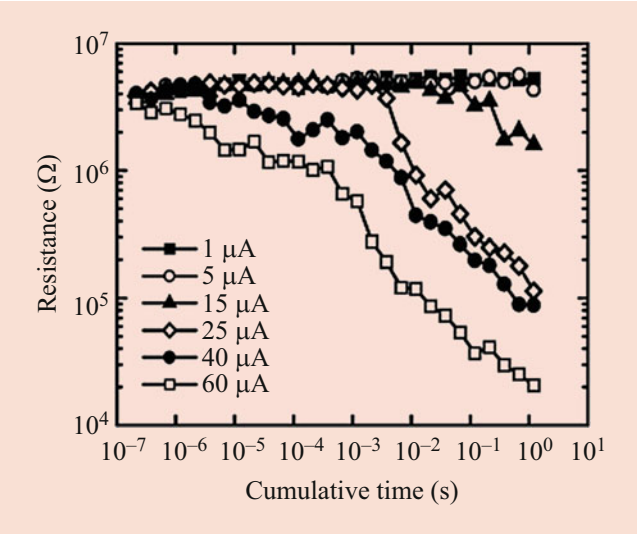

Fig. 30.30 Resistance decrease as a function of the cumulative time spent in the HRS after the last RESET operation. (Reprinted, with permission, from [91] © (2004) IEEE)

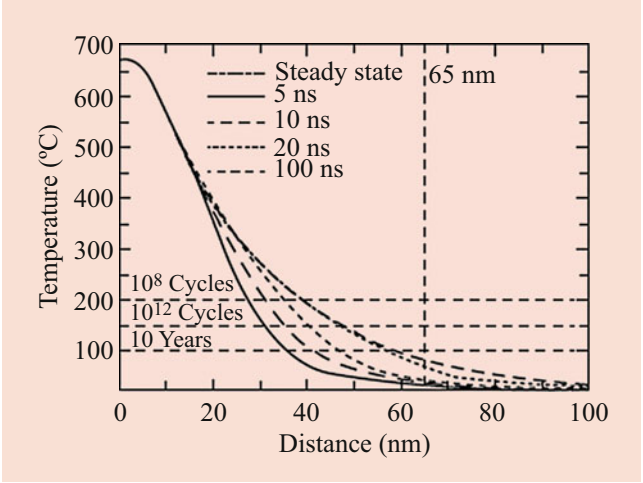

Fig. 30.31 Temperature profile during RESET as a function of distance and time for a μ-trench cell at the 65-nm node. The horizontal lines are the target conditions for the victim cell. (Reprinted, with permission, from [92] © (2003) IEEE)

The impact of the current on the read disturb can be assessed by suitable models combining carrier transport and stochastic crystallization. Given a PCM lifetime of about 10 years, and a reading pulse of about 100 ns, if a write-once single cell were continuously read over its lifetime, about 10^{15} cycles are counted. If reading were instead performed serially throughout all cells of an array, that number is greatly reduced to 10^4 cycles for Gbit arrays. In a typical write-once scenario (e.g., in automotive applications), where only few cells of the array are stressed by repeated READs, an intermediate result is obtained, and a lower limit of about 10^{10} cycles before failure is targeted at the memory design stage. Starting from this constraint, it is possible to estimate as about 1 μA the maximum reading current that can safely be applied during READ operations to prevent read disturbs.

Thermal Disturb

As reported in Sect. 30.3.2, during a RESET pulse, a very high peak temperature is reached and a side effect is the heating of the surrounding cells or thermal cross-talk. If this Joule heating is sufficient to give origin to an unwanted SET operation in one of the neighboring cells, a thermal disturb (also known as proximity disturb or programming disturb) occurs. The programmed cell is often referred to as the aggressor, and the disturbed cells are identified as victims. As for the case of the read disturb, the probability of inducing a recrystallization in a victim cell depends on the programming pattern of the aggressor and on the cumulative time spent under thermal stress. Under the likely condition that one aggressor cell is normally programmed a few percent of its endurance cycle before the victim is refreshed, it is possible to target that one victim cell should survive about 10^6 cumulative write cycles of its aggressors.

The impact of the thermal disturb is usually assessed by means of thermal simulations [92], combined with data-retention experiments. As shown in Fig. 30.31, thermal cross-talk in μ-trench cells undergoes a quick decline with distance from the aggressor cell and is low enough not to constitute a significant concern for recrystallization at the 65-nm node. Furthermore, Russo et al. [102] found that isotropic scaling (i.e., preserving the aspect ratio of the PCM cell) has no impact on the victim cell, but the temperature profile would be significantly different if only the lateral dimension is scaled down. Nevertheless, an aggressive scaling is not fully compatible with contact-minimized geometries, where a unique chalcogenide layer is deposited on top of multiple heaters: since the amorphous dome must always be larger than the heater, the inter-cell spacing cannot be reduced proportionally, increasing the risk of thermal cross-talk. On the contrary, volume-minimized cells benefit from scaling and mostly from the presence of the confining oxides separating neighboring cells. The TBRs at the interfaces, in fact, have the effect of cutting the thermal flow and do not reduce with scaling, minimizing the risk of thermal disturb.

Thermal cross-talk is probably a minor concern in a single-level PCM but can have a more pronounced effect in MLCs. The conduction in the amorphous phase is largely attributed to the presence of defective states within the mobility gap, whose annihilation with time is a thermally activated process. A temperature profile that is not a concern for recrystallization can however accelerate the annihilation of these defective states [103], enlarging the mobility gap due to structural relaxation, thus enhancing the resistance

drift, reducing the reliability of intermediate-resistance level and, eventually, leading to data loss.

30.5.2 Performance Improvements and Perspectives

The high potential of the PCM technology has been recognized for many years but is still jeopardized by the correlations existing between material properties, speed, performances, and reliability issues. By way of example, a material offering a high crystallization temperature leads to a better thermal stability and longer data retention but also to slower and more energy-demanding devices [82]. Depending on the application, engineers focus on one aspect or another: in SCM, where a high number of writing cycles is expected, a large cycling endurance is preferable, rather than thermal stability and longer data retention, which are instead key requirements for embedded PCM to maintain stored data after soldering. Since chalcogenides can be tailored to match specific technological needs, acting on materials and compositions is the primary source for PCM optimization.

Stoichiometric alloys like GST-225 suffer from important technological limitations due to the high RESET currents and to a low crystallization temperature that brings in a limited data retention at moderately high temperature. Many efforts have been made to improve the performances of these alloys by N or C doping, by Ge enrichment, and by considering new compositions along different tie lines [104]. Doping with light elements like C or N extends the thermal stability range and allows one to meet the specifications required by automotive applications (10 years retention at 150 °C), at the price of slowing down the switching speed. However, the achieved improvement is still insufficient for the soldering step, whose target is set to 2 min at 260 °C. Ge-rich alloys further extend the thermal stability of programmed states, and Sb ensures a very fast switching speed, but a limited endurance is reported for non-stoichiometric compositions due to a larger phase segregation that can be stabilized by N doping [105]. The performance achieved by the standard GST-225 alloy, the so-called golden composition (GST-212 with increased Ge concentration along a second tie-line between Ge and Sb_2Te_3) [104], and variants of the golden compositions obtained by N incorporation and Ge enrichment [106] are summarized in Table 30.4.

The reduction of the RESET current is often pursued by the optimization of the PCM cell design, aiming at a better thermal efficiency and a more efficient Joule heating. It has been estimated that in non-optimized cells up to 99% of the energy is inefficiently spent in heating oxides and metal lines, which can also increase the thermal cross-talk between neighboring cells. Two approaches to decrease the RESET current by maximizing the thermal efficiency have been proposed. On the one side, carbon nanotubes and graphene sheets have been tested as contacts [80, 107] or as thermal confining materials [108] for the minimization of the thermal budget owing to their strong non-isotropic thermal conductivity. On the other side, multilayer dielectric stacks, with a lower thermal conductivity (also alternated to air gaps), can replace the confining dielectric [109].

A completely different approach to PCM technology is provided by interfacial PCM (iPCM), which are a superlattice phase-change material stack formed by two alternating crystalline layers of different composition [110, 111]. A typical example is obtained for the $[(GeTe)_x(Sb_2Te_3)_y]_n$ alloys by aligning the ⟨111⟩ direction of a cubic GeTe layer on top of the c-axis of a hexagonal Ge_2Sb_3 layer. According to Tominaga et al. [112], iPCM switch between the HRS and LRS without melting, but with a short-range movement of some atoms, which flip between two configurations corresponding to the SET and the RESET states. The resistance contrast of an iPCM is comparable to that of a conventional PCM up to 10^6 cycles, but the programming currents are roughly halved, and about a 40% reduction of the average power consumption is achievable under standard usage conditions.

One more development direction deals with increasing the storage density, which is pursued in NVM in general by creating a 3D stacking as in cross-point architectures, or by exploiting the large resistance contrast with the implementation of the multi-level storage. As we have warned earlier in this chapter, resistance drift is the strongest challenge for MLC. In order to cope with it, besides taking into account the broadening of each resistance window with time, new sensing schemes making use of ramped READ pulses and evaluating the time required to reach some current reference values have been proposed [113]. An alternative strategy

Table 30.4 Material properties (crystallization temperature, RESET current, crystallization time needed to complete 90% of the transformation, and SET speed) for different compositions

Material	T_x (°C)	I_{reset} (μA)	Recryst. time (ns)	SET speed (ns)
GST-225	150	>400	55	<80
Golden composition (G-c)	253	≥150	200	80
Ge-rich G-c	295	100–150	560	80
N-doped Ge-rich G-c	316	100–150	1750	80
Enhanced N-doped Ge-rich G-c	413	50–100	3115	160–240

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considers tailoring the chalcogenide layer. It has in fact been observed that Ge enrichment increases drift, but this effect is largely counterbalanced by the addition of dopants like N that contribute to form stable Ge-N bonds, as for the materials in the last two lines of Table 30.4. By tailoring the chalcogenide composition, a demonstrator with a material featuring a wider memory window and manageable resistance drift has been proposed also for MLC SCM applications [114].

In conclusion, as a consequence of great technological hopes, a lot of work on chalcogenide materials, PCM, and OTS devices was made in the last couple of decades. Following the Gartner hype cycle [115], the peak of inflated expectations was reached in the early 2000s, but, after that, disillusionment prevailed, as many difficulties about integration, performances, retention, and reliability quickly arose. Nevertheless, the interest of the semiconductor industry did not decline, and a deeper knowledge on PCM and OTS devices was recently achieved, renewing the interest back again. The present status of the technology, as well as promising projects sponsored jointly by academia, research centers, and the most important semiconductor companies, bodes well for reaching the plateau of productivity in the near future.

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Spin-Based Devices for Digital Applications

31

Viktor Sverdlov and Siegfried Selberherr

Contents

31.1 Introduction 1124
31.1.1 MOSFETs: Recent Developments 1124
31.1.2 Electron Spin as a Complement to Charge 1125

31.2 Spin-Based Switches for Digital Applications 1126
31.2.1 Electric Spin Injection into Semiconductors 1127
31.2.2 Single-Spin Transistor 1131
31.2.3 Silicon SpinMOSFET and SpinFET 1136
31.2.4 Spin Relaxation Suppression in Silicon Films 1140
31.2.5 Perspectives of a Spin Silicon Switch 1143

31.3 Nonvolatile Magnetoresistive Memories 1145
31.3.1 Spin-Transfer Torque MRAM 1146
31.3.2 Spin-Orbit Torque MRAM 1150
31.3.3 Advanced MRAM Developments 1155
31.3.4 Racetrack Memory 1156

31.4 Spintronic Logic 1157
31.4.1 Magnetic Domain Wall Logic 1157
31.4.2 Logic-in-Memory 1157
31.4.3 Stateful Logic 1158
31.4.4 Buffered Magnetic Logic Environment 1159
31.4.5 All-Spin Logic 1159
31.4.6 Benchmarking and Magnetoelectric Spin-Orbit Logic 1160

References 1161

Abstract

Scaling of semiconductor devices is the main driving force behind an outstanding performance increase of modern integrated circuits. However, it is apparent that transistor scaling shows signs of saturation, and an introduction of new solutions for energy-efficient computation becomes paramount.

The electron spin offers additional functionality to digital switches based on field-effect transistors. SpinFETs and SpinMOSFETs are promising devices, with nonvolatility introduced through the relative magnetization orientation between the ferromagnetic source and drain. Although several fundamental problems including spin injection from metal ferromagnets to a semiconductor, spin propagation and relaxation, as well as spin manipulation by the gate voltage were successfully demonstrated, increasing the magnetoresistance ratio as well as achieving efficient spin control represent the challenges to be resolved.

Magnetic tunnel junctions are perfectly suited as key elements of nonvolatile CMOS-compatible magnetoresistive memory. Purely electrically addressable spin-transfer torque and spin-orbit torque magnetoresistive memories are superior compared to flash memories and will compete with DRAM and SRAM. MRAM possesses a simple structure, long retention time, high endurance, and fast operation speed. In addition, a combination of nonvolatile elements with CMOS devices allows to bring close or to even shift data processing capabilities into the nonvolatile segment. This paves the way for a new low-power and high-performance computing paradigm based on logic-in-memory and in-memory computing architectures, where the same nonvolatile elements are used to store and to process the information.

Keywords

Digital spintronics · SpinFET · SpinMOSFET · Spin-transfer torque · STT · Spin-orbit torque · SOT · MRAM · In-memory computing

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31.1 Introduction

31.1.1 MOSFETs: Recent Developments

Continuous miniaturization of metal-oxide-semiconductor field-effect transistors (MOSFETs) is one of the main drivers behind the recent tremendous increase in speed, performance, density, and complexity of modern integrated digital circuits. Although the name MOSFET was not modified since its invention until now, the transistor structure has become dramatically more complex. Numerous outstanding technological challenges have been resolved on the exciting journey of continuous transistor downscaling. The main challenge with transistor dimensions' reductions is to preserve a good electrostatic channel control by the gate to guarantee steep switching between the open (on) and closed (off) transistor states with several orders of magnitude current difference.

Modern MOSFETs feature channel strain as a mobility booster, which allows improving the on-current while maintaining other characteristics including the off-current unchanged. Strain first introduced in 2003 for the 90 nm technology node [1] is currently routinely delivered to the channel by appropriately engineering the capping layers and/or replacing silicon in the source and drain extensions with a material with larger (smaller) lattice constant, which stresses the channel compressively (tensely). As donor n- or acceptor p-doped silicon channels require tensile or compressive strain to boost the carrier mobility, in modern complimentary metal-oxide-semiconductor (CMOS), technology strain is independently delivered to each transistor. To boost the mobility in n-silicon channels, tensile capping materials are used, while in p-channels compressive capping layers are complemented by epitaxially regrown SiGe source and drain [1].

To continue shrinking the CMOS technology to the 45 nm technology node, the traditional SiO_2 gate oxide had to be replaced with a high permittivity (high-k) dielectric [2]. Since this replacement has required a major modification in the gate stack process technology, it also demanded the replacement of heavily doped silicon by a metal to negate the depletion length in the gate. These replacements have allowed to enhance the electrostatic channel control by reducing the effective dielectric thickness while maintaining the physical oxide thickness sufficiently large to inhibit parasitic tunneling leakage currents. However, to proceed to the 22 nm technology node and beyond, a new architecture of three-dimensional tri-gate transistors has been introduced [3]. By making the fins higher and thinner, this technology combined with strain techniques and high-k dielectrics/metal gates allows continuing the scaling down to 14 nm [4] and 10 nm [5] feature size and offers great performance and power advantages over planar structures. Combining the technology with pitch splitting, self-aligned patterning, and EUV lithography, the device miniaturization is continuing its pace down to 7 nm feature size.

To proceed with scaling to the 5 nm technology node, an introduction of a new channel material with improved characteristics, such as strained SiGe [6] for p-MOSFETs or III-V materials [7], is foreseen. To further improve the channel control, gate-all-around devices are considered. In order to sustain the high on-current through the transistor, the channel in such devices contains several nanosheets surrounded by the gate. The introduction of new materials with higher mobility combined with the gate-all-around nanosheet architecture for improved electrostatic control will potentially allow to proceed with scaling at the 5 nm technology node and beyond [8].

Although single devices with gate length as short as a few nanometers, which is close to what is believed to be an ultimate limit, were demonstrated [9] long ago, fabrication, control, integration, and reliability issues will slowly lead to unbearable hurdles. Growing critical technological challenges and soaring costs will gradually bring the CMOS scaling to a saturation. Another important limitation for transistor scaling is related to the heat generation. Even though the transistor size is scaled down, the load capacitance per unit area of a circuit stops decreasing. This suggests that the on-current must increase to boost the operation speed or stay the same to guarantee the same high clock frequency.

However, in ultra-scaled MOSFETs the current is close to ballistic and is determined by the number of transversal propagating modes in the channel, so that the channel conductance ceases to depend on the channel length. It then follows that with the transistor scaling the supply voltage must remain the same to maintain the same current through a transistor regardless of its channel length. This results in an approximately constant power dissipation of a single MOSFET. The generated heat increases rapidly with increased transistor size, which puts clearly foreseeable limitations to the continuation of the increase in the performance of integrated circuits, and research for finding alternative technologies and computational principles becomes urgently important.

Carriers in graphene are characterized by a mobility which can exceed silicon mobility by an order of magnitude [10], making this material very attractive for future electronic device applications. However, Dirac fermions do not possess a gap and can be transmitted through a classically forbidden region without any reflection. Therefore, applying a gate bias, which would normally switch off a traditional MOSFET, does not stop the current flow through a graphene sheet. A high on-off current ratio can be obtained, if the graphene sheet is used as a base of a bipolar-like transistor [11], albeit advantages steaming from the high graphene carrier mobility are not used. Nanoribbons may open a gap in

the Dirac spectrum, thus making reflection from a forbidden region possible [12]. However, in order to avoid strong edge roughness scattering [13], the edges of nanoribbons must be atomistically perfect, which makes the practical use of nanoribbons at the current technology level development hypothetical.

Recently, a single layer of molybdenum disulfide MoS_2, a purely two-dimensional material, has attracted interest [14]. In contrast to graphene, this is a direct gap semiconductor and is thus suitable for making a MOSFET. However, both electron and hole mobilities are limited by the carriers' interaction with homopolar phonons [15, 16]. It remains to be seen, if the electron mobility and current in this material can be sufficiently boosted [17] to make it competitive with CMOS.

Inspired by the continuing efforts in graphene and transition metal dichalcogenide monolayer devices, a search for novel two-dimensional monolayer semiconductors has intensified. Potentially, atomically thin-layered semiconductors free from dangling bonds possess excellent electronic properties and are suitable for the ultimate transistor scaling. Although a large number of two-dimensional semiconductors have been discovered and explored [18], they still suffer from reproducibility and scalability due to the lack of large-scale synthetic processes. At the moment, the best performing transistors reported are merely comparable to standard silicon devices as the performance of the current two-dimensional semiconductor transistors is compromised by defects at their interfaces or contacts [18].

31.1.2 Electron Spin as a Complement to Charge

The principle of MOSFET operation is fundamentally based on the charge degree of freedom of an electron. The electron charge interacts with the gate-induced electrostatic field. The gate potential can open or close the transistor by creating a potential barrier. However, it is well known that the electron possesses another intrinsic degree of freedom, namely, the electron spin. As the downscaling of charge-based CMOS devices is approaching its saturation, the electron spin attracts at present much attention as a possible candidate for complementing or even replacing the charge degree of freedom in future microelectronic devices [19–28]. Indeed, the electron spin state is characterized by one of the two possible spin projections on a given axis, a property which could be potentially used in digital electronics for information processing. In order to switch between the two aligned spin states, an amazingly small amount of energy is required, which is very attractive for low-power applications.

The electron spin may be pointing not only up or down along a certain axis. As a quantum mechanical property, spin can point at any direction on a unit Bloch sphere. The electron spin offers the whole Bloch sphere of states to process and store information by initializing, manipulating, and detecting the spin orientation. As the electron spin is a purely quantum mechanical property, the set of states on a Bloch sphere is termed a quantum bit, or a qubit, as opposed to a bit of classical, binary information. A computer using qubits for information processing is named a quantum computer. Due to their intrinsically quantum mechanical nature, qubits could form an entangled state. This state cannot be represented as a direct product of independent qubits, wherein a single qubit state is entangled with other qubits and thus cannot be described independently. Qubits' entanglement generates intrinsically quantum correlations between the qubits, which go beyond classical correlations and even cannot be described at a classical level.

Single-electron spin systems in semiconductors can be broadly classified into two large categories: atomic impurities [29] and spins in quantum dots [30]. A quantum computer consisting of interacting qubits potentially offers an advantage over traditional digital computers in resolving certain computationally involved tasks. A quantum computation scheme utilizing spins of electrons in quantum dots [31] was suggested almost simultaneously with a quantum-mechanical computer employing the nuclear spins of donors in silicon [32]. A review of group IV semiconductors' proposals for quantum computation is given in [33]. Carriers in quantum dots are strongly confined in all three spatial directions. If the confinement potential possesses a symmetry, the degenerate energy levels in quantum dots, like in real atoms, form shells. For this reason, the electron system in a quantum dot is often called an artificial atom. Properties of artificial atoms can be tailored by adjusting confinement so that the number of particles in a dot and the total spin can be controlled [34]. Single-atom qubits [29] offer a spin lifetime of several seconds [35] to 30s [36]. The single-atom technology was recently shown to have a potential toward large-scale quantum computers as it allows growing three-dimensional silicon quantum chips, in which precise interlayer alignment and highly accurate measurement of spin states are achieved [37]. A successful implementation of a quantum computer based on spins requires the possibility of efficient spin initiation, coherent manipulation, and reliable readout. An unprecedented advantage in these fields has been achieved [38, 39]. With two-qubit operation [40] a processor performing quantum algorithms [41] has already been successfully demonstrated; a pressing challenge is now to proceed to a larger computational network.

Silicon predominantly consists of ^{28}Si nuclei with zero magnetic spin, with a few percent admixture of magnetic ^{29}Si nuclei. In isotopically purified silicon cleaned from the magnetic isotope ^{29}Si, the dephasing of donors' electron spins is significantly reduced [42], resulting in a coherence time

of about 10 s at $T = 1.8$ K. Thanks to its unique properties for spin applications, silicon, the main material of modern microelectronics, is promising for spin-driven devices. Compatibility of spin-based devices with charge-based silicon CMOS technology would greatly facilitate their integration on the same chip. However, at least at the current level of the technological development, this integration requires the capability of room temperature operation, which at the moment excludes the use of quantum-mechanical properties of localized electron spins in silicon due to fast dephasing, causing the loss of quantum information at (sub)nanosecond scale before a quantum gate operation is performed.

More promising for room temperature quantum bit storage are the nuclear spins of the ionized shallow donors in purified ^{28}Si, because they display an unprecedentedly long spin coherence time close to 40 min [43]. This considerably exceeds the coherence time of two seconds demonstrated at room temperature in a quantum bit consisting of a single ^{13}C nuclei/nitrogen vacancy in an isotopically purified diamond crystal [44]. Spins of impurities in solids combined with nearby nuclear spins in the lattice form a quantum register [45]. Coherent coupling of the registers with photons results in high-fidelity state initialization, manipulation, and readout, yields long retention quantum memory, and allows long-distance transmission of quantum information [45]. These important ingredients institute impurity spins as unique building blocks for realizing quantum networks at room temperature. However, the technology also requires a controllable creation of high-density near-surface defects with given charge state and long-living spin state, which represents a significant challenge for modern semiconductor technology.

There exists yet another opportunity to employ the electron spin in digital electronics. The relaxation time for non-equilibrium spins of conducting electrons toward its equilibrium value is in the range of nanoseconds in undoped bulk silicon [46, 47]. As the corresponding spin diffusion length is in the micrometer range, the spin of conducting electrons can be used to encode, transfer, and process information. In this case, the electron spin degree of freedom is employed in its binary mode, as the information is stored as a positive or negative spin projection on a given axis usually defined by a ferromagnetic electrode's magnetization direction. As the spin does not interact with the electric field and diffuses from the spin accumulation region regardless of the electric field applied, transferring the spin information does not in general require any charge current to flow, although spins belong to the electrons which are of course the charged particles. The ability to decouple spin from charge and to generate pure spin currents makes the spin degree of freedom potentially promising for low-power digital applications.

Novel microelectronic devices have to be smaller and faster than the traditional ones and be more efficient, in order to reduce the power consumption of future integrated electronic circuits. Because the scaling of conventional MOSFETs is rapidly approaching its fundamental limits, new engineering solutions have to be introduced. Utilizing spin properties of electrons opens a great opportunity to design devices with superior characteristics which cannot be achieved with the present transistor technology.

An attractive path to mitigate the unfavorable trend of increasing power at standby is to introduce nonvolatility in the circuits. The development of an electrically addressable nonvolatile element, which combines fast operation, simple structure, and high endurance, is essential to mitigate the increase of the standby power and the power needed for data refreshment. Nonvolatile elements also enable instant-on architectures without the need of data initialization when going from the standby to an operation regime.

The spin field-effect transistor (SpinFET) [19] is a switch which employs the spin properties of electrons. The SpinFET is composed of a semiconductor channel region sandwiched between the two ferromagnetic contacts, source and drain. The source contact injects spin-polarized electrons in the semiconductor region. The gate voltage-dependent spin-orbit interaction in the channel is used to modulate the current through the SpinFET. It causes the electron spin to precess during the electron propagation through the channel. Only the electrons with their spin aligned to the drain contact's magnetization can leave the channel through the drain contact, thus contributing to the current. The spin-orbit interaction is controlled electrically by applying an external gate voltage.

In this chapter, we briefly review first the current status of spin-based digital switches including the recently demonstrated SpinFET and the SpinMOSFET, and we outline the exciting challenges still preventing the spin-based switches from entering mass production. Thereafter we document the present status in spin-based purely electrically addressable nonvolatile magnetoresistive memories, which are proven to be competitive with flash memory and possess a considerable potential to enter the dynamic and static RAM markets. We conclude the review with an outlook focusing on nonvolatile logic architectures.

31.2 Spin-Based Switches for Digital Applications

The idea of using spin to complement or even to replace the charge degree of freedom in digital computing was around for more than three decades. However, even a proof-of-concept demonstration of basic elements necessary for digital spin-related applications, such as injection of spin-polarized currents in a semiconductor, spin transport, spin manipulation by electric field, and spin detection, was extremely challenging. Conceptual and technological difficulties to inject spin-

polarized electrons in silicon were preventing researchers from studying spin propagation in silicon. One of the reasons is that, contrary to III-V semiconductors, silicon is an indirect gap semiconductor. Therefore, techniques based on optical excitations with the absorption/emission of circularly polarized photons used to introduce spins in, for example, GaAs, cannot be applied [46, 47].

Although it seems that injecting spin-polarized carriers from a ferromagnetic contact into silicon bypassing the current is straightforward, non-equilibrium spin accumulation was not seen in earlier attempts. The reason was understood just relatively recently [48]. It appears that all known ferromagnets at room temperature are metals. Due to a fundamental spin conductivity mismatch [48] between the ferromagnetic metal contact and the semiconductor, no spin accumulation is dynamically injected in the semiconductor, when the electric current runs from the ferromagnetic metal into the semiconductor. Even though there is a large difference in the densities of states between the spin-up and spin-down electrons in the metal, the density of states in silicon for either spin projection is still much lower than that for the minority spin in the metal. As silicon is a nonmagnetic semiconductor, the densities of states for spin-up and spin-down electrons are equal. Then, when the current runs through the interface between a ferromagnetic metal electrode and a semiconductor, the supply of both spin-up and spin-down electrons into semiconductor is overwhelmingly high so that both spin-up and spin-down channels are fully and therefore equally populated (Fig. 31.1a). It results in a total zero dynamically injected spin accumulation in silicon.

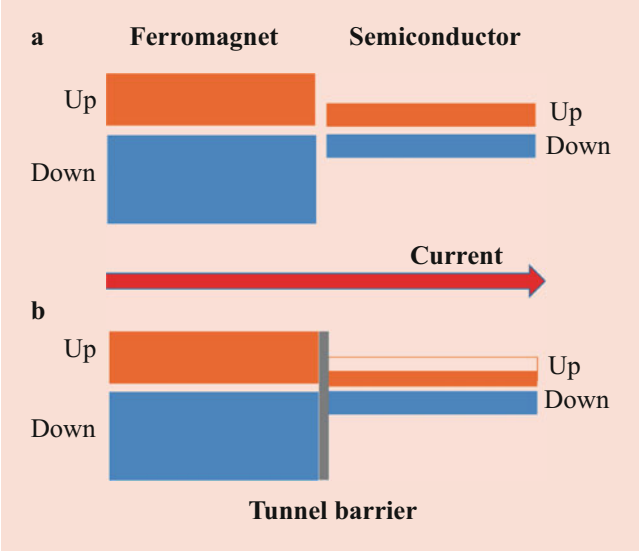

Fig. 31.1 Electric current-induced dynamic spin injection from a ferromagnetic metal into a semiconductor. (**a**) Regardless of a large difference in the density of states between the spin up/down electrons, both spin up/down channels in the semiconductor are equally populated due to their much smaller densities of states. It illustrates the spin impedance mismatch between a ferromagnetic metal and a semiconductor. (**b**) The introduction of the tunneling barrier reduces the electron flow, so that the spin channels in the semiconductor are proportionally populated resulting in a spin accumulation

31.2.1 Electric Spin Injection into Semiconductors

The problem of reliably injecting spins into silicon by electrical means was long without solution. Indeed, to resolve it, one employs either a ferromagnetic semiconductor or a half-metallic ferromagnet to inject spins. Although ferromagnetic semiconductors are known, their Curie temperature is around 100 K [49, 50], well below room temperature. Half-metallic ferromagnets are promising, because they contain only one spin polarization as the density of states for the minority spins at the Fermi level is zero. They are therefore characterized with maximal spin polarization. However, the interface between the half-metallic ferromagnet and a semiconductor is not well understood and not controlled, so typically the high spin current polarization impinging from the half-metal is lost [51] presumably at the interface due to intensive spin-flip events.

A different approach was adapted in [52]. A special technique based on hot-electron injection and a simultaneous attenuation of spins antiparallel to the magnetization of the ferromagnetic film allowed creating an imbalance between the electrons with spin-up and spin-down in silicon, thus injecting spin-polarized current. The spin-coherent transport through the device was studied by applying an external magnetic field which causes a precession of the spins during their propagation in silicon from source to drain. The detection is performed with a similar hot-electron spin filter. Therefore, the drain currents are small due to the carriers' attenuation in the source and drain filters. However, the experimental setup represents a significant breakthrough as it demonstrates the first spin-driven silicon device which can potentially operate at room temperature. The first demonstration of coherent spin transport through an undoped 350-μm-thick silicon wafer [53] has ignited a great interest and gave hope for silicon spintronics to be implemented within the next decade.

As a generalization of the hot-electron injection method [52, 53], an optically assisted method to achieve large spin injection into semiconductors including a monolayer MoS_2 from a ferromagnet with help of a femto-second laser is gaining momentum [54, 55]. A plausible explanation is as follows: a short laser pulse in the ferromagnet excites the large population of strongly out-of-equilibrium electrons with both spins. However, the minority spins are characterized by a much stronger relaxation rate and lose their energy quickly. So, in analogy with the hot carrier spin injection [52, 53] only the majority spins with their energy higher than the

conduction band minimum can diffuse into the semiconductor resulting in a giant, almost 100% spin polarization. It remains to be seen if this approach is competitive as it requires expensive and technologically involved equipment.

A purely electrical method to inject spins in a semiconductor was suggested by E. Rashba already in 2000 [56]. The current which flows into the semiconductor from a ferromagnetic metal is reduced by introducing a tunnel barrier. This allows to occupy the corresponding density of states for the majority and minority spins in a semiconductor proportionally to their ratio in the ferromagnet (Fig. 31.1b). However, this technique requires the tunnel barrier to be not too thick to have a signal nor too thin to avoid the spin impedance mismatch problem. In addition, the quality of the barrier and interfaces should guarantee a very low rate of spin flips in the stack [57]. Therefore, it took almost a decade until first experimental evidences of electrical dynamic spin injection in silicon appeared [58–61], which resulted in a systematic study of spin transport properties in silicon [27]. In particular, many promises were due to the large signal interpreted as a spin accumulation observed in the so-called three-terminal injection scheme [60, 61], where the same ferromagnetic electrode is used to inject and to detect the spin accumulation. However, it appears that the signal is orders of magnitude larger as compared to what a simple estimate would give [57, 60], which certainly rang the bells that a phenomenon different from spin accumulation generated the signal. It is currently established [62] that the spins are reliably injected into silicon from a ferromagnetic electrode through a tunnel barrier, with a value consistent with a theoretical estimate of spin accumulation. However, the main signal relating the additional voltage modulation with the magnetic field in the three-terminal injection scheme is determined by the magnetoresistance due to spin-dependent trap-assisted resonant tunneling [63] or hopping [64]. We briefly describe in what respect the spin-dependent hopping differs from its spin-independent counterpart and highlight an idea of a single-spin switch in the following.

Spin-Dependent Trap-Assisted Hopping from a Ferromagnet to Silicon

Single-electron hopping plays an important role in determining transport properties in undoped semiconductors and dielectrics. The Coulomb interaction plays an important role as well, as it leads to the repulsion of the charges on a trap and to the Coulomb blockade, thus forbidding the double occupancy of a trap. The Coulomb repulsion results in strong charge correlations at transport. Indeed, when electrons tunnel through a trap [65], a second electron from a metallic contact cannot enter the trap, if it is already occupied by an electron. However, when the electron is released from the trap to a contact, the Coulomb repulsion does obviously not prevent another electron entering the trap. Therefore, the electron transport is performed in sequences consisting of an electron hopping from the source electrode to the trap, followed by the electron escaping from the trap to the drain electrode. Because the Coulomb repulsion is a purely classical interaction, electron tunneling through the trap represents an example of classically correlated charge transport.

From the point of view of devices, the Coulomb blockade has led to the discovery of the single-electron transistor [65], which is a three-terminal device consisting of a small metallic island (dot) weakly coupled to the source and drain electrode by means of tunneling through the thick potential barriers. Because of the weak coupling, electrons are allowed to jump on the dot from the source and to escape to the drain one by one. However, due to the Coulomb blockade, the transport through the dot at small source-drain voltages is suppressed, unless the free energy to add an electron to the dot occupied with $(N - 1)$ electrons or to extract an electron from the dot occupied with N electrons is exactly zero [65]. As the potential of the dot and, therefore, the addition/extraction energies can be tuned by the gate electrode capacitively coupled to the dot, a current switch between the on and off states can be built. As the transport through the dot is carried out by a single-electron jumping on/from the dot, the switch is termed single-electron transistor.

In addition to its electron charge, the electron possesses spin. From the physical phenomena related to a single spin, the Pauli, or spin, blockade is known to the single-electron transport, in addition to the Coulomb blockade. The Pauli exclusion principle forbidding two electrons with the same spin projections to occupy the trap quantum state results in yet another correlation affecting the transport through the double-quantum dot system in a magnetic field [66].

The spin blockade is very sensitive to the spin decoherence and relaxation effects and is therefore typically observed at low temperature. However, recently spin correlations resulting in large magnetoresistance and magnetoluminescence effects in organic semiconductors and organic light-emitting diodes [67] were reported at room temperature. The transport is due to the variable-range spin-dependent single-electron hopping through a network of traps. Due to the Pauli blockade, the current is very sensitive to the strength of the external magnetic field which aligns the spins and inhibits the current.

In the case when the source and/or drain electrodes are ferromagnetic, the spin correlations are observed at the transport through a *single* quantum dot. Indeed, an electron impinging a ferromagnetic electrode from a trap has a larger probability to escape, if its spin is parallel to the magnetization $\mathbf{M}$ of the electrode [68]. In this case, the drain electrode plays a role similar to the second quantum dot in the Pauli spin blockade experiments [66], which results in a Pauli blockade-like trap-assisted tunneling transport between the ferromagnetic electrodes. The signal has been observed at temperatures as high as 500 K [61], envisioning that a single-spin switch seems conceivable.

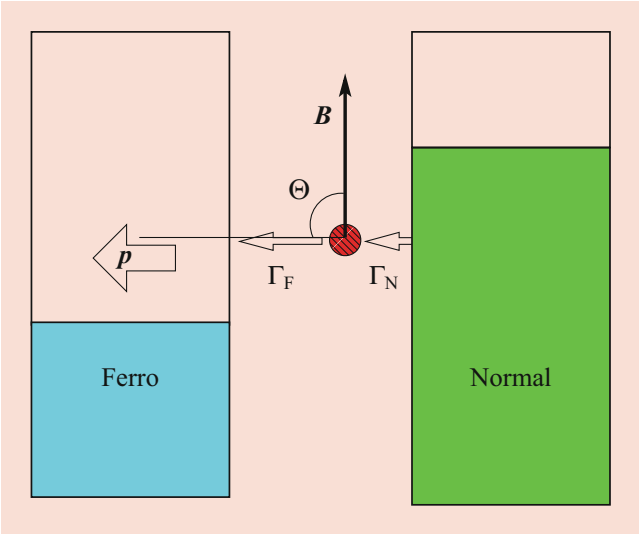

Fig. 31.2 Schematic illustration of trap-assisted tunneling from a semiconductor to a ferromagnet. The magnetic field $\boldsymbol{B}$ forms an angle Θ with the direction of the magnetization in the ferromagnet

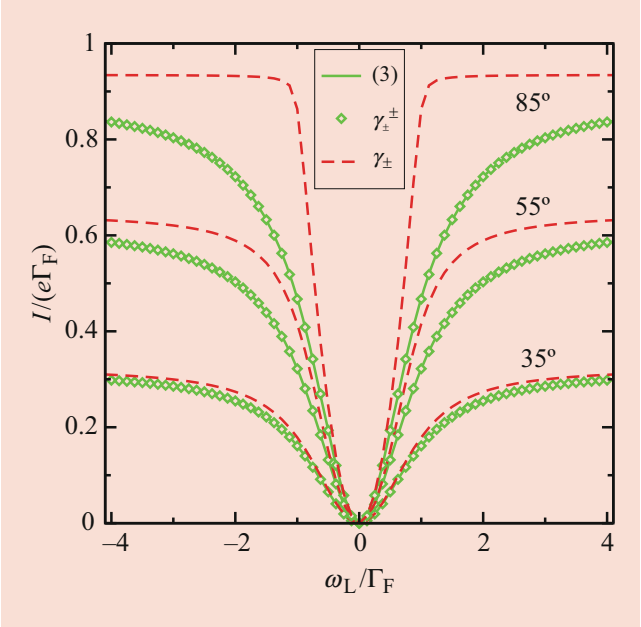

Fig. 31.3 Magnetoresistance computed with the stationary solution of (3) for spin-dependent sequential tunneling (diamonds). The results are compared with the findings in [63] (solid lines) and [69] (dashed lines)

Here we report on a three-terminal single-spin switching device employing for its operation both the spin and the Coulomb blockade. The switch consists of a trap weakly coupled to three ferromagnetic electrodes by tunneling transition rates. In this case, the spin on the trap is a vector quantity determined by the magnetic polarizations of the electrodes, transition rates, as well as the weak non-quantizing magnetic field, which results in unusual correlations in the three-terminal device. In order to describe the switch, we first elaborate on spin-dependent trap-assisted hopping between a normal metallic and a ferromagnetic electrode. We then generalize the description to spin-dependent hopping in a magnetic tunnel junction with both electrodes being ferromagnetic. After that we analyze a multiterminal device governed by spin-dependent hopping by considering an example of a three-terminal switch, where the source, the gate, and the drain are ferromagnetic.

We consider the transport due to spin-dependent trap-assisted tunneling. The trap is located between a normal metallic and a ferromagnetic electrode (Fig. 31.2). The trap can be empty or occupied by a single electron. The non-quantized magnetic field $\boldsymbol{B}$ is applied at an angle Θ with respect to the magnetization direction in the ferromagnetic drain contact.

The tunneling rate Γ_N from the normal metallic contact to the trap does not depend on spin, while the tunneling rate from the trap to the ferromagnet is spin-dependent and is determined by the two rates $\Gamma_\pm$ for the spin projection on the trap aligned and anti-aligned with $\mathbf{M}$. The rates can be expressed as

$$\Gamma_\pm = \Gamma_F (1 \pm p), \tag{31.1}$$

where the spin current polarization at the interface of the ferromagnet $p \leq 1$ is defined as [63]

$$p = \frac{\Gamma_+ - \Gamma_-}{2\Gamma_F}. \tag{31.2}$$

The equations for the site occupation probability n and the spin $\mathbf{s}$ on the trap are determined from the equations [64]

$$\frac{\mathrm{d}}{\mathrm{d}t} n = \Gamma_N (1 - n) - \Gamma_F n - \Gamma_F \mathbf{ps}, \tag{31.3a}$$

$$\frac{\mathrm{d}}{\mathrm{d}t} \mathbf{s} = -\Gamma_F \mathbf{s} - \boldsymbol{p}\Gamma_F n + [\mathbf{s} \times \boldsymbol{\omega}_L], \tag{31.3b}$$

where $\boldsymbol{p} = p\,\frac{\mathbf{M}}{M_s}$, M_s is the saturation magnetization, and $\omega_L = \frac{eB}{mc}$ is the Larmor precession frequency. In the case $p = 0$, one obtains the standard balance equation for the occupation decoupled from the spin. The spin polarization of the ferromagnetic drain electrode couples the spin degree of freedom into the equation for the site occupation, which results in the resistance dependence on the magnetic field [63] shown in Fig. 31.3 by solid lines, for several values of Θ.

The transport process consists of two consecutive hops from the normal metallic source electrode to the trap and an escape from the trap to the ferromagnetic electrode [70].

The first step is characterized by a single-rate Γ_N. However, the escape from the trap is described by a matrix because of the coupling between the spin and the occupation at the trap. The escape probability $P(t)$ from the trap in the case of spin-independent hopping is described as

$$P_2(t) = 1 - n(t), \tag{31.4}$$

where $n(t)$ is the solution of the differential equation [64]

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{pmatrix} n \\ s_x \\ s_y \\ s_z \end{pmatrix} = -\mathbf{A}\begin{pmatrix} n \\ s_x \\ s_y \\ s_z \end{pmatrix} \tag{31.5}$$

The 4×4 relaxation matrix $\mathbf{A}$ is written in the coordinate system with the OZ axis parallel to the magnetic field $\boldsymbol{B}$:

$$\mathbf{A} = \begin{pmatrix} \Gamma_F & p\Gamma_F \sin\Theta & 0 & p\Gamma_F \cos\Theta \\ p\Gamma_F \sin\Theta & \Gamma_F & \omega_L & 0 \\ 0 & -\omega_L & \Gamma_F & 0 \\ p\Gamma_F \cos\Theta & 0 & 0 & \Gamma_F \end{pmatrix} \tag{31.6}$$

Because the trap is populated by hopping from the normal metallic electrode, spin-up and spin-down states are occupied with equal probabilities. Thus, the initial spin at the trap is zero, and the initial condition for (31.6) is

$$\begin{pmatrix} n \\ s_x \\ s_y \\ s_z \end{pmatrix}(t=0) = \begin{pmatrix} 1 \\ 0 \\ 0 \\ 0 \end{pmatrix}. \tag{31.7}$$

The charge transport consists of a series of repeated cycles. An electron jumps from the normal metallic electrode to the trap with the rate Γ_N and then escapes from the trap to the ferromagnetic electrode with the probability $P(t)$ (31.4). Double occupancy of the trap is prohibited by the Coulomb repulsion. One electron charge is transferred at each cycle during the time $\tau_1 + \tau_2$. The average time τ_1 is evaluated in accordance with the escape probability $P_1(t) = 1 - \exp(-t\,\Gamma_N)$. The time τ_2 is computed according to $P_2(t) = 1 - n(t)$. In contrast to spin-independent tunneling, the probability is not determined by a single exponential distribution. As it follows from the solution of (31.5, 31.6 and 31.7), the escape probability (31.4) is defined by the four eigenvalues of the 4×4 relaxation matrix $\mathbf{A}$ (31.6):

$$\gamma_{\pm}{}^{+} = \Gamma_F \pm \left(\frac{1}{2}\left(p^2\Gamma_F{}^2 - \omega_L^2\right) + \sqrt{\frac{\left(p^2\Gamma_F{}^2 - \omega_L^2\right)^2}{4} + \omega_L^2 p^2 \Gamma_F{}^2 \cos^2\Theta} \right)^{1/2} \tag{31.8a}$$

$$\gamma_{\pm}{}^{-} = \Gamma_F \pm \left(\frac{1}{2}\left(p^2\Gamma_F{}^2 - \omega_L^2\right) - \sqrt{\frac{\left(p^2\Gamma_F{}^2 - \omega_L^2\right)^2}{4} + \omega_L^2 p^2 \Gamma_F{}^2 \cos^2\Theta} \right)^{1/2} \tag{31.8b}$$

The solution of (31.5, 31.6 and 31.7) is then written as

$$\begin{pmatrix} n \\ s_x \\ s_y \\ s_z \end{pmatrix}(t) = \sum_{\sigma,\sigma'} C_{\sigma'}^{\sigma}\, \boldsymbol{u}_{\sigma}^{\sigma'} \exp\left(-t\gamma_{\sigma}^{\sigma'}\right), \tag{31.9}$$

where $\boldsymbol{u}_{\sigma}^{\sigma'}$ are the eigenvectors of $\mathbf{A}$ in (31.6). The coefficients $C_{\sigma'}^{\sigma}$ are uniquely determined by the initial condition (31.7).

The first component of (31.9) determines the escape probability $P_2(t) = 1 - n(t)$. The average time τ_2 can be calculated analytically. The stationary current I computed as

$$I = \frac{e}{\tau_1 + \tau_2} \tag{31.10}$$

which is shown in Fig. 31.3 with diamonds. The current from (31.10) coincides with the one obtained in [63] (Fig. 31.3, solid lines) but is significantly lower than the current computed with the expression from [69] shown with dashed lines in Fig. 31.3. In fact, the current values from [69] are too large for all directions of the magnetic field except the one, when $\boldsymbol{B}$ is parallel to $\boldsymbol{p}$. This implies that the escape times used in [69] are shorter. The escape time distribution probability in [69] is determined by the two tunneling rates (31.8a) from each of the Zeeman levels renormalized by coupling to the ferromagnetic contact. This approximation is appropriate only in the case when the magnetic field is aligned with the magnetization. In the general case, the consideration based on the matrix Eqs. (31.5, 31.6 and 31.7) is necessary to reproduce the correct transition probabilities and currents. This explains [64] the controversy between the results in [63, 69].

Spin-Dependent Hopping in Magnetic Tunnel Junction

The spin-dependent trap-assisted hopping between a ferromagnetic metal and a nonmagnetic semiconductor is the key to explain the peculiarities of the magnetic field-dependent signal [63] in electrical spin injection experiments [27, 57–61]. The main conclusion which can be drawn from [63] is that the observed voltage signal is not due to the nonequilibrium spin injection but rather due to the strong magnetoresistance effect (Fig. 31.3). Another important physical system is a magnetic tunnel junction (MTJ). A MTJ represents a sandwich made of two ferromagnetic metals separated by a tunnel junction. As the current properties through the structure are solely determined by tunneling, a proper description of spin-dependent trap-assisted tunneling is paramount.

We consider the spin-dependent hopping transport between two noncollinear ferromagnetic contacts (Fig. 31.4). The ferromagnetic contacts are characterized by the spin current polarizations $\boldsymbol{p}_{1,2} = \frac{\Gamma^+_{1,2}-\Gamma^-_{1,2}}{2\Gamma_{1,2}} \frac{\mathbf{M}_{1,2}}{M_{1,2}}$ and the saturation magnetization $\mathbf{M}_{1,2}$. The tunneling rates from the source to the trap and from the trap to the drain are defined as an average of the rates with the spin-up (+) and spin-down (−) projection on the magnetization direction in the corresponding electrode: $\Gamma_{1(2)} = \frac{\Gamma^+_{1(2)}+\Gamma^-_{1(2)}}{2}$. In order to determine the escape probability $P_2(t) = 1 - n(t)$ from the trap, one has to solve (31.4). The tunneling rate from the ferromagnetic source electrode to the trap defining the occupation is the sum of the tunneling rates with the spin-up and the spin-down projections on the axis oriented along the source polarization p_1:

$$\Gamma_{\mathrm{S}\to\mathrm{Trap}} = \Gamma^+_1 + \Gamma^-_1 = 2\Gamma_1 \tag{31.11}$$

The rate (31.11) plays a similar role as Γ_N in sequential tunneling considered in the previous section. Although $\Gamma_{\mathrm{S}\to\mathrm{Trap}}$ does not depend on the spin polarization of the source, the electron on the trap originating from the ferromagnetic source electrode exhibits nonzero spin defined by the spin polarization p_1 as the ferromagnetic source electrode injects electrons with the spin defined by the source polarization vector. The nonzero initial spin generalizes the initial condition (31.7) to the case of trap-assisted tunneling between the two ferromagnetic electrodes [64]:

$$\begin{pmatrix} n \\ s_\mathrm{x} \\ s_\mathrm{y} \\ s_\mathrm{z} \end{pmatrix} (t=0) = \begin{pmatrix} 1 \\ p_1 \sin\zeta\cos\varphi \\ p_1 \sin\zeta\sin\varphi \\ p_1 \cos\zeta \end{pmatrix} \tag{31.12}$$

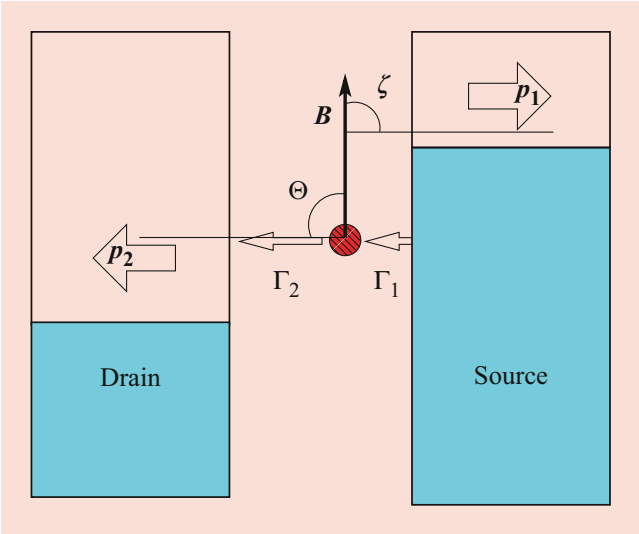

Fig. 31.4 For tunneling between two ferromagnetic electrodes, the direction of the source magnetization is specified by ζ and the polar angle φ, in addition to the angle Θ between the magnetic field and the drain magnetization

In order to evaluate the stationary current, it remains to solve (31.4, 31.5 and 31.6) with the initial condition (31.12) and the matrix $\mathbf{A}$ be modified so that $\boldsymbol{p}$ is replaced by $\boldsymbol{p}_2$ and Γ_F by Γ_2.

Results of the calculations are shown in Fig. 31.5. The magnetoresistance displays a more pronounced minimum at small magnetic fields as compared to tunneling from a normal metallic electrode. This is due to the fact that the probability to inject spins with the orientation opposite to p_2 causing the spin blockade is mostly determined by Γ^-_1 for the parameters chosen in Fig. 31.5 and is thus reduced as compared to the probability of tunneling of 50% from a normal metallic source electrode. The magnetoresistance also shows a dependence on the direction of the magnetic field in the case when $\boldsymbol{B}$, $\boldsymbol{p}_1$, and $\boldsymbol{p}_2$ are not lying within the same plane, although at high magnetic fields the symmetry with respect to the direction of the magnetic field is restored.

31.2.2 Single-Spin Transistor

We now analyze a three-terminal device in the configuration shown in Fig. 31.6, where the source "S," the gate "G," and the drain "D" are ferromagnetic, each described by the corresponding spin polarization $p_\alpha (\alpha = \mathrm{G(gate)}, \mathrm{S(source)}, \mathrm{D(drain)})$. The potential at the trap is determined by the gate voltage V_GS, the drain-source voltage V_DS, and the capacitances C_α, which are assumed equal to C. The current I_α is defined positive, if it flows from the electrode $\alpha = \mathrm{G(gate)}$,

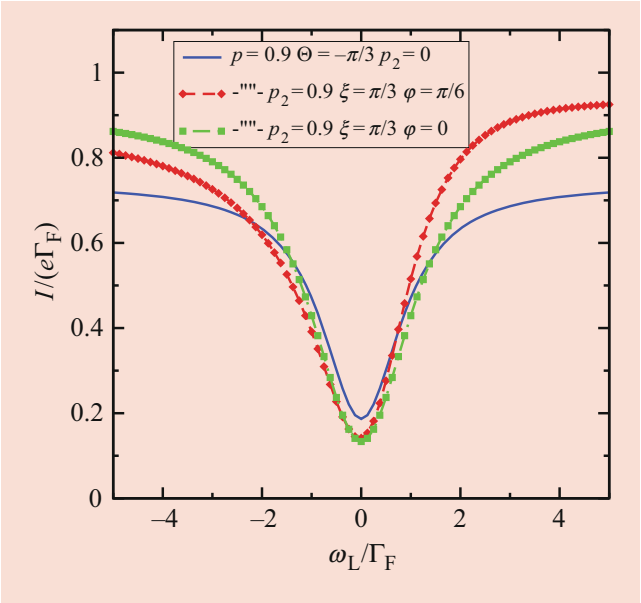

Fig. 31.5 Tunneling magnetoresistance for $p_1 = 0.9$, for different orientation and polarization p_2 of the source contact

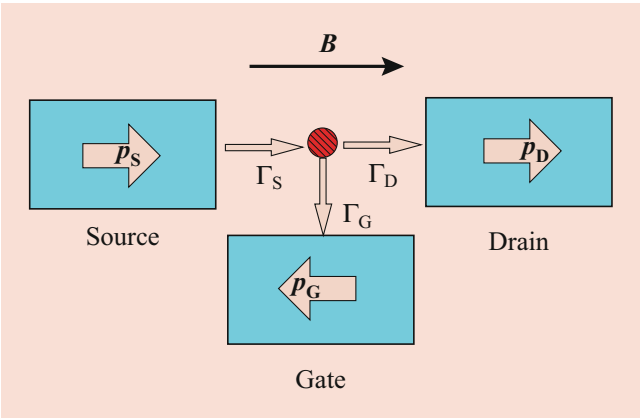

Fig. 31.6 A single-electron switch composed of an electron trap and three ferromagnetic contacts with an arbitrary relative magnetization orientation. Electron transport is due to trap-assisted spin-dependent hopping between the ferromagnetic contacts

S(source), or D(drain) to the trap. The current continuity $I_G + I_S + I_D = 0$ is thus automatically ensured.

In the case when there are several ferromagnetic terminals shown in Fig. 31.6, the spin correlations and thus the currents through each junction are determined by the generalized Eqs. (31.13a and 31.13b):

$$\frac{\mathrm{d}}{\mathrm{d}t}n = \Gamma_2\,(1-n) - \Gamma_1 n - \Gamma_1 \boldsymbol{p}_1 \mathbf{s},$$
$$\Gamma_{1(2)} = \sum_{\alpha'(\alpha'')} \Gamma_{\alpha'(\alpha'')} \tag{31.13a}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\mathbf{s} = \Gamma_2\,(1-n)\,\boldsymbol{p}_2 - \Gamma_1 \mathbf{s} - \boldsymbol{p}_1 \Gamma_1 n + [\mathbf{s}\times\boldsymbol{\omega}_\mathrm{L}],$$
$$\boldsymbol{p}_{1(2)} = \frac{1}{\Gamma_{1(2)}} \sum_{\alpha'(\alpha'')} \boldsymbol{p}_{\alpha'(\alpha'')}\Gamma_{\alpha'(\alpha'')} \tag{31.13b}$$

The sum is performed over the junctions $\alpha'(\alpha'')$ with the rates $\Gamma_{\alpha'(\alpha'')}$ of hopping from the electrode to the trap (from the trap to the electrode).

First we consider the single-electron transistor mode, where there is no tunneling between the trap and the gate $\Gamma_G = 0$ and all electrodes are non-ferromagnetic ($p_\alpha = 0$) (Fig. 31.7a). We apply a constant gate voltage $V_{GS} = e/C_G$. We evaluate the current by using the rates standard to single-electron tunneling as [71]

$$\Gamma_\alpha\,(V_\mathrm{eff}) = \Gamma_\alpha \left(\frac{V_\mathrm{eff}}{V_\mathrm{GS}}\right), \tag{31.14}$$

where $V_\mathrm{eff} = (V_\mathrm{b} + V_\mathrm{a})/2 > 0$ is the effective voltage of the junction α calculated as an average of the voltages before V_b and after V_a the electron jump.

For zero drain-source voltage V_{DS}, we are in the Coulomb blockade region with a single electron on the trap, and no current can flow between the source and drain (Fig. 31.7b). For $V_{DS} < V_{GS}/2$ the junction "trap-drain" is biased in opposite direction, and there is no source-drain current (Fig. 31.7b). As soon as $V_{DS} > V_{GS}/2$, the "trap-drain" junction is biased such that the electron can escape the trap. The Coulomb blockade is overcome by the drain voltage, and the current starts flowing (Fig. 31.7b).

If we now allow tunneling between the trap and the gate, $\Gamma_S = \Gamma_G = \Gamma_D \equiv \Gamma$, an electron from the trap can escape to the gate at $V_{GS} = e/(4C_G)$ (Fig. 31.8a). The electrodes are considered metallic with $p_\alpha = 0$. At $V_{DS} = 0$ the source is not biased with respect to the drain, and equal currents flow through the source and drain junctions from the electrodes, which then combine into the gate current (Fig. 31.8b). At $V_{DS} = V_{GS}$ the drain and gate junctions are equivalent, and the corresponding currents are equal. Making the source electrode ferromagnetic with high spin current polarization $p_S = 0.99$ does not modify the current-voltage characteristics as the escape from the trap is spin-independent in the case of a non-ferromagnetic gate and drain $p_G = p_D = 0$ (Fig. 31.8b).

However, when the drain is also ferromagnetic, $p_S = p_D = 0.99$, $p_G = 0$ (Fig. 31.9a), one observes an increase of the drain current at $V_{DS} > V_{GS}/2$ shown by the dashed-dotted lines in Fig. 31.9b. At these conditions the drain junction is positively biased, and the current flows easily between the source and drain since the magnetizations of the electrodes are parallel $p_S = p_D$. Therefore, the spin at the trap is also parallel to the magnetizations. Because the

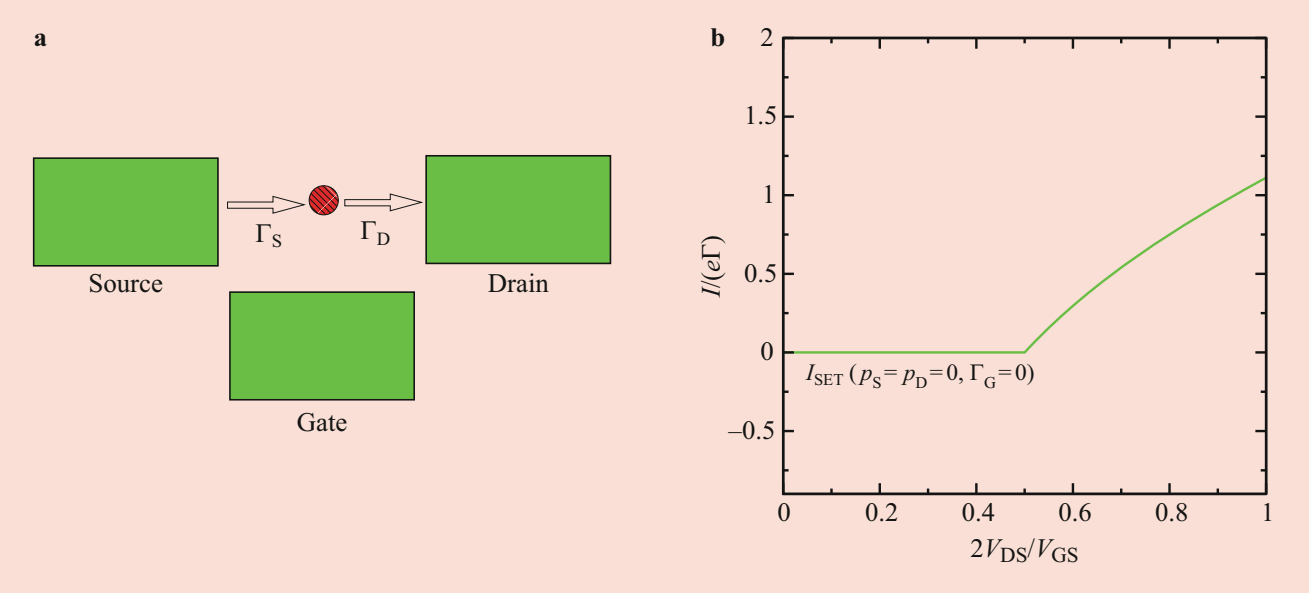

Fig. 31.7 (**a**) Single-electron transistor, (**b**) its source-drain current

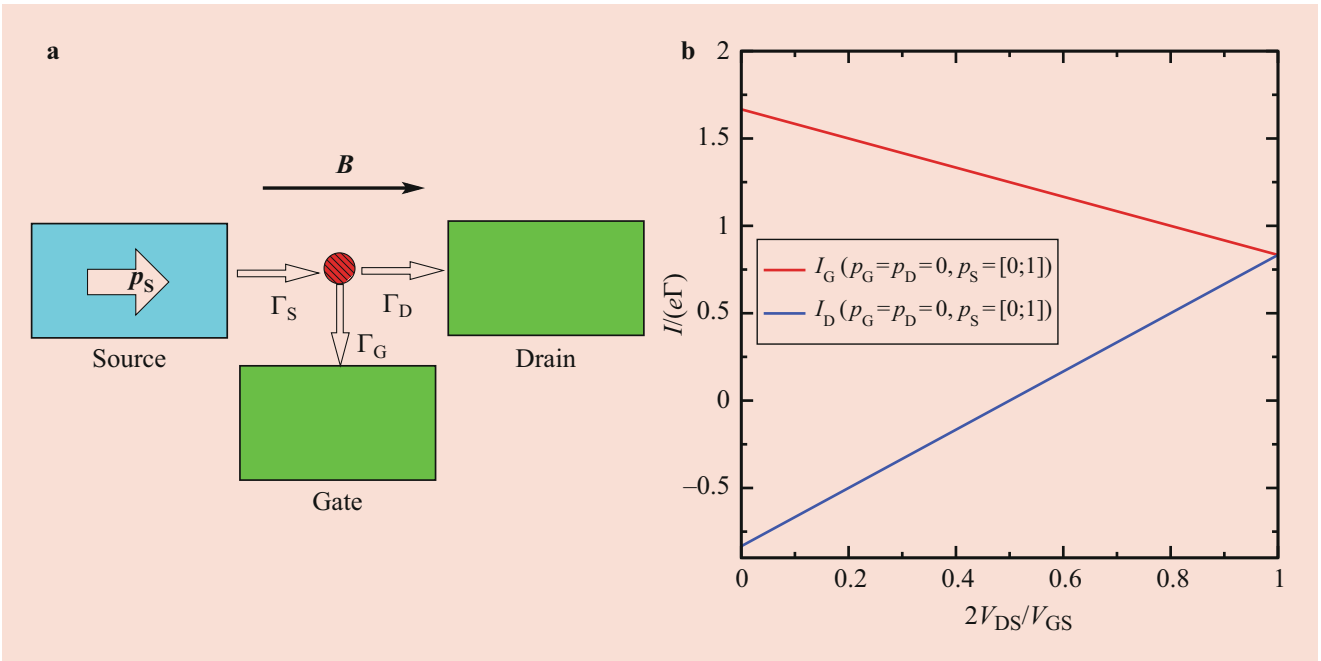

Fig. 31.8 (**a**) The source electrode is ferromagnetic, (**b**) currents through the gate and drain junctions

electron at the trap is spin-polarized, its probability to escape through the gate junction is reduced as only a single spin-polarized channel is open, in contrast to a spin-unpolarized electron, when both channels for spin-up and spin-down are open.

The situation changes dramatically when the gate is ferromagnetic, $p_G = 0.99$, $p_S = p_D = 0$ (Fig. 31.10a). At $V_{DS} < V_{GS}/2$, both the source and drain junctions are negatively biased, so that the electrons flow from these junctions to the trap and then try to escape to the highly polarized gate. The system is similar to the one with the trap-assisted tunneling between the normal metallic and the ferromagnetic electrode. In complete analogy to this case, the current suppression characteristic to spin-dependent hopping is observed in Fig. 31.10b.

At $V_{DS} > V_{GS}/2$, the drain junction is positively biased, and the spin blockade is lifted. An electron from the trap can always escape to the drain regardless of its spin. This leads

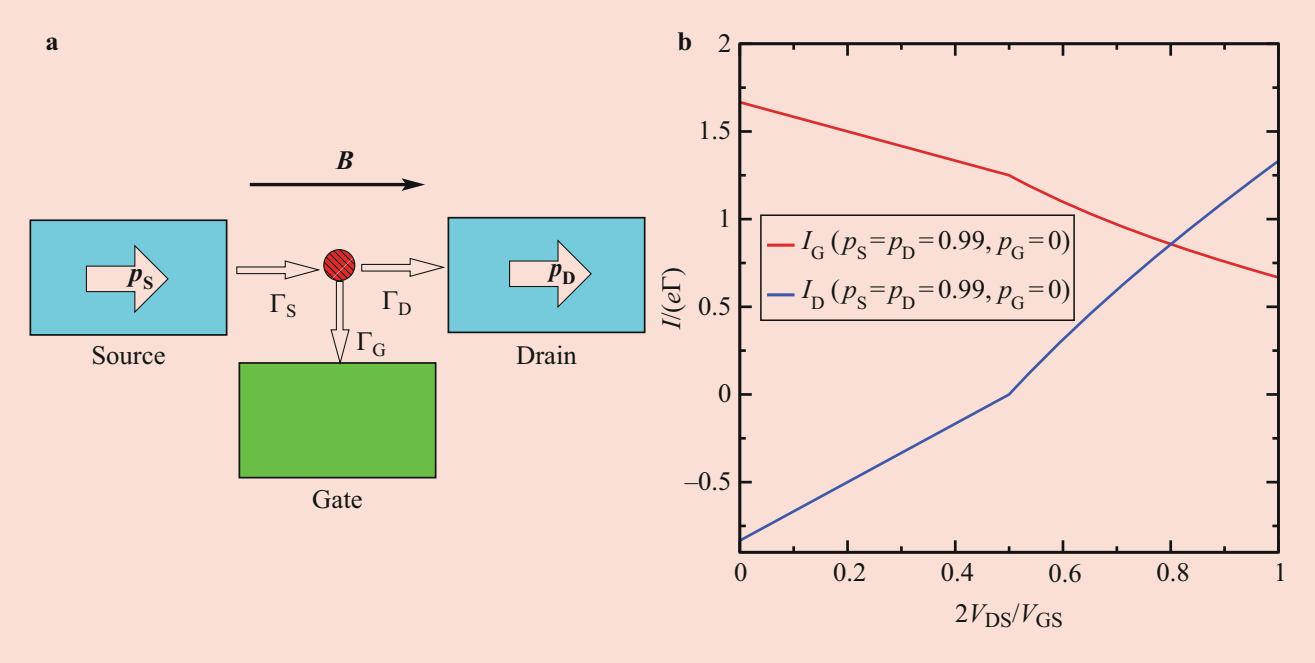

Fig. 31.9 (**a**) The source and drain electrode is ferromagnetic, (**b**) currents through the gate and drain junctions

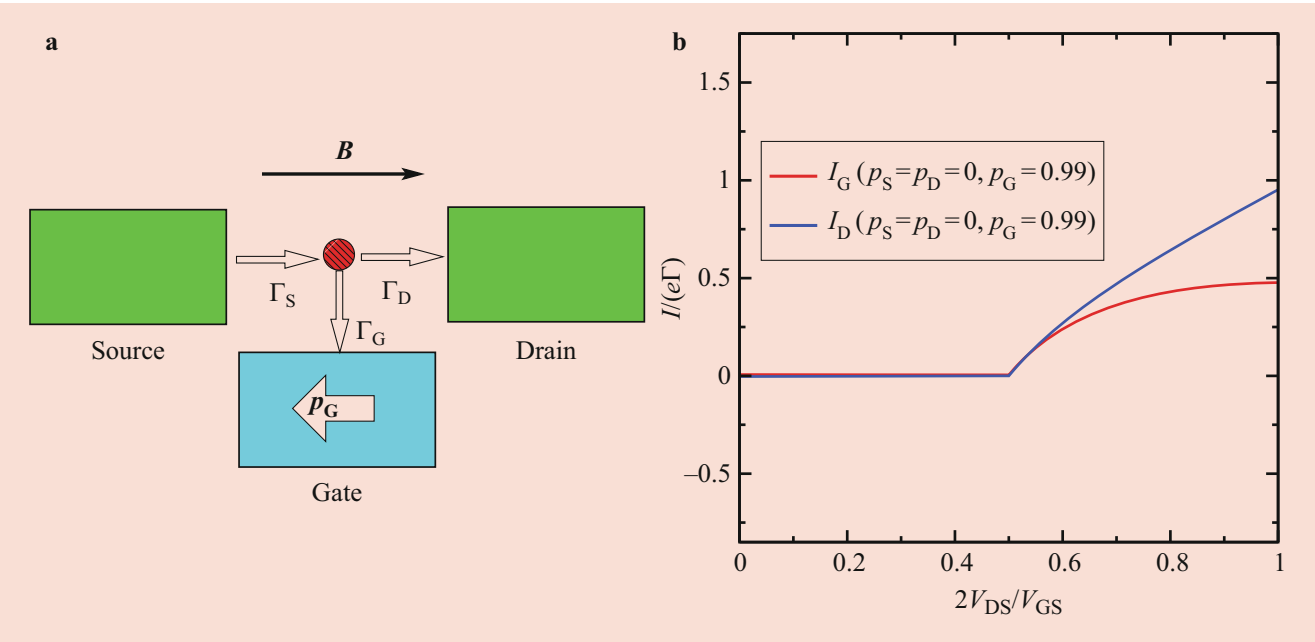

Fig. 31.10 (**a**) The gate electrode is ferromagnetic, (**b**) currents through the gate and drain junctions

to a nonzero drain current (Fig. 31.10b, solid line). Because the trapped electron with its spin opposite to p_G (which could not tunnel to the gate for $V_{DS} < V_{GS}/2$ and was responsible for blocking the gate current) can now easily escape to the drain, it does not block the current to the gate, and the gate current also starts flowing (Fig. 31.10b).

Adding ferromagnetism to the drain in the configuration shown in Fig. 31.11a ($p_G = -p_D, p_G = p_D = 0.99, p_S = 0$) does not alter the current-voltage behavior significantly (Fig. 31.11b). Since the source remains non-ferromagnetic, it provides electrons with spin parallel or antiparallel to p_G (or vice versa for p_D) with equal probability (50%). The

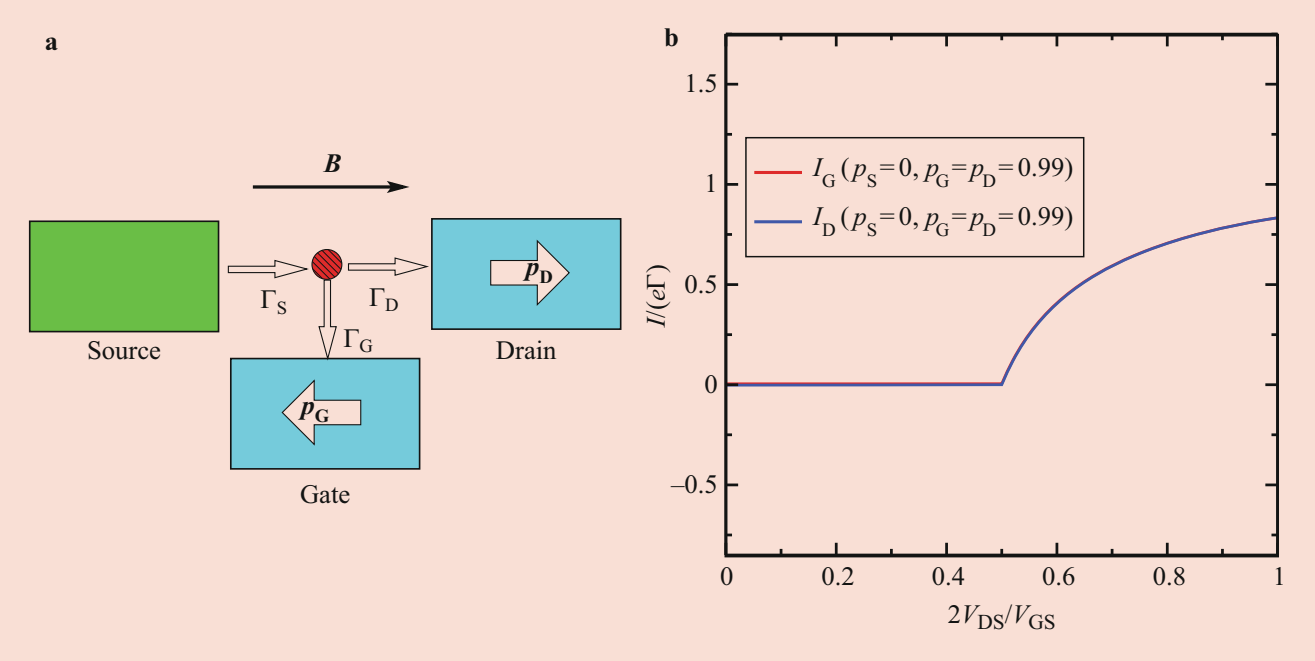

Fig. 31.11 (**a**) The gate and source electrodes are ferromagnetic, (**b**) currents through the gate and drain junctions

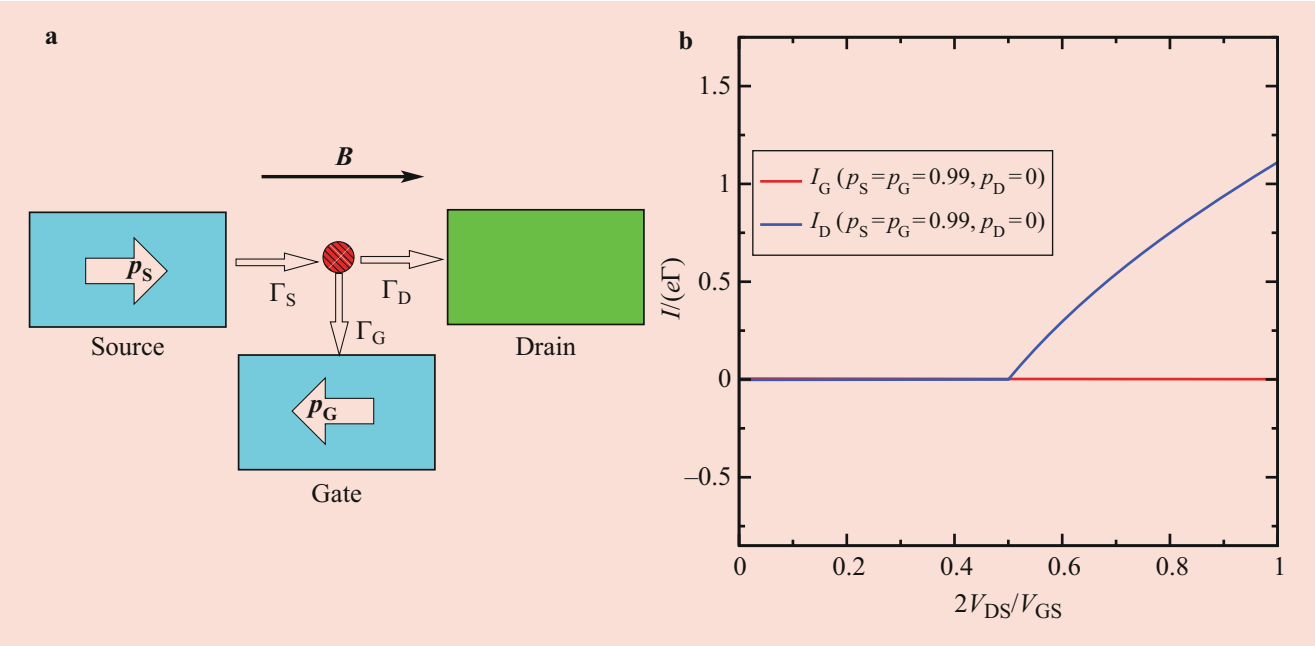

Fig. 31.12 (**a**) The source and gate electrodes are ferromagnetic, (**b**) currents through the gate and drain junctions

drain and gate currents are equal at $V_{DS} = V_{GS}$, although it is surprising that the currents are actually equal in the whole range $V_{DS} > V_{GS}/2$ (Fig. 31.11b).

Adding ferromagnetism to the source instead of the drain in the configuration in Fig. 31.12a ($p_G = -p_S$, $p_S = p_G = 0.99, p_D = 0$) does not alter the currents' blocking at $V_{DS} < V_{GS}/2$ (Fig. 31.12b). Indeed, the drain junction is negatively biased which prevents an electron to tunnel from the trap to the drain. The tunnel current into the gate is suppressed by the spin blockade as the drain electrode delivers electrons with the spin antiparallel to p_G with 50% probability, while the source delivers with probability 99%. These electrons cannot tunnel to the gate and thus block the gate current (Fig. 31.12b).

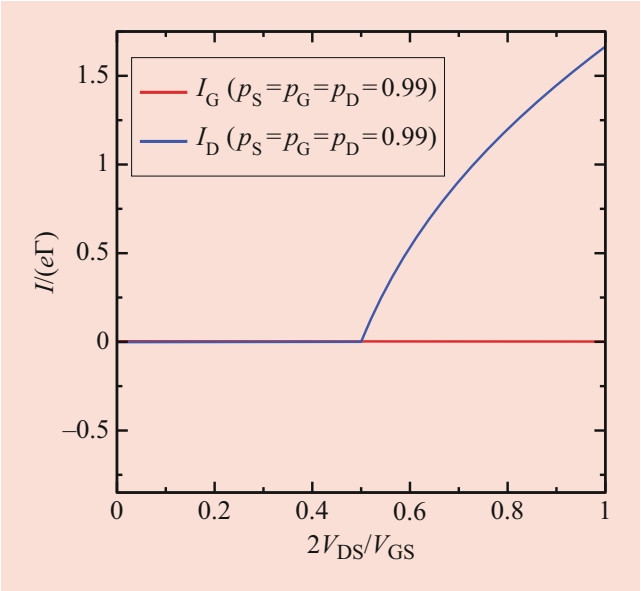

Fig. 31.13 Single-spin switch characteristics shown in Fig. 31.6. Electron transport is due to trap-assisted spin-dependent hopping between the ferromagnetic contacts

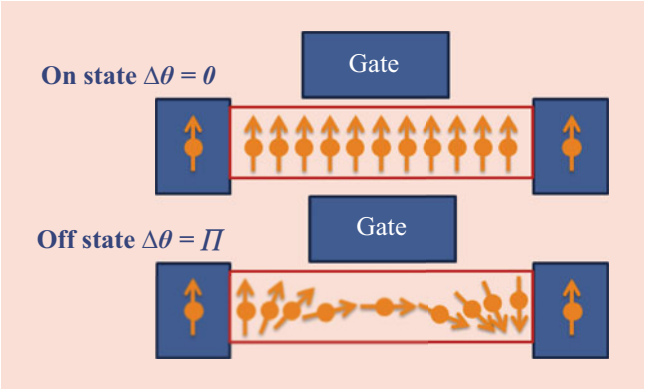

Fig. 31.14 Illustration of the SpinFET functionality [19]. Spin-polarized electrons are injected from a ferromagnetic source and absorbed by a ferromagnetic drain. The electron spins in the channel can be additionally manipulated by means of the gate voltage-dependent spin-orbit field

Because the source provides electrons with their spins mostly opposite to p_G, they cannot tunnel from the trap to the gate. The drain junction is positively biased at $V_{DS} > V_{GS}/2$, and the drain does not deliver electrons to the trap. Therefore, in contrast to Fig. 31.11b, the gate current remains negligible in the whole range of V_{DS} (Fig. 31.12b). The drain current is substantial at $V_{DS} > V_{GS}/2$ as electrons are allowed to tunnel to the normal metallic drain electrode.

Finally, if one considers all electrodes to be ferromagnetic in the configuration shown in Fig. 31.6 ($p_S = p_D = -p_G$, $p_S = p_G = p_D = 0.99$), mostly the electrons with their spins opposite to p_G are delivered to the trap. The gate current remains negligible in the whole range of V_{DS} Fig. 31.6. The drain current is blocked at $V_{DS} < V_{GS}/2$ (Fig. 31.13) as the gate junction is negatively biased, which prevents electrons tunneling to the drain. At $V_{DS} > V_{GS}/2$, the drain current flows. Since the source and the drain are strongly polarized with their magnetizations aligned, the current value shown in Fig. 31.13 is larger than in the case of a non-ferromagnetic drain (Fig. 31.12b) as only one-half of the states is now available in the drain to accommodate polarized electrons from the source. We stress that, although the current-voltage characteristic in Fig. 31.13 is qualitatively similar to that of a single-electron transistor (Fig. 31.7b), the suppression of the gate current and the switching is due to the spin correlations and the spin blockade at spin-dependent trap-assisted hopping in the considered three-terminal device with ferromagnetic electrodes.

31.2.3 Silicon SpinMOSFET and SpinFET

Successful injection and propagation of spins through a non-degenerate silicon channel lead to the first demonstration of a spin metal-oxide-semiconductor field-effect transistor (SpinMOSFET) [72] called by the analogy to a traditional charge-based MOSFET, the working horse of modern microelectronics. In contrast to the MOSFET, the current in SpinMOSFET flows between two ferromagnetic contacts. These contacts (source and drain) are connected by a nonmagnetic semiconducting channel region. Metallic ferromagnetic contacts serve not only as an injector/detector of the electron charge current in the channel. Because of their magnetization, these electrodes inject/detect electron spins [19]. The electron current is enhanced in the case of parallel alignment between the source/drain electrodes as electrons injected with spins parallel to the drain magnetization can easily escape from the channel to the drain. Alternatively, the current is suppressed for antiparallel magnetization alignment. As the magnetization of the source/drain can be manipulated by means of the external magnetic field and/or current (by means of the spin-transfer torque), the two on-current states for parallel/antiparallel magnetization alignment potentially enable the design of reprogrammable logic [73]. Importantly, the relative magnetization orientation between the source and drain is preserved without external power, which makes reprogrammable logic partly nonvolatile.

The spin signal is obtained as the current difference in parallel and antiparallel configuration of the source and drain magnetizations. For the first time, a high on/off ratio of spin signals was demonstrated [72] and, what is most important, at room temperature. However, the demonstrated device is different from the SpinFET first proposed in [19].

The SpinMOSFET differs from the SpinFET (Fig. 31.14) in one important aspect, namely, the gate voltage does not affect the spin polarization of the current. Indeed, the gate voltage is used to control the current through the channel. However, the spin orientation is solely determined by the injecting ferromagnetic contact orientation. The important ingredient of the SpinFET [19] is to employ the gate voltage-dependent effective spin-orbit field [74] to additionally manipulate spins propagating in the channel.

The idea is based on an earlier discovery of the gate voltage-dependent Bychkov-Rashba spin-orbit field [74]. In analogy with the magnetic field, the effective spin-orbit field acts on the electron spin and provides an additional momentum-dependent energy splitting between the opposite spin projections. This opens a possibility for a purely electrical way to manipulate the spin of a propagating electron. In a SpinFET the charge functionality is complemented and enhanced by the electron spin. In order to inject spins, the nonmagnetic source and drain electrodes are replaced by their ferromagnetic counterparts. The example of the SpinMOSFET demonstrates that the total current through the device depends on the relative orientation between the magnetization direction of the drain and the electron spin polarization at the end of the semiconductor channel. The electron current is maximal in the case of parallel alignment between the source and drain electrodes as electrons injected with spins parallel to the drain magnetization can easily escape from the channel to the drain. In contrast, the current is minimal when the source and drain are in antiparallel configuration. Therefore, the electron spin polarization orientation at the end of the channel relative to the drain magnetization direction additionally modulates the current through the SpinFET. As the spin polarization orientation can be manipulated by the gate voltage, it provides an additional knob to regulate the current through the device by means of spin.

Since the strength of the spin-orbit field depends on the potential gradient in the direction perpendicular to the channel, or the effective electric field, it can be conveniently controlled by the gate voltage. The fact that the spin-orbit field also depends on the electron momentum guarantees that all ballistically propagating electrons acquire the same spin rotation at the end of the channel [19]. This is in contrast to the case, where the spins are simply manipulated by the constant external magnetic field [52, 53], when the electron spin at the end of the channel depends on the time the electron travels through the channel. Because the electrons are injected with different velocity projections relative to the source-drain direction, the electrons reach the end of the channel with different spin orientations resulting in additional spin dephasing. Spin manipulation by means of the spin-orbit field is free from this unwanted dephasing, at least in the case of ballistic electron propagation through the channel. All electrons at the end of the channel acquire the same angle relative to the drain magnetization, the value of which is determined only by the strength of the spin-orbit field. The spin precession angle $\Delta\theta$ defined as the difference between the orientation of the spin of the electron at the end and at the beginning of the semiconductor region is [19].

$$\Delta\theta = \frac{2\alpha_R m^*}{\hbar^2} L, \tag{31.15}$$

where α_R is the strength of the spin-orbit interaction, which depends on the effective field, m^* is the effective mass of the electron, $\hbar$ is the reduced Plank's constant, and L is the length of the semiconductor channel. The strength of the spin-orbit interaction determines the minimum length of the semiconductor channel, sufficient to alternate the spin orientation.

The two dominant mechanisms of the spin-orbit interaction in well-investigated III-V semiconductor heterostructures are of the Rashba and the Dresselhaus type. The Rashba spin-orbit interaction is due to the geometrically induced structural asymmetry [74] in the system, while the Dresselhaus spin-orbit interaction is caused by the bulk inversion symmetry breaking [75]. The effective Hamiltonian of the spin-orbit interaction due to the confinement along the z-axis is in the form (Rashba type)

$$H_R = \frac{\alpha_R}{\hbar}\left(p_x\sigma_y - p_y\sigma_x\right), \tag{31.16}$$

where α_R is the effective electric field-dependent parameter of the spin-orbit interaction, $p_{x(y)}$ is the electron momentum projection, and σ_x and σ_y are the Pauli matrices. This is the typical gate-controlled contribution to the spin-orbit interaction in confined III-V semiconductor devices.

In silicon thin films, however, the Rashba spin-orbit interaction is relatively weak. Its strength is approximately one tenth of the value of the dominant contribution which, surprisingly, has a Dresselhaus form of the corresponding effective Hamiltonian [76, 77]:

$$H_D = \frac{\beta}{\hbar}\left(p_x\sigma_x - p_y\sigma_y\right) \tag{31.17}$$

This major contribution to the spin-orbit interaction is due to interfacial-induced disorder which breaks the inversion symmetry. The strength β of the Dresselhaus-like spin-orbit interaction depends almost linearly on the effective electric field, which is the case: $\beta \cong \beta^1 E_z$, where β^1 is the intra-valley coupling constant [77]. For a field strength of 50 kV/cm, the strength of the spin-orbit interaction is found to be $\beta \approx 2$ μeVnm [78], which is in agreement with the value reported experimentally [77], while $\alpha_R \approx 0.1$μeVnm. This

value of the Dresselhaus spin-orbit interaction in confined silicon structures is sufficient to consider them for applications as SpinFET channels.

To calculate the transport properties of the ballistic spin field-effect transistor, we consider a model similar to the one used in [79, 80]. The Hamiltonian in the ferromagnetic regions has the following form:

$$H = \frac{p_x^2}{2m_\mathrm{f}^*} + h_0\sigma_\mathrm{z}, \quad x < 0, \tag{31.18a}$$

$$H = \frac{p_x^2}{2m_\mathrm{f}^*} \pm h_0\sigma_\mathrm{z}, x > L, \tag{31.18b}$$

where m_f^* is the effective mass in the contacts, $h_0 = 2pE_\mathrm{F}/(P^2+1)$ is the exchange splitting energy with p defined as the spin polarization in the ferromagnetic regions, E_F is the Fermi energy, and σ_z is the Pauli matrix; $\pm$ in (31.18a and 31.18b) stands for the parallel and antiparallel configuration of the contact magnetizations. The spin-orbit interaction is taken in the Dresselhaus form relevant for silicon. The effective Hamiltonian in the channel is

$$H = \frac{p_\mathrm{x}^2}{2m^*} + \delta E_\mathrm{c} - \frac{\beta}{\hbar}\sigma_\mathrm{x}p_\mathrm{x} + \frac{1}{2}g\mu_\mathrm{B}B\sigma^*, \tag{31.19}$$

where m^* is the subband effective mass, g is the Landé factor, μ_B is the Bohr magneton, B is the magnetic field, and $\sigma^* \equiv \sigma_\mathrm{x}\cos\gamma + \sigma_\mathrm{y}\sin\gamma$ with γ defined as the angle between the magnetic field and the transport direction.

To calculate the dependence of the transport properties on the strength of the spin-orbit interaction, we take the wave function in the left contact as follows:

$$\Psi_\mathrm{L}(x) = \left(\mathrm{e}^{ik_\uparrow x} + R_\uparrow \mathrm{e}^{-ik_\uparrow x}\right)\begin{pmatrix}1\\0\end{pmatrix} + R_\downarrow \mathrm{e}^{-ik_\downarrow x}\begin{pmatrix}0\\1\end{pmatrix} \tag{31.20}$$

$$\Psi_\mathrm{L}(x) = R_\uparrow \mathrm{e}^{-ik_\uparrow x}\begin{pmatrix}1\\0\end{pmatrix} + \left(\mathrm{e}^{ik_\downarrow x} + R_\downarrow \mathrm{e}^{-ik_\downarrow x}\right)\begin{pmatrix}0\\1\end{pmatrix} \tag{31.21}$$

where (31.20) represents the incoming spin-up electrons and (31.21) the incoming spin-down electrons; correspondingly, $k_{\uparrow(\downarrow)} = \sqrt{2m_\mathrm{f}^*(E \mp h_0)/\hbar^2}$ is the wave vector of the spin-up (spin-down) electron, and $R_{\uparrow(\downarrow)}$ is the amplitude of the reflected wave. For the right contact, the wave function is given by

$$\Psi_\mathrm{R}(x) = C_\uparrow \mathrm{e}^{ik_\uparrow x}\begin{pmatrix}1\\0\end{pmatrix} + C_\downarrow \mathrm{e}^{ik_\downarrow x}\begin{pmatrix}0\\1\end{pmatrix}. \tag{31.22}$$

For the semiconductor region, the wave function can be written as

$$\begin{aligned}\Psi_\mathrm{S}(x) = A_+\mathrm{e}^{ik_{\mathrm{x1}}^{(+)}x}\begin{pmatrix}k_1\\1\end{pmatrix} + B_+\mathrm{e}^{ik_{\mathrm{x2}}^{(+)}x}\begin{pmatrix}k_2\\1\end{pmatrix}\\ A_-\mathrm{e}^{ik_{\mathrm{x1}}^{(-)}x}\begin{pmatrix}k_3\\-1\end{pmatrix} + B_-\mathrm{e}^{ik_{\mathrm{x2}}^{(-)}x}\begin{pmatrix}k_4\\-1\end{pmatrix},\end{aligned} \tag{31.23}$$

where $k_{\mathrm{x1}(x2)}^{(+)}$ and $k_{\mathrm{x1}(x2)}^{(-)}$ are the wave vectors obtained by solving the equations $\frac{\hbar^2k^2}{2m^*} + \delta E_\mathrm{c} \pm \sqrt{\left(\frac{Bg\mu_\mathrm{B}\cos(\gamma)}{2}\right)^2 + \left(\frac{Bg\mu_\mathrm{B}\sin(\gamma)}{2} - \beta k\right)^2} = E$, respectively. The constants k_1, k_2, k_3, and k_4 are calculated as

$$k_1 = -\frac{i\left(Bg\mu_\mathrm{B}\sin(\gamma) - 2\beta k_{\mathrm{x1}}^{(+)}\right) - Bg\mu_\mathrm{B}\cos(\gamma)}{2\sqrt{\left(\frac{Bg\mu_\mathrm{B}\cos(\gamma)}{2}\right)^2 + \left(\frac{Bg\mu_\mathrm{B}\sin(\gamma)}{2} - \beta k_{\mathrm{x1}}^{(+)}\right)^2}}, \tag{31.24}$$

$$k_2 = -\frac{i\left(Bg\mu_\mathrm{B}\sin(\gamma) - 2\beta k_{\mathrm{x2}}^{(+)}\right) - Bg\mu_\mathrm{B}\cos(\gamma)}{2\sqrt{\left(\frac{Bg\mu_\mathrm{B}\cos(\gamma)}{2}\right)^2 + \left(\frac{Bg\mu_\mathrm{B}\sin(\gamma)}{2} - \beta k_{\mathrm{x2}}^{(+)}\right)^2}}, . \tag{31.25}$$

$$k_3 = \frac{i\left(Bg\mu_\mathrm{B}\sin(\gamma) - 2\beta k_{\mathrm{x1}}^{(-)}\right) - Bg\mu_\mathrm{B}\cos(\gamma)}{2\sqrt{\left(\frac{Bg\mu_\mathrm{B}\cos(\gamma)}{2}\right)^2 + \left(\frac{Bg\mu_\mathrm{B}\sin(\gamma)}{2} - \beta k_{\mathrm{x1}}^{(-)}\right)^2}}, \tag{31.26}$$

$$k_4 = \frac{i\left(Bg\mu_\mathrm{B}\sin(\gamma) - 2\beta k_{\mathrm{x2}}^{(-)}\right) - Bg\mu_\mathrm{B}\cos(\gamma)}{2\sqrt{\left(\frac{Bg\mu_\mathrm{B}\cos(\gamma)}{2}\right)^2 + \left(\frac{Bg\mu_\mathrm{B}\sin(\gamma)}{2} - \beta k_{\mathrm{x2}}^{(-)}\right)^2}}. \tag{31.27}$$

The reflection and transmission coefficients are determined by applying the standard boundary conditions at the ferromagnet/semiconductor interfaces. We compute the current through the device as

$$\begin{aligned}I^{\mathrm{P(AP)}}(V) = \frac{e}{h}\int_{\delta E_\mathrm{c}}^{\infty}\left[T_\uparrow^{\mathrm{P(AP)}}(E) + T_\downarrow^{\mathrm{P(AP)}}(E)\right]\\ \left\{\frac{1}{1+\mathrm{e}^{\frac{E-E_\mathrm{F}}{k_\mathrm{B}T}}} - \frac{1}{1+\mathrm{e}^{\frac{E-E_\mathrm{F}+eV}{k_\mathrm{B}T}}}\right\}\mathrm{d}E,\end{aligned} \tag{31.28}$$

where k_B is the Boltzmann constant, T is the temperature, and V is the voltage. The spin-up ($T_\uparrow^\mathrm{P}$) and spin-down ($T_\downarrow^\mathrm{P}$) transmission probabilities for the parallel configuration of the contact magnetization are defined as

$$T_{\uparrow}^{\mathrm{P}} = \left|C_{\uparrow}\right|^2 + \frac{k_{\downarrow}}{k_{\uparrow}}\left|C_{\downarrow}\right|^2, \tag{31.29}$$

$$T_{\downarrow}^{\mathrm{P}} = \frac{k_{\uparrow}}{k_{\downarrow}}\left|C_{\uparrow}\right|^2 + \left|C_{\downarrow}\right|^2. \tag{31.30}$$

For the antiparallel configuration of the contact magnetization, the transmission probability is obtained in a similar fashion.

The conductance is defined as

$$G^{\mathrm{P(AP)}} = \lim_{V\to 0}\frac{I^{\mathrm{P(AP)}}}{V}. \tag{31.31}$$

In the limit of low temperatures, the conductance must coincide with the one obtained from the Landauer-Büttiker formula:

$$G^{\mathrm{P(AP)}} = \frac{e^2}{h}\left(T_{\uparrow}^{\mathrm{P(AP)}}(E_{\mathrm{F}}) + T_{\downarrow}^{\mathrm{P(AP)}}(E_{\mathrm{F}})\right) \tag{31.32}$$

Finally, the magnetoresistance ratio (MR) is computed as

$$\mathrm{MR} \equiv \frac{G^{\mathrm{P}} - G^{\mathrm{AP}}}{G^{\mathrm{AP}}}. \tag{31.33}$$

To facilitate the injection of the spin-polarized current into the channel, we introduce, following [79, 80], delta-function barriers of the strength U at the interfaces between the contact and the channel, which we characterize by the dimensionless effective strength $z = 2m_{\mathrm{f}}^* U/\left(\hbar^2 k_{\mathrm{F}}\right)$, where $k_{\mathrm{F}} = \sqrt{2m_{\mathrm{f}}^* E_{\mathrm{F}}/\hbar^2}$ at the interfaces between the contact and the channel.

The dependence of the MR on the strength of the spin-orbit interaction is shown in Fig. 31.15, for several channel lengths, at zero temperature. A more pronounced magnetoresistance modulation with the strength of the spin-orbit interaction is obtained for longer channels. In order to completely benefit from the magnetoresistance modulation, the channel length L should be larger than the inverse of the characteristic wave vector $k_{\mathrm{D}} = m^*\beta/\hbar^2$, which determines the dependence of the MR on the value of the strength of the Dresselhaus spin-orbit interaction β: $L \geq 1/k_{\mathrm{D}}$.

A thin silicon film channel of *[100]* orientation possesses a larger transport effective mass m^* [81, 82] compared to one which is *[110]* oriented. Therefore, a smaller variation of β is required in *[100]* oriented films to achieve the same k_{D} and thus the same variation of the MR. Thus, *[100]* oriented channels are best suited to be used as channels in silicon SpinFETs.

Figure 31.16 displays the magnetoresistance dependence on the strength of the spin-orbit interaction at different temperatures for a device with an 8-μm-long channel, for 1 meV source-drain voltage. The MR modulation is preserved at higher temperatures opening a practical possibility to modulate the current by changing the value of β at room temperature.

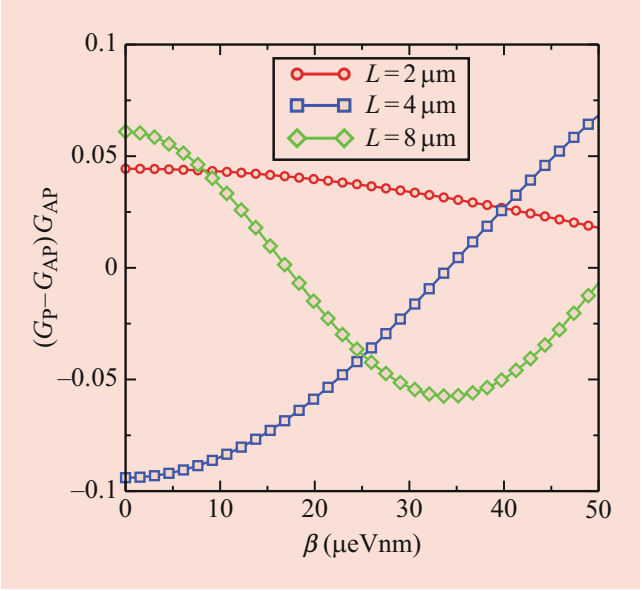

Fig. 31.15 MR dependence on the value of the Dresselhaus spin-orbit interaction for several channel lengths. The Fermi energy in the ferromagnetic source and drain is $E_{\mathrm{F}} = 2.47$ eV, the electrode spin current polarization $p = 0.4$, the silicon conduction band offset $\delta E_{\mathrm{c}} = 2.154$ eV, the tunnel barriers of the strength $z = 1$

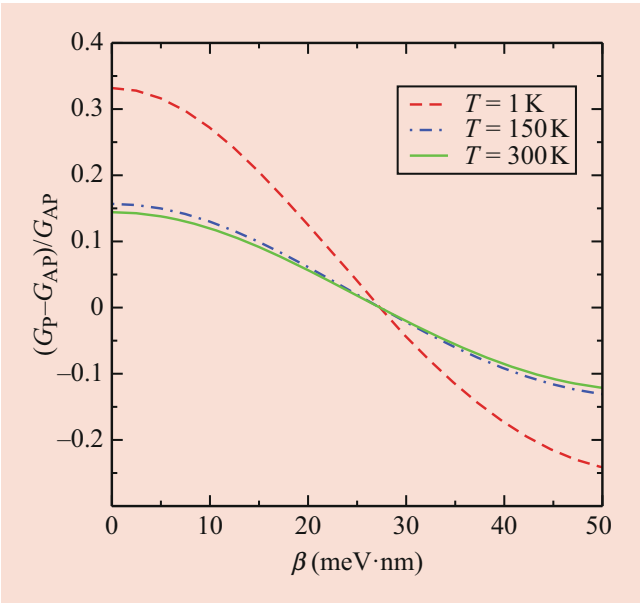

Fig. 31.16 Magnetoresistance dependence on the strength of the spin-orbit field for a *[100]* oriented channel with length $L = 8$ μm, for $E_{\mathrm{F}} = 2.47$ eV, $\delta E_{\mathrm{c}} = 2.154$ eV, $P = 0.4$, $z = 3$, $V = 1$ meV

Therefore, in principle, the spin-orbit field in silicon could be used to manipulate spins and to achieve the current modulation by means of spin. However, to potentially benefit from the current modulation due to the gate voltage-dependent

strength of the spin-orbit field, the silicon channel length must be as long as a few microns. Even if a silicon SpinFET were fabricated, it must compete with modern devices with a channel 100 times shorter. In order to decrease the channel length, the gate voltage-dependent spin-orbit field shall be increased.

The effective electric field-dependent parameter of the spin-orbit interaction is several orders of magnitude larger in III-V semiconductors, so the channel length needed for current modulation due to the voltage-dependent spin-orbit field can be shorter. However, the strong spin-orbit field needed for spin manipulation leads to a strong spin relaxation as well. Indeed, the spin-orbit field depends on the electron momentum. After a scattering event, the electron momentum changes, as does the direction of the spin-orbit field. Because the spin-orbit field defines the axis around which the electron spin precesses, the spin precesses around a different axis after scattering. After another scattering event, the field and the axis of precession are changed again. The most important scattering mechanism in bulk semiconductors at room temperature is electron-phonon scattering. As the electron-phonon scattering happens at random position and time, the information about the initial spin orientation and the angle it acquires while propagating along the channel are rapidly randomized. In order to avoid the randomization and maintain the spin precession coherence, one way is to reduce electron-phonon scattering. Therefore, a SpinFET made with a III-V semiconductor channel can only operate at cryogenic temperature.

An elegant solution to the problem of injecting spin-polarized electrons without using ferromagnetic contacts was proposed recently [83]. It resulted in the first demonstration of an all electrical SpinFET [83] with two gates. The idea is to employ again the spin-orbit field. The effective spin-orbit field guarantees that the electrons having their momentum along the propagation direction are spin-polarized. This idea allows to reliably inject spin-polarized electrons through the point contact created electrostatically by the corresponding additional gates [83]. By applying the potential difference between these gates, one ensures that the electrons moving from the contact to the channel and therefore having the momentum in this direction are spin-polarized. Using this innovative injection technique, the current modulation by means of the gate voltage-dependent spin-orbit field was confirmed. This provided the first successful demonstration of a SpinFET [83] 25 years after it had been predicted [19].

31.2.4 Spin Relaxation Suppression in Silicon Films

Before concluding the spin switches part, let us briefly discuss spin relaxation mechanisms in silicon. In contrast to the electron charge, the non-equilibrium spin accumulation injected into the channel relaxes to its equilibrium zero value while propagating through the channel and is not conserved. Spin relaxation is an important detrimental factor affecting the SpinFET functionality as it reduces the current modulation due to spin functionality. To avoid spin dephasing, the experiment [83] must be performed at an extremely low temperature of 30 mK.

The question then appears why silicon SpinMOSFET functionality was demonstrated at 300 K with a channel length of four micrometers [72]. Of course, the spin-orbit interaction is much weaker in silicon. In addition, the spin relaxation manifests itself completely different in semiconductors of the group IV, in which silicon belongs to, in contrast to III-V semiconductors. The crystal lattice of silicon obeys the inversion symmetry, while the crystal structure of III-V materials does not. If, in addition to the time-reversal symmetry, the structure obeys the inversion symmetry, then the electrons with spin-up and spin-down propagating with the same momentum are not allowed to have different energies, so the effective spin-orbit field causing the energy splitting in III-V semiconductors is zero in silicon. The spin relaxation in silicon is governed by a different mechanism [47, 84] called the Elliott-Yafet spin relaxation mechanism. A short explanation of the spin relaxation is as follows. Spins are injected with a fixed spin projection. However, the wave function with fixed spin projection is not an eigenstate of the Hamiltonian with the microscopic spin-orbit interaction included. In other words, the spin eigenfunction contains both a spin-up and a small spin-down part with respect to the axis of spin injection. Therefore, a small but finite probability to flip the electron spin appears at every scattering event, even if the scattering potential is spin-independent. This is the Elliott process [47] contributing to the spin relaxation in silicon. This process is complemented by the Yafet spin-flip events due to the spin-dependent contribution to the scattering potential. In bulk silicon the electron spin relaxation is determined by the transitions between non-equivalent valleys [47]. As uniaxial stress lifts the degeneracy between these valleys, the rates of the inter-valley transition are decreased, and the spin lifetime can be efficiently controlled by stress [84].

However, if a silicon SpinMOSFET is implemented in the future, it must be fabricated with the help of the technology used to produce modern CMOS transistors. In contrast to the experiment [72], where the current modulation through an 80-nm-thick silicon layer was performed by the back gate, the channel in modern CMOS devices is represented by a narrow fin or a thin sheet. As the electrons are transferred close to the interface, the role of the surface roughness in determining the spin relaxation in thin silicon channels must be understood. Indeed, it is known that the electron mobility in thin silicon body channels is determined not only by the

electron-phonon interaction but mostly by surface roughness scattering [85] and is significantly reduced as compared to the electron mobility in the bulk. An important question therefore is to determine how surface roughness scattering affects the spin relaxation in thin silicon films and what can be done in order to reduce the spin relaxation and to enhance the spin lifetime and the spin diffusion length.

In order to compute the spin relaxation, the rates must be evaluated. To do so, the scattering mechanisms as well as the corresponding wave functions and an effective Hamiltonian to determine the wave functions must be established. We adopt a **k**·**p**-based approach [86–88] suitable to describe the unprimed electron subbands in (001) silicon films in the presence of strain and spin-orbit interaction. The effective Hamiltonian includes only the relevant *[001]* oriented valleys with spin degree. The other valleys or, to be more precise, the corresponding subbands have larger energies due to a smaller effective quantization mass [86] and are disregarded.

Without the spin interaction, the unprimed subbands resulting from *[001]* oriented valleys are degenerate in the unstrained (001) film. The Hamiltonian is written in the vicinity of the X point along the k_z-axis in the Brillouin zone. The basis is conveniently chosen as $[(X_1,\uparrow), (X_1,\downarrow), (X_{2'},\uparrow), (X_{2'},\downarrow)]$, where $\uparrow$ and $\downarrow$ indicate the spin projection at the quantization $z-$ axis and X_1 and $X_{2'}$ are the basis function corresponding to the two *[001]* valleys. The effective **k**·**p** Hamiltonian reads as

$$H = \begin{bmatrix} H_1 & H_3 \\ H_3^{\dagger} & H_2 \end{bmatrix} \tag{31.34}$$

where H_1, H_2, and H_3 are defined as [28]

$$H_1 = \left[\frac{\hbar^2 k_z^2}{2m_l} - \frac{\hbar^2 k_0 k_z}{m_l} + \frac{\hbar^2\left(k_x^2 + k_y^2\right)}{2m_t} + U(z) \right] I_{2\times 2}, \tag{31.35}$$

$$H_2 = \left[\frac{\hbar^2 k_z^2}{2m_l} + \frac{\hbar^2 k_0 k_z}{m_l} + \frac{\hbar^2\left(k_x^2 + k_y^2\right)}{2m_t} + U(z) \right] I_{2\times 2}, \tag{31.36}$$

$$H_3 = \begin{bmatrix} D\varepsilon_{xy} - \frac{\hbar^2 k_x k_y}{M} & \left(k_y - k_x i\right)\Delta_{SO} \\ \left(-k_y - k_x i\right)\Delta_{SO} & D\varepsilon_{xy} - \frac{\hbar^2 k_x k_y}{M} \end{bmatrix}. \tag{31.37}$$

Here $I_{2\times 2}$ is the identity 2×2 matrix, m_t and m_l are the transversal and longitudinal silicon effective masses, $k_0 = 0.15 \times 2\pi/a$ is the position of the valley minimum relative to the X point in unstrained silicon, a is the silicon lattice constant, ε_{xy} denotes the shear strain component, $M^{-1} \approx m_t^{-1} - m_0^{-1}$, and $D = 14$ eV is the shear strain deformation potential. The effective spin-orbit term $\Delta_{SO}\,\tau_y \otimes (k_x\,\sigma_x - k_y\,\sigma_y)$ couples the states with the opposite spin projections from the opposite valleys. σ_x and σ_y are the spin Pauli matrices and τ_y is the y-Pauli-like matrix in the valley degree of freedom space. In the Hamiltonian (31.1) $U(z)$ is the confinement potential, and the value $\Delta_{SO} = 1.27$ meVnm computed by the empirical pseudopotential method (Fig. 31.17) is close to the one reported by Li and Dery [47].

The Hamiltonian H_3 describes the coupling between the two valleys along *[001]* direction. Shear strain term couples the two valley states with the same spin projection, while the spin-orbit term couples the two states from the opposite valleys with the opposite spin projections. In the case $H_3 = 0$, each eigenstate of the Hamiltonian (31.1) is four times degenerate with respect to the valleys and spin quantum numbers. The confinement potential does not lift the degeneracy. With the confinement potential included, one obtains the ladder of four times degenerate two-dimensional unprimed subbands.

It is known that shear strain lifts the degeneracy between the unprimed subbands [28]. Applying shear strain results in a stress-dependent mobility enhancement along the tensile stress direction. However, the electron mobility enhancement is determined by inter-valley scattering. Therefore, the electron mobility enhancement is due to the transport effective mass reduction with strain.

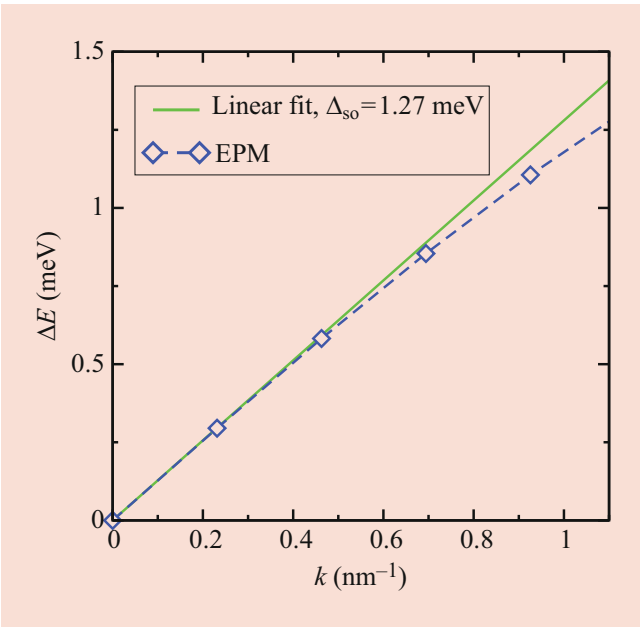

Fig. 31.17 Empirical pseudopotential calculations of the spin-orbit interaction strength by evaluating the energy difference between the *[001]* valleys at the X-point as a function of k_x. The linear fit is also shown

The spin relaxation in silicon is determined by inter-valley scattering. Therefore, the role of strain-induced valley splitting must be more pronounced regarding the spin relaxation time dependencies. The spin-orbit interaction couples the opposite valleys along the *[001]* crystallographic axis and should also result in valley splitting. However, in the case of a symmetric confinement potential, the spin degeneracy must be preserved, as it is required by the inversion and the time-reversal symmetries of the system.

To demonstrate this, we perform the unitary transformation of the Hamiltonian by transforming the four basis functions $X_{1\uparrow}$, $X_{1\downarrow}$, $X_{2\uparrow}{}'$, $X_{2\downarrow}{}'$,for the two [001] valleys with spin up and spin down as

$$\Psi_1 = \frac{1}{2}\left[\left(X_{1\uparrow} + X'_{2\uparrow}\right) + \left(X_{1\downarrow} + X'_{2\downarrow}\right)\frac{k_x - ik_y}{\sqrt{k_x^2 + k_y^2}}\right], \tag{31.38}$$

$$\Psi_2 = \frac{1}{2}\left[\left(X_{1\uparrow} + X'_{2\uparrow}\right) - \left(X_{1\downarrow} + X'_{2\downarrow}\right)\frac{k_x - ik_y}{\sqrt{k_x^2 + k_y^2}}\right], \tag{31.39}$$

$$\Psi_3 = \frac{1}{2}\left[\left(X_{1\uparrow} - X'_{2\uparrow}\right) + \left(X_{1\downarrow} - X'_{2\downarrow}\right)\frac{k_x - ik_y}{\sqrt{k_x^2 + k_y^2}}\right], \tag{31.40}$$

$$\Psi_4 = \frac{1}{2}\left[\left(X_{1\uparrow} - X'_{2\uparrow}\right) - \left(X_{1\downarrow} - X'_{2\downarrow}\right)\frac{k_x - ik_y}{\sqrt{k_x^2 + k_y^2}}\right], \tag{31.41}$$

$$X_1 = \Psi_1 \cos\left(\frac{\Theta}{2}\right) - i\Psi_3 \sin\left(\frac{\Theta}{2}\right), \tag{31.42}$$

$$X_2 = \Psi_2 \cos\left(\frac{\Theta}{2}\right) + i\Psi_4 \sin\left(\frac{\Theta}{2}\right), \tag{31.43}$$

$$X_3 = \Psi_3 \cos\left(\frac{\Theta}{2}\right) - i\Psi_1 \sin\left(\frac{\Theta}{2}\right), \tag{31.44}$$

$$X_4 = \Psi_4 \cos\left(\frac{\Theta}{2}\right) + i\Psi_2 \sin\left(\frac{\Theta}{2}\right). \tag{31.45}$$

Here $\tan(\Theta) = \frac{\Delta_{SO}\sqrt{k_x^2+k_y^2}}{D\varepsilon_{xy} - \frac{\hbar^2 k_x k_y}{M}}$. The transformation decouples the two degenerate sub-ladders. In the new basis, the Hamiltonian (31.34) can be recast as

$$h = \begin{bmatrix} h_1 & h_3 \\ h_3 & h_2 \end{bmatrix} \tag{31.46}$$

h_1, h_2, and h_3 are defined as

$$h_1 = \left[\frac{\hbar^2 k_z^2}{2m_l} + \frac{\hbar^2\left(k_x^2 + k_y^2\right)}{2m_t} - \delta + U(z)\right] I, \tag{31.47}$$

$$h_2 = \left[\frac{\hbar^2 k_z^2}{2m_l} + \frac{\hbar^2\left(k_x^2 + k_y^2\right)}{2m_t} + \delta + U(z)\right] I, \tag{31.48}$$

$$h_3 = \begin{bmatrix} \frac{\hbar^2 k_0 k_z}{m_l} & 0 \\ 0 & \frac{\hbar^2 k_0 k_z}{m_l} \end{bmatrix}, \tag{31.49}$$

where

$$\delta = \sqrt{\left(D\varepsilon_{xy} - \frac{\hbar^2 k_x k_y}{M}\right)^2 + \Delta_{SO}^2\left(k_x^2 + k_y^2\right)}. \tag{31.50}$$

It is straightforward to see that the 4×4 Hamiltonian (31.46) splits into the two 2×2 Hamiltonians

$$L_{1,2} = \begin{bmatrix} \frac{\hbar^2 k_z^2}{2m_l} + \frac{\hbar^2\left(k_x^2+k_y^2\right)}{2m_t} - \delta + U(z) & \frac{\hbar^2 k_0 k_z}{m_l} \\ \frac{\hbar^2 k_0 k_z}{m_l} & \frac{\hbar^2 k_z^2}{2m_l} + \frac{\hbar^2\left(k_x^2+k_y^2\right)}{2m_t} + \delta + U(z) \end{bmatrix} \tag{31.51}$$

acting on the independent sub-spaces with the basis functions X_1, X_3 and X_2, X_4, correspondingly. We note that the spin projection of X_1 (X_3) is opposite to that of X_2 (X_4). Therefore, the Hamiltonians $L_{1,2}$ define the two sub-ladders of the subbands. As the Hamiltonians $L_{1,2}$ have the same form, the energies of the corresponding subband from the two sub-ladder are the same. However, the degenerate states from the two different sub-ladders possess opposite spin projections. Although the degeneracy with respect to the spin degree of freedom between the two sub-ladders of subbands is preserved, within each sub-ladder the valley degeneracy is lifted by the spin-orbit interaction and/or shear strain. In the case when the confinement potential is approximated by an infinite square well, a quite accurate approximation [28] for the energy difference between the two unprimed subbands (the valley splitting) is obtained as

$$\Delta E_{\mathrm{n}} \approx \frac{2y_{\mathrm{n}}^2\delta}{k_0 t\sqrt{\left(1-y_{\mathrm{n}}^2-\eta^2\right)\left(1-y_{\mathrm{n}}^2\right)}} \left|\sin\left(\sqrt{\frac{1-y_{\mathrm{n}}^2-\eta^2}{1-y_{\mathrm{n}}^2}}k_0 t\right)\right|, \tag{31.52}$$

with y_{n} and η, defined as

$$y_{\mathrm{n}} = \frac{\pi n}{k_0 t}, \tag{31.53}$$

$$\eta = \frac{m_{\mathrm{l}} B}{\hbar^2 k_0^2}. \tag{31.54}$$

It follows from (31.52) that within each sub-ladder, the subband minima are two times degenerate in unstrained (001) silicon films. At finite momenta k_{x}, k_{y} the degeneracy is lifted. The splitting within each sub-ladder is determined by the spin-orbit interaction term alone, if the momentum is either along the *[100]* or *[010]* axis. Along these lines the spin-orbit interaction leads to a large mixing between the spin-up and spin-down states along these axes. Because of the large spin mixing, the regions in the momentum space close to these axes determine the spin relaxation and are called spin relaxation hot spots.

If the silicon film is stressed along the *[110]* direction, the shear strain component $\varepsilon_{\mathrm{xy}}$ is nonzero. The spin relaxation hot spots are determined by the condition

$$\left(D\varepsilon_{\mathrm{xy}} - \frac{\hbar^2 k_{\mathrm{x}} k_{\mathrm{y}}}{M}\right) = 0. \tag{31.55}$$

It then follows that the spin relaxation hot spots are moved toward higher energy in strained films as shown in Fig. 31.18. In the case when the hot spots are pushed higher than the Fermi (plus the thermal energy), the spin relaxation is significantly decreased, which must lead to the enhanced spin lifetime.

To compute the spin relaxation time, we consider surface roughness scattering as well as intra- and inter-valley scattering by acoustic [28] and optical phonons [88]. The wave functions are numerically calculated for an infinite square well potential in the basis X_1, X_2, X_3, X_4 and then transformed to the initial basis $[(X_1,\uparrow),(X_1,\downarrow),(X_{2'},\uparrow),(X_{2'},\downarrow)]$ with spin up or down relative to the axis z perpendicular to the silicon film. A proper linear combination of the eigenfunctions is taken [89] in order to obtain the wave functions with spin projections on a given axis.

Figure 31.19a, b show the total spin lifetime and partial contributions due to surface roughness, acoustic, and optical phonons scattering as a function of strain, for two different thicknesses (3 nm and 5 nm). The spin of the injected electrons is oriented along the z axis in *[001]* direction. For the thinner film of 3 nm thickness, the contribution due to electron-phonon scattering with longitudinal acoustic (LA) phonons is similar to the contribution due to surface roughness for small shear strain values. If the strain is increased, the LA phonons introduce the main contribution to the total spin lifetime.

For the thicker film shown in Fig. 31.19b, the role of the surface roughness scattering is reduced, and the total spin lifetime follows the same trends as the spin relaxation due to longitudinal acoustic phonons. The intersubband optical phonons calculated as g-process can be ignored for the film of 3 nm thickness, while their contribution for the thicker film is more pronounced at high strain. As a conclusion, the spin lifetime is significantly increased just by applying shear strain, which is today routinely used to boost the electron mobility in modern MOSFETs.

31.2.5 Perspectives of a Spin Silicon Switch

Silicon, the main element of modern microelectronics, is promising for spin-driven applications. Silicon is composed of nuclei with predominantly zero spin, which reduces the conduction electrons' spin relaxation due to their interactions with the nuclear spins. Silicon is also characterized by a weak strength of spin-orbit coupling, which results in long, approximately 10 ns, spin relaxation time at room temperatures suitable for SpinFET and SpinMOSFET operation. However, in electrically gated laterally confined silicon structures, the spin relaxation is enhanced [90], which could compromise

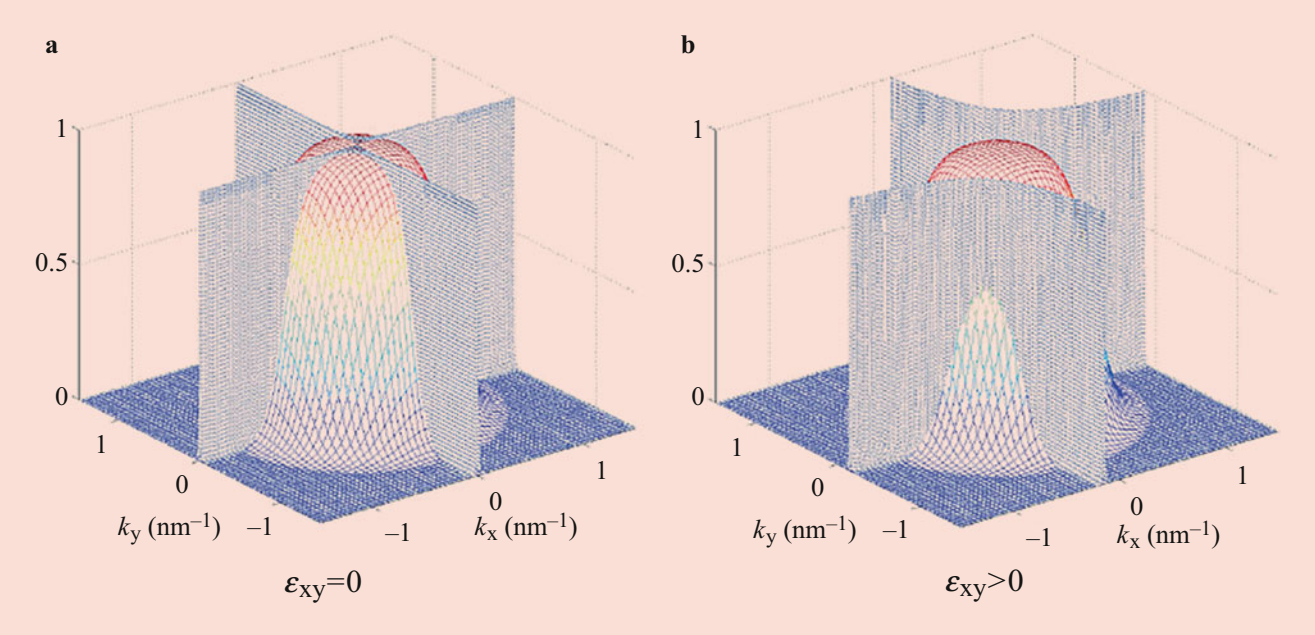

Fig. 31.18 (**a**) Spin relaxation hot spots in an unstrained silicon thin film and in a film stressed tensely along the *[110]* axis. (**b**) In the stressed film, the hot spots are pushed to higher energies toward unoccupied states

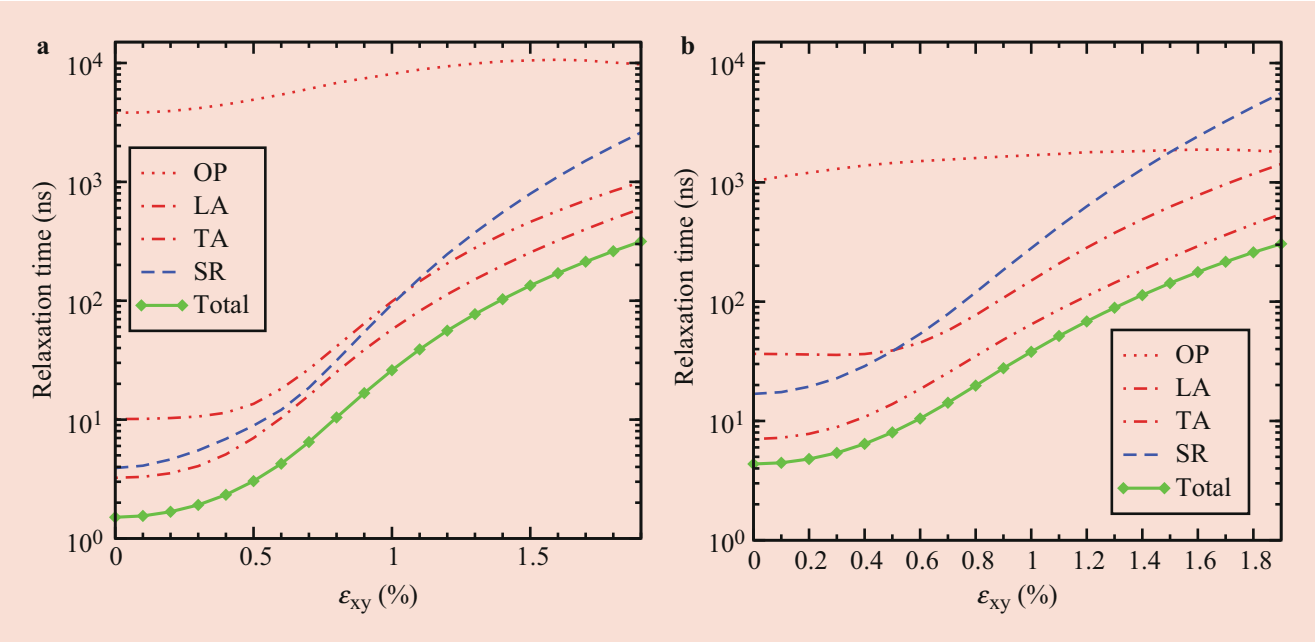

Fig. 31.19 The spin relaxation time in a (001) silicon film with a thickness (**a**) 3 nm and (**b**) 4 nm as a function of shear strain. Surface roughness (SR), longitudinal acoustic (LA), transversal acoustic (TA), and optical (OP) phonon-mediated scattering are considered

the reliability device and become an obstacle in realizing spin-driven devices. We demonstrate that shear strain is efficient to increase the spin lifetime by at least one order of magnitude. Shear strain is routinely used to boost the electron mobility in modern MOSFETs due to the strain-dependent transport effective mass. In contrast to the electron mobility determined by the inter-valley scattering processes, the spin relaxation is controlled by inter-valley scattering. Shear strain lifts the degeneracy between the valleys, which results in a substantial spin lifetime increase.

The increased spin lifetime leads to a longer spin diffusion length in thin silicon films. The inversion symmetry in thin

silicon films can be broken by applying a perpendicular electric field. This results in an electric field-dependent spin-orbit Rashba-like field which can be used to manipulate the electron spins while they propagate through the channel. It is therefore conceivable to perform an experiment at room temperature, which can demonstrate the spin manipulation in silicon, as the spin lifetime and the spin diffusion length can be significantly increased by applying shear strain. However, as the spin-orbit field in silicon is also weak, the channel length required for achieving a proper and useful spin manipulation is about several micrometers. In order to benefit from the gate voltage-induced spin and current manipulation in modern MOSFETS with a channel length of only 20 nm, a conceptually new method to manipulate spins by the gate voltage at such short distances is required.

The first experimental demonstration of a SpinMOSFET [72] confirmed that the electron spins are successfully injected into silicon. The spin diffusion length was a few microns at room temperature sufficient to demonstrate a large absolute difference between the currents in parallel and antiparallel source-drain magnetization configuration. However, the relative ratio of the on-currents, a characteristic similar to the tunneling magnetoresistance ratio, is still several orders of magnitude lower [72] than the tunneling magnetoresistance (TMR) in magnetic tunnel junctions, the main element of the magnetoresistive nonvolatile memory discussed later. In the experimental SpinMOSFET, a magnetoresistance ratio less than 0.1% was reported. In order to make a useful device, the ratio should be increased by at least two orders of magnitude to the level of the tunneling magnetoresistances in magnetic tunnel junctions. Our calculations show that the ratio depends on the source-drain spin polarization which must be increased. Another important ingredient is the tunnel barrier between the ferromagnet and the semiconductor. The defects apparently do not necessarily play a detrimental role. Spin-dependent trap-assisted transport study is in its incipient stage. However, it already reveals new concepts for devices, which, by analogy to a single-electron transistor, employ a single spin for their operation. More material research as well as experimental and theoretical work is needed in order to better understand the influence of the dielectric between the ferromagnet and silicon used to provide the spin injection.

Efficient spin injection is the key to boost the resistance difference between the two states with parallel and antiparallel alignment of the source-drain magnetization. New ideas to obtain a high spin polarization in the channel are urgently needed. One interesting option to boost the spin injection efficiency is to employ an electric field at the contact interface between the ferromagnet and the two-dimensional electron gas to increase spin-to-charge conversion [91]. Although a large MR of 80% was reported on a III-V surface layer at low temperature needed to avoid spin relaxation, the technique of boosting spin-to-charge conversion possesses potential for being also employed in silicon at room temperature.

New two-dimensional materials (graphene, transition metal dichalcogenides) are attractive for emerging microelectronics applications as they allow developing new concepts, in particular for spin switches [92]. Spin-polarized electrons injected into a graphene sheet propagate to the drain and remain spin-polarized as the spin relaxation in graphene is weak. However, if a MoS_2 single layer is introduced on the top of graphene, a parallel path for electrons through MoS_2, the material with strong spin relaxation, is open, and the current reaching the drain is not spin-polarized. As the chemical potential of the MoS_2 layer can be tuned from the conduction band to the gap, this opens the opportunity to have a switch between spin-polarized and spin-unpolarized drain currents depending on the gate voltage.

Although many fundamental problems and technological challenges have been resolved, and a SpinFET and a SpinMOSFET have been successfully demonstrated, both devices still rely on the charge current to transfer the spin, which may set some limitations for the applicability of such devices in mainstream microelectronics. In addition, the absence of an efficient and purely electrical spin injection scheme results in a small difference between the resistances in parallel and antiparallel source-drain configuration. New innovative ideas and physical principles which would allow an efficient spin manipulation by purely electrical means at ambient temperature are urgently needed to extend the functionality of modern MOSFETs by including electron spin. Nonvolatile devices based on magnetic tunnel junctions possess the tunneling magnetoresistance suitable for practical applications, in particular in memory devices discussed below.

31.3 Nonvolatile Magnetoresistive Memories

An attractive path to mitigate the unfavorable trend of increasing power dissipation, especially at a standby mode, is to introduce nonvolatility in the circuits. Nonvolatility is an ability to keep the data even if the supply power is turned off. Introduction of nonvolatility enables standby power-free integrated circuits. Indeed, if no information is lost, there is no need to recollect and recover the data, when the power is turned on. Nonvolatility is crucial for eliminating the leakage power dissipation and data refreshment cycles. Apart from standalone applications, e.g., critical program and data storage devices in extreme environments employed in the airspace industry, it is particularly promising to use nonvolatility in the main computer memory as replacement of conventional volatile CMOS-based dynamic random-access memory (DRAM) [93, 94]. In addition, this memory could be embedded on chip, which removes one of the bottlenecks of

the Von Neumann computing architecture, when memory is physically far away from the central processing unit (CPU). This way a lengthy and energy-consuming procedure of data exchange between the memory and the CPU is omitted.

In modern multicore processors, much of the energy consumption takes place in the hierarchical multilevel cache memory structure. To reduce this energy consumption, a viable approach is to replace the caches with a nonvolatile memory which desirably also offers a reduced memory cell size compared to static random-access memory (SRAM) [93, 94]. In addition, this helps bridging the speed gap between the last level caches serviced by fast CMOS SRAM and much slower main computer memory mastered by CMOS DRAM.

The development of a novel electrically addressable nonvolatile memory is essential to mitigate the increase of the standby power and to introduce instant-on architectures without the need of data initialization when going from a standby to an operation regime. To be competitive with the traditional, volatile memory technologies and also with nonvolatile flash memory, emerging nonvolatile memories must offer a fast switching time, a high integration density supported by good scalability, a long retention time, a high endurance, and a low-power consumption. At the same time, they must possess a simple structure to reduce fabrication costs. An important requirement is that emerging memories must be compatible with CMOS technology to benefit from the advantages provided by the well-developed CMOS fabrication technology.

Applications driven by magnetic moments and induced magnetic fields had a large share in typical information technology products in the past as the coupling between magnetic fields and currents in coils was employed in the first electronic devices. However, the coupling was weak, which resulted in low efficiency and high energy supply costs. An efficient coupling between the electrical and the magnetic degree of freedom is possible on a quantum mechanical level and was discovered in 1986 as a phenomenon called the giant magnetoresistance (GMR) effect. This facilitated a reliable, purely electrical read operation of the information encoded in the magnetization orientation. Based on this principle, hard disk drive storage devices with extremely high density appeared on the market. The tremendous impact of this discovery on the development of information technology was recognized by awarding the inventors the Nobel Prize in 2007 [95, 96].

The next generation of storage devices with even higher density was based on the unique properties of the MTJ. As was already briefly discussed, the tunneling current through the MTJ structure strongly depends on the relative polarization of the ferromagnetic contacts. The difference in the MTJ resistivity can reach several hundred percent at room temperature [97]. Using MTJs as data storage elements yields an efficient way of converting the spin (magnetization) degree of freedom into a charge (current) employed by CMOS devices. It is important that the typical resistance of an MTJ is similar to that of a MOSFET, which makes MTJ-based memory electrically compatible with CMOS circuitry without extra amplifiers needed. Thanks to this technology, a new generation of hard disk drives with even higher storage densities has been developed [98, 99].

In order to be fully compatible with CMOS circuitry, MTJs must be complemented with the ability to efficiently convert charge information into magnetic moment orientation. In earlier field-driven magnetoresistive random-access memories, the information writing was performed with the help of a magnetic field [100, 101]. Although a very fast switching of a specially designed free magnetic layer [102] has been achieved by applying carefully engineered orthogonal current pulses, MRAM with field-induced switching cannot be scaled beyond the 90 nm technology node [103]. Indeed, the magnetic field is generated by the electric current passing through the write lines next to the cell, which leads to an unbearable current density increase with scaling [101]. Therefore, in order to support the scaling, a new purely electrical way of MRAM information writing without magnetic field must be implemented.

Below we briefly discuss the three most prominent emerging concepts of nonvolatile magnetoresistive memories: spin-transfer torque MRAM, spin-orbit torque MRAM, and advanced magnetoresistive memories including racetrack memory.

31.3.1 Spin-Transfer Torque MRAM

The spin-transfer torque effect (STT) [104, 105] has been proven to be perfectly suited for purely electrical data writing by passing a current through the MTJ (Fig. 31.20a). When electrons pass through a fixed ferromagnetic layer, their spins become aligned with the magnetization. When these spin-polarized electrons enter the free magnetic layer, they become aligned with the magnetization of the free layer within a transition layer of a few angstroms. Due to the conservation of the total angular momentum, the change of the electron spin is compensated by the modification of the free layer magnetization. Therefore, the spin-polarized current exerts a torque on the magnetization of the free layer. If the current is sufficiently strong to overcome the damping, this torque causes magnetization switching. If the current tends to switch the magnetization from the parallel to the antiparallel configuration, altering the current direction will result in the magnetization switched from the antiparallel to the parallel state.

STT-MRAM is considered as a perfect candidate for future universal memory applications. STT-MRAM is fast (10 ns), possesses high endurance (10^{12}), and has a simple structure. It is compatible with CMOS technology

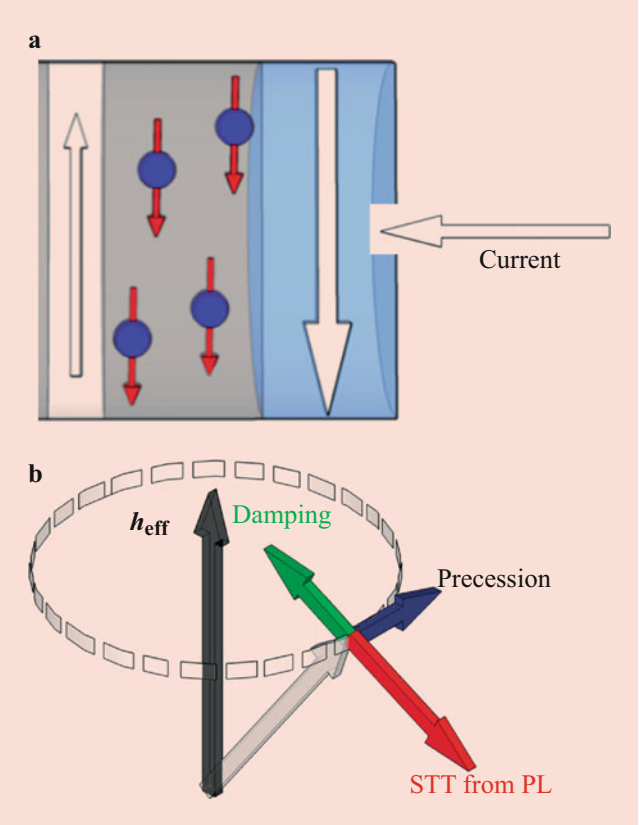

Fig. 31.20 (**a**) Charge current running through a magnetic tunnel junction's pinned layer (PL) creates a spin-transfer torque acting on a free recording magnetic layer. (**b**) torques acting on the magnetization: spin-transfer torque, damping, effective magnetic field torque

and can be straightforwardly embedded in circuits [101]. It is particularly promising to employ nonvolatility in Internet of Things (IoT) and automotive applications, as well as a replacement of conventional volatile CMOS-based DRAM and nonvolatile flash memory. High-density STT-MRAM arrays with 4Gbit capacities have been already demonstrated [106]. For embedded applications, a successful implementation of 8 Mb 1T-1MTJ STT-MRAM on a 28 nm CMOS logic platform [107] was demonstrated. Recently, 128 Mb embedded MRAM with 14 ns write speed was reported [108]. An embedded MRAM solution compatible with 22FFL FinFET Intel's technology is available [109].

With STT-MRAM currently emerging as a commercial product for standalone and embedded applications, it is critically important to introduce STT-MRAM in the main computer memory. This potentially creates a new innovative multibillion dollar industry. Bringing STT-MRAM into the vast computer memory market as standalone and embedded applications for traditional high-performance and low-power mobile platforms will result in an exponential growth of the nonvolatile memory market share in the near future.

Regardless of the first commercial STT-MRAM-based products for standalone applications being available, one critical aspect of the currently used STT-MRAM technology is a relatively high switching current, which is in sharp contrast to the overall demand for reduced energy consumption. This might prevent MRAM from successfully entering the vast computer memory market. The problem of high switching current and large active writing energy jeopardizes the advantages provided by nonvolatility, such as zero standby power, no data refreshment, and no data recovery. At the same time, the minimum energy barrier separating the two stable memory states must be large, at least 60–80 times the thermal energy, to negate the errors due to unwanted thermally agitated magnetization switching in big (1 Gb) memory arrays at long (10 years) retention time. Since the same barrier must be overcome for memory writing, the switching current reduction problem is challenging to address.

Several plausible approaches to address these issues are currently pursued. They include the replacement of the in-plane magnetization orientation in magnetic tunnel junctions (MTJs) with perpendicular magnetization, the use of composite free recording layers, decoupling the write and read current paths, controlling magnetization by voltage, and employing new materials with improved properties and characteristics.

The availability of high-capacity nonvolatile memory close to high-performance CMOS circuits allows exploring conceptually new logic-in-memory [110] and computing-in-memory [111, 112] architectures for future artificial intelligence and cognitive computing [113].

The interest in STT-MRAM has increased significantly after the observation of spin torque-induced switching in AlO_x-based cells [114]. However, the exciting journey of bringing STT-MRAM to the market was ignited by the observation of spin torque-induced switching in MgO-based [115] cells. Depending on the orientation of the layer magnetization, the magnetic pillars can be divided into two categories: (i) perpendicular with out-of-plane magnetization direction and (ii) in-plane with the magnetization lying in the plane of the magnetic layer.

The magnetization dynamics of switching is determined by the Landau-Lifshitz-Gilbert equation [116, 117] complemented by the corresponding torque:

$$\frac{\partial \boldsymbol{m}}{\partial t} = -\gamma\left(\boldsymbol{m} \times \boldsymbol{h}_{\text{eff}}\right) + \boldsymbol{\alpha m} \times \frac{\partial \boldsymbol{m}}{\partial t} - \frac{g\mu_{\text{B}} J}{e\gamma M_{\text{s}} d} \cdot g\left(\theta\right) \left(b\left(\boldsymbol{m} \times \boldsymbol{p}\right) - \left(\boldsymbol{m} \times \left(\boldsymbol{m} \times \boldsymbol{p}\right)\right)\right) \tag{31.56}$$

$\gamma = 2.3245 \cdot 10^5 \text{m/(A·s)}$ is the gyromagnetic ratio, g is the g-factor, α is the Gilbert damping parameter, b is a nonadiabaticity parameter, μ_{B} is Bohr's magneton, J is the current density, e is the electron charge, d is the thickness of the free layer, $\boldsymbol{m} = \mathbf{M}/M_{\text{s}}$ is the position-dependent normalized vector of the magnetization in the free layer, $\boldsymbol{p} = \mathbf{M}_{\text{p}}/M_{\text{sp}}$ is

the normalized magnetization of the first pinned layer, and M_s, M_{sp} are the saturation magnetizations of the free layer and the pinned layer, correspondingly. We use Slonczewski's expressions for the MTJ with a dielectric layer [118]:

$$g(\theta) = 0.5 \cdot p \cdot \left[1 + p^2 \cdot \cos(\theta)\right]^{-1} \tag{31.57}$$

The local effective field is calculated as

$$\boldsymbol{h}_{\text{eff}} = \boldsymbol{h}_{\text{ext}} + \boldsymbol{h}_{\text{ani}} + \boldsymbol{h}_{\text{exch}} + \boldsymbol{h}_{\text{demag}} + \boldsymbol{h}_{\text{th}} + \boldsymbol{h}_{\text{amp}} + \boldsymbol{h}_{\text{ms}} \tag{31.58}$$

$\boldsymbol{h}_{\text{ext}}$ is the external field, $\boldsymbol{h}_{\text{ani}}$ is the magnetic anisotropy field, $\boldsymbol{h}_{\text{exch}}$ is the exchange field, $\boldsymbol{h}_{\text{demag}}$ is the demagnetizing field, $\boldsymbol{h}_{\text{th}}$ is the thermal field, $\boldsymbol{h}_{\text{amp}}$ is the Ampere field, and $\boldsymbol{h}_{\text{ms}}$ is the magnetostatic coupling between the pinned layers and the free layer. Typical values of the parameters characteristic to CoFeB/MgO/CoFeB structure are $M_s = M_{sp} = 8.9{\cdot}10^5$A/m, $A = 1{\cdot}10^{-11}$ J/m, $\alpha = 0.01$, and $p = 0.63$ [119].

Figure 31.20b schematically shows the torques and fields acting on the magnetization during the switching. When the current of the corresponding polarity runs through the structure, it creates the STT which tilts the magnetization away from its equilibrium position. When tilted, the magnetization experiences the effective magnetic field, around which it precesses. The damping term tries to bring the magnetization back to its equilibrium position. The switching occurs, if the STT overcomes the damping term. From this condition the critical current for switching is obtained.

However, the magnetization switching can occur spontaneously due to thermal fluctuations without any current. This is an undesired event, which leads to the loss of the stored information. An important parameter of MRAM is the thermal stability factor which is defined as the ratio of the thermal stability barrier to the operating temperature. For gigabit applications the thermal stability barrier should be at least 80 kT to guarantee the required retention time of 10 years. Achieving large thermal stability and a low switching current for fast switching simultaneously represents one of the main challenges to engineer a good MRAM cell. In in-plane magnetized structures, the shape anisotropy defines the two stable magnetization directions (Fig. 31.21a). In these structures the minimum energy difference separating the two stable magnetization states is determined by the energy difference between the two states with the magnetization in-plane perpendicular and parallel to the easy anisotropy axis. The switching barrier is larger than the thermal barrier defined as the minimum energy barrier separating the two stable magnetization states. This is because at switching the magnetization must get out-of-plane, which results in a large demagnetization energy contribution to be overcome, in addition to the thermal barrier.

For in-plane MTJs, faster switching can also be achieved, when the composite free layer is made of two half-ellipses separated by a narrow gap (Fig. 31.21b). The peculiarities of the magnetization dynamics of the two parts of the composite free layer [111, 120], which occur in opposite senses to each other, lead to the magnetization switching in-plane (Fig. This way the large demagnetization31.21c). This way the large demagnetization penalty of the magnetization getting out-of-plane is avoided, and the switching barrier becomes equal to the thermal barrier. Because the thermal barrier depends on the free layer volume, the required large thermal stability factor of ~80 kT is easily achieved in this structure.

For the perpendicular structures (Fig. 31.22a), the magnetization orientation is already out-of-plane. The large demagnetizing energy penalty one has to pay while writing an in-plane structure does not exist for switching perpendicular structures. Perpendicular MTJs (p-MTJs) with the thermal barrier equal to the switching barrier are thus preferred, because they allow to reduce the switching current. In addition, p-MTJs are better suited for high-density memory [110]. However, it is difficult to find a material with the uniaxial anisotropy so strong that it can overcome the demagnetization field of a thin ferromagnetic layer. A critical technological step allowing to solve this problem was the discovery of an interface-induced perpendicular anisotropy at the CoFeB/MgO interface [121], which makes the very thin CoFeB layer perpendicularly magnetized (Fig. 31.22a).

Both field-induced and STT switching can be complemented with heat-assisted switching [101]. This technology was routinely used in hard disk drives in order to facilitate writing. Methods using thermally assisted switching in MRAM have already been developed. In addition to assisting switching, heat can facilitate new unique functionalities, for instance, using an MRAM cell with a soft reference layer as a magnetic logic unit [122]. This extends the MRAM research and development area toward logic-in-memory architectures and nonvolatile computing.

Regardless of the undeniable success of the first MRAM products appearing on the market, several important challenges still remain. The general requirements for any memory type including MRAM are the ability to write the data with low energy without damaging the device, long data retention, and the ability to read the recorded data without destroying them.

Improving one or two aspects of its functionality usually leads to a degradation of the remaining functionalities [101] in STT-MRAM. Therefore, a careful parameter optimization specific to a particular technology is the main subject which must be addressed in order to facilitate production of high-density memory arrays suitable for replacing SRAM caches and DRAM main computer memory.

As was mentioned already, one of the main problems of STT-MRAM is the relatively high critical current required for

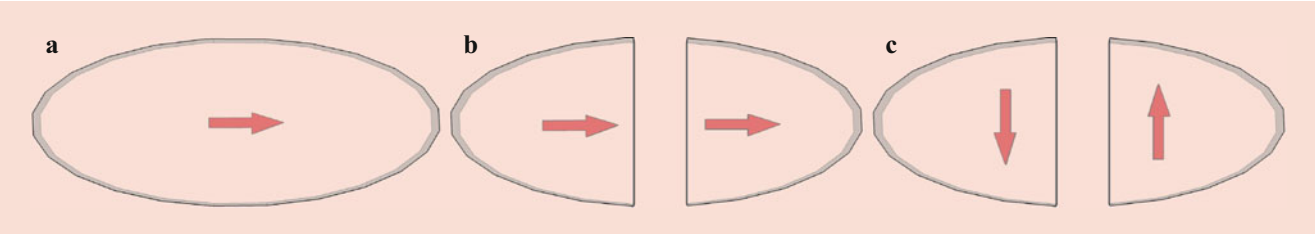

Fig. 31.21 (**a**) Shape anisotropy defined magnetization direction in an elliptic free magnetic layer; (**b**) Stable magnetization direction in a composite free magnetic layer with a narrow splitting between the two parts; (**c**) The magnetic configuration with a maximum energy through which the composite free layer proceeds at STT switching. The composite free magnetic layer switches in-plane, which results in a lower switching barrier and faster switching [111, 120]

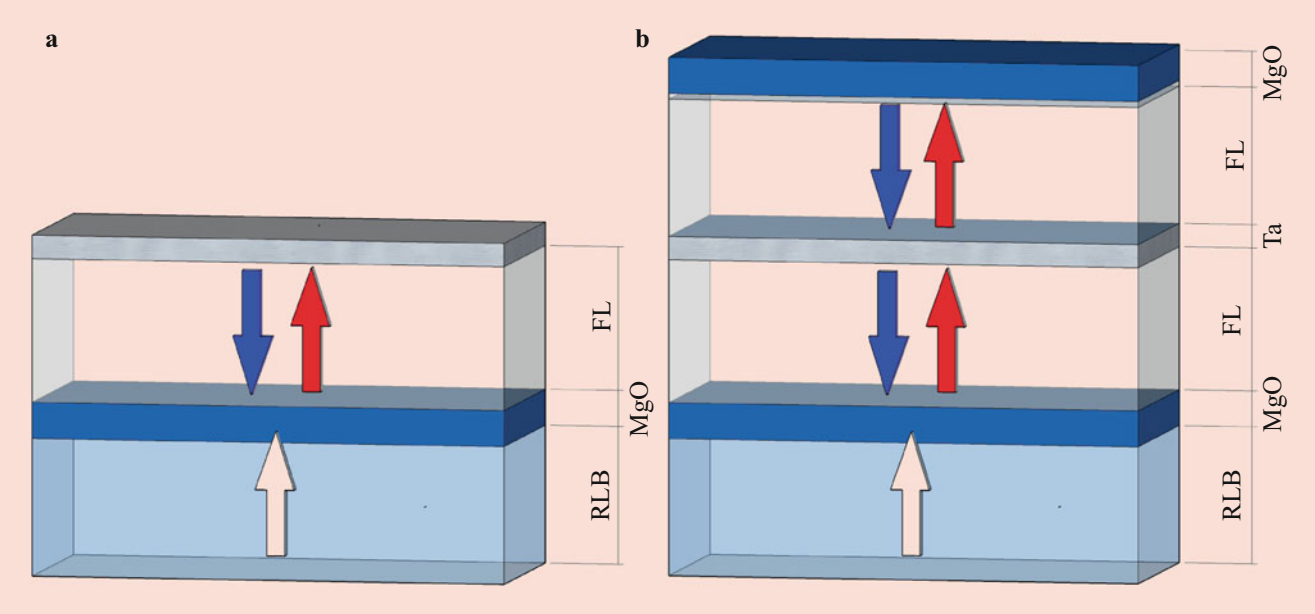

Fig. 31.22 (**a**) Illustration of a perpendicularly magnetized MTJ. The perpendicular uniaxial anisotropy is interface-induced [118]. (**b**) The thermal stability is enhanced by adding a second CoFeB/MgO interface with interface-induced anisotropy [123]. The Gilbert damping is also reduced for the composite free layer made of two thin ferromagnetic CoFeB layers separated by a Ta metallic spacer [123]

STT-induced magnetization switching. This fact has several implications. Firstly, due to the relatively high energy required for writing, memory should not be written frequently as it may negate the benefits of nonvolatility provided by MRAM. Secondly, large switching currents are supplied via an access transistor. This potentially puts scaling limitations on the transistor dimensions of a one-transistor (1T)-1MTJ memory cell.

In order to reduce the switching current density and to preserve the large thermal barrier at the same time, one has to reduce the Gilbert damping and increase the spin current polarization. An interface-induced p-MTJ structure with a composite free layer CoFeB/Ta/CoFeB with two MgO interfaces [123] (Fig. 31.22b) allows boosting the thermal barriers. It turns out that the use of the p-MTJ structure with the two CoFeB/MgO interfaces also reduces the Gilbert damping by half, thus allowing to simultaneously boost the thermal barriers and to reduce the switching current. To scale the diameter of the MTJ beyond 10 nm, the use of shape anisotropy was suggested [124]. It has been shown that the thermal stability can be boosted for small diameters without sacrificing on TMR and without any need of new materials, as FeB for the ferromagnetic free layer and MgO for the tunnel barrier were used.

In order to integrate STT-MRAM with the CMOS fabrication process, MTJs must sustain 400 C temperature typical for the back-end-of-line process. Recently, IMEC reported a process allowing to preserve the high TMR and thermal stability of MTJs [125]. The idea is to invert the free and the fixed layer by putting the fixed layer on top of the MTJ. An additional synthetic ferromagnet instead of an antiferromagnet is employed to pin the magnetization of the fixed layer. This design requires a compensating magnet to be in addition integrated in the structure. Optimization of this magnet can

be used to achieve symmetric switching between the parallel and the antiparallel configuration and back.

A large TMR ratio is needed for reliably reading the information in MRAM. Indeed, the middle reference resistance to which the low and high resistance MTJ states are compared must be well separated from either of them. However, with downscaling it becomes increasingly difficult to control the bit-to-bit resistance variation which results in sacrificing the read margin. As the resistance variation dispersion increases, the TMR must also increase to provide a sufficiently broad window for reliable reading. Obtaining a TMR larger than 350% [126] is an important challenge needed to continue with the devices scaling down.

With growing data services such as Big Data analysis, the need for additional memory capacity and speed as well as in-memory computing has increased dramatically. The last-level cache memory must be increased [127–129] to bridge the memory-bandwidth gap between CPUs and the main memory. The CPU performance can be significantly boosted by using fast nonvolatile memories in cache for data storing without the need to address the main memory.

Advanced STT-MRAM is characterized by high-speed access with 10 ns. It is thus in principle suitable for last-level caches where it guarantees power reduction by a factor of ten [130–132], while other types of nonvolatile memories are much slower and cannot provide the desired high-speed access. Various major foundries including Samsung [133] announce the beginning of production of embedded STT-MRAM based on the 28 nm silicon-on-insulator technology node [134], while GlobalFoundries is planning STT-MRAM production based on the 22 nm fully depleted silicon-on-insulator technology [132]. We are therefore witnessing the beginning of nonvolatile STT-MRAM entering the DRAM and potentially SRAM markets, traditionally dominated by CMOS-based volatile devices. If successful, it will result in an exponential expansion of the STT-MRAM market with a momentous impact on information storage and processing in the near future.

Although the use of STT-MRAM in last-level caches is conceivable [131], the switching current for operating in high-level caches at sub-nanosecond speed is growing rapidly. Increasing critical currents result in large current densities flowing through the magnetic tunnel junctions. This leads to oxide reliability issues, which in turn reduces the MRAM endurance to that of the flash memory. A new technological solution is thus required to use MRAM in L1 and L2 caches.

31.3.2 Spin-Orbit Torque MRAM

The engineering of an electrically addressable nonvolatile memory combining high speed (sub-ns operation) and high endurance suitable for replacing SRAM in higher-level caches of hierarchical multilevel processor memory structures with a nonvolatile memory [110] cannot be based on STT, and the use of new physical principles is required. Among the newly discovered physical phenomena suitable for next-generation MRAM is spin-orbit torque (SOT)-assisted switching at room temperature in heavy metal/ferromagnetic [135–142] or topological insulator/ferromagnetic [143–146] bilayers. In this memory cell, the MTJ's free layer is grown on a material with a large spin Hall angle. The SOT acting on the adjacent magnetic layer is generated by passing the current through this material. The relatively large switching current is injected in-plane along the heavy metal/ferromagnetic bilayer and does not flow through the MTJ, while a much smaller read current is applied through the MTJ. This results in a three-terminal configuration where the read and write current paths are decoupled. Since the large write current does not flow through the oxide in the MTJ, this prevents the tunnel barrier from damage. It improves device reliability by eliminating correlations between the switching current and the retention time. Therefore, three-terminal MRAM cells are promising candidates for future generations of nonvolatile memory for fast sub-ns switching [141]. SOT-MRAM is an electrically addressable nonvolatile memory combining high speed and high endurance and is thus particularly suitable for applications in caches [141]. Although the high switching current is not flowing through a magnetic tunnel junction but rather through a heavy metal wire under it, the current is still high, and its reduction is the pressing issue for SOT-MRAM development.

Topological insulators (TIs) are promising materials for reducing the switching current as they are characterized by a high spin Hall angle and large efficiency Θ_{SH} of charge to spin conversion due to the peculiar perpendicular spin-momentum locking in the interface states [143, 144]. In addition, the strong spin-orbit interfacial Rashba field helps in generating the required spin density in TIs in order to boost the charge to spin conversion efficiency above 100%.

Although a high charge to spin conversion efficiency in TIs has been reported, the electrical conductivity of TIs needed for practical applications to build a high-density, ultra-low power, and ultra-fast nonvolatile memory is not sufficiently high because of the insulating bulk. Recent developments introduce BiSe- [145] and BiSb [146]-based TIs as suitable candidates for emerging SOT-MRAM as they possess a charge to spin conversion efficiency of 18.8 and 52, respectively. This allows to reduce the switching current by two orders of magnitude as compared to W-based SOT-MRAM. In addition, BiSb samples [146] possess very high electrical conductivity making thin BiSb films leading candidates for emerging fast and low-power SOT-MRAM, and the process integration of BiSb into a MTJ stack is currently under scrutiny [146].

The proper integration of the SOT-MRAM fabrication steps with the CMOS process represents a significant challenge as the memory cells must withhold at least the back-end-of-line thermal budget. As IMEC presented recently a technology to integrate a perpendicular beta-phase W/CoFeB/MgO/CoFeB/synthetic antiferromagnetic stack for a SOT-MRAM on a 300 mm CMOS wafer by only CMOS compatible processes [147], there is a cautious confidence that fast low-power nonvolatile magnetoresistive memory suitable for processor caches will be available soon.

Despite the undisputable progress in developing SOT-MRAM, there is one important issue which has not been convincingly resolved so far, namely, a static magnetic field is still required to guarantee deterministic switching [148, 149] or a perpendicularly magnetized free layer. Several paths to achieve the deterministic switching without magnetic fields were suggested. They require solutions to break the mirror symmetry either by means of the shape of the dielectric [150] or the free layer [151] or by controlling the crystal symmetry of the metal line at the microscopic layer [152]. Biasing the free layer by employing an exchange coupling to an antiferromagnet [153–155] and the use of a peculiar tapered sample shape, which controls the switching [156], were recently reported. However, even if in most of these studies field-free switching was reported, these methods either require a local intrusion into the fabrication process or are based on solutions (antiferromagnets, shapes), which complicate large-scale integration of the fabricated memory cells.

To achieve magnetic field-free switching, a scheme based on two sub-nanosecond orthogonal current pulses is promising [111]. This scheme is suitable for integration in a cross-bar architecture. Applied to in-plane structures, the switching scheme has been shown to accelerate the switching of the in-plane structure by a factor of three.

The two-pulse switching scheme can be applied to a free magnetic layer with perpendicular magnetization [157]. Results of simulations described below show that deterministic, fast, and external magnetic field-free switching of the perpendicularly magnetized layers is achieved.

The SOT switching scheme based on the use of two consecutive orthogonal sub-nanosecond current pulses is sketched in Fig. 31.23. The first pulse is applied to the heavy metal line NM1 with a large spin Hall angle. It results in a large spin current in the out-of-plane direction, which impinges the ferromagnetic layer. The spin current creates the SOT acting on the magnetization. The SOT brings the magnetization in-plane in the direction perpendicular to the current direction in MN1. It implies that the current density in the first current pulse is larger than the critical current density [141]. The second consecutive current pulse is applied through the wire NM2 also possessing a large spin Hall angle.

The free layer of dimension $a \times b \times d = 52.5 \times 12.5 \times 2\ \mathrm{nm}^3$ overlaps fully with the heavy metal line NM1 of 3 nm thickness, with the effective Hall angle Θ_{SH} describing the efficiency of the charge-to-spin conversion. Another heavy metal wire NM2 possesses an overlap from the right side lesser than the total free layer width. The magnetization dynamics of the system due to the spin current densities and the spin accumulations is well described by the Landau-Lifshitz-Gilbert equation (31.59):

$$\begin{aligned}\frac{\partial \boldsymbol{m}}{\partial t} &= -\gamma \boldsymbol{m} \times \boldsymbol{h}_{\mathrm{eff}} + \boldsymbol{\alpha} \boldsymbol{m} \times \frac{\partial \boldsymbol{m}}{\partial t} + \\ &+ \gamma \frac{\hbar}{2e} \frac{\Theta_{\mathrm{SH}} J_1}{\mathbf{M}_{\mathrm{S}} d} \left[\boldsymbol{m} \times (\boldsymbol{m} \times \boldsymbol{y})\right] \Theta(t) \Theta\left(t_1 - t\right) - \\ &- \gamma \frac{\hbar}{2e} \frac{\Theta_{\mathrm{SH}} J_2}{M_{\mathrm{S}} d} \left[\boldsymbol{m} \times (\boldsymbol{m} \times \boldsymbol{x})\right] \\ &\Theta\left(t - t_1 - \tau\right) \Theta\left(t_2 + t_1 + \tau - t\right)\end{aligned} \tag{31.59}$$

where $\boldsymbol{m}$ is the position-dependent magnetization $\mathbf{M}$ normalized by the saturation magnetization M_{S}, $\boldsymbol{m} = \mathbf{M}/M_{\mathrm{S}}$, γ is the gyromagnetic ratio, α is the Gilbert damping parameter, e is the electron charge, $\hbar$ is the reduced Plank constant, Θ_{SH} is an effective Hall angle relating the strength of the spin current density to the charge current density J_i ($i = 1,2$) passing through NM1 and NM2, $t_{1,(2)}$ is the duration of the first (second) pulse, and τ is a time delay between the pulses. The spin-orbit torques due to the charge currents through NM1 and NM2 represented by the third and fourth terms on the right hand side of (31.59) are acting on the free layer at the places of the overlaps of the FL with NM1 and NM2 (Fig. 31.23).

We use the parameters (listed in Table 31.1) typical for the perpendicular CoFeB free layer on a MgO tunnel barrier. The thermal stability factor is around 40. Although this thermal stability is not sufficient for standalone applications, this memory cell is suitable for applications in high-level caches, where the requirements for TMR and the stability are relaxed in favor of fast operation.

Table 31.1 Parameters used in the simulations

Name	Value
Saturation magnetization M_{S}	4×10^5 A/m
Exchange constant A	2×10^{-11} J/m
Perpendicular anisotropy K	2×10^5 J/m^3
Gilbert damping α	0.05
Spin Hall angle Θ_{SH}	0.3
Free layer dimensions	$52.5 \times 12.5 \times 2$ nm^3$25 \times 25 \times 2$ nm^3
NM1: $w_1 \times l$	12.5 nm × 3 nm
NM2: $w_2 \times l$	5–52.5 nm × 3 nm

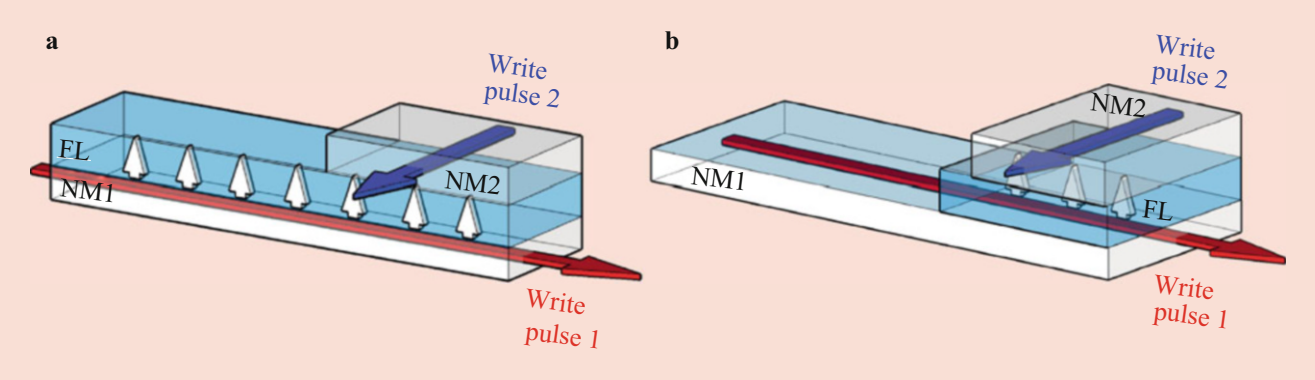

Fig. 31.23 The switching scheme [111] based on two short consecutive orthogonal current pulses provides fast, deterministic, and magnetic field-free magnetization reversal of a perpendicularly magnetized free layer of (**a**) a rectangular shape and (**b**) a symmetric square shape

To realize the switching scheme, a 100 ps short and 100 μA strong current pulse is applied through NM1. The current density equals 2.6×10^{12} A/m^2, which is slightly larger than the critical current density 2×10^{12}A/m^2 reported in [148]. The consecutive perpendicular current pulse is applied through NM2. Thermal effects at 300 K on the magnetization dynamics are described by a fluctuating magnetic field. Different realizations of the field produce diverse realizations of the switching process. Importantly, no external magnetic field is applied.

The time-dependent magnetization dynamics for 20 realizations is shown in Fig. 31.24, where the current density of "Write pulse 2" with 200 ps duration is larger than the critical current applied to NM2 with the width 52.5 nm (equal to the free layer width, complete overlap). Although the current is high (1 mA), it does not provide deterministic switching. It orients the magnetization in-plane against the **x** axis, but there is no torque along the **z** axis. Therefore, after the current is turned off, the magnetization randomly relaxes either in the same or in the opposite direction with equal probability because of the perpendicular magnetic anisotropy.

Unexpectedly, when the current is reduced to 200 μA and the current density to 1.25×10^{12} A/m^2, which is below its critical value, the switching becomes deterministic for all 20 realizations (Fig. 31.25). In this case, the torque due to "Write pulse 2" is not sufficiently strong to align the magnetization along **x** direction, and it only tilts the magnetization away from the **y** direction. In this case, the switching becomes deterministic as the tilted magnetization precesses about the shape effective anisotropy field along the **x** direction, which plays the role of the external field required for making the switching of perpendicular structures deterministic [148]. The polarity of the second pulse therefore defines whether the magnetization relaxes up or down relative to the **z** axis.

If now the current in the second pulse is further decreased to $I_2 = 100$ μA, the switching is robust only, if the second pulse is either short (50–70 ps) or long (>1 ns) (Fig. 31.26).

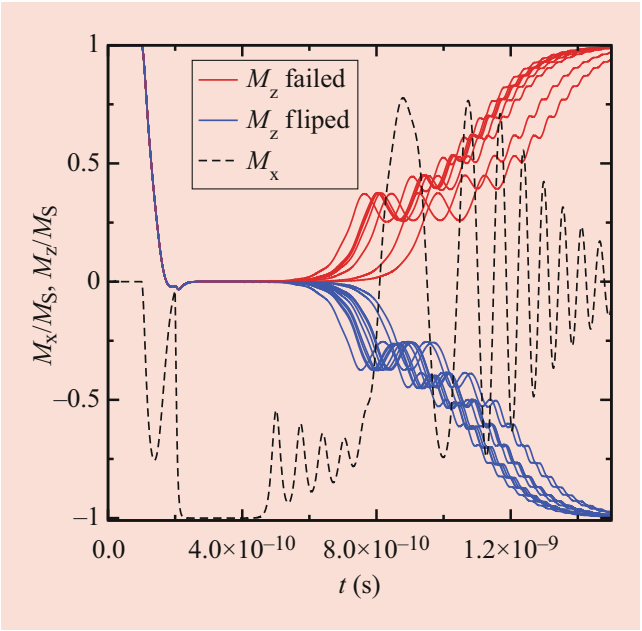

Fig. 31.24 Time evolution of the magnetization in two-pulse switching (second pulse 1 mA/200 ps). Twenty different switching realizations are obtained after 100 ps initial thermalization

The switching becomes fully deterministic for intermediate pulse durations, if the overlap of NM2 with the free layer is reduced to approximately 30%, for the current $I_2 = 100$ μA (Fig. 31.27). As is seen from Fig. 31.27, the "Write pulse 1" puts the magnetization of the free layer in-plane perpendicular to the "Write pulse 1" direction (Fig. 31.27). Depending on the "Write pulse 2" polarity, the corresponding SOT slightly tilts the magnetization in-plane toward the left or right end of the rectangle. Then the magnetization experiences the shape anisotropy field which plays the role of the external field to complete the switching 100% reliably. Figure 31.28 shows that the switching is extremely robust

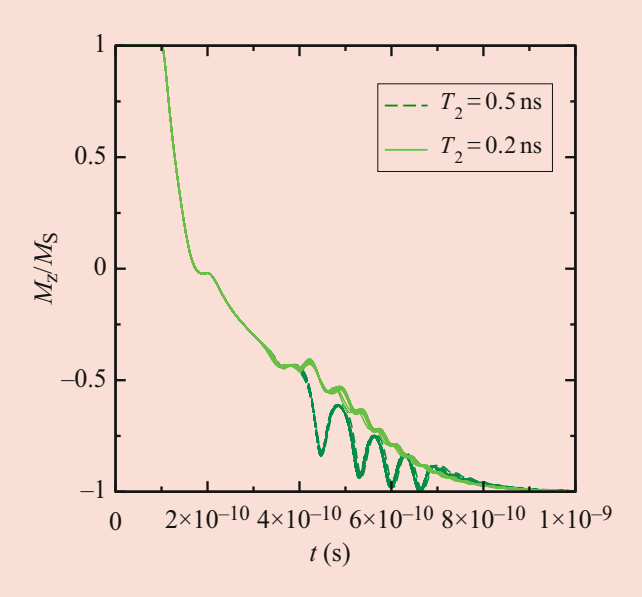

Fig. 31.25 Same as in Fig. 31.24, but with a second pulse current of 200 μA, for two different durations of the second pulse. The 20 realizations switch evenly, almost without dispersion. The switching is deterministic

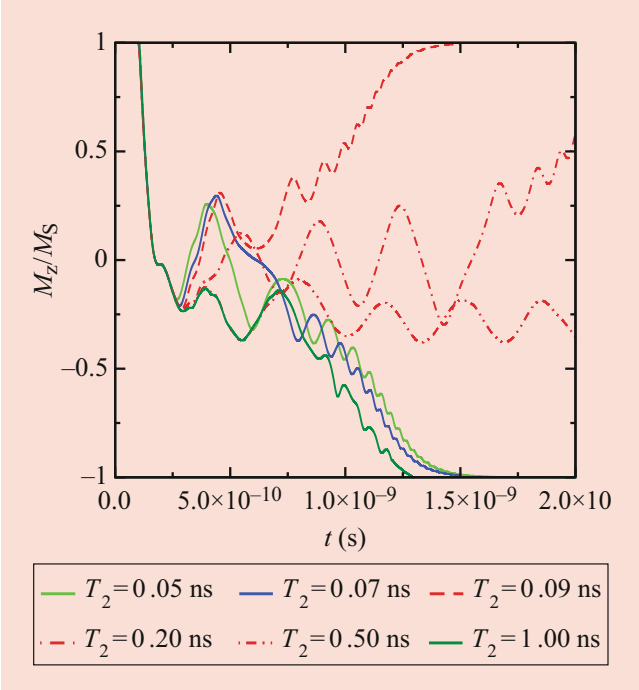

Fig. 31.26 $m_z(t)$ for NM2 fully overlapping with the FL averaged for 20 realizations. $I_1 = I_2 = 100$ μA. For 70 ps $< T_2 <$ 1 ns the switching fails (shown in *red*)

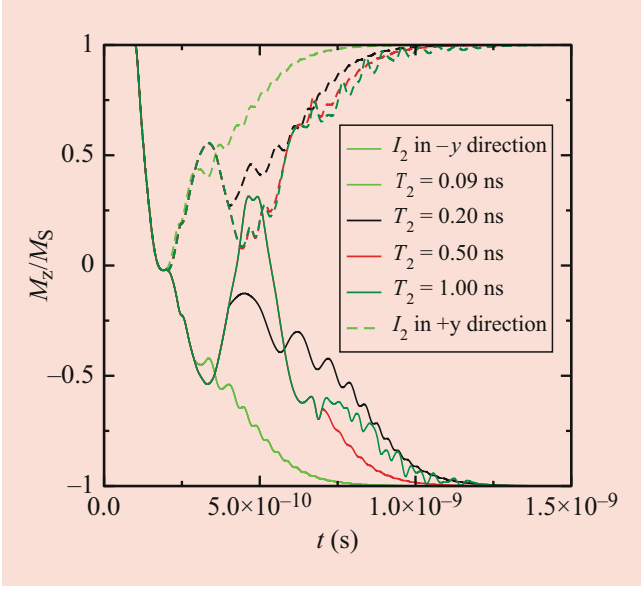

Fig. 31.27 Average of 20 realizations of $m_z(t)$, with $m_z(0) = 1$ for NM2 = 12.5 nm, $I_1 = I_2 = 100$ μA, several T_2, and $\tau = 0$

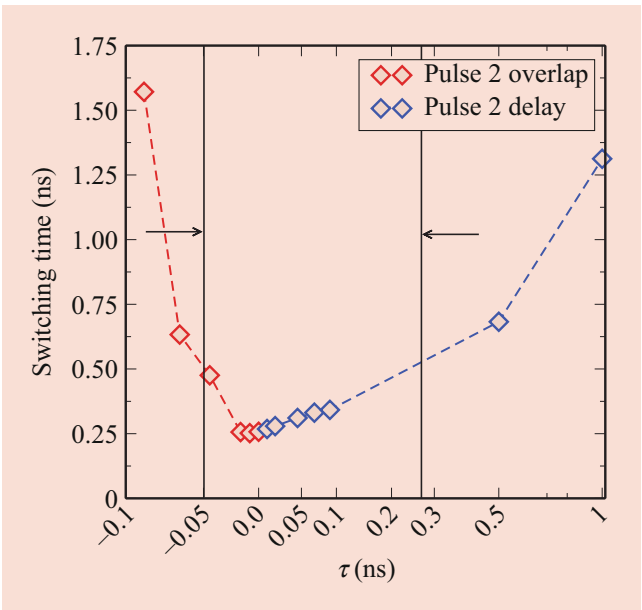

Fig. 31.28 Robust switching at pulse delays between −90 ps $< \tau <$ 1 ns (defined in (31.59)), for $w_1 = w_2 = 12.5$ nm and equal write pulses ($I_1 = I_2 = 100$ μA, $T_1 = T_2 = 100$ ps). Sub-0.5 ns switching is obtained at −50 ps $< \tau <$ 250 ps

with respect to the delay τ, which proves the scheme suitable for practical implementation.

We have demonstrated that the two-pulse switching scheme works for a rectangular sample. However, although footprint size requirements are relaxed in SRAM memory, to grow non-symmetric free layers for benefitting from the extra magnetic shape anisotropy appears superficial as it requires more space and complicates the etching. It is therefore desirable to develop a method for switching a symmetric free layer with perpendicular magnetic anisotropy. Below we demonstrate that the two-pulse SOT switching scheme also

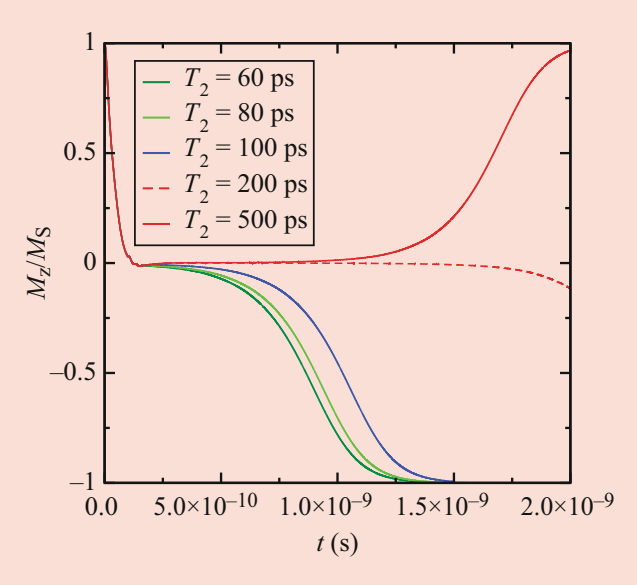

Fig. 31.29 Average of 20 switching realizations. For a partial overlap $w_2 = 17.5$ nm, reliable switching of a square FL at short T_2 pulses appears

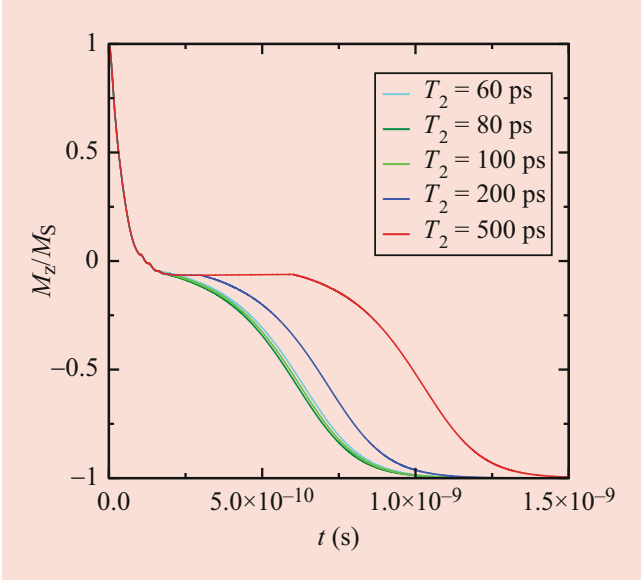

Fig. 31.30 Average of 20 switching realizations for $w_2 = 10$ nm. Reliable switching is observed for all T_2

works for a free layer with the dimensions $25 \times 25 \times 2$ nm^3 of a square form. Again, the free layer overlaps fully with NM1 of $l = 3$ nm thickness. The first pulse of a fixed duration $t_1 = 100$ps and fixed current $I_1 = 200$ μA is applied through NM1. Another heavy metal wire (NM2) of $l = 3$ nm overlaps partly with the FL, $w_2 < a$ and serves to apply the second consecutive perpendicular current pulse $I_2 = (w_2/a)200$ μA of the same current density as in "Write pulse 1," with a variable duration t_2.

If the NM2 overlap with the free layer is reduced to $w_2 = 17.5$ nm, deterministic switching is observed for all 20 realizations, when the duration T_2 of "Write pulse 2" becomes shorter than 200 ps (Fig. 31.29). If the overlap w_2 is further reduced below 15 nm, the switching becomes deterministic for all pulse durations T_2 considered (Fig. 31.30). The magnetization snapshot in Fig. 31.31 demonstrates the position-dependent magnetization just after the "Write pulse 2" was turned on. The magnetization under NM2 rotates due to the SOT of the second pulse. The stray field of the magnetization rotated by the pulse through NM2 creates an effective in-plane magnetic field for the rest of FL. This field makes the magnetization to precess around it away from its in-plane orientation. The whole magnetization of the free layer precesses in the same sense after "Write pulse 2" is turned off. Fig. 31.32 proves the main result of the work that the switching scheme is robust not only with respect to $t_2 = 80 \pm 20$ ps fluctuation but also to fluctuations of $w_2 = 11 \pm 4$ nm as almost the same fast switching time is obtained.

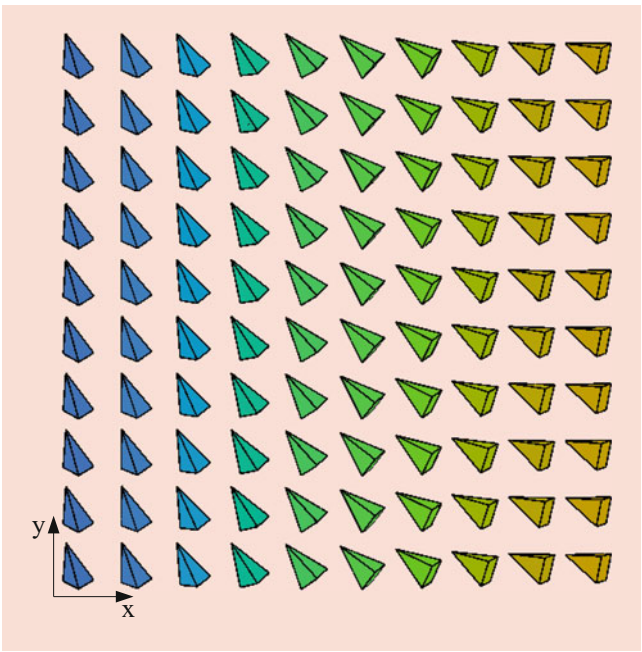

Fig. 31.31 Magnetization in the free layer just after the second pulse is turned off. The magnetization in the left part of the free layer starts precessing about the stray magnetic field created by the right part. This stray field plays the role of the external magnetic field required for deterministic switching of a perpendicular free layer by SOT

We conclude that the two-pulse SOT switching scheme allows fast, robust, and the external field-free switching of a free layer with perpendicular magnetization of arbitrary shape. The spin-orbit torque due to the first pulse tilts the magnetization of the free layer in-plane perpendicular to the "Write pulse 1" direction. In a rectangular sample, the spin-

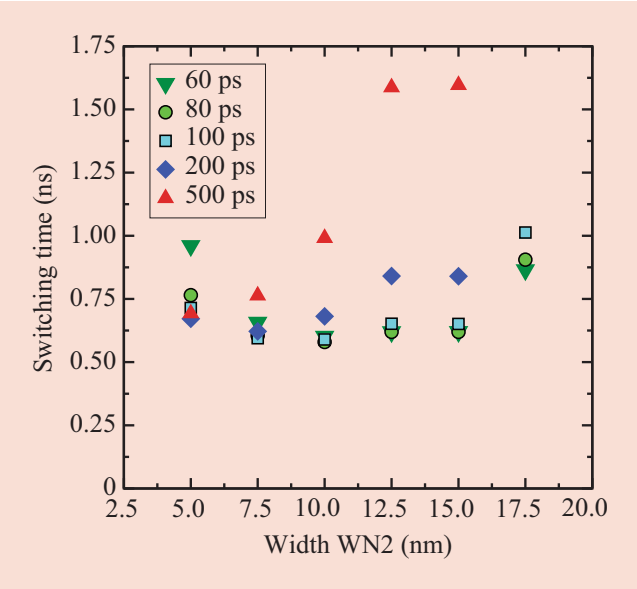

Fig. 31.32 The switching time as a function of the NM2 width. The NM2 width of 12.5 nm is optimal as it guarantees fast, robust, and deterministic switching which is insensitive to small variations of the pulse duration or NM2 width

orbit torque of the second consecutive current "Write pulse 2" pushes the magnetization toward one of the ends of the sample. Then the magnetization starts precessing around the shape anisotropy field. The shape anisotropy field plays the role of the external in-plane magnetic field needed to make the SOT switching of a perpendicularly magnetized free layer deterministic.

If the overlap of NM2 with the rectangular free layer is not complete, the magnetization in the part which overlaps with NM2 is tilted in-plane faster than the rest of the free layer. An additional stray magnetic field due to the faster moving magnetization acts on the rest of the free layer in complement to the shape anisotropy field. The stray magnetic field due to the magnetization of the free layer part overlapping with NM2 is sufficient to make the switching deterministic in a symmetric free layer of a square form. Therefore, the suggested two-pulse SOT switching scheme yields fast and reliable magnetic field-free switching of a symmetric perpendicular free layer, which is suitable for large-scale integration.

31.3.3 Advanced MRAM Developments

The two types of emerging magnetoresistive memory, STT-MRAM and SOT-MRAM, rely on writing the information by means of overcoming the energy barrier between the two memory states with a torque. If the energy barrier is suppressed, for example, by applying a voltage to the structure, the magnetization, which precesses around an effective magnetic field, can be put into the alternative magnetization state, if a barrier is re-introduced at the end of the voltage pulse [158]. An MRAM controlled by voltage [159–162] is a viable option for last-level cache applications.

Because the voltage-induced switching is unipolar, the voltage-controlled MRAM is free from the read disturbance which is characteristic of STT-MRAM. A voltage-controlled MRAM cell is a two-terminal device, where the separation between read and write is performed by alternating the polarities during these two operations.

Voltage-controlled MRAM has a few issues preventing it from being broadly used in applications. One of the problems originates in an undesirable variability due to the thermal noise. As the final state after the switching depends on the initial state after the barrier lowering, the thermally induced magnetization fluctuations can result in write errors.

Another problem is related to data reading. As no current is required to switch the magnetization, the tunnel barrier separating the two ferromagnets in a voltage-controlled memory cell is typically larger than the barrier in an STT-MRAM cell. This leads to a larger resistance of the voltage-controlled memory cell, which results in smaller currents. Small currents lead to a longer delay while reading the state by a sense amplifier. Both problems can be solved [162] by carefully tailoring and optimizing the entire circuit. Extending the ideas of voltage-controlled magnetic anisotropy, the voltage pulse can be applied not only to lower the potential barrier between the two magnetization states. For an opposite voltage polarity, the switching barrier is increased, which additionally prevents the switching while reading [163].

A device operating by using both voltage-controlled magnetic anisotropy and SOT switching was suggested in [164]. The switching is mediated by a spin-orbit and/or spin Hall torque generated by the current flowing through a conductive line made of a heavy metal underneath the MTJ, after the perpendicular magnetic anisotropy is weakened by a voltage applied. For reading a voltage pulse with a polarity opposite to that used for writing is applied to rise the potential barrier, which hardens the cell immunity against read disturb errors.

A conceptually new voltage-controlled magnetic memory device exploring unconventional properties of a heterostructure is composed of a topological insulator and a magnetic insulator [165]. The magnetization is reoriented by means of an electric field which creates the current only through the surface states in the topological insulator interfacing the magnetic insulator. The spin accumulation at the interface with the magnetic insulator is then created by means of the spin Hall effect. The spin accumulation provides a torque acting on the magnetization of the magnetic insulator, which ensures the magnetization switching [166].

From emerging device concepts based on innovative physical principles, antiferromagnetic spintronics [167] possesses numerous potential opportunities for the future of spintronic

applications. Antiferromagnetic materials do not generate any stray field. They are extremely robust against magnetic field perturbations. Importantly for applications, antiferromagnets are characterized by ultrafast dynamics and may be suitable for cache applications. As the antiferromagnetic order parameter can also be inverted by spin-orbit torques [168], memory concepts similar to STT-MRAM were suggested. However, as an antiferromagnet does not possess a net magnetization, the anisotropic magnetoresistance effect [168] is employed in order to read the information. As the anisotropic magnetoresistance of an antiferromagnet at room temperature is still weaker compared to the tunneling magnetoresistance in a magnetic tunnel junction, to benefit from both fast antiferromagnetic dynamics and large TMR, the use of partly compensated antiferromagnets with a nonzero net magnetization is promising [169].

31.3.4 Racetrack Memory

Modern spintronic devices undoubtedly play an increasing role in future microelectronics. Spintronics-based solid-state magnetoresistive memories STT-MRAM and SOT-MRAM discussed in details up to now possess no moving parts to record or to read the information, in contrast to magnetic hard disk drives with magnetic recording and read heads [170]. Magnetic racetrack memory [171–173] combines the two concepts of solid state-memory and hard disk drive-based memory with moving heads. Magnetic data encoded in a series of magnetic domain walls in a magnetic nanowire is shifted back and forth along the nanowire: the magnetic racetracks. Like in a hard disk drive, the information is recorded and read by magnetic heads [172]. As many domain walls can be created on a single racetrack, the memory offers an extremely high-density capacity. In addition, each racetrack can be arranged on U-shaped wires standing vertically over a grid of read/write heads. The memory is promising to store a large amount of data comparable to that on a hard disk drive, but allowing a much better performance at significantly less power.

The important property of racetrack memory is that magnetic domain walls are shifted together synchronously in the same direction when the electric current is run through the racetrack. Domain walls are moved by means of spin-transfer torque generated by a spin-polarized current acting on the nonuniform magnetization within the walls. In the initial demonstration of the first generation of racetrack memory [174], the maximum velocity of the domain walls was about 100 m/s and was limited by the current density when unwanted heating of the nanowire was detected.

In order to increase the storage density on a racetrack, the domain walls must be made more compact. Nanowires composed of magnetic ultra-thin Co and Ni multilayers develop a perpendicular magnetic anisotropy, which allows to reduce the domain walls' dimensions to just a few nanometers. As the domain walls were moved by the spin-transfer torque acting on the volume of domain walls, their velocities in the second generation of racetrack memory were similar to those in the first generation. Thin films of CoFeB on MgO can be used to build perpendicular magnetic anisotropy domain wall racetrack memory [175]. It was demonstrated that its cell area can be reduced down to $\sim$2–3 F^2/bit to achieve Gb storage/die. The data storage speed was reported to achieve 500 MHz at a low power $< \sim$1 pJ. Additionally, MTJs instead of magnetic heads were used in order to write and read information.

Similar to the transition from slower STT-MRAM to faster SOT-MRAM, the use of more efficient interface-induced spin-orbit torques instead of spin-transfer torques allowed to boost the domain wall velocity up to several hundred m/s. Another important magnetic interfacial contribution, the Dzyaloshinskii-Moriya exchange interaction, helps forming compact Neel chiral domain walls [176]. Fast motion of chiral domain walls resulted in the third generation of racetrack memory.

Control of magnetic domain wall pinning and motion is of great importance to develop nonvolatile memory and logic circuits based on materials compatible with CMOS technology. Recently, an efficient pinning was engineered by growing CoFeB/MgO ultra-thin magnetic films with perpendicular anisotropy on a nano-patterned substrate [177]. Steps could be quite easily generated with a pitch scalable to the limits of lithography of less than 10 nm. The process is adopted from a well-known CMOS industrial process guaranteeing low costs at large-scale mass production.

Ferromagnetic domains generate a long-range magnetostatic field acting on the neighboring domains and the unwanted interaction between domain walls within and between racetracks poisoning the performance [170]. The use of a racetrack made of a synthetic antiferromagnet largely eliminates the magnetostatic fields [178]. The domain walls were moving extremely fast with the velocity of 750 m/s, thanks to the so-called giant exchange torque due to the antiferromagnetic coupling within the synthetic antiferromagnet [178]. Such high domain wall velocities indicate the fourth generation of racetrack memory for picosecond applications. It demonstrates that the last generation of racetrack memory is ready for industrial applications, with the research focus shifting toward reliability and reproducibility of domain wall motion and thermal stability.

Domain wall motion can be employed not only for accessing the stored information by bringing the relevant bit to a reading head or an MTJ. Recently current-driven magnetic domain wall logic [179] discussed in the next section was introduced.

To conclude the section, we mention the idea of using skyrmions or anti-skyrmions instead of domain walls as the memory storage element [180]. This will definitely acceler-

ate the progress in racetrack memory in particular and magnetoresistive nonvolatile memories in general. Nevertheless, describing the method here goes well beyond the scope of the chapter.

31.4 Spintronic Logic

Spin-based devices are considered as promising candidates to surpass the limits of state-of-the-art CMOS-based logic circuits by introducing nonvolatility into logic circuits. Although spin switches based on spin-enhanced transistors have been successfully demonstrated, the increase of the on-current ratio between the parallel and antiparallel source/drain magnetization configuration at room temperature and the efficient gate-voltage-induced spin control remain the main challenges preventing these devices from entering the market so far. In addition, as all proposed up-to-date spin switches require the charge current to transfer the spin, it sets limitations for the applicability of such devices in mainstream microelectronics which is already suffering from high power demand, and new ideas to realize spin-based switches for digital applications are urgently needed.

31.4.1 Magnetic Domain Wall Logic

A complete logic architecture which uses magnetic thin wires and domain wall motion along these wires was suggested at the beginning of the new century [181]. In order to perform data processing with this magnetic domain wall architecture, no electronic elements like transistors are required, so all calculations are performed in the magnetic domain. By engineering the magnetic wires and making junctions of a particular shape, all basic CMOS logic elements and gates can be implemented. The information is stored in the two magnetization orientations relative to the magnetic wall propagation direction. The signal fan-out is easily implemented by splitting a magnetic wire into two or more branches. Then, like in a splitter, the domain wall continues propagating through the branches.

A logic AND gate is implemented, if domain walls are coming to a splitter from the direction opposite to that in fan-out. The domain wall propagates further through the wire after the junction, if and only if the walls are arriving through each of the two input branches.

If now the two magnetic wires connected under a very small angle form a cusp, the domain wall changes the propagation direction after passing the cusp. As now the magnetization orientation relative to the propagation direction is opposite to the one before the cusp, the cusp-like structure represents a natural implementation of a NOT logical gate. In [181] the domain wall motion was driven to be an external rotating in-plane magnetic field which played simultaneously the role of a clock and a power supply. The logic gates can be arranged in a magnetic circuit, and a 5-bit magnetic shift register was demonstrated [181]. An advantage of the magnetic domain wall logic is that all the calculations are performed in the magnetic domain. However, an external magnetic field is required to operate magnetic circuits, which limits the technology's scalability.

Recently, the idea of using fully electrical current-induced domain wall motion to generalize domain wall logic was realized [182]. The architecture based on magnetic domain walls takes advantage of their fast motion discussed in the previous section and of the flexible design to store and to process information. The chiral coupling between neighboring magnetic domains due to the interfacial Dzyaloshinskii-Moriya interaction promotes a noncollinear spin alignment and helps realizing a domain wall inverter. Several reconfigurable NAND logic gates were successfully cascaded to perform the operations XOR and full-add by electrical control of the magnetic data. The energy consumption of a single NOT operation in a 10×10 nm^2 racetrack is estimated at 2×10^{17} J. Although comprehensive benchmarking of the proposed concept is pending [183, 184], it is positioned as a scalable platform to all electrically manipulated magnetic logic suitable for low-power, "instant-on" nonvolatile applications.

31.4.2 Logic-in-Memory

Magnetoresistive memories are CMOS compatible and can be embedded directly on top of a CMOS logic chip. This layout allows not only to introduce memory close to logic; it is also practical as it facilitates three-dimensional integration of circuits. The advantage of such an integration is that high-performance CMOS layers are separated by low energy-consuming nonvolatile MRAM containing spacers. At the same time, a combination of fast nonvolatile memory with CMOS circuits is a fertile playground for realizing microprocessors with reduced power consumption working on an entirely new principle. Placing MRAM arrays directly on top of CMOS circuits allows reducing the length of interconnects and the corresponding delay time. The computer architecture, where nonvolatile elements are located on a chip with CMOS devices, is traditionally called logic-in-memory architecture, although as of yet no information is processed in nonvolatile elements. Therefore, these hybrid CMOS/MTJ logic circuits employ MTJs only for storage. The actual logic operations are still carried out by CMOS components. Power-efficient MRAM-based logic-in-memory concepts have already been demonstrated [110]. They include field-programmable gate arrays and ternary content addressable memory, as well as other variants. These CMOS/spintronic hybrid solutions are already competitive

in comparison to the conventional CMOS technology with respect to power consumption and speed. The introduction of nonvolatility in circuits helps cutting the power consumption typically by 50%, with an outstanding 90% reduction in specific circuits [110]. As there is no general recipe for a transition toward large-scale logic systems, thorough and extensive studies to benchmark the different hybrid CMOS/MTJ logic circuits are required [183, 184].

31.4.3 Stateful Logic

Placing the actual computation into the magnetic domain by introducing nonvolatile processing elements reduces the need of converting magnetically stored information into currents and voltages for processing and helps to simplify the circuit layout and to increase the integration density. MTJs could be used as elementary blocks for nonconventional in-memory computing architectures. It was demonstrated in [185–187] that the direct communication between STT-MTJ devices can be exploited to realize conditional resistance switching on a target MTJ. The conditional switching depends on the initial resistance logic state and can be mapped to a specific Boolean operation. The initial resistance states of the MTJs act as the logic inputs and the resistance states after the operation hold the logic output. For these operations a readout of the MTJs' resistance states prior to a subsequent logic operation is not needed. Thus, stateful logic circuits exhibit a simple architecture in comparison to the hybrid CMOS/MTJ logic circuits with a CMOS-based logic implementation. Two types of stateful logic gates [111], reprogrammable logic gates [185, 186] and material implication gates [187, 188], are briefly discussed below.

The reprogrammable gates can realize conventional Boolean logic operations in two steps through a proper preset operation (TRUE or FALSE) in the output MTJ and then apply a certain voltage level to the gate. Depending on the reprogrammable logic states of the input MTJs, the preset state of the output MTJ, and the applied voltage level, a conditional switching behavior is performed on the output MTJ, which corresponds to a particular logic operation. Input MTJs are left unchanged as the current flowing through the output MTJ is divided between several inputs, thus becoming insufficient to alter their initial states.

Any two of the 1T-1MTJ cells in an MRAM array can also perform a conditional switching of a target MTJ depending on the state of the source MTJ [187, 189], an operation called material implication. The material implication operation (IMP) can, in combination with the FALSE operation, cover the whole space of all Boolean operations. A current-controlled implication logic gate proposed in [187] (Fig. 31.33) realizes a conditional switching behavior on the target MTJ (right) depending on the initial logic states of both the source and the target MTJ.

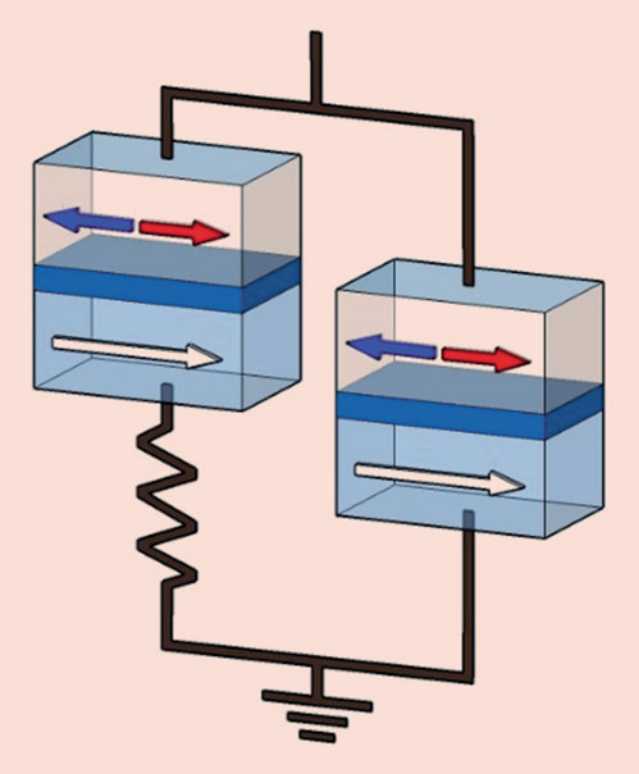

Fig. 31.33 A current-controlled implication logic gate [187] realizes a conditional switching behavior on the target MTJ (right) depending on the initial logic states of both the source (left) and the target MTJ

A comprehensive reliability study and comparison between the reprogrammable and the implication logic gates has been carried out in [190]. It has been shown that in order to reduce the switching errors, the TMR ratio must be increased. It has also been demonstrated that for a given TMR ratio, the implication gate exhibits a more reliable behavior in comparison to the reprogrammable logic gate devices. Due to a superior reliability of the material implication gate, implication-based logics outperforms the reprogrammable gate for complex logic functions like XOR and full-add operations. It makes the implication-based logics an implementation of choice for large-scale circuits.

By integrating MTJs on top of a CMOS circuit, one-transistor/one-MTJ (1T/1MTJ) cells are realized. These 1T/1MTJ cells typical for STT-MRAM structures can be assembled in an array and exploited for logic circuits and the development of novel nonvolatile large-scale logic architectures [191]. The advantages of the MRAM-based stateful logic are highlighted by demonstrating the STT-MRAM-based implementation of the fundamental arithmetic functions and a stateful spintronic full-adder [192]. The latter involves only 6 1T-1MTJ cells and 27 subsequent FALSE and IMP operations [192]. Recently, a massively parallel NOT operation based on IMP implementation by using

the voltage asymmetry of the voltage-controlled magnetic anisotropy effect and the precessional dynamics of the switching process was proposed [112]. By elaborating on design examples, the trade-off for such technologies with respect to the execution time, the energy consumption, and the reliability was investigated; however, a complete benchmarking [183, 184] is still missing.

The logic architectures described above are based on devices acting primarily as memory elements supplemented by computing functionalities. An alternative option is to follow a conventional path with memory and computing units separated, in which both elements are nonvolatile and implemented in the magnetic domain. The motivation for placing the actual computation into the magnetic domain is to eliminate the need of converting magnetically stored information into currents and voltages for processing and to operate only with spin degrees of freedom.

31.4.4 Buffered Magnetic Logic Environment

The use of a composite free layer results in significantly faster switching in STT MRAM cells as discussed in Sect. 31.3.1 The idea of combining several MTJs with a common free layer enables the realization of a nonvolatile magnetic flip-flop [193]. It consists of three antiferromagnetically coupled spin polarizer stacks featuring out-of-plane magnetization (Fig. 31.34). The polarizer stacks are grown on top of a common free layer with a perpendicular magnetic anisotropy. The stacks are separated from the free layer by MgO tunnel layers. The left and right stacks are used as inputs, while the middle stack is for readout. The information is stored in the magnetization orientation of the common free layer. Depending on the *polarity* of the input pulses, the torques acting on the free layer either add up or oppose each other. The resulting magnetization is preserved, if the input currents are opposite. This results in a HOLD operation. The magnetization can be put along the desired direction, if the currents run in the same direction, which results in SET/RESET operation. This behavior corresponds to flip-flop logic [194].

Extending the idea of a free layer common to several input signals applied through magnetic stacks, a majority gate [195] can be realized (Fig. 31.34). Together with the material implication gate, a majority gate-based calculation represents another example of performing logic operations differently as compared to CMOS circuits. In CMOS circuits any Boolean function is typically realized as a sequence of NAND operations. In contrast to NAND which gives an output "false" when all inputs are "true," the majority gate returns "true," when more than 50% of input signals are "true".

As first STT-based majority gate prototypes were recently fabricated [196], a realization of STT majority gate-based logic could already be possible in the near future. Processing with majority gates can be quite efficient. For example, complementing a majority gate with magnetic flip-flops used as buffers to store the output of the majority gate operation at a certain gate leg, a compact implementation of a one-bit full-adder is enabled. By connecting several majority gates through corresponding flip-flop buffers attached to their legs, the information transfer between different gates is ensured resulting in a nonvolatile processing environment [197]. The environment is capable of executing operations in parallel, and it offers the benefit of shared buffers between neighboring majority logic gates. Thus, it allows to reduce the energy and time spent for the information transport while maintaining a very dense layout. The synergetic combination of flip-flops and majority gates into a grid enables the flexible allocation of employed resources and gives generous freedom in reconfiguring its logic as the number of utilized buffers and gates can be adjusted depending on the task.

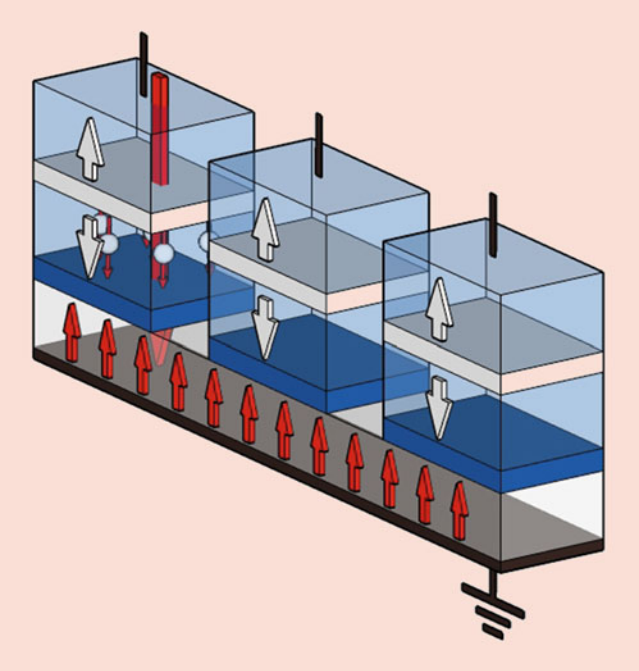

Fig. 31.34 Magnetic flip-flop [194] and a three-terminal majority gate [195, 196]. Three synthetic antiferromagnetic stacks are grown on a common free layer. The stacks provide spin-polarized currents running through the free layer. The spin polarization depends on the pulse polarity applied to a stack. The two stacks are used as inputs, while the stack in the middle is for reading. The magnetization of the free layer flips only if the two inputs are of the same polarity. This way a magnetic flip-flop is built [194]. By using the middle stack as output, a three-terminal majority gate is realized [195, 196]

31.4.5 All-Spin Logic

The fact that a spin signal is in principle independent from charge transport can be exploited for spintronic logic [198–

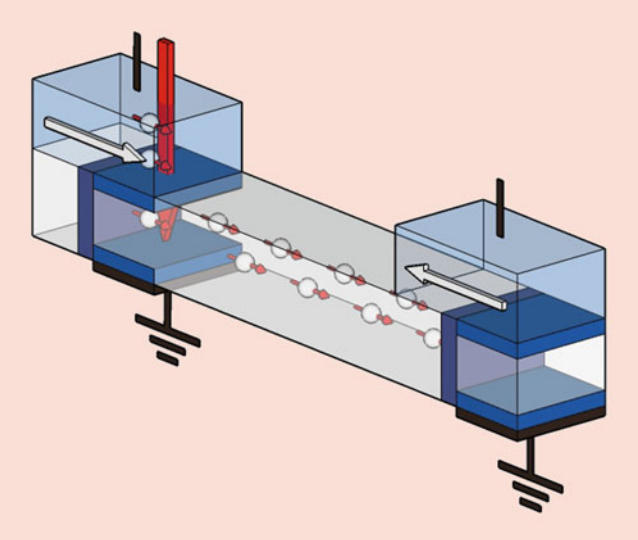

Fig. 31.35 All-spin logic. Non-equilibrium spin accumulation is created under a ferromagnetic layer (left) by passing the charge current through it. The spin accumulation diffuses along an interconnect and creates a spin-transfer torque acting on the right ferromagnetic layer

200]. The idea is to have a spintronic device which employs spin at every stage of its operation. This way a repeated spin-to-charge conversion is not needed. Input and output information are represented by the magnetization of nanomagnets. Physically separated nanomagnets are connected by nonmagnetic interconnects capable of carrying pure spin currents (Fig. 31.35). By inserting a charge current through a magnet, spin-polarized electrons are accumulated below the respective magnet in the interconnect. This spin accumulation diffuses along the interconnect to the next nanomagnet, where it exerts an STT on the magnetization. The generated spin signal is a pure spin current and can be used for sequential as well as combinational logic [198, 201, 202]. The all-spin-logic concept has gained popularity and ignited a wide variety of activities; however, even though the decoupling from the charge transport should reduce the power dissipation drastically, it appears to be not sufficient to outperform state-of-the-art CMOS circuits [183, 184, 203].

31.4.6 Benchmarking and Magnetoelectric Spin-Orbit Logic

Exploring the electron spin as a computational degree of freedom is a necessary step to proceed beyond charged-based CMOS devices in order to overcome CMOS-related limitations, namely, increasing demands to reduce the power consumption and, especially, the standby power with the introduction of new device generation nodes. A technology based on exploiting the magnetization orientation in ferromagnets to store the binary data promises a reduction in the standby power. However, the information is written by means of an STT exerted on a free layer created by spin-polarized currents. In STT-based logics, the spin-polarized currents are produced by the electrical currents running through the structure. As the current densities and the currents needed for the magnetization reversal of free layers with a sufficiently high thermal stability are large, a comparative benchmarking of emerging logic devices with respect to state-of-the-art CMOS logic is necessary. A comprehensive methodology proposed in [183, 184] demonstrates that although the introduction of spintronic devices into circuits is beneficial for specific applications, the overall performance of emerging spin-based circuits is still inferior as compared to CMOS circuits. Results of benchmarking [183, 184] SpinFET logic [73], STT/domain wall-based logic [193, 204], spintronic majority gate logics [195–197], and all-spin logic [198, 200] with respect to high-performance CMOS logic are shown in Table 31.2. One concludes that although circuits based on emerging spintronic devices are characterized by a lower power density and therefore smaller area, they possess a much longer delay and provide a much lower data throughput as compared to high-performance CMOS. One can also observe that SpinFET-based architectures and all-spin logics do not allow to reduce substantially the power density [183]. Although a careful benchmarking of STT material implication-based logic [187, 190] and magnetic domain wall-based logic [179] is pending, their operational principle is still based on torques generated by electric currents. Therefore, with a certain degree of confidence, one could conclude that it is unlikely these concepts will outperform CMOS logic, at least at the current technological level.

Table 31.2 Comparison of several logic circuits based on CMOS and spintronic devices with respect to delay (picoseconds), power density (watts per area), and throughput (number of 32-bit arithmetic logic unit operations per unit time and unit area, in units of tera-integer operations per second, TIOPS)

Name	Delay (ps)	Power density (W/cm^2)	Throughput ($TIOPS/cm^2$)
CMOS high performance	84 [183]	46.5 [183]	90 [205]
SpinFET	282 [183]	18 [183]	30 [183]
STT/domain wall	112,820 [183]	0.2 [205]	1.2 [205]
Spintronic majority gate	38,094 [183]	0.6 [205]	18 [205]
All-spin logic	26,261 [183]	38.2 [183]	7.5 [205]
MESO	2100 [205]	0.6–3.5 [205]	150 [205]

For energy-efficient solutions, it is mandatory to preserve the obvious advantages of spintronic logic devices, namely, nonvolatility and reconfigurability. As STT-based devices are not as fast as CMOS devices and STT-driven magnetization manipulation is energy consuming, a new fully electrical but

much more energy-efficient magnetization switching principle is required. The magnetoelectric effect defined as an ability to manipulate the magnetization by applying an electric field is extremely attractive as no charge current is flowing through or near the information storing magnetic layer. An electric field control of the magnetization direction at *room temperature* has been recently established in Pt/CoFe/Cu/-CoFe/$La_{0.1}Bi_{0.9}FeO_3$ [205]. A switching voltage lower than 1 V has already been demonstrated [205], while the ultimate goal to achieve switching at 0.1 V is currently pursued.

As no current is required for information writing, the efficient reading of the magnetization information and its transfer to the next device remain the critical steps prone to high power dissipation. To achieve the magnetization reading, a supply current flows through a part of the ferromagnetic layer overlapping with a material characterized by large spin-to-charge conversion efficiency. As in all-spin logic, the current becomes spin-polarized after passing the ferromagnetic layer, and the spin current is accompanying the flow of the supply current. The spin current generates a large charge current in the material due to the large spin-to-charge conversion [205]. The conversion is due to an inverse spin Hall effect. The promise of converting the spin current into a large charge current is enabled by the ongoing advances in spin-to-charge conversion using topological or high spin-orbit-coupling materials.

The charge current generated from the spin current due to the inverse spin Hall effect flows along the axis orthogonal to the spin polarization and spin current. An interconnect transfers the information to the next device. The charge current direction in the interconnect is determined by the magnetization direction of the ferromagnetic layer. This current supplied to the next device ensures the accumulation of the charge in its ferroelectric capacitor sufficient to manipulate the ferromagnetic layer. This way a highly energy-efficient logic based on magnetoelectric spin-orbit (MESO) devices is enabled [205].

The use of two physical principles, namely, the magnetoelectric effect for efficient and fast writing and large spin-to-charge conversion efficiency in emerging materials for efficient reading, puts nonvolatile electrically manipulated MESO-based devices as clear winner within the previously used benchmarking [183, 184, 205]. In particular, by simulating a 32bit arithmetic logic unit performance, the MESO logic shows a data throughput similar to high-performance CMOS logic, but at a one order of magnitude lower power density [205]. The logic based on MESO devices also demonstrates the lowest delay as compared to all spintronic logics [205], which makes it a clear favorite for building future fast nonvolatile energy-efficient logic. Examples of logic based on nonvolatile devices do not exhaust the whole variety of conceivable combinations between emerging nonvolatile devices and mature and very well-established CMOS devices. The availability of high-capacity nonvolatile memory close to high-performance processing units enables new computing architectures for future artificial intelligence and cognitive computing [113]. Nonvolatile MTJs are suitable for neural network realizations as they can be considered as a current-driven programmable resistor, a memristor [206]. MTJ-based neural networks featuring nonvolatile synapses [207] allow for high-speed pattern recognition with about a 70% reduction in gate count and a 99% improvement in speed as compared to their CMOS counterparts. All-spin binary neuromorphic computing systems with probabilistic inference and online learning can enable a new generation of state-compressed and low-power computing platforms [208]. Neuromorphic computing is becoming a reality, with self-learning chips already appearing on the market [209].

The successful adoption of nonvolatility in microelectronic systems by developing various logic, logic-in-memory architectures and in-memory processing will inevitably result in increasing dissemination of this technology for other applications such as ultralow-power electronics, high-performance computing, Big Data analysis, automotive electronics, and the Internet of Things and is expected to have an enormous impact on neuromorphic computing and artificial intelligence.

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Memristive/CMOS Devices for Neuromorphic Applications

32

Valerio Milo, Gerardo Malavena, Christian Monzio Compagnoni, and Daniele Ielmini

Contents

32.1 Introduction 1167

32.2 Memory Transistor and Mainstream Flash Technologies 1170

32.3 Neuromorphic Networks Based on Memory Transistor Synaptic Arrays 1172

32.4 Neuromorphic Networks Based on SRAM Arrays 1178

32.5 Memristive Devices 1181
32.5.1 2-Terminal Memristive Devices 1181
32.5.2 3-Terminal Memristive Devices 1182

32.6 Neuromorphic Networks with Memristive Devices 1184
32.6.1 SNNs with Memristive Devices 1184
32.6.2 DNNs with Memristive Devices 1186

32.7 Discussion 1189

32.8 Conclusions 1191

References 1192

Abstract

Neuromorphic computing aims at processing information in a way which is similar to the human brain, therefore featuring the ability to learn, adapt, and generalize with high computing parallelism and energy efficiency. To pursue this ambitious goal, neuromorphic computers must adopt brain-inspired architectures, which radically differ from the von Neumann concept of conventional computing. Neuromorphic computing thus typically relies on neural networks, consisting of neurons and synapses which are ideally compact, scalable, and operated at low voltage and current. Several device technologies have been proposed for neuromorphic computing, including both conventional memory devices based on the complementary metal-oxide semiconductor (CMOS) technology, and alternative memory (or memristor) technologies, where the storage concept is not based on charge, rather it relies on the local modification of the active material.

This chapter will review the status of neuromorphic devices including both CMOS-type and memristive devices. First, neuromorphic concepts using floating-gate and static random access memory (SRAM) arrays will be described, followed by memristive synapses and neurons which offer unprecedented density and scalability. The applications and performance of the various neuromorphic computing concepts will be illustrated and discussed.

Keywords

Neuromorphic computing · Floating-gate memory transistor · Memristor · Spiking neural network (SNN) · Deep neural network (DNN) · Backpropagation · Spike-timing dependent plasticity (STDP) · Inference accelerator

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32.1 Introduction

The complementary metal-oxide semiconductor (CMOS) technology has been the industrial platform for computing since the start of the microelectronics industry in the last century. The main advantage of the CMOS technology is its industrial manufacturability, where the parameters of the transistors and diodes can be controlled via the fabrication

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process and, most importantly, the scaling according to the Moore's law [1]. Despite all difficulties in the physical scaling of the transistor size, sub-10 nm technology nodes have been recently announced and soon will be commercially available [2, 3]. Approaches to further scale the technology in the future include multigate transistors [4] and 3D integration [5], which supports CMOS technology as the industrial mainstream technology platform for the future years and decades.

Besides scaling, the computing architecture is also facing significant challenges. Digital computers are all based on the von Neumann architecture, where data are processed in a central processing unit (CPU) and stored in a working memory, such as a dynamic random access memory (DRAM). The von Neumann architecture, however, suffers from significant latency and energy required by the movement of data between the CPU and the memory. This is a key challenge for big data tasks, where the information to be processed mainly consists of unstructured data such as audio, video, and other sensor data. The movement of large amount of input data and processing parameters, such as the synaptic weights in a neural network, constitutes a significant overhead from the point of view of latency and energy consumption. The memory bottleneck of von Neumann computers can be radically solved by in-memory computing (IMC), where data are processed in situ, directly within the memory [6]. In-memory computers do not follow the von Neumann architecture, in that there is no physical distinction between processing and memory units. The memory is constructed such that the computing can be executed physically within the data, for instance employing the concept of physical matrix-vector multiplication (MVM) in a cross-point array of resistive memory elements [7]. In-memory MVM has been fruitfully demonstrated for various applications, including the training of neural networks [8], the processing of image files [9, 10], and the solution of linear systems [11, 12].

Among the various approaches to IMC, the neuromorphic approach is one of the most fundamental and promising. Neuromorphic computing takes inspiration from the brain, to process information via neural networks consisting of neuron and synaptic elements. As in the human brain, there is no distinction between memory and processing units in a neural network, which accounts for the extreme energy efficiency of the brain, consuming only 20 W on average [13]. A generic neural network is the one originally proposed by McCulloch and Pitts in 1943 [14]. As shown in Fig. 32.1, input signals (x_1, x_2, etc.) are transferred to the neuron via synapses, which multiply the input signal by a characteristic weight (w_1, w_2, etc.). The weighted inputs are then summed within the neuron, and transformed by a characteristic non-linear activation function, such as a sigmoidal function, which yields the neuron output. Figure 32.2 shows a generalized neural network including 4 neuron layers, namely, the input layer, the output layer, and 2 intermediate or hidden layers.

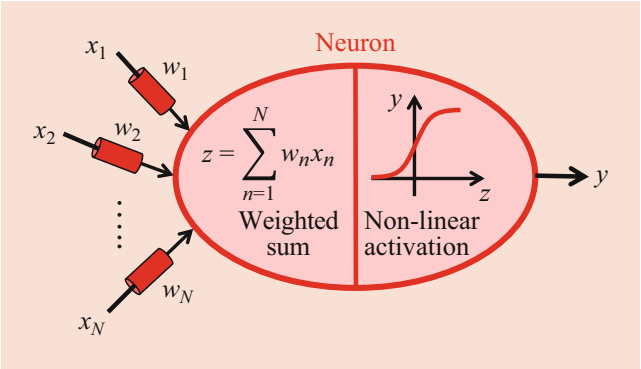

Fig. 32.1 Scheme of mathematical model of McCulloch and Pitts neuron where the sum of input signals x_n weighted by synaptic weights w_n is converted into the output y by application of a nonlinear activation function

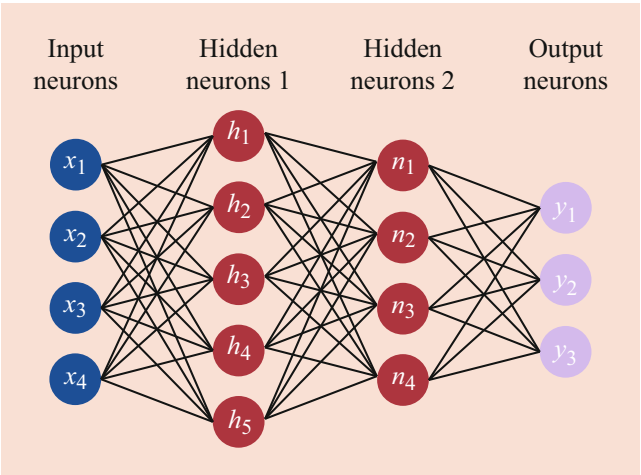

Fig. 32.2 Sketch of a multilayer perceptron (MLP) neural network, where the signal fed to the input layer forward propagates to the output layer passing through two hidden layers. Every neuron within the first three layers is fully connected to the neurons of next layer by individual synaptic connections. (Adapted from D. Ielmini et al. [23])

Originally proposed by Rosenblatt in 1957 [15], this neural network, also known as multilayer perceptron (MLP), is able to recognize, classify, and generalize, similar to our brain. The synaptic weights can be tuned for a certain task, e.g., recognizing between motorcycles and cars, by supervised learning algorithms, which iteratively optimize the value of each weight until the network reaches an acceptable classification accuracy [15, 16]. The MLP provides the fundamental basis for deep learning, where neural networks with many hidden layers are trained for recognition of images, speech, video, and other types of unstructured data [17–19]. A key issue for all deep learning machines is that they rely on conventional hardware based on the von Neumann architecture, such as the graphics processing unit (GPU) [20] and the tensor processing unit (TPU) [21]. To overcome the memory bottleneck issue, neuromorphic hardware must be developed

by adopting more radical, innovative circuit schemes, where non-von Neumann architecture and advanced devices allow for parallel computation and high energy efficiency [22].

From a device viewpoint, the MVM with memory devices can support the neuromorphic training and inference, while also providing schemes for compact representation of synaptic plasticity taking place in the human brain [23, 24]. Therefore, truly brain-inspired concepts of neuromorphic computing can be developed adopting nonvolatile memory devices. CMOS-based memories, such as static random access memory (SRAM) [22, 25] and floating-gate memories [26–30] have been proposed as possible synaptic devices to represent the weight of neuron-to-neuron connection. However, SRAM devices are volatile, thus requiring an initial upload of all synaptic parameters at system boot. On the other hand, floating gate memories, such as Flash, are typically affected by high operation voltages, and relatively slow program/erase. Most recently, emerging devices, broadly referred to as memristors, have been shown to provide a compact, functional, and brain-inspired option for implementing synaptic and neuron elements. A memristor consists of a two-terminal device where the resistance or conductance can change by the application of a relatively large voltage exceeding a threshold voltage. Memristor devices include resistive switching random access memory (RRAM), phase change memory (PCM), and other devices based on ferromagnetic and ferroelectric memory effects at the nanoscale. The size/-voltage scalability of these devices, combined with the nonvolatile nature of the storage, makes memristive approaches extremely promising for implementing brain-inspired, non-von Neumann neuromorphic systems.

Neuromorphic circuits can be organized into two main domains of neural networks, which can be referred to as deep neural network (DNN) and spiking neural network (SNN). Although both these types of network rely on the structure shown in Fig. 32.2, the input processing and learning mechanism are different. In DNN, all input signals are generally applied at the same time, encoding the input information via either amplitude or duration [31]. The input signals then propagate in the forward direction by multiplication with synaptic weights and summation at hidden and output neurons. Learning is generally carried out via supervised training techniques, where input patterns, e.g., images of faces, objects, digits, etc., are presented to the input layer together with a characterizing label. After forward propagation, the resulting output is compared with the ideal output corresponding to the label, thus allowing to calculate an error. This error is used to update the synaptic weights according to the backpropagation technique [32]. The training goes on for several epochs, each consisting of the presentation of the whole dataset of the patterns, until the recognition accuracy reaches a given threshold, generally above 90% [17–19]. In most cases, the supervised training is operated off-line, i.e., in a dedicated supercomputer equipped with high performance GPU or TPU. The synaptic weights are then stored in neural networks to carry out the inference operation, namely, the recognition of real-time images on the field. On the other hand, on-line supervised training has also been proposed, where the learning stage is operated in situ within the neural network, thus allowing for a compensation of nonidealities of the synaptic arrays, such as the cell-to-cell variability of conductance window and update characteristics [8, 33].

Contrary to the DNN, the SNN is more deeply anchored to the human brain model, where the most relevant information is the spike time, with less relevant roles played by amplitude and pulse width [34]. Neurons in an SNN typically have an integrate-and-fire structure, where incoming spikes are integrated until a threshold is reached, at which point a spike is emitted to the next neuron layer. Similar to the human brain, an SNN can implement a number of unsupervised training methods, all relying on the synaptic plasticity concept. In fact, many learning mechanisms in our brain are unsupervised, i.e., without labels, rather they take place by inherent feedback and interaction of sensory information within the biological neural network. Such type of learning can be supported by spike-timing dependent plasticity (STDP) rule described in Fig. 32.3. According to STDP, the weight of a synapse changes depending on the time delay Δt between spikes taking place at the pre-synaptic neuron (PRE) and the post-synaptic neuron (POST). If the POST spike follows, after a relatively short time, the PRE spike ($\Delta t > 0$), then the synaptic weight is potentiated (Fig. 32.3a). On the other hand, if the PRE spike follows the POST spike within a short time window ($\Delta t < 0$), the synaptic weight is depressed (Fig. 32.3b). STDP behavior has been evidenced in biological synapses in the hippocampus [35] and has been proven to lead to unsupervised learning of image patterns in stochastic SNNs [36–41]. Other spike-controlled plasticity processes have been proposed, namely, triplet-based STDP [42, 43] and spike-rate dependent plasticity (SRDP) [44, 45], and demonstrated in hardware [46–48]. In addition to unsupervised learning and the ability to replicate brain-inspired cognitive processes, SNNs benefit from a reduced energy consumption, as computation occurs only when it is needed, i.e., at the arrival of a spike. CMOS and memristive devices may play a leading role in both DNNs and SNNs, to enable scaling, nonvolatile storage of the synaptic weights, physical computation (e.g., by the MVM concept), and real-time adaptation by memory update processes.

This chapter reviews the current status regarding neuromorphic hardware developed with CMOS and memristive devices. Artificial synapses will be described referring to both DNNs for specific datasets (e.g., images, faces, objects, etc.) and SNNs able to learn by local STDP. The chapter is organized as follows: Sect. 32.2 reviews the operation principles of memory transistor and mainstream NAND and

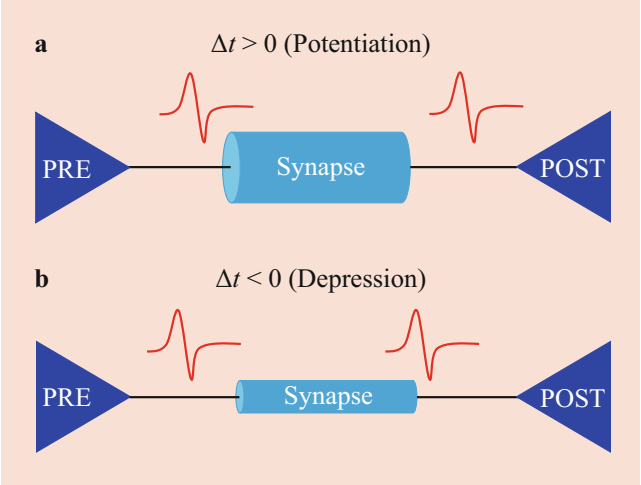

Fig. 32.3 Illustrative sketch of STDP experimental protocol controlling the synaptic plasticity. (**a**) If the spike emitted by PRE at certain time arrives just before the POST spike at synapse ($\Delta t > 0$), the weight of synaptic connection increases. (**b**) On the contrary, if PRE spike arrives just after the POST spike at the synapse ($\Delta t < 0$), the weight of synaptic connection decreases

NOR Flash technologies. Sections 32.3 and 32.4 are devoted to CMOS implementations, specifically focusing on synaptic circuits and neuromorphic networks based on floating-gate and SRAM arrays, respectively. Section 32.5 addresses the memristive devices with 2-terminal and 3-terminal structure. Section 32.6 reviews the synaptic implementations and hardware demonstrators of neuromorphic SNNs and DNNs with memristive devices. Section 32.7 discusses the existing applications and possible challenges of neuromorphic computing with CMOS/memristive devices. Finally, Sect. 32.8 presents the conclusions of the chapter.

32.2 Memory Transistor and Mainstream Flash Technologies

The memory transistor is the basic storage element adopted in mainstream nonvolatile memory technologies. Its working principles can be traced back to the change of threshold-voltage (V_T) of MOS devices arising from fixed charge in their gate insulator [49]. In order to exploit this effect to achieve a reliable memory device, an isolated charge storage layer is introduced in the gate stack of an MOS transistor (typically, an n-channel device). This layer may be either highly-doped polycrystalline silicon (polysilicon) or a dielectric material with a high density of microscopic defects able to capture/release charge carriers, as shown by the elementary structures schematically depicted in Fig. 32.4. In the former case, the charge storage layer is called a floating-gate. In the latter, it is called a charge-trap layer. In either case, the resulting gate stack allows not only to store a large amount of charge at a well-defined vertical distance from the gate of the transistor, i.e., inside the floating-gate or the charge-trap layer, but also to keep the charge stored at that distance over a timescale of months or years, thanks to the dielectric barriers blocking the emission of the stored charge toward the gate and the channel. The charge Q_S in the storage layer can then be considered as the parameter defining the state of the memory transistor and, by suitably discretizing it, digital information can be stored in a nonvolatile way in the device. Sensing of this information can be easily achieved by exploiting the proportionality between Q_S and the resulting shift of V_T (ΔV_T) with respect to the neutral storage layer condition, according to $\Delta V_T = -Q_S/C_{sg}$, where C_{sg} is the capacitance between the storage layer and the gate. In particular, the bits stored in the device can be determined on the basis of the value (high/low) of the drain current (I_D) resulting when, with a fixed drain bias (V_D), suitable gate biases (V_G) in-between the V_T values resulting from the discretization of Q_S and ΔV_T are applied, as shown in Fig. 32.5.

Changing the amount of charge in the storage layer and, in turn, the stored bits can be accomplished by means of different physical mechanisms. Among them, those which are by far the most exploited are Fowler-Nordheim (FN) tunneling and channel hot-electron injection (CHEI) [49, 50] (Fig. 32.6). FN tunneling may be achieved by applying a positive or negative V_G high enough to trigger a large flow of charge carriers between the channel and the storage layer by quantum mechanical tunneling through the energy barrier separating them (a flow of charge carriers between the gate and the storage layer may also take place, but this is typically undesired during device operation and thus minimized by suitable design choices). CHEI requires, instead, heating the carriers in the inversion layer of the transistor by means of a high V_D and redirecting them over the energy barrier separating the channel from the storage layer through a high V_G. While both FN tunneling and CHEI can be used to increase device V_T (program operation), only the former mechanism can be used to reduce V_T (erase operation).

It is worth mentioning, moreover, that FN tunneling typically requires much higher voltages than CHEI to move a similar amount of charge into the storage layer within a comparable time period. However, almost all the net charge flowing through the source and drain contacts of the memory transistor during a FN program operation is injected into the storage layer, while only a small fraction of the net charge flowing from source to drain is injected into the storage layer in the case of CHEI. This means that while the injection efficiency (corresponding to the ratio between the current injected into the storage layer and the current flowing at the source and drain terminals) of FN tunneling may in principle approach 1, that of CHEI is much smaller, typically close to 10^{-5}. Thus, the former mechanism is highly power-efficient and the latter is more power-hungry.

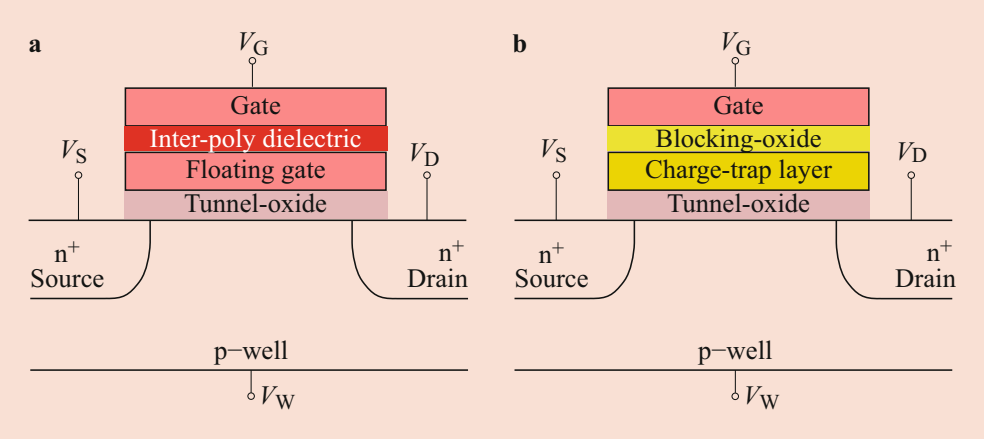

Fig. 32.4 Schematic of a memory cell exploiting (**a**) a highly-doped polysilicon layer and (**b**) a dielectric layer with a high density of microscopic defects for charge storage

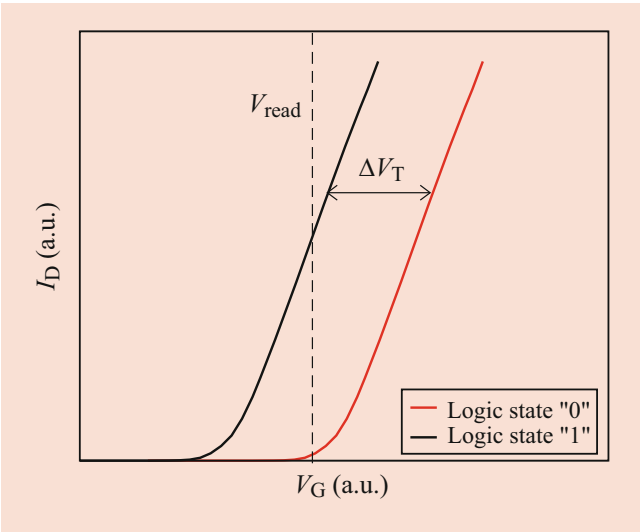

Fig. 32.5 Memory cell I-V curve for two amounts of charge in the storage layer, determining two different logic states

Due to their severe electrical stress on the gate dielectrics of the device, the number of program and erase operations that can be safely performed on a memory transistor for digital data storage is hardly higher than 10^5. The generation of microscopic defects in the bulk of the gate dielectrics and at the channel surface induced by program and erase operations, in fact, compromises the possibility to control device V_T and thus to store data in a reliable way. In particular, these defects may affect the program and erase performance and accuracy and, after V_T placement, may introduce relevant time-dependent instabilities in V_T itself due to their capturing/releasing charge carriers or their acting as stepping stones for the charge exchange between the storage layer and the channel or the gate of the memory transistor. All these effects may be particularly negative when the cells are used for machine learning applications, since they may compromise the accuracy of operations such as the MVM.

Starting from the elementary device structures reported in Fig. 32.4 and the general working principles discussed in the previous paragraphs, the specific design of memory transistors, their operating conditions and their organization into arrays strictly depend on the target applications of a memory technology. To understand this point, it is worth referring to the technologies representing the dominant solid-state solutions for nonvolatile data storage today, i.e., the NOR and NAND Flash technologies. Both these technologies make use of n-channel memory transistors as storage elements. However, their different aims lead to a different design of the memory devices, to the adoption of different working conditions and to a different organization of the memory array. The adoption of FN tunneling for the erase of a large number of cells in parallel (in a flash, hence their name) is, anyway, a common feature of the two solutions.

NAND Flash technologies target the storage of large amounts of data and, therefore, tend to minimize the cost per bit and to maximize the operating data throughputs of the memory chip. Since minimizing the cost per bit of the chip corresponds to maximizing its bit storage density, i.e., the ratio between the chip capacity and area, the reduction of (i) the silicon area per memory transistor, (ii) the number of contacts and service elements needed to address the memory cells in the array, and (iii) the array segmentation, represent some of the most important solutions that allowed to achieve the goals of the technology [51]. In a NAND Flash array, then, memory transistors are connected in series into strings (Fig. 32.7a) and a large number (tens of KBytes) of them belonging to different strings are programmed and read in parallel to maximize the operating throughput of the memory chip during data storage and retrieval (tens and hundreds of MBytes/s are, respectively, typical program

and read throughputs of NAND Flash chips nowadays). The possibility to program a very large number of cells in parallel is one of the benefits coming from the adoption of FN tunneling for both program and erase operations, allowing to limit the total current needed to transfer charge to/from the storage layer of the memory transistors thanks to the high injection efficiency of this mechanism. Drawbacks of the previous solutions are, however, the long times needed to perform single program operations (in the hundreds of μs timescale) and to access randomly selected stored bits (in the tens of μs timescale) in the array. It is worth mentioning, finally, that the improvement of the performance parameters of the technology and, in particular, of its bit storage density has long been pursued by means of a scaling process involving the reduction of the device feature size. This process led to the development of memory transistors with feature size as small as 15 nm in the middle of the 2010's decade and was then replaced by an equivalent scaling approach consisting of stacking many (currently, up to 128) memory cells in the vertical direction [51]. Figure 32.8 shows a schematic for a 3-D vertical NAND Flash array, highlighting the adoption of cylindrical gate-all-around memory transistors with vertical channel.

Differently from the NAND Flash case, NOR Flash technologies are mainly intended for code storage and, therefore, tend to minimize the time needed to store and retrieve small packets of data (a few Bytes). In particular, allowing a random access time to the stored bits shorter than 100 ns is mandatory for the target applications of the NOR Flash technology. To this aim, a strong array segmentation is adopted to reduce the delay times arising from the lines driving each memory transistor and, within each array sector, cells are connected in parallel (Fig. 32.7b). This results in a number of contacts per cell higher than that of NAND Flash arrays. To achieve the goals of the technology, CHEI is used for the program operations, while the use of FN tunneling is limited to the erase operations. The need for a simultaneous gate and drain voltage, in fact, makes CHEI a mechanism allowing to easily achieve fast (in the μs timescale) and single-cell selective program operations within the NOR architecture. As previously discussed, moreover, this mechanism involves moving high-energy electrons above the energy barrier separating the channel from the storage layer of the memory transistors and does not require to reach vertical electric fields as high as those needed to make electrons tunnel through the same energy barrier. This allows to perform the program operations at voltages lower than those required by FN tunneling and to use a dielectric isolating the storage layer from the channel thicker than in the NAND Flash case (the thickness of that dielectric is typically about 10 nm in the NOR Flash case and about 6 nm in the NAND Flash case). However, the relatively high V_D needed for device operation does not allow to minimize the channel length of the memory transistors, which is therefore much longer than in a NAND Flash technology of equal feature size. This contributes, along with the previously discussed features of NOR Flash arrays, to reducing the bit storage density of the technology and, in the end, to increasing the cost per bit of a NOR Flash chip over that of a NAND Flash chip. The cost increase, anyway, allows the NOR Flash technology to offer faster random access operations on the array at the Byte level and to target code storage applications successfully. In this regard, the use of thicker dielectrics isolating the storage layer and of memory transistors with larger dimensions than in the NAND Flash case allows the NOR Flash technology to satisfy another important requirement of code storage applications, i.e., that of an extremely good raw array reliability. It is worth mentioning, finally, that assuring proper array operation and suitable raw array reliability has strongly limited the scaling path of the NOR Flash technology with respect to the NAND Flash technology, with the feature size of the former being about 40 nm at the state-of-the-art.

32.3 Neuromorphic Networks Based on Memory Transistor Synaptic Arrays

Arrays of memory transistors represent a viable alternative to non-volatile memory cross-point arrays to be exploited as synaptic arrays in artificial neural networks (ANNs) and brain-inspired neural networks. Indeed, their main element, often employing a floating-gate as charge-storage layer, can conveniently embed in a single device the wanted synaptic functionalities. In particular, when exploited as synaptic element, a floating-gate transistor is operated in subthreshold regime, where the following well-known exponential relation

$$I_{DS} = I_0 \cdot e^{\frac{q\alpha_G\left(V_{GS}-V_T^{ref}\right)}{mkT}} \cdot e^{-\frac{q\alpha_G\Delta V_T}{mkT}} \tag{32.1}$$

holds between V_{GS} and I_{DS}. Here, I_0 is the current prefactor, q is the elementary charge, m is the subthreshold slope ideality factor, kT is the thermal energy, α_G is the gate-to-floating-gate capacitive coupling ratio, and ΔV_T represents the floating-gate transistor V_T shift from an arbitrary chosen reference $V_T{}^{ref}$. In so doing, I_{DS}, to be considered as the output signal, is the product between a function of V_{GS}, to be considered as the input signal, and a remaining factor $W = e^{-\frac{q\alpha_G\Delta V_T}{mkT}}$ depending on ΔV_T, playing the role of the synaptic weight.

The low currents typical of the subthreshold regime make floating-gate transistors attractive for neuromorphic applications in terms of reduced power consumption. Some other intriguing features are fine weight granularity, coming from the virtually analog and bidirectional tuning of the charge

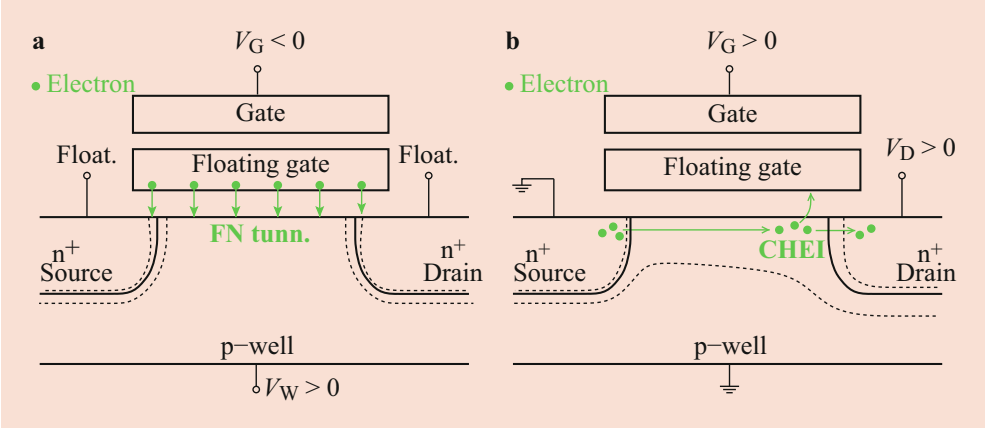

Fig. 32.6 Physical mechanisms and corresponding voltage schemes exploited to change the amount of charge in the cell storage layer, consisting of (**a**) Fowler-Nordheim (FN) and (**b**) channel hot-electron injection (CHEI). (Adapted with permission from G. Malavena et al. [50], Copyright 2019 IEEE)

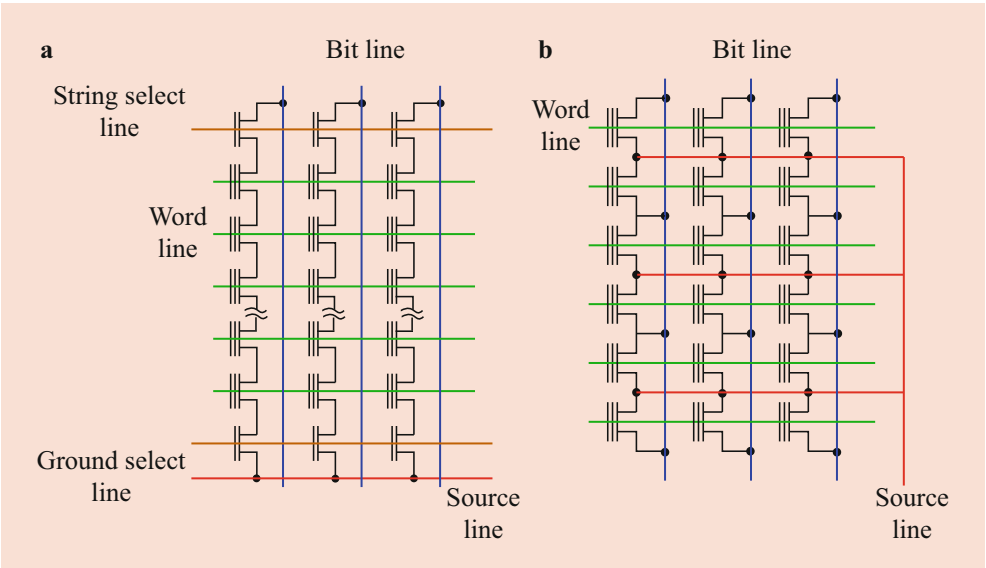

Fig. 32.7 Schematic of memory arrays based on (**a**) NAND Flash and (**b**) NOR Flash architecture

stored in the floating-gate, and a mature and reliable CMOS compatible fabrication technology, resulting from the continuous effort devoted in the last decades to make non-volatile memory technologies keep pace with Moore's scaling paradigm. Note that while building synaptic arrays using a consolidated technology as floating gate memory transistors is an appealing solution, the issue due to the single cell V_T tunability remains a mandatory requirement to be addressed. For this reason, NOR Flash architecture appears as the most natural candidate for neuromorphic applications, being the memory cells connected in parallel, with all their contacts made available through signal lines. However, the classical NOR Flash program and erase schemes are not suitable for the purpose; in fact, as already pointed out in Sect. 32.2, while the program operation, based on CHEI at the drain side, can be performed on a single cell, the erase operation, relying on FN tunneling, involves a large number of cells at the same time. For this reason, the main approach adopted to enable the necessary single-cell selective erase operation and to build floating-gate transistor-based synaptic arrays consists of making some changes to the memory transistor structure, to the NOR Flash array design or to its working schemes.

The first proposal of exploiting a floating-gate transistor to build an artificial analogue synapse, dating back to the late 1990s [52–54], consisted of modifying its structure to accommodate an additional contact to be exploited for the erase operation. Such device, usually called synaptic transistor, is shown in Fig. 32.9, together with its main features and the adopted program and erase mechanism. A synaptic transistor is essentially equivalent to an n-channel floating-gate transistor, in which its floating-gate is extended

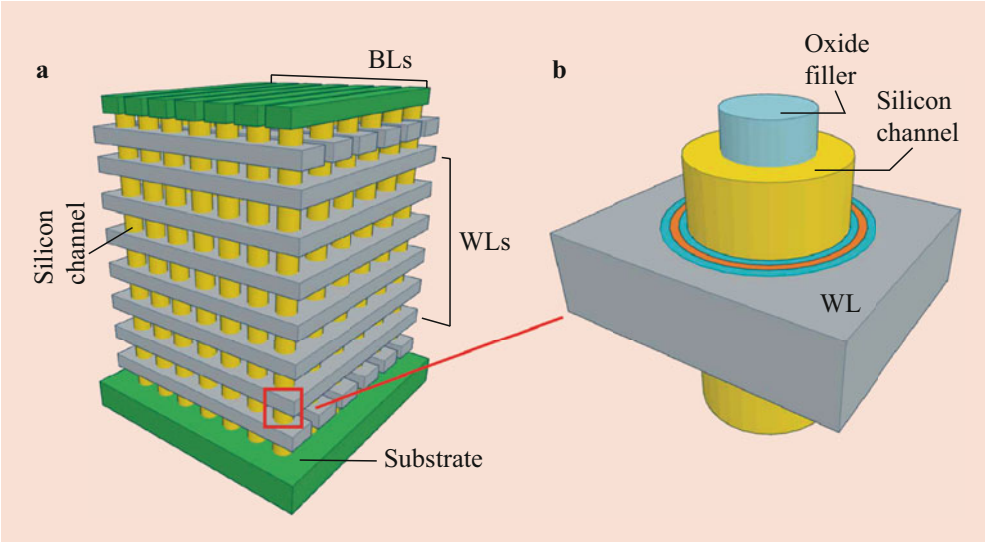

Fig. 32.8 Schematic of a 3D NAND Flash memory array (**a**) and vertical gate-all-around cell structure (**b**). (Adapted with permission from C. Monzio Compagnoni et al. [51], Copyright 2017 IEEE)

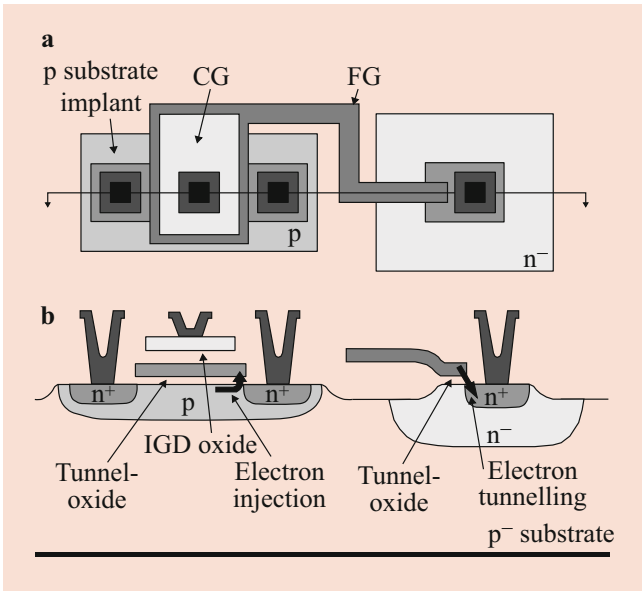

Fig. 32.9 Top view (**a**) and side view (**b**) of the synaptic transistor. Physical mechanisms exploited for program (electron injection) and erase (electron tunneling) are highlighted too. (Adapted with permission from C. Diorio et al. [54], Copyright 1997 IEEE)

as shown in Fig. 32.9 and capacitively coupled to an n^+ contact implantation, referred to as tunneling junction. By applying a positive voltage to the tunneling junction with respect to the gate, electrons stored in the floating-gate can be removed by FN tunneling with single-cell selectivity; in fact, during this operation, the p-substrate, common to all the array cells, is always kept to ground. On the contrary, the program operation is unchanged with respect to its classical scheme, consisting of CHEI at the drain side and achieved by simultaneously applying a positive voltage to gate and drain. A first demonstration of MVM and weight update is reported in [54], while LTP and LTD schemes based on the STDP learning rule are implemented in [29].

More recently, after neuromorphic systems brought renewed attention, other solutions based on custom devices fabrication were proposed [55–57]. In [55] a double-gate floating-body synaptic transistor is introduced, exploiting hot-hole injection in the gate ONO stack to achieve selective erase. In [56], instead, the authors came up with a TFT-transistor with a half-covered floating-gate, with its erase scheme still consisting of stored electrons tunneling out from the floating-gate. Both devices were tested in brain-inspired neural networks in [56] and [57], respectively.

Another approach, alternative to custom device fabrication, consists of slightly modifying commercially available NOR Flash arrays architecture, while keeping the single cell structure unchanged [58–61]. In Fig. 32.10a and b, a schematic cross-section and the equivalent circuit of the 180 nm technology cell by Silicon Storage Technology (SST) [62] chosen for the purpose are depicted, consisting of a floating-gate transistor with a highly asymmetric structure, with its gate overlapping the drain region, while being separated from the source region by a floating-gate. By applying a positive voltage between source and drain, with a positive voltage at the cell gate too, the program operation is performed by CHEI at the source side. On the contrary, the erase scheme requires only a positive voltage drop between gate and source (the drain voltage does not play any relevant role here), allowing trapped electrons to tunnel out from the floating gate. Figure 32.10c shows how such cells are arranged in a NOR Flash array, together with the voltages applied to all the lines during the erase protocol. In this

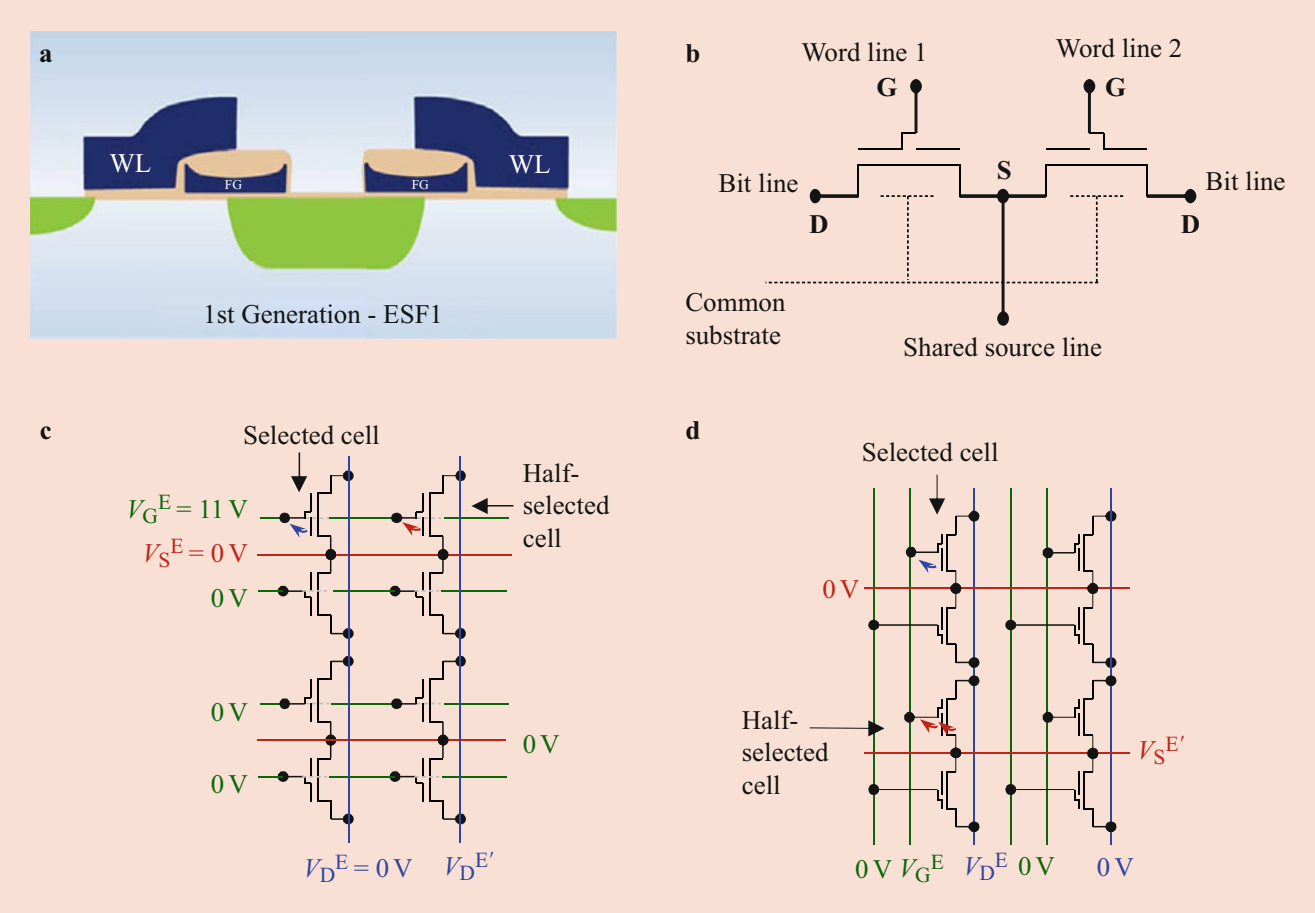

Fig. 32.10 (**a**) Schematic cross-section and (**b**) equivalent circuit of the SST cell structure. NOR array with (**c**) classic and (**d**) modified routing together with the respective erase protocol. (Adapted with permission from F. Merrikh-Bayat et al. [58], Copyright 2015 IEEE)

commercial architecture both WLs and SLs run parallel connecting cells belonging at the same row, hence the erase operation is performed simultaneously on a whole row (this is not true for the program operation since the BL, shorting the drains of all the cells in a column, runs perpendicular to the WL and the SL). To guarantee single-cell selective erase, mandatory for neuromorphic applications, the routing of the array is modified as in Fig. 32.10d, with the WLs now running perpendicular to the SLs. In this way, the voltage scheme depicted in Fig. 32.10d allows to access one single cell at the time, inhibiting any V_T change in the remaining ones. Note that selectivity during program is preserved after this modification.

Two such re-routed NOR Flash arrays have been exploited in [59] and [60] as synaptic arrays to demonstrate a fully integrated three-layer (784 × 64 × 10) ANN, which was trained offline on the Modified National Institute of Standards and Technology (MNIST) handwritten digit database by the backpropagation algorithm.

In order to reduce random drifts and also to implement negative weights, the differential scheme of Fig. 32.11a was adopted. Each synaptic connection is implemented through two adjacent memory cells of each column and each neuron through a differential current operational amplifier summing the resulting BL currents, followed by an activation function block. A schematic for the high level architecture of the whole chip (having a total active area below 1 mm^2) is reported in Fig. 32.11b, where two synaptic arrays (whose dimensions of 785 × 128 and 65 × 20 are determined by the chosen differential implementation), two neuron layers and some additional required circuitry are shown. The resulting network has shown a 94.7% classification accuracy with one-pattern classification time and energy equal to 1 μs and sub-20-nJ, respectively. Moreover, performance is expected to increase considerably when moving from the currently adopted 180 nm to the next 55 nm technology, which was already tested for MVM implementation at array level in [61].

Despite the encouraging results, a drawback associated with the routing in Fig. 32.10d is the increased area per cell, being 2.3 times larger than the original one, due to the additional area needed to accommodate two gate lines for each column [60]. An alternative approach, with the

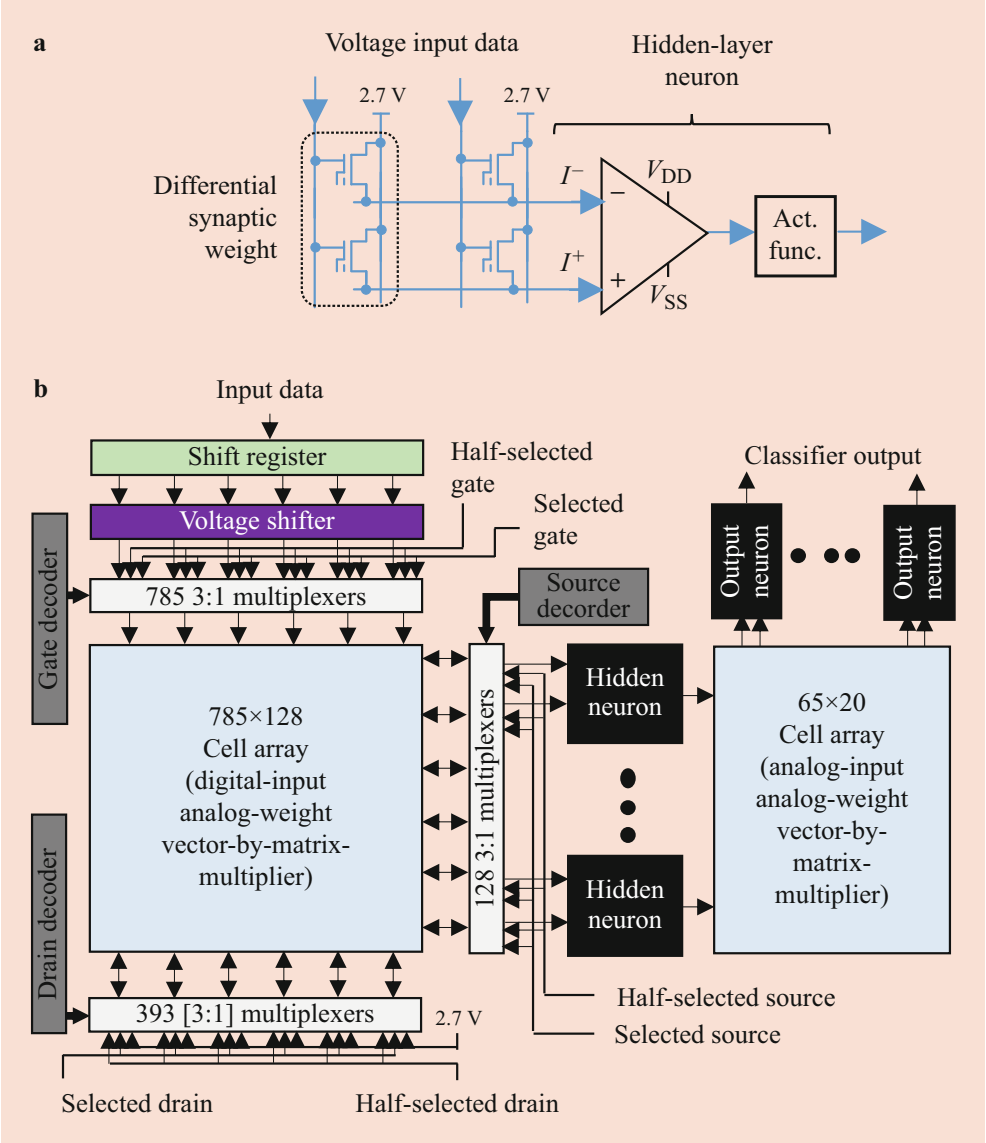

Fig. 32.11 (**a**) Differential implementation of a synaptic connection followed by a hidden-layer neuron, consisting of a differential summing operational amplifier and an activation-function block. (**b**) High-level architecture of the ANN and needed additional circuitry. (Adapted with permission from F. Merrikh-Bayat et al. [60], Copyright 2018 IEEE)

advantage of keeping the area per cell unchanged, is reported in [50, 63, 64]. With no change either in the cell or the array design, a simple yet effective single-cell selective erase scheme is suggested and tested on a mainstream common-ground NOR Flash array in 40 nm embedded technology by STMicroelectronics (Fig. 32.12a). As shown in Fig. 32.12b, keeping the CHEI mechanism for cell programming, the parallel cell erase operation, typical of Flash arrays based on FN tunneling, was overcome by exploiting hot-hole injection (HHI) in the floating-gate. In fact, the combined effect of negative WL and positive BL voltages (while grounding the remaining lines) results in holes generated by band-to-band tunneling at the drain side; a fraction of the generated holes, accelerated by the horizontal electric field developed by the drain-to-body voltage drop, are injected in the cell floating-gate reducing the cell V_T. Starting from this program/erase scheme, the STDP learning rule is reproduced through the pre-synaptic and post-synaptic waveforms depicted in Fig. 32.13a. In fact, depending on the time delay Δt between the pre-synaptic and post-synaptic spikes, this scheme makes the rectangular BL pulse occur either during the positive ($\Delta t < 0$) or negative ($\Delta t > 0$) front of the WL waveform. In the former case CHEI takes place, resulting in LTD, while in the latter case HHI is triggered, resulting in LTP. The functionality of this working scheme was proven in a prototype spiking neural network learning according to the STDP rule (Fig. 32.13b) and tested on a pattern recognition task.

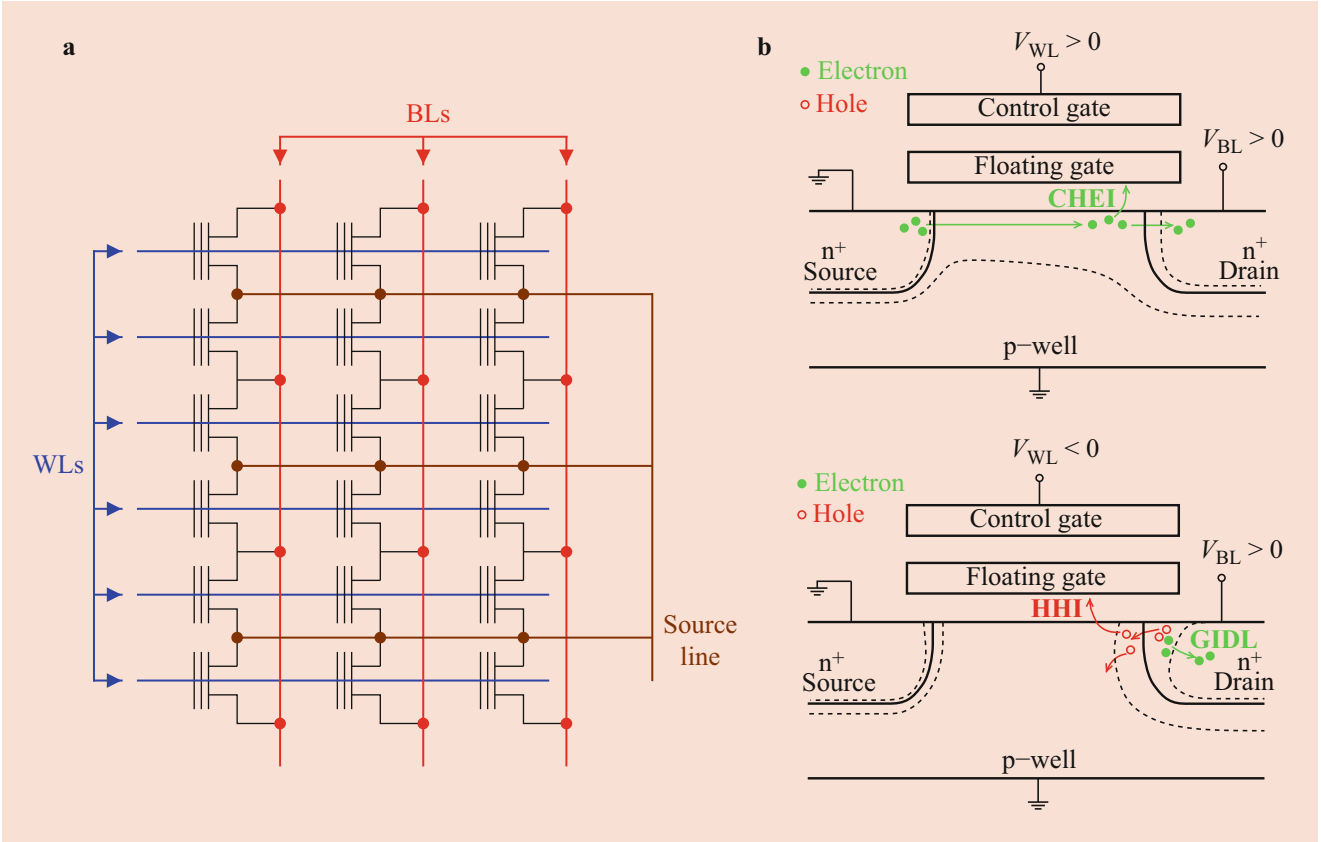

Fig. 32.12 (**a**) Schematic for a mainstream common-ground NOR Flash array and (**b**) physical mechanisms exploited for (**b**) program and (**b**) erase operations. (Adapted with permission from G. Malavena et al. [63], Copyright 2018 IEEE)

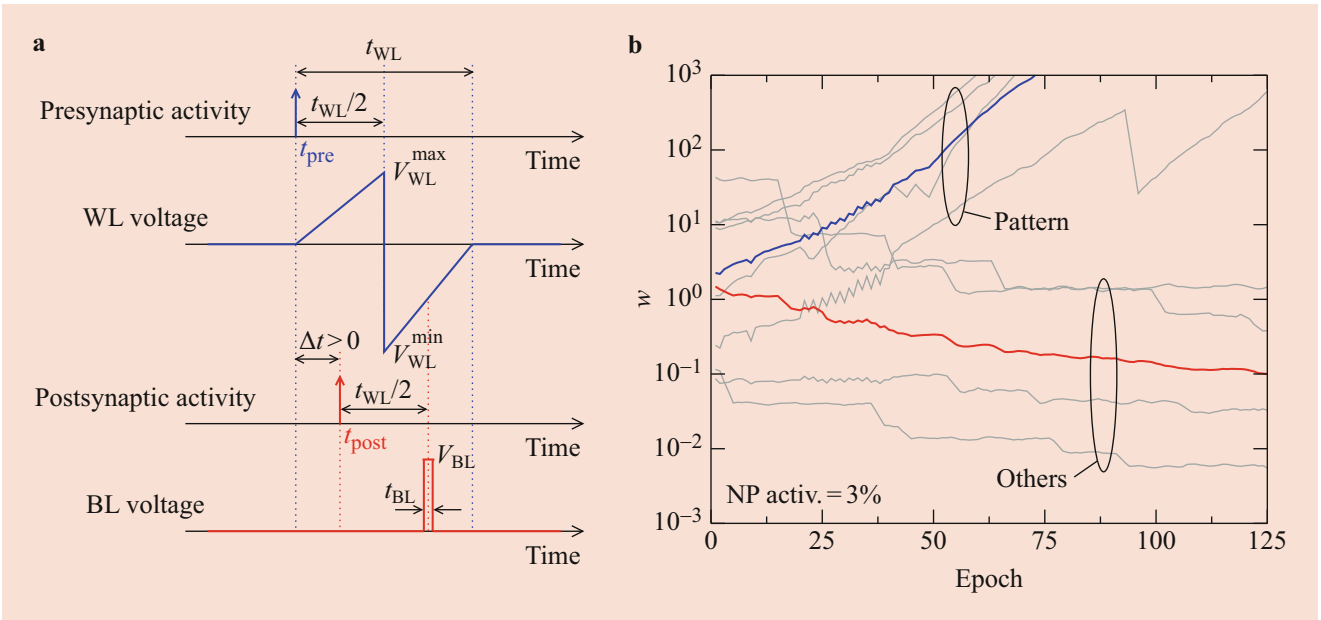

Fig. 32.13 (**a**) Pulse scheme proposed to implement the STDP waveform exploiting the program and erase mechanisms shown in Fig. 32.12b and (**b**) evolution of the weights of the implemented NOR Flash-based spiking neural network during the learning phase. (Adapted with permission from G. Malavena et al. [63], Copyright 2018 IEEE)

A final important aspect that needs to be addressed is the unavoidable uncertainty coming with the tuning procedure of the weights and their stability during the operation of the network. This point is of key importance in DNN inference, for which the weights are transferred to the memory array with closed-loop tuning algorithms to achieve high precision and pre-trained network stability plays a major role. A comprehensive statistical simulation-based investigation of a common-ground NOR Flash-based digit classifier accounting also for V_T placement accuracy and instabilities is reported in [65]. Here the ANN weight distribution resulting from standard network training and testing based on the MNIST database is transferred to the arrays cells. This is done by placing their V_T exploiting the incremental step pulse programming (ISPP) algorithm, widely adopted for program in storage NOR Flash arrays, and, in so doing, evaluating the impact of the statistical nature of electron injection in the floating-gate on the performance of the network (Program Noise, PN). After that, the impact of V_T oscillations due to Random Telegraph Noise (RTN) arising from capture/release of charge carriers in tunnel-oxide defects is also assessed. Starting from a parametric analysis, the authors give some quantitative criteria to determine the accuracy required in the tuning algorithm and the size to which NOR Flash array cells can be scaled when targeting neuromorphic applications.

32.4 Neuromorphic Networks Based on SRAM Arrays

Besides floating-gate memory arrays, another CMOS approach based on SRAM arrays has been extensively investigated for achieving hardware implementation of neuromorphic networks. Despite the limitations due to its volatile storage principle and large footprint, it was demonstrated that a conventional 6T SRAM cell can combine computing and memory functions, thus enabling the implementation of a machine learning classifier based on an SRAM array [66, 67]. Fig. 32.14a shows the architecture of an in-memory machine learning classifier based on a 130 nm CMOS 128×128 SRAM array which, by means of periphery circuits, can be driven in SRAM mode (weight read/write operation) and Classify mode, respectively. In Classify mode, each column of SRAM array operates as a linear classifier making a decision d according to the equation

$$d = \mathrm{sgn}\left(\sum_{i=1}^{N} w_i \cdot x_i\right) \tag{32.2}$$

where w_i is the weight stored in the i-th SRAM column cell and x_i is i-th element of feature vector applied at once to the SRAM array via analog DACs controlling the wordlines WLs.

As shown in Fig. 32.14b, after precharging the bitline pair BL and BLB to the supply voltage, the 5-bit feature vector application to WLs activates a current $I_{BC,i}$ within every cell leading to a proportional BL or BLB discharge depending on the logic value 0/1 stored in the bit cell. Importantly, note that if BL/BLB is treated as a differential voltage signal, one can observe that each element of analog input vector is weighted by −1/+1 and all the column bit currents are summed on BL/BLB, returning a net discharge voltage which is then compared with a threshold by a comparator circuit. As a result, the Classify mode operation of SRAM-based columns provides an energy-efficient and highly parallelized IMC implementation. However, despite these significant benefits, this linear classifier concept, which is a 'weak' classifier since it cannot be trained to fit very complex data distributions, is affected by two critical issues consisting of the non-idealities in MVM due to bit cell variations and BL/BLB discharge non-linearities, and limited weight precision. To overcome these issues, a training procedure based on an error-adaptive classifier boosting algorithm able to compensate fitting errors along with circuit non-idealities by using many weak classifiers [68] combined with the integration of binary weight quantization during error function minimization was developed. Using this training approach, the authors of [66, 67] built a mixed hardware/software image recognition demonstrator employing 45 SRAM column-based classifiers for training and recognition of 9×9 cropped MNIST images, achieving a test accuracy of 90% and a 12× energy saving against an ideal conventional SRAM/digital-adder system with linear classifiers based on binarized weights. In a following work [69], an SRAM-based three-layer binarized DNN capable of a higher test accuracy than the one above discussed was presented. Here, 3 chips were used to implement a three-layer DNN based on a 10×10 input layer, two hidden layers with 96 neurons, and an output layer with 10 neurons. In particular, the hardware demonstration is only limited to training/inference forward propagation while error signal backpropagation and weight updates were computed in software with the data exchange between chip and simulator managed by software-controlled DAQs. This neural network prototype, where any neuron of input and hidden layers is given by an SRAM IMC column, was trained on 50,000 images from MNIST train dataset with cropped size of 10×10 pixels, then quantized to 5-bit inputs, and tested on all 10,000 test images. After a training procedure based on binarized weights and activation functions as theoretically proposed in [70], the three-layer binarized DNN accelerator achieved a maximum on-chip inference accuracy very close to the baseline of 94% after 20 training epochs (<0.4%), with a significant improvement in terms of energy efficiency compared to the same network implemented with standard digital hardware (26×), at a very high efficiency of 700 TOPS/W and 6 TOPS/mm^2 for inference operation.

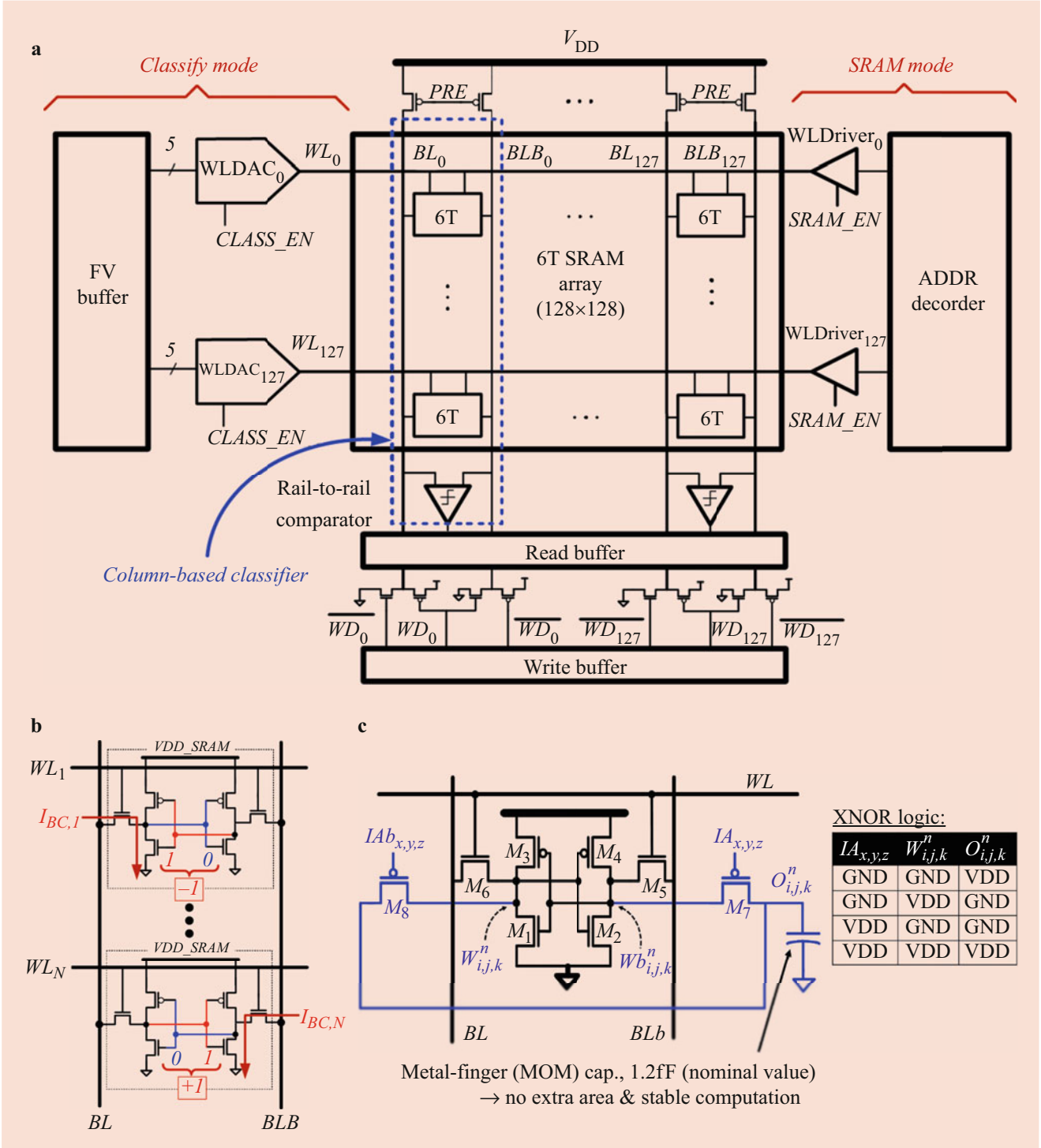

Fig. 32.14 (**a**) Architecture of an in-memory machine learning classifier based on a standard 6T SRAM array that can be operated in SRAM mode (read/write of stored weight) and SRAM classify mode (in-memory multiplication and accumulation along a column). (**b**) SRAM array column implementing a linear weak classifier. (**c**) 8T SRAM cell including a precisely controlled metal-oxide-metal capacitor to sample the charge resulting from an in-memory binary multiplication (XNOR) between the input activation *IA* and the stored weight *W*. (Adapted with permission from J. Zhang et al. [67], H. Valavi et al. [73], Copyright 2017, 2019 IEEE)

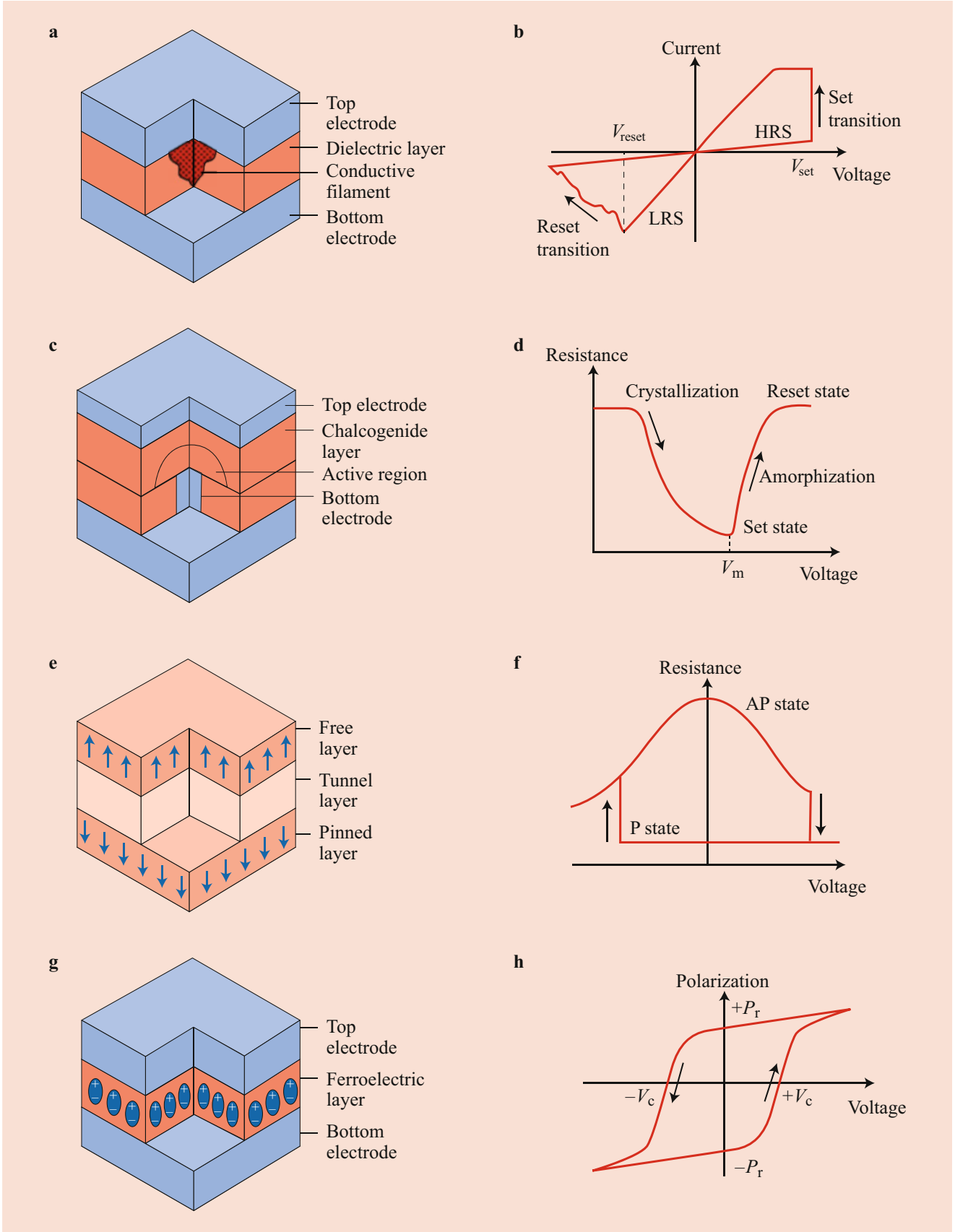

Fig. 32.15 (continued)

Besides this implementation, note that other competitive binary DNN accelerators based on 6T SRAM-based IMC have been recently proposed [71].

Fig. 32.14c shows a novel SRAM-based device concept, referred to as 8T SRAM, which combines a standard 6T SRAM with 2 additional PMOS and a finger metal-oxide-metal capacitor [72]. This cell performs the multiplication between a binary 1-bit input signal IA and a 1-bit weight stored in the 6T SRAM, which corresponds to an XNOR function. Compared with standard 6T SRAM cell, the 8T SRAM cell includes a capacitor where the multiplication result is sampled, which allows it to bypass the bit-line variability of standard cell since the cell capacitance can be better controlled in the modern VLSI technology. Thanks to this advantage, the 8T SRAM cell was operated to perform MVM in a binarized convolutional DNN, achieving software-equivalent test accuracy on MNIST dataset (98.6%) and CIFAR-10 dataset (83.3%), and exhibiting an energy efficiency of 866 binary TOPS/W and a throughput of 19 TOPS [73]. Finally, to tackle the binary precision limitation, a novel IMC cell based on two 8T SRAM (T8T SRAM) cells was proposed in [74]. This new cell concept enabled the design and implementation of multibit convolutional DNNs at array level capable of a significant improvement in terms of inference accuracy, in particular for a challenging dataset as CIFAR-10 (from 83.3% to 90.42%).

32.5 Memristive Devices

Achieving brain-inspired functionalities in hardware neural networks requires the identification of technologies suitable to replicate realistic behavior of synapses and neurons. To this end, novel materials-based device concepts referred to as memristors [75, 76] have recently received increasing interest since they offer attractive features such as the opportunity to store information at nanoscale in analogue and nonvolatile states. Moreover, memristive devices can also be operated to execute data processing in situ, thus paving the way to the development of IMC approach [6]. Depending on their structure, memristive devices can belong either to the class of 2-terminal devices or to the class of 3-terminal devices, which results in different functionalities as explained in the following.

32.5.1 2-Terminal Memristive Devices

Figure 32.15 shows the 2-terminal memristive device concepts receiving the greatest interest for neuromorphic hardware. All the devices exhibit a simple structure where two metal electrodes sandwich an insulator and/or active layer. Also, the application of external voltage pulses at the device electrodes called top electrode (TE) and bottom electrode (BE), respectively, leads material properties of these devices to undergo a modification resulting in a change of resistance or magnetic/electric polarization depending on the material.

Figure 32.15a schematically shows an RRAM device, consisting of a metal-insulator-metal (MIM) stack where the resistance of the insulating layer, typically based on transition metal oxides such as HfO_2 [77], TaO_2 [78], TiO_2 [79, 80] and SiO_2 [81], can change from a high resistance state (HRS) to a low resistance state (LRS) and vice versa via the creation and disruption of percolation paths called conductive filaments (CFs), respectively [82–84]. To initiate a CF into an RRAM device, a soft dielectric breakdown called forming is preliminarily performed, leading to a high conductivity enhancement via generation of a high concentration of ionized defects, such as oxygen vacancies and/or metal impurities, in a highly localized region of insulator layer. After forming operation, the application of voltage pulses with the same polarity in case of unipolar RRAM [85–88] or opposite polarities in the case of bipolar RRAM [84] can cause a set transition, which leads the device from HRS to LRS, and a reset transition, which leads the device from LRS to HRS. These resistance transitions are clearly evidenced by the typical current-voltage (I-V) characteristics of bipolar RRAM devices shown in Fig. 32.15b where set process exhibits an abrupt current increase as the applied voltage reaches the set voltage V_{set} whereas the reset process, which starts at negative voltage V_{reset}, shows more gradual dynamics. Specifically, as positive voltage across the RRAM reaches V_{set}, a defect migration driven by drift mechanism is activated from the defect reservoir at TE to the BE causing the formation of CF connecting two electrodes, which results in a resistance decrease. On the other hand, the application of a negative voltage V_{reset} activates a defect migration

Fig. 32.15 Sketch of the main 2-terminal memristive devices recently used for IMC applications such as neuromorphic computing. (**a**) Structure and (**b**) current-voltage characteristics of an RRAM device. RRAM consists of a MIM stack where the creation of a CF within the insulator layer achieved at positive voltages higher than V_{set} leads the device to LRS (set transition) while the dissolution of CF achieved at negative voltages above V_{reset} leads the device to HRS (reset transition). (**c**) Structure and (**d**) resistance-voltage characteristics of a PCM device. In PCM, crystallization of chalcogenide active layer at positive voltage below melting voltage V_m leads the device to LRS, while the melting and amorphization of active layer at voltages above V_m leads the device in HRS. (**e**) Structure and (**f**) resistance-voltage characteristics of an STT-MRAM device. In STT-MRAM, LRS and HRS are achieved depending on whether magnetic polarization in the free layer is parallel (P) or antiparallel (AP) aligned with the magnetic polarization in the pinned layer. (**g**) Structure and (**h**) polarization-voltage characteristics of a FERAM device where a residual positive/negative polarization is exhibited depending on whether the applied voltage is higher than $+V_c$/-V_c, where V_c is a coercive voltage. (Reprinted with permission from D. Ielmini et al. [6], Copyright 2018 Springer, Nature)

driven by drift and diffusion mechanisms in the opposite direction, leading to the rupture of CF and the creation of a gap region with low defect concentration, which results in a resistance increase. Resistance in RRAM devices can be tuned in gradual or analogue mode enabling RRAM to exhibit multilevel operation [89–92] which is extremely useful in neuromorphic applications. To this purpose, RRAM also offers high scalability [93] and 3D integration capability [94].

Figure 32.15c shows the structure of a PCM device where the resistance change relies on the phase transformation of an active material [95–98], typically based on a $Ge_2Sb_2Te_5$ (GST) chalcogenide [99] or high-temperature chalcogenide materials such as GeSb [100] and Ge-rich GST [101]. Chalcogenide active material can switch between two different atomic configurations called crystalline phase and amorphous phase, respectively. In PCM, the transition from crystalline to amorphous phase is achieved by a reset operation consisting of the application of an electrical pulse of amplitude higher than the melting voltage V_m, which leads to local melting within the active material, hence a resistance increase to HRS due to the pinning of Fermi level at the midgap [102]. On the other hand, the transition from amorphous to crystalline phase is triggered by a set operation consisting of the application of an electrical pulse of amplitude lower than V_m capable of rapidly inducing active material crystallization via Joule heating [102], thus leading the device to LRS. Resistive switching between two states is also shown by resistance-voltage (R-V) characteristics of PCM in Fig. 32.15d, where positive voltages below V_m cause a gradual resistance change from HRS to LRS due to the crystallization process whereas the application of voltages above V_m leads PCM from LRS to HRS via amorphization process, thus displaying a unipolar switching behavior. Compared to RRAM where the ratio between HRS and LRS is approximately of the order of magnitude of $10–10^2$, PCM exhibits a larger resistance window ranging from 10^2 to 10^4 [103]. This makes PCM very suitable for multilevel operation as demonstrated in [104] where the feasibility of 3 bits/cell PCM is investigated.

Figure 32.15e shows the MIM stack of a spin-transfer torque magnetic random access memory (STT-MRAM), referred to as magnetic tunnel junction (MTJ), where a tunneling insulating layer, typically in MgO, is sandwiched between two ferromagnetic (FM) metal electrodes, typically in CoFeB [105, 106]. STT-MRAM enables to store two resistance states, namely, LRS and HRS, depending on the alignment of magnetic polarization between the free FM layer, where its free polarization can be switched by a spin-transfer torque [107, 108], and the pinned FM layer, where the polarization is fixed [106, 109]. If magnetic polarizations of the two FM layers are parallel (P), a coherent tunneling of spin-polarized electrons is enabled within the MTJ, leading the device to LRS. On the contrary, in case of antiparallel (AP) alignment between free and pinned layer, spin electron tunneling is prohibited, thus leading the device to HRS [106, 109]. Figure 32.15f shows the R-V characteristics of an STT-MRAM device where the set transition from AP to P state takes place at positive voltage whereas the reset transition from P to AP state occurs at negative voltage. It is also noted that abrupt dynamics of set and reset transitions combined with a resistance window of only 200% due to the tunnel magnetoresistance (TMR) effect [110], makes STT-MRAM less suitable for multilevel operation with respect to RRAM and PCM. However, STT-MRAM device exhibits other attractive features including high scalability up to 11 nm [111], very high cycling endurance [112, 113], and fast switching speed [114] as a result of purely electronic nature of polarization switching process in FM free layer.

Figure 32.15g shows a ferroelectric random access memory (FERAM) device exhibiting a MIM structure with an insulating layer based on a ferroelectric (FE) material, such as $PbZrTiO_3$ (PZT) [115], $SrBi_2Ti_2O_9$ (SBT) [116] or doped HfO_2 [117], sandwiched between two metal electrodes [118]. The physical mechanism underlying FERAM operation consists of the switching of orientation of electrical dipoles in FE layer by application of external voltage pulses. Specifically, as shown by polarization-voltage (P-V) characteristics in Fig. 32.15h, the application of a positive voltage higher than a coercive voltage V_c at TE leads the device to display a positive residual polarization $+ P_r$ while a negative residual polarization - P_r is achieved in the FE layer as a negative voltage above V_c in absolute value is applied. Importantly, resistance does not depend on FE polarization in this device, which means that FERAM is not a resistive memory. However, FE state can be measured by probing displacement currents activated by polarization switching, thus enabling a read operation which is unfortunately destructive of previous state. This involves an overhead in terms of energy and time consumption.

32.5.2 3-Terminal Memristive Devices

Memristive concepts can also be implemented with 3-terminal devices, therefore showing more similarities with CMOS-type devices and additional functions with respect to 2-terminal devices. Figure 32.16 shows three examples of 3-terminal memristive synapses, namely, (a) the ferroelectric field-effect transistor (FEFET) [119], (b) the electro-chemical random access memory (ECRAM) [120], and (c) the spin-orbit torque magnetic random access memory (SOT-MRAM) [121].

The FEFET shown in Fig. 32.16a consists of a MOS transistor where the gate dielectric is based on a ferroelectric material, such as a perovskite [118] or doped HfO_2 [122]. In fact, 2-terminal memory devices based on ferroelectric

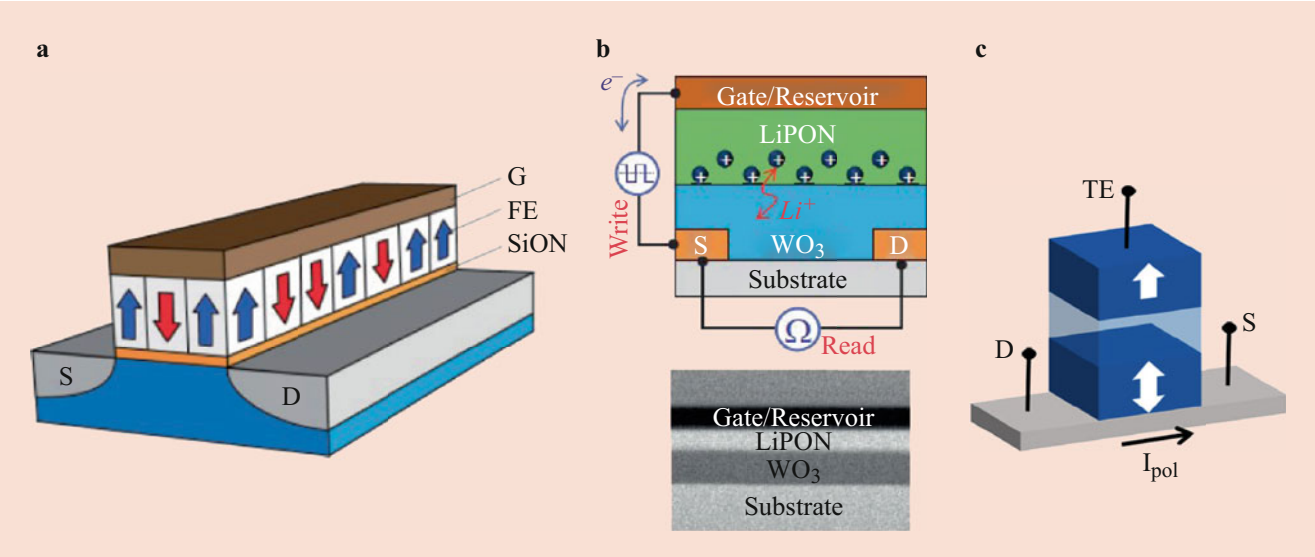

Fig. 32.16 Sketch of three types of three-terminal memristive devices used for synaptic applications. (**a**) Device structure of a ferroelectric field-effect transistor (FEFET), where the channel conductance (weight) modulation is achieved changing the threshold voltage via ferroelectric switching in FE material. (**b**) Device structure of an electro-chemical random access memory (ECRAM), where the channel conductance changes via migration of ionic species such as Li^+ in the electrolyte material due to the application of a voltage at gate terminal. (**c**) Device structure of spin-orbit torque magnetic random access memory (SOT-MRAM), where the MTJ resistance changes because of the magnetic polarization switching induced in the free layer by an in-plane polarization current flowing along the heavy metal write line. (Adapted with permission from H. Mulaosmanovic et al. [119], J. Tang et al. [120], D. Ielmini et al. [23]. Copyright 2017, 2018 IEEE)

capacitors suffer from difficulties due to transient read currents and destructive read [118]. In the FEFET, instead, the permanent polarization of the ferroelectric gate oxide results in a change of the threshold voltage of the transistor, which can be straightforwardly sensed by reading the drain current. The FEFET thus operates similar to a floating-gate memory, except that the ferroelectric material allows for relatively low operation voltage and high speed of polarization switching [123]. FEFET devices can be arranged in high-density arrays with 3D architectures [124], that make FEFET extremely attractive for neuromorphic approaches. FEFET have been employed for neuromorphic synapses [119, 125] and spiking neurons [126, 127]. As the device size is reduced to the 10-nm range, FEFETs increasingly display discrete levels associated with the presence of few individual ferroelectric domains within the small device area [128]. The single-domain effects of V_T might be a challenge toward achieving analogue conductance control of FEFET synapses.

The ECRAM device shown in Fig. 32.16b also relies on the transistor structure where the gate dielectric is replaced by a solid-state electrolyte for Li^+ ion migration [120]. Both inorganic materials, such as lithium phosphorous oxynitride (LiPON) [129] and organic materials as poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS) [130], were adopted as electrolyte materials. The migration of Li^+ ions into a $LiCoO_2$ channel causes a decrease in conductivity via Li reduction and intercalation [129]. Alternatively, the Li^+ intercalation in a WO_3 channel induced by an applied positive gate voltage was shown to lead to an increase in conductance (synaptic potentiation), while a negative gate voltage was shown to lead to a decrease in conductance (synaptic depression) [120]. Despite the incomplete physical understanding of the process, ECRAM usually displays very high linearity and symmetry of potentiation/depression processes, which satisfy the constraints for backpropagation training in supervised neural networks [8]. Potentiation/depression in the Li^+ ECRAM with WO_3 channel can be operated at the ns-scale, which makes this synaptic device extremely promising for high speed training of ANNs [120].

Figure 32.16c shows a SOT-MRAM device, which combines an MTJ used to sense the magnetic polarization in an FM layer, similar to the STT-MRAM device, with a heavy metal (HM) line underneath [121, 131, 132]. The HM line is usually made of Pt [133] or Ta [134] and serves for the programming of the MTJ in its parallel or antiparallel states. In fact, a horizontal current flow across the HM line causes a spin accumulation via the spin Hall or the Rashba effects [135], which in turn results in the magnetization switching of the MTJ free layer. The state of the MTJ can be sensed by the vertical current flowing across the MTJ via the TMR effect. Since the programming and reading current paths are decoupled, the device endurance can be significantly extended with respect to STT-MRAM, which is instead affected by MTJ degradation and breakdown due to the high field during the switching process. SOT-MRAM has been adopted to develop

synapses for ANNs [136] and associative memories [137]. SOT-MRAM based neurons were also developed taking advantage of the bistable switching in the MTJ via the HM current [138]. Other 3-terminal devices were also explored for neuromorphic computing, including 2D semiconductor-based mem-transistors [139, 140] and domain-wall-based magnetic memories [141, 142].

32.6 Neuromorphic Networks with Memristive Devices

32.6.1 SNNs with Memristive Devices

To embed learning function in memristive SNNs, STDP demonstration in hardware memristive synapses played a fundamental role. One of the earliest implementations at device level was demonstrated in [143]. In this work, synaptic conductance (weight) modulation was achieved in an Ag/Si-based conductive bridge random access memory (CBRAM), namely, an RRAM device where the CF creation relies on migration of metallic cations from an active Ag/Cu TE to the BE [144, 145], by using a time-division multiplexing scheme with synchronous time frames to convert the relative neuron spike timing Δt into the pulse-width of programming voltage pulses applied across the memristive synapse. To overcome the complexity of this scheme, another approach based on the overlap of voltage spikes with a suitably tailored shape at memristor terminals was developed in [146] and [147], which enabled the STDP functionality in PCM- and RRAM-based synapses, respectively. Based on this approach, brain-inspired SNNs with synapses employing various memristive concepts were simulated and realized in hardware by memristive crossbar arrays [148–152].

However, the implementation of this overlap-based programming scheme typically features some drawbacks. Although the use of a memristor as synapse allows to maximize the synaptic density in a hardware crossbar array, the application of long programming spikes limits network throughput. Also, the use of filamentary-switching RRAM synaptic devices necessarily requires a current compliance mechanism to avoid an uncontrollable CF growth during the potentiation process due to the positive feedback loop between CF size and migration driving forces [153, 154]. To solve these issues, some solutions based on novel materials and/or structures have been investigated. On the one hand, some memristive materials such as SiO_xN_y:Ag [155] and Ta_2O_{5-x}/TaO_2 [156] exhibit a diffusive dynamics enabling non-overlap programming, hence a non-overlap modulation of device conductance suitable for the implementation of a non-overlap STDP protocol. On the other hand, a novel hybrid CMOS/memristive structure where a memristive element is serially connected to a FET, also known as 1T1R structure, received increasing interest thanks to its ability to combine significant advantages for synaptic applications such as current limitation during potentiation, the independent control of communication and plasticity phases thanks to the additional terminal, and the suppression of sneak paths in crossbar arrays.

Figure 32.17a schematically shows a 1T1R structure where a FET is serially connected to an RRAM device with $Ti/HfO_x/TiN$ stack [39]. To achieve an electronic synapse, the 1T1R structure was operated in a neuromorphic circuit as the one depicted in Fig. 32.17b [41]. Here, the application of voltage pulses at gate terminal of FET activates the 1T1R structure enabling the transmission of a current spike proportional to RRAM conductance toward the input of the POST via BE since the TE is generally biased by a low voltage to allow for communication between PRE and POST. After entering the POST, the synaptic current is integrated by an integrate-and-fire circuit inside the POST leading to an increase in its internal potential V_{int}. As this increasing voltage becomes larger than a certain internal threshold, the POST emits a forward voltage spike being delivered to the next neuron layer and a feedback spike, based on a positive pulse followed by a negative pulse, being delivered at TE to implement STDP protocol in 1T1R RRAM synapse. STDP functionality in 1T1R RRAM synapse can be verified as follows. If the PRE spike arrives before the POST spike ($\Delta t > 0$), the PRE spike can overlap only with the positive pulse within the POST spike, thus leading to synaptic potentiation since the amplitude of the POST pulse V_{TE+} was designed to be higher than V_{set} (Fig. 32.17c). Otherwise, if the PRE spike arrives after the POST spike ($\Delta t < 0$), overlapping spikes lead the synapse to undergo depression since a negative voltage V_{TE-} larger than V_{reset} in absolute value is applied at TE (not shown). The application of this overlapping scheme for variable Δt and initial synaptic resistance R_0 resulted in the experimental STDP characteristics shown in Fig. 32.17d. Here, the relative change in conductance $\eta = \log_{10}(R_0/R)$ supports synaptic potentiation for $\Delta t > 0$ and synaptic depression for $\Delta t < 0$. Also, it should be noted that R_0 plays a key role since it dictates the amount of synaptic update. In the case of positive Δt, if R_0 is the HRS, 1T1R synapse undergoes maximum potentiation whereas if R_0 is the LRS, no change occurs since the synapse is already in LRS. In the case of negative Δt, if R_0 is the HRS, 1T1R synapse undergoes no depression because it is already in HRS whereas if R_0 is the LRS, maximum depression takes place. Note that the overlap window ranging from -10 ms to 10 ms makes that no conductance change can be achieved for $|\Delta t| > 10$ ms.

STDP implementation in 1T1R synapse with PCM or RRAM memristive element enabled simulation-based and hardware demonstrations of SNNs capable of fundamental neuromorphic tasks such as unsupervised learning/recogni-

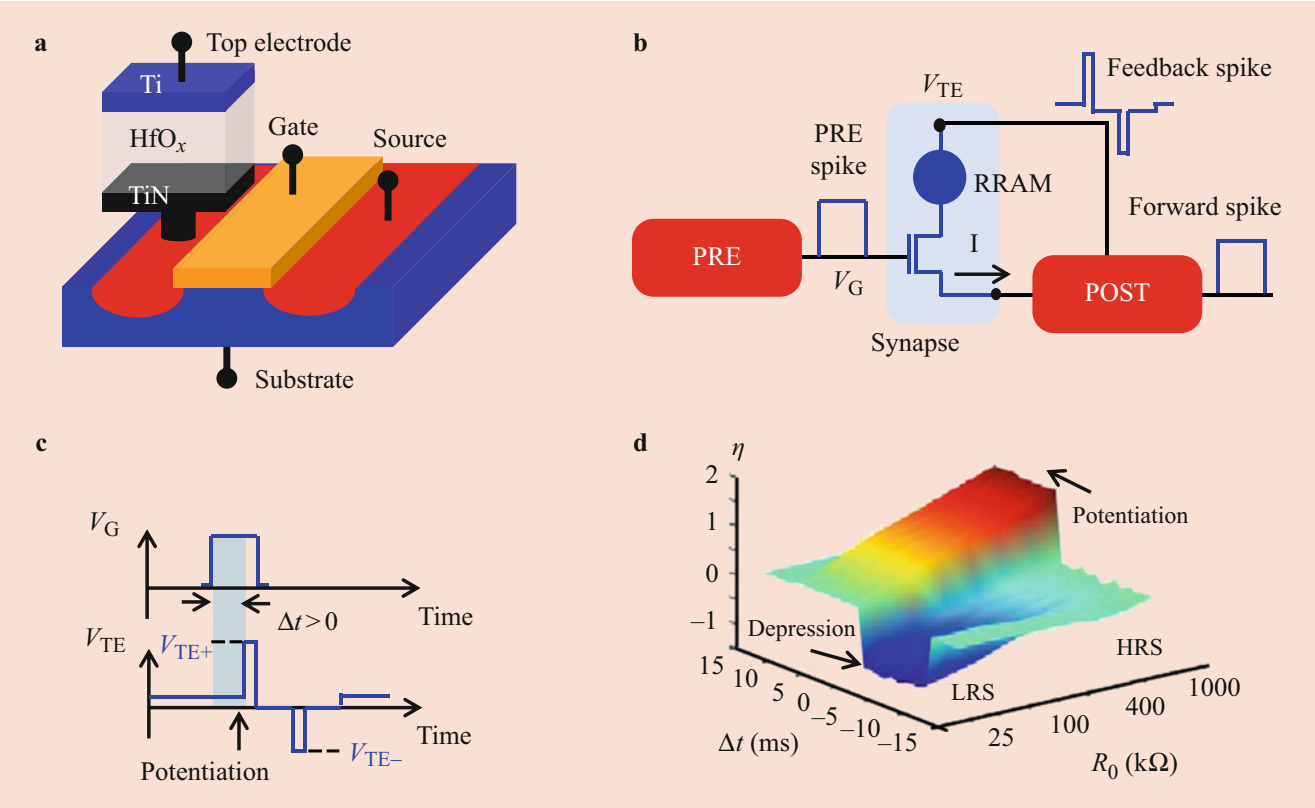

Fig. 32.17 (**a**) Sketch of 1T1R structure displaying a FET and a Ti/HfO$_x$/TiN RRAM used in serial configuration. (**b**) Schematic representation of a 1T1R structure used as synapse connecting a PRE with a POST. The application of the PRE spike at gate terminal activates a current within the 1T1R cell leading the internal potential of POST to increase. As the internal potential crosses an internal threshold, the POST fires a forward spike toward the next neuron layer and a suitably-designed feedback spike at synaptic TE to allow for the update of synaptic weight. (**c**) As the PRE spike anticipates the POST spike ($\Delta t > 0$), the PRE voltage overlaps with the positive pulse of the POST spike, leading the 1T1R synapse to undergo a set transition resulting in the synaptic potentiation. (**d**) 3D color map showing the relative change of synaptic weight $\eta = \log_{10}(R_0/R)$ as a function of the initial resistance state R_0 and the time delay Δt, evidencing that synaptic potentiation is achieved for positive Δt starting from high resistance states whereas synaptic depression is achieved for negative Δt starting from low resistance states. (Adapted with permission from S. Ambrogio et al. [39], Copyright 2016 IEEE, and G. Pedretti et al. [41])

tion of space [37, 39–41, 157, 158] and space/time [159] patterns and pattern classification [160–162].

Figure 32.18a shows the schematic representation of a perceptron neural network [15] where 16 PREs are connected to a single POST via individual synapses implemented by the 1T1R RRAM structure described in Fig. 32.17a. This network was implemented in hardware using an Arduino Due microcontroller (μC) to drive the PRE switches responsible for the generation of voltage pulses at the synaptic gates [41]. These spikes activate synaptic currents whose sum is integrated by μC, leading to the generation of a POST spike as a threshold is hit. At this point, depending on the relative time delay with PRE spikes, the POST spike applied at TE of 1T1R synapses can induce either synaptic potentiation or depression. Based on this network operation, unsupervised learning in hardware SNN was tested by the sequential submission of first three 4 × 4 images from left shown in Fig. 32.18b to the input layer. To achieve unsupervised learning, a stochastic approach consisting of random alternation with equal probability of the submitted input pattern and a random noise image, e.g., the last image in Fig. 32.18b, was implemented. This allowed to achieve depression in synapses outside the pattern, also called background synapses, as a result of the uncorrelation of PRE noise spikes after POST spikes. Figure 32.18c shows the color plot of measured synaptic conductance at the end of each learning phase starting from an initial HRS weight configuration, evidencing the network ability to adapt to submitted input within the end of each training phase, and to forget the previously stored pattern during the following phase. Figure 32.18d shows the sequence of PRE spikes within the submitted pattern and noise applied at input layer during the training experiment, and Fig. 32.18e shows the detailed time evolution of synaptic conductance during the experiment, which displays the convergence of pattern/background conductances to LRS/HRS at the end of each phase. Note that the application of the stochastic approach in this hardware SNN with 1T1R RRAM synapses also allowed to demonstrate both unsupervised

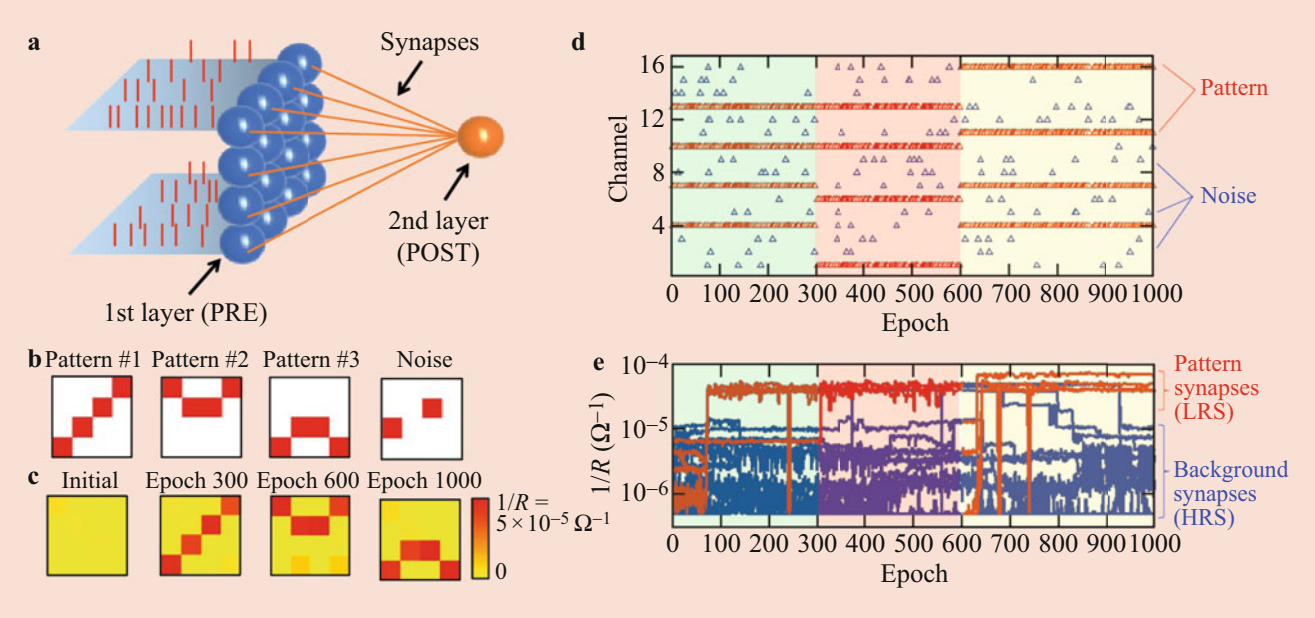

Fig. 32.18 (**a**) Illustrative scheme of a 4 × 4 perceptron neural network where every neuron of the input layer is connected to the single POST by individual synapses implemented by 1T1R devices. (**b**) Sequence of three 4 × 4 input patterns and an example of random noise pattern used during the pattern learning experiment. (**c**) Sequence of color plots displaying the evolution of synaptic weights into the perceptron network at epochs 0, 300, 600, and 1000. At the end of each training phase, the synaptic weights support the network ability to adapt to the pattern applied at the input. (**d**) Raster plot of PRE spikes applied to all the input channels during the pattern learning experiment evidencing the randomly alternated submission of pattern and noise images. (**e**) Evolution of experimental conductance within pattern and noise synaptic weights supporting the learning ability of the network via fast convergence of pattern conductance to LRS and slower convergence of background conductance to HRS. (Adapted from G. Pedretti et al. [41])

learning of competitive patterns thanks to the introduction of software-based lateral inhibitory synapses between two POSTs in the second layer and unsupervised learning of gray-scale images [41].

In addition to SNNs with perceptron architecture, 1T1R synapses were also used in recurrent SNNs to achieve another brain-inspired function as the associative learning [163–165]. Figure 32.19a shows the schematic circuit of the hardware recurrent SNN with Hopfield architecture [166] implemented in [163] where 10 neurons are connected by all-to-all bidirectional PCM synapses with 1T1R structure. To demonstrate associative learning capability, this network was trained submitting in sequence the two non-overlapping patterns shown in Fig. 32.19b, namely, by application of a voltage pulse to neurons within red pixels and no signal to the neurons within blue pixels. As shown in Fig. 32.19c, pattern submission leads the neurons within red pixels to fire causing the application of programming voltage pulses at both input, which controls the TE of column 1T1R cells, and output, which controls the gate of row 1T1R cells. The voltage signal overlap leads the PCM devices of 1T1R synapses shared by externally stimulated neuron pairs to undergo a gradual set transition, hence a synaptic potentiation process. By using this training approach inspired by biological Hebb's postulate [167], the network stores memory states linked with submitted patterns, also known as attractor states [168], which are evidenced by potentiated synaptic weights into the color map shown in Fig. 32.19d.

After the training phase, the Hopfield neural network is operated in the recall mode, namely, its memory states are tested by submitting incomplete versions of original patterns at the input. Fig. 32.19e displays the operation scheme of the neural network during the attractor recall phase, evidencing that an incomplete presentation of the Pattern 1 (no external stimulation at N_6) is able to reactivate N_6 by leading the input current I_6 to overcome $I_{threshold,6}$ thanks to the positive feedback in the attractor state dynamics. Also, Fig. 32.19f shows the spiking response of the Hopfield neural network during the recall of the Pattern 1, thus supporting that the submission of a partial version of original pattern without N_6 on-pixel leads the network to retrieve a sustained output spiking activity within all the attractor neurons after 9 epochs.

32.6.2 DNNs with Memristive Devices

Although the implementation of cognitive computing has recently made great progress thanks to hardware development of memristive SNN prototypes, this kind of neural network emulating brain learning is not yet able to match state-of-art

performance achieved by DNNs in emerging neuromorphic tasks such as pattern classification, recognition of faces and speech, and natural language processing [169]. DNN is a fully-connected neural network where the signal is forward propagated from input to output layer passing through many hidden layers. Differently from SNNs, which are based on unsupervised learning rules such as STDP and SRDP, the weight update in DNNs is generally executed by a supervised learning approach relying on backpropagation. This training method allows to optimize the synaptic weights minimizing a cost function after the iterative presentation of training dataset for many training epochs [17–19]. Implementing this scheme in hardware DNNs however introduces critical issues since the supervised weight update requires synaptic devices exhibiting a bidirectional conductance response with deterministic, linear, analogue, and symmetric behavior [170, 171]. In most cases, memristive devices including RRAM and PCM do not feature such characteristics [8, 170], even if recently investigated three-terminal memristive devices, such as the ECRAM [120] and the ionic floating-gate memory [172], display a conductance response very close to the ideal behavior. Nevertheless, many DNNs have been recently demonstrated in small/medium-scale hardware memristive crossbar arrays by exhibiting increasing performance in terms of processing speed and energy consumption for various applications such as pattern/face classification [173–180], feature extraction [181], and dimensionality reduction [181].

One the earliest experimental demonstrations of DNNs with memristive synapses was carried out in [174]. Figure 32.20a schematically shows the structure of three-layer DNN implemented in [174], consisting of an input layer with 528 neurons, a first hidden layer with 250 neurons, a second hidden layer with 125 neurons and an output layer with 10 neurons. While the synaptic weights were implemented using PCM devices, the neurons were implemented at software level as processing units converting the weighted sum of input signals into an output voltage driving the next layer by a hyperbolic tangent non-linear activation function. This network was designed to classify the handwritten digits of MNIST database which were cropped from 28 × 28 pixel size to 22 × 24 pixel size. As schematically depicted in Fig. 32.20b, network operation relies on the application of backpropagation rule as training scheme. According to backpropagation, the input signal x is forward propagated from input to output via hidden layers resulting in a local gradient δ given by the error signal calculated as the difference of the computed output vector x^D and the desired output vector g. Subsequently, the error term is backward propagated from output to input layer to adjust all the synaptic weights according to the weight update rule $\Delta w_{ij} = \eta \bullet x_i \bullet \delta_j$, where η is the learning rate parameter. To achieve this update rule, synaptic weights were implemented using 2 1T1R PCM cells by encoding the weight into the conductance difference G^+-G^- (Fig. 32.20c). In this way, by applying a complex overlap-based scheme where the weight increase/decrease is achieved by application of identical partial set pulses at G^+/ G^-, the 500 × 661 array including 165,000 PCM-based synapses was programmed. After the weight storage into the array, DNN classification accuracy was tested submitting unseen images from MNIST test dataset. Figure 32.20d shows the result of network operation in classification mode, evidencing a maximum test accuracy of 83% in both experimental test and software-based simulations. To significantly improve this classification performance strongly affected by non-linearity and asymmetry of PCM conductance response, a new synaptic device combining 2 1T1R PCM cells with a 3-transistor/1-capacitor (3T-1C) analogue conductance device was proposed in [179], which allowed to reach a hardware classification accuracy comparable with software performance on MNIST and CIFAR-10/CIFAR-100 datasets [182]. Since then, weight programming has been further optimized in the presence of PCM variability, asymmetry and non-linearity using PCM-only weight storage techniques [183].

The experimental demonstration proposed in [174] was followed by other memristive implementations which were however limited to very small crossbar arrays [175–178]. This limitation has been recently overcome in [180] where a two-layer neural network was implemented into a 1T1R crossbar array with 128 × 64 Ta/HfO_2/Pt RRAM cells. To achieve a classification performance on MNIST test dataset higher than 83%, an on-line in-situ supervised training scheme exploiting the linear and symmetric conductance response exhibited by Ta/HfO_2/Pt RRAM devices was developed (Fig. 32.21a). According to this scheme based on backpropagation, after calculating the desired weight update ΔW for every weight in the software, each weight change was programmed into the 1T1R array cells, increasing the device conductance ($\Delta W > 0$) via coupled application of suitable voltages at TE and gate terminals or decreasing the device conductance ($\Delta W < 0$) by application of a positive reset pulse at BE followed by a gradual set to reach the desired state.

Figure 32.21b shows the circuit schematic of neural network implemented in an 8-kbit RRAM crossbar array, which includes 64 neurons in the input layer, 54 neurons in the hidden layer, and 10 neurons in the output layer. This figure also shows that the weights were encoded by differential pairs of 1T1R RRAM cells while the neurons were implemented partly in software. After the training phase carried out on a MNIST training dataset including 8 × 8 gray-scale handwritten digit images, network inference was evaluated on MNIST test database, leading to a high experimental recognition accuracy of 91.71% (Fig. 32.21c). Also, the au-

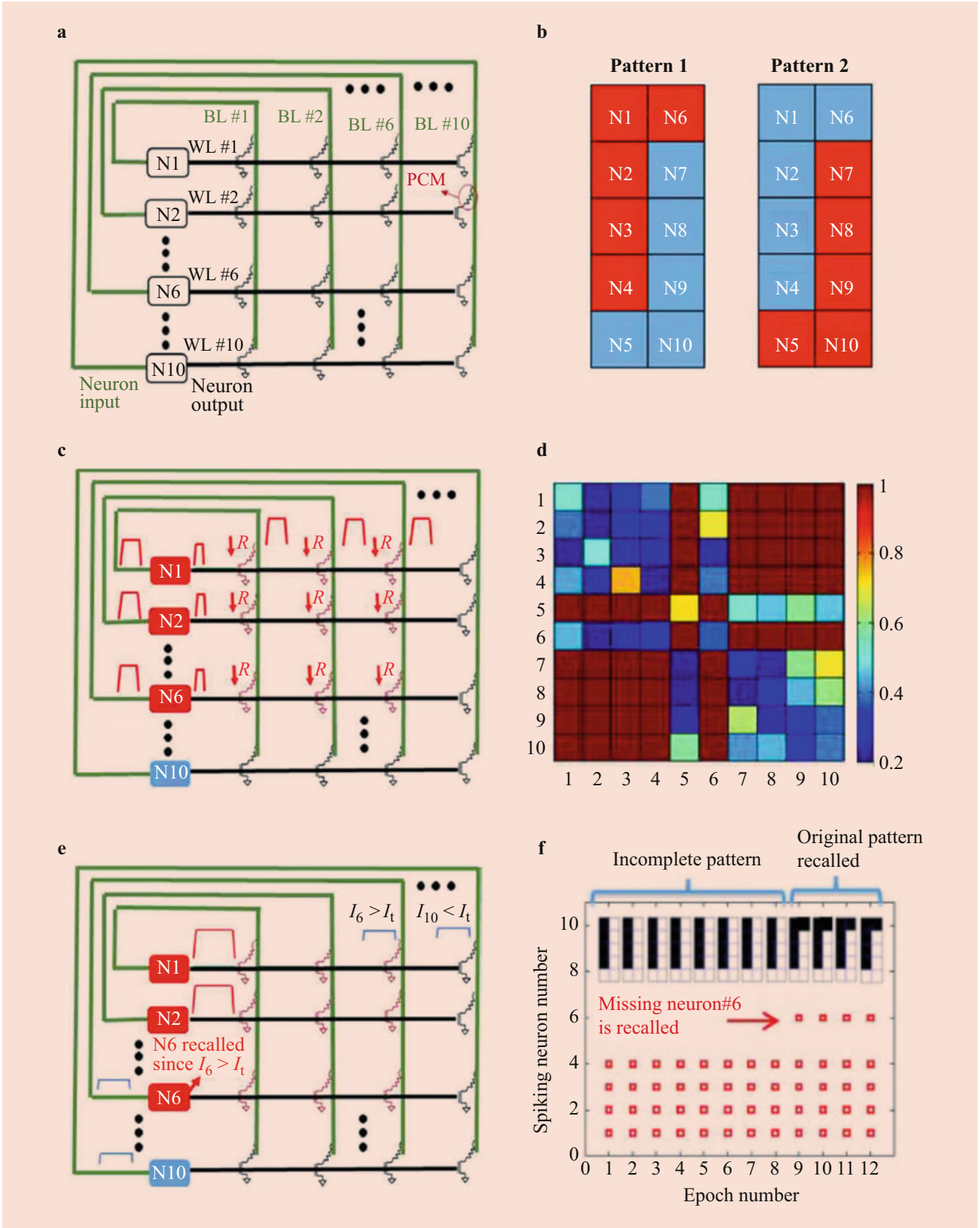

Fig. 32.19 (continued)

thors calculated a larger perceptron network in a 1024 × 512 RRAM-based crossbar array, demonstrating the possibility to achieve inference performance up to 97%. These experimental/simulation implementations thus support the adoption of analogue memristive devices in large memristive arrays as a fundamental step to bring inference performance in hardware closer to software performance.

Although on-line training of neural networks in crossbar arrays is a promising solution to achieve high inference accuracy, another approach aiming at combining high inference accuracy and low power consumption was recently explored in [184]. Here, MNIST classification was addressed by implementation of a two-layer perceptron neural network including 197 input neurons, 20 hidden neurons and 10 output neurons (Fig. 32.22a) in a 4-kbit RRAM array with $HfAlO_x$ 1T1R cells. After performing an off-line network training in software, the precision of synaptic weights was reduced to only 5 levels, thus obtaining a 5-level weight matrix being mapped into the array by application of a novel multilevel incremental step pulse with verify algorithm (M-ISPVA) capable of programming 5 levels in the RRAM devices [185]. Note that the storage of negative synaptic weights given by software simulations was experimentally obtained through the difference of a conductance G and a fixed reference conductance G_r, which provide a positive and negative current term, respectively, as schematically depicted in Fig. 32.22b. Figure 32.22c shows the experimental distributions of synaptic currents read at 0.5 V, evidencing some overlap for 5 programmable levels because of the variability affecting RRAM programming operation [186]. After array programming operation, the inference accuracy of neural network was tested in simulation using the experimental weights. The simulations returned a maximum classification accuracy of about 83%, which is supported by the corresponding confusion matrix collecting inference performance for each digit class (Fig. 32.22d). In addition to the competitive classification accuracy achieved despite the small size of array, this array level network implementation also exhibits low power operation as a result of the storage of synaptic weights into RRAM devices featuring a maximum conductance much lower than the maximum conductance of synaptic devices used in other network implementations such as that discussed in [180].

32.7 Discussion

The combination of good scaling behavior, nonvolatile storage, low-voltage operation, and physical MVM makes CMOS and memristive devices extremely promising for implementation of neural networks such as SNNs and DNNs. Some challenges remain however toward the development of neuromorphic hardware that can be industrialized at large scale. One of the major issues is the limited precision of the synaptic weight stored in the memory device. While digital computers can compute with arbitrary precision, e.g., 16- or 32-bit precision, nanoscale memory devices are affected by physical limitation in determining the conductance. For instance, the precision of the threshold voltage in a Flash memory is limited by the number of electrons stored in the floating gate [187]. Similarly, RRAM conductance is determined by a fixed number of defects that is associated to a certain level of stochastic variation [186]. In addition, some devices such as STT-MRAM can only store binary weights, while others can display drift or fluctuations of the analogue conductance [188, 189]. The limited precision of the synaptic weights results in an approximated MVM and a certain lack of accuracy in recognition, which requires alternative schemes for improved performance [179].

Besides their inherent physical limitations, memory devices could provide additional bio-inspired functionalities thanks to their unique physics. For instance, short-term and long-term memory effects have been evidenced in RRAM, where the retention time can be controlled by either the frequency of the applied spikes [190], or their current [191]. Short-term effects can support STDP [155], short-term memory and spatiotemporal pattern recognition [192]. Stochastic integrate-and-fire neurons have also been proposed based on volatile RRAM [161] and paramagnetic MTJs [193]. These results support the ability to describe relatively complicated functions, such as a stochastic spiking neuron or an STDP synapse, with a single device instead of a circuit with large-area CMOS transistors and capacitors. From this standpoint, the combination of various materials and device concepts is extremely promising, as a wider portfolio of physical properties can be implemented in a single circuit. For instance, the combination of an MTJ neuron and a memristive synapse

Fig. 32.19 (**a**) Circuit implementation of a Hopfield recurrent neural network based on 10 neurons connected with each other by bidirectional 1T1R PCM synapses. (**b**) Input patterns sequentially submitted to the network during the training phase. (**c**) Schematic representation of training phase where externally stimulated neurons fire output spikes overlapping input spikes, leading to potentiation process within 1T1R PCM synapses shared by firing neuron pairs. (**d**) Color plots of synaptic weights after training displaying storage of two memory states linked with submitted patterns. (**e**) Schematic representation of recall phase where the input submission of a partial copy of a training pattern leads the neurons within original patterns with no external stimulation to retrieve their firing activity thanks to the attractor dynamics in the network. (**f**) Recall demonstration at network level using an input pattern without N_6 stimulation. (Adapted from S. B. Eryilmaz et al. [163])

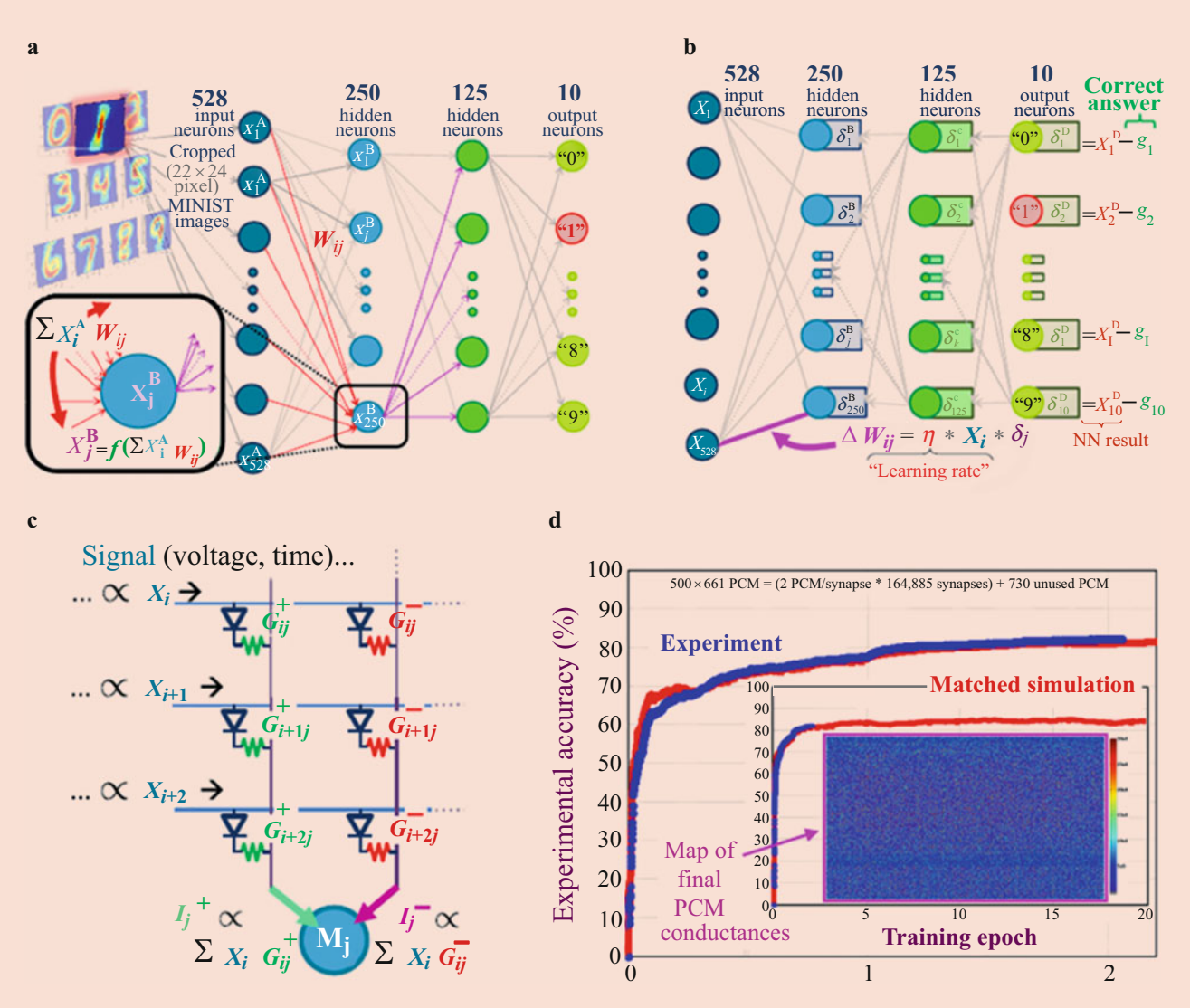

Fig. 32.20 (**a**) Schematic representation of a three-layer DNN for MNIST classification task where every software neuron converts the sum of input currents into a voltage by application of tanh activation function. (**b**) Schematic explanation of backpropagation rule used to train the DNN on MNIST dataset. Input submission leads the output layer to generate an output response which is compared with the correct answer given by input label. The result of this comparison, called error signal, is then backpropagated from output to input layer to calculate the correction term for every weight via the backpropagation weight update rule. (**c**) Schematic representation of the synaptic weight implementation via a differential scheme encoding the weight into the difference of two conductances. (**d**) Experimental and simulated test accuracy achieved in the three-layer DNN with 1T1R PCM synapses. (Adapted with permission from G. W. Burr et al. [174], Copyright 2014 IEEE)

[138] or the combination of a volatile RRAM neuron and nonvolatile RRAM synapses [161], have been proposed for small area, energy-efficient neuromorphic networks.

Finally, it is worth noting that neuromorphic circuits are not limited to applications in cognitive systems to mimic the human brain but can also be applied to a large range of computing problems. It is known, indeed, that recurrent Hopfield networks can support the solution of constraint satisfaction problems (CSPs) such as Sudoku [194], Max-Cut [195], and the Ising spin-glass problem [196]. Hardware accelerators of CSPs have been previously developed by adopting CMOS neuromorphic circuits [197], FPGAs [198], and quantum computing circuits [199]; however, resistive/memristive devices enable the implementation of neural networks in crossbar arrays and provide an intrinsic noise which is essential for the stochastic simulated annealing within the recurrent network [200]. Given the ubiquity of CSPs in many practical fields, such as industrial logistic and scheduling, the neuromorphic computing appears as a valid technology to address real-life problems. Also, very recently it has been

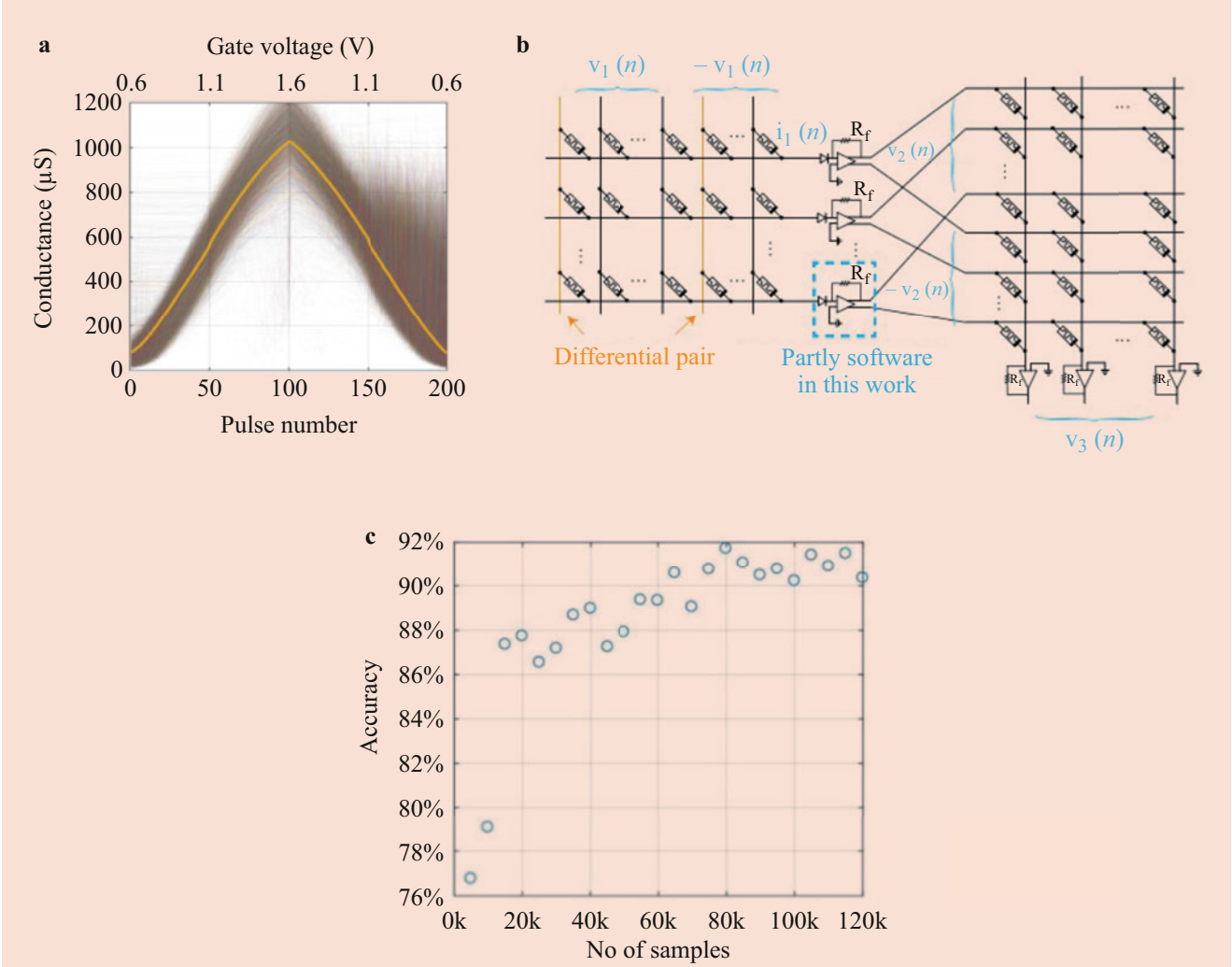

Fig. 32.21 (**a**) Conductance response of Ta/HfO_2/Pt RRAM devices for increasing number of pulses and V_G exhibiting high linearity and symmetry in both directions. (**b**) Schematic representation of the two-layer perceptron network used for MNIST classification task, where neurons are implemented in software whereas the synaptic weights are encoded in differential conductance pairs. (**c**) Classification accuracy on MNIST test dataset achieved by an 8-kbit perceptron using experimental weights after an on-line in-situ training. (Adapted from C. Li et al. [180])

shown that memory arrays with a negative feedback loop, similar to a Hopfield network, can support the solution of general-purpose linear matrix problems, such as linear systems, eigenvector problems, and matrix inversion, in only one computational step [12]. This is a further demonstration that memory devices may have a strong impact on future computing technologies, thanks to physical, analogue, and parallel computing properties.

32.8 Conclusions

This chapter presented the current status of neuromorphic computing based on memory devices, including CMOS and memristive devices. Memory arrays can support the major types of neural networks, namely, DNNs and SNNs, thanks to the unique physics and strong scaling potential of the memory devices. Applications range from typical artificial intelligence tasks, such as recognition of images and speech, to general purpose computing, such as CSPs and linear matrix problems. CMOS/memristive technologies thus appear as a major enabler for the development of scalable, energy-efficient neuromorphic computing systems.

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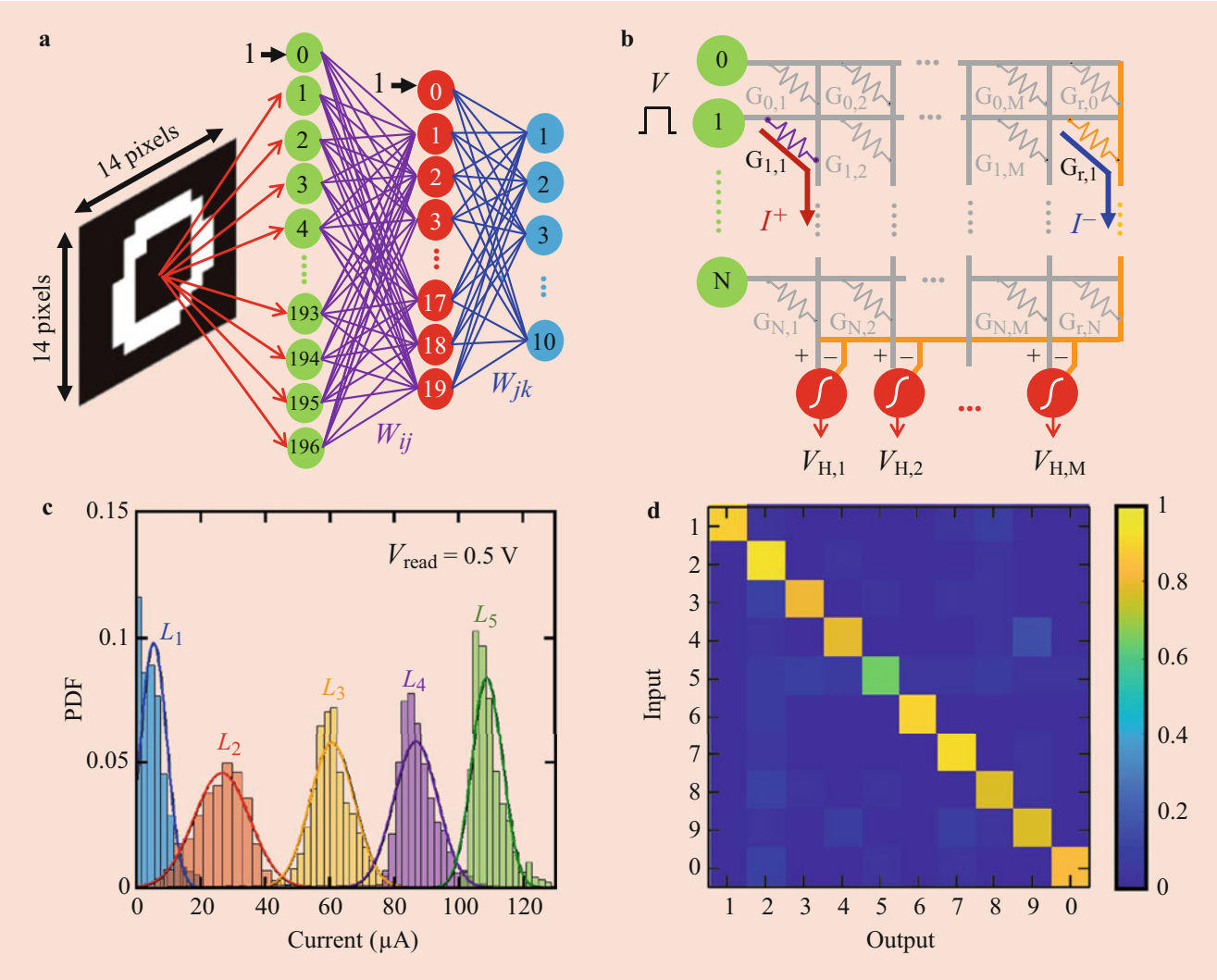

Fig. 32.22 (**a**) Sketch of a two-layer perceptron network implemented into a 4 kbit RRAM array for MNIST classification task. (**b**) Illustrative scheme of synaptic weights connecting the input layer with the hidden layer. In this implementation, each weight is encoded in $G - G_r$, where G_r is a conductance used as reference. (**c**) Experimental distributions of 5 discrete levels programmed into the array after the software-based training phase. (**d**) Confusion matrix showing the classification accuracy achieved for each digit class during an inference simulation with experimental weights. On average, classification accuracy is 83%. (Adapted from V. Milo et al. [184])

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Nanoelectronic Systems for Quantum Computing

33

David K. Ferry

Contents

33.1 Introduction 1201
33.1.1 Moore's Law 1202
33.1.2 Where the Industry Appears to Be Going 1202
33.1.3 New Computational Models: Quantum Computing 1203
33.1.4 State of the Art in Quantum Computing 1203

33.2 Qubits and Entanglement 1204
33.2.1 Bits and Qubits 1204
33.2.2 Qubits as Two-Level "Atoms" 1205
33.2.3 Entanglement 1207

33.3 The Silicon Qubit 1208

33.4 The Josephson-Based Qubit 1209
33.4.1 The Charge Qubit 1211
33.4.2 The Flux Qubit 1212
33.4.3 The Hybrid Charge-Flux Qubit 1212
33.4.4 Coupling Qubits 1213

33.5 Integrated Optics 1213
33.5.1 The Jaynes-Cummings Model 1215
33.5.2 Qubits 1216
33.5.3 Qubits and Gates 1217

33.6 Other Qubits 1218
33.6.1 NV Centers 1218
33.6.2 Braiding 1220
33.6.3 Surface Bonds 1222
33.6.4 Flying Qubits 1222

33.7 Summary and Conclusions 1223

References 1223

Abstract

Nanoelectronic systems have driven the technology advances for the past half century. But, as we move forward in the twenty-first century, new concepts for computing, notably quantum computing, have appeared that promise dramatic increases in computational efficiency. While these are new systems concepts, they likely will continue to be manufactured using the technology of nanoelectronics. Here, we discuss a variety of approaches which are currently being studied for applicability to quantum computing. But, issues such as scalability, which has facilitated the development of nanoelectronic systems so far, pose important questions for these new and novel approaches.

Keywords

Quantum computing · Entanglement · Superconducting qubits · Spin qubits

33.1 Introduction

The initial idea of constructing a computing machine dates at least to the analytical engine of Charles Babbage at the middle of the nineteenth century. But, it was the theoretical work of Alan Turing in the 1930s that pushed the ideas forward [1]. This led to efforts at many sites to develop computing machines, with commercial development following after World War II. The key driver for nanoelectronics appeared with the invention of the integrated circuit in the 1950s by Jack Kilby [2]. This latter invention enabled the rapid development of integrated circuits with ever smaller critical dimensions and the evolution of what has become known as Moore's law [3]. In this, Moore suggested that the number of transistors on an integrated circuit would continue its trend of doubling every 18 months, leading to the exponential growth that allowed first microelectronics and then nanoelectronics to revolutionize everyday life throughout the world. The physical approach which allowed this was the principles of scaling that applied to the integrated circuits [4]. The scaling approach was based upon the principles that all dimensions

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and voltages of a device should be reduced by the exact same factor, so that the electrostatics of the device would be unchanged. As a result, the reduced dimensionality did not, in principle, change device operation as it was downsized. This little overlooked fact meant that integrated circuit was a scalable technology, and this scalability led to the impact of nanoelectronics on the world [5].

33.1.1 Moore's Law

For almost six decades now, evolution in the integrated circuit has continued to follow Moore's dictum on the development of this technology. This steady progress has brought us to the situation today, where the newest leading edge chips are known as the 5 nm generation. While this nomenclature is no longer applied to the most critical dimension, the channel length, it is still an indicator of the progress being made as we move from one generation to the next. While many have predicted the end of Moore's law, we still move on with this scalability of the technology. This has occurred through a number of paradigm shifts, from the planar MOSFET to the tri-gate or FinFET to nanowire FETs. Many, if not most, people have regarded Moore's law as a technology law simply because the most evident appearance is associated with the microprocessor. Many other technologies follow such evolutionary laws. And, the important point is that *Moore's law is, in fact, an economic law*!

In its original version, Moore's law was driven by three technological factors: (1) reducing the transistor size (and therefore the silicon area occupied by it) with the scaling factor, (2) increasing the size of the microchip itself, and (3) circuit cleverness (by which the number of transistors required to perform a given function could be reduced). The key, however, lies in the fact that the cost to manufacture a single integrated microprocessor (i.e., the cost per square centimeter of the chip) has not significantly changed in the last six decades. The reduction in size means that many more transistors, and many more functional units, can be placed on a single chip, resulting in the cost per functional unit decreasing exponentially with time. In the 1970s, the new supercomputers, such as the Cray, cost 10s of millions of dollars. The fact that such a computer can be placed on a single chip (many times over) today suggests that such a computer could be built for less than a single dollar today. In fact, the modern laptop has thousands of times more computing power than that first Cray. Even the modern personal phone has significantly more computing power than that first Cray. It is this economics argument that drives Moore's law, and it is scalability of the technology that enables such an economics driving force. And this leads us to the conclusion that if any new technology is to prove useful, it must be scalable.

33.1.2 Where the Industry Appears to Be Going

Scaling theory involves not just reducing dimensions and voltages, but also the introductions of new technologies along the way. For example, Intel introduced HfO_2 as a new gate insulator with the 45 nm generation, because of its higher dielectric constant. This allowed the use of thicker insulators for the gate dielectric while maintaining the equivalent thinner electrical thickness of SiO_2. Then, they introduced hyper-threading with the 35 nm Xeon processor, which meant that each node could process at least two data threads. Thus, a six-node, hyper-threaded chip could achieve something close to a 12× speedup in processing. Then, they introduced the new tri-gate, or FinFET, technology at the 22 nm node, which turned the transistor on its side. Instead of being planar, it was now vertical with the gate wrapped around the top and two vertical sides. This meant that a much larger gate periphery (width) could be obtained at a smaller net silicon surface area. This was done primarily to reduce the off-state leakage current and resulted in much lower power dissipation on the chip. Today, we are at the 5 nm node, although there have been significant delays in introducing the new chips (as of early 2018) [6]. Even today, the technology for this node is still being developed and discussed. Nevertheless, the device technology for this node is still being discussed. Nevertheless, TMSC has announced production of their this chips [7], and ARM and Cadence are planning to use these chips [8]. Indeed, the new (2021) iPhone 11 uses a 15 nm chip, the ARM A15, which is produced by TSMC using EUV lithography. This chip has eight nodes and utilizes neural net technology for some of the phone's learning processes. On the other hand, Global Foundries have stopped their planned production of 7 nm chips, allegedly for the lack of demand on the part of users [9].

The industry may be at a crossroad for another technological change, and this may involve a move to nanowires fabricated in a gate-all-around technology, where the gate wraps completely around the nanowire. This has been studied in research labs for almost two decades. Nanowires placed parallel to one another on the surface of silicon are not an attractive approach. This is because, if we are to save silicon surface area, the nanowire has to have a large diameter, and this means that it cannot compete with the FinFET in saving Si area and achieving high circuit density [10, 11]. But, another approach is possible, and that is to stack the nanowires vertically [12], an approach which is being developed by many companies [13, 14]. Subsequently, these wires have been made by a variety of techniques, including inductive plasma etching [15], nano-stencil lithography [16], and reactive ion etching [17, 18]. Naturally, there have been studies to see how these devices compared with others such

as SOI MOSFETs [19] and FinFETs [19–21]. At this node, there is also a consideration whether or not to incorporate doping in the channel region, and this has been studied as well for the vertical stacked nanowires [22, 23]. As may be expected, there is certainly a problem with line edge roughness on these nanowires [24–27]. But, perhaps the best sign that this technology is ready for prime time applications is the entry of the major semiconductor producers into the field [28].

33.1.3 New Computational Models: Quantum Computing

The idea of using quantum mechanics to provide more power than classical computers seems to have begun around 1981–1982 [29], but Deutsch put the concept on a sounder footing a few years later [30]. Deutsch reformulated the Turing thesis with the assertion that every finite realizable physical system can be perfectly simulated by a universal model computing machine operating by finite means. However, he pointed out that the output of a quantum machine, although fully determined by the input state, is not an observable itself. Hence, the user must provide some cleverness if this state is to be determined. Benioff in his earlier work pointed out the need for this quantum state to have experienced interference, some indeterminism, and was a non-separable state. Today, we would assign these properties to the presence of entanglement in the quantum state, and Deutsch realized that quantum parallelism was required of such a computer. He also realized that non-dissipative evolution was unphysical, so immediately it became clear that a great deal of effort would be required to minimize the decoherence of the physical states. Deutsch then provided some input as to what type of states or systems might be usable in this process [31]. Jozsa mathematically showed that one could associate a quantum state with each function that one desired to evaluate [32]. This evaluation needed to be a superposition of the various quantum states, with the particular superposition labeled by the desired function. Jozsa and Deutsch were then able to show that this should lead to a rapid solution of problems via the quantum computer [33].

Progress beyond mathematical approaches came shortly after the above when Lloyd suggested that arrays of weakly coupled quantum systems might be able to serve as the quantum computer if they were subjected to a sequence of controlled electromagnetic pulses, which could place the quantum bits into the desired superpositions [34]. This shifted the problem to arranging for the superpositions, and this required algorithms. Perhaps the first such algorithm came from Peter Shor [35, 36] who introduced the idea of the quantum Fourier transform in dealing with numbers generated by the product of prime numbers, a key element in many encryption techniques. Another for fast data base searches was developed by Grover [37]. Sometime, however, the algorithms stimulate rethinking classical approaches by which the new classical approach is just as fast [38].

By the mid-1990s, progress was beginning to speed up in the quest for quantum computers with suggestions for realizable gates and their universality [39–41]. Nevertheless, it was realized that even small amounts of dissipation could upset the computation, and the need for error correction began to be addressed [42, 43], although there are some who assert that general qubit errors are not completely correctable [44]. There has been considerable discussion and debate since the beginning about whether or not error correction will work and even if quantum computing will work [45–49]. Nevertheless, progress has continued and is even accelerating. We will discuss the current (2018) situation with respect to the interests of various companies in the next subsection; it is worth pointing out that much of the discussion has not turned to "if," but to "when." In fact, a recent article has raised the issue of "quantum supremacy," the point at which performing a quantum computation on a quantum computer will prove to be beyond the capabilities of any classical computer [50]. While the processes discussed here are necessarily dated, they can point the way to find the newer, updated results.

33.1.4 State of the Art in Quantum Computing

The quest for quantum computers begins with the qubits. We will describe qubits and their difference from bits in the next section, and the following sections will describe various types of qubits that are in use. Before taking up this task, however, it is worthwhile to examine the approaches which builders of quantum computers have taken, as this particular area has had exponential growth in just the last few years. As a result, it is important to understand that this brief section is the state of the art in late 2018, and it may well change within a few short years. Some more recent developments are also mentioned.

D-Wave Systems delivered the first quantum computer in 2010, but this had an architecture different from a general purpose machine. It was instead focused on an energy minimization structure that is used for what is called artificial annealing. Nevertheless, the machine has been used by several commercial firms. In 2018, D-Wave introduced a 2000 qubit machine using the same architecture. The qubits themselves are made from superconducting circuits with Josephson junctions. More importantly, they launched this same year a real-time application (programming) environment called Leap.

The best known name in the area is IBM, who has become a leader in the field. In fact, they provided web access to their first five-qubit machine so that researchers and

developers could begin software efforts. To aid this, they provided a modular open-source programming environment called Qiskit. More recently, they have developed a 20 qubit machine and later a 50 qubit machine using superconducting Josephson junction technology. In fact, nearly all the companies involved in quantum computers are currently using this approach. One of these is Alibaba, a Chinese company, who has an 11 qubit machine. Google has announced a 72 qubit processor, and Intel has recently announced a 49 qubit chip. Quantum Circuits and Rigetti are also developing qubit systems with the superconducting Josephson technology. Importantly, in 2019, IBM attached their quantum processer to one of their main stream supercomputers, in order to gain information of the usage of the quantum processor. As a result, IBM now claims that about 100 companies have gained experience with quantum computing. In addition, this has changed the focus for future development from the science of the qubit to the algorithmic nature of the circuits themselves.

There are some differences with other manufacturers, however. Intel has developed a 26 qubit processor in which the qubits are built upon the idea of using spin as the logic variable. This chip has qubits which measure only 50 nm across and are quite scalable. IonQ is developing qubits based upon trapped ions, in which an atom is trapped in an electromagnetic confinement environment and the logic state rests in the state of the atom. Then, Microsoft seems to be focusing upon systems composed of topological materials [51], a relatively recently developed, and still not fully understood, class of materials. Here, the interaction between the qubits depends upon what is called braiding [52] approaches which control the phase between the qubits.

For quite some time, there was a belief that quantum supremacy could be achieved if only we could reach 50 qubits in the system. The above discussion shows that while we have reached this number of qubits, the issue of quantum supremacy is still in the air. In late 2019, Google claimed to achieve quantum supremacy with their 53 qubit processor [53]. However, this claim was challenged by several competitors, notably IBM. This is complicated by the fact that IBM has carried out simulations of a 49 qubit system on a classical computer [54], which suggests that we are in fact quite far from reaching the needed supremacy. Similar simulations on 64 qubits have also been performed on normal computers [55]. This should not be viewed negatively, as there is absolutely no doubt that the quest for quantum supremacy will continue with the development of ever larger numbers of qubits, especially as a path has been given [50].

Then, we should ask once again our question about scalability. While the size of the chips discussed above, in terms of the number of qubits, is certainly increasing, mostly, the actual chip size is increasing, and it is not clear whether or not the qubit density is increasing. So, it would seem that the issue of scalability seems to not yet be answered. And, the systems listed above all seem to be of a relatively low number of qubits. This, by itself, is not an issue per se, as modern classical computers are not composed of massive number of bits in their central processing unit (cpu). Indeed, a 64 bit arithmetic computer tends to have a few registers, each of 64 bits, and some control hardware within the cpu. Thus, in the IBM experience, the five qubits were basically the cpu and were used multiple times within the computation. Even so, there are issues that have been raised. Michielsen et al. [56] have pointed out that for a device that maps input data to output data via an algorithm to qualify as a computer, it must achieve two things: (1) for each instance of the input data, the output data should be the correct output data, and (2) for the same input data, the output data should be unchanging when the machine is in the stationary state. These authors have run several algorithms on the IBM Quantum Experience with 5 qubits and find that this machine often fails these tests. In some cases, failure arises for the same algorithm and input data run on different days. These authors offer some explanations as to why this might be the case, but it is nonetheless quite worrying if we are expecting to enjoy the success of quantum computers.

But, there are other problems on the horizon, and these deal with the accuracy, or more precisely the errors, in the quantum computation. It was pointed out above that this leads to erroneous results in some calculations on the current qubit processors. Certainly, error correction can help, but there are doubts among many of the researchers if the required size of the quantum computer can ever be achieved while still maintaining the required accuracy of the calculation using what are basically analog qubits. It is an important issue that is still the subject of intense debate [57].

33.2 Qubits and Entanglement

While it may not appear to be the case, with the similarity of name between bit and qubit, these two quantities are basically quite different. To begin with, the normal bit, the basis of our binary computation in everyday classical computers, has only two values, 0 and 1, which form the binary base. While the qubit also has a 0 and a 1, it is analog in that we may define arbitrary complex values in any manner in which the magnitude of the qubit remains 1. In this section, we want to go through this idea in some detail to understand how we get to qubits with the properties required to make quantum computers.

33.2.1 Bits and Qubits

When the ENIAC was first developed at the University of Pennsylvania, it computed with base-10 circuits [58]. The simplest operation, the addition of two numbers took 0.2 ms.

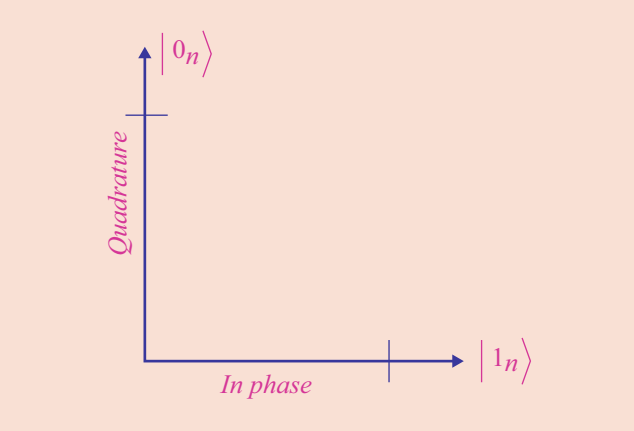

Fig. 33.1 The coordinate set for an arbitrary bit, here the *n*th bit, showing how the axes correspond to the values 0 and 1

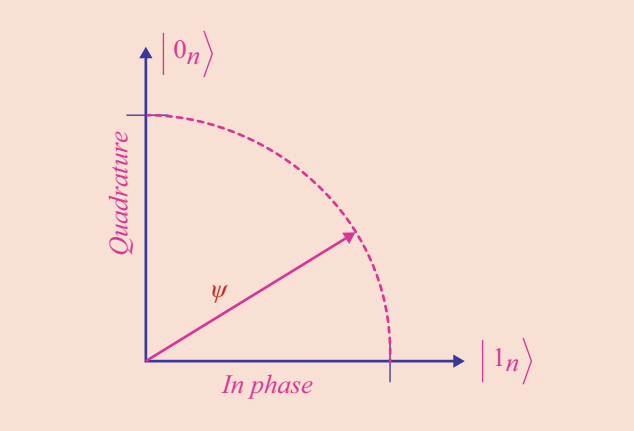

Fig. 33.2 The value of the qubit now is analog and the magnitude of the wave function is now unity

But, calculation in base-10 is somewhat wasteful of computer resources. It was John von Neumann who suggested that the binary system should be used (and he also suggested the stored program approach, which along with binary arithmetic, formed the idea of the von Neumann architecture [59], and both were incorporated in the EDVAC which was the successor to the ENIAC). Essentially, all computers from this time forward have used the binary system, as it is eminently suitable to two-state bits. In Fig. 33.1, the idea of the bit/qubit is presented in as two orthogonal axes in a configuration space (for reasons that will become apparent later). In this space, we define the two unit values on each axis as the states 0 and 1. Then, using quantum notation, we define the state of a classical bit in this space as

$$|\psi\rangle = a\,|0\rangle + b\,|1\rangle\,, \tag{33.1}$$

where

$$a, b \subset (0, 1)\,, a + b = 1. \tag{33.2}$$

Hence, a and b can be either a 0 or a 1, but the two must be different.

In the computer itself, a particular state is defined by the values of the bits used to describe the state. Then, one can define a state transition diagram, in which each possible state is a node, and transitions between these nodes indicate the action taken when a control signal is applied. Various outputs arise from the set of transitions and the state of the machine after the transition. Hence, an algorithm is a set of instructions that guide the system through a set of transitions, changing the various bits under the guidance of the control signals, to a desired result. Good algorithms lead to the machine halting at the end of the algorithm and yield a desired output (and with bad algorithms, the machine sometimes never stops). This same operational model will exist also in the quantum computer. That is, the qubits will define a state; state transitions will depend upon control signals.

33.2.2 Qubits as Two-Level "Atoms"

When we move from the bit to the qubit, the change is rather subtle. We use the same diagram of Fig. 33.2 for the qubit. We still have the two coordinate axes representing the 0 and the 1. But, now the wave function is analog and can take any value on the unit circle. Hence, Eq. (33.1) is still valid, but now the coefficients are related by

$$|a|^2 + |b|^2 = 1. \tag{33.3}$$

Thus, the two coefficients may be complex numbers, and Eq. (33.3) tells us that the net wave function must have a magnitude of 1, the sum over the phase space of the square magnitude of the wave function must be unity, due to its probability interpretation. Now, the problem that arises is that this formulation is overly *restrictive* to the actual wave function for the quantum qubit.

The two states 0 and 1 can be thought of as representing real energy levels of a two-level atom (we will return later to why we use the atom model). Equally well, they can be thought of as the two possible spin states of a fermion – spin up and spin down. Normally, these are aligned along the Z-axis in spherical coordinates. From the latter concept, we then tend to write the Hamiltonian representing this two-level system as

$$H = \frac{\Delta}{2}\sigma_z, \tag{33.4}$$

where Δ is the energy spacing between the two levels and σ_z is a Dirac spinor, given by the 2×2 matrix

$$\sigma_z = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}. \tag{33.5}$$

Hence, we have mapped the (0,1) states into the states (−1,1), in terms of $\Delta/2$. Hence, the upper level is taken to be the 1 state and the lower level the −1 state. In terms of these two states, we can then rewrite the wave function as

$$\psi = \begin{bmatrix} a \\ b \end{bmatrix} = \begin{bmatrix} |a| \, e^{i\phi_1} \\ |b| \, e^{i\phi_2} \end{bmatrix}. \tag{33.6}$$

So, each coefficient has its own phase, which we will deal with shortly.

Now, it is convenient to write the wave function in a slightly different form which characterizes the system, but make the two phases somewhat less arbitrary. Hence, we write the two-level system in terms of the density matrix

$$\rho = \begin{bmatrix} |a|^2 & ab^* \\ a^*b & |b|^2 \end{bmatrix}, \tag{33.7}$$

from which we infer that, from Eq. (33.3), we can write

$$\text{trace}\,(\rho) = 1. \tag{33.8}$$

It is a property of two-level systems that we can define the density matrix slightly differently by using the full set of the Dirac spinors. In this approach, we introduce the polarization **P** and write Eq. (33.7) as

$$\rho = \frac{1}{2}\,(I + \mathbf{P} \cdot \boldsymbol{\sigma})\,, \tag{33.9}$$

where I is the unit matrix and the vector $\boldsymbol{\sigma}$ has the components $\sigma_x, \sigma_y, \sigma_z$. Thus, we are able to write the three component of the polarization as

$$P_x = 2\text{Re}\left(a^*b\right)$$

$$P_y = 2\text{Im}\left(a^*b\right). \tag{33.10}$$

$$P_z = |a|^2 - \lceil b \rceil^2$$

The language in the above description of the density matrix gives the polarization in the real three-dimensional space. But, we can think of the polarization itself as a vector in an abstract three-dimensional Euclidean space. In this space, the state 0 is a unit vector pointing in the $+z$ direction, while the state 1 is a unit vector pointing in the $-z$ direction. The polarization itself resides on the unit sphere in this space; this unit sphere is called the *Bloch sphere*. Such a Bloch sphere is shown in Fig. 33.3, and the two angles are defined as the polar angle and the azimuthal angle, where the former is the angle away from the $+z$ axis, and the latter lies in the (x,y) plane and is measured from the X-axis, as is normal for spherical coordinates. This many qubit operations are easily expressible as rotations around the three axes.

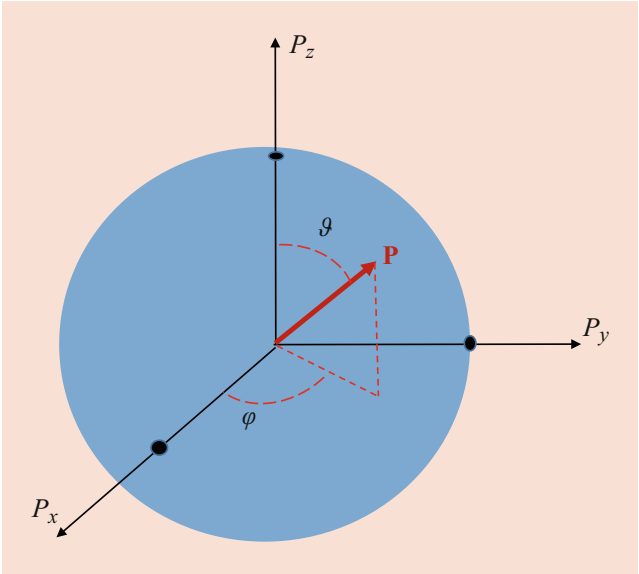

Fig. 33.3 The Bloch sphere allows the polarization to rotate in three directions. Then, many qubit operations are expressible as rotations around one of the three axes

In the above discussion, we talked about the qubit as a two-level system, specifically a two-level atom. This could be two specific levels of a real atom, such as in the ion trap system, or in an artificial atom such as a quantum dot. The important point is that the phrase "two-level atom" is often a "code word" for the qubit system. This is because the energy levels in an atom are nonlinearly spaced; that is, they vary as $1/n^2$. Hence, the two desired levels are separated by an energy that is not the same as the separation of any other two levels. If the levels were linearly spaced, as in a normal harmonic oscillator, one has a problem. For example, if the lower two levels are those of interest, they are separated by exactly the same energy as any other two adjacent levels. This means that excitation of the lower two levels can also be absorbed by any other two levels, and this constitutes a sizable source of decoherence in the qubit. Hence, one desires the energy levels to be nonlinearly spaced, so that the two levels of the qubit do not couple to other unused energy levels. Since, the atom has this property, the phrase "two-level atom" is often applied to any qubit system to indicate it has the desired properties.

33.2.3 Entanglement

Erwin Schrödinger called entanglement the most important aspect of quantum mechanics [60]. This paper was his response to the Einstein-Podolsky-Rosen paradox published earlier in the year. His point was that once the two particles (envisioned by the latter authors) interacted, they were no longer independent from one another. Rather, they must now be described by a single entangled wave function incorporating both particles. And, it was this entanglement that differentiated the quantum system from the classical one. Needless to say, it is entanglement that has become the crucial ingredient in quantum computing that gives rise to the possibility of major speedup in the computation. In the quantum computer, we want qubits to interact with each other under controlled circumstances. When two qubits interact, they become entangled, just as the two particles in EPR. They remain entangled until some mechanism gives rise to decoherence, which breaks up the entanglement. As a result, one needs long decoherence times in the qubits. In this subsection, we want to examine how this entanglement can occur.

In general, the quantum computer works on controlled gates, as these gates provide the interaction between the qubits. As an example, we take the so-called CNOT gate, or controlled NOT. In the classical system, any transistor (or CMOS gate) is naturally a NOT gate. This is because the transistor inverts its input. If we take a high voltage as a logical 1 and a low voltage as a logical 0, then a 1 input to the gate causes the transistor to turn on, which lowers the output voltage, and this gives a 0 output. Similarly, when the input voltage is low, the transistor is in the off state and the output voltage is high. Thus, the input is inverted, which means that the logical output is NOT(input). The CNOT differs from this slightly, in that the action of the transistor gate is controlled in a manner that makes the classical XOR gate. Now, the XOR gate has two inputs, which are called a and b. If either a or b is high (a 1), then the output is also high. But, if both inputs are either high or low, the output of the gate is low. In other words, the output of the XOR gate is 1 if either a or b is high, but not when both are high.

In the quantum CNOT gate, one of the two inputs is taken to be the control signal, which then operates upon the other input, as shown in Fig. 33.4. Here, the control input (e.g., our a) is labeled as c. The input wave function (e.g., our b), from a previous qubit, is denoted by x. The symbol on the bottom line indicates binary arithmetic modulo 2. So, if the control bit is high, the output y is 0 (the carry is ignored). On the other hand, if the control is 0, the current state of the signal x is passed unchanged to the output. This then gives us the XOR function. We can illustrate this further with a "truth table" as

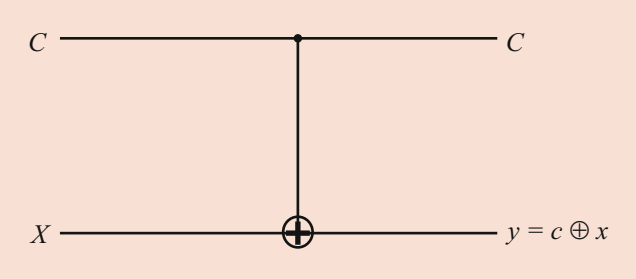

Fig. 33.4 The CNOT gate, where c is the control input and x is the target input. The two are added modulo 2 to produce the output

x	c	y
0	0	0
1	0	1
0	1	1
1	1	0

Here, we can see that the output y is high when either of the two inputs is high, but not when both are the same. We can write the output as a wave function, in which the state of the control bit is the first signal and the state of x is the second variable

$$y \rightarrow |\psi\rangle = \frac{1}{2}\left(|0\rangle\,|1\rangle \pm |1\rangle\,|0\rangle\right) = \frac{1}{2}\left(|01\rangle \pm |10\rangle\right). \tag{33.12}$$

That is, if the control bit is 0, y is 1 only if x is 1, and if the control bit is 1, y is 1 only if x is 0. The wave function (Eq. 33.12) is entangled. That is, if we take the control bit as a two state Hilbert space, and the input bit as a two state Hilbert space, then the entangled output lies in a tensor product Hilbert space, denoted as $H^2 \otimes H^2$. But note that the wave is not a simple product, and it cannot be separated into parts that lie in only one of the individual Hilbert spaces. This is what defines the entanglement. Hence, the wave function in Eq. (33.12) is an entangled wave function. The plus/minus sign gives two possibilities, which both give the same value of 1 for the square magnitude of the wave function (the factor of 1/2 provides proper normalization).

The introduction of the control is really accomplished by the manner in which the interaction between qubits is accomplished and managed. To carry out an algorithm, one has to manipulate the control signals, which actually change the interactions in a specific manner so that entanglement is created, manipulated, or destroyed. This is no different than

the classical computer where bit strings are pushed around, manipulated, and then stored or erased. Here, however, we have the entanglement and the increased power of individual qubits.

33.3 The Silicon Qubit

The idea for a qubit based upon Si effectively dates from the suggestion of Kane to use a ^{31}P dopant in isotopically pure ^{28}Si [61]. In this approach, it was suggested to use the nuclear spin of the P atom, which is 1/2, and the fact that the particular isotope of Si does not have a nuclear spin. Then, the electron wave function for the positively charged donors extends extensively through the conduction band and can mediate the interaction between the nuclear spins on neighboring P atoms. Such a qubit is interesting because it has the promise of a long spin relaxation time and is scalable [62]. Getting the P atoms into the right position thus constitutes a serious problem, but the latter authors have demonstrated that it is possible to create an atomically precise linear array of single P bearing molecules on a Si surface and that these P atoms can act as quantum qubits.

The process of getting a P atom to a precise location turns out not to be so difficult. One method is to hydrogenate the dangling bonds on the Si surface and then to remove particular hydrogen atoms using a scanning tunneling microscope (in ultra-high vacuum) [63]. Removing the hydrogen allows the molecule to be chemically attached to that particular site [64]. In the particular case mentioned above, the molecules from phosphine gas are used to deposit the P atom at the desired position, and then the difficult task is to deposit isotopically pure Si while maintaining the P atom at the desired position [62]. Another approach to locating the P atom is to pursue single atom implantation [65–67]. This latter technology has progressed relatively rapidly, and qubits based upon P atoms have been fabricated with both approaches.

It has also been suggested to use the electron spin rather than the nuclear spin in a semiconductor nanostructure [68]. Use of the electron spin, rather than a nuclear spin, lies in the fact that the electron spin resonance transition for the electron can be rather effectively tuned by electrostatic gates, which are a common part of the single-electron quantum dot structures [69]. In fact, the study of single-electron gate-defined dots in an MOS structure is relatively old [70]. The use of both the single-electron device and electron spin has been reviewed recently [71]. The operation of multiple donor qubits, controlled by surface gates, has been discussed by Witzel et al. [72] and by Mohiyaddin et al. [73]. In particular, the exchange coupling between qubits has been studied further [74]. The operation of a single donor qubit under control of surface gates and measured with a single-electron transistor was evaluated by Dehollian et al. [75]. In Fig. 33.5, we give some information about the operation of this donor qubit formed on the P atom from this latter paper. Here, they use gate set tomography (GST), which is a tool for characterizing logic operations in the qubit. The qubit itself is formed by the spin states of an electron bound to a ^{31}P atom, implanted into the isotopically pure silicon substrate. The spin states are split by an applied magnetic field, and switching is achieved via coupling of the electron spin to the nuclear spin, resulting in a two-spin, four-level system. Qubit preparation is handled by tunneling to/from a single-electron transistor, which is also used for sensing the state. The aluminum gates are placed on top of a SiO_2 layer. In addition, an electron spin resonance signal is used for qubit manipulation.

Sigillito et al. [76] have suggested moving to Ge for better tenability via the bias-induced Stark effect, while Wolfowicz et al. [77] have suggested that surrounding the donor with ^{29}Si nuclear spins may be useful for creating a complete qubit register. Finally, Pakkiam et al. have suggested using quadruple donors together to create a pair of qubits in a singlet-triplet configuration [78].

While much of the effort on single impurity qubits has focused on donors, there has also been some work directed at the use of acceptors as well. There is a feeling that the dopants for this type of qubit need to be near an interface in order to interact well with surface gates. Hence, the use of acceptors near the surface of both Ge an Si has been studied as well [79, 80]. This group has proceeded to demonstrate entanglement and control for the acceptor qubits [81].

The case for nearly all of the above dopant-based qubits is that the dynamic variable is the spin itself. It is possible to consider a hybrid qubit in which the dynamical variable depends upon both spin and charge. The hybrid qubit requires neither nuclear-state preparation nor micromagnets for control and becomes considerably more amenable to systems [82]. This has been studied by these latter authors for the double quantum dot, which is defined lithographically by surface gates (as shown in Fig. 33.6). Here, a more traditional double dot system, similar to those in single-electron transistors, is used for the qubits. Three electrons are used in the system, with the gates tuned so that there are two electrons in the left dot and one in the right dot to define the (2,1) state. Changing the voltage on gate L to raise the energy difference between the dots favors the opposite situation and the state (1,2). The singlet state in the right dot, state (2,1), is taken to be the $|0\rangle$ state. The triplet state in the right dot, the (1,2) state, is taken to be the logical $|1\rangle$. The presence of the extra electron means that the hybrid states of the dots are not pure singlet or triplet and fast electric field techniques can be used to manipulate the qubit in either X or Z rotations on the Bloch sphere.

The coherence can be extended when the hybrid qubit is composed of three electrons in a double quantum dot [83].

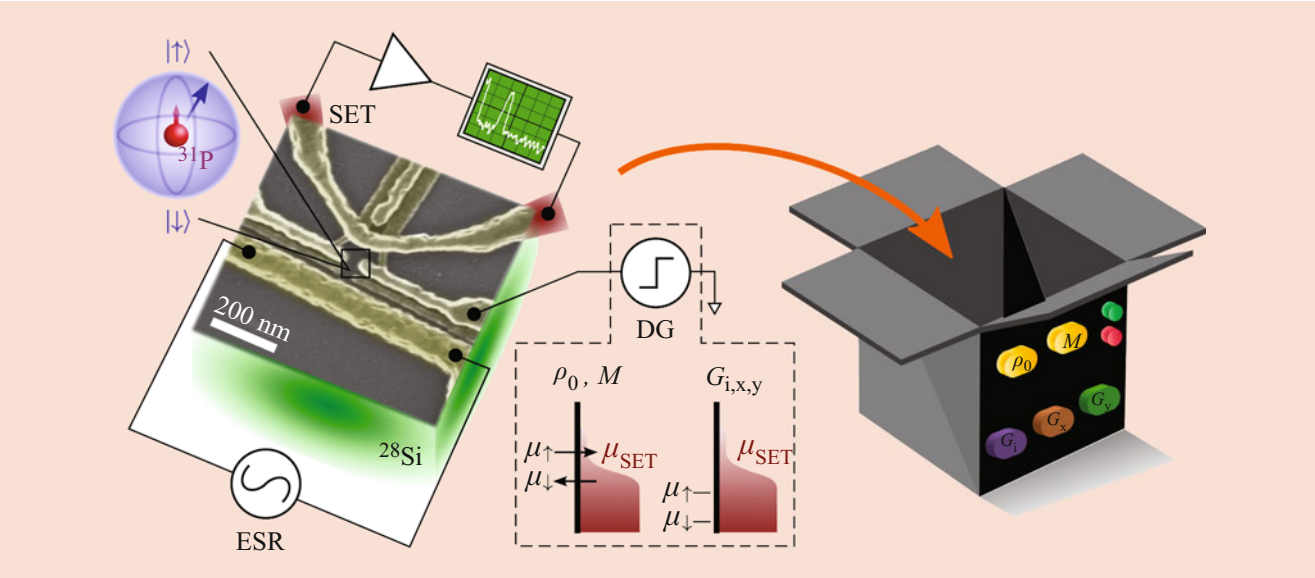

Fig. 33.5 Diagram of qubit device and the gate set tomography (GST) model of a qubit. SEM image of the on-chip gate structure is shown to the left. The aluminum gates have been false colored for clarity. Depicted in red are the source-drain n^+ regions which couple the single-electron transistor to the current measurement electronics. For initialization and measurement, the donor gates are pulsed such that $\mu_\uparrow > \mu_{SET} > \mu_\downarrow$, inducing spin-dependent tunneling between the donor and the SET. When applying a gate sequence, the DG are pulsed to higher voltage to prevent the donor electron from tunneling to the SET. The inset diagram – zoomed from the approximate donor location – represents the Bloch sphere of the qubit, consisting of the spin of an electron confined by an implanted ^{31}P donor, with its nuclear spin frozen in an eigenstate. The GST model treats the qubit as a black box with buttons (right) which allow one to initialize (ρ_0), apply each gate in the gate set ($G_{i,x,y}$), and measure (M) in the observable basis ($|\uparrow\rangle$ *or* $|\downarrow\rangle$). (Reproduced under the Creative Commons Attribution 3.0 licence from J. P. Dehollian et al., "Optimization of a solid-state electron spin qubit using gate set tomography," New J. Phys. **18**, 103,018 (2016) DOI: https://doi.org/10.1088/1367-2630/18/10/103018)

Similar surface control gates have been used in the pure spin qubit case as well [84], where multiple dots are used to suppress charge noise. This was studied for a pair of singlet-triplet qubits, each of which was composed of two electrons in a double quantum dot. More recently, the importance of the spin-orbit interaction in these gate-defined dots has been studied [85, 86], and the impact of atomic-scale structure in the energy dispersion on decoherence was investigated [87].

The singlet-triplet qubit is attractive for many reasons, particularly for its high fidelity, at least for single qubit operations. However, for two qubit operations leading to entanglement, it can be problematic in a sense that there are a range of operations over which the interaction can occur, and this leads to a preferred set for good performance [88]. In addition, the interaction between a hybrid qubit (discussed above) and other types of qubits has been studied, since such an interaction can usually be tuned between different operating modes via the gates [89].

Spin qubits formed of quantum dots in the Si/SiO_2 system have been formed in a manner to have from 1 to 3 electrons in the dots [90]. Then, pulsed electron spin resonance is used to exercise coherent control over the qubit. With these structures, these authors then demonstrated the achievement of valley splitting (normally, in the MOS system, the six ellipsoids of the conduction band break into a twofold and a fourfold set due to the inversion potential, and one seeks to further split the lower lying twofold set) [91]. The role of disorder on this valley splitting has also been studied [92]. Another work has suggested that the MOS structure could lead to a maximum density of quantum information when the hybrid qubits are utilized [93].

Quantum dots have also been created in the Si/SiGe heterostructure system. High fidelity gating of a single hybrid qubit has been achieved in this system [94]. The use of a stray magnetic field to switch a spin qubit has also been studied [95]. The optimal geometry for the gates for such a spin qubit in this heterostructure (or in GaAs) has been studied for a single qubit [96] and for a qubit linear array [97]. This theme has been continued with the study of circuit QED for linear arrays of quantum dots [98]. Finally, the coupling of the quantum dot state to that of a photon has been studied in these quantum dots [99, 100].

33.4 The Josephson-Based Qubit

It was clear from the discussion in Sect. 33.1.4 that the dominant current approach lies with superconductivity and the use of Josephson junctions for qubits. The Josephson junction is a tunnel junction in which the materials on either

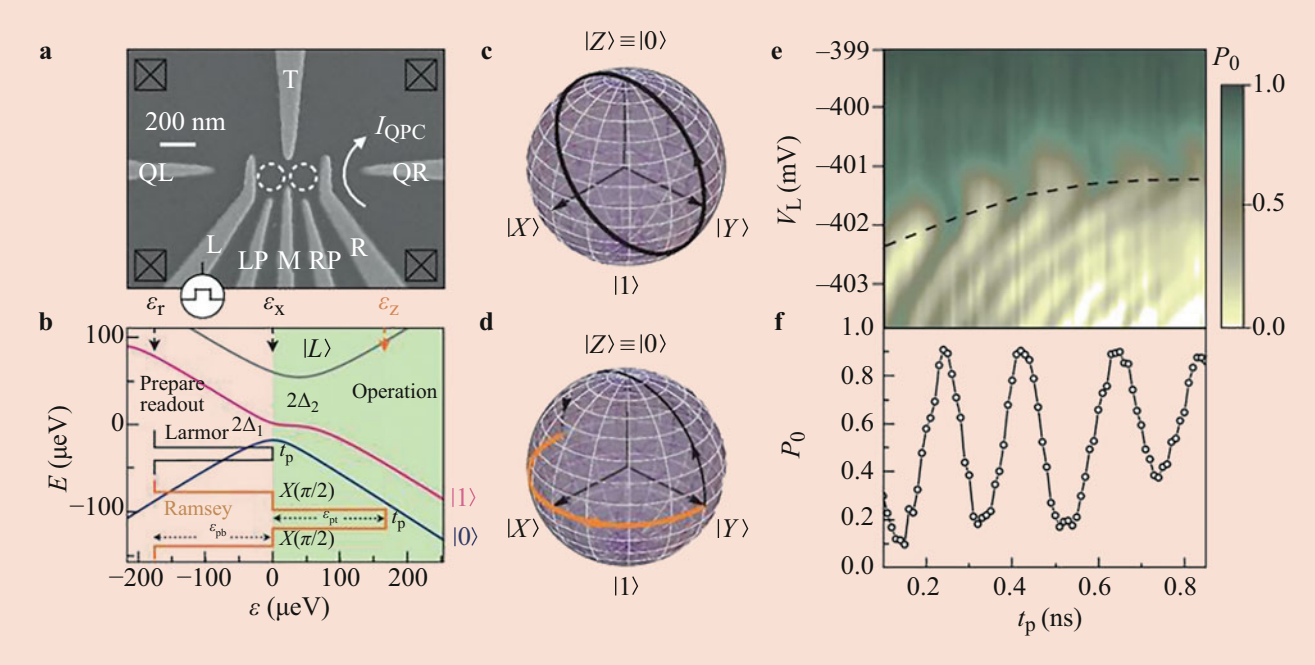

Fig. 33.6 A Si/SiGe hybrid qubit device, energy levels, and measurements. (**a**) A scanning electron microscope image of a device defined lithographically with the locations of the double dot shown by white dashed circles. The current through the quantum point contact I_{QPC} is used for charge sensing via a measurement of the change in the presence of manipulation voltage pulses applied to gate *L*. The voltage on gates QL, QR, LP, M, RP, and R is used to determine the overall operating point. (**b**) Diagram of the calculated energy levels *E* versus detuning ε, including the ground states of the (2,1) and (1,2) charge configuration. The singlet-triplet splitting δE and the first excited state of the (1,2) charge configuration, with Hamiltonian parameters shown. The resulting blue, magenta, and gray solid curves show logical states $|0\rangle$ and $|1\rangle$ and the primary leakage state $|L\rangle$. The overlaid curves show the pulse sequence used for implementation and measurement of rotations about the *X*-axis (black) and *Z*-axis (orange). (**c**, **d**) Schematics of the evolution of the Bloch vector during these latter two sequences. (**e**) Probability of the state to be $|0\rangle$, measured for the *X*-rotation pulse sequence as a function of the voltage V_L and pulse duration t_P. Dashed curve shows a path along $\varepsilon \approx 0$. (**f**) Line cut of the probability along the dashed curve in (**e**), as a function of t_P, starting at $V_L \approx -402$ mV with pulse amplitude $\varepsilon_{PB} \approx 160$ μeV, showing ∼5.2 GHz quantum oscillations with coherence time $T_2^* \approx 2$ ns. (Reprinted by permission from Macmillan Publishers, Nature: "Quantum control and process tomography of a semiconductor quantum dot hybrid qubit," D. Kim et al., Nature **511**, 70–74 (2014). Copyright 2014)

side of the insulator (or nonsuperconducting material) are superconductors. As it is a tunnel junction, it is natural that the Wigner function comes into play just as for semiconductor tunnel junctions. In one of the earliest uses for this device, a very small junction was used such that single-electron behavior could be observed [101] (in superconductors, for temperatures above absolute zero, the carriers are a mix of Cooper pairs and normal electrons above the gap). Normally, with Josephson junctions, the tunneling is carried out by Cooper pairs, but these authors have generated a master equation that describes both the Cooper pair tunneling and the single-electron tunneling. It is also known that the Josephson junction can be a microwave source, and it has been observed that one can see a so-called Riedel peak in the response of the junction [102, 103]. The Josephson frequency is given by $f_J = 2eV/h$, and the Riedel peak is observed at $f_J = 4\Delta/h$. This peak lies at a bias voltage of $2\Delta/e$ [103]; Δ is the superconducting gap (the factor of 2 appears as the normal energy to raise a Cooper pair above the gap is twice the energy gap due to the $2e$ charge). In the modeling of the single-electron tunneling, it is found that the Riedel peak and the gap for the quasi-particle-pair interference are shifted to $2\Delta/e - e/2C$, while the quasi-particle tunneling gap shifts to $2\Delta/e + e/2C$ [101]. Here, the term $e/2C$ is the Coulomb charging energy for single-electron effects, where *C* is the capacitance of the small junction. Hence, there is a hybridization between the superconducting gap and the Coulomb gap. In this latter paper, the master equation was developed for the Wigner function describing the charging effect on Cooper pairs and quasi-particle pairs, as well as the single electron tunneling in the junction.

The step from a Josephson junction toward a qubit based upon this device was taken in 2005 when the quality factor of a microwave cavity was measured by coupling it to a superconducting qubit device. This approach was used to bring the cavity quantum electrodynamics (cQED) to the table [104]. But, this was not the beginning. Interest in superconducting qubits goes back further. In looking at this, one needs to distinguish two types of qubits: microscopic and macroscopic [105]. The microscopic qubit is based upon

an internal charge or spin, much like the Si qubits of the previous section, or upon two natural levels as in an atom. Macroscopic qubits are based on quantum levels representing collective degrees of freedom like the persistent current in a superconducting ring [106] or excess charge on a superconducting island [107, 108]. Hence, one might think that the macroscopic form will be physically larger, but this is usually only a perception. When superconducting components are used in electrical circuits, then these circuits become quantum objects, which can then be used in either type of qubit. The pursuit of superconducting qubits can be a Cooper pair box charge qubit, the persistent current flux qubit, or a hybrid charge-flux qubit [105]. As a group, this is the pioneering approach adopted by IBM for its initial quantum computers [109].

33.4.1 The Charge Qubit

The charge qubit is composed primarily of the Cooper pair box, where the box is formed by a pair of small Josephson junctions so that single electron tunneling (or Cooper pair tunneling) governs the excitation of the box itself, which is isolated by the two junctions. A single Cooper pair box [110] is a unique artificial solid-state system [107]. Although there are quite a few electrons on the island (box), they all form Cooper pairs in the superconducting state and then condense into a single macroscopic quantum state. This state is separated from the normal electrons by the superconducting gap Δ, discussed above. The only low-energy excitations arise from Cooper pair tunneling when the gap is larger than the charging energy $E_C = e/2C$. On the other hand, if the charging energy is larger than the gap energy, and the thermal fluctuations are suppressed, the system can be considered to be a two-level system in which the lowest two energy states differ by one Cooper pair. The separation of the two levels of interest can be controlled by an additional gate voltage. In Fig. 33.7, we show such a charge qubit from the work of Nakamura et al. [107].

When the island is small, the charging energy dominates the qubit operation, but one can write a simple Hamiltonian as [105]

$$H = 4E_C\left(N - n_g\right)^2 - 2E_J \cos\left(\vartheta\right) \cos\left(\frac{1}{2}\varphi_e\right), \qquad (33.13)$$

where E_J is the Josephson energy ($=\Phi_0 I_c/2\pi$, where $\Phi_0 = h/e$ is the flux quantum and I_c is the critical current in the junction), n_g is indicative of the gate voltage (through the capacitor coupling), φ_e is the external flux, and θ is the difference in the Josephson phases of the two junctions. With the two junctions, the box can be tuned with the external flux passing by the reservoir, much like a SQUID, which is discussed below.

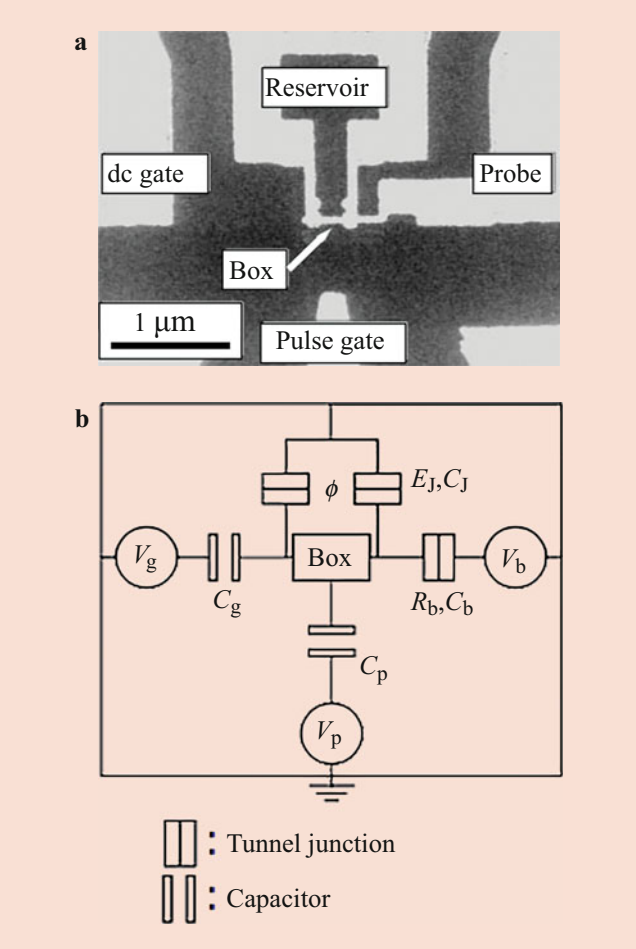

Fig. 33.7 Single Cooper-pair box with a probe junction. (**a**) Micrograph of the sample. The electrodes (light areas) were fabricated by electron-beam lithography and shadow evaporation of Al on a SiN_x insulating layer (400 nm thick) above a gold ground plane (100 nm thick) on an oxidized Si layer. The box electrode is 700 × 50 × 15 nm Al and contains ~10^8 conduction electrons. The reservoir electrode was evaporated after a slight oxidation of the box Al, so that the overlap produces two parallel low-resistance tunnel junctions with Josephson energy E_J. The latter can be tuned by a flux passing through the enclosed void in the reservoir. The box is coupled (through further oxidation) to the probe junction, which is highly resistive. Two other electrodes at left and bottom are capacitively coupled to the box. (**b**) Circuit diagram of the device. (Reprinted by permission from Macmillan Publishers, Nature: "Coherent control of macroscopic quantum states in a single-Cooper-pair box," Y. Nakamura et al., Nature **398**, 786–788 (1998). Copyright 1998)

When the charge qubit is shunted by a capacitor, as a method of reducing current noise, the device has been called a *transmon* [111]. The shunt capacitor also reduces the charging energy and hence increases the size of the Josephson energy relative to the charging energy. Measurement and control of the box qubit is commonly done by means of microwave resonators with the techniques usual in quantum

electrodynamics, as in other superconductor qubits [112]. As a result, it is possible to couple a pair of transmons to photons and produce nonlinear optical effects such as photon blockade [113].

33.4.2 The Flux Qubit

One of the most interesting aspects of circuits is that a resonant circuit can be a quantum oscillator, much akin to the harmonic oscillator [114]. In the absence of dissipation, the Hamiltonian can be written as

$$H = \frac{q^2}{2C} + \frac{\Phi^2}{2L}, \tag{33.14}$$

where the charge q and flux Φ are the conjugate variables and satisfy a commutator relation with one another. Of course, to reach the quantum limit, we must work at low temperature, which naturally makes a connection with superconducting circuits. In the presence of dissipation, we need to have a good-quality factor $Q\ (= \omega\tau \gg 1)$. Hence, when we couple a Josephson junction to a superconducting ring (the junction is placed in the ring itself), we obtain the persistent current flux qubit, sometimes called an RF superconducting quantum interference device (RF-SQUID). Here, we need to have $E_J \gg E_C$ [106, 115], so the charging energy cannot be too large. The eigenstates of the ring represent two counter-rotating persistent currents, corresponding to a fixed number of flux quanta (h/e) in the loop. The inductance of the ring gives rise to a parabolic potential, like the harmonic oscillator, and adding the Josephson oscillating potential provides the needed nonlinearity to separate off the lowest states from the linear chain, as discussed earlier. For the two levels of the qubit, the Hamiltonian can be written as [105]

$$H = 4E_C n^2 + E_L(\varphi - \varphi_e + \varphi_{int}\sigma_z)^2 - E_J \cos(\varphi), \tag{33.15}$$

where the interaction term arises from the effect of the external bias flux on the two persistent current states. When $\varphi_e = \varphi_0/2$, the lower part of the potential is a symmetric double well creating nearly degenerate $|L\rangle$ and $|R\rangle$ states which lead to bonding and anti-bonding hybrids of these two states. These latter two states are created by the macroscopic tunneling through the Josephson junction which couples the two persistent current states, and these hybrid states provide the two levels of the qubit. The Wigner function in number-phase representation shows that the state of the system evolves into a quantum superposition of two coherent states which clearly demonstrate interference and negative values for the Wigner function description of the system. Yet, when the system is represented in the number-phase coordinates, the Wigner function evolves in a classical manner [115]. This ring-junction system was studied further to investigate the role of dissipation on the evolution of the Wigner function description of the system [116]. In this latter case, the dissipation is incorporated by coupling the system to a reservoir, and this expanded system is then projected back onto the reduced density matrix for the ring-junction system. They conclude that the two coherent states survive even in the presence of dissipation, at least for weak dissipation.

The flux qubit can also be prepared with a three junction ring, much like the hybrid qubit of the next section. This qubit can then be coupled to a transmission line resonator to produce cavity QED interactions. The capacitance between the qubit and the resonator can be controlled by varying the width of the capacitance line, so that the coupling depends upon the number of qubits placed in the overall circuit [117, 118]. We note that this can also be done with single junction qubits [119].

33.4.3 The Hybrid Charge-Flux Qubit

If we add a second Josephson junction in the ring, we can have both the charge box between the two junctions and flux coupled through the ring. If the Coulomb energy E_C dominates the Josephson energy, we have the charge qubit limit. If the Josephson energy dominates the Coulomb energy, we reach the flux qubit limit, but if we have $E_J \geq E_C$, we are in the charge-phase or hybrid charge-flux qubit regime [105]. In many situations, the system acts as a two-level atom, which is called a quantronium [108]. A quite similar version of the quantronium is shown in Fig. 33.8 [120]. The two lower Josephson junctions create the charge box part of the circuit, but the ring from these to the larger third junction creates the supercurrent, flux reservoir. This look is coupled (not shown) to an external flux circuit that is used to vary the flux enclosed in this ring. The box charge is varied through the coupling capacitor and gate voltage. The pair of capacitors are used to reduce the noise, while the current source provides the current drive to the qubit itself. The Hamiltonian for the circuit is given as [120]

$$H = E_C(N - n_g)^2 + E_J\left[1 - \cos\left(\frac{\varphi + \gamma}{2}\right)\cos(\varphi)\right] + \frac{Q^2}{2C} + E_{J0}(1 - \cos\gamma) \tag{33.16}$$

where the different parameters are defined in the figure in terms of the fluxes through the various junctions with $\varphi = (\varphi_1 + \varphi_2)/2$ and n_g has its former meaning. The fluxes are normalized to the flux quantum. The lowest and first

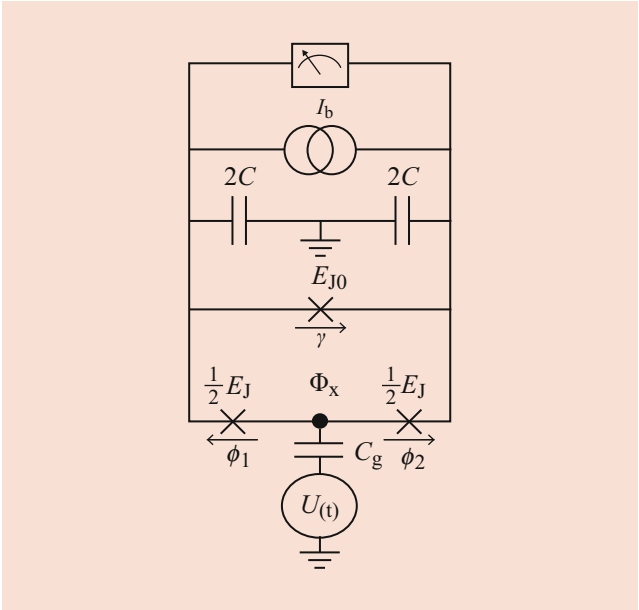

Fig. 33.8 Circuit diagram of the quantronium charge-flux qubit. (Reprinted with permission from G. D. Hutchinson et al., Phys. Rev. A 74, 062302 (2006). Copyright 2006 by the American Physical Society)

excited states of the quantronium are taken to be the $|0\rangle$ and $|1\rangle$ states. In this configuration, the circuit is operated so that the applied flux Φ_x is set to zero and the normalized gate charge is set to 1/2 so that the qubit levels are separated by the Josephson junction coupling energy. Then the Hamiltonian can be written as

$$H' = E_J \left[1 - \cos\left(\frac{\gamma}{2}\right)\right] \sigma_z + E_{C0} N^2 + E_{J0} (1 - \cos\gamma), \tag{33.17}$$

where $E_{C0} = 2e^2/C$ and N is the charge operator for the large Josephson junction. This Hamiltonian describes a two-level system, with the levels separated by an energy given by the first term on the right of Eq. (33.17). The phase in this term provides the coupling between the qubit and the readout junction.

As discussed above, the charge-flux qubit is operated normally at this charge degeneracy point and is controlled and switched via microwave pulses in order to demonstrate the presence of Rabi oscillations between the two qubit states. It often can have a fairly long coherence time and thus can perform hundreds of well-controlled single qubit gate operations. In simulations of the circuit, it is found that during the readout pulse for the circuit of Fig. 33.8, the coherence time of the qubit is of the order of 0.2 ns after the bias current has been applied (the role of the bias current is to dephase the qubit). The simulation results have been compared with the experimental data obtained by Vion et al. [108].

33.4.4 Coupling Qubits

The development of quantum computers now requires one to move from the qubit level to the gate level and the achievement of long coherence times. The development of single qubit gates [121, 122] and two-qubit gates has allowed this process to become real in the recent years. In a major step forward, five qubits have been integrated into a single circuit with the resonators used for readout and the control lines to operate the gates [122]. The qubits used in this chip are variants of the transmon qubit described above. The chip is shown in Fig. 33.9. Each of the qubits is a cross-shaped Xmon variant of the transmon qubits and are placed in a linear array. These qubits are read out by five meandering coplanar waveguide resonators, one used for each qubit. These resonators are coupled to a single readout line, made possible by frequency multiplexing of the resonators. Individual qubits are driven through individual microwave control lines (denoted by *XY* in the figure) as well as inductively coupled d.c. lines (denoted by *Z* in the figure). The operation of the qubits on the Bloch sphere is also indicated in the figure.

Other schemes have been suggested to couple qubits together. The use of capacitors to couple charge qubits via a SQUID circuit is one such scheme [123]. It has also been suggested to couple flux qubits through an *XY*-type of exchange interaction [124]. Nevertheless, the growth of several approaches to the use of superconducting qubits, described in Sect. 33.1.4, clearly points out that quite a few methods similar to that of Fig. 33.9 have appeared in commercial endeavors.

33.5 Integrated Optics

There has been tremendous interest in optical qubits and systems, not the least because of the interest in quantum communications systems. Our connection to nanoelectronics lies in the existence of integrated optics, e.g., putting the optical system on a chip. While we will discuss such chips, it is meaningful to introduce the critical optical processes if we are to understand how such chips work, because they are different from other qubits. One approach has treated qubit-oscillator states. In its most basic form, this is just another variation of the Jaynes-Cummings model in which the two-state atom is replaced by the qubit. This Jaynes-Cummings model is quite old [125] and involves coupling a two-state atom to an electromagnetic resonator. We will discuss it in some detail in the next subsection. The variation of the model involves replacing the two-state atom with a qubit that possesses its own complex nature. Squeezed states have also been used for representing qubits. Measuring these states relies upon the existence of non-demolition detectors that can detect a single photon without destroying it in an

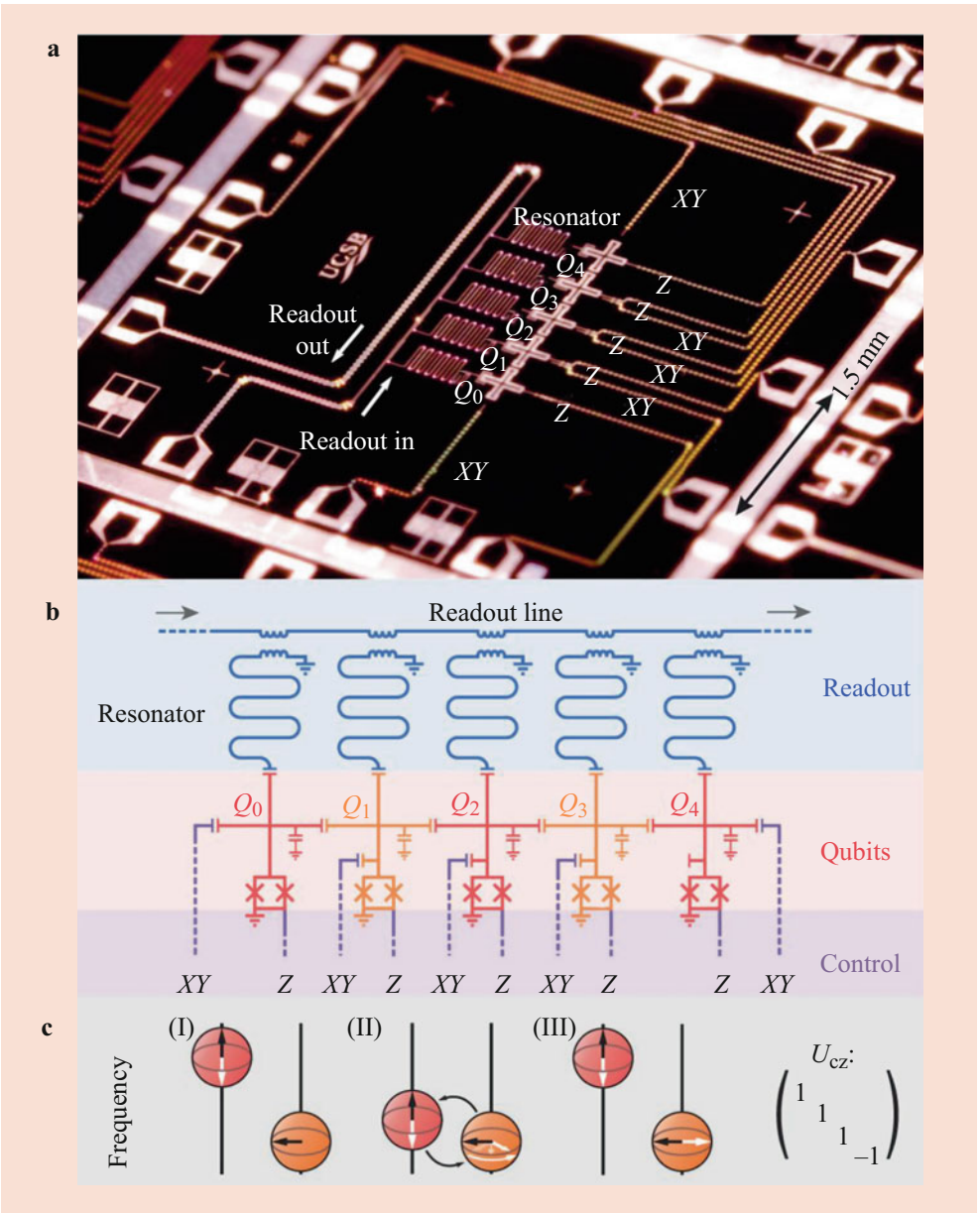

Fig. 33.9 (**a**) Optical image of the integrated Josephson quantum processor consisting of aluminum (light) on sapphire (dark). The five cross-shaped items in the center are the Xmon variants of the transmon qubits. To the left are the resonators and readout lines, while the control lines are to the right. (**b**) Circuit diagram of the chip. (**c**) Schematic representation of an entangling operation, on the Bloch sphere, using a controlled-phase gate with unitary representation U_{CZ}: (i) qubits at rest (at distinct frequencies with no interaction); (ii) when brought near resonance, the state-dependent frequency shift brings about a rotation in the qubit states; (iii) qubits returned to rest. (Reprinted by permission from Macmillan Publishers, Nature: "Superconducting quantum circuits at the surface code threshold for fault tolerance," R. Behrends et al., Nature **508**, 500–503 (2014). Copyright 2014)

absorption process. Such detectors often rely upon the phase shift produced by the photon traveling through a nonlinear medium [126]. Recently, two-mode qubit-like entangled squeezed states have been compared with entangled coherent states, through the use of the Wigner functions for the two types of states [127]. The Wigner function and its negative excursion have been used to signify the entanglement of as many as 3000 atoms by a single photon [128]. The role of entanglement for the generation of the negative portions of the Wigner function has also been studied for multi-qubit GHz-squeezed states [129].

The qubit-oscillator system has also been used to create what are called Schrödinger kitten states [130–132], so called because it is a microscopic superposition of two coherent states with opposite phases [133]. By passing these states through a Kerr medium, the gain by such a process can exceed

the normal optical losses and lead to squeezed kitten states. Such kitten states, as well as single-photon states, have been also generated from the steady-state output of a continuously driven optical parametric oscillator [134]. In principle, the kitten state can be generated by subtraction of photons from a squeezed vacuum state [135]. Needless to say, there has been an effort to create chips for these optical circuits; one of the first ones was designed to continuously generate and manipulate entangled states of light [136]. While the goal is to discuss such chips, we begin with understanding the key concepts that differ optics from charge or flux-based systems.

33.5.1 The Jaynes-Cummings Model

The coupling between a two-level atom and a resonant (quantized) electromagnetic cavity is described by a relatively old model, termed the Jaynes-Cummings model [125], that we have already mentioned above. It turns out that the process of coupling a coherent optical beam to such an atom is of great interest in quantum optics, so we want to discuss the model in a little more detail. The model treats the atom as a two-level system and describes the interaction of this atom with a quantized mode of an optical cavity. The principle of the model is analogous to the problem of two coupled classical pendulums that are connected to produce an interaction. This interaction leads to a coupling of the two modes in a way in which all of the energy oscillates between the two pendulums. At a given instant of time, pendulum 1 may be static, while all the energy is in the oscillation of pendulum 2, and at a later time, the process is in the opposite state. In the quantum case, one pendulum is the harmonic oscillator mode of the electromagnetic cavity, while the second is the atom, which is described as an oscillator by its Rabi frequency. Hence, the field can interact with the atomic state and lead to Rabi oscillations of the atomic state population. As with the pendulums, the Rabi oscillation is not static in amplitude. Something different happens, in that the Rabi oscillations collapse and then reappear periodically, just as the energy moves from one pendulum to the other. The temporal time over which this collapse and reappearance occurs has been termed the revival time [137]. When the field in the cavity is in a coherent state, and the atom is prepared in an excited state, it is found that the atomic and field states become rapidly entangled and then subsequently disentangle at one-half the revival time [138]. That is, the maximum entanglement of the atomic states occurs when the Rabi oscillations are strongest and the minimum entanglement occurs when the Rabi oscillations are minimal. More recently, it has been observed that the photon parity operator also shows similar behavior with one important difference. The peaks of the amplitude of the parity operator seem to occur when the Rabi oscillations are at their minimum. So, the amplitude and decay of this parity operator seems to be shifted by half a period from the Rabi oscillations [139]. Because the parity operator is proportional to the number density of the photon field, this latter is also in agreement with the two pendulum concept, as the Rabi oscillation is a minimum when the majority of the energy is in the photon oscillator. The Jaynes-Cummings model was revived in this century [140] and applied explicitly to the problem of a trapped ion interacting with a laser field (which was mentioned in the introduction in connection with one of the commercial approaches to a quantum computer).

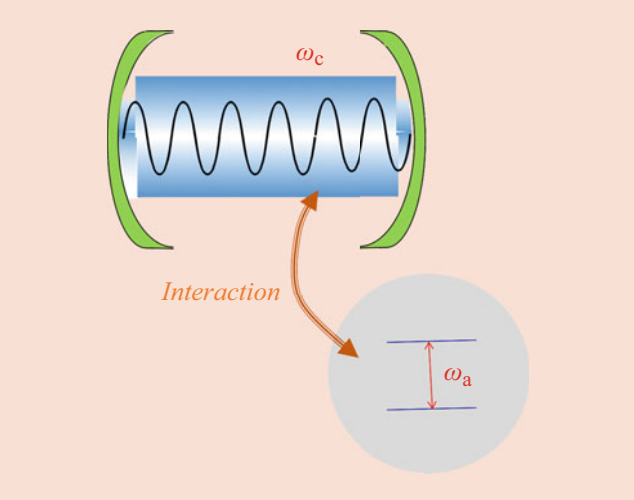

Fig. 33.10 Pictorial representation of the Jaynes-Cummings model in which a two-level atom (lower right) interacts with a mode of a resonant cavity (top)

The Hamiltonian can be described relatively simply in terms of the various components, as discussed above, and shown in Fig. 33.10. First, the electromagnetic field, or the laser field, is quantized as usual in QED in terms of a series of harmonic oscillators that describe each of the modes that can exist in the cavity or wave [141]. Since, we are interested in a single mode, we write the wave energy as

$$H_{\mathrm{EM}} = \hbar\omega_{\mathrm{C}}\hat{a}^{\dagger}\hat{a}, \tag{33.18}$$

where the operators are the normal creation and annihilation operators for the field harmonic oscillator representation of the single mode of the cavity and ω_{C} is the frequency of this mode. The atomic levels are just the two levels of the atom, which we describe with a pseudo-spin index with the spin up state as the upper level and the spin down state as the lower level, so that we can write the Hamiltonian as

$$H_{\mathrm{a}} = \hbar\omega_{\mathrm{a}}\frac{\hat{\sigma}_z}{2}. \tag{33.19}$$

Hence, the atomic frequency describes the separation of the two states. The state of the atom is described by its polarization

$$\hat{S} = \hat{\sigma}_+ + \hat{\sigma}_-, \tag{33.20}$$

where $\hat{\sigma}_+$ and $\hat{\sigma}_-$ are the normal raising and lowering operators of the two-level atom in its own harmonic oscillator notation (See, e.g., [142]). Hence, the polarization is equivalent to the position operator in a normal harmonic oscillator, with the various parameters being folded into a pre-factor discussed shortly. The interaction between the electromagnetic field and the atom occurs through the electric field of the wave. Normally, the potential would be proportional to $eE_z z$, so here we take the position as the polarization and write the interaction energy as

$$H_{\text{int}} = \frac{\hbar\Omega}{2} E_z \hat{z}\hat{S} = \frac{\hbar\Omega}{2} E_z \left(\hat{a}^\dagger + \hat{a}\right)\left(\hat{\sigma}_+ + \hat{\sigma}_-\right). \tag{33.21}$$

The parameter Ω incorporates all the various constants arising from the connection between the operators (from the harmonic oscillators) that appear in Eq. (33.21) and their corresponding position operators. The creation and annihilation operators each have their time variation determined by their respective frequencies, so the four cross terms will have fast variations due to the sum of the frequencies and slow variations due to the difference in the two frequencies. Generally, the fast components are ignored, and only the slow components are retained in what is called the rotating wave approximation. The Hamiltonian is generally separated into two commuting parts, which are described by

$$\begin{aligned} H_1 &= \hbar\omega_C \left(\hat{a}^\dagger\hat{a} + \tfrac{\hat{\sigma}_z}{2}\right), \\ H_2 &= \hbar\delta\tfrac{\hat{\sigma}_z}{2} + \tfrac{\hbar\Omega}{2}\left(\hat{a}\hat{\sigma}_+ + \hat{a}^\dagger\hat{\sigma}_-\right), \end{aligned} \tag{33.22}$$

where $\delta = \omega_a - \omega_C$ is the so-called detuning of the frequency between the field and the atom. This creates a proper 2×2 Hamiltonian, whose eigenvalues are given in terms of the number operator (first term in the parentheses of line one of Eq. (33.22)) for the field as

$$E_\pm = \hbar\omega_C \left(n + \frac{1}{2}\right) \pm \frac{\hbar\Omega_n(\delta)}{2}, \tag{33.23}$$

where

$$\Omega_n = \sqrt{\delta^2 + \Omega^2 n + 1} \tag{33.24}$$

is the Rabi frequency for the specific detuning parameter. If the detuning is small, the atomic state Rabi oscillations occur with an average frequency $\Omega_C = 2\Omega\sqrt{n+1}$. As the mode occupation builds up, the Rabi frequency increases, and the amplitude of these oscillations increases. The photon parity operator is then defined as

$$\Pi_F = (-1)^n = e^{in\pi}. \tag{33.25}$$

The normal expectation value of this operator is found to be [139]

$$\langle \Pi_F(t) \rangle = e^{-n} \sum_{s=0}^{\infty} (-1)^s \frac{n^s}{s!} \cos\left(2\Omega t\sqrt{s+1}\right), \tag{33.26}$$

where the time dependence arises from the time dependence of the effective Rabi frequency. The interesting fact is that for $t = 0$, the cosine is unity, and the expectation value of the parity operator goes asymptotically to zero (the time is scaled with the same coupling factor). Hence, when the density peaks and the Rabi oscillations are strongest, the parity operator vanishes and vice versa.

Many variations on the Jaynes-Cummings model have appeared over time. First, the model has been generalized through the development of a Markovian master equation approach, rather than sticking with the Hamiltonian form [143, 144]. Then, the model has been extended to a double Jaynes-Cummings model by incorporating two two-level atoms within the structure [145–147], as well as to a pair of three-level atoms [148]. An anti-Jaynes-Cummings model used the interchange of the two field operators in the second term of H_2 in Eq. (33.22) [149]. Finally, Miranowicz et al. replaced the electromagnetic field with the phonon field in the study of a nanomechanical resonator [150].

33.5.2 Qubits

The introduction of the quantum process in the previous section on the Jaynes-Cummings model gives us a nice transition into the discussion of optical qubits. Just as the qubit was coupled to a resonator in the superconducting qubit, a similar approach has treated optical qubit-oscillator states. In its most basic form, this is just another variation of the Jaynes-Cummings model in which the two-state atom is replaced by the qubit. In this case, the Hamiltonian becomes [151]

$$H = \hbar\omega_C \hat{a}^\dagger\hat{a} + \frac{\hbar\Omega}{2}\hat{\sigma}_x + \frac{\hbar\Omega}{2} E_z \hat{\sigma}_x \left(\hat{a}^\dagger + \hat{a}\right), \tag{33.27}$$

which differs from Eqs. (33.18–33.21) only in the choice of spinors in the last two terms, e.g., the "atom" and interaction terms. The change introduces the complex nature of the qubit which replaces the two-state atom. This has been studied again, more recently, within the rotating wave approximation [130, 152]. This latter work has used the results to examine the differences among various information-theoretic measures.

Squeezed states have also been used for representing qubits. One of the most ubiquitous objects in quantum mechanics is the Gaussian wave packet, because it can be used to create the minimum uncertainty wave packet, and this Gaussian wave packet is the starting point for squeezed states. Normally, the Gaussian wave packet is a minimum uncertainty wave packet, and, as it is positive definite, it is a classical quantity. The minimum uncertainty packet can be used to make a so-called coherent packet by adding a propagator to it, as

$$\psi(x) = \sqrt{\frac{1}{\sqrt{2\pi}\sigma}} \exp\left[-\frac{x^2}{4\sigma^2} + ik_0 x\right], \tag{33.28}$$

where σ is the standard deviation and k_0 is the wave number for the momentum of the packet. This can be Fourier transformed to an equivalent coherent state in momentum space and the two combined via the Wigner-Weyl transform to provide a Wigner function as

$$f_\psi(x, k) = \frac{1}{h} \exp\left[-\frac{x^2}{4\sigma^2} - 2\sigma^2(k - k_0)^2\right]. \tag{33.29}$$

Hence, the coherent state (Eq. 33.28) gives us a standard Wigner function in phase space that moves with the average momentum of the wave packet. We note that this Wigner function is positive semi-definite (it can take the values of zero at infinite distances from the center in either position or momentum) [153]. So, in quantum optics, the idea of a single photon is represented by a minimum uncertainty wave packet. The idea of the minimum wave packet lies in just this position and momentum spreading of the packet. One problem, of course, is that the photon is supposedly traveling at the speed of light. This gives a great difficulty in describing just what the spread in momentum represents. On the other hand, if the photon represents a particular mode in a resonator, such as in the Jaynes-Cummings experiments of the previous section, then it has a mode momentum that differs from the speed of light. We have to remark that in both cases, there is a difference between the expectation value of the momentum and the speed of light, if for no other reason that that the photon has zero mass. Hence, momentum is described by the propagation constant of the wave, which is linear in the frequency (in free space) as

$$k = \frac{\omega}{c} = \frac{p}{\hbar}. \tag{33.30}$$

In the Wigner function, we note that the spread in position and the spread in momentum are naturally described by the standard deviation σ. The idea of a *squeezed state* is to reduce the uncertainty in the amplitude of the wave [154, 155], by utilizing nonlinear optics. In the first case [154], four-wave mixing was used, while in the latter case [155], parametric down conversion was applied to the optical wave. These nonlinear processes now produce true quantum states, hence the terms quantum optics.

Measuring these squeezed states relies upon the existence of non-demolition detectors that, as mentioned above, can detect a single photon without destroying it in an absorption process. Such detectors often rely upon the phase shift produced by the photon traveling through a nonlinear medium [126]. Recently, a two-mode qubit-like entangled squeezed state has been compared with entangled coherent states, through the use of the Wigner functions for the two types of states [127]. The Wigner function and its negative excursion have been used to signify the entanglement of as many as 3000 atoms by a single photon [128]. The role of entanglement for the generation of the negative portions of the Wigner function has also been studied for multi-qubit GHz-squeezed states [129]. But, it is important to point out that it is the qubit-oscillator system that can be used in the strong coupling limit to produce the nonclassical states necessary for the qubit [156, 157].

The qubit-oscillator system has also been used to create what are called Schrödinger kitten states [130, 132, 152, 158], so called because it is a microscopic superposition of two coherent states with opposite phases [133]. By passing these states through a Kerr medium, the gain by such a process can exceed the normal optical losses and lead to squeezed kitten states. Such kitten states, as well as single-photon states, have been also generated from the steady-state output of a continuously driven optical parametric oscillator [134]. In principle, the kitten state can be generated by subtraction of photons from a squeezed vacuum state [135]. It is these nonclassical states of light that are used in the qubit systems [159].

33.5.3 Qubits and Gates

It is probably not surprising that the idea of a qubit can be extended to multiple qubits and various forms of gates. It is also not surprising that the optical gates are not as far advanced as those for silicon and superconducting technologies. But, the

optical approach has the advantage that it can be foreseen to operate efficiently at room temperature, an advantage that should not be overlooked. Nevertheless, significant progress has been made recently. One approach is to follow the results discussed above and extend the Jaynes-Cummings model to the case of multiple atoms and a resonator which yields the extension of Eqs. (33.18, 33.19, 33.20, and 33.21) to

$$H(t) = \hbar\omega_C \hat{a}^\dagger \hat{a} + \frac{\hbar\omega_a}{2} \sum_{i=1}^{N} \sigma_z^i + \frac{\hbar\Omega}{2} E_z \sum_{i=1}^{N} \left(\hat{a} + \hat{a}^\dagger\right) \hat{\sigma}_x^i, \tag{33.31}$$

where the prefactor of the second term is now interpreted as the qubit/dimer splitting. This has been used to show that a pulsed source can be used to generate many-body correlations in light-matter systems and to determine the time evolution of an N qubit system coupled to the global resonator [160]. A similar approach has been used where the atoms are replaced by exciton levels in charged quantum dots [161] to produce a three-qubit system. In a slightly different approach, two qubits are encoded in the modes of the optical cavity that is coupled to a three-level atom within the cavity [162]. Going a step further, a multi-resonator system has been coupled to a multi-target qubit to produce another type of phase gate [163].

An actual optical system has been integrated on a silicon process to make an effective optical processing chip. In this case, optical ring resonators are coupled to photon-pair sources to produce a path-entangled two qubit state [164]. The schematic of the chip is shown in Fig. 33.11. The laser pump pulse enters from the left and produces a superposition of photon pairs via four-wave mixing with the photon pairs from the resonator. This spontaneous four-wave mixing is a result of the third-order nonlinearity of the silicon waveguide core. Hence, these photon pairs are produced on the chip. The two constituents of the pair are referred to as the signal and idler frequencies, which are equally spaced on either side of the original laser pulse. The two photon source/resonator serves to annihilate two photons from the pump pulse and create the two new photons that are the constituents of the output pair. This pair is then separated into separate paths for the blue and red photons (the high-signal and low-idler frequencies of the pair). This process is done in both the upper path and lower path, and then photons from each of the two paths are entangled in the central section of the chip. The remainder of the chip analyzes the results optically with single-photon counting detectors. These authors have shown that silicon photonics can be used to prepare and manipulate delicate quantum entanglement.

As we have seen in the above discussion, entangled path-encoded qubits can be generated by coherently pumping two photon-pair sources. While the above were generated using four-wave mixing, they can also be created by parametric down conversion [165]. With this in mind, it has been shown how an entire large-scale programmable optical processor can be integrated onto a chip [166]. The photon pair generation can be handled using a photonic hybrid laser based upon silicon [167]. A different chip from Fig. 33.11 has recently been created that also exhibits two-qubit entanglement with integrated optics on a silicon platform [168, 169]. In addition, a chip has been made to entangle higher-dimensional quantum states, called qudits (a qubit is two dimensional, a qutrit is three dimensional, etc.) [170]. Generation of single quantum emitters has been integrated on chip as well [171].

Possible other types of photonics circuits for quantum communications have been reviewed in [172]. Since then, there have been several possible integration approaches for these quantum communications applications [173–175]. Finally, there has been at least one strong argument for the use of photonics for processing, either quantum computing or quantum communications [176].

33.6 Other Qubits

As we pointed out above, quantum computers begin with the qubits. So far, we have described the most common qubits that are in use. But, there are other solid-state qubits that are under consideration, and some of these may prove fruitful. Here, we discuss a few of these. But as before, it is important to understand that this brief section is the state of the art in late 2019, and it may well change within a few short years.

33.6.1 NV Centers

The nitrogen-vacancy (NV) complex centers have been considered for possible qubits for the past few years [177, 178]. The most common material in which this has been created is diamond, a wide band gap semiconductor (5.47 eV). These NV centers are one kind of defect often referred to as a "color center." There are a variety of actual N and V configurations within the crystal structure, each of which produces a different range of defect energy levels [179]. While the center has been found in GaAs [180] and SiC [181–183], diamond remains the most common carrier. The various levels for these centers can be in the infrared or visible for use in these qubit applications. And, the nature of the qubit structure varies, as some approaches use the coupling of the electronic and nuclear spins [184], while others couple the electronic spin to a strain in the crystal [185]. In the latter case, the divacancy has also been used [180].

Normally, the configuration used is with a substitutional nitrogen atom on the diamond lattice with an adjacent vacancy. This NV center is usually discussed in terms of a six-

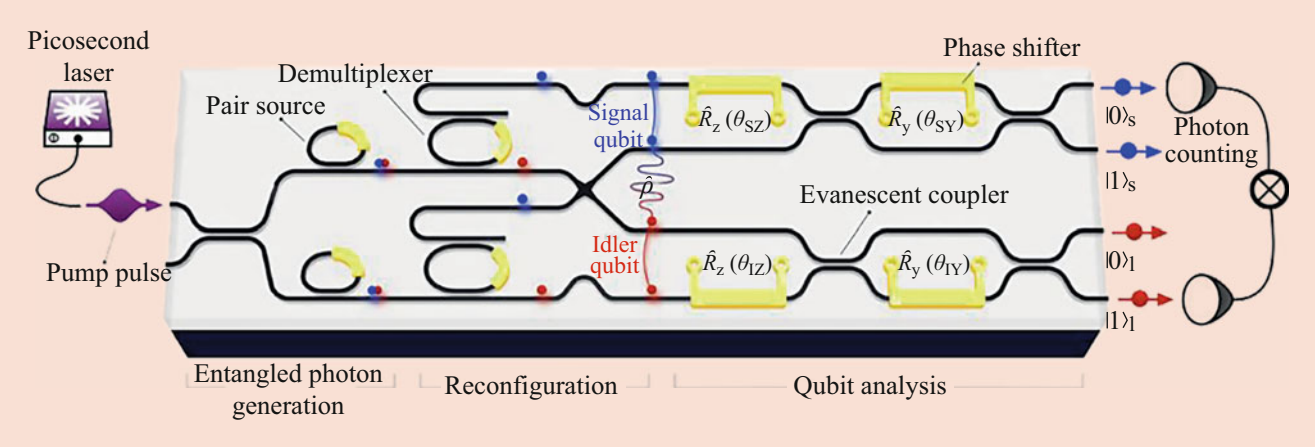

Fig. 33.11 Schematic layout of the silicon photonics chip. A laser pulse is coupled to the chip, where it creates a superposition of photon pairs via spontaneous four-wave mixing. This superposition is separated into blue (high frequency) and red (lower frequency) path qubits, which are analyzed by two interferometers incorporating phase shifters. Photons at the output are separated from the residual pump signal by fiber wavelength-division multiplexers and collected by single-photon detectors. (Reprinted under the Creative Commons 4.0 license from J. W. Silverstone et al., "Qubit entanglement between ring-resonator photon-pair sources on a silicon chip," Nature Commun. **6**, 7948 (2015), copyright 2015 by Nature-Macmillan)

electron model [186]. In this model for the negatively charged center, there is a ground state of an ^{3}A spin triplet, with a zero-field splitting of 11.88 μV between the $m_S = 0$ and the $m_S = \pm 1$ sub levels. The degeneracy of the $m_S = \pm 1$ can be lifted with an external magnetic field, so that either one of these levels, together with the $m_S = 0$ level, form a well-defined two-level system. This two-level system is the physical realization of the qubit [187]. The spin states can be polarized by excitation of an electron to the upper ^{3}E triplet with a green laser and then readout by using the florescence. The quantum state of this spin qubit can be manipulated with the application of a microwave signal [184], especially to affect the interaction between this two-level system and the hyperfine interaction with neighboring ^{13}C atoms. This role of the microwaves can be reversed in that the qubit can be used to sense the presence of the microwaves [188]. Similarly, newer techniques (than above) have been developed to achieve readout of the spin state in a single shot [189].

Now, the problem with using the lower states and their splitting by ∼12 μV is that these states have no chance to push the qubit to room temperature. In SiC, the NV centers appear as nearest neighbor pairs, with the same electronic structure of a ^{3}A triplet ground state and a ^{3}E excited state [190]. In 3C-SiC, a zero phonon line has been predicted at a wavelength of 1.5 μm [191], which could lead to creating a spin qubit with a relatively long lifetime. Experiments have demonstrated three such zero phonon lines in the near infrared, with a line at 1.468 nm being assigned to the transition between the excited and ground states of the NV^- center, showing that this center can be used for quantum communications [183]. Then, it has been shown that one can entangle the qubits formed from two NV centers in diamond via a damped mechanical resonator [192]. Then, the NV center in a nano-diamond crystal was used to show photon bunching and anti-bunching properties and to provide the nonlinearity needed to create four-wave mixing with visible lasers at nitrogen temperatures [193].

The ability to work at higher temperatures may suggest that the NV center will be useful as a quantum memory even if the main qubit computation system is at low temperature. In any case, quantum memories remain a significant problem which can be addressed via these NV centers. A necessary requirement is to protect the qubit of the NV center in a manner to extend the coherence time. The nuclear spin qubit of the neutral NV center has been lengthened through the control by nanometer scale gate electrodes [194]. Another approach used the spin of the NV center and protected it by decoupling the noise environment from the qubit [195]. Then, a so-called loop-gap resonator was shown suitable for applications with spin-based hybrid quantum systems and tested with the NV centers in diamond [196]. Finally, the spin NV center in diamond has been coupled to a superconducting transmon qubit [197] and a superconducting flux qubit mediated by a ferromagnet [198].

Recently a room temperature two-qubit quantum gate has been demonstrated using the electron-nuclear entanglement of the nitrogen-vacancy center in diamond [199]. In this process, the gate functions via microwave control of the geometric phase in a manner that demonstrated nonadiabatic and non-Abelian holonomic control with the polarized microwaves. The operation is demonstrated pictorially in Fig. 33.12. Similar spin entanglement of the nuclear spins has also been achieved with a mechanical resonator [200].

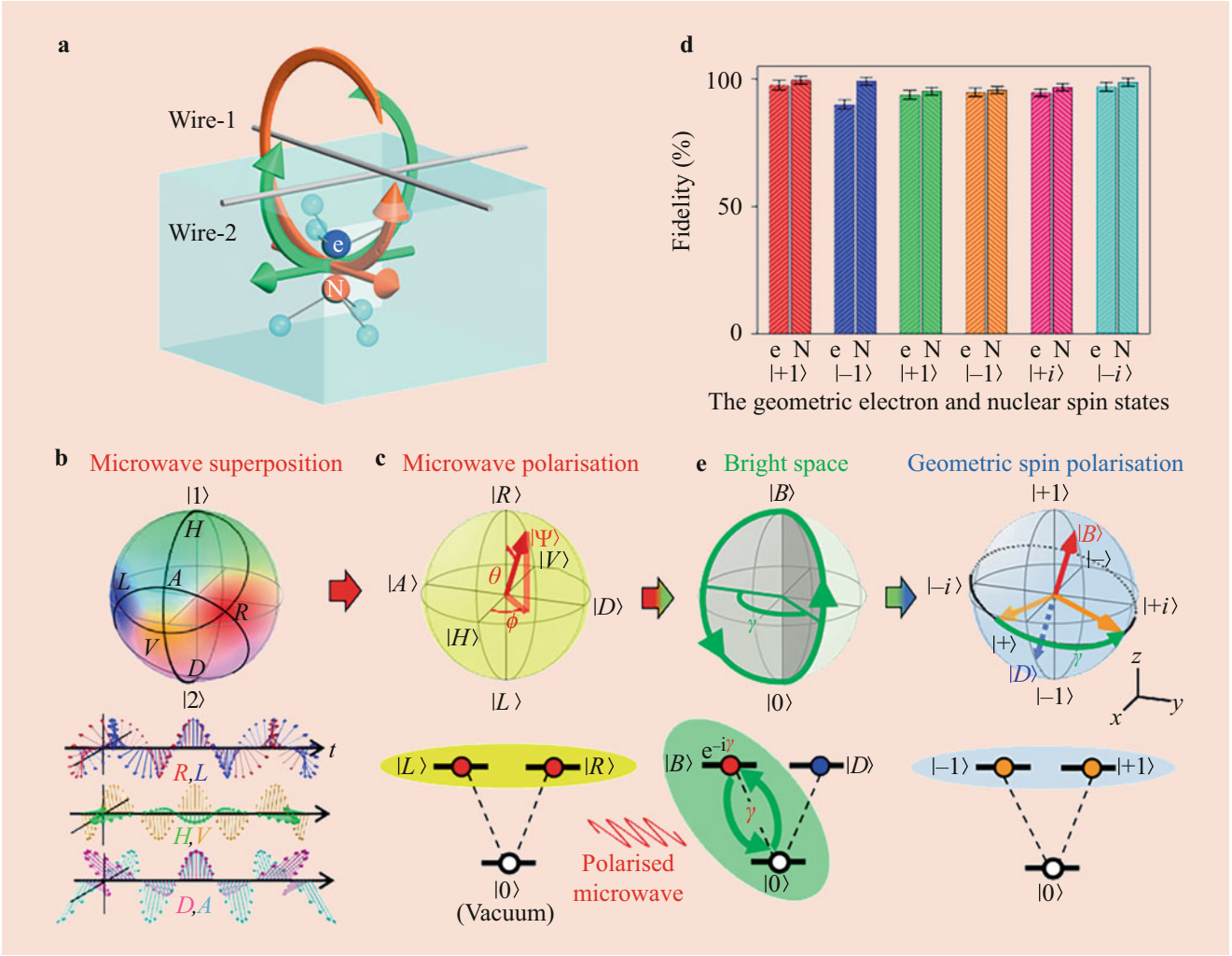

Fig. 33.12 Polarization-based holonomic quantum gates. (**a**) The configuration of the two crossed wires to produce a polarized microwave at the position of an NV center. (**b**) Mapping from the relative amplitude and phase of the microwaves generated by the two crossed wires into the polarizations effective for the electron or nitrogen (^{14}N) nuclear spin in an NV center under a realistic configuration. The $|1\rangle$ and $|2\rangle$ represent microwaves generated from, respectively, wires 1 and 2. (**c**) The mechanism underlying the holonomic quantum gate. The polarized microwaves induce a cyclic evolution of the geometric spin in the bright space based on the bright state $|\beta\rangle$ and the ancillary state $|0\rangle$ with a solid angle 2γ to induce a geometric phase γ on $|\beta\rangle$, resulting in the rotation of the geometric spin around an angle defined by $|\beta\rangle$ and the unchanged dark state $|D\rangle$. (**d**) The fidelities of the state preparation and measurement for the geometric electron (**e**) and nitrogen nuclear (N) spin. Error bars are defined as the s.d. of the photon shot noise. (Reproduced from K. Nagata, K. Kuramitani, Y. Sekiguchi, and H. Kosaka: "Universal holonomic quantum gates over geometric spin qubits with polarized microwaves," Nature Comm. **9**, 3227 (2018) under the Creative Commons 4.0 license, copyright 2018 by Nature Communications)

More extensively, it has been shown that radio-frequency pulses can be used to demonstrate initialization, control, and readout of an ensemble of nuclear spins in NV centers [201]. Such a quantum system has also been created by coupling the ensemble of NV centers to surface polaritons [202].

33.6.2 Braiding

Quite generally, the idea of braiding can be connected to the method of which strands of hair are interleaved to form the braids of the hair. In essence, we move strands around other strands, and a mathematical theory for this arises from knot theory [203]. In physics, the importance of knots lies in the interpretation and analysis of graphs, such as the state transition graphs in computer science. For a graph with n vertices, one must evaluate $2n$ possible states of the system in order to compute the partition function. It can easily be imagined that this is a difficult and complex problem. Hence, one has to devise clever means to avoid such a calculation, and one approach is given by the Yang-Baxter equation [204, 205]. Basically, the equation is based upon the idea that particles may preserve their momentum even while scattering

and changing their quantum states. This becomes important to knot theory and the ideas of braid groups through the definition of an R matrix which describes the swapping of two strands (or braids). And, when we apply this idea to quantum computing, we find that such matrix operators provide the operations of quantum gates [206]. As a result, we can use evolution of topologically stabilized states as the basis for the braids, and quantum computing is obtained by the interchanges of these braids. Hence, in the idea of a topological quantum computer, we merely push quasi-particle excitations of some two-dimensional systems around each other. The true significance of the topological approach is the stability provided which means that one likely does not need error correction. The motion of each quasi-particle forms its own braid in $2+1$ dimensions (two spatial dimensions plus time). More importantly, it has subsequently been shown that we only need a single mobile "quasi-particle" in order to do the computation [207]. This has led to a more intense study of braid groups and the discovery of new types [208, 209] as well as approaches to optimizing the choice of braids [210]. A recent review has discussed the character of various braids and their system usage [211].

Braiding was recognized quite early as a method for implementing quantum computing, particularly with anyons. Anyons are generalized quasi-particles in two-dimensional systems, that is, they can be fermions or bosons. In particular, they can be used in quantized systems such as the quantum Hall effect, where the anyon is a quasi-particle moving in one of the edge states. Moreover these states are topologically stabilized, so generally are difficult to create or destroy, which gives some "error correction" to these states in quantum computing [212]. One belief is that appropriate theories to describe the incompressible quantum Hall state are the Chern-Simons gauge theories, in which it is the vortex, or flux tube, that provides the exotic quantum statistics that characterizes the interactions of the quasi-particles in the fractional quantum Hall effect [213]. These interactions move the quasi-holes in a manner that causes the representative wave functions to be multiplied by phase factors and hence furnish a one-dimensional representation of the braid group. Subsequently, experiments were carried out in a unique experiment in which fractional quantum Hall edge states where circulated within an open quantum dot with varying density ([214] see also [215]). Here, the outer edge states were in the 1/3 state, while the inner edge states were in the 2/5 state. The quasi-particles of the 1/3 state circulated around those of the 2/5 state and thus accumulated statistical phase. They found that the phase difference in this process created a shift of $-2\pi/15$, clearly demonstrating the correctness of the braiding assumption. At about the same time, there were theoretical suggestions supporting the idea of using the 2/5 state to generate non-Abelian statistics [216, 217].

At this point, it is probably useful to remind ourselves that Microsoft is pursuing topological quantum computing in its quest to build a quantum computer. More recently, this group has shown that the braiding operation can be done by using an anionic quantum state teleportation, which removes the need to physically transport the anyons around each other [218]. Different fractional Hall state descriptions have appeared, but it seems that it is the state and not its wave function representation that is important [219, 220]. An advantage of the anyon approach is that it should be inherently insensitive to noise in the system, and protocols can be developed to assure this insensitivity [221]. But, it has been pointed out that using the fractional quantum Hall state anyons can implement only a certain set of qubit operations [222] and that new geometric operations are required to realize universal quantum computers. Recently, an approach using lattice models for the anyons has appeared [223]. Finally, an experiment has shown that anyon braiding for qubits created with superconducting circuits composing 7 qubits can obtain a state fidelity of 0.688, for which anyonic excitations and braiding were achieved in single qubit operations [224].

A few years ago, it was realized that one could effectively stabilize the simplest type of non-Abelian anyon in a computing application by using the topological properties. In particular, this state is a defect binding Majorana fermions. Indeed, by combining a "standard" fractional quantum Hall device with a standard superconductor, the resulting structure could support exotic non-Abelian defects with a parafermion, which is a generalized Majorana bound state [225]. Now, the Majorana fermion is itself a rather exotic particle. Ettore Majorana hypothesized the existence of a zero energy particle as a solution to the Dirac equation, which would be its own anti-particle [226]. (Shortly after this, he apparently disappeared in what has become a scientific mystery.) The mention of the Majorana fermion in connection with a topological insulator material and proximity superconductivity seems first to have occurred in 2008 [227], although the possibilities of their use in computing are somewhat earlier. Then experiments using proximity superconductivity in InSb nanowires, which have a large spin-orbit coupling allowing the spins to be separated in a magnetic field, coupled to a topological superconductor, exhibited possible signs of the existence of the Majorana fermion [228]. However, braiding operations are not possible in single nanowires since the exchange operation of two Majorana fermions, located at the edge of a nanowire will cause them to annihilate when they meet. Hence, nanowires need to have an extra leg section to locate one particle, while the other moves around [229]. Yet, there has been progress in using nanowires coupled to superconducting islands to create circuits capable of quantum computing [230].

Then, it has been shown experimentally that a microwave signal can induce Rabi oscillations between adjacent Majo-

rana bound states, and this creates a single qubit gate [231]. In proceeding with the introduction of topological insulators, the desired protected states are surface states. Since they occur on opposite surfaces, this can complicate their use. It has been recently shown that these can be decoupled with "normal" gating operations [51]. Additionally, it has been shown that in the non-Abelian braiding of surface code (surface codes are various error correcting codes that depend upon the nature of the topological surface in use. One form is the toric code, so named because of the two-dimensional surface being wrapped onto the two torus), defects, which can be moved as if they were particles (similar to the Majorana fermions), one can obtain multi-qubit operations [232]. Other novel circuits have also been proposed to achieve quantum computing with Majoranas [233]. While there are many approaches, the nanowire circuits have received the most attention in recent years. Studies of the nanowires themselves have used crossed InSb nanowires. These have shown that ballistic transport is present as indicated by conductance plateaus, which means that the nanowires are not dominated by any disorder [234]. This conductance quantization also occurs with the Majoranas [235]. Then, a structure coupling a 3D Dirac semi-metal (Cd_3As_2) nanowire with superconducting Nb contacts has been studied as well [236].

33.6.3 Surface Bonds

There is a new approach to a silicon qubit, based upon a surface dangling bond. It has long been known that one could saturate the two bonds per atom that were not saturated at the [100] silicon surface by introducing hydrogen (or deuterium). This covers the surface and fully saturates these bonds. By using an STM, one can then remove selected hydrogen atoms to produce a single dangling bond. One can then attach another atom (such as the P atom discussed above [62]) or molecule for the purpose of further study. It has also been demonstrated that the dangling bond itself has two states that can be used for charge transitions that could be adapted to serve as a qubit [237]. The bond acts as a quantum dot, and such dots can be separated by as little as adjacent atoms, and are certainly of sub-nanometer dimension. Moreover, the quantum dot can have several electron trapping states. When pairs are created at adjacent atoms, there can be very high tunneling rates between them [238]. In fact, creating a line of such quantum dots can create an "atomic" wire with appropriate transport properties [239] and which can be gated. More importantly, the carrier capture rates at each quantum dot can be tuned with external gates [240]. Finally, it has been demonstrated that single charges can be controllably moved between two wells, in a chain of paired quantum wells, in such a manner that one can consider how these chains can be used to created qubit gates useful in quantum computing [241]. In general, the charge state can be manipulated in a manner to place its energy level above or below the bulk Fermi level by as much as a few hundred meV, which suggests that this process may be useful at room temperature. Nearly all current embodiments of quantum computers work at extremely low temperatures. The possibility of room temperature operation should open a new approach to creating quantum computers.

33.6.4 Flying Qubits

The idea of flying qubits lies in the use of a single propagating electron as an implementation of a qubit. The idea began in the work of Bertoni et al. [242], where the electron arrives in one quantum wire and either transfers, or not, to a second quantum wire. A more recent implementation has been given by Yamamoto et al. [243], in which an Aharonov-Bohm ring has entrance and exit ports composed of two parallel quantum wires. These parallel wires replace the normal single wire entrance and exit of such a ring, and the purpose is to control tunneling between the two wires in these ports. However, as these authors point out, the study of tunneling between two such quantum wires is much older [244]. Subsequently, the tunneling from one quantum wire to a side wire was studied theoretically [245]. Later, the coupling between two quantum wires, mediated by a quantum dot, through which the coupling occurred, was studied experimentally [246]. This work was later extended by replacing the quantum dot with a simple quantum point contact [247], which is more in keeping with the structures studied by the Modena group [248–250]. Most recently, the flying qubits have been suggested for quantum Hall edge states [251].

While the idea of the flying qubit continues to excite effort on the part of many groups [252], it is not clear that it will make much of an impact on the commercial efforts discussed in Sect. 33.1.4. However, conceptually, this type of qubit may have as much chance as the NV centers discussed in Sect. 33.6.1. But, there are many questions that can arise over the use of quantum-Hall states for the flying qubit. First, of course, is the fact that the stability of the edge states lies to some extent in the presence of charge in them. The separation of the different edge states, and their stability, arises from the many-body interactions between the electrons that result in compressible and incompressible regions [253, 254], a situation which has been imaged by scanning gate microscopy [255]. Will the desired flying qubit reside in an otherwise empty edge state, or will it ride on top of an already present density of electrons? If the former, how sensitive is it to noise in the magnetic field; when it is known that a variation of one flux quantum at the onset of occupation of the next edge state can lead to fractionally charged excitations [256]? Then, of course, there is the fact the quantum Hall edge states are more normally connected with the topological stability and use in

the braiding approach to quantum computing being pursued by Microsoft.

33.7 Summary and Conclusions

If we refer back to Sect. 33.1.4, we know that most prospective quantum computers are focused on using the Josephson technology. And, from the rest of this chapter, it is easy to see that this approach is the most advanced of several possible approaches. In all of these approaches, we are dealing with nanoelectronics. This is expected as this is the industry with the ability to manufacture the needed chips. But, we cannot know which of these technologies will evolve to become the leader in 5 or 15 years. Even optical approaches to quantum computing, which deals more with microelectronics than the nano version, depend upon the ability to produce the chips. And, it is highly likely, with blue lasers, that the optical approach will evolve into nanoelectronics. But, we still must consider that the goal is not to just make quantum computers, but to make quantum computers that operate at room temperature and are general-purpose machines. An important additional consideration is: If these remain special purpose machines operating at very low temperatures, are the results worth the tremendous costs that have been, and will continue to be, expended in the quest to develop these machines.

Another consideration, also mentioned in Sect. 33.1.4, is whether the results obtained in test machines, such as the IBM five-qubit system, can be believed. That is, are they sufficiently accurate? We have to remember that to work on a small system, like the five-qubit machine, the problem has to be parsed into small segments for which the five qubits can process. This means that the control signals, the presence of cache (quantum memory), and transfer systems all must work error-free. Moreover, it is hard to assign where the error occurs. It is well recognized that quantum memory remains a significant problem. The qubits themselves may be functioning in an exact manner, but failure of the other parts provides many possible sources that can contribute to erroneous results. Some of these answers may well come from the studies being carried out on the IBM supercomputer to which the quantum processor has been attached.

Then there is the question of how many qubits are needed to create a general purpose quantum computer. For sure, the five-qubit IBM chip may not be the answer. Predictions that we need millions or billions of qubits are pushing a little too far. The answer needs to be closer to the design of the machine which may not be that different from a classical machine. Numbers like 10^{300} which are bandied about (along with statements that this is more than the sum of all the particles in the universe) are somewhat off-base. Numbers of this size have been used in computers for more than half a century. They are handled with floating point numbers, which have a mantissa and an exponent. And, at least in today's laptops, they are handled with processing registers that are typically only 64–128 bits long. The point is that, it is not the size of the number that is important; it is the accuracy with which you want to know the number. That means that if I want to factor a very large integer, do I need hundreds of qubits, or can I get by with parsing the procedure into smaller segments. Hence, the question is whether or not Shor's algorithm for factoring can be parsed into smaller segments while still controlling the quantum coherence through the entire set of numbers. And, then the question becomes one of determining just how long we can extend the coherence time. In this regard, the technical inquiry shifts from the science of the qubit to that of the quantum system in its entirety, which is the subject of another field.

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Part IV

Modeling

Compact/SPICE Modeling

34

Wladek Grabinski and Daniel Tomaszewski

Contents

34.1 Introduction . . . 1233

34.2 Passive SPICE Models . . . 1234
34.2.1 Resistor . . . 1234
34.2.2 Resistor R3_CMC . . . 1235
34.2.3 Thin Film Resistor . . . 1235
34.2.4 Capacitor . . . 1235
34.2.5 Moscap . . . 1235
34.2.6 Capacitor with Frequency-Dependent Capacitance . . . 1236
34.2.7 Chip Capacitor . . . 1236
34.2.8 CPW Capacitor . . . 1236
34.2.9 Inductor . . . 1236
34.2.10 Inductor Coupling Coefficient . . . 1237
34.2.11 Linear Controlled Sources . . . 1237
34.2.12 Dynamic Nonlinear Sources . . . 1238
34.2.13 Transmission Lines . . . 1238
34.2.14 Linear Models for Transmission Line Systems . . . 1238

34.3 Active SPICE Models . . . 1239
34.3.1 Diode . . . 1239
34.3.2 Photo Diode . . . 1240
34.3.3 Fowler-Nordheim Diode . . . 1240
34.3.4 BJT . . . 1240
34.3.5 MOSFETs . . . 1243
34.3.6 SOI MOSFET Models . . . 1247
34.3.7 JFETs . . . 1250

34.4 HV/Power Compact Models . . . 1252
34.4.1 LDMOS . . . 1252
34.4.2 MM20 LDMOS Model . . . 1252
34.4.3 HiSIM-HV: A Compact Model . . . 1252

34.5 Organic TFT . . . 1252
34.5.1 RPI a-Si TFT Model . . . 1253
34.5.2 AIM-SPICE MOS15 . . . 1253

34.6 Progressive Modeling Directions . . . 1253
34.6.1 Single-Electron Transistors (SET) . . . 1253
34.6.2 Quantum Dot . . . 1253
34.6.3 Resonant Tunneling Diode . . . 1254
34.6.4 Rapid Single-Flux Quantum (RSFQ) Device . . . 1254
34.6.5 Memristor . . . 1254
34.6.6 Negative Capacitance Model . . . 1254
34.6.7 Magnetic Tunnel Junction . . . 1254

34.7 Conclusions . . . 1255

References . . . 1255

Abstract

The microelectronics and nano-electronics industry strongly relies on compact models to reduce a new microelectronic product development costs. The goals of this review are to highlight critical issues for the development of compact models for microelectronics and nano-electronics. In this chapter, we've covered the main principles of the compact device modeling. Also discussed are the possibilities of integrating compact models into circuit simulation and design tools, with an emphasis on the Verilog-A standardization, which simplify model implementation into EDA tool.

Keywords

Compact models · SPICE · Verilog-A standardization · Equivalent circuits · IC design · Semiconductors · Modeling · Simulation

34.1 Introduction

The accuracy of the circuit-level simulation results in computer-aided design (CAD) is always proportional to the accuracy of the models. Having "ideal" mathematical descriptions for all components, the computer circuit

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simulation program (e.g., SPICE [60]) produces "ideal" results, within the machine's capability. It is unfortunate that the models of some devices are sometimes quite difficult to obtain and many specific cases must be approximated. Selected SPICE models which are reasonably accurate for a wide variety of IC applications are available and are presented in this chapter. There are two basic steps in device modeling. The first step is to develop the mathematical equations or the equivalent circuit which is to represent the particular semiconductor device. The second step, which goes beyond the scope of this chapter, is to determine how to obtain the parameters, which are necessary for the equivalent device representation. Many equivalent circuits have been presented in the literature for various devices.

In this chapter, equivalent circuits are presented for the six most common semiconductor devices. The models presented are not, in all cases, the most sophisticated possible. In fact, some of the models may always need further improvements. These SPICE models do, however, give excellent results in most applications. The measurement procedures are purposely developed using the minimum of complex equipment, in order to make the process available to the widest variety of users.

In addition to illustrating the model and showing the measurement procedures, each device is used in a SPICE application, which verifies to some extent the model obtained. Obviously, for complete verification, many additional tests must be made; however, those shown illustrate the procedure. The device models presented in each section are not derived or developed in this text. References are given for the interested reader; however, the measurement techniques which are not generally available are described in great detail.

A set of programs have been developed for the characterization of the DC and transient behavior of MOS integrated circuits. The DC analysis program calculates and plots the voltage transfer and power dissipation characteristic of an MOS inverter approached from a new point of view. The algorithm enables the characterization of basic MOS IC cells on desktop calculators. The program for the transient characterization calculates and plots the output waveform of three simple MOS cells most often occurring in MOS ICs. The MOS transistor is simulated in terms of a four-terminal large-signal model described by device processing parameters. Complex MOS ICs can be also characterized by appropriately combining earlier SPICE programs [100,101]. Compact device modeling is a very critical issue in microelectronics and nano-electronics because compact models are the type of device models used in circuit simulation and design tools. 2D and 3D numerical simulators are too cumbersome and too much time-consuming to be used in circuits with hundreds or thousands of devices. Compact models, with an analytical or semi-analytical formulation, are therefore of crucial importance for the microelectronics and nano-electronics and sensor industry. Circuit design is not possible without accurate compact models for the devices which are components of the targeted circuits. The application of new device technologies is only feasible when compact models for those new devices are available. Compact model implementation and its simulator validation are also discussed at such open forums like MOS-AK [69] and NEEDS of NanoHub [70], IEEE EDS Compact Modeling Technical Committee [68], series of the compact modeling workshops [61,71], as well as industrial Si2 Compact Modeling Coalition (CMC) [64].

34.2 Passive SPICE Models

This section reviews basic passive SPICE models for circuit simulations and IC design.

34.2.1 Resistor

The resistor model values depend on the process-related device data that allow resistance calculations from its geometric layout information and also include temperature dependence.

General SPICE R instance is:

```
Rname N1 N2 VALUE
```

where N1 and N1 are the positive and negative element nodes, respectively, and VALUE is the resistance in Ohms (Ω), which should not be equal to zero (0). The nominal resistance is calculated knowing the sheet resistance RSH, the geometrical parameter NARROW, and L and W geometries of the resistor device:

$$R = \mathrm{RSH}\frac{L - \mathrm{NARROW}}{W - \mathrm{NARROW}} \tag{34.1}$$

and its temperature dependence follows a simple quadratic scaling rule:

$$R(T) = R\,(T_0)\left[1 + \mathrm{TC1}\,(T - T_0) + \mathrm{TC2}\,(T - T_0)^2\right] \tag{34.2}$$

where TC1 and TC1 the temperature scaling coefficients is in Ω/°C and Ω/°C^2, respectively (Fig. 34.1).

Fig. 34.1 R SPICE symbol

34.2.2 Resistor R3_CMC

R3_CMC 3-terminal resistor model is a three-terminal nonlinear (diffused and polysilicon) resistor element and JFET model [56]. R3_CMC is Verilog-A-based and implemented accordingly [64]. The R3_CMC-*type* parameter controls the p or n type of the substrate. The extraction and simulation of the temperature parameters are controlled using the *tnom* and *trise* parameters, respectively. Parameter default and truncation values are identical to those found in the standard Verilog-A model code. In addition to modeling the depletion pinching effect, accurate modeling of highly linear resistors involves modeling correct velocity saturation. Modeling short devices is considered important only for velocity saturation. However, its effect on nonlinearity is important even for the resistors with "long" L resistor dimension. An interesting and useful way to analyze this phenomenon is in a reciprocal sense, as an effect on mobility:

$$\mu_{\text{red}}(E) = \mu_0/\mu(E) \tag{34.3}$$

There are two common models for μ_{red}; they are:

$$\begin{aligned} \mu_{\text{red}}(V) &= 1 + \frac{\mu_0}{v_{\text{sat}}}\frac{|V|}{L} \\ \mu_{\text{red}}(V) &= \sqrt{1 + \left(\frac{\mu_0}{v_{\text{sat}}}\frac{|V|}{L}\right)^2} \end{aligned} \tag{34.4}$$

where the symbols have their conventional meaning. The first form is often used for analytic simplicity, the second for improved accuracy and lack of singularity at $V = 0$ bias point. For a general velocity saturation model, the total resistor current can be rewritten as $I_{\text{ds}} = I_{\text{depl}}/\mu_{\text{red}}$.

34.2.3 Thin Film Resistor

Thin film resistors are mainly used for MMIC, coplanar waveguide ICs, and related applications. These elements, the CPW TF resistors, are treated as a lossy CPW line with a complex characteristic impedance. The sheet resistance R_{S} of a CPW TF resistor may be scaled with frequency in accordance with the formula:

$$R_S(f) = R_S(F)\sqrt{\frac{f}{F}} \tag{34.5}$$

The scaling can be activated and estimated in advance:

$$F_{\text{GHz}} = \frac{25.33}{(\sigma 10^{-7})\, t^2} \tag{34.6}$$

where σ is the bulk conductivity of the resistive film in S/m and t the thickness of the resistive film in microns. At this frequency, the thickness of the resistive film is the skin depth. If F is set in accordance with this formula, scaling of R_{s} is implemented only for $F > f$; otherwise, for $f < F$, R_{s} stays constant. Typically, frequency F is very large due to small bulk conductance of the resistive material (e.g., hundreds of gigahertz), and setting $F = 0$ is recommended.

34.2.4 Capacitor

General `SPICE` capacitor C instance:

```
Cname N1 N2 VALUE <IC=INCOND>
```

where: N+ and N- are the positive and negative element nodes, respectively, VALUE is the capacitance in Farads (F), and IC can be used to define initial simulation conditions (Fig. 34.2).

34.2.5 Moscap

Standard MOS varactor `SPICE` modeling is based on the simplified expressions for the capacitance, which has limited application in transient simulation compared to charge-based modeling [99]. Applying analytical charge modeling of MOSFETs can be done using surface-potential analysis [76]. To obtain the value of the gate capacitance C_{GB} of an MOS capacitor, the total charge gate charge $Q_{\text{G}} = -Q_{\text{s}} - Q_{\text{o}}$ (where Q_{s} and Q_{o} are the silicon and fixed interface charges) has to be calculated accordingly:

$$\begin{aligned} V_{\text{GB}} &= V_{\text{FB}} + \psi \\ &\quad + \gamma\,\text{sgn}(\psi)[\phi_{\text{t}}(\text{e}^{-(\psi/\phi_{\text{t}})} - 1) + \psi \\ &\quad + \phi_{\text{t}}\text{e}^{(\psi - 2\phi_{\text{F}})/\phi_{\text{t}}} - \text{e}^{-2\phi_{\text{F}}/\phi_{\text{t}}}(\phi_{\text{t}} + \psi)]^{1/2} \end{aligned} \tag{34.7}$$

$$\frac{Q_{\text{G}}}{LWC_{\text{OX}}} = V_{\text{GB}} - V_{\text{FB}} - \psi \tag{34.8}$$

Equations (34.7) and (34.8) have no time dependence. To integrate the frequency-dependent effects of the inversion carriers, a rate equation can be used:

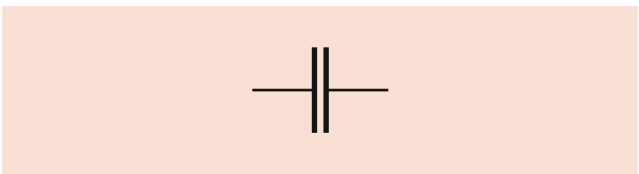

Fig. 34.2 Capacitor C `SPICE` symbol

$$\frac{dQ_I}{dt} = \frac{Q_{I,static} - Q_I}{\tau} \tag{34.9}$$

The time-dependent surface potential in (34.7) can yield convergence in 1–2 Newton iterations for MOSFET modeling above flatband [12]. The AC simulated MOSCAP gate capacitances C_{GB} over a range of frequency ranging from 0.01 to 100 Hz are in Fig. 34.3.

34.2.6 Capacitor with Frequency-Dependent Capacitance

The capacitor with user-specified frequency dependence of capacitance and loss can be modeled too. These models are implemented as a series connection of lossy capacitor and frequency-dependent resistor. Parasitic inductance is in series with a lossy capacitor with L, Q, and R parameters specified as frequency-dependent:

$$R_q(f) = Q(f)/[2\pi f C(f)] \tag{34.10}$$

34.2.7 Chip Capacitor

The chip capacitors are implemented with frequency-dependent Q:

$$Q(f) = Q\left(\frac{f}{FQ}\right)^{\text{ALPH}} \tag{34.11}$$

$$L = \frac{1}{(2\pi FR)^2 C}. \tag{34.12}$$

The impedance Z of the capacitor is given by:

$$Z = \frac{1}{2\pi f C\left(\frac{1}{Q(f)} + j\right)} + j2\pi f L \tag{34.13}$$

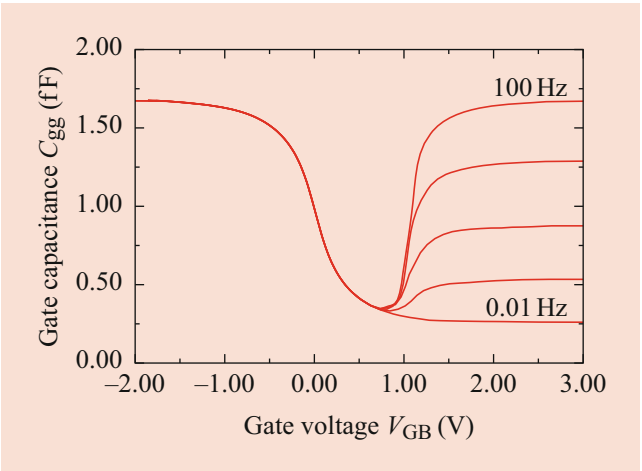

Fig. 34.3 Simulated MOSCAP CV for AC frequency ranging from 0.01 to 100Hz

More advanced chip capacitor models include several important RF phenomena:

- Finite, frequency-dependent Q
- Series and parallel resonance
- Dielectric losses

34.2.8 CPW Capacitor

The models of coplanar waveguide interdigital capacitors represent a transverse metallic strip connecting fingers at both input ports, two lateral grounded conductors, and optional backing ground. To consider interactions between fingers, EM quasi-static coupled lines are used in these models. A coplanar waveguide interdigital capacitor can be modeled using the EM quasi-static technique with a wide range of conductor thicknesses [6]. A quasi-static model can be used for modeling by applying the method of moments by creating a 1D mesh covering the contours of each conductor.

34.2.9 Inductor

The general `SPICE` instance of the inductor model is:

```
Lname N1 N2 VALUE <IC=INCOND>
```

where N+ and N− are the positive and negative element nodes, respectively, and VALUE is the inductance in Henry (H) (Fig. 34.4).

`SPICE` offers several elements and models to analyze inductors in switching regulators, transformers, mutual inductive circuits and other applications. These elements include magnetic winding elements, mutual cores, and magnetic core models, among which are saturable chokes, linear transformers, and transformers. Every inductor model has the effective inductance as a function of temperature with TC1 and TC2 temperature scaling coefficients:

$$L(T) = L\left(1 + TC1(T - T_0) + TC2(T - T_0^2)\right. \tag{34.14}$$

For two inductors L_1 and L_2, the mutual inductance is defined as the coupling coefficient:

$$K = \frac{M}{(L_1 L_2)^{1/2}} \tag{34.15}$$

Fig. 34.4 Inductor L `SPICE` symbol

SPICE transient analysis of the inductors solves the following equations:

$$v_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}$$
$$v_2 = L_2 \frac{di_2}{dt} + M \frac{di_1}{dt} \tag{34.16}$$

In AC simulations, the linear branch relations are:

$$V_1 = (j\omega L_1)\, I_1 + (j\omega M) I_2$$
$$V_2 = (j\omega L_2)\, I_2 + (j\omega M) I_1 \tag{34.17}$$

Nonideal inductors are modeled as SPICE subcircuits with additional elements to define parasitic effects: the DC resistance of the wire R_{DC} and its self-capacitance C_p. These two additional parameter values are easily extracted from the inductor specifications or specific RF measurement. The following example is a SPICE subcircuit inductor model with its simulations results in Fig. 34.5:

```
.SUBCKT IND4EL 1 2
LO  3 2 POLY 1E-3 0 -6.25E-6
RDC 1 3 0.173
CP  1 2 39.6E-12
RP  1 2 250K
.ENDS
```

In a three-element RLC inductor model, given R_p the relation between the quality factor Q, the inductance L, and the self-resonance frequency f_o (see the Fig. 34.5 plot) is given by:

$$Q = \frac{R_p}{2\pi f_o L_o} \tag{34.18}$$

34.2.10 Inductor Coupling Coefficient

Parameter K provides the mutual coupling between inductors. This element is for use between two inductor elements and should be connected to the "K" ports of those elements. The mutual inductance is calculated as:

$$M = K\sqrt{L1L2} \tag{34.19}$$

where M is the mutual inductance, K is the coupling coefficient, $L1$ is the inductance connected at port 1, and $L2$ is the inductance connected at port 2 (see Eq. 34.15).

34.2.11 Linear Controlled Sources

The controlled sources (CC) are standard features of SPICEThe transformation allowed between input and output of a CC is a multidimensional polynomial. With two types (voltage and current) of input and CC output yield four combinations of input/output and are given SPICE device types of E, F, G, and H, respectively:
The E voltage-controlled voltage source (VCVS)
The F current-controlled current source (CCCS)

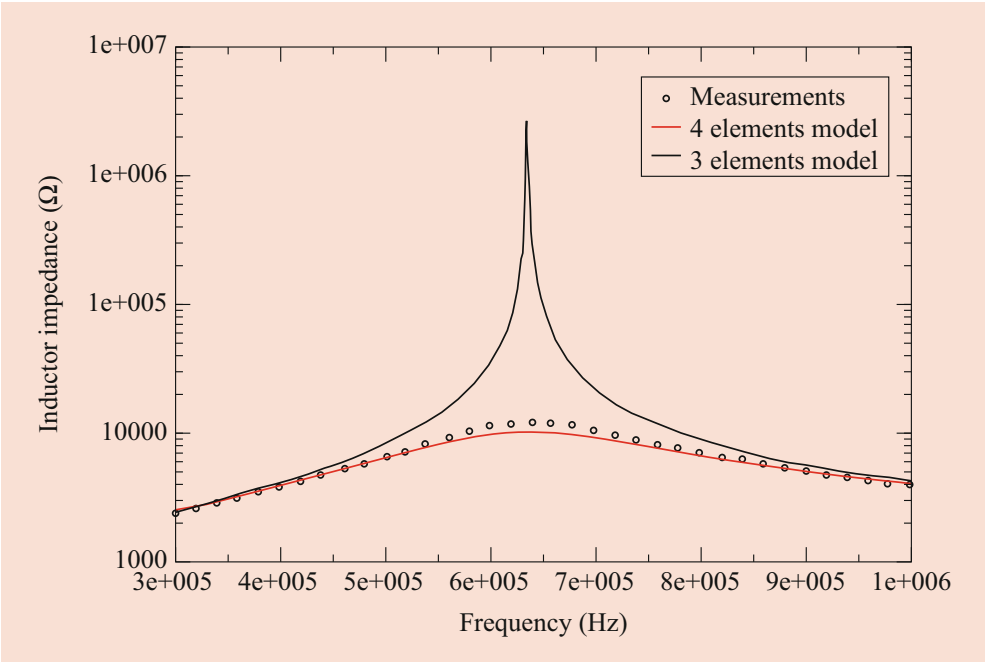

Fig. 34.5 Simulation of two L subcircuit models

The G voltage-controlled current source (VCCS)
The H current-controlled voltage source (CCVS)

These devices act as mathematical functions:
VCVS is the function $v_0 = E(v_1, v_2, v_3, ...)$
CCCS is the function $i_0 = F(i_1, i_2, i_3, \ldots,)$
VCCS is the function $i_0 = G(v_1, v_2, v_3, \ldots)$
CCVS is the function $v_0 = H(i_1, i_2, i_3, ...)$

34.2.12 Dynamic Nonlinear Sources

The behavior of the nonlinear voltage-controlled current (VCCS) or voltage source (VCVS) depends on a given analytical equation EQN. In a simple case, EQN can be defined as:

$$\text{EQN} = A0 + A1V0 + B0V1 \tag{34.20}$$

The voltage variables $V0$ and $V1$ create a four-node source. Three dynamic parameters are created: $A0$, $A1$, and $B0$, accordingly.

34.2.13 Transmission Lines

The SPICE circuit simulator provides three types of models for coupled transmission lines:

- Lumped models
- Distributed models with mutual capacitance C_m and inductance L_m
- Distributed models with decoupled transmission lines

The ideal line is available as a passive network element in SPICE. The corresponding element statement begins with a T and is of the form:

```
T (name) A1 A2 B1 B2
+ Z0 = characteristic impedance
+ (TD = runtime) (IC = .....)
```

where A1 and A2 denote the node names at the beginning of the line and B1 and B2 the node names at the end of the line.

Microstrip lines are formed as planar, conductive strips on a dielectric substrate over a conductive baseplate. Figure 34.6 shows the microstrip line, which is essentially an integrated microwave circuit. Because of the high dielectric of the substrate materials used (e.g., Al_2O_3 with $\epsilon_r = 9.8$), the field lines run predominantly in the substrate between the stripline and the back on ground potential ("ground plane"). The characteristic impedance of the stripline can be used for thin conductor tracks, whose layer thickness is less than a tenth of the web width, and usually can be determined approximately.

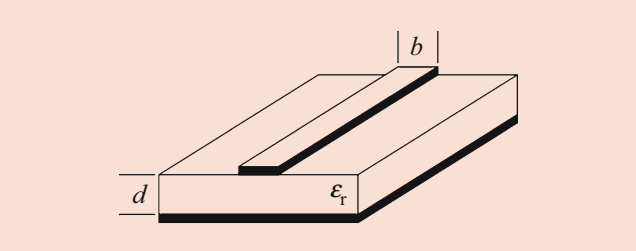

Fig. 34.6 Microstrip line

Thereafter, the following applies to wide lines ($b/d > 1$):

$$Z_0 \approx \frac{120\pi}{\sqrt{\epsilon_r}} \frac{1}{1.393 + b/d + 0.667\ln(1.444 + b/d)} \tag{34.21}$$

The capacitance C' of the microstrip line follows from (34.22) and, for $b/d < 1$ and $b \lesssim \lambda/4$, leads to the approximation formula:

$$Z_0 = \frac{\sqrt{\epsilon_r}}{c_0 C'} \tag{34.22}$$

with ϵ_r the permittivity of selected material and c_0 speed of light in vacuum. By curve fitting to the numerical solutions, it can be shown that for forward stripline design yields Z_0 as:

$$Z_0 \approx \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{b}{d + 0.441b} v\,(\Omega) \tag{34.23}$$

$$C' = 0.556 \frac{\epsilon_{r,\text{eff}}}{\ln[8d/b + b/(4d)]} \quad \left(\frac{\text{pF}}{\text{cm}}\right) \tag{34.24}$$

The corresponding microstrip inductance L' can be calculated using C' and Z_0. In the case of $b/d < 1$, it is

$$L' = 2\ln\left(\frac{8d}{b} + \frac{b}{4d}\right) \quad \left(\frac{\text{nH}}{\text{cm}}\right) \tag{34.25}$$

34.2.14 Linear Models for Transmission Line Systems

Linear models of a distributed transmission line system fit into one of the following categories [89] and can be simulated using free and online CAD tools:

1. Discontinuity Models: These models are meant to predict electrical effects of the connections between transmission line sections. These models include bends, dimensional changes, and the union of up to four transmission lines at a single junction.
2. Transmission Line Models: These models are meant to model the lengths of lines between connections. These models include single lines and coupled lines.

34.3 Active SPICE Models

This section reviews basic active SPICE models for circuit simulations and IC design.

34.3.1 Diode

Standard SPICE diode model implementation allows simulations of the silicon diffused diodes, Zener diodes/pn junctions, Schottky barrier diodes, and nonvolatile memory diodes (with the Fowler-Nordheim tunneling current through gate insulators to model and simulate nonvolatile EEPROM memory effects). The general SPICE instance of the diode model is:

```
Dname N1 N2 MODname <area><OFF><IC=VD0>
```

and SPICE diode model call statement is (Fig. 34.7)

```
.MODEL MODname D <IS=Is N=n ...>>
```

The pn diode model in SPICE is implemented as a voltage-controlled current source which follows the Shockley equation:

$$I_{\mathrm{d}} = I_{\mathrm{s}} \left(\mathrm{e}^{V_{\mathrm{d}}/(N v_{\mathrm{t}})} - 1 \right) \tag{34.26}$$

where:

I_{s} is the saturation current.
V_{d} is the voltage across the pn junction.
N is the nonideality coefficient
v_{t} is the thermal voltage (kT/q).
k Boltzmann constant.
q elementary charge.

to model the IV characteristics of the ideal pn junction diode. Both I_{s} and N model parameters can be easily extracted as the slope and intercept of the semilogarithmic plot of the forward IV diode characteristic. For a reverse-biased diode, the current breakdown occurs at a specific voltage defined as BV; the corresponding breakdown current is set by the IBV parameter value. The diode depletion charge at its pn junction is stored in a voltage-dependent junction capacitance, C_{j} (Fig. 34.8):

$$C_{\mathrm{j}} = C_{\mathrm{j0}} / (1 - V_{\mathrm{j}}/\phi)^{M} \tag{34.27}$$

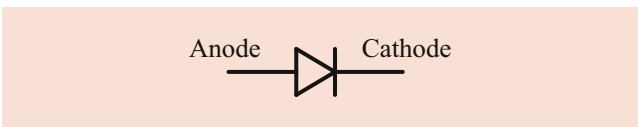

Fig. 34.7 D SPICE symbol

where:

C_{j0} is the zero bias capacitance value.
V_{j} is the junction barrier potential.
M is the grading coefficient ($\frac{1}{2}$ for step and $\frac{1}{3}$ for linearly graded junctions).

Noise diode model is implemented as an independent current sources in parallel with the resistor $\mathrm{RS}_{\mathrm{eff}}$, modeling both noise components: the thermal noise i_{nrs} (34.28) and the shot/flicker noise i_{nd} (34.29) that a resistor generates, using the following equations:

$$i_{\mathrm{nrs}} = \left(\frac{4kT}{\mathrm{RS}_{\mathrm{eff}}} \right)^{1/2} \tag{34.28}$$

$$i_{\mathrm{nd}} = \left(2qi_{\mathrm{d}} + \frac{\mathrm{KF}\,(i_{\mathrm{d}})^{\mathrm{AF}}}{f} \right)^{1/2} \tag{34.29}$$

where KF and AF are SPICE noise model coefficients.

JUNCAP Model

JUNCAP is an advanced model developed by Philips (now NXP). It includes 3D effects from geometrical differences in the sidewall, bottom, and gate-edge-junction profiles; these three contributions are calculated separately. JUNCAP (level=200) model [62] describes all the physical effects: depletion capacitance, ideal diode current, Shockley-Read-Hall recombination and generation currents (in forward and reverse regimes), trap-assisted tunneling (in forward and reverse regimes), band-to-band tunneling, avalanche breakdown, and advanced shot noise. The JUNCAP model uses quasi-static approximations (similar to the MOS modeling of the charge equations) to define current equations and to model corresponding AC effects. The geometrical layout effects are differences in the sidewall, bottom, and

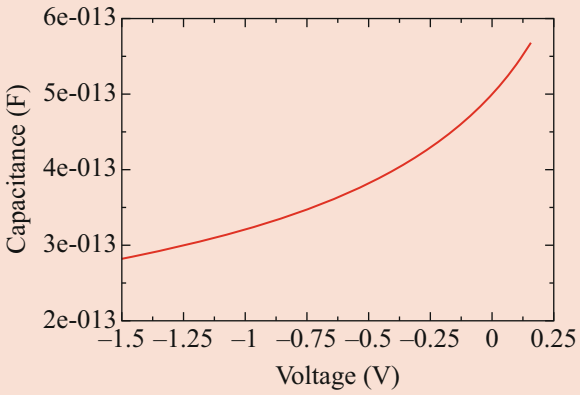

Fig. 34.8 PN diode CV simulations

gate-edge (at a device surface) junction profile contributions to the total current (34.30); the latter includes the diffusion J_d and the generation J_g currents, and the IV characteristic reads:

$$I = J_d \left[n_i^2 + \left(J_g \left(n_i, V \right) \right] \left[\exp\left(\frac{qV}{kT} \right) - 1 \right] \right. \tag{34.30}$$

where n_i is intrinsic carrier concentration with its temperature dependence. The JUNCAP charge of the junction capacitance, with corresponding model parameters P and V_D, reads:

$$Q = Q_j \left[1 - \left(1 - \frac{V}{V_D} \right)^{1-P} \right] \tag{34.31}$$

Finally, total JUNCAP current equations sum all contributions:

$$I = (I_{DB} + I_{GB}) + (I_{DS} + I_{GS}) + (I_{DG} + I_{GG}). \tag{34.32}$$

34.3.2 Photo Diode

The general SPICE instance of the photo diode symbol is (Fig. 34.9) and its simplified model is (Fig. 34.10):

For a photo diode operating in the visible light range, its static characteristic is obtained by solving the continuity equations describing the carrier-transport features of the device. A mathematical model of the photogenerated current density on a pn junction PD was presented [78]. Photodiode stationary 1D continuity equations are solved in the quasi-neutral region along y axis assuming the minority carriers mainly move by diffusion:

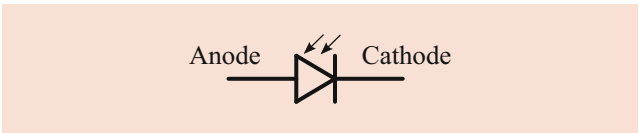

Fig. 34.9 Photodiode SPICE symbol

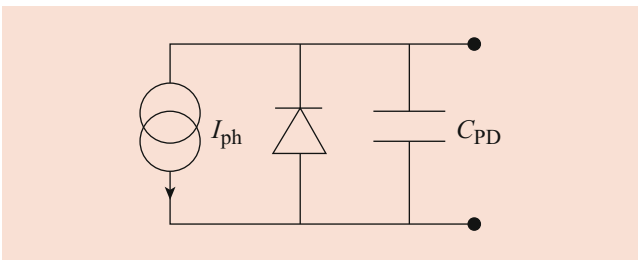

Fig. 34.10 Simplified electrical Verilog-A photodiode model

$$D_n \frac{\partial^2 \left(n_p - n_{p0} \right)}{\partial y^2} - \frac{n_p - n_{p0}}{\tau_n} + G(y) = 0 \tag{34.33}$$

$G(y) = -\partial\Phi/\partial y$ is the optical generation rate, i.e., the number of photogenerated electron-hole pairs per unit volume and time (where Φ is the photon flux). The procedure is similar for holes in the n+ region (Fig. 34.10). The total lateral current component is found by integrating the current density at the boundary of the depletion region over the lateral junction area [10]:

$$I_{ph} = qD_n \frac{8x_{ph}}{y_w} \sum_{n=1}^{\infty} I_1 \left(y_w \right) I_2 \left(x_s \right) I_3 \left(y_j \right) \tag{34.34}$$

Such electrical model has been implemented in Verilog-A [11].

34.3.3 Fowler-Nordheim Diode

Fowler-Nordheim (FN) diode models can be either an MIS or an SIS layer device, assuming its insulator layer is sufficiently thin (100 Å) to permit tunneling of carriers. It models electrically alterable memory cells, air gap switches, and other insulation breakdown devices. Both forward (F) and reverse (R) nonlinear current source DC equations with corresponding $(R \mid F)$ sign of the FN diode are:

$$I_{NFR|F} = \pm A_{eff} J_{R|F} \left(\frac{V_d}{T_{ox}} \right)^2 e^{\frac{E_{R|F} T_{ox}}{V_d}} \tag{34.35}$$

A constant FN diode capacitance is assumed and then defined as:

$$C_{NF} = A_{eff} \frac{\varepsilon_{ox}}{T_{ox}} \tag{34.36}$$

34.3.4 BJT

The general SPICE instance of the bipolar junction transistor (BJT) model is (Fig. 34.11):

```
Qname Nc Nb Ne <Ne> MODname <area><OFF>
+ <IC=Vbeo ...>
```

and the SPICE BJT model call statement is (Fig. 34.12):

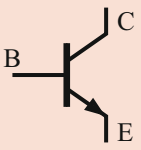

Fig. 34.11 BJT SPICE symbol

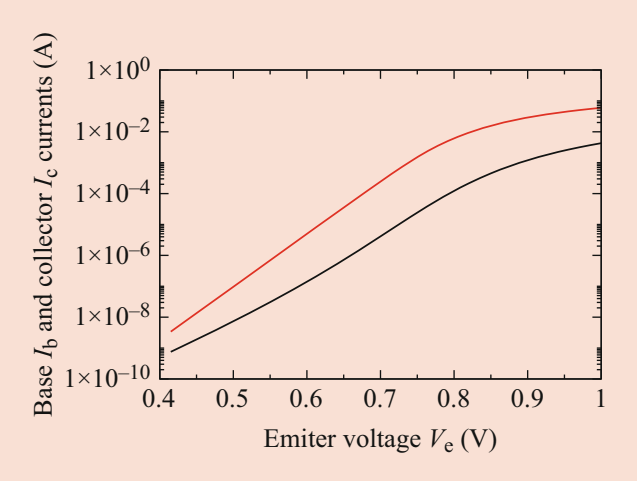

Fig. 34.12 BJT Gummel plot

```
.MODEL MODname NPN/PNP <IS=Is BF=bf
 ...>>
```

Ebers and Moll BJT Model

The Ebers and Moll (EM) BJT model is one of the very first (in 1954), simple nonlinear BJT models; it was proposed by Ebers and Moll [26]. The EM model is valid in all BJT operational regions: saturation, inverse, normal, and off. It is a DC model implementation without any characterization of the charge storage in the device. Basically, all latter BJT DC and large-signal, nonlinear models are referring to the EM model implementation. The injection EM version refers to two current components I_F and I_R, the currents thru the BJT diodes. The EM BJT terminal currents can be mathematically defined following [38], in case of a common base (CB) connected BJT:

$$I_C = \alpha_F I_F - I_R \tag{34.37}$$

$$I_B = (1-\alpha_F)\, I_F + (1-\alpha_R)\, I_R \tag{34.38}$$

$$I_E = -I_F + \alpha_R I_R \tag{34.39}$$

The transport EM model version refers to two current components I_{CC} and I_{EC}, which are flowing thru the BJT diodes; both I_{CC} and I_{EC} represent currents collected or transported across the base:

$$I_C = I_{CC} + \left[-\frac{1}{\alpha_R}\right] I_{EC} \tag{34.40}$$

$$I_B = \left[\frac{1}{\alpha_F} - 1\right] I_{CC} + \left[\frac{1}{\alpha_R} - 1\right] I_{EC} \tag{34.41}$$

$$I_E = \left[-\frac{1}{\alpha_F}\right] I_{CC} + I_{EC}. \tag{34.42}$$

An alternative form of the EM model is its nonlinear hybrid π model as defined in [57], which makes computer linearization to the small-signal model easier.

The EM model has a rather simple temperature dependency and assumes only temperature changes of I_S of the following form:

$$I_S(T) = I_S(T_{nom}) \left[\frac{T}{T_{nom}}\right]^3 \exp\left(\frac{-E_g}{k}\left[\frac{1}{T} - \frac{1}{T_{nom}}\right]\right) \tag{34.43}$$

There are further improvements to the EM model known as EM2 and EM3. The EM2 model allows for a first-order modeling of the charge storage effects to estimate device time responses. It has also a more accurate DC implementation with three ohmic bulk resistances, as well as additional diffusion capacitances C_{DE} and C_{DE} and three junction capacitances C_{jE}, C_{jC}, and C_{SUB}.

Gummel-Poon (GP) BJT Model

The Gummel-Poon (GP) BJT model has been formulated in 1970 [39] and has been implemented into SPICE2 [9, 60]. The element instance for a transistor in the SPICE netlist is:

```
Q(name) CBE <S> Mname <AREA>
```

C denotes the name of the collector node, B the name of the base node, E the name of the emitter node, and S the name of the substrate node, the specification of which is optional. Mname indicates the used transistor model, the parameters of which are shown in a separate .MODEL instruction to be listed. To describe the elements of the wholesale signal model, more than 50 parameters are provided. For NPN, PNP, and lateral PNP transistors, different model instructions are used:

```
.MODEL Mname NPN  (Model parameters)
.MODEL Mname PNP  (Model parameters)
.MODEL Mname LPNP (Model parameters)
```

More complex BJT models for integrated ICs are schematically shown in Fig. 34.13.

The Gummel-Poon model has been well-tested and broadly used model for decades. It delivers sufficient accuracy of the simulation results for many IC design applications. Nevertheless, there are some points in which an improved description is desirable:

- Working point dependency of the standardized base charge q_B for a precise description of the Early effect, of high-injection effects in the base area, and for an HBT with graded base characteristic effects:
- Transit time with high injection
- Base and collector path resistance

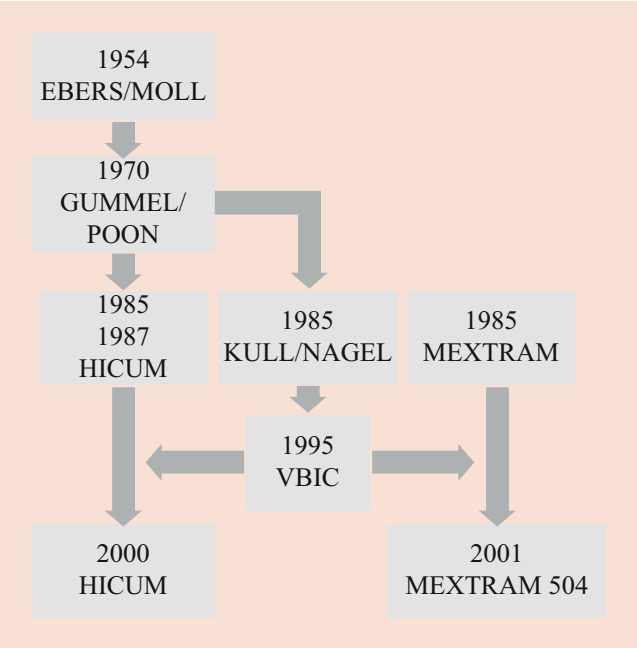

Fig. 34.13 Evolution of advanced BJT models

- Reverse currents and breakthrough
- Temperature dependency, self-heating
- Non-quasi-static effects
- Effects of the pn junction between the collector and the substrate
- Geometry dependencies

VBIC Vertical BJT Model

The VBIC vertical BJT model was developed by representatives of the IC and CAD industries to improve existing, generally used Gummel-Poon `SPICE` model. VBIC includes improved modeling of the Early effect (output conductance), substrate current, quasi-saturation, and behavior over temperature which are necessary for accurate modeling of current state-of-the-art devices. However, it has additionally been defined so that, with default parameters, the model will simplify to be as similar as possible to the Gummel-Poon model [55]. Advantages of VBIC over the Gummel-Poon model include: An Early effect model based on the junction depletion charges A modified Kull model for quasi-saturation valid into the Kirk regime (the high-injection effect at the collector) Inclusion of the parasitic substrate transistor An improved single-piece junction capacitance model for all three junction capacitances Improved static temperature scaling First-order modeling of distributed base and emitter AC and DC crowding Overall improved high-level diffusion capacitance modeling (including quasi-saturation charge) Inclusion of parasitic overlap capacitances Inclusion of the onset of weak avalanche current for the base-collector junction High-order continuity current equations A noise model similar to that of the Gummel-Poon model, with improved shot, thermal, and $1/f$ components

MEXTRAM Model

MEXTRAM bipolar transistor model developed by Philips [24] deploys equations that are explicit functions of the internal branch voltages; therefore, no internal quantities are solved iteratively. Transistor parameters are discussed where relevant; most parameters can be extracted from capacitance, DC, and f_T measurements and are process- and transistor-layout (geometry)-dependent. Initial/predictive parameter sets can be computed from process and layout data. This model does not contain extensive geometrical or process scaling rules (only multiplication factors to put transistors in parallel). The extended modeling of reverse behavior, the increase of the avalanche current when the current density in the epilayer exceeds the doping level, and the distributed high-frequency effect are optional and can be switched on by setting flags. Besides the NPN transistor, a PNP model description is available, both with and without substrate (discrete transistors) modeling. Advantages of MEXTRAM model include: Temperature effects Charge storage effects Substrate effects and parasitic PNP High-injection effects Built-in electric field in base region Bias-dependent Early effect Low-level nonideal base currents Hard- and quasi-saturation conditions Weak avalanche Hot-carrier effects in the collector epilayer Explicit modeling of inactive regions Split base-collector depletion capacitance Current crowding and conductivity modulation for base resistance First-order approximation of distributed high-frequency effects in the intrinsic base (high-frequency current crowding and excess phase shift) In the MEXTRAM model, the Moll-Ross relation is used to take into account the depletion and diffusion charges (Q):

$$I_n = \frac{(I_f - I_r)}{1 + (Qt_e + Qt_c + Qb_e + Qb_c)/Qb_0} \tag{34.44}$$

The computation of the diffusion charges Qb_e and Qb_c is based directly on the solution of the differential equation for the majority carriers in the neutral base region and relates the charges to the injected minority carrier concentrations at the emitter and collector edges. The substrate current of the PNP transistor takes into account high injection. The parameters are substrate saturation current and knee in the substrate current. When the substrate current value is low, the reverse current gain increases at medium reverse current levels.

HiCUM

HiCUM is a scalable physics-based compact bipolar transistor model [83]. Its name derives from **hi**gh-**cu**rrent **m**odel. Generally, bipolar processes span a variety of device struc-

tures and types. The compact BJT models are split into two categories: (1) vertical devices with high-speed NPN transistors and (2) lateral devices with PNP transistors. HICUM is targeted toward the first category. However, it may be necessary to divide the first category into "low-power" ($BV_{CEO} < 10\,V$) and "high-power" ($BV_{CEO} > 10\,V$) transistors if the difference in device design and the electrical application range turns out to be too large for a single model. From an industrial point of view, these requirements can be drawn for a compact model: high accuracy over a wide electrical (and temperature) range; laterally scalable parameter calculation, including variable-contact configurations, in order to allow circuit optimization; numerical stability and fast execution time, although this is somewhat dependent on the application; physics-based derivation, allowing for predictive and statistical modeling; reliable and well-defined extraction procedures, which should be available together with test structures; also, the use of standard equipment and setups only which is important for, e.g., fast throughput; and modular formulation of the model equations, minimizing interrelations between different electrical regions and facilitating simple implementation into circuit simulators. The important physical and electrical effects taken into account by HICUM can be briefly listed: high-current effects (including quasi-saturation); distributed high-frequency model for the external base-collector region; emitter periphery injection and associated charge storage; emitter current crowding (through a bias-dependent internal base resistance); two- and three-dimensional collector current spreading; parasitic (bias-independent) capacitances between base-emitter and base-collector terminal; vertical non-quasi-static (NQS) effects for transfer current and minority charge; temperature dependence and self-heating; weak avalanche breakdown at the base-collector junction; tunneling in the base-emitter junction; parasitic substrate transistor; bandgap differences (occurring in HBTs); and lateral scalability. In contrast to MOS transistor models, the geometry-dependent calculations have been implemented in a separate program (TRADICA [84]) for various reasons. The experimental results indicate that HICUM has been proven to be highly accurate and it has been already applicable for a variety of different technologies, from a relatively low-speed and high-voltage process to commercial SiGe technologies.

IGBT

Isolated gate bipolar transistor (IGBTs) have become widely accepted among circuit designers as an alternative to power BJTs or Darlington transistors in a broad range of power converter and motor drive applications [4]. To design power electronic circuits containing IGBTs, circuit simulations are needed to examine the behavior of the power element within the circuit. A simple SPICE IGBT model was proposed [43] and [42], and it is one of the very first physics-based models

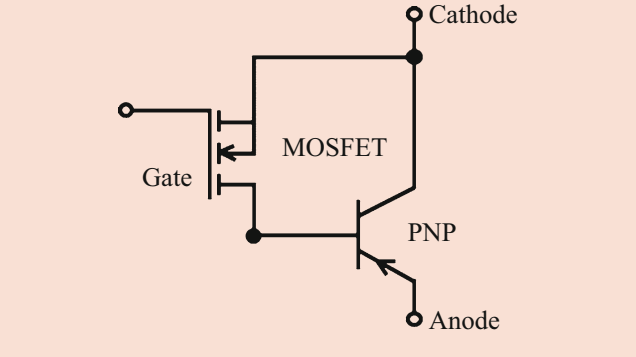

Fig. 34.14 IGBT SPICE subcircuit symbol

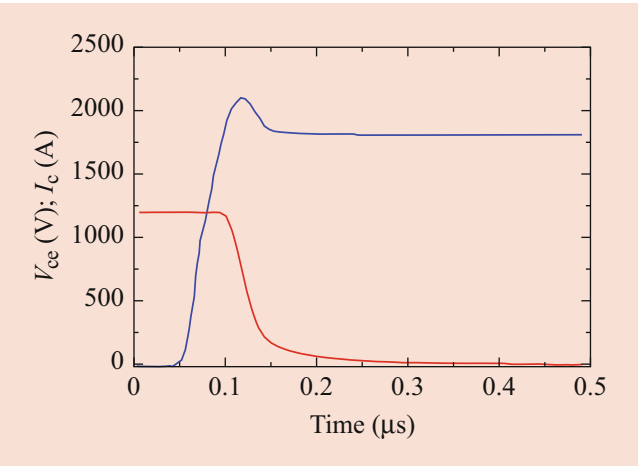

Fig. 34.15 Transient IGBT SPICE simulations

for the low-gain, high-level injection bipolar transistor of the IGBT power device type. To describe the high-level injection operation of the wide base bipolar transistor of the IGBT type (Fig. 34.14) and of other conductivity-modulated power devices, the ambipolar transport theory of the IGBT model describes the transport of electrons and holes in the base and the transient behavior, not available in earlier, conventional quasi-static modeling approaches. Figure 34.15 shows results of transient IGBT SPICE simulations.

34.3.5 MOSFETs

The essential difference among compact models is the choice of the main variables in terms of which the physical processes in the transistor are described. Known-to-date compact models use three different approaches. First developed and most widely used (from the 1960s to the present times) are the models based on the concept of threshold voltage (Vth-based approach) [50,103]. These include LEVEL1-LEVEL3, MM9, BSIM2, BSIM3, and most others [3,35,36,51]. How-

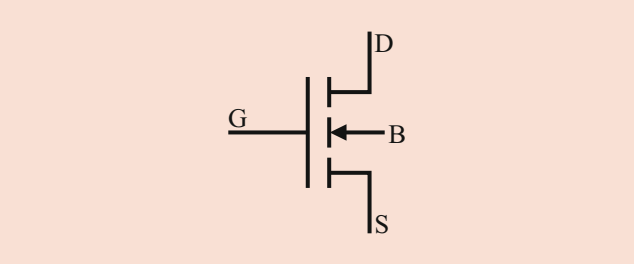

Fig. 34.16 M SPICE symbol

ever, this approach causes too many intractable problems when modeling transistors manufactured by technology with design standards less than 100 nm, with low supply voltage, and intended for analog- and radio-frequency circuits.

Six MOSFET models are implemented in standard SPICE: MOS1 is described by a square-law I–V characteristic [87], MOS2 is an analytical model, while MOS3 [100] is a semiempirical model; MOS6 [80] is a simple analytic model accurate in the short-channel region; MOS4 [77, 86] and MOS5 [46] are the BSIM (Berkeley short-channel IGFET model [85]) and BSIM2. MOS2, MOS3, and MOS4 include second-order effects such as channel length modulation, subthreshold conduction, scattering-limited velocity saturation, small-size effects, and charge-controlled capacitances. Standard SPICE provides six MOSFET device models, (Fig. 34.16) which differ in the formulation of the I–V characteristic. The variable LEVEL specifies the model to be used:

LEVEL=1 - Shichman-Hodges (as described in [87])
LEVEL=2 - MOS2 (as described in [101])
LEVEL=3 - MOS3, a semiempirical model (as described in [101]; Fig. 34.17 shows its IV plot)
LEVEL=4 - BSIM (as described in [86])
LEVEL=5 - BSIM2 (as described in [46])
LEVEL=6 - MOS6 (as described in [80])

$$v_{\mathrm{T}} = v_{\mathrm{TO}} + K_2\left[(-v_{\mathrm{SD}} + \psi)^{1/2} - \psi^{1/2}\right] \qquad V_{\mathrm{SD}} > V_{\mathrm{SS}} \tag{34.45}$$

Berkeley Short-Channel IGFET Model

BSIM1 is the first model that has properties typical of second-generation models [85]. Instead of accurately describing the subtle submicron effects using complex equations, this model uses empirical fit parameters determined with optimization procedures. A large number of parameters simplify the model equations and allow one to more accurately fit equations to experimental data. However, this is achieved at the cost of weakening the connection between the parameters of the technological process and those of the model, i.e., at the

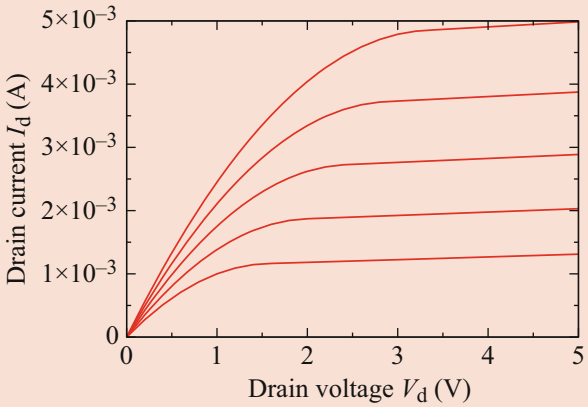

Fig. 34.17 MOSFET Level3 $I_d(V_d)$ plot

cost of deteriorating the predictive ability of the model. BSIM1 takes advantage of earlier Level3 model definition and a number of improvements. This includes the expression for the dependence of the mobility on the vertical electric field that introduces the substrate bias. The equation for the threshold voltage includes an additional term that takes into account inhomogeneous doping of the substrate. The model introduced a more accurate expression for the subthreshold current, which is smoothly connected with the above-threshold characteristic, ensuring continuity of the first derivative. To simulate the saturation of the carrier velocity and its dependence on the longitudinal component of the electric field, completely new dependencies are introduced, essentially simplifying the equation for the drain current, including the equation for saturation current. With a decrease in the effective channel length to 0.8 μm and of the oxide thickness to 15 nm, the BSIM1 model becomes inapplicable [32, 46].

HSPICE Level28

The decrease in geometric dimensions of the transistors has made the shortcomings of the BSIM1 model to appear more and more noticeably. To overcome them, HSPICE Level28 model was proposed [31]. The Level28 has a very wide distribution, thanks to the fact that it was built into the HSPICE program, which was used by the vast majority of CMOS VLSI developers. The HSPICE Level28 model is based on BSIM1 but removes many of its flaws, including that related to discontinuity of the second derivative of the drain current with respect to the gate voltage. For this, the current equations in the subthreshold region were smoothly connected with the equation for the strong inversion mode. Moving from the linear to the saturation region in earlier models was performed as follows: first, the saturation voltage was determined, and then the drain current in the active

region at saturation was made equal to the saturation current at the same point; this did not guarantee the continuity of the derivatives at the connection point. In the HSPICE Level28 model, this problem is solved by applying smoothing functions that have two fitting parameters. The model is a proprietary product and is supplied as an integral part of the HSPICE program, which is a significant drawback.

BSIM3

The previous version (model BSIM2) had gaps, negative conductance, and spurious outliers in the transfer conductance versus gate voltage dependence. To eliminate these problems, the BSIM3v3 model uses smoothing functions, ensuring the continuity and smoothness of the expressions for the drain current and terminal charges. BSIM3 takes into account a more detailed description of the inhomogeneous doping of the channel region in both vertical and horizontal directions and takes into account many new effects associated with small sizes. The model is valid only for transistors with a channel length larger than 0.15 μm [21]. BSIM3v3 was the first compact MOSFET model to successfully pass the standardization procedure at the Compact Model Coalition (CMC) [64].

BSIM4

BSIM4 is a further development of the BSIM3 model for application to MOS transistors made using the 100 μm technology or less. These models, unlike PSP and HiSIM, use the threshold voltage, not the surface potential, as a state change indicator. BSIM4, unlike BSIM3, includes the following: an accurate new model of input impedance for internal nodes; improved model of the substrate for modeling radio-frequency circuits; a new accurate channel thermal noise model and the model noise extension for induced shutter noise; a model that takes into account non-quasi-static effects for both transfer conductance and capacitance; an accurate model of current tunneling through the gate; a flexible, geometry-dependent model of parasitic elements; an improved model for transistors with steep retrograde distribution of impurities in the substrate; an improved model of threshold voltage for devices with implantation into pockets, taking into account the asymmetry of the resistances of the source and drain and their dependence from voltage and accounting (at the user's choice) for electrical, physical, or equivalent thickness of the gate dielectric; a quantum mechanical model of the inversion layer thickness and effective oxide thickness; a refined mobility model; improved models of the effects of GIDL/GISL leaks; an improved model of thermal and flicker noise; the ability to set various volt-ampere and volt-farad characteristics for the source and drain junctions; models of pn junctions with and without current limitation, taking into account the effects of strained silicon; a unified model of the drain-current saturation effect, which takes into account the mechanisms of saturation of the drift velocity of carriers and of the abnormal increase in mobility; the possibility of choosing other materials besides polysilicon, silicon, and SiO_2; a new definition of the threshold voltage to improve the fitting of subthreshold characteristics; and empirical consideration of the well proximity effect (WPE).

The disadvantages of the BSIM4 model include a quite large number of parameters, the appearance of negative resistances and capacitances in some modes, the discontinuity of the derivatives of the drain current and terminal charges in the Gummel symmetry test [54] at $V_{ds} = 0$, the lack of symmetry of some IV and CV characteristics.

BSIM6

BSIM6 is a new generation of the charge-based BSIM Bulk MOSFET model [17]. Its charge-based core is derived from Poisson's solution and has the following features: physical effects (SCE, CLM, etc.) taken from BSIM4; parameter names matched to BSIM4 parameters for compatibility; Gummel symmetry is fulfilled (the model is symmetric for DC/AC modes at $V_{DS} = 0$); Capacitances and corresponding derivatives are also symmetric at $V_{DS} = 0$. The BSIM6 implementation is continuous in all regions of operation with no glitches, this resulting in smooth IV current and CV capacitance behavior; it features physically sound capacitance modeling with short-channel velocity saturation for CV modeling and related effects; physical implementation of BSIM6 model is using global extraction procedure. BSIM6 solves the charge equation using first- and second-order Newton-Raphson technique to obtain analytical expression of q_i without any approximation to calculate the charge equation. Defining the BSIM6 drain current:

$$I_D = I_{drift} + I_{diff} = \mu W \left(-Q_i \frac{d\Psi_S}{dx} + V_T \frac{dQ_i}{dx} \right) \quad (34.46)$$

its mobility model second with the order effects has been adopted from BSIM4:

$$I_D = \frac{\mu_v}{\sqrt{1 + \left(\frac{\mu_v}{v_{sat}} \left| \frac{d\Psi_S}{dx} \right| \right)^2}} W \left(-Q_i \frac{d\Psi_S}{dx} + V_T \frac{dQ_i}{dx} \right) \quad (34.47)$$

and using charge linearization and parameter normalization [27]:

$$\begin{aligned} &2q_i + \ln(q_i) \\ &\quad + \ln\left[\frac{2n_q}{\gamma} \left(\frac{2n_q}{\gamma} q_i \right) + 2\sqrt{-2q_i + \psi_p} \right] \\ &\quad = \psi_p - 2\phi_f - v_{ch} \end{aligned} \quad (34.48)$$

yields the BSIM6 total current expression [81]

$$i_{\mathrm{d}} = \frac{\left(q_{\mathrm{s}}^2 + q_{\mathrm{s}}\right) - \left(q_{\mathrm{d}}^2 + q_{\mathrm{d}}\right)}{\frac{1}{2}\left(1 + \sqrt{1 + \left[\lambda_{\mathrm{c}}\left(q_{\mathrm{s}} - q_{\mathrm{d}}\right)\right]^2}\right)} \tag{34.49}$$

Global BSIM6 parameter extraction [75] produces a single set of parameters for the entire range of MOSFET device lengths, and allows for an accurate evaluation of the next nanoscaled technology nodes [65].

Philips MOS Model 9

MOS Model 9 (version 902) [98] is a compact MOS transistor model intended for the simulation of circuit behavior with emphasis on analog applications. The model gives a complete description of all quantities related to the transistor actions: nodal currents and charges, noise power spectral densities, and weak avalanche currents. The equations describing these quantities are based on the gradual channel approximation with a number of first-order corrections for small-size effects. The consistency is maintained by using the same carrier density and electric field expressions in the calculation of all model quantities. Model 9 provides a model for the intrinsic transistor only; junction charges and leakage currents are not included.

Philips MOS Model 11

MOS Model 11 (MM11), the successor to MOS Model 9, has been developed by Philips [96]. MM11 gives an accurate description not only of charges and currents and their first-order derivatives (transconductance, conductance, capacitances) but also of their higher-order derivatives. In other words, it gives an accurate description of the MOSFET distortion behavior, and as such, MM11 is suitable for digital, analog, as well as RF circuit design. MOS Model 11 is a symmetrical, surface-potential-based model. It includes an accurate description of all physical effects important for modern and future CMOS technologies, such as gate tunneling current, gate-induced drain leakage, influence of pocket implants, poly-depletion, quantum-mechanical effects, and bias-dependent overlap capacitances. Including all of the above, MOS Model 11 achieves superior accuracy as compared to MOS Model 9 without an increase in the number of parameters and with only a slight increase in simulation time.

PSP MOSFET Model

PSP MOSFET model [33] was developed by merging the best features of the two surface-potential-based compact models: SP (developed at the Pennsylvania State University) [18], [33], and MM11 (developed by Philips) [96]. The major features of PSP include the following: physical surface-potential-based formulation in both intrinsic and extrinsic model modules; physical and accurate description of the accumulation region; inclusion of all relevant small geometry effects; modeling of the halo implant effects, including the output conductance degradation in long devices; Coulomb scattering and non-universality in the mobility model; non-singular velocity-field relation enabling the modeling of RF distortions including intermodulation effects (IM3); complete Gummel symmetry; midpoint bias linearization enabling accurate modeling of the ratio-based circuits (e.g., R2R circuits, such as as defined in [34]); quantum mechanical corrections; correction for the polysilicon depletion effects; GIDL/GISL model; surface-potential-based noise model including channel thermal noise, flicker noise, and channel-induced gate noise; advanced junction model including trap-assisted tunneling, band-to-band tunneling, and avalanche breakdown; spline collocation-based NQS model including all terminal currents; and stress model.

The normalized drain charge along the channel length x given in the Ward-Dutton partition [102] by the integral:

$$Q_{\mathrm{D}} = \frac{1}{L}\int_0^L \frac{x}{L} q_{\mathrm{i}} \mathrm{d}x \tag{34.50}$$

becomes in the PSP model:

$$Q_{\mathrm{D}} = \frac{q_{\mathrm{im}}}{2} + \frac{\alpha\Delta\psi}{12}\left(1 - \frac{\Delta\psi}{2H_{\mathrm{PSP}}} - \frac{\Delta\psi^2}{20H_{\mathrm{PSP}}^2}\right) \tag{34.51}$$

The expressions for the current and terminal charges obtained in this manner are continuous and smooth in all regions of operation from accumulation to deep inversion. Another unique feature of PSP is the adequate intermodulation (IM3) modeling of a simple passive mixer. Modeling and simulation of this type of IC are a rather difficult problem. The issue is that (unlike the case for active mixers) passive mixer modeling is sensitive to any singularity at zero drain bias. The non-singular nature of PSP allows proper IC mixer simulations and yields a correct slope (3 dB/dB) for the third harmonic [8].

Since 2016, the PSP model is supported by the CEA-Leti modeling group [63].

EKV2.6

The EKV model version 2.0 appeared in 1994 [27] and has continuously being developed up to the present time. Details of the model and simulation examples can be obtained from the website [66]. The model is built by analyzing physical processes in deep submicron MOS transistors and is designed to simulate analog and analog-digital circuits, operating at low currents and voltages (1.2–1.5 V and below). The model is based on the charge of the inversion layer and

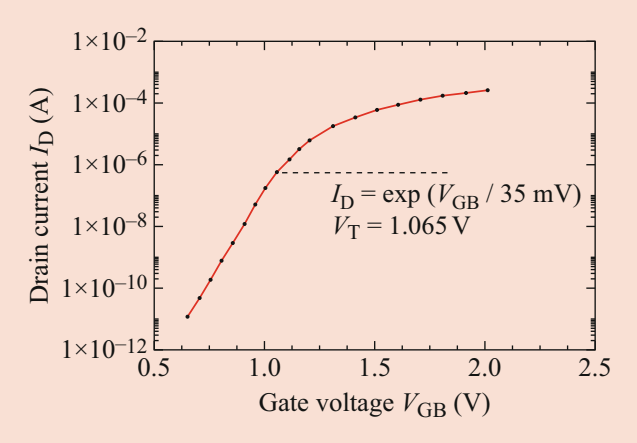

Fig. 34.18 EKV $I_d(V_g)$ plot

is the only widespread model built on this principle. Initial publications on weak inversion (or subthreshold) MOSFET operation date back to the early 1970s [5, 29, 73, 92, 95]. EKV compact model developments are focused on MOSFET operation in the weak inversion. The model uses the bulk substrate terminal as the reference to preserve source-drain symmetry. In the EKV definition has similarities with the Ebers-Moll bipolar transistor model. An internal feature of EKV model is the slope factor n:

$$I_D = \frac{W}{L} I_{DO} e^{\frac{V_G}{nU_T}} \left[e^{\frac{-V_S}{U_T}} - e^{\frac{-V_D}{U_T}} \right] \tag{34.52}$$

$$\frac{W}{L} I_{DO} = I_S e^{\frac{-V_{TO}}{nU_T}} \tag{34.53}$$

Unlike previous generations, the EKV model has the following properties that are important in modeling ultralow-power analog ICs: it provides an accurate modeling of the g_m, g_{ds} conductances at all internal nodes; it takes into account the non-quasi-static effects; it features an accurate model of white and flicker noises; it has a small number of parameters (the model kernel uses only ten parameters) and a simplified procedure for parameter extraction (Fig. 34.18 shows its transfer plot).

EKV3

The EKV3 model [13] is based on the ideas of EKV2.6. Additionally, it takes into account a number of effects necessary for modeling deep submicron MOS transistors, mainly in the area of weak and moderate inversion [15]. The model is designed for the ultralow-power analog device modeling and IC simulations. Work [14] compares the simulation results with experimental 100-nm CMOS data for frequencies up to 20 GHz, with a channel length from 110 nm to 2 μm; it shows that the Y-parameters of the model are in good agreement with the experimental data over the entire frequency range and at all bias voltages and also shows that non-quasi-static effects. Non-quasi-static effects have been investigated for long-channel transistors at frequencies up to 20 GHz. Importantly, in the short-channel transistors it takes into account extrinsic parasitic elements. Based on the results, it can be concluded that the model can be used for analog circuits as well as for RF CMOS circuits.

HiSIM MOSFET Model

All transistor characteristics are described by the HiSIM (Hiroshima-University STARC IGFET Model) model as a function of surface potential, which is calculated iteratively at each applied voltage under the charge-sheet approximation [58]. The concept of surface potential allows one to obtain the general expression for the sum of the diffusion and drift currents, which eliminates the need for smoothing functions. The basic HiSIM equations for the inversion layer charge Q_i and the depletion layer charge Q_b are written at position y along the channel with the effective gate voltage V'_G:

$$\begin{aligned} Q_i(y) &= -C_{ox}\left(V'_G - \phi_S(y)\right) - Q_b(y) \\ Q_b(y) &= -qN_{sub}L_D\sqrt{2\beta\left(\phi_S(y) - V_{bs}\right) - 1} \end{aligned} \tag{34.54}$$

HiSIM takes into account all significant short-channel effects, known by now. Particularly accurate and without applying binning, this model takes into account the gate-induced drain leakage (GIDl) effect.

Other MOSFET Compact Models

The academic and industrial R&D groups continue developments of other MOSFET compact models:

ACM—Universidade Federal de Santa Catarina, Brazil
aMOS—Texas Instruments, USA
ASIM/CSIM—AT&T Bell Labs, USA
MISNAN—Carleton University, Canada
PCIM—Digital Equipment Corp., USA
SSIM—Motorola, USA
USIM—Agere Systems, USA
Xsim/DOUST—Nanyang Technological University, Singapore
Ultras—Peking University, China

34.3.6 SOI MOSFET Models

The MOS transistors fabricated on the silicon-on-insulator (SOI) substrate are different from conventional MOSFETs. The device layer, in which the conducting channel is located, is on a buried oxide (BOX) insulating it from the silicon substrate. A number of categories of SOI MOSFETs can be distinguished. They can be realized as devices with Schottky barrier junctions, pn junctions, or as devices with l-h junc-

tions, which in the extreme are junctionless transistors. In the extremely downscaled SOI MOSFETs, the architecture of source/drain regions and of their contacts is of great importance. The transistors with pn junctions work in the inversion mode, whereas the transistors with l-h junctions work typically in the accumulation mode. According to the device layer thickness and doping concentration, two types of the SOI MOSFETs can be distinguished: partially depleted (PD) SOI MOSFETs and fully depleted (FD) SOI MOSFETs. The PD SOI MOSFETs appeared at the beginning of the SOI technology de and are still in use. However, the state-of-the art SOI MOSFETs have channels with very low doping to minimize the random doping fluctuation (RDF) effect, to minimize the carrier mobility degradation, and to enhance the gate control over the channel conductance. Due to this, their mode of operation changes between full depletion in the OFF state to the full inversion or accumulation in the ON state. According to a shape of SOI MOSFETs, different geometries may be distinguished, e.g., planar and fin-type ones. There are also devices with pi- and omega-type channels. However, they were developed in the past rather for research purpose. Finally, according to a number of gates, among practical solutions of the SOI MOSFETs, there are single-gate, double-gate, and gate-all-around (GAA) devices. Standard PD, FD SOI MOSFETs are single-gate devices. FinFETs and ultrathin body and buried oxide FD SOI (UTBB FD SOI) MOSFETs are double-gate devices (in the FinFETs, both the gates are shortened). In the state-of-the-art nanosheet and nanoribbon transistors, the channels are wrapped with the gates. Other solutions, though theoretically possible, do not have a practical meaning. A large variety of the SOI MOSFET architectures, modes of operation, and gate control need compact modeling for the process/device/circuit development. In this section, only a few implemented and most often used ones will be briefly presented and discussed.

PD SOI MOSFET

The physical model of the n-channel PD SOI MOSFETs is presented in [93, 94] with available Verilog-A description [37]. It takes into account the basic phenomena in such devices including diffusion/drift transport in the front and bottom (if exists) channels, avalanche ionization in the drain-body junction depletion area, thermal recombination in the source-body space charge area and nearby, thermal generation in the drain-body space charge area and nearby. Taking these effects into account allows to determine the floating-body potential and next all the internal and terminal DC current components. Obviously, the "kink" effect both in the subthreshold and strong inversion ranges is clearly visible on the output characteristics. Having the DC model characteristics, it is possible to determine the non-quasi-static (NQS) small-signal (AC) characteristics of the SOI MOSFET. The NQS AC model was developed based on the Hauser approach [41]. This approach is physically more sound than the quasi-static (QS) approach, in which the capacitances are calculated as the derivatives of the charges assigned to the terminals with respect to the terminal potentials. Moreover, it does not use a channel charge sharing between the source and drain terminals [102], which in fact results only from mathematical transformation.

Figure 34.19 shows general current flow in the PD SOI MOSFETs, which can be described in two modes assuming small-signal analysis:

$$i_{\mathrm{S}}(t) + i_{\mathrm{Gf}}(t) + i_{\mathrm{D}}(t) + i_{\mathrm{Gb}}(t) = 0 \tag{34.55}$$

$$u(t) = U + u^{*}\mathrm{e}^{j\omega t} \tag{34.56}$$

in DC mode:

$$I_{\mathrm{S}} + I_{\mathrm{Gf}} + I_{\mathrm{D}} + I_{\mathrm{Gb}} = I_{\mathrm{S}} + I_{\mathrm{D}} = 0 \quad \Rightarrow V_{\mathrm{BS}} \tag{34.57}$$

in AC mode:

$$i_{\mathrm{s}}^{*} + i_{\mathrm{gf}}^{*} + i_{\mathrm{d}}^{*} + i_{\mathrm{gb}}^{*} = 0 \quad \Rightarrow v_{\mathrm{bs}}^{*} \tag{34.58}$$

This yields the expressions for the drain current in both sides, source and drain, respectively:

$$\begin{aligned}
i_{\mathrm{cf}}^{*}(0) &= \left\{\lambda_{\mathrm{f0}}\left[v_{\mathrm{s}}^{*} - \left(v_{\mathrm{gf}}^{*} - v_{\mathrm{tf}}^{*}\right)\right]\right. \\
&\quad \left. + \mu_{\mathrm{f0}}\left[v_{\mathrm{d}}^{*} - \left(v_{\mathrm{gf}}^{*} - v_{\mathrm{tf}}^{*}\right)\right]\right\}/\Theta_{\mathrm{f}} \\
i_{\mathrm{cf}}^{*}(L) &= \left\{\lambda_{\mathrm{fL}}\left[v_{\mathrm{s}}^{*} - \left(v_{\mathrm{gf}}^{*} - v_{\mathrm{thf}}^{*}\right)\right]\right. \\
&\quad \left. + \mu_{\mathrm{fL}}\left[v_{\mathrm{d}}^{*} - \left(v_{\mathrm{gf}}^{*} - v_{\mathrm{thf}}^{*}\right)\right]\right\}/\Theta_{\mathrm{f}} \\
Y_{xy} &= \delta_{xy} i_{x}^{*}/v_{y}^{*}; \\
C_{xy} &= \mathrm{Im}\left(Y_{xy}\right)/\omega; \\
&\text{where}: \quad x, y \in \{s, gf, d, gb\}
\end{aligned} \tag{34.59}$$

BSIM SOI

BSIM-SOI is a compact model for SOI devices. BSIM-SOI model variants are BSIM-IMG, a model for independent multi-gate (usually front and back gate) MOSFETs, and BSIM-CMG, a model for common multi-gate MOSFETs [65]. The whole BSIN-SOI family represents different approaches to the SOI MOSFET modeling: threshold voltage-, charge-, and surface-potential-based. The basic BSIM-SOI v.4.6.1 model is a threshold voltage-based model constructed similarly to the BSIM4 model of the conventional MOSFETs. It enables simulation of operation of a variety of planar devices. The model parameter SoiMod serves as a selector for the PD device model (SoiMod=0), for the unified PD&FD model (SoiMod=1), for the ideal FD device model (SoiMod=2), and for the model selection by BSIMSOI itself.

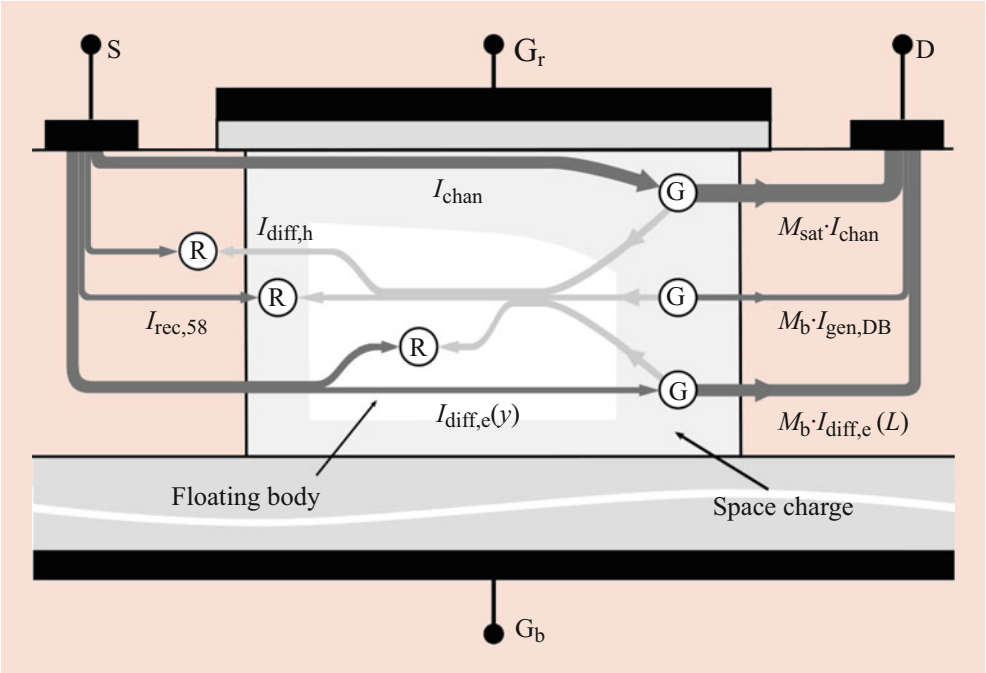

Fig. 34.19 Approximation of the distribution of current components in the non-fully depleted SOI MOSFET

The BSIM-CMG model accounts for different transistor architectures, which are declared by a parameter GEOMOD, namely, double-gate (GEOMOD=0), e.g., FinFET, triple-gate (GEOMOD=1), quadruple-gate (GEOMOD=2), cylindrical (GEOMOD=3), and unified (GEOMOD=4). In all these cases, the gate effective width is modified according to the declared architecture. The model accounts also for two types of FinFET substrate selected by a parameter BULKMOD. FinFETs on SOI substrate or on Si substrate are selected by setting BULKMOD=0, 1 accordingly. As opposed to BSIM-SOI, the BSIM-CMG model is constructed based on the charge-based approach, i.e., the primary variables of the model are the channel charge densities at the source and drain ends of the channel q_{is} and q_{id} derived from the electrostatics.

The surface-potential-based BSIM-IMG model serves for simulation of the double-gate (DG) SOI MOSFETs with both gates independently biased. The gate stacks at the gates may be different, i.e., different work functions, fixed charge densities, and gate insulator thicknesses can be specified. To determine the surface potentials for both gates, the Poisson's equation is solved iteratively taking into account a coupling between both gates.

HiSIM SOI

Developed at the Hiroshima University [67], HiSIM SOI is fully depleted. SOI-MOSFET is developed based on the surface-potential description, considering the potential distribution vertical to the channel and parallel to the surface explicitly. Besides the comparison to measured I–V data, the model is verified with 1/*f* noise analysis, sensitive to the carrier concentration and distribution along the channel. And furthermore, for the accurate modeling of the short-channel effects, the parasitic electric field induced through the buried oxide is considered.

The SOI MOSFET device has thee Si-SiO_2 interfaces as schematically shown in Fig. 34.20, and corresponding charges are induced at all these surfaces. The following three basic equations are derived from the Poisson equation and the Gauss law, by considering boundary conditions assuming an approximation of a linearly decreasing current distribution into the bulk of SOI MOSFET device:

$$V_{gs} - V_{fb} = \phi_{s,SOI} - \frac{Q_i + Q_{dep} + Q_{b,SOI} + Q_{s,bulk} + Q_G}{C_{OX}} \tag{34.60}$$

$$\phi_{s,SOI} = \phi_{b,SOI} - \frac{Q_{s,bulk} + \frac{1}{2}Q_{dep}}{C_{SOI}} \tag{34.61}$$

$$\phi_{b,SOI} = \phi_{s,bulk} - \frac{Q_{s,bulk}}{C_{BOX}} \tag{34.62}$$

Corresponding capacitances C_{OX}, C_{SOI}, and C_{BOX} are functions of the SOI device layer thicknesses; V_{gs} and V_{fb} are the gate-source bias voltage and the flat-band voltage, respectively. ll charges appearing in the above equations are

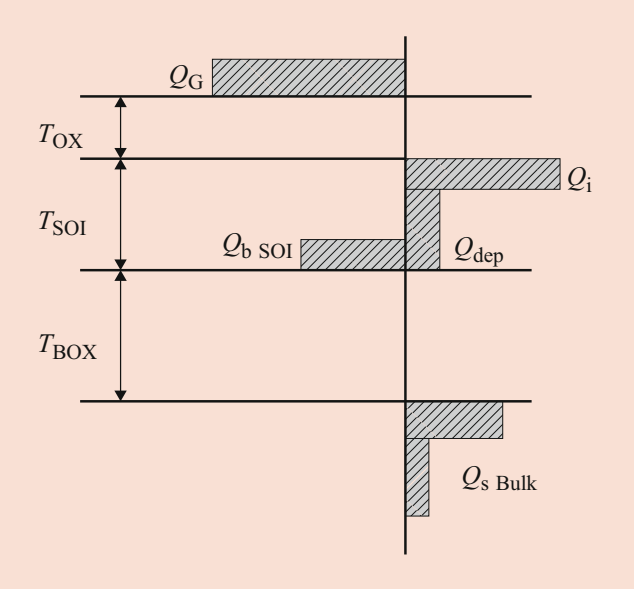

Fig. 34.20 Charges in HiSIM SOI model

functions of the three surface potentials in the SOI devices. To guarantee accurate and flexible circuit simulation for a device with the various SOI layer and BOX layer thicknesses at any operating conditions, the above three equations are solved iteratively in the HiSIM SOI model. Modeled physical phenomena in the HiSIM SOI can be summarized as follows: physical dependence on device parameters, short-channel effects, narrow-channel effects, impact ionization effect, poly-depletion effect, quantum mechanical effect, pocket implantation effects, low- and high-field mobility model, leakage current models, noise models for all conduction mechanisms, floating-body effect, history effect, body-tie effect, self-heating effect, both DC and AC Gummel symmetries, and diode model for S/D junctions.

Leti L-UTSOI

L-UTSOI is a surface-potential-based compact model dedicated to FD-SOI technologies with thin lightly doped device layers, in particular for UTBB devices accounting for back interface inversion. It was developed by CEA-Leti [72], and it has been selected in 2020 by the CMC as a standard compact model for FD SOI devices. An FD SOI transistor is a four-pin transistor with a back gate that allows tuning the device in a low-leakage and low-power operating regime or higher-performance operating regime. The L-UTSOI symmetry between front and back interface has been respected in all equations of the core model. Its core is also valid for all independent double-gate MOSFETs. The L-UTSOI accounts for numerous physical effects, namely, interface coupling, back interface inversion/dual-channel operation; ground-plane depletion; quantum confinement; velocity saturation; short-channel effects; channel length modulation; series resistance with gate voltage-dependence; parasitic currents (gate current, GIDL/GISL); parasitic capacitances (overlap, fringe); self-heating effect; stress model; noise models (flicker, thermal, induced gate, shot); and source/drain junction asymmetry. The model accuracy was verified against DC/AC characteristics for the 28-nm FD SOI process, measured for nFETs with 7-nm device layer thickness, 25-nm BOX thickness, and n-type backplane. This unique capability offered by FD-SOI technology allows the fabrication of smaller, faster, and denser chips than standard complementary metal oxide semiconductor (CMOS) technology.

UFSOI/UFPDB/UFDG

The UFSOI models (UFPDB and FD/SOI) are developed by the University of Florida and implemented into `SPICE` [30], [22]. The original bases of the models are described under "SOISPICE/ UFSOI." The UFPDB model (evolved from the NFD model) is unified for application to PD/SOI and bulk-Si MOSFETs with just one small set of model parameters. Recently, the models have been upgraded to include gate-body direct tunneling current and an option for a strained Si/SiGe channel. The FD/SOI model has been evolved into a separate model (UFDG) for generic double-gate MOSFETs, which is also applicable to UTB FD/SOI devices

34.3.7 JFETs

The JFET device (Fig. 34.21) is formed by diffusing a pn junction as a gate diode between the source and drain. Similarly, in MESFETs, the gate is created as a metal layer over the gate-control region, which provides a Schottky-contact diode. To control the current flow, both technologies modulate the depletion region of the gate diode.

Modeling basic JFET and MESFET effects include:

- Charge-conserving gate capacitors
- Back-gating the substrate node
- Mobility degradation due to gate field
- Computationally efficient DC model [23, 90]
- Subthreshold equation
- Physically correct width and length

The ideal current equation accounts for all DC currents of the JFET device, and its two pn junctions are modeled by these ideal diode equations:

$$I_{gd} = I_{Seff}\left(e^{\frac{V_{gd}}{Nv_t}} - 1\right) \quad \text{for } V_{gd} > -10Nv_t \tag{34.63}$$

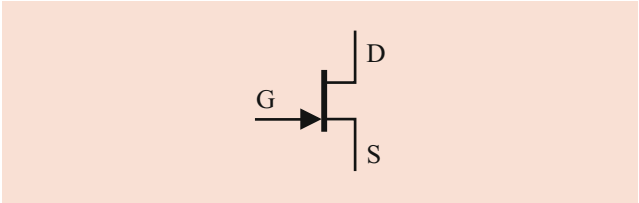

Fig. 34.21 JFET SPICE symbol

$$I_{gd} = -I_{Seff} \text{ for } V_{gd} \leq -10Nv_t \tag{34.64}$$

$$I_{gs} = I_{Seff}\left(e^{\frac{V_{gd}}{Nv_t}} - 1\right) \quad \text{for } V_{gs} > -10Nv_t \tag{34.65}$$

$$I_{gs} = -I_{Seff} \text{ for } V_{gs} \leq -10Nv_t \tag{34.66}$$

The SPICE .MODEL statement selects a JFET or MESFET model to simulate a netlist

```
.MODEL mname NJF <Level = val>
<pname1 = val1> ...
```

The variable LEVEL specifies the model to be used for SPICE simulations:

- Level=1 JFET model
- Level=2 JFET model
- Level=3 MESFET model
- Level=4 TOM3 MESFET model
- Level=5 Materka model

Basic JFET or MESFET IV characteristics are defined by the model parameters VTO and BETA, which also determine the variation of drain current with gate voltage. LAMBDA determines the output conductance, IS the saturation current of the two gate junctions. Two ohmic resistances, RD and RS, are included. The charge storage is modeled by nonlinear, depletion layer capacitances for both gate junctions, which vary as the $-M$th power of the junction voltage and are defined by the parameters CGS, CGD, and PB. Noise model parameters KF and AF are also a function of the JFET source and drain series resistances (RS and RD), as well as a function of temperature. Parameters ALPHA and A model noise in MESFETs. SPICE JFETs models are mostly used regional approaches [16, 25, 82]. The most complete treatment until now [105] includes empirical subthreshold definition in above-threshold JFET operation.

Recently, a unified charge-based model for double-gate and cylindrical architectures of junction field-effect transistors (JFETs) has been developed [45]. JFETs were mainly used in analog low-noise ICs; with the recent advances in SiC technology, there are an increasing number of JFET applications in power electronics. Advanced JFET models can be implemented as junctionless FETs with an infinite gate capacitance, as proposed in [45]. The model was derived without the need to develop a new physical set of analytical relations. Assuming that the whole JFET channel operates in depletion, the gate-channel pn junction should be reversely biased ($V_{GS} < 0$) in order to avoid the gate leakage current. The JFET channel charge density and its potentials in depletion mode are expressed as follows:

$$V_{GS} - V_{ch} - \Delta\phi_{ms} - U_T \ln\left(\frac{N_D}{n_i}\right) \overset{dep}{\approx} -\frac{Q_{sc}^2}{8qN_D\varepsilon_{si}} - \frac{Q_{sc}}{2C_{ox}} + U_T \ln\left[1 - \left(\frac{Q_{sc}}{Q_{fix}}\right)^2\right] \tag{34.67}$$

As anticipated above, a JFET can be described as a JLFET with an infinite gate capacitance:

$$V_{GS} - V_{ch} - V_{bi} \overset{dep}{\approx} \frac{-Q_{sc}^2}{8qN_D\varepsilon_{si}} + U_T \ln\left[1 - \left(\frac{Q_{sc}}{Q_{fix}}\right)^2\right] \tag{34.68}$$

JFET threshold voltage is the gate voltage where Q_m tends to zero (at $V_{DS} = 0$) with the JFET pinchoff voltage V_P defines as:

$$V_{TH} = V_{bi} + V_P \tag{34.69}$$

The JFET drain current in depletion mode can be obtained using:

$$I_{DS} = \frac{W\mu}{L_G} f(Q_m)\Big|_S^D = \frac{W\mu}{L_G}[f(Q_{m,d}) - f(Q_{m,s})] \tag{34.70}$$

where $f(Q_m)$ is a function of the mobile charge densities fulfilling $Q_{sc} = Q_{fix} + Q_m$.

A symmetric double-gate junction FET (three-terminal DG JFET) proposed in [52] models drain current and total charges of corresponding nodes, as well as their derivatives, accordingly. The total node charges at source and drain are calculated by integrating the charge density along the channel, applying the well-known Ward-Dutton partitioning. The gate charge is obtained from charge balance as:

$$Q_G = -(Q_D + Q_S) = -W_{ch}\int_0^{L_{ch}} Q_m dx \tag{34.71}$$

and this allows to analytically estimate the transcapacitances as the partial derivatives of the node charges versus terminal voltages:

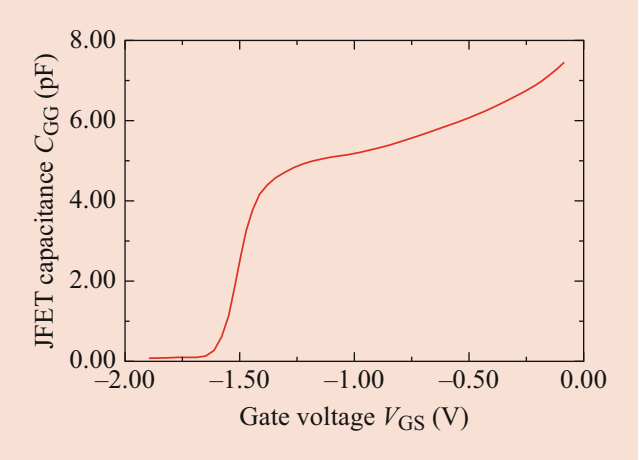

Fig. 34.22 JFET gate capacitance plot

$$C_{ij} = \pm \frac{\partial Q_i}{\partial V_j} \tag{34.72}$$

where i and j correspond to G, D, or S nodes of the JEFT device. The analytical definition of all JFET transcapacitances simplifies the model validation and Verilog-A implementation. Figure 34.22 shows the CV plot of a JFET gate capacitance.

34.4 HV/Power Compact Models

In this section, selected HV/power compact models are presented.

34.4.1 LDMOS

High-voltage MOSFETs are those that can support a higher V_{DS} voltages and currents I_D than regular MOSFETs. Because of this versatility, they are used to switching loads ON/OFF, to up- or down-convert between different voltage levels or, more generally, for power management and RF backend to provide high-power amplification (Fig. 34.23).

34.4.2 MM20 LDMOS Model

MOS Model 20 (MM20) is a compact MOSFET model intended for analog circuit simulation in high-voltage MOS technologies. It describes the electrical characteristics of double-diffused MOS devices including a lateral MOS device under a thin gate oxide layer [1]. MOS Model 20 gives a self-consistent description of all quantities related to transistor action: nodal currents, nodal charges, and noise power spectral densities. The equations describing these quantities are

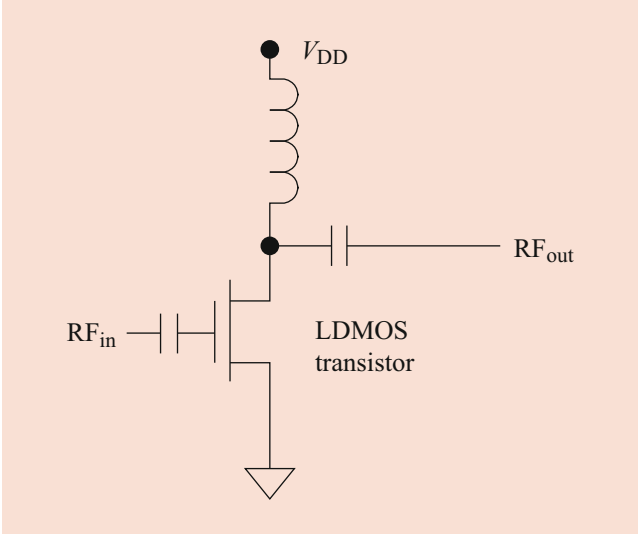

Fig. 34.23 Basic LD MOSFET RF subcircuits

based on surface-potential formulations, resulting in equations valid over all operation regimes (i.e., accumulation, depletion, and inversion in both the channel region and drift region). The surface potential as a function of the terminal voltages is obtained by the explicit expression derived earlier [97]. The currents through MM20 device consist of the DC current I_{DS} from drain to source and the charging currents at the drain, gate, source, and bulk terminal. Therefore, the total current into corresponding terminal is given by:

$$\begin{aligned} I_D &= I_{DS} + I_{DB} + (\mathrm{d}Q_D/\mathrm{d}t) \\ I_G &= \mathrm{d}Q_G/\mathrm{d}t \\ I_S &= -I_{DS} + (\mathrm{d}Q_S/dt) \\ I_B &= -I_{DB} + (\mathrm{d}Q_B/dt) \end{aligned} \tag{34.73}$$

34.4.3 HiSIM-HV: A Compact Model

The HiSIM-HV [53] is high-voltage MOSFET model based on the HiSIM (Hiroshima-University STARC IGFET Model) model for conventional bulk MOSFETs [58] and features a consistent potential description across MOSFET channel and drift region. Symmetric and asymmetric device types are covered for up to several 100 V switching capability. HiSIM-HV has accurately implemented scaling channel and drift region lengths as well as channel width properties. The model is based on the charges controlled by voltages.

34.5 Organic TFT

Selected organic TFT compact models are presented in this section.

34.5.1 RPI a-Si TFT Model

RPI a-Si TFT model (Fig. 34.24) is an amorphous silicon (a-Si), thin film transistor (TFT) model [88]. The field-dependent mobility of RPI a-Si TFT is determined by the gate voltage overdrive, the same as in other TFT models [20]. However, it is superior to earlier models, since it considers effects resulting from localized energy states in the thin-film bandgap, especially for downscaled TFT devices. This allows for more accurate prediction of threshold voltages, field-dependent mobility, leakage currents, kink effects, and drain currents above threshold.

34.5.2 AIM-SPICE MOS15

MOS15 amorphous silicon (a-Si) thin film transistor (TFT) model is implemented in AIM-SPICE [44]. The models have been compared with experimental data to validate its implementation with device gate lengths down to 2 μm (for poly-Si) and 4 μm (for a-Si) in a temperature range of 25–150 °C at the frequencies up to 10 MHz. Its main features include modified charge control model and induced charge trapped in localized states. Above threshold includes field-effect mobility becoming a function of gate bias and band mobility dominated by lattice scattering. Below threshold includes Fermi level located in deep localized states and related position of Fermi level, including the deep DOS back to the gate bias, as well as empirical expression for current at large negative gate biases for hole-induced leakage current; interpolation techniques are applied to the equations to unify the model.

Features of the MOS15 a-Si TFT model include:

- Modified charge control model and induced charge trapped in localized states
- Above-threshold operation includes:
  - Field-effect mobility becoming a function of gate bias
  - Band mobility dominated by lattice scattering
- Below-threshold operation includes:
  - Fermi level located in deep localized states
  - Relate position of Fermi level, including the deep DOS back to the gate bias
  - Empirical expression for the current at large negative gate biases for hole-induced leakage current
- Interpolation techniques applied to the equations to unify the model.
- AIM-Spice includes an automatic.

34.6 Progressive Modeling Directions

Future compact models, which set new development challenges, are discussed in this section.

34.6.1 Single-Electron Transistors (SET)

A constant interaction (CI) SET model (Fig. 34.25) describes the energetics most straightforwardly [49] and inexpertly assumes that the Coulomb interaction between the electrons is independent of the doping concentration [48].

34.6.2 Quantum Dot

Quantum dot devices with semiconductor optical amplifier have already shown excellent characteristics (Fig. 34.26). Studies have demonstrated the usefulness of QDs for optical amplification, all-optical switching, and signal processing [91]. The different parts of the equivalent circuits interact together to represent the gain recovery process, saturation properties, and chirp behavior in both linear and nonlinear operation regimes of QD-SOA. The equivalent circuits are then used for `SPICE` simulation. It has been shown that `SPICE` simulation results agree well with the full, numerically calculated results [79].

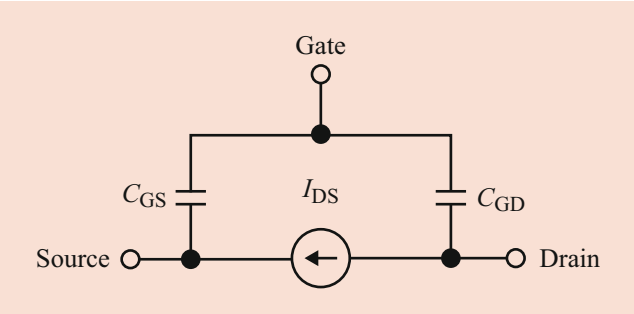

Fig. 34.24 Organic RPI a-Si TFT model

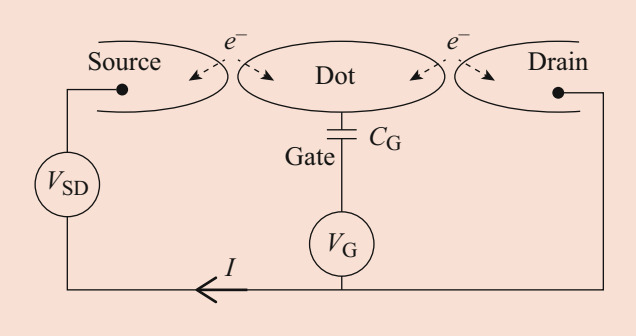

Fig. 34.25 Coulomb interaction in single-electron transistors

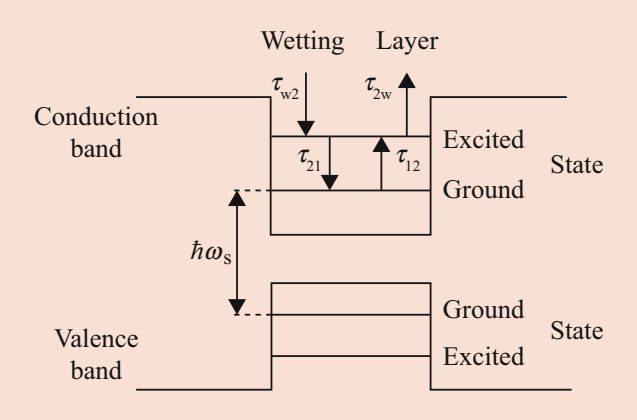

Fig. 34.26 Quantum dot

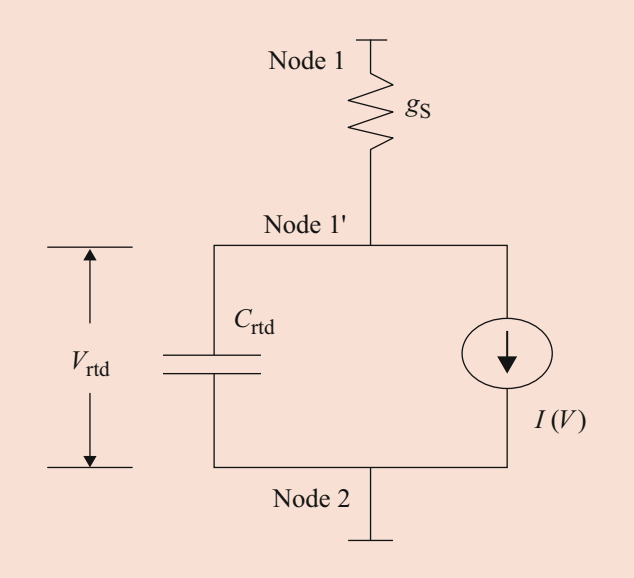

Fig. 34.27 Resonant tunneling diode model

34.6.3 Resonant Tunneling Diode

Figure 34.27 shows a general equivalent circuit model for resonant tunneling diode (RTD). The component g series is used to represent contact resistance and some other losses which appear during the manufacturing process. The voltage-controlled current source I(V) represents the DC IV characteristic of the RTD. The capacitance CRTD represents the CV characteristic of the RTD [59].

34.6.4 Rapid Single-Flux Quantum (RSFQ) Device

Recent developments concerning the rapid single-flux-quantum (RSFQ) circuit family are reviewed (Fig. 34.28).

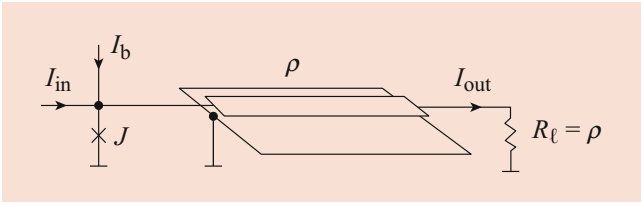

Fig. 34.28 Rapid single-flux quantum (RSFQ) device

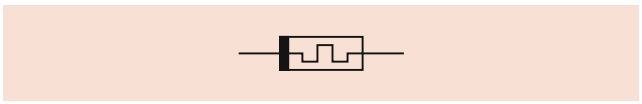

Fig. 34.29 Memristor SPICE symbol

Elementary cells in this circuit family can generate, pass, memorize, and reproduce picosecond voltage pulses with a nominally quantized area corresponding to the transfer of a single magnetic flux quantum across a Josephson junction [19].

34.6.5 Memristor

In the paper published by Dr. Williams [104] manufacturability of a memristor, the so-called fourth elementary passive element, has been reported. Theoretical symmetry between the nonlinear resistor (voltage vs. current), nonlinear capacitor (voltage vs. charge), and nonlinear inductor (magnetic flux linkage vs. current) has been reviewed by Chua in his 1971 paper [25]. Several models for memristors have been developed with their Verilog-A implementations, e.g., the linear ion drift model, the nonlinear ion drift model, the Simmons tunnel barrier model, and the threshold adaptive memristor (TEAM) model (Fig. 34.29).

34.6.6 Negative Capacitance Model

A recent paper has proposed a negative capacitance model [2]. The negative capacitance (NC) effect, observed in various semiconductor devices, physical mechanisms, and their effects are discussed in detail with the theoretical interpretation of experimental data [28]. Quantum transport properties of negative capacitance transistors (NC-FETs) with monolayer black phosphorus (ML-BP) are theoretically studied (Fig. 34.30).

34.6.7 Magnetic Tunnel Junction

The magnetic tunnel junction (MTJ) is defined in [74] and [7,40]. A new spin-transfer torque (STT) model allows circuit designers to simulate key aspects of spin-transfer torque

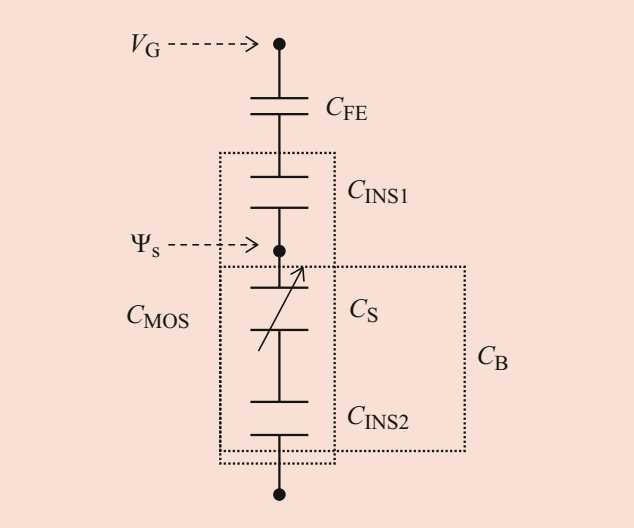

Fig. 34.30 Negative capacitance model

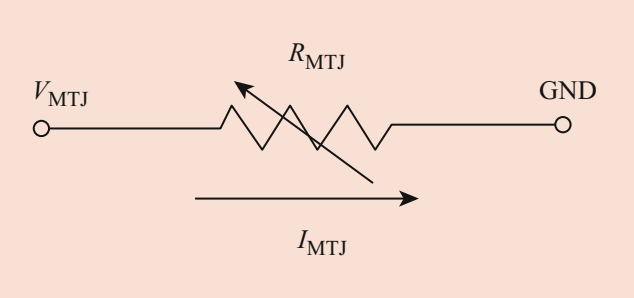

Fig. 34.31 Magnetic tunnel junction

MRAM (STT-MRAM), such as read and write delays. It is a self-contained, physics-based magnetic-tunnel junction (MTJ) `SPICE` model that can reproduce realistic MTJ characteristics based on user-defined input parameters, such as the free layer's length, width, and thickness parameters [47]. Using the MTJ `SPICE` model, scalability studies of both in-plane and perpendicular MTJs can be performed across different technology nodes with minimal effort (Fig. 34.31).

34.7 Conclusions

Developing compact models for the microelectronics /nanoelectronics industry is crucial for reducing product development costs and gaining access to new technologies. In this chapter, we have addressed critical issues for developing compact models for microelectronic and nano-electronic devices. We have analyzed the main fundamentals of compact device modeling, the typical assumptions made, and the main principles that circuit simulation and design tools use in conducting analyses based on device models. Moreover, we have discussed the possibilities of integrating compact models into circuit simulation and design tools, with particular emphasis on Verilog-A standardization, which makes the implementation of the compact models into EDA tools easy. The key parameter extraction strategies are beyond the scope of this chapter. We have also discussed the main challenges of developing compact models for emerging devices, many of them utilizing new materials, that are enabling new applications such as quantum computing, cryogenics, flexible and wearable electronics, and bioelectronics.

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Process Simulation

35

Jürgen Lorenz and Peter Pichler

Contents

35.1 Scope and History of Process Simulation 1260

35.2 Simulation of Ion Implantation 1261
35.2.1 Analytical Models 1261
35.2.2 Monte Carlo Simulation 1268

35.3 Simulation of Diffusion and Activation 1271
35.3.1 Intrinsic Point Defects and Impurities 1271
35.3.2 Basic Diffusion and Reaction Mechanisms 1273
35.3.3 Macroscopic Diffusion Behavior of Dopants 1275
35.3.4 Dopant Diffusion at High Concentrations 1278
35.3.5 The Influence of Surface Processes on Dopant Diffusion 1279
35.3.6 Transient Diffusion Effects During Post-Implantation Annealing 1280
35.3.7 Electrical Activation, Clusters, and Solid Solubility . . . 1281
35.3.8 Segregation 1282
35.3.9 Simulation Methodologies 1283

35.4 Simulation of Oxidation 1283
35.4.1 One-Dimensional Simulation of Oxidation 1283
35.4.2 Multidimensional Simulation of Oxidation 1285
35.4.3 Multidimensional Simulation of Stress-Dependent Oxidation 1285

35.5 Lithography Simulation 1286
35.5.1 Basic Principle of Lithography 1286
35.5.2 Principle of Lithography Simulation 1287
35.5.3 Simulation of Imaging 1287
35.5.4 Simulation of Resist Development 1290
35.5.5 State-of-the-Art Lithography Simulation 1290
35.5.6 Examples for State-of-the-Art Lithography Simulation 1290

35.6 Simulation of Deposition and Etching 1291
35.6.1 Outline of Equipment Simulation 1291
35.6.2 Discretization and Movement of Surfaces 1293
35.6.3 Models for Deposition and Etching Rates 1294

35.7 Process Variations 1296
35.7.1 Sources of Systematic Process Variations 1296
35.7.2 Hierarchical Simulation of the Impact of Process Variations 1297

35.8 Conclusions 1297

References 1298

Abstract

In this chapter an outline of the very diverse topic of process simulation is given. This includes the process steps of ion implantation and thermal annealing, which introduce, activate, and modify dopant distributions, and the process steps lithography, deposition, and etching, which are used to structure the semiconductor wafer. The section on oxidation deals with the simulation of the oxide growth, whereas the aspect of dopant segregation is included in the section on diffusion. Finally, the impact of process variations is outlined. Overall, the process simulation chapter primarily deals with the physics and the related models for the various process steps, whereas the discussion of generic algorithms, e.g., for the solution of partial differential equations, is left for another dedicated chapter of this book. However, some algorithms which are specific for process simulation are also briefly described in this chapter.

Due to the diversity of the area of process simulation, this chapter could not strive for completeness in the presentation of the physical models. We largely refer to silicon technology, whereas most models can also be applied for or adapted to other top-down semiconductor technologies where, in contrast to bottom-up technologies based on self-assembling, patterning steps, ion implantation and high-temperature process steps are used to generate three-dimensional geometries and dopant distributions.

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Equipment simulation · Process simulation · Geometry · Dopant distribution · Defect distribution · Point defects · Stress · Process variations

35.1 Scope and History of Process Simulation

This chapter deals with the physical and chemical processes employed to fabricate semiconductor devices based on semiconducting material such as silicon, namely, to generate their geometries and the spatial distributions of dopants, mechanical stress, and potentially further quantities which determine and influence the electrical behavior and the reliability of the devices. The processes to be studied may be grouped into those which primarily influence the geometry, namely, lithography, etching, and deposition, and those which primarily introduce and modify dopant distributions and their activation, namely, ion implantation and thermal annealing. Oxidation primarily changes the local geometry but also affects dopant distributions. Epitaxy is used both to deposit semiconducting layers with desired properties and to introduce dopants, and silicidation is a combination of metal deposition and annealing to form metal-silicon alloys to act as contacts.

Process simulation is an integral part of technology computer-aided design (TCAD). The overall industrial benefit of TCAD in terms of the reduction of development times and costs was already in the 2011 International Technology Roadmap for Semiconductors (ITRS) [1] estimated at about 40%. Although no serious assessment is available on how much process simulation contributes to this benefit, its impact is in any case very significant. Especially, there were also statements from industry that the impact of TCAD cannot be given in percent, because several technological developments would even not be possible at all without the use of TCAD.

Historically and long ago, these processes could be described with macroscopic process parameters, such as the temperature to which wafers were exposed in a furnace reactor, used for annealing or oxidation. During the last decades and in parallel with device scaling, it got increasingly important and difficult to reliably and accurately control such parameters in both space and time. In turn, it has got more and more important to characterize, simulate, and control how such parameters depend on the process equipment used. One of the first effects considered already decades ago was the temperature profiles which occur when a wafer is introduced into a furnace reactor for annealing or oxidation: Whereas the wafer is initially at room temperature, it is gradually heated while being pushed into the furnace reactor. The temperature to which a dopant is then exposed depends on the temperature distribution in the furnace, the movement of the wafer into its target position, and the thermal conduction within the wafer. This is one of the first examples for the need to simulate not only geometries and dopants at transistor scale but also the development of spatial and temporal distributions in the process equipment. This so-called equipment simulation is therefore also considered in this chapter. Especially it is also highly relevant for the advanced fabrication steps used for current nanoscale transistors, such as millisecond annealing, and lithography steps employed to generate patterns far smaller than the wavelength of the light used (e.g., 40 nm structures with 193 nm wavelength double patterning immersion lithography, according to the 2013 International Technology Roadmap for Semiconductors (ITRS) [2]).

With both physical processes and device architectures being driven to their limits, systematic and stochastic variations of the processes used can no more be neglected. The most famous and obvious effect is random dopant fluctuations (RDF) [3]: For example, for threshold voltage implants of 10^{12} cm^{-2}, at mean 4 ions are implanted into a 20-nm-long and 20-nm-wide transistor channel. Because ion implantation is a statistical process, this means that the real number of ions implanted into the channel fluctuates around the mean value of 4. In turn, also the threshold voltage is distributed around its nominal value. Such variations are critical for the overall yield in semiconductor fabrication. A short overview of this aspect is given at the end of this chapter.

The scope of process (including equipment) simulation outlined above is very wide and diverse. In turn, the detailed discussion of the large set of processes and models needed to simulate them would require a dedicated and rather thick book: One of the first reviews of the at that time emerging area of process simulation was published in 1984 as one chapter of a book on the simulation of semiconductor devices in general [4]. Twenty years later, the book on just one (very important) area within process simulation, the modeling of dopant diffusion and activation, published by one of the authors [5] extended to more than 500 pages. Since then, the diversity and complexity of process and equipment models has further grown, due to shrinking features and new processes, materials, and physical effects having come into play. Therefore, this chapter cannot give a comprehensive review of all details. Rather, it intends to give the reader an overview how the input data needed for device simulation, in terms of geometries, active dopants, and strain, can be generated by simulation and which merits and limitations the approaches employed have. In view of this and of the limited space available, we do not include epitaxy, silicidation, and chemical-mechanical polishing CMP. Whereas the chapter

generally refers to silicon as the semiconductor material used, most models can also be applied or adapted to other semiconducting materials. Generally, we refer to specific literature for further details.

Another important aspect to consider is that the level and effort of simulation has historically changed and will continue to do so: Whereas for the simulation of a transistor with one micron channel length, the use of (kinetic) Monte Carlo methods was neither necessary nor possible, a completely different situation applies for sub-decananometer transistors, where shrinking feature sizes both necessitate and partly enable more sophisticated simulation methods. Compared with device simulation, ab initio approaches are hardly used for process simulation, but nevertheless can support the development of computationally more efficient models. During the last decades, simulation has developed from one-dimensional process simulation with academic tools around 1980 [6–8] through two-dimensional process simulation in the 80th and 90th [9, 10] to the current situation where three-dimensional process simulation with commercial tools [11, 12] is the industrial standard. Moreover, in the early days of technology computer-aided design, the individual process steps were mostly treated in isolation, in order to optimize the process step in question, e.g., the annealing steps employed to create high dopant activation while maintaining a shallow junction. In the course of device scaling and more physical models being developed, the interactions between the individual process steps became ever more important. A common example is that dopant diffusion and activation critically depend on the distribution of point defects, which is influenced not only by the annealing step itself but also by other preceding process steps, such as ion implantation or thermal oxidation. In turn, integrated simulation of whole process flows, or the most important part of them, became mandatory. Concerning the transfer of process results into device simulation, in some cases simplistic assumption on device geometry and dopant distributions were made to simplify device studies, e.g., using Gaussian dopant profiles or abrupt junctions. However, such assumptions are sometimes physically not sound and are especially for current nanoscale devices misleading and likely invalidate the results of subsequent device simulations. In turn, the result of the simulation of the whole process flow must be transferred into the device simulator to be used, in most cases necessitating major remeshing. Currently even the gap between the device community and the lithography community is closing, because transistors no more depend on the footprint of the resist structures patterned in lithography steps, but also on the impact of in general non-vertical edges of the resist lines on subsequent etching and deposition processes. This adds to the impact non-vertical nitride, poly, or oxide masks on implanted profiles, which has been included in state-of-the-art process simulation since long.

35.2 Simulation of Ion Implantation

For decades, analytical models have been the workhorse for the simulation of ion implantation. Therefore this chapter starts with this approach and describes it in some detail.

35.2.1 Analytical Models

Some fundamentals of the analytical description of ion implantation can still be taken from the very early book mentioned above [4]. In general, analytical models use distribution functions $f(x)$ which are normalized to unity and vanish for very large (positive and negative) x:

$$f(-\infty) = f(\infty) = 0; \int_{-\infty}^{\infty} f(x)\,\mathrm{d}x = 1 \tag{35.1}$$

The dopant distribution $C(x)$ is then obtained by multiplying the distribution function $f(x)$ with the implanted dose N_D. The part of the vertical distribution for x smaller than zero does not stand for a dopant profile. Rather, it is assumed that the integral across the negative axis corresponds to the amount of particles which are backscattered from the wafer surface during implantation [13].

The analytical models use range moments of the distribution $f(x,y)$, both in vertical (x) and in lateral direction (y), and also partly mixed moments in both directions. Here, x refers to the direction parallel to the incident ion beam and y to the direction perpendicular to this. The first moment in vertical direction is the mean value of the depth in which the ion is stopped, the so-called projected range:

$$R_\mathrm{p} = \int_{-\infty}^{\infty} x \cdot f(x)\,\mathrm{d}x \tag{35.2}$$

whereas the further moments in vertical direction, the range straggling ΔR_p, the skewness γ, and the kurtosis β are centered around R_p:

$$\Delta R_\mathrm{p} = \sqrt{\int_{-\infty}^{\infty} \left(x - R_\mathrm{p}\right)^2 f(x)\,\mathrm{d}x} \tag{35.3}$$

$$\gamma = \frac{1}{\Delta R_\mathrm{p}^3} \int_{-\infty}^{\infty} \left(x - R_\mathrm{p}\right)^3 f(x)\,\mathrm{d}x \tag{35.4}$$

$$\beta = \frac{1}{\Delta R_\mathrm{p}^4} \int_{-\infty}^{\infty} \left(x - R_\mathrm{p}\right)^4 f(x)\,\mathrm{d}x \tag{35.5}$$

In case of two-dimensional distributions in x and y, $f(x)$ must be replaced by $f(x,y)$, and the integration runs across x and y.

Due to symmetry, the odd moments in lateral direction are equal to zero. Important lateral moments are the lateral range straggling $\Delta R_{\mathrm{p,l}}$ and the lateral kurtosis β_{l}:

$$\Delta R_{\mathrm{p,l}} = \iint_{-\infty}^{\infty} y^2 f\,(x, y)\ \mathrm{d}x\,\mathrm{d}y \tag{35.6}$$

$$_{\mathrm{l}} = \frac{1}{\Delta R_{\mathrm{p,l}}^4} \iint_{-\infty}^{\infty} y^4\, f\,(x, y)\ \mathrm{d}x\,\mathrm{d}y \tag{35.7}$$

Because the lateral shape of the implanted doping profile generally depends on the depth x, it is also useful to introduce mixed moments $X^i\,Y^j$ [14]:

$$X^i Y^j = \frac{1}{\Delta {R_{\mathrm{p}}}^i \cdot \Delta {R_{\mathrm{pl}}}^j} \iint_{-\infty}^{\infty} \left(x - R_{\mathrm{p}}\right)^i y^j\, f\,(x, y)\,\mathrm{d}x\,\mathrm{d}y \tag{35.8}$$

Whereas again odd moments in y vanish, moments X^iY^2 describe the change of the profile width with depths. Moments X^iY^4 describe the change of the lateral kurtosis with depth.

One-Dimensional Analytical Models

The analytical description of ion implantation is based on distribution functions from statistics, which in the context have no physical background except that ion implantation is a statistical process and that dopant profiles have certain shapes.

Simplest but sometimes still used is the Gaussian distribution, which approximates the vertical distribution as

$$C(x) = \frac{N_{\mathrm{D}}}{\sqrt{2\pi}\,\Delta R_{\mathrm{p}}}\ \exp\left(-\frac{\left(x - R_{\mathrm{p}}\right)^2}{2\Delta R_{\mathrm{p}}^2}\right) \tag{35.9}$$

It is apparent that due to the non-negligible implantation energy, the depth distribution of implanted ions is not symmetric, and not Gaussian. Generally, Pearson distributions have been shown [15] to best describe vertical profiles of implanted ions. These are defined as solutions of the differential equation:

$$\frac{\mathrm{d}f(x)}{\mathrm{d}x} = \frac{x - a}{b_0 + b_1 \cdot x + b_2 \cdot x^2} \tag{35.10}$$

Here, the parameters a, b_0, b_1, and b_2 depend on the vertical range moments; see Eqs. (35.2), (35.3), (35.4), and (35.5) [4]. Depending on the values of b_0, b_1, and b_2, the denominator of Eq. (35.10) may have singularities. In turn, different types of Pearson distributions result, depending on the values of skewness and kurtosis, from which b_0, b_1, and b_2 are calculated; see Fig. 35.1 [4].

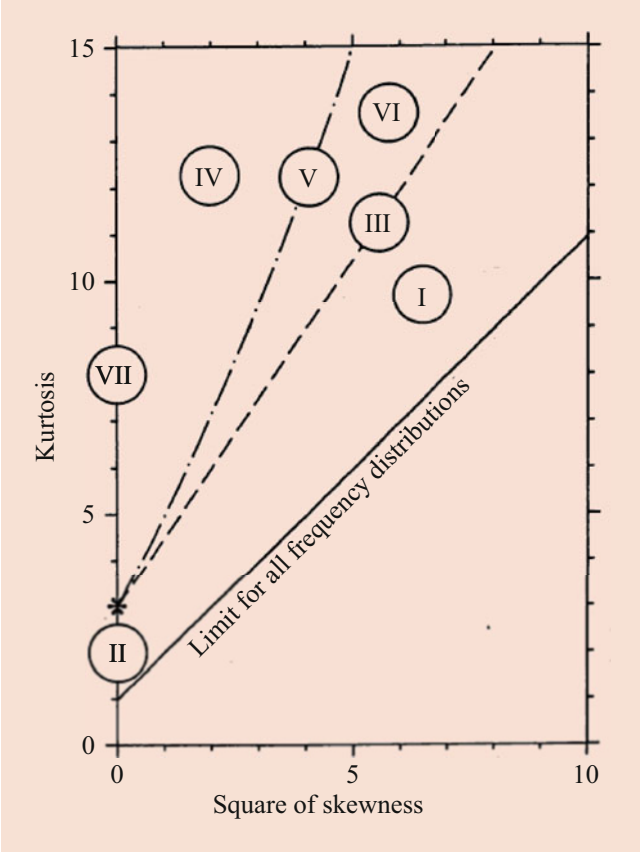

Fig. 35.1 Domains of validity of type (Roman number) of Pearson functions [4] depending on skewness and kurtosis

For vertical distributions, mostly Pearson IV distributions are suited best:

$$f(x) = K\left[-\left\{b_0 + b_1\left(x - R_{\mathrm{p}}\right) + b_2\left(x - R_{\mathrm{p}}\right)^2\right]^{1/2b_2}\right. \cdot \exp\left[-\left(\frac{b_1 / {b_2}^{+2\cdot a}}{\sqrt{4\cdot b_2\cdot b_0 - b_1^2}}\right) \cdot \arctan\frac{2b_2\left(x - R_{\mathrm{p}}\right) + b_1}{\sqrt{4\ b_2 b_0 - b_1^2}}\right] \tag{35.11}$$

For vanishing skewness, symmetric Pearson II, Pearson VII, and also Gaussian distributions (for a kurtosis of three) result. Depending on the parameter values, these are used for the lateral dopant distributions.

A very essential aspect in ion implantation is channeling: A larger amount of the ions penetrate deeper into the target if they are implanted along a low indexed crystalline direction.

Generally, implantation is performed with a tilt angle of about 7° to 10° [16], in order to minimize channeling. This situation is described by the Pearson distributions of type IV discussed above. For other (non-standard) tilt angles, range parameters may need to be adapted, depending on the amount of channeling occurring, or Monte Carlo methods should be used, as outlined in Sect. 35.2.2. For implantation into amorphous targets, where no channeling occurs, generally the asymmetric Pearson I and Pearson VI distributions are applicable, with Pearson III and Pearson V as limiting cases. In case of high-dose implantation into crystalline targets, amorphization occurs during the process. This situation can be described by the weighted addition of a Pearson distribution with parameters for a crystalline target and another Person distribution with parameters for an amorphous target [17].

Analytical One-Dimensional Multilayer Models

Ion implantation is not restricted to the ideal cases where the wafer can be divided into areas of bare silicon and areas which are masked by a layer which is not penetrated by the ions. Rather, ions are partly implanted through layers, and mask edges have a finite height and are in general not parallel to the implantation direction. In view of this, models are needed to describe the implantation into multilayer targets. In principle, such models would need to take the differences in the electronic stopping and in the nuclear scattering of the layers into account. Whereas the projected range of the implanted ions is strongly influenced by both electronic stopping and nuclear scattering, the range straggling is primarily influenced by the nuclear scattering as the dominating statistical process in ion implantation. In view of this, some models were published which approximate the change of the doping profile in silicon due to the influence of masking layers by taking the differences of the projected ranges and/or in the projected range straggling in the materials in question into account. The first and well-known model [18] assumed Gaussian profiles for both the mask (layer 1, with thickness t) and the silicon (layer 2) below, using for both layers the projected range and the projected range straggling in question. In addition, the profile in the silicon layer was shifted by

$$d = t \cdot \left(1 - \frac{\Delta R_{p2}}{\Delta R_{p1}}\right) \tag{35.12}$$

The weaknesses of this model were its limitation to Gaussian functions and that the ratio of the projected range stragglings did not sufficiently describe the changes in the stopping powers and, in turn, the profile shift. A generalization of this model [19] removed the restriction to Gaussian profiles:

$$C(x) = C_1(x), x \le t \tag{35.13}$$

$$C(x) = \frac{\Delta R_{p1}}{\Delta R_{p2}} \cdot C_1\left(\frac{\Delta R_{p1}}{\Delta R_{p2}}\, x - t\left(\frac{\Delta R_{p1}}{\Delta R_{p2}} - 1\right)\right), x > t \tag{35.14}$$

However, it still used the modified profile of the first layer also for the second layer and yields wrong results for the limiting case of $t \to 0$, where the profile in the second layer should be C_2 (x) and not ΔR_{p1} $/\Delta R_{p2} \cdot C_1$ $(\Delta R_{p1}$ $/\Delta R_{p2} \cdot x)$.

A model which well considers the original profile shape in the material in question and the changes in projected range due to masking layers is the Numerical Range Scaling model (NRS) [19, 20]. Here, for all layers in the stack, Pearson distributions are used with the range parameters for the material in question. Then, for all but the first layer, the layers on top are considered by shifting the profile based on the thicknesses of the layers on top and the ratios of the projected ranges.

For the implantation through a mask of thickness t (layer 1) into layer 2, this reads

$$C(x) = C_1(x) \text{ for } 0 \le x \le t \tag{35.15}$$

$$C(x) = \alpha \cdot C_2\left(x - t\left(1 - \frac{R_{p2}}{R_{p1}}\right)\right) \text{ for } x > t \tag{35.16}$$

Here, α is a scaling factor after which the model is named: Because no simplifications are made for the profile shapes $C_1(x)$ and $C_2(x)$ (unlike, e.g., in the Ishiwara-Furukawa model [18] where Gaussian distributions are assumed), α cannot be given in analytical form but results from numerical integration, to ensure that $C(x)$ is normalized to the total implanted dose.

A similar scaling of the ranges was also suggested in the LAYER model [21], however restricted to Gaussian profiles, for which dose conservation could be achieved by an analytical scaling factor. In the LAYER model, for the distribution in the second layer, a joint half Gaussian distribution was used, which assumes different range stragglings before and after its maximum, both depending on the projected range in the material of the first layer and projected range stragglings in the materials of the first and the second layer. By comparison with Monte Carlo simulations, it was shown that the range straggling in the second layer does not match especially for very thin or very thick masks [22].

As an extension of the NRS model, in the Improved Numerical Range Scaling model (NRS') [20], the projected range stragglings are corrected based on the layer thickness and the ratios of the projected range stragglings and the projected ranges:

$$\Delta R'_{p2} = \Delta R_{p2} + t \left(\frac{\Delta R_{p1}}{R_{p1}} - \frac{\Delta R_{p2}}{R_{p2}} \right) \tag{35.17}$$

Figure 35.2 shows the comparison between the Numerical Range Scaling model (NRS) and the Improved Numerical Range Scaling model (NRS') and measurements using secondary-ion mass spectroscopy (SIMS) for the implantation of boron with an energy of 100 keV and a dose of 10^{15} cm^{-2} through a silicon nitride layer into silicon. Whereas the NRS model already well describes the shift of the dopant profile in the silicon due to the different stopping power of the nitride layer, NRS' also yields a good description of the profile width in the silicon. However, it still fails to predict the change of the width in case of strange material combinations, such as the implantation of lithium into a stack of cadmium on gold. These are better described by a further refinement of the NRS' model, which was motivated by some aspects of the LAYER model and resulted in a further modified range straggling in the second layer [22]:

$$\Delta R'_{p2} = \Delta R_{p2} + t \left(\frac{\Delta R_{p1}}{R_{p1}} \cdot \frac{R_{p2} + \Delta R_{p2}}{R_{p1} + \Delta R_{p1}} - \frac{\Delta R_{p2}}{R_{p2}} \right) \tag{35.18}$$

The multilayer models outlined above in some way approximate the shift of the doping profile in the buried layers due to the different stopping power of the masking layer or layers and partly also the changes of the profile width. However, during ion implantation backscattering plays an important role. In result, the doping profile in a masking layer may also be influenced by a layer situated below. This holds especially in case of a light masking layer on top of a heavy substrate, and if the maximum of the doping profile is in the second layer, and compared with the projected range not too far from the interface. Based on considerations for the reflection of implanted ions at interfaces and in thin films, a simple model for the reflection at the interface between layers was developed, which is in the following outlined for a masking layer on top of a substrate. Here, the backscattered particles are described by half of a Gaussian distribution, located in the masking layer with its maximum at the interface. The reflected dose equals to a reflection coefficient times the amount of dopants passing the interface, and the projected range straggling of the reflected particles depends on an approximation of the maximum depth of the implantation profile in the masking material, the mask thickness, the implantation energy, and the mean particle energy at the interface. Good agreement with Monte Carlo simulations has been reported even for extreme combinations of implanted ions such as implantation of Li into a stack of silicon on gold [23].

Another effect which is at the edge of the possibilities of an analytical multilayer model is the treatment of channeling. As mentioned above, for implantation into a single semi-infinite layer, the double Pearson approach outlined above yields a good description. In principle, this can be extended by simply applying one of the multilayer models outlined

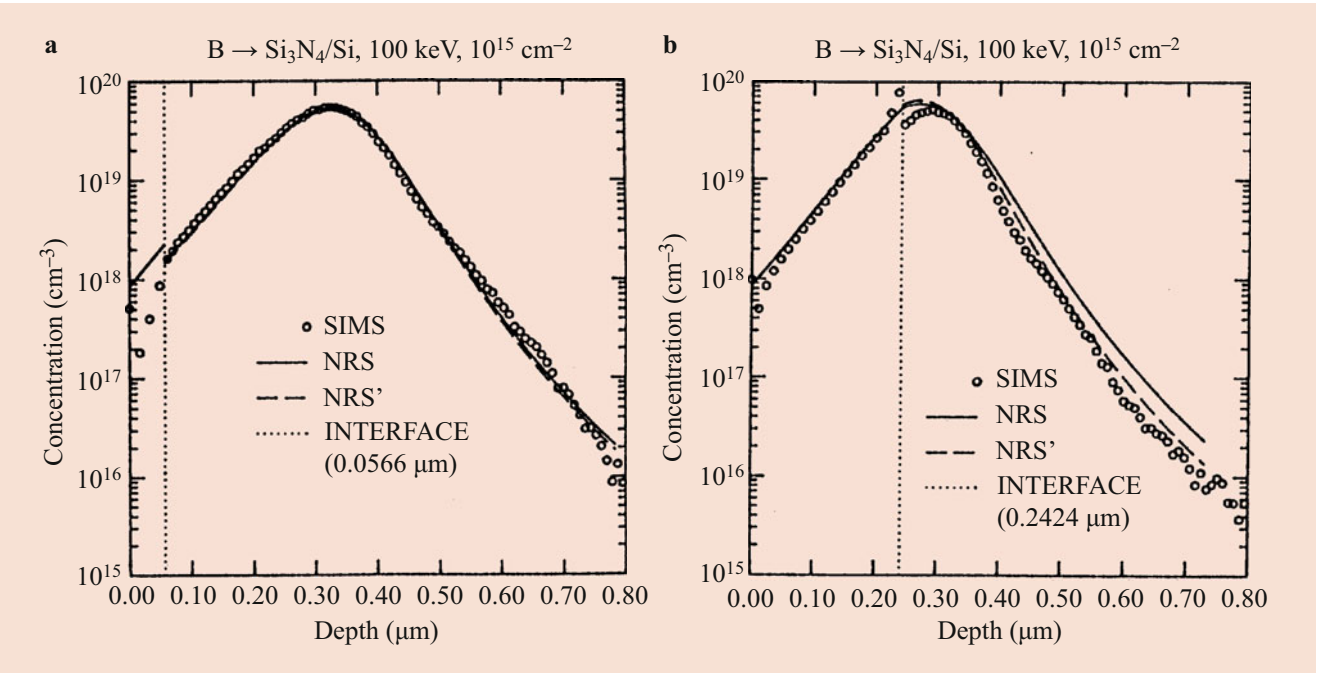

Fig. 35.2 Comparison of the analytical multilayer models NRS and NRS' with SIMS measurements for the implantation of boron at an energy of 100 keV and a dose of 10^{15} cm^{-2} through a Si_3N_4 layer of (**a**) 0.0566 μm; (**b**) 0.2424 μm thickness into silicon [20]

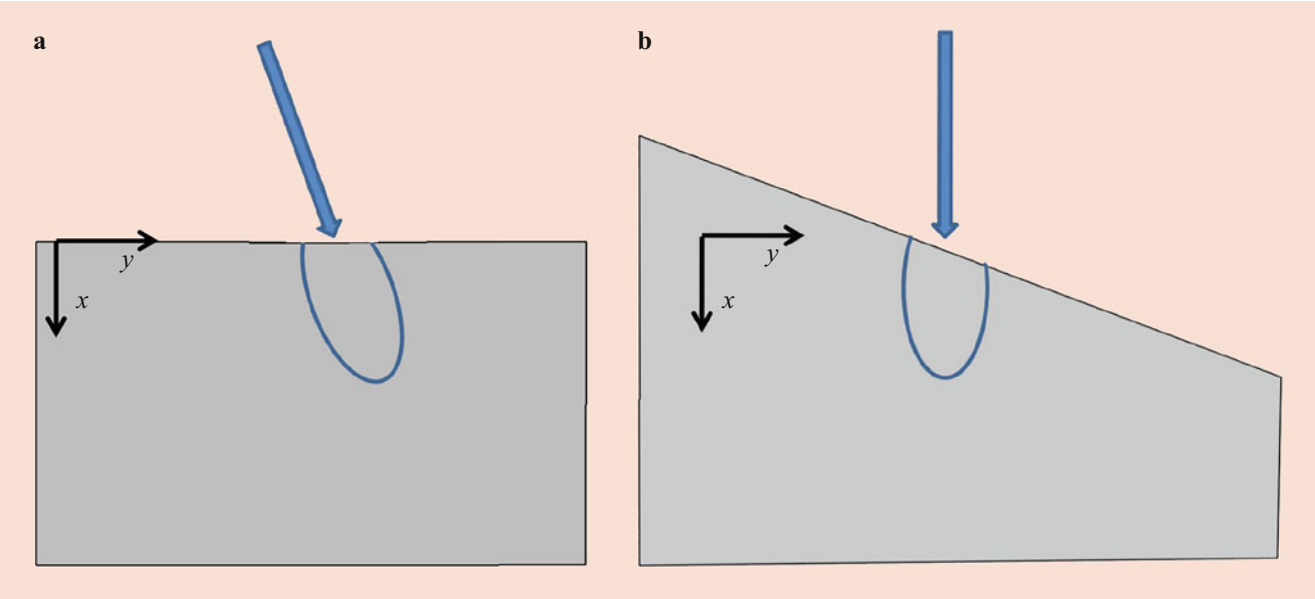

Fig. 35.3 Basic two-dimensional sketch for point response function for titled ion implantation. (**a**) Tilted implantation in standard coordinate system; (**b**) equivalent situation of vertical implantation into tilted wafer

above to both the crystalline and the amorphous Pearson distribution. However, already for the Numerical Range Scaling model explained above, a reasonable agreement with SIMS measurements was reported, and the benefit of applying the double Pearson approach together with NRS was rather limited [22].

In conclusion, in many cases Pearson distributions combined with the Numerical Range Scaling model (NRS) or better the Improved Numerical Range Scaling model (NRS') yield good approximations for one-dimensional dopant profiles. This depends of course on the quality of the range parameters, which must be provided upfront from other sources, as outlined below. The NRS model is also partly being used in commercial process simulation programs [11], however without the modification of the projected range straggling included in the NRS' model. The importance of the use of appropriate model parameters (range moments) is among others highlighted by the availability of different data sets, linking to earlier simulation programs, in current tools. Further refinements of one-dimensional analytical models for ion implantation appeared not to be very useful, due to the growing complexity of description and the need to provide additional parameters which would be difficult to obtain. This would diminish the advantages of analytical implantation models and can be considered as reason why the state-of-the-art in one-dimensional implantation models is about stable since many years.

Multidimensional Implantation Models

The basic approach in all multidimensional implantation models is that first a point response function $g(\boldsymbol{\eta}, \boldsymbol{\zeta})$ is calculated which describes for each point $\boldsymbol{\eta}$ in two or three dimensions the normalized distribution of the ions implanted just at one point $\boldsymbol{\zeta}$ of the wafer surface. Here, it is necessary to take into considerations that the implantation is usually tilted (by about 7°) compared with the wafer normal and rotated out of a two-dimensional simulation plain. This is equivalent to tilting and rotating the wafer geometry by the opposite angles and then considering vertical implantation into this modified structure; see Fig. 35.3. Therefore, in the following "vertical" means in direction of the implantation beam, and "lateral" means perpendicular to the implantation beam.

The two- or three-dimensional dopant distribution then results from the integration across all incident ions beams and multiplication with the implanted dose N_D:

$$C(\boldsymbol{\eta}) = N_\mathrm{D} \cdot \int g(\boldsymbol{\eta}, \boldsymbol{\zeta}) \, \mathrm{d}\boldsymbol{\zeta} \tag{35.19}$$

The main topic for multidimensional implantation models is then how to get the point response functions g. The methods range from simplistic analytical assumptions to extracting the point response functions from Monte Carlo simulations; see the corresponding subsection below. Similar to the one-dimensional (vertical) distribution described above, also g must be normalized to unity when integrating across the full two- or three-dimensional space.

The first model published dealt with the implantation through an ideal mask window, where vertical mask edges are situated at $-a$ and a. Strictly speaking the mask should

be infinitely thin (to avoid scattering of ions out of the mask into the mask window), but nevertheless the mask should completely stop ions implanted into the mask. Gaussian shapes of the point response function both in vertical and lateral direction (x and y) were assumed. For implantation at a point (0,y'), this reads

$$g(x,y) = \frac{N_\mathrm{D}}{\sqrt{2\pi}\,\Delta R_\mathrm{p}} \exp\left(-\frac{(x-R_\mathrm{p})^2}{2\Delta R_\mathrm{p}^2}\right) \cdot \frac{1}{\sqrt{2\pi}\,\Delta R_\mathrm{pl}} \exp\left(-\frac{(y-y')^2}{2\Delta R_\mathrm{pl}^2}\right) \tag{35.20}$$

and the convolution in Eq. (35.19) results in the two-dimensional dopant distribution [24].

$$\begin{aligned} C(x,y) &= \int g\left(x, y-y'\right) \mathrm{d}y' \\ &= \frac{N_\mathrm{D}}{\sqrt{2\pi}\,\Delta R_\mathrm{p}} \exp\left(-\frac{(x-R_\mathrm{p})^2}{2\,\Delta R_\mathrm{p}^2}\right) \cdot \\ &\quad \frac{1}{2}\left[\mathrm{erfc}\left(\frac{y-a}{\sqrt{2}\Delta R_\mathrm{pl}}\right) - \mathrm{erfc}\left(\frac{y+a}{\sqrt{2}\Delta R_\mathrm{pl}}\right)\right] \end{aligned} \tag{35.21}$$

where erfc is the complementary error function. Approaches like Eq. (35.21) are appropriate in case of device simulation studies which start from analytical dopant profiles. For different mask windows, simply the integration limits need to be changed accordingly. The simplest assumption for implanted and then annealed dopant profiles is to replace the standard deviations ΔR_p and ΔR_pl by

$$\sqrt{\Delta R_\mathrm{p}^2 + 2Dt} \text{ and } \sqrt{\Delta R_\mathrm{pl}^2 + 2Dt} \tag{35.22}$$

respectively, because after this replacement, both the point response function of Eq. (35.20) and in turn the dopant profile in Eq. (35.21) satisfy the linear diffusion equation valid for intrinsic diffusion:

$$\frac{\partial C}{\partial t} = D\Delta C \tag{35.23}$$

It should be kept in mind that both Gaussian point response functions for ion implantation and linear diffusion are very crude assumptions. However, assuming Gaussian implantation profiles also in lateral direction, without carrying out the convolution which leads to the complementary error functions erfc in Eq. (35.21), would lead to unphysical results and must be strictly avoided also as input for device simulation.

Two aspects are essential for the generalization of the point response function approach given in Eq. (35.19): First, $g(\boldsymbol{\eta}, \boldsymbol{\zeta})$ depends for each entry point $\boldsymbol{\zeta}$ on the local material and on the masking layers on top. Second, it is unphysical to assume that the lateral profile shape, e.g., for the implantation at just one point of the wafer surface, stays constant, independent of the depth: Heavy ions like arsenic are scattered less than light ions such as boron. In result the doping profile somewhat broadens with depth for heavy ions like arsenic, whereas it gets narrower for boron which has a higher likelihood to be backscattered toward the wafer surface. For easier presentation, in the following the two-dimensional case is discussed, whereas the extension to three dimensions is obvious. These effects can be considered by assuming a convolution between a vertical multilayer profile $f(x,y')$ as discussed in the preceding subsection and a lateral profile $g(x',y–y')$ which depends on the depth x':

$$C(x,y) = \int f\left(x,y'\right) g\left(x', y-y'\right) \mathrm{d}y' \tag{35.24}$$

Since the vertical distribution $f(x,y')$ is calculated at the lateral coordinate y', the masking effects of the layers through which the ion has passed is taken into consideration. For the lateral distribution $g(x',y–y')$, depending on the range parameters in question, a symmetric Pearson distribution should be used [25]. The vertical coordinate x' can either be equal to x, as in the original publication, or be equal to the entry point into the target for the lateral coordinate y', which is more complicated to implement. The usage of mixed models $X^i\,Y^j$ according to Eq. (35.8) allows to well describe the depth dependence of the lateral projected range [26] and the lateral kurtosis [27]. In the latter paper, a mix of a parabolic and an exponential approach was given for the depth dependence of the square of the lateral range straggling, whereas an exponential approach was presented for the depth dependence of the lateral kurtosis, in both cases depending on the vertical, the lateral, and the mixed range moments introduced in Eqs. (35.2), (35.3), (35.4), (35.5), (35.6), (35.7), and (35.8). Figure 35.4 shows as an example the comparison of the analytical model with Monte Carlo simulations, assuming depth-independent lateral profiles, depth-dependent lateral straggling, and depth-dependent lateral straggling and lateral kurtosis, respectively. In this latter case, the analytical model and the Monte Carlo simulations agree within the statistical error of the Monte Carlo results.

Model Parameters for Analytical Models

As mentioned above, analytical models need suitable vertical, lateral, and partly also mixed range moments. These must be provided upfront as tables depending on the combination of ion and target material, implantation energy, and potentially dose. For the latter two, a suitable number of

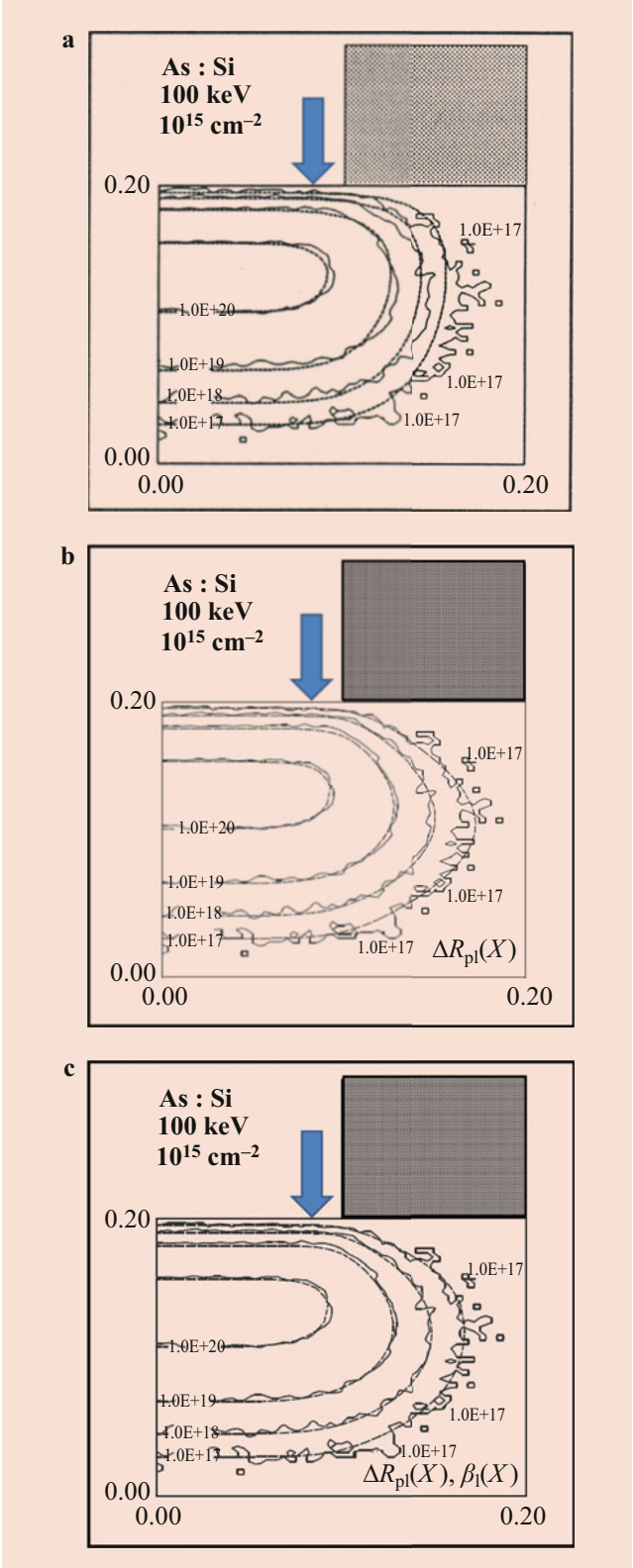

Fig. 35.4 Comparison between analytical model (broken lines) and Monte Carlo simulation of implantation of arsenic at an energy of 100 keV and a dose of 10^{15} cm^{-2} near an ideal mask edge. Equiconcentration lines of 10^{20} cm^{-3}, 10^{19} cm^{-3}, 10^{18} cm^{-3}, and 10^{17} cm^{-3} shown. (**a**) Standard model with ΔR_{pl} and β_{l} independent of depth x; (**b**) ΔR_{pl} depending on x; (**c**) ΔR_{pl} and β_{l} depending on x, leading to better agreement for low concentrations

discrete values is used. Whereas state-of-the-art characterization techniques such as SIMS enable the accurate measurement of vertical range profiles and, in turn, the extraction of appropriate vertical range moments, the possibilities for extraction of lateral and especially of mixed range moments from experiment are limited, and the experimental effort becomes excessive. Alternatively, for amorphous targets, all these range moments may be efficiently and accurately extracted from Boltzmann transport calculations, where this equation is not solved directly but its moments are calculated including their dependence on the implantation energy, starting from an infinitesimally small value. This approach was used in the RAMM code [14]. The range moments both for amorphous and for crystalline targets can also be extracted from two-dimensional Monte Carlo simulations, as described below. Here, a sufficient number of particle trajectories must be traced to yield sufficient accuracy of the moments while keeping computation time per implantation energy acceptable for the extraction of tables with various ion/target combinations and implantation energies. Both for the use of Boltzmann transport and Monte Carlo simulations, the use of appropriate physical models for electronic stopping and nuclear scattering, as outlined below, is mandatory. It was demonstrated in the literature [28] that for amorphous targets (vertical), range moments extracted from Boltzmann transport calculations with RAMM and from Monte Carlo simulations using the well-known TRIM code [29] agree well with experimental values obtained by SIMS measurements.

Analytical Models for Intrinsic Point Defects

Because subsequent annealing steps are critically influenced by the distribution of intrinsic point defects (especially vacancies and interstitials of crystal atoms), including those generated during ion implantation, there is a need to also include them in the analytical models for ion implantation. The problem is, however, that the capabilities to measure the distributions of intrinsic point defects are by far not sufficient to extract range moments. In turn, either very simple models are used for point defects or the required parameters have to be extracted from Monte Carlo simulations, as described below. It is also essential to take into account that point defects diffuse very fast and neighboring vacancies and interstitial atoms may partly recombine already during the implantation itself. In turn, in the "+1 model" as the simplest approach, it is assumed that one interstitial and no vacancies are generated per (and at the same position as the) ion implanted.

An established model which is also used in commercial simulators [11] was published already in 1988 [30]. Here, no difference is made between vacancies and interstitials. For the implantation of light ions such as boron and phosphorus, an exponential and a Gaussian function are joined at a position x_0 (naming of variables adapted from [30]), with the

parameters adjusted to assure continuity of the distribution and of its derivative at x_0:

$$(x) = \begin{cases} C_1 \cdot \exp\left(\frac{x}{a_1}\right), x \le x_0 \\ C_2 \cdot \exp\left[-\frac{(x-a_2)^2}{2 \cdot a_3{}^2}\right], x > x_0 \end{cases} \tag{35.25}$$

For heavy ions such as arsenic or antimony, the exponential and the Gaussian distribution are interchanged. The parameters C_1 and C_2 depend on a_1, a_2, a_3, the implantation dose, and the number of point defects generated per ion. In the literature the parameters a_1, a_2, and a_3 were extracted from Monte Carlo simulations, resulting in good agreement between the analytical defect profile and Monte Carlo simulations for the examples presented there. In addition, the lateral defect profile from Monte Carlo simulation could be fitted well with a Gaussian distribution.

For a further brief description of the assumptions used as initial condition for the simulation of post-implantation annealing, see Sect. 35.3.6.

35.2.2 Monte Carlo Simulation

For the Monte Carlo simulation of ion implantation, a large number of ion trajectories is traced until the implanted ions have been stopped, which means that their energy has been reduced to a negligible value. In case of relatively high doses and large structures (e.g., 100 nm scale, as shown in Fig. 35.4), the number of ion trajectories calculated is orders of magnitude smaller that the number of the particles implanted in reality. In consequence, in the simulations pseudo-particles are considered, which have the same properties as the real particles but each represent a large number of them.

The ion trajectories are governed by the energy transfer to the electron gas in the target, which is modeled by the so-called electronic stopping S_e and by the scattering at the (shielded) charges of the crystal lattice, the so-called nuclear scattering S_n:

$$S_{n,e} = -\frac{1}{N}\left(\frac{dE}{dx}\right)_{n,e} \tag{35.26}$$

The first general assumption made is the so-called binary collision approximation, in which only two-body problems are considered, where the impinging ion is at a time only scattered by the potential of one target atom. Because the masses of the implanted ions and of the target atoms are comparable (none of these can be neglected compared with the other), the scattering process is usually calculated not in the laboratory system but in the center-of-mass system. The relationship between implantation energy, masses, and scattering angles in both the laboratory system and the center-of-mass system is given in standard textbooks on mechanics or in standard literature on implantation [31]. First, the reduced mass m_c and the energy E_c of the projectile in the center-of-mass system have to be calculated from its mass m_1, energy E_0, and velocity v_0 in the laboratory system and the mass m_2 of the target atom:

$$m_c = \frac{m_1 \cdot m_2}{m_1 + m_2}; E_c = \frac{1}{2} m_c \cdot {v_0}^2 \tag{35.27}$$

The final results for the scattering angle in the center-of-mass system, Θ, the scattering angle in the laboratory system, ϑ; and energy transfer from the implanted ion to the target ion in the laboratory system are given by

$$\theta = \pi - 2\int_{r_{min}}^{\infty} \frac{p\,dr}{r^2 \cdot \sqrt{1 - \frac{V(r)}{E_c} - \frac{p^2}{r^2}}} \tag{35.28}$$

$$\tan\vartheta = \frac{m_2 \sin\Theta}{m_1 + m_2 \cos\Theta} \tag{35.29}$$

$$T = \frac{4\, m_1 m_2}{(m_1 + m_2)^2} E_0 \sin^2\left(\frac{\Theta}{2}\right) \tag{35.30}$$

Here, r is the distance between implanted ion and target atom during scattering, r_{min} its minimum value, for which the denominator in Eq. (35.28) equals zero. p is the impact parameter: the minimum distance between the implanted ion and the target in case the ion would not be scattered.

Physical Models

Besides the mechanical problem summarized above, physical models are needed for both the electronic stopping S_e and the nuclear scattering S_n. Because these should be applicable for arbitrary combinations of ions and targets, it is advisable to develop universal models which hold for all combinations. This is generally done by introducing an interatomic screening function $\phi(r)$ [31]:

$$\phi(r) = \frac{V(r)}{Z_1 Z_2 e^2 / r} \tag{35.31}$$

where the numerator is the actual shielded coulomb potential of the target ion and the denominator is the unshielded potential of the implanted ion with charge $Z_1\, e$ and the target atom with charge $Z_2\, e$. As discussed in literature [31], the so-called universal screening potential ϕ_U yields good interatomic potentials, with the Bohr radius a_0 of about 0.529 Å as the length scale:

$$\phi_U = 0.1818\, e^{-3.2x} + 0.5099\, e^{-0.9423x} + 0.2802\, e^{-0.4029x} + 0.02817\, e^{-0.2016x} \tag{35.32}$$

$$x = \frac{r}{a_u} \quad a_u = \frac{0.8854\, a_0}{Z_1^{2/3} + Z_2^{2/3}} \tag{35.33}$$

For the electronic stopping S_e, no universal equation is available. Calculation starts from a fit of the stopping power for protons and includes several scaling and correction steps [31].

Implementation

Current Monte Carlo (MC) simulation programs for ion implantation can be categorized according to the way the target is treated, either as amorphous or crystalline, and whether modifications of the target during implantation are considered or not. Furthermore, several approaches are available to speed up Monte Carlo simulations. Well-known historical examples for MC codes are the amorphous Monte Carlo code TRIM [29] and the crystalline Monte Carlo code MARLOWE [32]. Current MC codes are numerous, including implementations provided by software houses.

Amorphous Monte Carlo simulation: In the simplest case, the target is treated as amorphous, and the effect of modifications during the implantation process on the particle trajectories is neglected. In this case, the true positions of the target atoms are not considered. Employing the binary collision approximation mentioned above, a straight ion trajectory is assumed between the individual scattering effects, which are separated by an assumed mean free path length L. Because most scattering processes occur at impact parameters p which are that large that the scattering angles ϑ (and the transferred energy T) can be neglected, for L a value significantly larger than the interatomic spacing of the (neglected) crystal lattice can be chosen. In parallel, the maximum impact parameter p_{max} to be considered is limited. For consistent simulation, the cylinder with p_{max} as radius and L as length must contain one target atom:

$$\pi \cdot p_{max}^2 \cdot L = \frac{1}{N} \tag{35.34}$$

where N is the density of target atoms. Besides that Eq. (35.34) must be fulfilled, the choice of L and p_{max} depends on the Monte Carlo simulator in question. The actual value of p^2 is then selected at random between 0 (head-on collision with scattering angle 180°) and ${p_{max}}^2$. The scattering angle ϑ and the energy loss T of the ion in the laboratory system are calculated according to Eqs. (35.27), (35.28), (35.29), (35.30), (35.31), (35.32), and (35.33). Between the individual scattering events, the ion energy is reduced by integration of the electronic stopping S_e along the straight path between the scattering events. An approximation for the number of point defects generated is frequently made based on the Kinchin-Pease formula [33, 30], according to which this number is proportional to the ratio of the transferred energy T (or a fraction of this) and the energy needed to generate a Frenkel pair (crystal atom leaving its site and generating a pair of vacancy and interstitial).

Whereas the analytical simulation of ion implantation is in general computationally less expensive, the use of amorphous Monte Carlo simulations is advisable if no suitable range parameters are available, or especially if implanted ions cross interfaces between different layers (including free space) beyond the limitations of the multilayer or multidimensional analytical models summarized above. A common situation where this applies is ion implantation into the neighborhood of a trench. In this case, a significant fraction of the implanted ions is scattered out of the material and into the trench, causing doping of the opposite sidewall of the trench. An example is given in Fig. 35.5.

Crystalline Monte Carlo simulation: The inclusion of the crystal structure increases the program complexity and the computational effort. In essence, based on the current position and direction of flight of the ion, the next neighboring crystal atom is located, or the next few neighboring crystal atoms are identified. In the first case, the binary collision approximation can be used directly, calculating the impact parameter p and subsequently the transferred energy T and the scattering angle ϑ. In the second case in principle, the scattering of an ion in the superposition of two or more screened potentials ϕ_i would need to be calculated, for which in general no analytical formula is available. In turn, this problem is approximated by applying the binary collision approximation separately to each of the scattering processes identified. The details how to extract the final energy transfer T and the scattering angle ϑ for these individual scattering events depend on the simulation code in question. Random parameters are mainly the impact parameter of the first collision of the incident ion with a crystal atom and partly thermal vibrations of the target atoms.

The benefit of the crystalline Monte Carlo simulation, beyond the amorphous Monte Carlo simulation outlined above, is its capability to simulate channeling. For standard implantation into crystalline silicon, where tilt and rotation angles are selected to minimize residual channeling, also analytical models can provide appropriate distributions of implanted ions, provided the models summarized at the beginning of this section are used with suitable range parameters for the combination of implanted ion and crystalline target in question. Such range parameters can be extracted from point response functions obtained from crystalline Monte Carlo

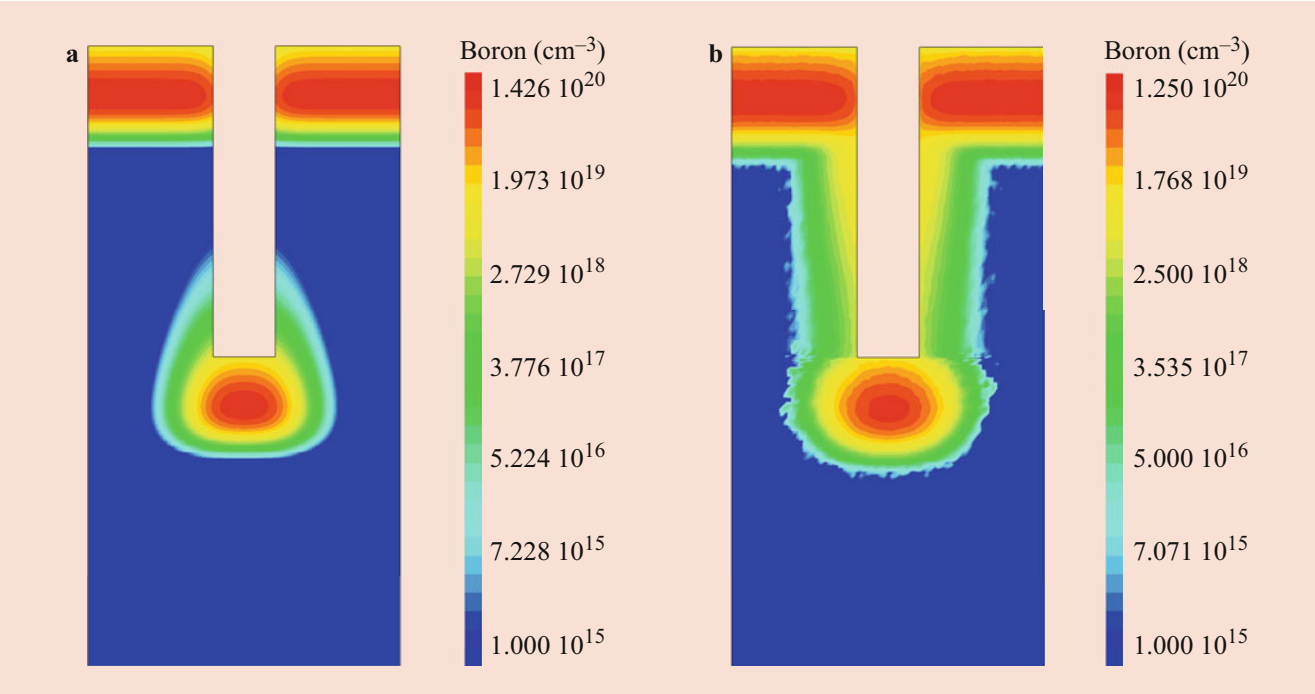

Fig. 35.5 Simulation of implantation of boron at an energy of 20 keV and a dose of 10^{15} cm^{-2} into amorphous silicon with a trench. (**a**) Analytical simulation; (**b**) amorphous Monte Carlo simulation. The doping of the sidewall for the trench cannot be described with analytical methods

simulations or partly from measurements of dopant profiles. On the other hand, advanced materials such as SiC partly show pronounced channeling effects which moreover depend on covering layers of oxide, as illustrated in Fig. 35.6 [34]. The doping spikes occurring here cannot be reasonably described by analytical models.

Dynamic Monte Carlo simulation: The next extension is the inclusion of target modifications which occur when the implanted ion kicks a crystal atom (or an ion implanted before) from its current position. This may even generate cascades of secondary particles. Here, an atom leaves its position in case the energy T transferred to it exceeds a critical value. In consequence, the trajectory of this knock-on particle must be simulated with the same approach as the trajectory of the implanted ion. This increases both the amount of data to be stored and the computational effort. The benefit is that dynamic effects like target modification (e.g., sputtering and amorphization) and the dose dependence of channeling are as well included in the simulations as the extraction of the distributions of the vacancies and interstitials generated.

Statistics: Generally, Monte Carlo simulations require the calculation of a large number of ion trajectories, depending on the dimensionality of the problem and on the size of the simulation domain. For example, for the three-dimensional simulation of source-drain implantation about 100,000 ion trajectories should be calculated to achieve a "smooth" doping profile without artificial fluctuations, resulting in computation times of minutes to hours on a standard PC, depending on ion mass and energy. This situation changes if the simulation domain and the implantation dose are small enough to allow the simulation of the trajectory of each implanted ion: Here, the fluctuations are physically meaningful and part of the results required.

The statistics of Monte Carlo simulations can easily be improved in either of two ways: The first approach is to just calculate a point response function for one surface point and then to copy this on a suitable mesh of surface points, rather similar to the calculation and use of analytical point response functions [35]. Second, in the trajectory split approach [36], the pseudo-particles are split into two or more particles as soon as they enter areas with low concentration of implanted species. The pseudo-particles resulting from these split then represent an accordingly smaller number of real particles and are in turn considered with a lower statistical weight. Their further trajectories are then calculated using random numbers which are independent between these trajectories. This splitting procedure may be repeated several times for decreasing concentrations of the implanted ions. In consequence, additional calculations are only carried out for the relatively rare parts of the trajectories which are situated in low-concentration areas.

Monte Carlo simulation can also be applied to describe novel processes such as plasma doping (PLAD) (also named plasma immersion ion implantation), where charged ions are extracted from a plasma, in order to generate shallow doping profiles with high ion currents. Besides source-drain profiles,

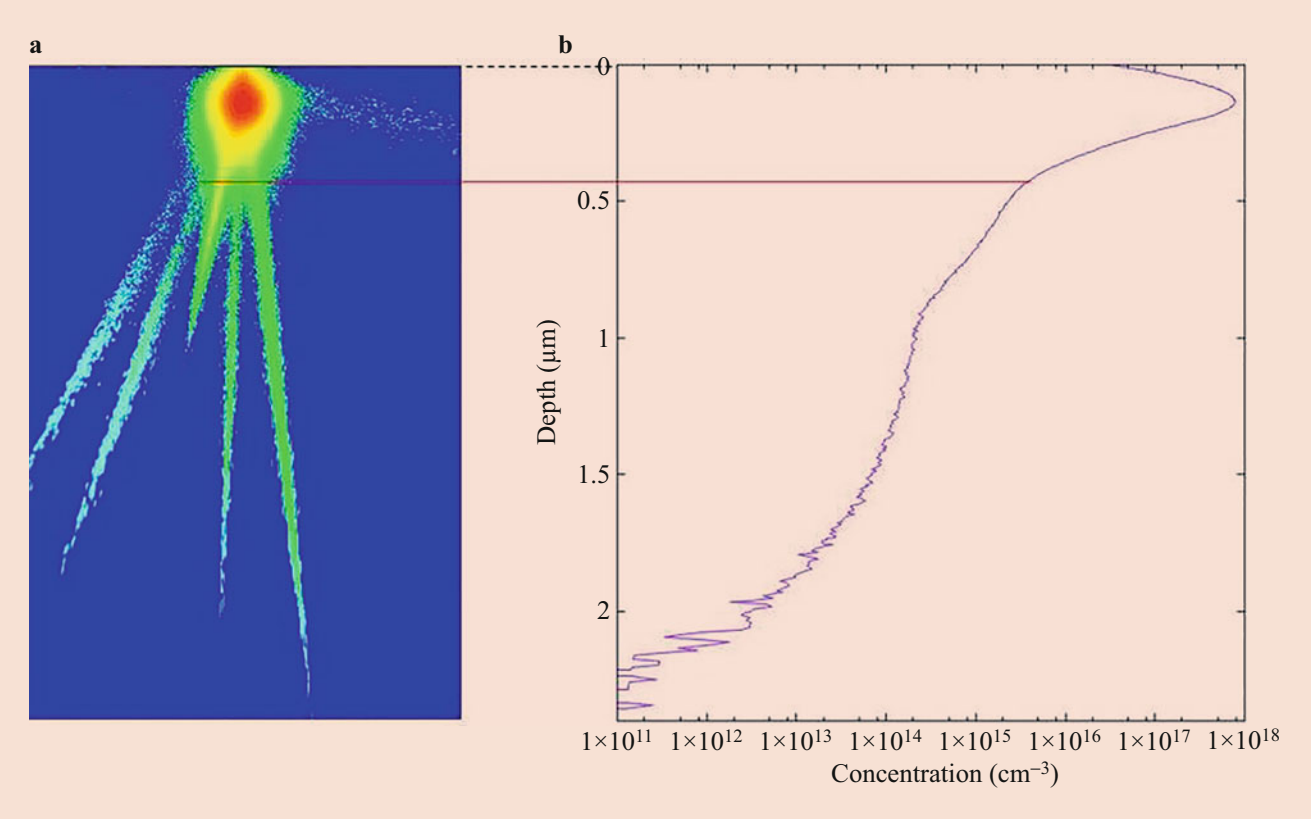

Fig. 35.6 Monte-Carlo simulation of implantation of aluminum at an energy of 140 keV and a dose of 10^{13} cm^{-2} into 4H SiC covered with a 30 nm thick oxide layer: (**a**) 2D point response function and (**b**) 1D vertical profile [34]

PLAD can also be used to generate surface-conformal doping of trenches or FinFETs. For the simulation of PLAD, the energetic distribution of ions can be extracted from physical considerations on the plasma sheath [37] and finally be approximated by analytical expressions, as, e.g., in [38]. This distribution can then be fed into Monte Carlo simulators as described above, which are then used to calculate the spatial distribution of the implanted ions.

35.3 Simulation of Diffusion and Activation

During any process steps at elevated temperatures, the thermally induced movement of dopant atoms and other impurities may lead to a noticeable broadening of their distribution as well as to quasi-chemical reactions with other atoms of the same or other impurity species or with intrinsic point defects. For dopants, the latter typically manifests itself in an electrical activation which is lower than the respective total concentration. Annealing processes at elevated temperatures are used intentionally, e.g., to drive-in dopants deeply into power semiconductors or to electrically activate implanted dopants and to anneal the damage created by the ion implantation processes. However, as indicated already, diffusion and reduced electrical activation may originate from any technological process at high-enough temperatures whether during front-end or back-end processing. In the following, the most important concepts associated with diffusion phenomena in semiconductors are outlined with an emphasis on silicon. For a more comprehensive presentation, the interested reader is referred to reviews such as [5, 39, 40, 41].

35.3.1 Intrinsic Point Defects and Impurities

In crystalline semiconductor materials like silicon, germanium, or SiGe alloys, most of the atoms of which the semiconductor consists are arranged in the form of a diamond structure. In other semiconductors like SiC, the atoms may be arranged in cubic or hexagonal structures. Only few atoms may be missing from their lattice sites or can be found elsewhere. Since such defective atomic arrangements affect only their nearest neighbors, they are referred to as "point defects." Point defects comprising only atoms of which the semiconductor consists of are called "intrinsic point defects." Empty lattice sites, as shown schematically in Fig. 35.7a, are referred to as vacancies. For silicon, even close to the

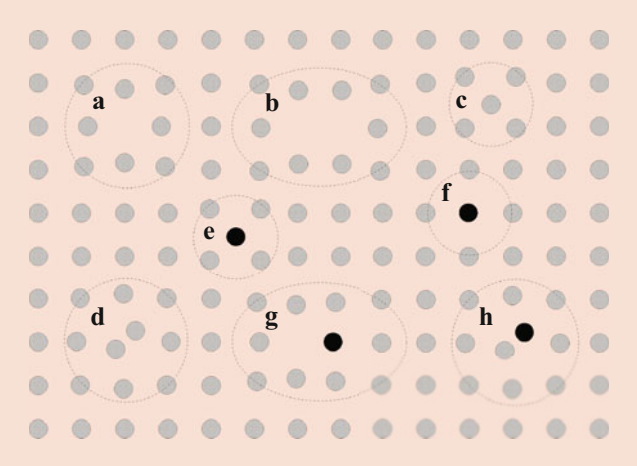

Fig. 35.7 Schematic representation of point defects in elemental semiconductors: (a) Vacancy, (b) divacancy, (c) self-interstitial, (d) interstitialcy, (e) interstitial impurity, (f) substitutional impurity, (g) impurity-vacancy pair, (h) impurity-self-interstitial pair. (after [5])

melting point, less than one out of 10^7 silicon atoms are expected to be missing. Vacancies on neighboring sites (see Fig. 35.7b) are called divacancies. The counterpart of vacancies are semiconductor atoms which either occupy as self-interstitials sites between the lattice atoms as in Fig. 35.7c or share with another semiconductor atom a lattice site as in Fig. 35.7d. Such an atomic configuration is usually referred to as interstitialcy, split-interstitial, or dumb-bell interstitial. Similar to vacancies, less than one out of 10^7 silicon atoms are expected to occupy such interstitial positions even close to the melting point.

Atoms differing from the semiconductor atoms are called impurities. Some of them like oxygen or hydrogen occupy preferentially interstitial sites as indicated in Fig. 35.7e. By far the most important impurities for the Group-IV semiconductors (Si, Ge, SiGe, SiC, etc.) are dopant atoms from the Groups III and V of the periodic system. They preferentially substitute the lattice atoms as shown schematically in Fig. 35.7f. Dopants from Group III require an additional electron to satisfy the four valence bonds to the neighboring silicon atoms which leads to the formation of a hole in the valence band. Based on their ability to "accept" an electron, the Group III atoms are referred to as "acceptors." Substitutional Group V atoms, on the other hand, have one electron too many and can donate it to the conduction band. Accordingly, they are referred to as "donors." In addition to occupying interstitial and substitutional sites, impurities may be found in pairs with vacancies as in Fig. 35.7f or with silicon atoms sharing a regular lattice site as in Fig. 35.7h.

Vacancies can be thought to result from taking one of the lattice atoms from its site and dragging it to a kink at the surface of the semiconductor. Similarly, the intrinsic interstitial defects can be thought to result from dragging semiconductor atoms from a kink at the surface to the respective site. In addition, both can be created as pairs by dragging a lattice atom to an interstitial position and vice versa annihilated by dragging an interstitial atom to a vacancy. The latter processes are usually referred to as bulk generation and recombination of intrinsic point defects.

The probability to find intrinsic point defects in a specific metastable atomic configuration reflects the respective free energy of formation $G^{\mathrm{f}}_{\mathrm{X}}$. Accordingly, it is not "either-or" but rather "as well as" to find intrinsic point defects in the one or the other configuration. Because of that, it makes hardly sense to discern self-interstitials and interstitialcies, and all such configurations will be referred to as self-interstitials in the following. Besides the point-like configurations, vacancies and self-interstitials were assumed to exist in an extended state, i.e., that one atom in an overall tetrahedrally coordinated region comprising some 10–20 silicon atoms is missing or too much. In the most recent work of Voronkov and Falster [42], as an example, vacancies in three different configurations are postulated to coexist to explain a multitude of seemingly contradictory phenomena.

For the impurity complexes, the situation depends on how the impurities are introduced. For impurities in a closed system, the relative concentrations of the particular atomic configurations need to sum up to the total concentration. For systems in which dopants can enter from a reservoir, their formation energy in the semiconductor will determine the solubility concentration of the impurity in the semiconductor; see Sect. 35.3.8.

Given the concentration of possible sites C_{XS} at which a specific defect can be realized and the number Θ_{X} of internal degrees of freedom of the defect at a specific site, the concentration of a defect X in steady state is given by

$$C^{\mathrm{eq}}_{\mathrm{X}} = \Theta_{\mathrm{X}}\, C_{\mathrm{XS}} \exp\left(-\frac{G^{\mathrm{f}}_{\mathrm{X}}}{kT}\right) \tag{35.35}$$

with k standing for Boltzmann's constant and T for the absolute temperature. For charged defects, G^{f} will depend on the Fermi level. Deviations of the Fermi level can be expected for dopant concentrations which exceed significantly the charge carrier concentration n_{i} which would be found under intrinsic conditions, i.e., without dopants. Assuming Boltzmann statistics to be a valid approximation at elevated temperatures, the concentration of a defect in a particular charge state can be expressed in terms of the concentration C_{X^0} of the neutral charge state and the electron concentration n as.

$$\begin{aligned} C_{\mathrm{X}^-} &= C_{\mathrm{X}^0}\delta_{\mathrm{X}^-}\left(\frac{n}{n_{\mathrm{i}}}\right) & C_{\mathrm{X}^=} &= C_{\mathrm{X}^0}\delta_{\mathrm{X}^=}\left(\frac{n}{n_{\mathrm{i}}}\right)^2 \\ C_{\mathrm{X}^+} &= C_{\mathrm{X}^0}\delta_{\mathrm{X}^+}\left(\frac{n_{\mathrm{i}}}{n}\right) & C_{\mathrm{X}^{++}} &= C_{\mathrm{X}^0}\delta_{\mathrm{X}^{++}}\left(\frac{n_{\mathrm{i}}}{n}\right)^2 \end{aligned} \tag{35.36}$$

Therein, the charge states have been indicated by $-$, $=$, 0, $+$, and $++$ for singly negative, double negative, neutral,

positive, and doubly positive. The respective δ_X denote the relative concentration under intrinsic conditions.

35.3.2 Basic Diffusion and Reaction Mechanisms

Simple point defects diffuse by jumping from one energetically favorable site to a neighboring one. In case of simple interstitial impurities as depicted schematically in Fig. 35.7e or h, it is the migrating atom itself which performs the jumps. For the self-interstitial configurations in Fig. 35.7c, d, it could also be always the same silicon atom that moves from site to site. However, it could also be that a self-interstitial assumes the site of a neighboring lattice atom and displaces it to the interstitial site. Finally, the vacancies shown in Fig. 35.7a move when a neighboring semiconductor atom jumps into the vacant lattice site. As long as such point defects do not interact and as long as no forces like electric fields have to be considered, the evolution of their concentration can be described by Fick's laws. Fick's first law

$$J_X = -D_X \operatorname{grad} C_X \tag{35.37}$$

establishes a purely phenomenological definition of the diffusion coefficient D_X of a defect X as a proportionality constant between the net number of defects passing a unit area per time, the diffusion flux J_X, and the gradient of the defect concentration C_X. Fick's second law

$$\frac{\partial C_X}{\partial t} = \operatorname{div}(-J_X) = \operatorname{div}(D_X \operatorname{grad} C_X) \tag{35.38}$$

is a combination of Fick's first law with a continuity equation and constitutes a diffusion equation that can be used to calculate the change in concentration due to diffusion as a function of time t. The concept of a concentration and a gradient obviously requires a certain number of defects per unit volume considered. A complementary view can be obtained by observing the movement of a single defect through the crystal. Given the projection of the mean jump distance L between two stable configurations on one of the axes of the coordinate system, the mean square displacement of the defect from its origin

$$\langle D_N{}^2 \rangle = NL^2 \tag{35.39}$$

increases linearly with the number N of its jumps. As shown by Einstein more than a century ago, the mean square displacement can be used as an atomistic definition of the diffusion coefficient D in (35.37) and (35.38) in the form

$$D = \frac{\langle D_N{}^2 \rangle}{2t} = \Gamma \frac{L^2}{2} \tag{35.40}$$

with $\Gamma = N/t$ standing for the number of jumps per time. In general, the diffusion coefficient is a tensor. However, for diamond structures like silicon or germanium, it reduces to a scalar. Transitions between energetically favorable positions require that an energetically less favorable saddle point is assumed and overcome. Diffusive jumps usually require the motion of more atoms than just the moving one. Accordingly, not only the increase in enthalpy H^m at the saddle point has to be considered but also the different entropy S^m of the system. Altogether, the jump frequency is usually expressed as

$$\Gamma = \Gamma_0 \exp\left(\frac{S^m}{k}\right) \exp\left(-\frac{H^m}{kT}\right) \tag{35.41}$$

with the attempt frequency Γ_0. Combining (35.40) and (35.41), diffusion coefficients can be written in the form of an Arrhenius law

$$D = D_0 \exp\left(-\frac{H^m}{kT}\right) \tag{35.42}$$

where the prefactor D_0 comprises all temperature-independent terms. The diffusion coefficient of interstitial oxygen in silicon, as an example, follows this relationship from cryogenic temperatures to the melting point for more than 13 decades [43]. Depending on the species, usual values for the activation energy H^m range from 0 to 5 eV for silicon. To include the effects of mechanical stress on the diffusion coefficient, its temperature dependence (35.42) is completed for hydrostatic pressures P in the form

$$D = D_{P=0} \exp\left(-\frac{P\Delta V}{kT}\right) \tag{35.43}$$

introducing the activation volume ΔV. Positive numbers for the activation volume mean retarded diffusion for compressive stress and enhanced diffusion for tensile stress and vice versa for negative activation volumes. In magnitude, activation volumes are expected to range up to the volume associated with a lattice atom. For non-hydrostatic pressures, a tensor form has to be adopted in which the hydrostatic pressure is replaced by the strain tensor and the activation volume by a strain-activation tensor.

As indicated already above, defects are expected to coexist in a variety of charge states. In case of dopant concentrations exceeding the intrinsic concentration of charge carriers n_i, an electric field will be established in the semiconductor which exerts a force on the charged defects. Accordingly, the diffusive jumps will be biased since the defects gain or lose energy when they move in the field from their energetically favored site to the saddle point. To include such effects, Fick's first law is adapted in the form

$$J_X = -D_X \operatorname{grad} C_X - z_X \mu_X C_X E \tag{35.44}$$

where the charge state z has been defined here as the number of negative charges associated with the charge state (i.e., $+1$ for a singly negatively charged defect or -2 for a doubly positively charged defect). It should be noted, however, that an association of the charge state with the number of positive charges is just as common in the literature. The mobility μ was already shown by Einstein to be related to the diffusion coefficient by

$$D/\mu = kT/q \tag{35.45}$$

with q standing for the elementary charge. Expressing the electric field as the negative gradient of the electrostatic potential ψ, (35.44) takes the familiar form

$$J_\mathrm{X} = -D_\mathrm{X} \operatorname{grad} C_\mathrm{X} + z_\mathrm{X} D_\mathrm{X} C_\mathrm{X} \operatorname{grad}\left(\frac{\psi}{U_\mathrm{T}}\right) \tag{35.46}$$

with the thermal voltage U_T introduced for kT/q.

With defects co-existing in a number of charge states, any charge state contributes to the diffusion process with a different diffusion coefficient. Adding the contributions of the individual charge states to total concentrations and fluxes, one arrives again at the diffusion Eqs. (35.38) and (35.46). The diffusion coefficients and charge states in these equations are Fermi-level-dependent mean values weighted with the relative concentration of the respective charge state. However, particularly for vacancies and self-interstitials, the experimental knowledge is far from allowing to establish such dependences, and one pragmatically uses Fermi-level-independent values.

The situation becomes more complicated in case of dopants and other impurities which preferentially reside on substitutional sites as indicated in Fig. 35.7f. In such a configuration, the respective atoms are assumed to be immobile. To diffuse, they need to come into an interstitial configuration as depicted schematically in Fig. 35.7e, h or in a configuration with a vacancy as indicated in Fig. 35.7g. Diffusion as interstitials as in Fig. 35.7e is expected particularly for transition metals like gold and platinum. For boron in silicon, as another example, diffusion as pair with self-interstitials in analogy to Fig. 35.7h was suggested by Windl et al. [44] on the basis of ab initio calculations. Other elements like antimony in silicon and most dopants in germanium are assumed to diffuse via bound pairs with vacancies as shown schematically in Fig. 35.7g. Since even multiple exchanges of sites between vacancy and dopant would not lead to an effective movement, this mechanism requires that the vacancy partially dissociates from the dopant and returns to another nearest neighboring site of the impurity. In general, dopants will diffuse via both, self-interstitials and vacancies, although one of these mechanisms may dominate. Despite the atomistically completely different mechanisms, migrating interstitial atoms and pairs with intrinsic point defects are assumed to diffuse macroscopically as entities. As such, diffusion coefficients and charge states can be assigned to them, and their movement can be described in analogy to the concepts discussed above.

With substitutional impurity atoms being assumed immobile, the mobile dopant complexes must form dynamically. For boron and self-interstitials, De Salvador et al. [45] were able to clarify experimentally the complex reaction paths to mobile pairs. However, this is a rare case and for most other pair-formation reactions, such a detailed knowledge is not available. Accordingly, pair formation is usually described in a more generic way. Such pair-diffusion models were pioneered by Yoshida et al. [46] who proposed that substitutional impurities M_s form mobile MV pairs, depicted schematically in Fig. 35.7g, with vacancies V by the quasi-chemical reaction:

$$M_\mathrm{s} + V \underset{k_{\mathrm{MV}\leftarrow}}{\overset{k_{\mathrm{MV}\rightarrow}}{\rightleftharpoons}} \mathrm{MV}. \tag{35.47}$$

The analogy for self-interstitials I is the formation of mobile MI pairs, shown schematically Fig. 35.7h, via

$$M_\mathrm{s} + I \underset{k_{\mathrm{MI}\leftarrow}}{\overset{k_{\mathrm{MI}\rightarrow}}{\rightleftharpoons}} \mathrm{MI}. \tag{35.48}$$

Within the level of description of process simulation, it is not important whether MI is a bound impurity-self-interstitial pair or an interstitial impurity M_i. Interactions of self-interstitials with dopants were probably first considered by Seeger and Chik [47] in the form of their interstitialcy mechanism. For metal interstitials, one usually refers to the kick-out mechanism suggested by Gösele et al. [48]. In addition to the pairing reactions, one needs to include the bulk-recombination reaction

$$I + V \underset{k_{\mathrm{IV}\leftarrow}}{\overset{k_{\mathrm{IV}\rightarrow}}{\rightleftharpoons}} 0 \tag{35.49}$$

of self-interstitials and vacancies to an undisturbed lattice site symbolized by the "0." For metal diffusion, instead of the formation of vacancy pairs, one needs to consider the reaction of metal impurities with vacancies

$$M_\mathrm{i} + V \rightleftharpoons M_\mathrm{s} \tag{35.50}$$

proposed first by Frank and Turnbull [49] for copper in germanium. For the diffusion of dopants in semiconductors, such a reaction, just as the counterpart of a dopant-vacancy

pair reacting with a self-interstitial

$$\mathrm{MV} + I \rightleftharpoons M_s, \tag{35.51}$$

constitutes a dopant-concentration-dependent parallel path to the recombination of self-interstitials and vacancies which also influences the concentrations of the pairs in steady state.

A quantitative description of the full system requires that the interactions between intrinsic point defects, substitutional impurities, mobile impurities and mobile complexes of impurities with intrinsic point defects, etc., are taken into account. This is usually done via the methodology of diffusion-reaction equations by writing, e.g., the interaction of species A with species B to species C in the form of the binary quasi-chemical reaction

$$A + B \underset{k_{\leftarrow}}{\overset{k_{\rightarrow}}{\rightleftharpoons}} C \tag{35.52}$$

with $k_{\rightarrow}$ and $k_{\leftarrow}$ being the forward and backward reaction constants. The reaction term

$$R = k_{\rightarrow} C_\mathrm{A} C_\mathrm{B} - k_{\leftarrow} C_\mathrm{C} \tag{35.53}$$

is common to the continuity equations of the species A to C

$$\begin{aligned} &\frac{\partial C_\mathrm{A}}{\partial t} = \operatorname{div}(-J_\mathrm{A}) - R; \quad \frac{\partial C_\mathrm{B}}{\partial t} = \operatorname{div}(-J_\mathrm{B}) - R; \\ &\frac{\partial C_\mathrm{C}}{\partial t} = \operatorname{div}(-J_\mathrm{C}) + R \end{aligned} \tag{35.54}$$

and couples them. The different signs of the reaction term in the continuity equations mean that the concentrations of A and B are reduced when A and B react, while the concentration of species C increases. In the common case of several parallel reactions, the respective reaction terms are added or subtracted in the continuity equations of the species. For immobile species like substitutional dopants, the diffusion term is simply omitted in the continuity equation. In equilibrium or stead state, the concentration of the product can be expressed as

$$\begin{aligned} C_\mathrm{C}^\mathrm{eq} &= C_\mathrm{A}^\mathrm{eq} C_\mathrm{B}^\mathrm{eq} \frac{\theta_\mathrm{C}}{\theta_\mathrm{A}\theta_\mathrm{B}} \exp\left(\frac{G_\mathrm{A}^\mathrm{f} + G_\mathrm{B}^\mathrm{f} - G_\mathrm{C}^\mathrm{f}}{kT}\right) \\ &= \frac{\theta_\mathrm{C}}{\theta_\mathrm{A}\theta_\mathrm{B}} \exp\left(\frac{G^\mathrm{B}}{kT}\right) \end{aligned} \tag{35.55}$$

in terms of the respective concentrations of the reactants, the numbers of internal degree of freedom of the defects at specific sites θ_X, and their formation energies G_X^f. As long as charge is conserved in the reaction, the binding energy G^B will be independent of the Fermi level. A particular advantage of binary reactions is that the forward reaction rates can be estimated on the basis of Waite's theory of diffusion-limited reactions [50] in the form

$$k_{\rightarrow} = 4\pi a_\mathrm{R} (D_\mathrm{A} + D_\mathrm{B}) \tag{35.56}$$

as a function of the diffusion coefficients of the reacting species and the recombination radius a_R which is usually assumed to be on the order of the bond length between two lattice atoms. For the cases that both particles are electrically charged and that reaction barriers have to be overcome, extensions are available from Debye [51] and Waite [52], respectively. To determine the backward rate, two procedures have been used in literature. The first one is based on the concept that the backward reaction constant $k_{\leftarrow}$ is basically the break-up frequency of the defect. This is very similar to (35.43) with S^m and H^m replaced by the dissociation entropy and enthalpy of the defect C. The second method uses the fact that the forward and backward reaction rates of all reactions need to cancel out in equilibrium. Accordingly, the ratio of forward and backward reaction rate can be written in terms of the equilibrium concentrations of the species

$$\frac{k_{\rightarrow}}{k_{\leftarrow}} = \frac{C_\mathrm{C}^\mathrm{eq}}{C_\mathrm{A}^\mathrm{eq} C_\mathrm{B}^\mathrm{eq}} \tag{35.57}$$

which in turn can be written via (35.55) in terms of the binding energy of the reaction.

35.3.3 Macroscopic Diffusion Behavior of Dopants

Within the methodology of diffusion-reaction equations outlined in the previous subsection, mobile complexes are postulated to form via the reactions (35.47) and (35.48). In addition, the complementary reactions of the mobile complexes with intrinsic point defects via the reactions (35.50) and (35.51) need to be taken into account. To calculate the generation rate of the mobile complexes, concurrent reactions between substitutional dopants and intrinsic point defects in all charge states have to be included. For the mobile complexes, the single negative, neutral, and single positive charge states are usually considered, and steady state between them is assumed to be established rapidly. The resulting system of coupled partial differential equations then consists of the continuity equations for the self-interstitials and vacancies as well as for each dopant in continuity equations for the substitutional dopants and the pairs with self-interstitials and vacancies. Accordingly, this type of diffusion model is commonly referred to as "five-stream model." Although already a simplification, five-stream models are able to capture fairly complex diffusion phenomena. To illustrate some of

them, useful simplifications and their areas of application are discussed below.

As indicated first by Cowern et al. [53], a dynamic description of the formation of mobile dopant species is important to understand the macroscopic diffusion behavior for short annealing times. To illustrate this, we consider a simple system in which a substitutional impurity M_s changes with a frequency $1/\tau$ into the mobile state MI. Denoting the steady-state ratio of the concentrations in the substitutional and the mobile state by α and assuming that the diffusion flux follows Fick's first law (35.37), one arrives at a coupled system of equations in the form

$$\begin{aligned} \tfrac{\partial C_{M_s}}{\partial t} &= -\tfrac{1}{\tau} C_{M_s} + \tfrac{\alpha}{\tau} C_{\mathrm{MI}}, \\ \tfrac{\partial C_{\mathrm{MI}}}{\partial t} &= \operatorname{div}\left(D_{\mathrm{MI}} \operatorname{grad} C_{\mathrm{MI}}\right) + \tfrac{1}{\tau} C_{M_s} - \tfrac{\alpha}{\tau} C_{\mathrm{MI}}. \end{aligned} \tag{35.58}$$

Assuming that all atoms are initially in a narrow layer in a depth of 0.5 µm, the total concentration $C_{\mathrm{M}} = C_{M_s} + C_{\mathrm{MI}}$ for $\alpha = 1000$ and D_{MI} chosen so that the macroscopic projected diffusion length for the time τ equals $\sqrt{2 D_{\mathrm{MI}} \tau / \alpha} = 10$ nm is shown in Fig. 35.8 (coupled system) together with a simulation in which steady state between the substitutional and interstitial species is assumed (one equation). For the latter case, the diffusion equation results for all times in the Gaussian profiles shown. The same profiles are obtained for the coupled system for long diffusion times for which substitutional and mobile impurities are in steady state. In contrast, for the shortest time, the delta-doped layer is still clearly visible, and the profile has a characteristic shape with exponentially decreasing flanks.

For sufficiently long diffusion times, the substitutional impurities will be in steady state with the respective mobile species. To calculate concentrations of the mobile complexes, as emphasized by Cowern [54], one needs to consider the pairing reactions (35.47) and (35.48) as well as the reactions of the pairs with the opposite intrinsic point defects via the reactions (35.50) and (35.51). This leads in non-equilibrium situations to a nonlinear dependence of the pair concentration on both the self-interstitial and vacancy concentrations. However, for the important case that bulk recombination maintains local equilibrium between the intrinsic point defects ($C_{\mathrm{I}} C_{\mathrm{V}} \sim C_{\mathrm{I}}^{\mathrm{eq}} C_{\mathrm{V}}^{\mathrm{eq}}$), the same pair concentrations are predicted as in the case that the reactions (35.50) and (35.51) are ignored and the pair concentrations can be calculated from (35.55). Considering the diffusion of dopants, one has to keep in mind that acceptors on substitutional sites are negatively charged and donors positively. Accordingly, the concentrations of single negative, neutral, and single positive pairs C_{MX}, with X standing either for self-interstitials I or vacancies V, will be

$$\begin{aligned} C_{\mathrm{MX}^-} &= \eta_{\mathrm{MX}^-} C_{M_s^-} \frac{C_{\mathrm{X}}}{C_X^{\mathrm{eq}}}; \; C_{M\mathrm{X}^0} = \eta_{\mathrm{MX}^0} C_{M_s^-} \frac{C_{\mathrm{X}}}{C_{\mathrm{X}}^{\mathrm{eq}}} \frac{p}{n_{\mathrm{i}}}; \\ C_{\mathrm{MX}^+} &= \eta_{\mathrm{MX}^+} C_{M_s^-} \frac{C_{\mathrm{X}}}{C_{\mathrm{X}}^{\mathrm{eq}}} \left(\frac{p}{n_{\mathrm{i}}}\right)^2 \end{aligned} \tag{35.59}$$

for acceptors and

$$\begin{aligned} C_{\mathrm{MX}^-} &= \eta_{\mathrm{MX}^-} C_{M_s^+} \frac{C_{\mathrm{X}}}{C_{\mathrm{X}}^{\mathrm{eq}}} \left(\frac{n}{n_{\mathrm{i}}}\right)^2; \; C_{\mathrm{MX}^0} = \eta_{\mathrm{MX}^0} C_{M_s^+} \frac{C_{\mathrm{X}}}{C_{\mathrm{X}}^{\mathrm{eq}}} \frac{n}{n_{\mathrm{i}}}; \\ C_{\mathrm{MX}^+} &= \eta_{\mathrm{MX}^+} C_{M_s^+} \frac{C_{\mathrm{X}}}{C_{\mathrm{X}}^{\mathrm{eq}}} \end{aligned} \tag{35.60}$$

for donors. Therein, the $\eta_{\mathrm{MX}^{-/0/+}}$ stand for the temperature-dependent relative concentrations of pairs under intrinsic conditions ($n = p = n_{\mathrm{i}}$) with the respective point defects being in equilibrium ($C_X = C_{\mathrm{X}}^{\mathrm{eq}}$).

It should be noted that all the pair concentrations are proportional to the concentration of the substitutional atoms. In systems not too far from equilibrium, the concentrations of the pairs are expected to make up only a small fraction of the total concentration. As long as the concentrations of pairs remain small in comparison to the total dopant concentration, they will increase linearly with the respective point-defect concentration. In situations far from equilibrium, the formation of pairs will lead to a reduction of the substitutional concentration and consequently to a sublinear increase of the concentration of the dominating pair with the respective point defect concentration. In the limiting case, the redistribution of the dopants atoms takes place in the form of the dominating pairs with the respective diffusion coefficient.

In many important cases, the concentrations of pairs can be safely ignored. Then, the concentration of substitutional dopant atoms C_{M_s} in (35.59) and (35.60) can be replaced by the total dopant concentration C_M. Adding the continuity equations leads to the diffusion equation

$$\begin{aligned} \tfrac{\partial C_{\mathrm{M}}}{\partial t} = \operatorname{div}\Big(& D_{\mathrm{MI}} \operatorname{grad}\left(C_{\mathrm{M}} \tfrac{C_{\mathrm{I}}}{C_{\mathrm{I}}^{\mathrm{eq}}}\right) + D_{\mathrm{MV}} \operatorname{grad}\left(C_{\mathrm{M}} \tfrac{C_{\mathrm{V}}}{C_{\mathrm{V}}^{\mathrm{eq}}}\right) \\ & - z_{\mathrm{M}} \left(D_{\mathrm{MI}} \tfrac{C_{\mathrm{I}}}{C_{\mathrm{I}}^{\mathrm{eq}}} + D_{\mathrm{MV}} \tfrac{C_{\mathrm{V}}}{C_{\mathrm{V}}^{\mathrm{eq}}}\right) C_{\mathrm{M}} \operatorname{grad}\left(\tfrac{\psi}{U_{\mathrm{T}}}\right)\Big) \end{aligned} \tag{35.61}$$

with the diffusion coefficients D_{MX} given by

$$D_{\mathrm{MX}} = \eta_{\mathrm{MX}^-} D_{\mathrm{MX}^-} + \frac{\eta_{\mathrm{MX}^0} D_{\mathrm{MX}^0} p}{n_{\mathrm{i}}} + \eta_{\mathrm{MX}^+} D_{\mathrm{MX}^+} \left(\frac{p}{n_{\mathrm{i}}}\right)^2 \tag{35.62}$$

for pairs with acceptors and

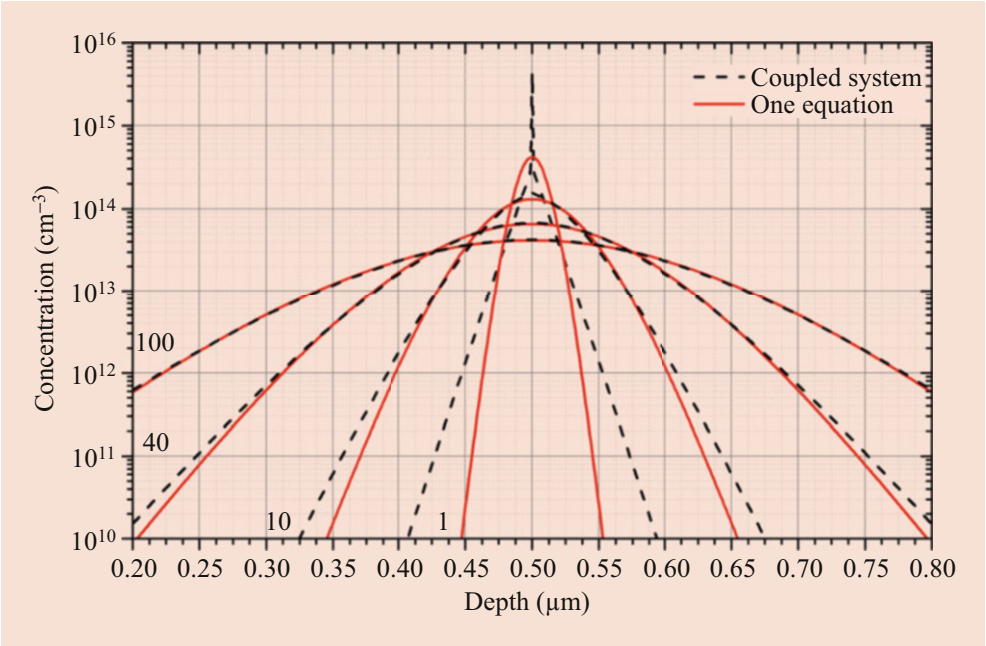

Fig. 35.8 Diffusion of impurities from an initially delta-doped layer, simulated by diffusion equations for mobile species and substitutional species and under the assumption of local equilibrium between these species. The running index is the diffusion time in multiples of the time constant τ. (After [5])

$$D_{\mathrm{MX}} = \eta_{\mathrm{MX}^-} D_{\mathrm{MX}^-} \left(\frac{n}{n_\mathrm{i}}\right)^2 + \eta_{\mathrm{MX}^0} D_{\mathrm{MX}^0} \frac{n}{n_\mathrm{i}} + \eta_{\mathrm{MX}^+} D_{\mathrm{MX}^+} \tag{35.63}$$

for pairs with donors. For both, the dependence of the diffusion coefficient on the Fermi level reflects the increase of the concentration of pairs in extrinsically doped semiconductors.

As long as the semiconductor is intrinsically doped, with vacancy and self-interstitial concentrations at equilibrium, and negligible strain effects, the respective diffusion coefficients of the dopants depend just on temperature. This "intrinsic diffusion coefficient" $D_0 = D_{\mathrm{MI}} + D_{\mathrm{MV}}$ shown in Fig. 35.9 for the main dopants in silicon and germanium is probably the best-studied property of dopants in semiconductors. An exception is boron in germanium for which only three experimental determinations are available which resulted in values which are orders of magnitude apart [55]. Comparing the other dopants for silicon and germanium, it is also noticeable that the fastest and slowest diffusers exchange places.

A further important property of dopants is the degree to which they diffuse via self-interstitials and vacancies. This is typically expressed in terms of the fractional diffusivity via self-interstitials:

$$f_\mathrm{I} = \frac{D_{\mathrm{MI}}}{D_{\mathrm{MI}} + D_{\mathrm{MV}}}. \tag{35.64}$$

The degree to which dopant atoms diffuse via vacancies and interstitial atoms was a subject of sharp discussions after Seeger and Chik [47] introduced the interstitialcy mechanism which lasted well after the review of Fahey et al. The current understanding of dopant diffusion in silicon was developed on the basis of diffusion studies in which some dopant atoms show enhanced diffusion, while the diffusion of others is retarded. Such studies, discussed in more detail in Sect. 35.3.5, in combination with information about the growth of extrinsic stacking faults led to the conclusion that boron and aluminum diffuse in silicon nearly exclusively via self-interstitials, while antimony has been found to diffuse nearly exclusively via vacancies. Arsenic in silicon diffuses via both, and phosphorus diffuses at low concentrations nearly exclusively via self-interstitials while at high concentrations a dominant diffusion via vacancies has been found. In germanium, all elements except boron were suggested to diffuse via a vacancy mechanism. For boron, the considerably lower diffusion coefficient in comparison to the other dopants is sometimes associated with an interstitial diffusion although no unambiguous experimental evidence is available.

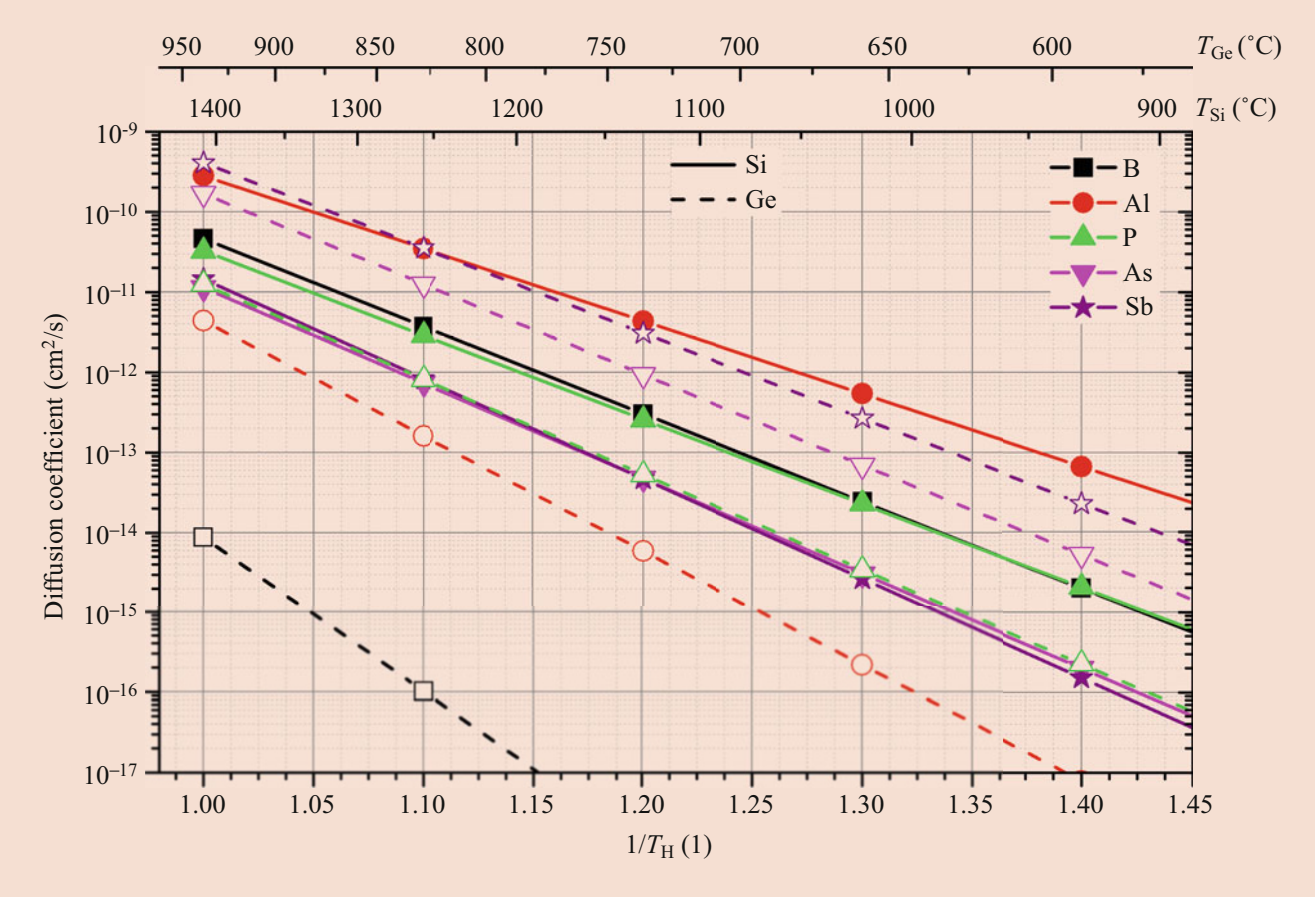

Fig. 35.9 Intrinsic diffusion coefficients of dopants in germanium and silicon as a function of the inverse homologous temperature. (The data are from [5] and [41] for silicon and germanium, respectively)

35.3.4 Dopant Diffusion at High Concentrations

Particularly for contact areas, the active doping concentration cannot be high enough. For such conditions, the charge carrier concentrations exceed the concentration n_i by far. The effects of such high doping levels on dopant diffusion will be discussed briefly in this subsection on the basis of an experiment reported by Orr Arienzo et al. [56] in which a highly doped polysilicon layer maintained a constant concentration of boron during the diffusion at 950 °C for 1 h.

The first simulation result shown in Fig. 35.10, denoted "Intrinsic diffusion," was obtained under the assumption of intrinsic diffusion with a constant diffusion coefficient. The resulting error function profile apparently underestimates the dopant penetration by far.

The second simulation result, denoted "+ Field effect," takes into account that the extrinsic doping concentration results in an electric field E which acts via (35.44) as an additional driving force for dopant redistribution. This manifests itself, as shown, e.g., by Smits [57], in an effective diffusion coefficient which depends via

$$D = D_0 \left(1 + \frac{C}{\sqrt{C^2 + 4n_i^2}} \right) \tag{35.65}$$

on the dopant concentration. However, the enhancement by a factor of two for $C \gg n_i$ remains too small to explain the experimental profile.

Considering also that boron diffuses predominantly via neutral pairs with self-interstitials, i.e., with an effective diffusion coefficient (35.62) which increases linearly with the hole concentration, one obtains the profile denoted "$D(p)$" in Fig. 35.10 under the assumption that the intrinsic point defects remain in equilibrium. In comparison to the previous simulations, the concentration-dependent diffusion coefficient results in pronounced platykurtic profiles which are flatter at the top but steeper at the flanks. Assuming an effective diffusion coefficient which increases quadratically with the respective charge carrier concentration would lead to a deeper penetration of the dopants but also to even steeper flanks.

To reproduce the gentler slope of the experimental profile as in the profile denoted "Full model," one has to take the

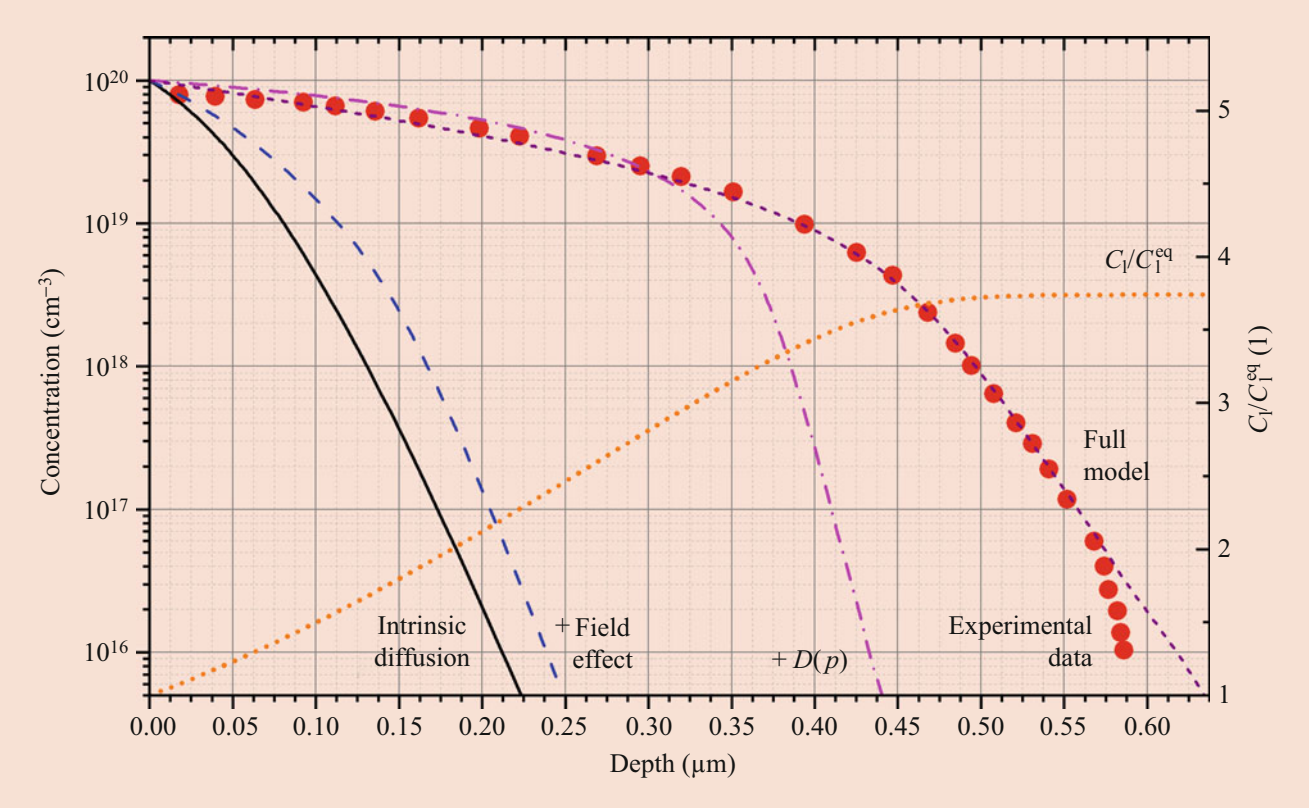

Fig. 35.10 Simulation of the diffusion of boron at high concentrations. (Courtesy C. Ortiz, Fraunhofer IISB) and comparison to the experiment of Orr Arienzo et al. [56] at 950 °C. After [5])

full interaction between boron atoms and self-interstitials into account: Boron-self-interstitial pairs form via (35.48) predominantly close to the interface to the polysilicon layer where the boron concentration is highest. When diffusing into the bulk, the boron concentration reduces, and the pairs are more and more likely to dissociate into substitutional boron and self-interstitials. This results, as shown by the line "C_I/C_I^{eq}" in Fig. 35.10, in an oversaturation of self-interstitials which increases with depth. There, the increase of the self-interstitial concentration compensates for the decrease of the effective diffusion coefficient with the charge carrier concentration so that the resulting doping profile becomes nearly error-function-like but with a much higher effective diffusion coefficient than in the case of intrinsic diffusion. Following their gradient, the self-interstitials will diffuse back to the surface so that their oversaturation depends on the interplay of transport into the bulk via dopant diffusion and transport back to the surface by self-diffusion. While the effect is rather unspectacular for boron, it is responsible also for the formation of pronounced kink and tail features in high-concentration phosphorus profiles and the broadening of the base region of bipolar transistors in areas below high-concentration phosphorus profiles, the so-called emitter-push effect [58].

At even higher phosphorus background concentrations, Nylandsted Larsen et al. [59] found that the diffusion of a variety of dopants increases steeply with the phosphorus concentration. Following the suggestion of Mathiot and Pfister [60], this was explained in terms of a percolation phenomenon. However, this explanation was discussed controversially, and Ramamoorthy and Pantelides [61], as an example, argued that the rapid diffusion should give rise to fast dopant clustering and the break-up of the percolation cluster.

35.3.5 The Influence of Surface Processes on Dopant Diffusion

First indications for the influence of surface chemical processes on dopant diffusion date back to the 1960s, when the (111)-oriented wafers prevalently used in industry were replaced by (100)-oriented wafers. Comparative diffusion studies at that time indicated an orientation-dependence of the diffusion of dopants which would not be expected for semiconductors with a diamond lattice. However, some researchers reported already then that such effects would be seen only for diffusion process in oxidizing ambient and not in inert ambient [62]. Later studies confirmed the oxidation-

enhanced diffusion of boron [63] and phosphorus [64] during dry oxidation of (100)-oriented silicon, while at the same time an oxidation-retarded diffusion of antimony was found [65]. Based on the observation of the concurrent growth of stacking faults identified unambiguously as self-interstitial agglomerates, it was suggested by Dobson [66] and Hu [67] that overstoichiometric silicon atoms are incorporated during the oxidation into the growing oxide layer and that these silicon atoms may segregate as self-interstitials into the silicon where they increase the concentration of self-interstitials beyond their equilibrium concentration. Because of bulk recombination of self-interstitials and vacancies (35.49), an oversaturation of the former ($C_\mathrm{I}/C_\mathrm{I}^\mathrm{eq} > 1$) will inevitably lead to an undersaturation of the latter ($C_\mathrm{V}/C_\mathrm{V}^\mathrm{eq} < 1$) and vice versa. The resulting effective diffusion coefficient under non-equilibrium conditions

$$D^\mathrm{eff} = D^\mathrm{eq}\left(f_\mathrm{I}\frac{C_\mathrm{I}}{C_\mathrm{I}^\mathrm{eq}} + (1-f_\mathrm{I})\frac{C_\mathrm{V}}{C_\mathrm{V}^\mathrm{eq}}\right) \tag{35.66}$$

will be higher than the diffusion coefficient D^eq under equilibrium conditions ($C_\mathrm{I} = C_\mathrm{I}^\mathrm{eq}$, $C_\mathrm{V} = C_\mathrm{V}^\mathrm{eq}$) for dopants diffusing preferentially via self-interstitials ($f_\mathrm{I} > 0.5$). Dopants diffusing preferentially via vacancies ($f_\mathrm{I} < 0.5$), on the other hand, may be retarded in their redistribution. In process simulation programs, the injection of self-interstitials is usually modeled empirically as a flux of self-interstitials which increases sublinearly with the oxidation rate.

While the dry oxidation of (100)-oriented silicon was always found to result in an enhanced self-interstitial concentration, opposite effects were found for the diffusion of (111)-oriented samples at high temperatures and long diffusion times. This was explained by Taniguchi et al. [68] by a preferential segregation of self-interstitials into the growing oxide for small oxidation rates.

More problematic to explain was the retarded diffusion of boron and phosphorus, the enhanced diffusion of antimony, and the shrinkage of self-interstitial agglomerates reported by Mizuo et al. [69] during the nitridation of silicon. Interpreted in terms of (35.66), the nitridation-enhanced diffusion of antimony indicated an injection of vacancies. However, kinetic models in analogy to those for the injection of self-interstitials during oxidation had the problem that the growth of surface nitrides almost stopped after a short time, while the effects on dopant diffusion and stacking-fault growth lasted for much longer. In addition, it was shown by Ahn et al. [70] that similar effects can be observed below deposited nitrides. An explanation for these phenomena was finally suggested by Cowern [71] who noted that the work done against overlayers has to be taken into account in the formulation of the formation energies of the intrinsic point defects.

Finally, it should be noted that also other surface chemical processes like the nitridation of oxide layers or the formation of silicides were reported to lead to non-equilibrium diffusion effects.

35.3.6 Transient Diffusion Effects During Post-Implantation Annealing

Because of its superior homogeneity and dose control, ion implantation has become the main process for the doping of semiconductors. Inevitably associated with ion implantation is the creation of damage due to elastic collisions of the impinging atoms with the lattice atoms. Depending on the mass and energy of the implanted atoms, some ten to many hundred self-interstitials and vacancies are generated per implanted atom. For high enough doses, an amorphous layer is formed in the semiconductor. To remove the damage, semiconductors need to be annealed after ion implantation. With all the intrinsic point defects being far from equilibrium, such annealings result in significant implantation-enhanced diffusion of the dopants.

To illustrate typical effects during post-implantation annealing, simulations of a 20 keV boron implantation with a dose of 5×10^{15} cm^{-2} and subsequent isothermal annealings at 900 °C are shown in Fig. 35.11. During the first 10 to 40 s, significant diffusion is observed in the tail of the boron profile. During this time interval, diffusive broadening is limited to concentrations up to about 1×10^{19} cm^{-3}. This value corresponds to the concentration of electrically active, i.e., substitutional boron atoms, which remains nearly the same. Increasing the annealing time to 1 min results already in a much smaller broadening, and increasing the time further to 10 min has an even much smaller effect. In contrast, a significant increase of the electrically active boron concentration is observed. Because of their eminent technological importance, transient diffusion and transient activation have been main research topics for decades. For the sake of brevity, we can only present the most important results here and must refer the interested reader to some more extensive reviews in this area [73, 74].

While it was clear already at an early stage that implantation damage was the cause of the implantation-enhanced diffusion, the exact mechanism was not as clear for some time. The consensus today is that the implantation leads to an excess of self-interstitials in the crystal which agglomerate during annealing and undergo Ostwald ripening. The oversaturation which drives dopant diffusion results from the cloud of self-interstitials that the extended defects maintain in their vicinity [75]. Quantitative information about the extended defects could be obtained by numerous TEM (transmission electron microscopy) studies with the work of Eaglesham et al. [76] and Bonafos et al. [77] just to give some prominent examples. Complementary information about the energetics of self-interstitial clusters which are too small to be investi-

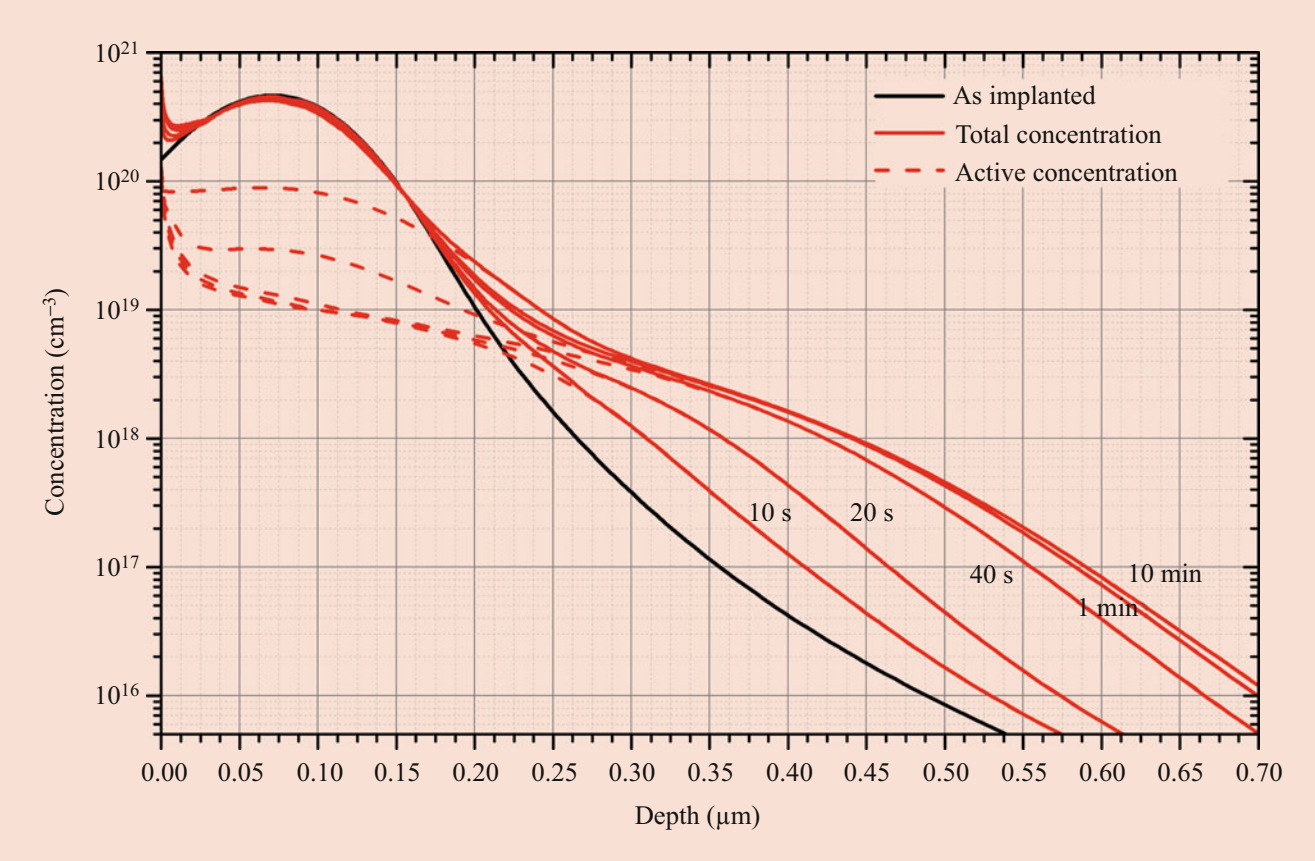

Fig. 35.11 Boron profiles after implantation with 20 keV and 5×10^{15} cm^{-2} and annealing at 900 °C simulated with Sentaurus Process [72]

gated by TEM became available by the experiment of Cowern et al. [78] in which the implantation-enhanced diffusion of narrow boron layers was induced by silicon implants. For a comprehensive review of the Ostwald ripening of extended defects, the review article of Claverie et al. [79] can be recommended. Among the many models suggested to capture the main aspects of the Ostwald ripening of small silicon clusters and extended {311} defects, the one of Zechner et al. [80] is particularly frequently used in process simulation since it combines predictive power with a minimum number of equations to be solved. For longer annealing times for which the {311} defects transform into stacking faults and perfect dislocation loops, extensions have been suggested by Zographos et al. [81] and Wolf et al. [82].

As initial conditions for the abovementioned models, the relevant concentration of self-interstitials needs to be calculated. This can, in principle, be done by the Monte Carlo techniques discussed in Sect. 35.2.2. However, the concentration of defects obtained would be far too high since vacancies and self-interstitials are created in pairs during the collisions with the impinging atoms and are likely to recombine early in the annealing stage. Accordingly, Giles [83] suggested for sub-amorphizing implants that only the extra atom introduced by the implantation needs to be taken into account as self-interstitial. While this assumption works well, e.g., for boron, it was found by Pelaz et al. [84] that the number of self-interstitials per implanted atom needs to be increased for heavier ions. Finally, for amorphizing implants, the amorphized region will regrow defect-free already at low temperatures like during the ramping stage of annealing. Accordingly, only the excess of self-interstitials in depths beyond the amorphous/crystalline interface needs to be taken into account and can be calculated by Monte Carlo simulations or by assuming an effective plus factor as for non-amorphizing implants [85].

35.3.7 Electrical Activation, Clusters, and Solid Solubility

One of the phenomena apparent from Fig. 35.11 is that a significant part of the atoms are immobile as well as electrically inactive. To explain such phenomena for arsenic in silicon, small electrically neutral clusters of two [86] and four arsenic atoms [87] were assumed to form. While the formation of such clusters can be described by binary reactions or chains of binary reactions, clusters Cl^n comprising n dopant atoms are usually assumed to form by the reaction

$$n\,M_s \underset{k_{Cl\leftarrow}}{\overset{k_{Cl\rightarrow}}{\rightleftharpoons}} Cl^n \tag{35.67}$$

which results in an additional continuity equation

$$\frac{\partial C_{Cl^n}}{\partial t} = k_{Cl\rightarrow}\left(C_{M_s}\right)^n - k_{Cl\leftarrow}C_{Cl^n} \tag{35.68}$$

for the clusters. Because of mass conservation, the right-hand term multiplied by n also appears in the continuity equation of the substitutional impurities. Since the total concentration of impurities C_M includes now also the atoms in the cluster, adding all contributions leads again to an equation similar to (35.61) but with the substitutional concentration C_{M_s} instead of the total concentration C_M in the term on the right hand side. The substitutional concentration can now be considerably smaller than the total concentration, which leads already to a significant retardation of the diffusion of the impurities. In addition, the clustering also reduces the charge-carrier concentration in the high-concentration regions and thus also the effective diffusivity (35.62) of the non-clustered dopant atoms.

Coming back to the post-implantation annealing of boron shown in Fig. 35.11, it is noticeable that the electrical active concentration remains virtually the same during the period of transient-enhanced diffusion, while it increases significantly thereafter. This indicates an involvement of self-interstitials in the formation of the complexes responsible. Accordingly, for the latter, the term boron-interstitial clusters (BICs) was introduced in literature. Based on ab initio calculations, schemes of binary reactions of substitutional boron atoms and BICs with boron interstitial atoms and self-interstitials were developed (see, e.g., [88]) and shown to be able to capture the main features of transient boron diffusion and activation. For arsenic and phosphorus, the reaction schemes were even extended toward mixed clusters involving self-interstitials or vacancies [89].

Particularly by ion implantation, the total concentrations of dopants can be increased almost unlimitedly. However, when a certain total impurity concentration, known as solid solubility, is exceeded, an impurity-rich phase is expected to form in equilibrium. Depending on the impurity and temperature, the impurity-rich phase may be a liquid, a pure impurity phase, or a silicide phase [90]. Dynamically, such a phase can form by spinodal decomposition or, often more likely, by nucleation and growth of precipitates. Since the latter process is kinetically limited, dopant precipitates are often observed only after annealing processes with high thermal budgets [91]. However, dopant precipitates are not only observed after ion implantation. During growth and annealing of phosphosilicate glasses, as a prominent example, so many phosphorus atoms segregate into the silicon that the (binary) solid solubility of phosphorus in silicon is exceeded there and SiP precipitates form [92].

35.3.8 Segregation

In real applications, semiconductors will always be in contact to other materials like silicon dioxide, silicides, or metals. During annealing processes, the atoms being present in either material will diffuse not only therein but also across the interfaces between the materials. In equilibrium, because of their different formation energies, discontinuous distributions of the atoms are expected at the interfaces. An example in this sense already mentioned above is the formation of large SiP precipitates in silicon where the phosphorus concentration is 50 at.% in the SiP, while the total concentration in silicon corresponds largely to the temperature-dependent solid solubility. At the interfaces, the discontinuous distributions of atoms in equilibrium are characterized by the segregation coefficients m as ratios of the respective concentrations at the two sides. During thermal processing, the flux of species between the phases A and B is usually written in form of a first-order kinetic model

$$J_X = h\left(C_X^A - mC_X^B\right) \tag{35.69}$$

as being proportional to the interface transport coefficient h and the difference in concentration normalized by the segregation coefficient.

Segregation of dopants from highly doped phosphosilicate or borosilicate glasses into silicon is used in solar and power electronics for the doping of silicon with concentrations which may be even above solid solubility. At lower concentrations, diffusion of dopants in silicon dioxide is rather slow so that segregation effects can be observed only when the interface moves during an oxidation process. During such processes, phosphorus, arsenic, and antimony pile up at the silicon side, while boron segregates preferentially into the growing oxide.

Pile-up of donors was observed also at stationary interfaces between silicon and silicon dioxide. Dedicated investigations showed that this pile-up occurs for phosphorus [93] and arsenic [94, 95] within few nm from the interface on the silicon side even if the dopants in the area below are homogeneously distributed. In contrast, a similar pile-up of boron was shown to result rather from large self-interstitial gradients toward the interface during post-implantation annealing [96]. In continuum simulators, interface segregation of phosphorus and arsenic is usually included via an approach suggested by Lau, Orlowski, and coworkers [97, 98]. It assumes that dopants adsorb and desorb from both materials to energetically favorable sites at the interface.

35.3.9 Simulation Methodologies

The dawn of numeric diffusion simulation began around 1980 with programs like SUPREM [6, 7] and ICECREM [8], when diffusion theories were already too complicated to be solved analytically. These programs like their two- and three-dimensional successors were based on a discretization of the diffusion-reaction equations discussed above. A big advantage of such continuum approaches is that the mesh used for discretization of the equations can be adjusted to the problem, i.e., made fine where necessary, while it can be left coarse elsewhere. A second potential advantage is that empirical models like the clustering Eq. (35.67) or the self-interstitial-complex ripening models mentioned in Sect. 35.3.6 can be implemented easily to reduce parameters and equations to be solved. On the other hand, there is an over-linear increase of computer resources and simulation time associated with an increase of the number of equations to be solved. Due to their excellent prediction accuracy and robustness for a wide range of applications from nanoelectronics to power electronics, continuum models are currently the workhorses of TCAD simulations in industry.

As an alternative, atomistic simulators like DADOS [99] were introduced at the end of the 1990s. These programs consider directly the diffusive jumps of non-lattice atoms and defects as well as the reactions among them by a kinetic Monte Carlo (KMC) algorithm. The big advantage of KMC simulators is that a plethora of different defects and defect reactions can be taken into account with a linear increase of computational efforts only. On the other hand, all non-lattice atoms and defects must be taken along in the simulations which make them feasible only for comparatively small volumes. However, with the continuing miniaturization of devices, this is becoming all the easier.

To simulate crystal-orientation-dependent phenomena like faceting during epitaxial deposition or shape changes during laser annealing, both continuum and KMC approaches lack predictive power. For such effects, it is necessary to include the host atoms in the calculations as in lattice kinetic Monte Carlo (LKMC) schemes [100]. However, it should be noted that classical LKMC implementations lack the ability to simulate other defects apart from vacancies and substitutional impurities.

35.4 Simulation of Oxidation

For many years, the simulation of oxidation was both a very important and a very difficult part of process simulation: Local oxidation ("LOCOS") was indispensable to generate three-dimensional structures for electrical isolation. It led to transition domains between the thin gate oxide and the isolation oxide, as shown in Fig. 35.12. The basic effect is

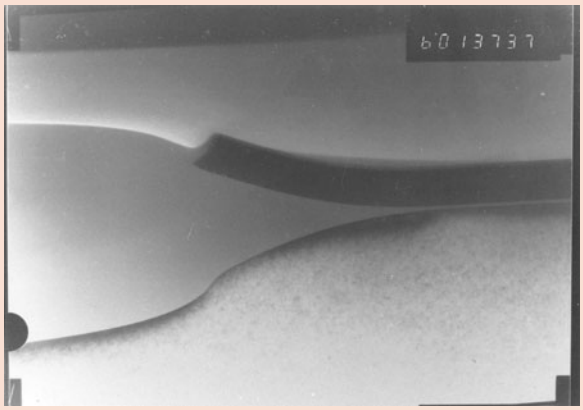

Fig. 35.12 SEM micrograph of transition domain ("bird's beak") between thick field oxide and thin gate oxide. Technology from the 1980s, with gate oxide thickness of about 100 nm

that during oxidation 2.27 volumes of oxide are generated from one volume of silicon. For local oxidation as shown in Fig. 35.12, the excess volume of oxide generated leads to a flux of oxide and the need to solve the resulting mechanical problem.

Simulation of oxidation includes simultaneously the diffusion of dopants and defects in the bulk semiconductor and in the (growing) oxide, the mechanics of the oxide flux, and the transport of dopant atoms across the moving interface between the semiconductor and the oxide, which in many cases critically affected the total amount of dopants near the channel, and in turn even top electrical parameters like the threshold voltage. In turn, the generation and adaptation of meshes to properly resolve the transport of dopants across moving interfaces was a key problem for three-dimensional process simulation.

For current nanoelectronic devices, the simulation of oxidation is far less important, because advanced device architectures do not include LOCOS oxidation, but merely thin oxides. Shallow trench oxidation is performed by growth of a thin oxide followed by oxide deposition. However, for applications like power electronics, thicker oxides are still needed, and the three-dimensional simulation of oxidation stays important for such cases.

35.4.1 One-Dimensional Simulation of Oxidation

The basic physical processes to be included in the one-dimensional simulation of oxidation are shown in Fig. 35.13. They are all fast compared with the oxide growth and can therefore be considered as stationary. At the interface between oxide and silicon, the oxidizing species O_2 in case of

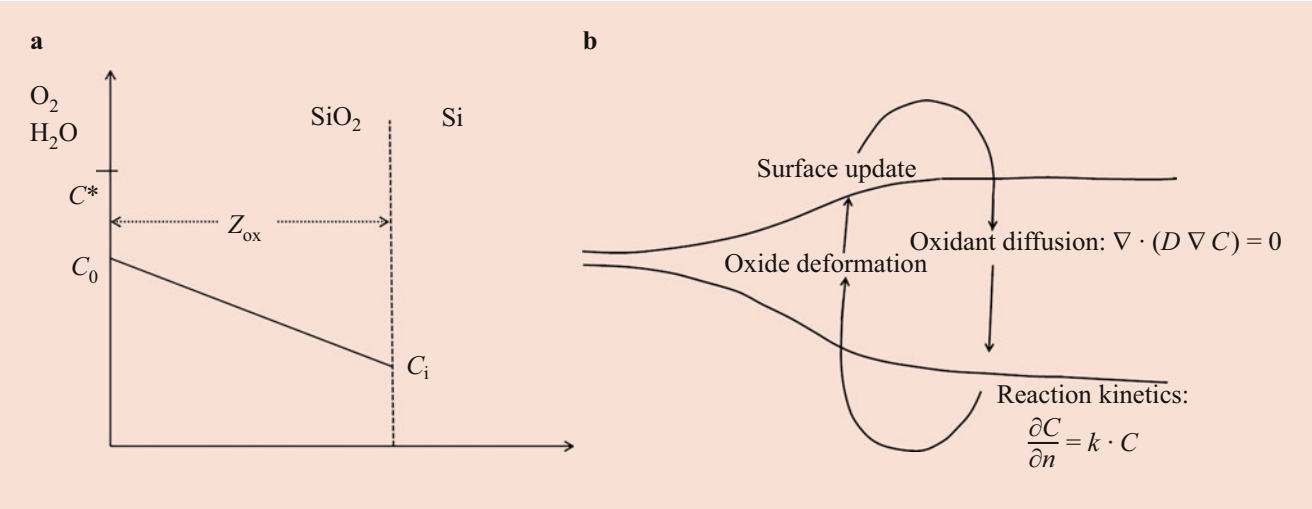

Fig. 35.13 Physical processes involved in the oxidation of silicon. (**a**) One-dimensional case (planar oxidation); (**b**) Two−/three-dimensional case as discussed in Sect. 35.4.2

dry oxidation and H_2O in case of wet oxidation react with silicon according to

$$\mathrm{Si} + \mathrm{O_2} \rightarrow \mathrm{SiO_2} \tag{35.70}$$

$$\mathrm{Si} + 2\,\mathrm{H_2O} \rightarrow \mathrm{SiO_2} + 2\,\mathrm{H_2} \tag{35.71}$$

The corresponding Deal-Grove model [101] consists of three steps, which can all be expressed as fluxes F of the oxidizing species. These species are first adsorbed at the oxide surface, resulting in a concentration C^*, which depends on the partial pressure of the oxidizing ambient (O_2 or H_2O). A parameter h describes the transfer of the species across the surface, giving rise to the concentration C_0 at the oxide side of the surface:

$$F = h \cdot \left(C^* - C_0\right) \tag{35.72}$$

Stationary diffusion with a diffusion coefficient D leads to a concentration C_i of the oxidizing species at the oxide side of the interface to silicon:

$$F = D \cdot \frac{(C_0 - C_\mathrm{i})}{z_\mathrm{ox}} \tag{35.73}$$

A constant k describes the first-order reaction of the oxidizing species at the interface between oxide and silicon:

$$F = k \cdot C_\mathrm{i} \tag{35.74}$$

Since the three fluxes in Eqs. (35.72), (35.73), and (35.74) are equal, a differential equation for the oxide thickness z_ox results [101]:

$$\frac{\mathrm{d}z_\mathrm{ox}}{\mathrm{d}t} = \frac{{kC^*}/{N}}{1 + \frac{k}{h} + k \cdot {z_\mathrm{ox}}/{D}} \tag{35.75}$$

Here, N is the density of the atoms in the silicon crystal. The solution of Eq. (35.75) is the well-known linear-parabolic relationship for the time dependence of the oxide thickness:

$$\frac{{z_\mathrm{ox}}^2}{k_\mathrm{p}} + \frac{z_\mathrm{ox}}{k_\mathrm{l}} = t + t_0 \tag{35.76}$$

Here, k_p and k_l are the parabolic and the linear oxide growth coefficients. They relate to the physical parameters given above according to

$$k_\mathrm{l} = \frac{C^*}{N\left(\frac{1}{k} + \frac{1}{h}\right)} \tag{35.77}$$

$$k_\mathrm{p} = 2D \cdot {C^*}/{N} \tag{35.78}$$

The linear regime applies for small oxide thicknesses z_ox and is determined by the transfer of the oxidant across the oxide surface and the reaction at the interface between oxide and silicon, expressed by the parameters k and h. For larger oxide thickness, the transport through the existing oxide layer limits the process, resulting in a growth asymptotically

approaching the square root of the oxidation time. The initial time t_0 is used to express the native oxide which is grown almost instantaneously. An increase of the initial oxidation rate can be described by Massoud's model [102], which adds an exponential term to Eq. (35.75):

$$\frac{\mathrm{d}z_{\mathrm{ox}}}{\mathrm{d}t} = \frac{kC^* \Big/ N}{1 + \frac{k}{h} + k \cdot z_{\mathrm{ox}} \Big/ D} + C\,\mathrm{e}^{\left(-\frac{z_{\mathrm{ox}}}{L}\right)} \tag{35.79}$$

In this case the oxide thickness is no more given in the analytical form of Eq. (35.76), but must be calculated as solution of the differential Eq. (35.79).

In Eqs. (35.75), (35.76), (35.77), (35.78), and (35.79), the physical parameters D, k, h, C, and L depend in various respects on the process to be simulated, including temperature, the orientation of the silicon crystal, the oxidizing species (O_2 or H_2O) and its partial pressure, additional HCl in the atmosphere, the dopant concentration on the silicon side of the interface between silicon and oxide, and stress.

35.4.2 Multidimensional Simulation of Oxidation

The one-dimensional oxidation model summarized above describes the situation where a homogeneous oxide layer is grown on a flat silicon surface. This does no more apply in areas where the silicon is structured (e.g., a trench) or partly masked. This situation is visualized in two dimensions in Fig. 35.13b. In this case, Eqs. (35.72), (35.73), and (35.74) are replaced by a stationary partial differential equation and the corresponding boundary conditions for the concentration C of the oxidizing species, depending on space and time. Here, $\frac{\partial}{\partial n}$ is the derivative in direction normal to the surface or interface:

$$\nabla\,(D \cdot \nabla C) = 0 \text{ in the oxide;} \tag{35.80}$$

$$D \cdot \frac{\partial C}{\partial n} = h \cdot \left(C^* - C\right) \text{ at the oxide surface;} \tag{35.81}$$

$$D \cdot \frac{\partial C}{\partial n} = k \cdot C \text{ at the interface between oxide and silicon.} \tag{35.82}$$

The dependence of the physical constants D, h, and k on the process to be simulated is in principle similar to the one-dimensional case. However, for non-planar or masked structures, the stress-dependent flux of the oxide must be simulated, which results from the generation of 2.27 volumes of oxide from one volume of silicon. In addition to the standard Arrhenius dependence on the temperature, this leads to

$$D = D_0 \cdot \exp\left(-\frac{E_{\mathrm{D}}}{kT}\right) \cdot \exp\left(-\frac{p \cdot V_{\mathrm{D}}}{kT}\right); \tag{35.83}$$

$$C^* = C_0 \cdot \exp\left(-\frac{E_{\mathrm{C}}}{kT}\right) \cdot \exp\left(-\frac{p \cdot V_{\mathrm{C}}}{kT}\right); \tag{35.84}$$

$$k = k_0 \cdot \exp\left(-\frac{E_{\mathrm{k}}}{kT}\right) \cdot \exp\left(\frac{\sigma_{\mathrm{nn}} \cdot V_{\mathrm{k}}}{kT}\right); \tag{35.85}$$

$$\eta = \eta_0 \cdot \exp\left(-\frac{E_\eta}{kT}\right) \cdot \exp\left(p \cdot \alpha(T)\right) \tag{35.86}$$

where the symbols have partly been adapted from the literature [103]. Here, E_{d}, E_{C}, E_k, and E_η are the activation energies in the respective Arrhenius laws, with k the Boltzmann constant. p is the hydrostatic pressure and σ_{nn} the normal stress at the interface between oxide and silicon, counted as positive if the oxide executes a pull on the silicon. V_{D}, V_{c}, V_{k}, and V_η (see Eqs. (35.83), (35.84), (35.85), (35.86), and(35.87)) are the activation energies for the stress dependencies of the respective parameters and α a parameter depending on temperature. Whereas according to [103], V_{k} is the difference between the molecular volume of SiO_2 and the atomic volume of Si, and equals to 25 Å^3, the other volumes are fitting parameters. It was shown [104] that for the oxidation of cylindrical structures, Eq. (35.86) leads to an equation for the hydrodynamic pressure p, which has no solution in case of some concave structures. It was therefore suggested to replace Eq. (35.86) by a model proposed by Eyring [105, 106]:

$$\eta = \eta_0 \cdot \exp\left(-\frac{E_\eta}{kT}\right) \cdot \frac{\sigma \Big/ \sigma_c}{\sinh\left(\sigma \Big/ \sigma_c\right)}, \text{ with } \sigma_c = 2kT \Big/ V_\eta \tag{35.87}$$

35.4.3 Multidimensional Simulation of Stress-Dependent Oxidation

Besides the specific physical models for the diffusion and reaction of the oxidizing species also the mechanical problem resulting from the generation of 2.27 volumes of oxide from

one volume of silicon must be solved numerically. In general, this needs the simulation of the viscoeleastic oxide flow. For this, the stress $\boldsymbol{\sigma}$ and strain $\boldsymbol{\varepsilon}$ must be considered. They are given by tensors (here displayed as six-dimensional vectors), and the hydrodynamic pressure p relates to them as follows:

$$\boldsymbol{\sigma} = \left(\sigma_x, \sigma_y, \sigma_z, \tau_{xy}, \tau_{xz}, \tau_{yz}\right) \tag{35.88}$$

$$\boldsymbol{\varepsilon} = \left(\varepsilon_x, \varepsilon_y, \varepsilon_z, \gamma_{xy}, \gamma_{xz}, \gamma_{yz}\right) \tag{35.89}$$

$$P = -\left(\sigma_x + \sigma_y + \sigma_z\right)/3 \tag{35.90}$$

Here, the indices of the first three components give the direction of the stress or strain.

For the shear stresses in last three components of the stress $\boldsymbol{\sigma}$, the first index indicates the normal to the surface to which the shear stress is applied, and the second index gives the direction of the shear stress. In this nomenclature one could also use σ_{xx} instead of σ_x, etc. The stain components give the changes of the shifts u, v, and w in directions x, y, and z:

$$\varepsilon_x = \frac{\partial u}{\partial x};\ \varepsilon_y = \frac{\partial v}{\partial y};\ \varepsilon_y = \frac{\partial w}{\partial y}; \tag{35.91}$$

$$\gamma_{xy} = \frac{\partial u}{\partial y} + \frac{\partial v}{\partial x};\ \gamma_{xz} = \frac{\partial u}{\partial z} + \frac{\partial w}{\partial x};\ \gamma_{yz} = \frac{\partial v}{\partial z} + \frac{\partial w}{\partial y} \tag{35.92}$$

The space available here does not allow for the discussion of the various approaches and approximations used for the simulation of stress in the literature. It is important to note that for temperatures of 960 °C and above, the viscous behavior of the oxide dominates [107] whereas below the oxide increasingly becomes elastic. In the viscous case, the velocity field $\boldsymbol{V}$ of the oxide flow can then be related to the hydrodynamic pressure P via

$$\eta \cdot \Delta \mathbf{V} = \nabla P \tag{35.93}$$

If the oxide is approximated as incompressible, Eq. (35.93) reduces to $\Delta \mathbf{V} = 0$. In that case all stress dependencies given in Eqs. (35.83), (35.84), (35.85), and (35.86) are neglected and only that Laplace equation is used to simulate the flow of the incompressible oxide caused by the extra volume generated during oxidation. This also means that masks are considered as flexible, executing no pressure on the growing oxide.

Figure 35.14 shows a sample oxide structure with the different kinds of interfaces at which boundary conditions for

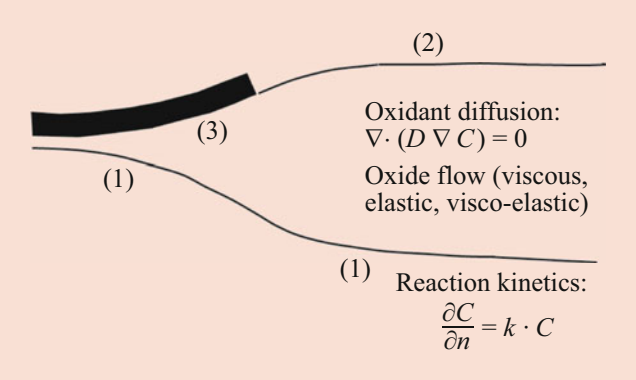

Fig. 35.14 Boundary conditions for multidimensional simulation of oxidation

$\boldsymbol{v}$ and P must be defined: (1) At the interface between oxide and silicon, $\boldsymbol{v}$ is normal to the interface, and its value is given by the rate at which silicon is transformed into oxide (equal to 0.44 times the oxide growth rate); (2) at the oxide surface, P is equal to the ambient pressure minus the surface tension; (3) at the interface between oxide and nitride, P is equal to the mechanical pressure executed by the nitride layer. This needs either mechanical calculations of the nitride bending or the use of suitable analytical approximations. For the then still missing boundary condition for the velocity at the free oxide surface, Chin used an additional relationship provided by an artificial compressibility algorithm [108].

35.5 Lithography Simulation

One of the most important process steps in semiconductor manufacturing is lithography, because it enables the transfer of the chip design onto the silicon wafer. Here, three properties are most important: the capability to generate tiny features (currently, the smallest dense features for single exposure are in the range of 20 nm); to establish the pre-defined links foreseen in the chip design between the transistors and capacitors acting as switches, amplifiers, or storage elements; and moreover to process up to hundreds of billion elements at the same time. Because a separate chapter of this handbook is dedicated to the lithography equipment and technology, below only a few technological aspects are outlined, which are necessary to present lithography simulation in a self-contained section.

35.5.1 Basic Principle of Lithography

Figure 35.15 shows the principle of a projection lithography step. Light from a suitable source illuminates a mask, where it is diffracted at the mask features. The diffracted light is

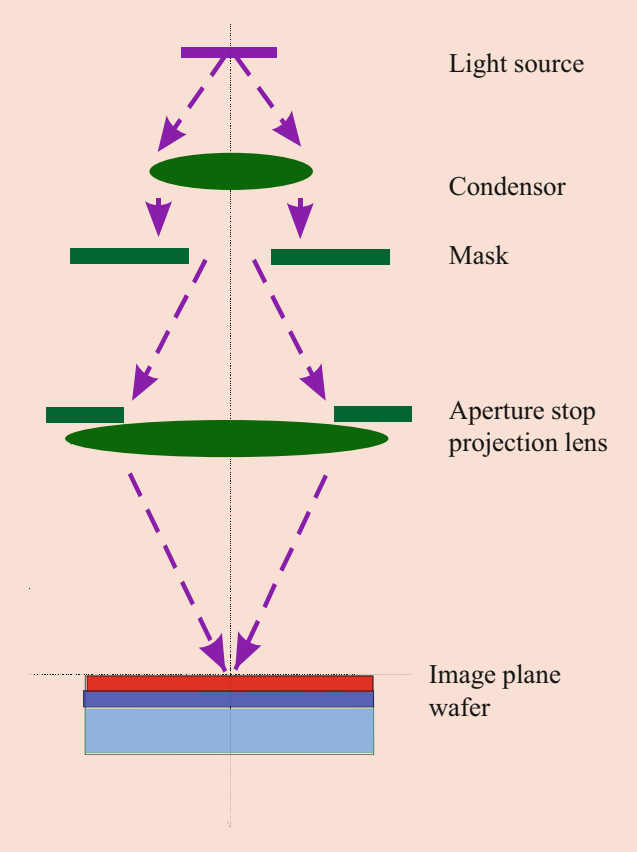

Fig. 35.15 Schematics of imaging in optical lithography

then collected via a suitable optical system and focused onto a photoresist. This part of the lithography process is called imaging and depends both on the mask and the lithography equipment, namely, the light source and the optical system. The resolution of this optical system is then given by the Rayleigh criterion [109].

$$d_{\min} = k_1 \cdot \frac{\lambda}{\mathrm{NA}} \tag{35.94}$$

where $d_{\min}$ is the minimum pitch which can be printed, λ is the wavelength of the light used, NA is the numerical aperture (equal to the relative refractive index of the medium times the sine of the opening angle of the last lens), and k_1 is the so-called technology factor, with a minimum value of 0.5. Because 193 nm is the smallest wavelength of laser light currently used in high-volume semiconductor device manufacturing, for which lenses are sufficiently transparent, the theoretical minimum pitch which can be printed in the so-called "dry" optical lithography (with air as medium between the last lens and the photoresist) is about 104 nm. Smaller pitches can either be printed via so-called multiple patterning lithography [110], with immersion lithography [111] or with extreme ultraviolet (EUV) lithography [112]. In the latter case, soft X-rays at a wavelength of about 13.5 nm are used, which then necessitate the replacement of the lenses in all parts of the optical system by multilayer MoSi mirrors. The projection process transfers an image of the mask patterns into the photoresist, leading to local deposition of energy into the photoresist. The image is diffraction limited, because the lenses cannot collect all diffraction orders from the mask. Furthermore, the image is disturbed by several other effects such as defocus, lens imperfections, or defects on the mask. After resist development parts of the resist which were exposed (positive tone resist) or not exposed (negative tone resist) are chemically modified and in turn (partly) removed. This latter part is influenced by chemistry and diffusion effects in the resist.

35.5.2 Principle of Lithography Simulation

Figure 35.16 illustrates the lithography process and its simulation, which is divided into two steps: First, for the imaging step, the intensity distribution, generated by the projection of the mask through the optical system, inside the photoresist is simulated. Second, the modification of the photoresist caused by the energy deposited during exposure, and governed by chemical reactions, diffusion, and temperature in case of a post-exposure bake process, is simulated. Different to the other process steps described in the other subsections, the imaging step requires simultaneous simulation on equipment, and feature-scale level to calculate from characteristics of the illumination source, the mask, and the optical system used the energy deposition in photoresists on a nanometer scale.

35.5.3 Simulation of Imaging

The physics of projection is well understood and could in principle be fully described by the well-known Maxwell's equations. However, due to the different size dimensions to be simulated during the projection step, different simulation methods derived from the Maxwell's equations must be applied. For example, the projection of the mask can be simulated very accurately with derivatives of the Hopkins's equation [113], whereas the mask diffraction is typically simulated by directly solving the Maxwell's equations either without any simplifications or, depending on the mask area and accuracy to be simulated, by using some derived simplified methods.

One common derivative of the Hopkins' equation is the Abbe approach [111], which basically consists of a Fourier transformation F of the mask transmission, a multiplication with pupil functions P in the Fourier space to describe the transmission behavior of the optical system, and finally an inverse Fourier transformation F^{-1} to simulate the intensity

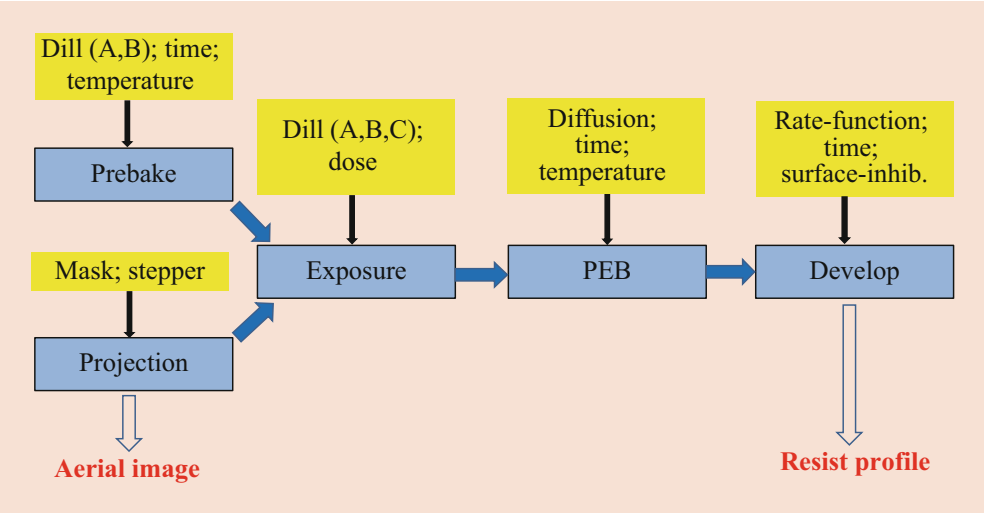

Fig. 35.16 Principle of lithography simulation

distribution in the image plane. This approach is based on the assumptions of an illumination with a single plane wave along the z-axis or with a tilt angle (t_x,t_y), a given complex mask transmission $t(x,y)$, and projection along the z-axis. Spatial frequencies f_x and f_y are introduced, which depend on the diffraction angles Θ_x and Θ_y in x- and y-directions, and the wavelength λ, and are used for the mask diffraction spectrum $s(f_x,f_y)$. In the following formulas, a scalar description not considering polarization is given:

$$f_x = \frac{\sin(\theta_x)}{\lambda}; f_y = \frac{\sin(\Theta_y)}{\lambda} \tag{35.95}$$

$$s(f_x,f_y) = F\{t(x,y)\} = \int t(x,y) \cdot \mathrm{e}^{-i2\pi\pi(f_x \cdot x + f_y \cdot y)} \mathrm{d}x\,\mathrm{d}y \tag{35.96}$$

For illumination with the tilt angle (τ_x,τ_y), the mask diffraction spectrum is shifted accordingly:

$$s(f_x,f_y) \to s\left(f_x - \frac{\sin\tau_x}{\lambda}, f_y - \frac{\sin\tau_y}{\lambda}\right) \tag{35.97}$$

The pupil function $P(f_x,f_y)$ expresses within the numerical aperture NA, for example, focus and aberrations, and is zero outside:

$$P(f_x,f_y) = 0 \text{ for } \sqrt{\sin^2\theta_x + \sin^2\theta_y} > \mathrm{NA} \tag{35.98}$$

The complex amplitude a_P of the light in the image plane resulting from a single source point P is then given by the inverse Fourier transformation of the pupil function times the diffraction spectrum, where the tilt is considered in the pupil function P:

$$a_P(x,y) = F^{-1}\left\{P\left(f_x - \frac{\sin\tau_x}{\lambda}, f_y - \frac{\sin\tau_y}{\lambda}\right) \cdot F\{t(x,y)\}\right\} \tag{35.99}$$

Alternatively, the tilt could also be considered in the diffraction spectrum s according to Eq. (35.97) while using the pupil function P without tilt.

The overall light intensity is then calculated as the incoherent sum across the images of all points P of the light source:

$$I_{\mathrm{tot}} = \sum_P a_P(x,y) \cdot a_P^*(x,y) \tag{35.100}$$

However, for state-of-the-art lithography technologies, the real topography of the masks and their materials, described by the complex refractive indices $n + ik$, must be considered as well as polarization effects. This is not possible with analytical approaches like the Kirchhoff approximation [114], which assumes an infinitely thin mask. Moreover, for some investigations, it is not sufficient to only calculate the image generated in the image plane (the so-called aerial image). Instead, the light transmission within the photoresist must be calculated, because the intensity changes due to absorption and reflection.

A possible approach, not using the Kirchhoff approximation, is to simulate the diffraction at the mask via an efficient numerical solution of Maxwell's equations, for example, via the so-called finite-difference time-domain (FDTD) method (see the standard reference [115]) or in Fourier space via a variant of the so-called rigorous coupled-wave analysis (RCWA) (see [116]). The key feature of FDTD is that Maxwell's equations are solved on a staggered grid, one subgrid for the electrical field $\boldsymbol{E}$ and another subgrid for the magnetic field $\boldsymbol{H}$, as visualized in Fig. 35.17: Here, the values of one field vector (either $\boldsymbol{E}$ or $\boldsymbol{H}$) at the time

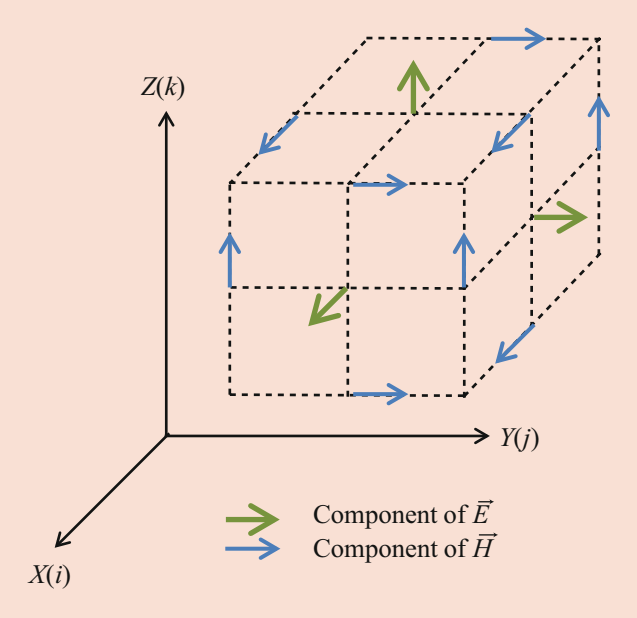

Fig. 35.17 Spatial discretization in the FDTD algorithm: distribution of E and H across the two staggered grids

t_n is calculated from the values of the other field vector (either $\boldsymbol{H}$ or $\boldsymbol{E}$) at the preceding time step t_{n-1}. Both the accuracy and the computation time are about proportional to the number of mesh points. Because the typical mesh size is about 5% of the wavelength λ, the computation time scales with about $1/\lambda^2$ [117]. The method is more appropriate for optical lithography than for EUV lithography where the ratio between wavelength and feature size is much smaller than in optical lithography. Figure 35.18a shows a schematic discretization of an alternating-phase-shift mask AltPSM.

The waveguide method (WG) [117] is a variant of the RCWA which is well suited for the simulation of the impact of EUV masks. Such masks consist of absorbers placed on top of the multilayer MoSi mirror. For the simulation the mask is divided into slices with homogeneous optical properties in the vertical direction; see Fig. 35.18b. Inside these slices or waveguides, both the electromagnetic fields and the permittivity profiles are expanded into Fourier series and are inserted into Maxwell's equations. The problem statement based on Maxwell's equations is transformed into the solution of an eigenvalue problem, which yields the eigenmodes of all mask slices. Using proper boundary conditions, the coupling of the modes of all slices leads to the overall physical response of the system. The computation time scales linearly with the number of inhomogeneous slices (more than one material inside the slice) and cubically with the numbers of the modes considered in both lateral directions. Both FDTD and WG and their advantages and drawbacks are explained more in detail in the literature [117].

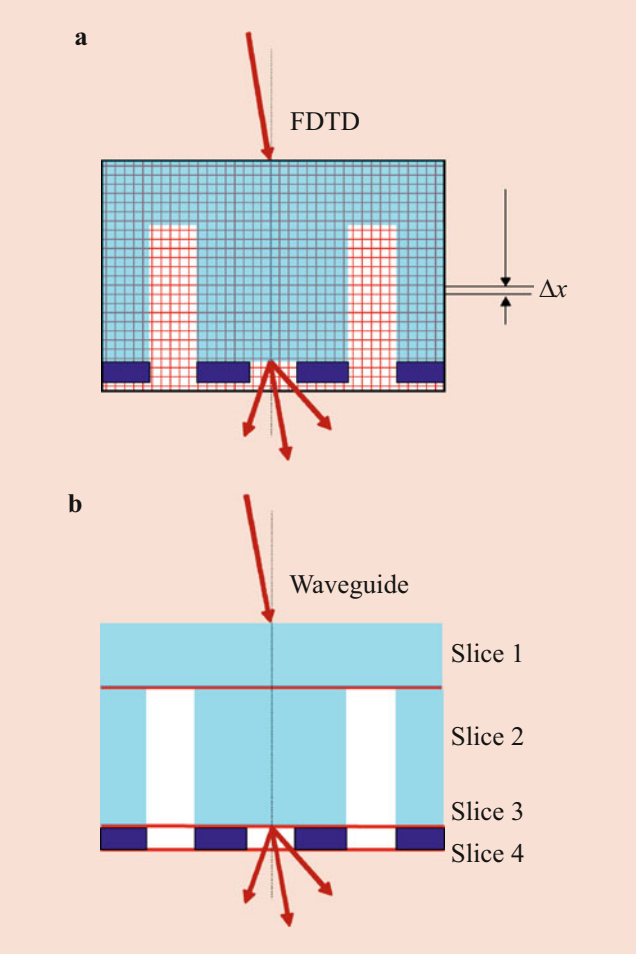

Fig. 35.18 Schematic mask representation for (**a**) FDTD and (**b**) waveguide. The figure shows one and a half periods of a standard alternating phase-shift mask AltPSM and the corresponding FDTD mesh and waveguide slices

Another approach used for the simulation of parts of resist exposure is the transfer matrix method for homogeneous layers. Here, the light intensity within the layer stack is calculated for a given number of layers with their refractive indices $n + ik$, angle of incidence, and polarization. The two variables considered are the amplitude of the incident and the reflected light within the system. Incident and reflected light within a layer propagate as a plain wave with damping constant k, described by a diagonal matrix. Transmission and reflection at the interfaces between layers depend on the complex refractive indices of the layer together with the angles of incidence and the polarization of the light and are expressed by a matrix where the off-diagonal elements describe the reflection. Besides the orientation of the mask features, the difference in the reflectivity between a transversal-electric and a transversal-magnetic wave may result in important polarization effects. A more detailed description of the transfer matrix method can be found in the literature, for example [114].

35.5.4 Simulation of Resist Development

The imaging process outlined above modifies the photoresist due to the locally deposited energy. In the subsequent development step, depending on the resist type used, either the (sufficiently) exposed or the (sufficiently) unexposed parts of the resists are removed.

The common description of this process is given by the Dill model [118]:

$$\frac{\partial M(r,t)}{\partial t} = -C\,\tilde{I}(r,t)\,M(r,t) \tag{35.101}$$

$$a(r,t) = A\,M(r,t) + B \tag{35.102}$$

Here, the concentration of the photoactive compound $M(r,t)$ decreases due to the deposited energy density $\tilde{I}(r,t)$, and the absorption $\alpha(r,t)$ depends on $M(r,t)$. A, B, and C are the Dill model parameters for the photoresist in question. Furthermore, the photoactive compound M diffused with a diffusion coefficient D:

$$\frac{\partial M(r,t)}{\partial t} = D\Delta M(r,t) \tag{35.103}$$

Finally, the local resist development rate $R(M)$ depends on M. Various refinements of this standard reaction-diffusion model were developed in order to describe state-of-the-art photoresists, e.g., chemically amplified resists (CAR).

35.5.5 State-of-the-Art Lithography Simulation

Current state-of-the-art lithography simulation tools employ selections of the basic approaches summarized below in various combinations, depending on the tool and the application in question. Commercially supported tools such as PROLITH [119], Sentaurus-Lithography [120], and OPTOLITH [121] additionally provide elaborated user interfaces, and especially Sentaurus-Lithography and OPTOLITH are integrated with other TCAD tools of the respective vendors. Examples shown in the following subsection have been generated with the research and development simulator Dr.LiTHO [122], which is designed especially for efficiency and flexibility in the implementation of physical models and algorithms.

The semi-analytical Kirchhoff approximation allows for some simple simulation studies where the mask can be approximated as a two-dimensional pattern of transparent and opaque arrays and where polarization effects can be neglected. State-of-the-art masks need to be simulated with numerical approaches such as FDTD, RCWA, or WG, which are also mandatory if polarization comes into play. Whereas these are needed for the near field of the mask, the imaging of this near field onto the wafer may further be simulated, for example, with the Abbe approach outlined above, utilizing the result of the mask simulations. As described above, energy deposition in the photoresist is simulated with the transfer matrix approach, and resist development is being simulated based on the Dill model.

Besides these aspects which are specific to lithography simulation, several more general techniques are also needed, customized, and employed in lithography simulation: During resist development, its surface is moved with one of the techniques described below in Sect. 35.7 on deposition and etching. In order to further improve the efficiency of simulation and to extend the possible sizes and use cases of the masks to be simulated, different domain decomposition methods [123] can be employed which may include not only three-dimensional but partly also two- or even one-dimensional simulations. This may also reuse results of prior simulations which were stored in a repository [123]. To enable important and promising technological approaches such as source-mask co-optimization [124], advanced global optimization algorithms such as genetic algorithms [125] are being employed. Furthermore, as mentioned below in Sect. 35.8 on process variations, lithography simulation is also an essential part of TCAD-based Design-Technology Co-Optimization (DTCO) approaches, in order to establish the link between mask layout and the performance of real devices and circuits.

35.5.6 Examples for State-of-the-Art Lithography Simulation

In the following, a few examples of results obtained with the research and development lithography simulator Dr.LiTHO [122] in the context of current research on the development of advanced lithography technologies are shown.

Figure 35.19 shows the impact of a particle located on an EUV mask pellicle on the printed feature size (critical dimension, CD) for an EUV system with a NA of 0.55 under specific imaging conditions [125]. The pellicle is a polysilicon membrane at 2.5 mm mask distance. One can see that larger particles are critical even in the presence of a mask protection membrane.

Figure 35.20 shows the impact of mask absorber 3D effects on the process window of 20 nm semi isolated lines of a NA 0.33 EUV system [123]. The black curve shows the result for an ideal absorber in combination with a real multilayer and the gray curve the same for a real absorber in combination with a real multilayer. In the simulations, the real absorber can be replaced by an ideal one to "switch off" the absorber-related 3D mask effects. The comparison

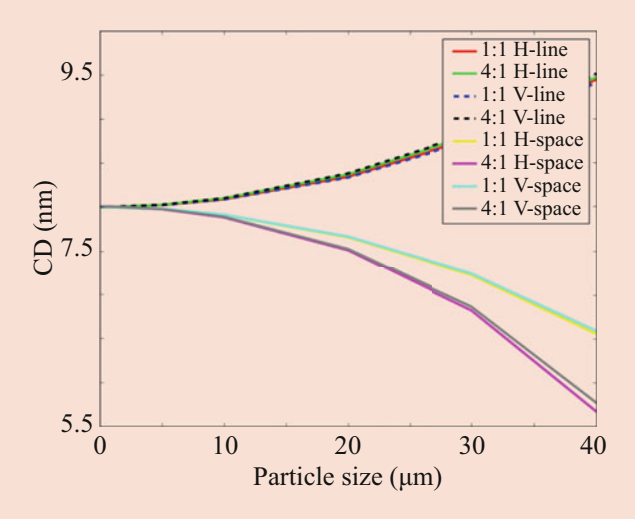

Fig. 35.19 Example for the impact of a particle located on an EUV mask pellicle on the printed CD, for different duty factors *n*:*m* of lines and spaces. The lines and spaces are located either in horizontal (H) direction (perpendicular to the chief ray angle of the system) or in vertical (V) direction (parallel to the chief ray angle of the system) [125]

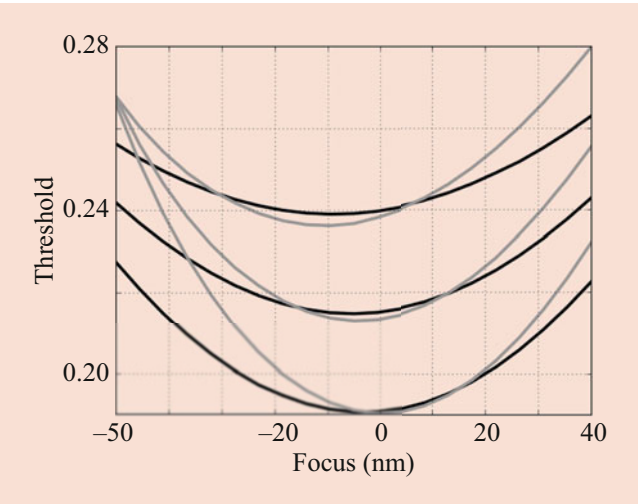

Fig. 35.20 Process windows of an ideal EUV absorber (black, infinitely thin absorber) and a real EUV absorber (gray) both on top of a real EUV multilayer [123]

with the fully real mask shows the effect caused by the real absorber geometry, which is mainly the expected asymmetric through focus behavior.

The defect-induced loss of reflected light and image intensity in the area of an EUV multilayer defect can be partly compensated by a removal of absorber in the vicinity of the defect. Figure 35.21 demonstrates a simulation of this method for 32 nm features at a NA of 0.33 [126]. The repair is done by removal of the absorber in a circle around the center of the defect; see dashed larger circles in the figure, with an optimum of 50 nm (wafer scale). Other defect positions and sizes may require more complex repair shapes, especially at larger NAs where more details of the defect will become visible.

35.6 Simulation of Deposition and Etching

Similar to lithography, also for deposition and etching, it is indispensable to take equipment effects into account when simulating the process results on feature scale. However, here mostly a clear separation can be made between the equipment and the feature-scale level: Equipment simulation (on a scale of centimeters to meters) can be used in a preparatory step to calculate quantities just above the (macroscopically flat) wafer, such as local gas or particle flows and local temperatures, which are affected by the reactor geometry, process recipes, and partly varying further parameters. These intermediate results can then be used as inputs for feature-scale simulation (on the scale of micro- to nanometers) of the local deposition and etching of layers. Figure 35.22 visualizes the separation between these simulation scales.

The area of the simulation of deposition and etching is very diverse in three respects: First, it includes macroscopic equipment and nanoscale feature simulation, and moreover also the (generally three-dimensional) simulation of the evolvement of partly complex surfaces. These aspects are reflected by the following subsections. Second, there is a huge variety of etching and deposition processes which cannot be covered within the space available for this section. Therefore, here only the basic principles and approaches are discussed, and no attempt is made to list the specific equations and parameters for the large variety of processes used in semiconductor technology.

35.6.1 Outline of Equipment Simulation

Whereas in the area of lithography integrated equipment and feature-scale process simulation is mandatory since long, as described in the preceding section, for both deposition and etching, the simulation at equipment level can be separated from the feature-scale simulation. Similar to this, this separation is also possible for diffusion and oxidation, whereas in these two areas, equipment simulation is rarely used. Except for plasma doping, e.g [127], for ion implantation equipment simulation has so far not been an issue.

In most cases equipment simulation consists of the following steps:

1. Three-dimensional discretization of the process reactor or furnace.
2. Establish assumptions on the physical/chemical modeling

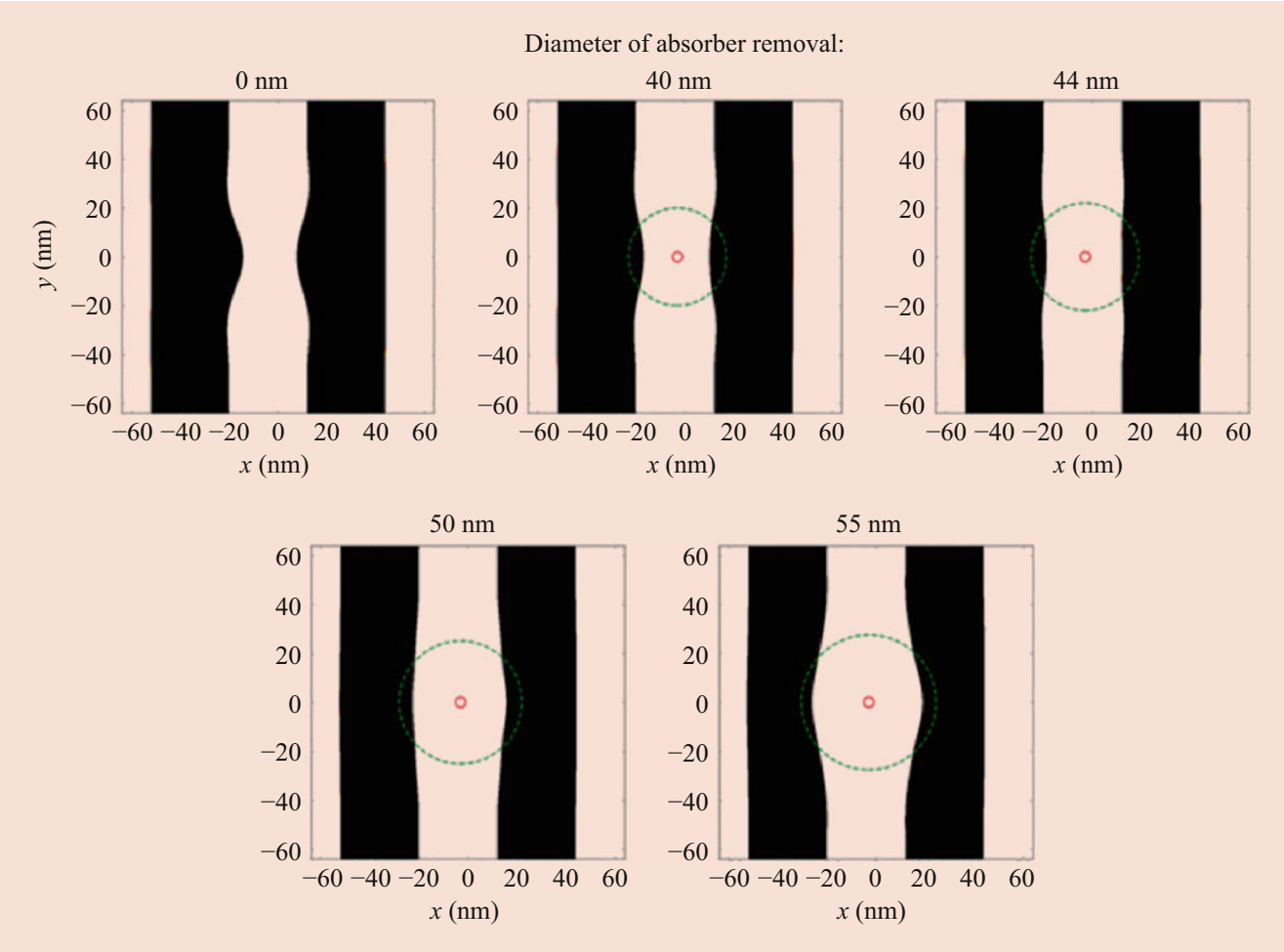

Fig. 35.21 EUV multilayer defect repair by increasing absorber removal around the defect. The defect caused line deformation is reduced with an optimum at 50 nm absorber removal [126]

components for the system in question, e.g., gas flow, resistive or inductive heating, radiative heat transfer, plasma physics, characteristics of sputter targets, chemical reactions, etc.

3. Set up and solve a system of partial differential equations, representing fluid dynamics, thermal behavior, plasma characteristics, electrical properties, and chemical reactions for the equipment, possibly including macroscopic models for the interaction with the wafers (e.g., as sinks or sources for heat or for chemical species). Such macroscopic models do not have to resolve the individual features on the wafer. This step can be omitted if, e.g., the particle flow can be extracted directly in step 4 from the characteristics of a sputter target defined in step 2.
4. Extract from the equipment simulations the quantities of interest directly above the wafer, e.g., temperature, pressure, species concentration, angular or energy distributions of ions, electrical field, or potential (without considering individual features on the wafer).

Whereas all these steps are necessary to define and describe the equipment and process in question, the main numerical effort is needed for step 3, except for cases where no fluid dynamics is involved. In order to efficiently implement step 3, usually well-established computational fluid dynamics [128] or plasma simulation codes [129] are employed, which then have to be supplied by the user with the relevant physical data and models, as described above.

As an example, Fig. 35.22a deals with the equipment simulation of the deposition of silicon oxide in a capacitively coupled plasma-enhanced chemical vapor deposition (PECVD) reactor using oxygen and TEOS chemistry. The contour colors in the figure represent the concentration of the oxygen radicals. The corresponding fluxes of oxygen radicals, together with the fluxes of oxygen ions, provide the boundary conditions for the feature-scale simulation, the result of which is shown in Fig. 35.22b. This figure represents a cross section of a contact hole with a non-conformally deposited silicon oxide layer.

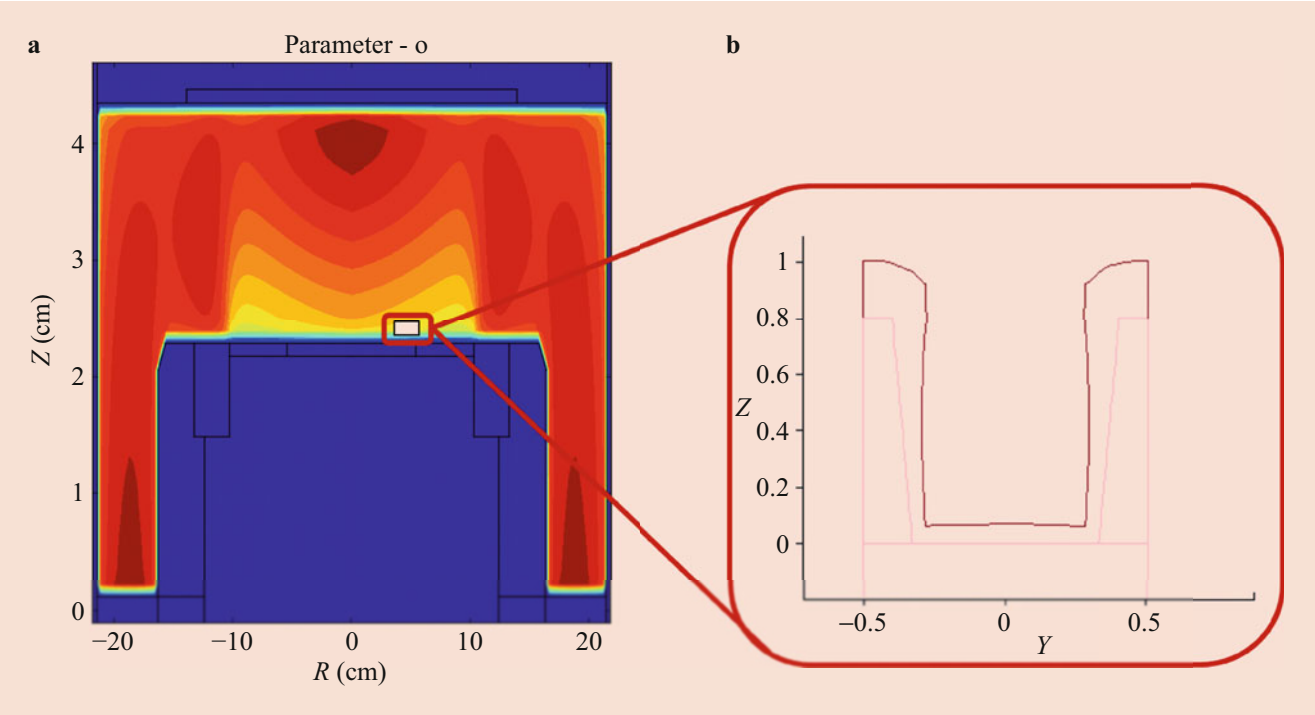

Fig. 35.22 Visualization of the scales of (**a**) equipment and (**b**) feature-scale simulation for deposition and etching. The clipping for feature-scale simulation in the left figure is not to scale

In case of diffusion and oxidation processes, the situation is somewhat easier, because the process gas does not react in the furnace volume, but only on the wafer (in case of oxidation, transforming silicon to silicon oxide). Here, step 3 is reduced to the simulation of fluid dynamics and thermal behavior. However, several transient effects might need to be considered, due to the movement of a wafer or a batch of wafers into or out of the preheated furnace or due to ramping the temperature up and down while the wafer is being processed. This is especially important in case of very short time annealing processes, such as spike or millisecond annealing, which need elaborated simulation of the transient local temperature distributions because these are not in equilibrium. For example, laser thermal annealing was discussed in [130].

35.6.2 Discretization and Movement of Surfaces

Deposition and etching do not only change the geometry of the device or structure during fabrication, but may also change its topology: New layers may be added, old layers may be completely removed, originally connected features may get disconnect and vice versa, and holes may be transferred into voids. Very small features may be critical, because they may, e.g., act as an etch stop. Also curved, tilted, and non-axis-aligned structures must be accurately described. In turn, it is vital to employ surface discretizations and algorithms for their update, which are numerically efficient and stable, can reliably handle arbitrary topographies and their changes and allow for adaptive control of the local number of elements used, to achieve a good compromise between accuracy and efficiency.

Three main methods have been used for the description of geometries and of their changes during processing. The simplest and most stable is the cell-based description and the related cell-removal algorithm [131], which is, however, due to its inherent limitations hardly used any more and here only mentioned for historical and reference purposes. The other two approaches are triangulation and the level set method. Triangulation is the three-dimensional extension [132] of the "string algorithm" which was generally used for two-dimensional topography simulation [133]. Here, surfaces and interfaces are discretized by triangles. Geometrical changes during processes are then described by moving the vertices of the triangles according to rates which result from physical models as described in Sect. 35.6.3. The main advantage is that these models can directly use the position, size, and orientation of these triangles. The main disadvantage is that it is difficult with this approach to deal with topological changes, e.g., in case that during layer deposition the opening of a hole closes to form a void, as it would happen if the process shown in Fig. 35.23 would be continued.

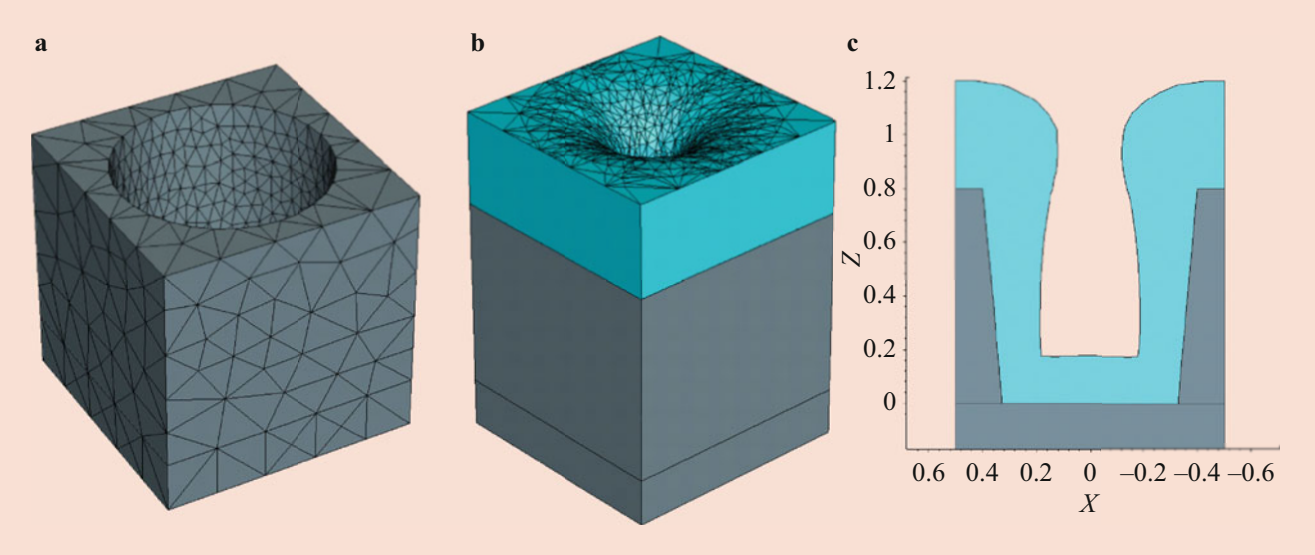

Fig. 35.23 Example for the discretization of a three-dimensional structure using triangles. (**a**) Initial contact hole; (**b**) simulation of non-conformal deposition of low-temperature oxide (LTO). Here, the side-wall faces of the simulation structure are discretized as rectangles; (**c**) cross-sectional view. The scale shown is in microns

The approach which is most frequently used for the discretization of three-dimensional surfaces and interfaces is the level set method: Here, the surface is described as the set of points $\boldsymbol{x}$ where a three-dimensional function $F(\boldsymbol{x}, t)$ equals zero, and the movement of the surface is simulated based on local rates $\boldsymbol{r}(\boldsymbol{x}, t)$:

$$\frac{\partial F(\boldsymbol{x}, t)}{\partial t} + \boldsymbol{r}(\boldsymbol{x}, t) \cdot \nabla F(\boldsymbol{x}, t) = 0 \tag{35.104}$$

The main advantages are that with this approach surfaces and interfaces are given as solutions of partial differential equations, which are solved on a three-dimensional mesh, similar to bulk variables like dopant concentrations, and that changes in topology should not lead to problems if the underlying three-dimensional grid is locally fine enough. The disadvantage is that surface elements and surface normals needed in the implementation of the physical models as outlined in Sect. 35.6.3 are not given directly and must be extracted separately from the level set description.

35.6.3 Models for Deposition and Etching Rates

Physical/chemical models for deposition and etching consider the interaction of different ionic or neutral species with the surface to allow the determination of local deposition or etching rates. Boundary conditions for the feature-scale modeling can be provided by equipment simulations or measurements, e.g., of temperature, pressure, species concentrations, or energies of neutrals and ions. In the following, as an example we discuss low-pressure chemical vapor deposition, where the mean free path is large compared with the feature size and the particles move isotropically in the volume of the reactor far away from the surface.

Assuming a triangulated surface, for each triangle I the reaction flux R_i depends on the flux of particles from free space A_i and from all other triangles j, S_{ij}. Whereas the impinging particles are incorporated into the growing layer with a sticking coefficient sc, the remaining particles are desorbed and may arrive at other parts of the surface. Here, the notation from the literature [132] is used, in which also more details are given:

$$R_i = \mathrm{sc} \cdot \left(A_i + \sum_j S_{ij} \right) \tag{35.105}$$

Here, the fluxes from free space and from all other triangles are calculated based on the solid angle for free sight to gas space Ω_{free}, the solid angle of free sight to all other triangles j, $\Delta\Omega_{ij}$, and the angle ϑ_{ij} between the surface normal of triangle i and the straight line between the centers of triangle i and triangle j; see Fig. 35.24:

$$S_{ij} = R_j \frac{1 - \mathrm{sc}}{\pi\ \mathrm{sc}} \cos\vartheta_{ij} \cdot \Delta\Omega_{ij} \tag{35.106}$$

The flux A_i from the gas volume is obtained by

$$A_i = G \int_{\Omega_{\mathrm{free}}} \cos\vartheta \, \mathrm{d}\Omega \tag{35.107}$$

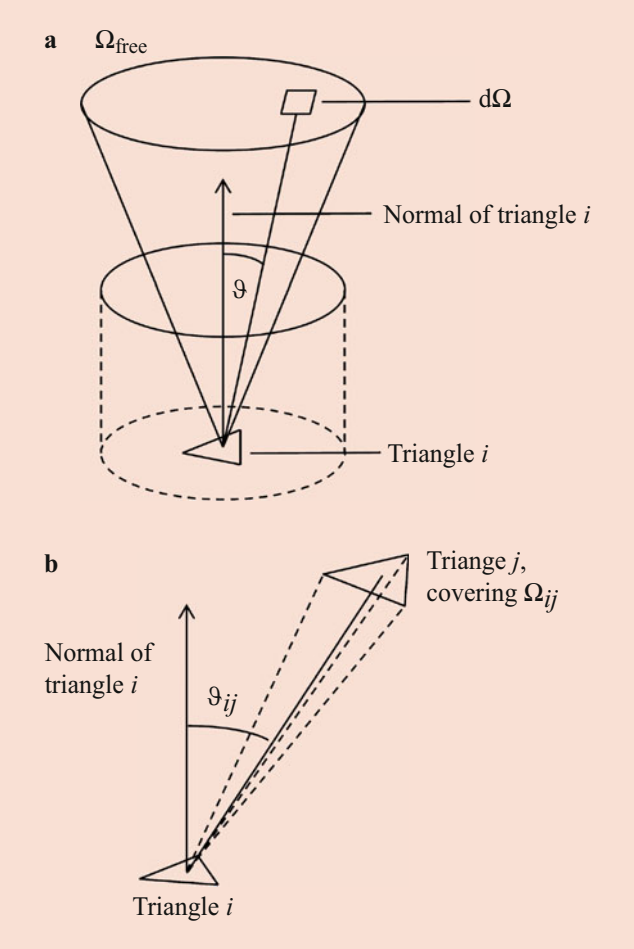

Fig. 35.24 (**a**) Solid angle Ω_{free} covering the region of free sight to gas space for a triangle *i* at the bottom of a cylindrical contact hole; (**b**) geometry for two arbitrary triangles with particle transfer to be calculated

where ϑ is the angle between the normal of triangle i and the direction from triangle i to dΩ (see Fig. 35.24).

Establishing the flux balance between all triangles and with free space results in a system of linear equations for the reaction fluxes R_i, with the transfer matrix T_{ij} between triangles *I* and j:

$$\pi R_i - \sum_{j \neq i} T_{ij} R_j = \pi - \frac{1}{1 - \mathrm{sc}} \sum_{j \neq i} T_{ij} \tag{35.108}$$

$$T_{ij} = (1 - \mathrm{sc}) \cos \vartheta_{ij} \cdot \Delta\Omega_{ij} \tag{35.109}$$

Here, for the transfer matrix elements T_{ij}, the calculation of the angles of free sight to gas space and especially to all other triangles is needed. For the latter, it must be checked if the view is (partly) blocked by any other triangle. In turn, for a surface discretization consisting of *n* triangles, the numerical effort scales with the third power of *n*.

Finally, the absolute deposition rates for each surface segment are obtained by normalizing to the deposition rate for a one-dimensional (flat) geometry. That one-dimensional deposition rate and the sticking coefficient are the only physical parameters of the process, whereas the transfer matrix characterizes the geometry. These have to be re-calculated after each time step to take the changes of the geometry into account.

In terms of computational efficiency, subsequent work has dealt especially with the optimum way to calculate the angles of free sight. Other numerical issues have been the appropriate adaptive surface discretization with one of the methods outlined in Sect. 35.6.2 and the efficient implementation of surface movement.

Figure 35.23 shows an example of a simulation that has been carried out with the model described above assuming a sticking coefficient of 0.15 which is a typical value for the modeling of a low-temperature oxide (LTO) process.

This basic model for deposition has been extended and adapted to the different deposition processes in various respects:

- Processes in which more than one mechanism contributes to the deposition. In the simplest case, the approach is applied simultaneously to two or more reaction species, which show no interaction and are each described by their one-dimensional deposition rate and their sticking coefficient.
- Long-throw sputter deposition which is characterized by the emission characteristics of the sputter source, collisionless movement of the sputtered particles due to low pressure, and a sticking coefficient of unity. Here, the transfer matrix is not needed, and the local deposition rates are calculated by integrating the contributions of the sputter source across the angle of free sight for the surface point in question, as discussed in the literature [134].
- Considering different species which either react on the surface and/or sputter away some already deposited atoms. This leads to additional terms in Eq. (35.105) while not changing the basic approach because the role and computation of the transfer matrix does not change. An example is ionized metal plasma deposition [135].

Such models can also be implemented by using Monte Carlo ray tracing instead of the transfer matrix method [136]: Here, trajectories of pseudo-particles are traced until they hit the layer surface. Similar to above, physical models are employed for the initial emission statistics of the particles and their adsorption, reaction, and desorption at the wafer surface. This also allows for the simulation of deposition

processes which are carried out in two steps, like atomic layer deposition (ALD) [137].

For etching, depending on the process in question, some or all of the elements discussed above for deposition may show up. In most cases of etching, physical and chemical sputtering play major roles, with the corresponding yields introduced as model parameters, replacing or complementing sticking coefficients [138]. However, adsorption/desorption and in turn transfer matrices may still play a role, because for some etching processes the emission and re-adsorption of species need to be modeled.

A detailed open-access review paper [139] deals especially with numerical aspects linked to the usage of the level set algorithm and physical models for etching simulation.

35.7 Process Variations

For advanced micro- and nanoelectronic devices and circuits, both statistical and systematical process variations come into play, which influence the performance of devices and systems. In result, although the nominal product, fabricated under ideal circumstances, may meet the specifications and required figures of merit, a considerable fraction of devices and circuits may fail to do so, causing yield loss and critical increase of fabrication costs per sold unit. In turn, the impact of such process variations must be known and minimized as much as necessary.

Statistical process variations such as random dopant fluctuations RDF [3], line edge roughness LER [140], and metal grain granularity MGG [141] result from the granularity of matter. They have been considered since long in dedicated device studies, employing special efficient device simulation tools [142] and simple but valid assumptions on the statistical distribution of these variations. This is in line with the frequent practice in device simulation to start from assumed idealized device geometries and dopant distributions. However, in a real fabrication environment not only the full process flow must be considered, which leads to non-idealized device geometries and dopant distributions, but also its variations. In the following, a brief overview of the sources of systematic process variations is given, together with a hierarchical approach to simulate their effect on devices and circuits.

35.7.1 Sources of Systematic Process Variations

Systematic process variations may occur in all major process steps. They can be grouped into two categories: First, inhomogeneity which is inherent to the equipment used and which can neither be completely avoided by optimizing the equipment design nor the process flow. Second, some process parameters cannot be controlled precisely or may have some drifts during processing or on the long run between repeated process steps.

For both optical and EUV lithography, both the distance between the optical system (last lens or last mirror) and the wafer and the energy emitted by the light source may change from illumination to illumination in the standard step-and-repeat process, leading to systematic variations between different dies on one wafer and especially between different wafers. The so-called process window in Fig. 35.25 shows examples how these variations of focus and dose, respectively, modify the size of the features generated in the lithography step, the so-called critical dimensions (CD).

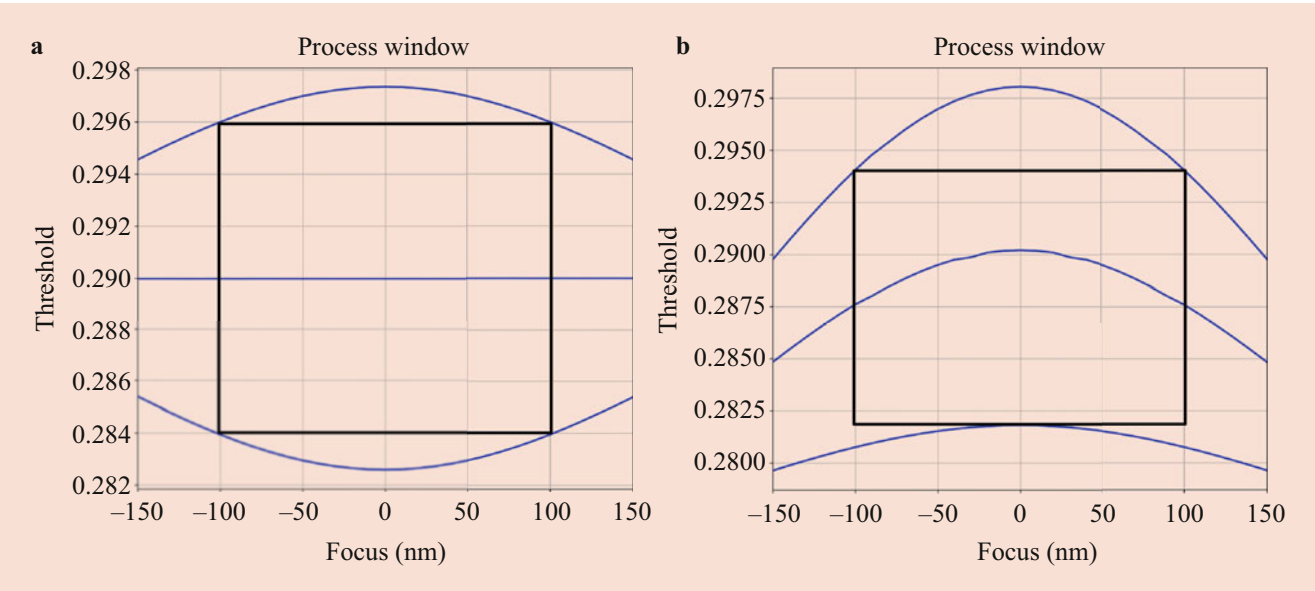

Fig. 35.25 Process window in optical lithography for (**a**) 120 nm pitch with 60 nm lines and (**b**) 72 nm lines

Here, the central line shows the combinations of focus and dose which lead to the nominal CD (60 nm left picture, 72 nm right picture), whereas the upper and lower lines show the combinations of focus and dose which lead to a CD increase or decrease by 10%, respectively. Whereas under specific imaging conditions, the CD stays constant for varying focus at a specific fixed dose, for other imaging conditions, this is not the case. Additionally, also some other process variations may occur in lithography steps, caused, e.g., by defects and imperfections of the optical system or imperfect wafer alignment.

For etching and deposition, especially inhomogeneous concentrations of ions and neutrals, the temperature distribution, or the emission characteristics of the sputter target lead to systematic process variations across the wafers or between wafers. Figure 35.26 shows an example for the dependence of the etch rate on the distance from the center of the wafer for reactive ion etching of silicon based on chlorine chemistry.

Further systematic process variations include among others differences between nominally equal temperature profiles in very short time annealing processes, such as millisecond or laser thermal annealing [130].

35.7.2 Hierarchical Simulation of the Impact of Process Variations

In order to predict the impact of process variations on devices and systems, it is necessary to trace them through the whole fabrications process: Not only the process step where the variation occurs must be simulated, but all subsequent process steps must be simulated, using as starting conditions both the intermediate results without and with the effects of that variation. Furthermore, it is necessary to make sure that numerical errors which occur throughout the simulation or when changing between the data representation of different simulation modules or tools do not invalidate the variability study: They must affect the result significantly less than the variation in question.

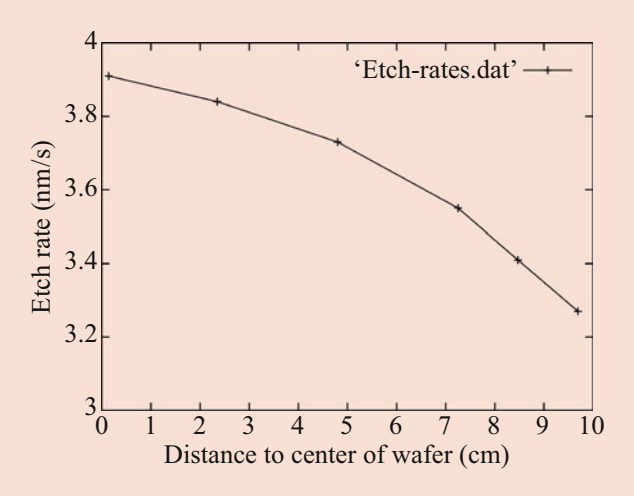

Fig. 35.26 Example for the dependence of etch rate of a silicon etching process on the distance from the center of the wafer

From the modeling point of view, the study of process variations requires to employ appropriate models: First, models which describe the effect of the process variation at the step at which it occurs – e.g., the impact of focus on the CD generated in a lithography step. Next, models must be used which are capable of tracing the changes of the results of that process step (here the CD) through all following process steps. Generally, both requirements can be met by selecting a suitable process model among the ones available.

In real cases, a state-of-the-art process flow may be affected by a large number of process variations. Considering just 10 process variations and just 5 parameter values for each of them would yield a final split of 5^{10} or nearly ten million process simulations, which is of course not feasible. In turn, it is necessary to first select the most relevant process variations (about 3–5) and then to employ a suitable design-of-experiment approach to define the set of process simulations needed, as discussed elsewhere [143].

In result, geometries, dopant distributions, and potentially other quantities which characterize a device (or interconnect) are simulated for different values of the input process variations. Considering, e.g., three process variations which are discretized with three values each, a matrix of $3 \times 3 \times 3$ devices results. In order to extract compact models which are aware of variations, first the nominal compact model for the nominal device without any variations is extracted. In the second step, this compact model is extended to also include the process corners considered, which means in the example addressed here the $3 \times 3 \times 3$ devices [144]. Finally, statistical device simulation is employed to extend this compact model to also include the statistical process variations, such as RDF [144]. A later improvement of this method [145] has enabled the direct usage of the values of the systematic process variations (e.g., defocus) in the second compact model extraction step outlined above [143]; see Fig. 35.27. As an example Fig. 35.28 shows the saturation current of a nanowire transistor.

More detailed descriptions of the sources of process variations and of the hierarchical simulation of their impacts on devices and are given in a related open-access papers [143] [145].

35.8 Conclusions

Process simulation is the virtual image of IC manufacturing on a computer: It covers the whole development from the bare silicon wafer to the final device and circuit. Its full benefit can only materialize if accurate physical models with proper parameters are available within numerically stable and correct simulators.

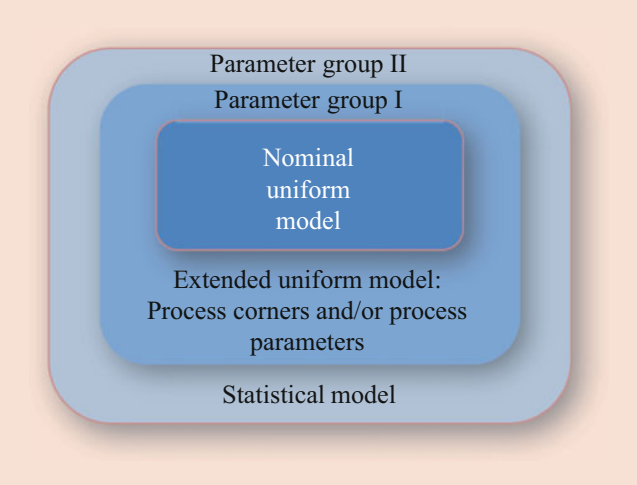

Fig. 35.27 Extraction and generation of hierarchical compact model aware of systematic and statistical process variations, following the approach published before [145]

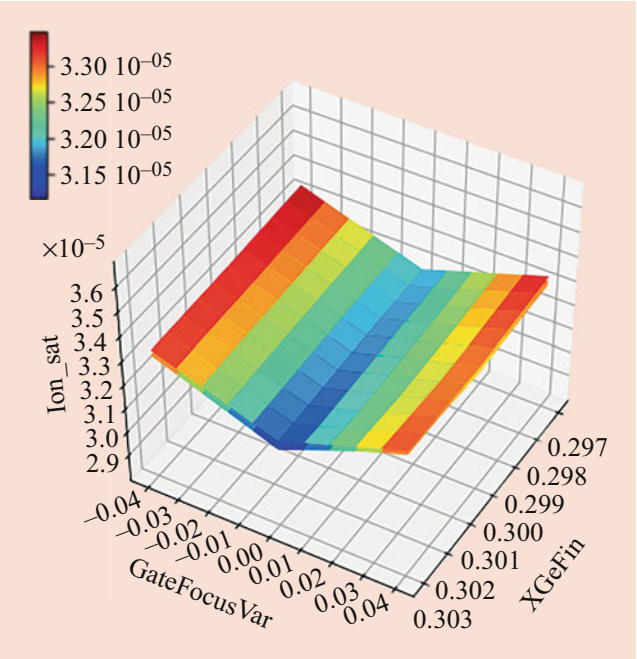

Fig. 35.28 Saturation current (color in amperes) of a nanowire NMOS described by the extended compact model (color in amperes) [145]

The applications of process simulation are manifold. Nowadays it is most frequently used in industry for the development and optimization of the process flows needed for the fabrication of devices. The success of this approach depends on the availability of advanced process simulation tools which cover the whole fabrication sequence, are closely linked with device simulation, and are accompanied by good user support. Because the speed of simulation is a key requirement for the simulation splits used in technology and device optimization, very frequently efficient models are used which depend on calibrations for the process flow in question. On the other hand, physically rigorous models are readily used for development and optimization of new advanced processes or pieces of equipment. Here, predictivity with as little calibration as possible is the key requirement, not the integration into an overall simulation system.

An increasingly important advantage of process simulation is that it can be used not only to study and select process options but also to quantify and minimize the impact of systematic process variations which are caused by the equipment used. Here, it makes indispensable contributions to the simultaneous development and optimization of technologies, devices, circuits, and designs, the so-called Design-Technology Co-Optimization (DTCO), which has in recent year developed into a key and indispensable method for the nanoelectronics industry.

With new semiconductor materials coming into use and new device architectures (including new carriers of information like spin or the phase of the material) emerging, the complexity of the processes to be simulated is continuing to grow. So are the requirements on model accuracy and generality and efficiency of simulation. There will also in future be several (but of course different from the past) challenges left for developers in the process simulation area.

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A Digital Twin for MEMS and NEMS

36

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Contents

36.1 General Considerations 1303
36.1.1 Digital Twinning for MEMS and NEMS 1304
36.1.2 A Formal Classification System for MEMS and NEMS 1305
36.1.3 The Structure of the Chapter 1307

36.2 Analytical Modeling 1308
36.2.1 Introduction 1308
36.2.2 Analytical Mechanics of MEMS 1308
36.2.3 Dynamics of Electromagnetic Levitation Micro-Systems 1310
36.2.4 Stability of Electromagnetic Levitation Micro-Systems 1313
36.2.5 Phenomenological Model of Heat Transfer in Hard-Disk Air Bearing 1315

36.3 Topology Optimization 1319
36.3.1 General Considerations in Topology Optimization 1319
36.3.2 Applications in Microfluidics and Nano-Optics 1322

36.4 Model Order Reduction 1326
36.4.1 Reduced Basis Method for Steady Linear Parametric Systems 1326
36.4.2 Structure Preserving MOR for Nonlinear Port-Hamiltonian Systems 1328
36.4.3 Application to Topology Optimization 1329

36.5 Conclusions 1330

References 1330

Abstract

In this chapter we consider a comprehensive, multiphysical digital twin for NEMS and MEMS, in particular, for a range of effects that are currently of interest in electromechanical MEMS. The chapter first approaches the formation of a digital twin from the viewpoint of analytical equations. Once these approach their validity limit, numerical approaches become necessary. This will, most generally, lead to a topology optimization formulation, in order to drive the discovery of optimal device layout, which is next described. Due to mesh refinement, such models quickly become unwieldly to handle, since they result in to many degrees-of-freedom. In the last section of the chapter, we consider model order reduction as a means to turn large discrete models into compact models, approaching the lower order analytical models in complexity, but retaining the specific accuracy of the general numerical approach.

Keywords

MEMS · NEMS · Modelling · Simulation · Topology optimization · Model order reduction

36.1 General Considerations

It is not clear who first claimed that "*The essence of engineering is design*", but for many engineering endeavours the statement holds fairly accurately, separating engineering somewhat from the natural sciences. As a result, the role of simulation and modelling has its own focus, namely, supporting the engineer in making better, more reliable, and more manufacturable (product) designs. In this context the special requirements of microelectromechanical systems (MEMS) and their tinier twins, nanoelectromechanical sys-

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tems (NEMS) is considered. Such systems are hardly ever conceived of outside of a particular application domain, and are expected to perform subject to the constraints of the application, which may for example demand error free operation for a long time under adverse conditions. As a result, the engineer will need to move her focus during a development cycle, starting with a broad concept to define the borders of focus, then zooming in to details, and once satisfied, zooming out again to the application. This might occur repeatedly. Design is typically iterative, since it is also a discovery process, hence the focus of an engineer (or team) will repeatedly vary so as to ensure meeting various kinds of constraint in the best possible manner. This chapter is hence focusing on numerical techniques that will be useful in supporting the engineer in this process, by facilitating the answering of questions related to design in an efficient manner, hopefully providing the engineer with additional tools to go beyond what is otherwise possible.

36.1.1 Digital Twinning for MEMS and NEMS

MEMS, NEMS, and semiconductor chips share the fact that they are produced at the wafer scale, in dustfree and environmentally controlled cleanrooms, with manufacturing based on a sequence of additive and subtractive processes interleaved by lithography steps, and followed by assembly and packaging. For MEMS and NEMS, significant differences to pure semiconductor manufacturing also exist. They are often physically closer to the application, because of their multiphysical character (measuring a fluid, or a gas, or being buried deep within a process or machine), integrating tiny detectors, actuators, or by being integrated into tiny machines. The differences to pure electronics mean that one requires a larger variety of manufacturing process steps, so that less of the steps are shared among the rather broad number of applications, placing MEMS and NEMS manufacturing also in direct opposition to semiconductor manufacturing.

Technology CAD is a term that has been coined to describe the **digital twin** of the semiconductor, and especially, the CMOS industry. It has been vastly successful, mirroring in software every single manufacturing and operational modality of a semiconductur chip, across the length scales, and even across the experimentation modes. This single fact has enabled the industry to rapidly advance from proof-of-principle considerations to systems and even statistical yield design.

It is therefore tempting to ask whether the CMOS success story can be copied for the MEMS and NEMS industry. Clearly, there is no fundamental reason why this should not be possible. Indeed, most MEMS and NEMS manufacturing steps have, at some point during their exploration, been mapped to a physical simulation program. There are however economic reasons why the task is considerably more difficult to establish in practise. Software is never stationary, and continuously needs to be updated. Computer hardware is evolving, as are compilers and libraries, so that the programmer is constantly adapting the code. The salary of the programmer (who might have a PhD in engineering) needs to be paid, requiring income from a customer, and if a particular manufacturing process step is not used by sufficiently many customers, the programmer cannot be funded.

Of course, not everything is completely hopeless, and indeed careful analysis can reveal common physical (theory) features among the processing steps, so that generic blocks of software may be useful in more than one manufacturing step, returning us back to an economic situation.

It is therefore worthwile to consider some of the differing MEMS processing steps. These are classified into two categories:

- 3D manufacturing:

  Anisotropic etching. Silicon can be wet-etched along its crystal planes. It can also be dry-etched vertically into the wafer using a plasma, such as the Bosch process or the Cryo process. This provides limited 3D patterning capabilities.

  3D (nano) lithography. Photopolymers can be structured using a highly-focused light beam. One method is stereolithography, whereby the upper surface of a liquid resist is transformed by a projected image or by a scanning laser spot. Another method is the use of two-photon absorption, achieving a resolution of 90 nm. Various methods exist to transform the polymer structures into other material patterns, e.g., metals. This provides almost unlimited 3D shaping capabilities [1].

  3D deposition. Using an aerosol jet, it is possible to deposit almost any material that can be formed into a spray (such as nanoparticle suspensions of ceramics and metals, or dissolved polymers) at high resolution on any 3-dimensional surface. Some free-form capabilities exist as well.

- Novel material systems:

  Carbon. Certain polymers, deposited in 3D at the nano to micro length scale, can be converted into pure glassy carbon by pyrolysis. Apart from the fairly high temperature required (ca. 700 °C), the method is very general, and the geometrical transformation highly predictable [2].

  Glass. By mixing glass nanopowder with a photopolymer of similar refractive index, it is possible to nanostructure green parts at the full resolution of current nanolithography. Subsequent sintering at sufficiently high temperature produces glass parts with exquisite fidelity [3].

Polymers. Increasingly, polymers are being introduced into MEMS and NEMS as tunable functional material systems. They are often available as photopolymers, which can be lithographically patterned, or otherwise, after plasma deposition, patterned by mask assisted plasma etching.

Self-assembly chemical frameworks. Using dipcoating processes, and simplified bonding chemistry (such as click chemistry), it is possible to form sophisticated quasi crystalline layers, layer by layer, conformally onto a 3-dimensional surface. Full molecular control of porosity is possible, for example by using metal-organic frameworks.

For many of the above processing steps (the exception is the crystalline wet-etching of Si), the manufacturing operations are sufficiently well described by either existing CMOS process simulation programs, or CAD-like geometry transforming processes, so that physical based simulation is often not even necessary at the digital twin level.

The situation is dramatically different for device and system simulation. The reason is that MEMS and NEMS are ultimately multi-physical, with novel opportunities emerging constantly, driven by current and future application domains. As a result, and in contrast to microelectronics with a focus on current and voltage effects at ever smaller dimensions and ever higher frequencies but with the roadmap fairly well laid out, MEMS and NEMS requires more planning to find the common elements to facilitate a possible roadmap, and a digital twin plan. Some of these ideas are now considered.

36.1.2 A Formal Classification System for MEMS and NEMS

In the late 1980s Professor Simon Middelhoek from Delft University of Technology defined [4] the famous sensor cube, an organisational device to bring structure to the field of transducers, and relevant to this day. The basic idea is that, every MEMS or NEMS device known transforms energy (power) among the basic energy domains *ED*, $ED \in$ {electrical, magnetic, mechanical, optical, chemical, spin, thermal, nuclear}. Thus a thermo-electric sensor operates between the thermal and the electrical domain. By forming a table of two or more dimensions, with the orthogonal table edges having an entry for each of the energy domains, it is possible to define for each square or cube in the matrix a particular coupling effect, such as the Seebeck, Faraday, Nerst, etc. effects. Some devices operate between three energy domains, through the use of an intermediate domain, hence the need for a cube in the relationship, and of course additional dimension is added when influence terms are also needed (such as the case of a transistor whose gate adds an influence axis to the table entry for an electrical to electrical transducer). The most successful system components are those that provide for influence or output terms in the electrical domain, making them intregratable with electrical circuitry (Fig. 36.1).

Physical Scales and Details

Often it is necessary to refer to the scale of things. For example, as sizes reduce, the importance of volume to area reduces, so that surface effects dominate at the micro and nano metre scale, and mass effects becomes relatively unimportant. An easily grasped example is the mosquito, which is held above water by surface tension effects, whereas humans are prone to sink. Similarly, time scales of volumetric effects reduce, increasing the importance of very fast inertial effects which can under circumstance catch up with the time scales of radiative effects. Here an interesting example is the ability of a nanobeam to oscillate as fast as radiofrequency waves, opening up interesting application opportunities. It is thus advisable to consider sensor effects under scaling laws (for example, by replacing each variable by its scaled version, then scaling the entire expression). This might necessitate to reconsider the modelling equations, and provide opportunities for simplification.

Numerical Techniques and Computational Methodologies

Software construction has become hugely successful due to the concept of reuseability, i.e., a software component is seen as a generic block that finds employment in a number of vastly different situations. At that point, it is important to standardise the interface to the component, so that software design can be performed for the remaining parts. A common understanding among component designs will naturally lead to even more efficiency for designing new software modules. It is a bit like agreeing on a metric system for nuts and bolts.

There are of course many levels of structure that can be organised. The most common are specific data structures that are particularly efficient in maintaining particular collections. Some interesting elements are:

List, or vector. This is the easiest form of data structure, since it easily maps to computer memory, simply occupying a contiguous section of it, and linearly indexed from the start. If contiguity is sacrificed, the list becomes a tree.

Lists of lists, or matrix. A concatenation of equal length lists can be grouped to form a matrix, which also can be efficiently stored in contiguous memory. The list unit then is either the row or column of the matrix.

Sparse matrix. Because many numerical methods operate on matrices that are very sparsely populated, vast amounts of memory can be saved by implementing suitable data structures that remove some or most of the reduncancy. A popular structure is the Matrix Market container for numerical matrices.

Tree. Tree structures are a useful efficient technique to localise sparse data w.r.t. ordering parameters. Binary,

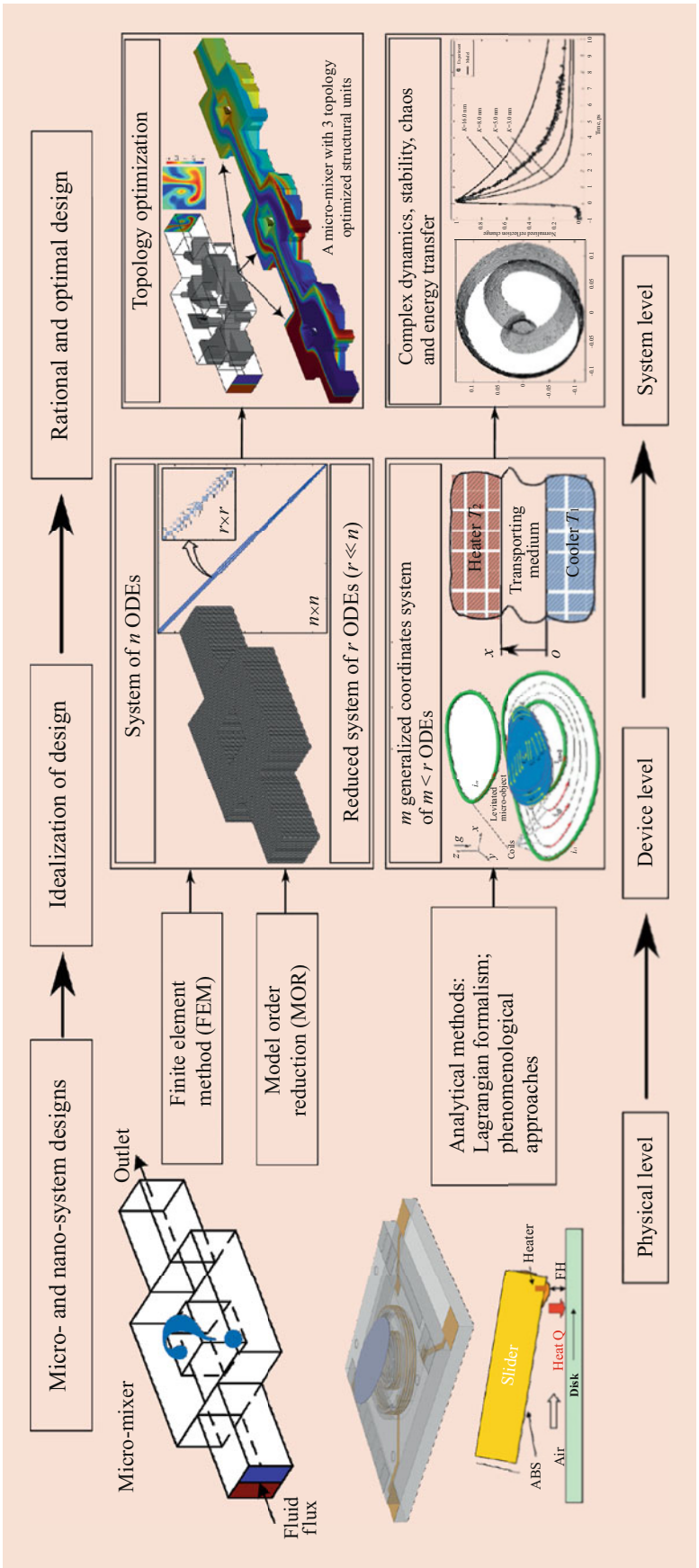


Fig. 36.1 Analytical ling and numerical simulation are twinned methods, differing in the degree of geometrical generality, and the number of unknowns. Analytical modelling always precedes numerical models, but without necessarily striving for simplicity. Analytical models are reduced in complexity by simplification and the application of symmetries. Numerical models are compacted using model order reduction. The forward problem (analytical or numerical) may be inversely solved using an iterative procedure, thereby directly facilitation the act of design

quad, and oct-trees are used when 1D, 2D and 3D spatial data is involved, but of course any form of abstraction is possible, as is anisotropy of the tree. In principle, a tree is grown according to a splitting rule, which might be decided on the fly, then leading to mixed trees.

Mesh. A mesh data structure is needed for certain computational methods, notably finite elements, boundary elements, or finite volume methods. The primitives are nodes, edges, faces, and volumes. All items will have local and global numbers, and knowing these will completely define the mesh, which is a form of graph. Numerous schemes have been invented to represent such a structure, and mainly depend on the degree of modifiability required. See next entry.

Winged edge. The winged edge is a special kind of 2D mesh representation that is particularly useful for mesh generation and mesh refinement. Essentially, the mesh edges surrounding an element face have pointers in all possible directions to all items, including nodes, faces, and other edges. Modifications of the mesh can only perform Euler operations, ensuring invariant consistency after modification.

Solid geometry. The Euler concept is also a foundation of any solid geometry representation, but now the represented object is 3-dimensional, and of various topological genus. Because only the surface of a solid object needs to be represented, a winged edge structure is also possible.

Parametrised data. Any computed solution is a set of data with discrete "tags", and typically an interpolation of the data is required (for a plot, or other reason). The tags are part of a parameter set. Generalising such a data set aids the handling of complex multidimensional data.

It is immediately clear that each data structure comes with its package of operations, which will include ways to instantiate, delete, modify, transform, and fill the data structure. It is therefore understandable that object oriented programming has become so successful, offering the programmer with a formal method of design, and a mechanism for maintaining the consistency of data.

Also of consequence are the data structures that arise from system simulation tasks. These are implicitly described by the following equations:

Linear system. This is the prototype equilibrium system. There is a complementary minimization problem associated with the linear system $A \cdot x = f$ with $A \in \mathbb{R}^{n\times n}$, $x, f \in \mathbb{R}^n$. The task is to find x that minimizes $g(x, f)$, where $g(x, f) = x^{\mathrm{T}} \cdot (A \cdot x/2 - f)$. The goal is to determine x corresponding to the loading f.

First order partial differential equation system. $A \cdot \dot{x} + B \cdot x = f$ with $A, B \in \mathbb{R}^{n\times n}$, $x, f \in \mathbb{R}^n$. The goal is to find $x[t]$ as a function of the excitation $f[t]$.

Linear time invariant system (LTI). Related to the previous entry, consider a key description popular in systems theory. $A \cdot \dot{x} + B \cdot x = f$ and $y = C \cdot x + D \cdot f$ with $A, B \in \mathbb{R}^{n\times n}$, $x, f \in \mathbb{R}^n$, $y \in \mathbb{R}^m$, and $C, D \in \mathbb{R}^{m\times n}$. The goal is to find the output $y[t]$ as a function of the excitation $f[t]$. This permits us to also define the transfer function in after Laplace transformation A.

Second order partial differential equation system. $M \cdot \ddot{x} + C \cdot \dot{x} + K \cdot x = f$ with $M, C, K \in \mathbb{R}^{n\times n}$, $x, f \in \mathbb{R}^n$. The goal is to find $x[t]$ as a function of the excitation $f[t]$. Also see Sect. 36.2.4.

Port Hamiltonian system. Many problems permit the definition of a Hamiltonian $H(x)$, so that a port-Hamiltonian system can be described with $\dot{x} = (J - R) \cdot \nabla_x H(\mathbf{x}) + B \cdot u(t)$, $y = B^{\mathrm{T}} \cdot \nabla_x H(x)$. Here $H(x) : \mathbb{R}^n \mapsto [0, \infty)$ is the Hamiltonian, $x \in \mathbb{R}^n$ the state vector, $\mathbf{y} \in \mathbb{R}^m$ is the output vector, $J = -J^{\mathrm{T}} \in \mathbb{R}^{n\times n}$ the connectivity of energy storage elements, $R = R^{\mathrm{T}} \geq 0 \in \mathbb{R}^{n\times n}$ the dissipation, and $B \in \mathbb{R}^{n\times m}$ the excitation weighting. The goal is the same as for the LTI system, and for certain manipulations such as model order reduction the structure can be preserved. Also see Sect. 36.4.2 and Eq. (36.14) of Sect. 36.2.2.

Eigensystem. The simpler eigensystem, typically arising in stability problems and first order differential equations under harmonic excitation, is prototypically written as $K \cdot x - \lambda I_n = 0$ with $K \in \mathbb{R}^{n\times n}$, $x \in \mathbb{R}^n$, $\lambda \in \mathbb{R}$, and I_n the n-dimensional identity matrix. A complimentary eigensystem arising from second order partial differential equations under harmonic excitation is $(K - \lambda M) \cdot x = 0$ with additionally $M \in \mathbb{R}^{n\times n}$. The goal is to find the eigenvectors x_i that correspond to the eigenvalues λ_i.

36.1.3 The Structure of the Chapter

The concept behind the chapter is to visualise that an analyst progresses from a mathematical description of a physical problem, to discretization and implementation of the forward problem into a numerical simulation program, after which design issues necessitate optimization, which leads to very large simulation tasks, which in turn necessitates conversion to a more efficient implementation. Because much of routine modelling and simulation is already the focus of many papers and monographs, it was thus decided to focus on three of the most challenging tasks, namely:

- the initial modelling effort, which requires considerable physical insight but which ultimately could also yield highly compact analytical solutions. The topic of levitation, which also requires concepts of control beside the considerations of the physical model;

- the optimization task, which requires a physical model and numerical discretization, before the actual optimization task and the formulation of appropriate constraints can be considered. Here fluidic and electromagnetic phenomena are considered;
- the efficiency task, for which a look at the formal methods of model order reduction is considered, which also offers an opportunity for direct integration into the discretization and optimization approaches.

These approaches or tasks thus form the contents of the following three sections.

36.2 Analytical Modeling

For the rational design of MEMS and NEMS, the analysis and investigation of their properties, as for the theoretical investigation of any other real physical system, adequate and accurate mathematical models based on differential equations describing diverse physical processes and phenomena, as well as their combinations in the designed system, are required to be developed. A mathematical model assumes to apply a certain idealization, which can never be avoided, to a system in order to simplify its true physical properties. Indeed, an enormous spectrum of physical processes occurring in MEMS and NEMS, upon applying such an idealization, can be reduced to a problem in which the space configuration of the system is completely defined by a particular limited number of *generalized coordinates* q and *generalized velocities* $\dot{q}$. In this case, differential equations can be compiled by *analytical methods*, in particular, including methods developed in analytical mechanics based on the Lagrangian and Hamiltonian formalisms, as well as *phenomenological approaches* derived in the field of energy transfer (thermodynamics, fluid mechanics, and heat transfer).

36.2.1 Introduction

Obtaining the mathematical model of the system in a form of a closed set of differential equations (DE) allows us to use the powerful apparatus of ordinary differential equations (ODE) and partial differential equations (PDE) for the model analysis and, consequently, the system under consideration. Thus, the system can be comprehensively studied both qualitatively as well quantitatively by covering its static, dynamic, and stability issues, including linear and non-linear aspects of the behaviour of the system. Developed numerical methods have been established and are widespread by means of commercially available software, as a standard tool of engineers, for designing MEMS and NEMS. However, emerging new technologies, created for further improvement of the performance of MEMS and NEMS, require new operational principles and physical phenomena to be accounted for in designing of these systems. Unfortunately, using available numerical methods will not always be successful in addressing these requirements, especially when compared with the agility of analytical methods.

For a particular case at hand, the recent progress in the technology of permanent micro-magnets [7] and 3D micro-coil fabrication [8] promotes the very promising application of electromagnetic levitation in micro-actuator systems. The stability or stable dynamics of levitating micro-actuators is the main and crucial issue requiring to be addressed at the onset of designing such actuators. In order to simultaneously solve all four types of forces, namely force, force, force, and force forces, and concomitant non-linear effects due to pull-in phenomena, mechanical contacts and impact must also be taken into account. Unfortunately, state-of-the-art multi-physics software does not offer the capability to solve such complex problems. However, a developed analytical technique based on the Lagrangian formalism [9,10] was successfully applied to a number of problems arising in inductive and hybrid levitation micro-actuators [11] related to their stability [12–14] and pull-in dynamics [15–17]. By taking into account dissipative, conservation and circulatory forces acting on a levitated micro-object, this analytical technique provides the fundamental understanding of the influence of these forces on its dynamics and stability in general, as well as its application to design a particular levitating micro-actuator.

In fact for MEMS and NEMS, due to shrinking device sizes, (especially when the size becomes comparable with the characteristic length in the material of the device,) leads to a change of the physical mechanisms of energy transport. Individual behaviors of energy carriers and their interactions with the device boundaries become more pronounced. As a result, to describe the energy transport at those scales, the classical phenomenological laws, such as the Fourier law for heat transfer and the Newton law for viscosity, are no longer applicable. In order to overcome this difficulty in the application of classical phenomenological laws at the micro and nano scales, they can be reformulated by accounting for *spatial* and *temporal* effects occurring in the transporting media [18, 19] through introducing the nonlocal (in space) and lagging (in time) behaviors in constitutive laws [20,21], and applied to study ultra-fast energy transport [22–25], also at the nano level [26–28].

36.2.2 Analytical Mechanics of MEMS

The systems which essentially couple mechanical and electromagnetic processes, and which occur at a micrometer-scale, are referred to as micro-electro-mechanical systems (MEMS). Studying such systems requires, at the beginning,

to formulate the prime assumptions, and to accept models which take into account only the essential phenomena (the major physical properties,) and neglect other phenomena of minor influence [5].

It is assumed, as usual in analytical mechanics, that the state of a mechanical part of MEMS can be modeled by n independent *generalized coordinates* $\mathbf{q} = (q_1, \ldots, q_n)$. The number of these independent coordinates is defined by constraints applied to the system, which are assumed to be holonomic and ideal [6]. For instance, let us consider a system of N point masses, which represents the mechanical part of MEMS, and this system has s holonomic constraints, then the number n of independent generalized coordinates is equal to $3N - s$. In the case of a rigid body, the number of coordinates is reduced to $6 - s$.

In order to define the state of an electromagnetic part of MEMS, the spatial distribution of vectors of the magnetic flux density $\vec{B}$ and the electric field intensity $\vec{E}$, as well their changing with time must be known. Considering the system as continuous one, the description of its state requires the application of the infinite number of time functions. However, vectors of $\vec{B}$ and $\vec{E}$ can be also modeled by means of electrical and magnetic circuits utilizing a finite number of parameters such as electrical current, voltage, magnetic flux, etc. Replacing vectors of magnetic and electric fields through these parameters is equivalent to introducing the generalized coordinates into the electromagnetic system. Let us suppose that the electromagnetic part of MEMS is represented by m electric circuits, each of them consists of the capacitor, inductor and resistor connecting in series. These electric circuits have no direct electrical connection to each of other, but of course they are coupled electromagnetically. Such the representation becomes possible if conditions of quasistationarity are hold. Also, it is assumed that a cross-section of conductor is much smaller than its length. Then, for an alternating current with relatively a high frequency, the inductance of circuit is defined by a shape of the conductor. The effect of the distribution of the current along the cross-section of the conductor on the inductance of the circuit can be neglected.

Let us denote i_k $(k = 1, 2, \ldots, m)$ as the current in the k-circuit and u_k as the electromotive force (e.m.f) applied to the k-circuit. The charges accumulated by capacitors are denoted as e_k $(k = 1, 2, \ldots, m)$ and they have the following relation with the current $\mathrm{d}e_k = i_k \mathrm{d}t$. Then, the resistor and capacitor belonged to the k-circuit are denoted as R_k and C_k, respectively. In general, the relative motion of mechanical elements of MEMS leads to changing in positions of electrodes of capacitors with respect to each other and the shape of conductors. Consequently it is assumed that the capacitor and inductor are functions of generalized coordinates, namely, $C_k = C_k(q_1, \ldots, q_n)$, $L_{kk} = L_{kk}(q_1, \ldots, q_n)$ and $L_{kr} = L_{kr}(q_1, \ldots, q_n)$, where L_{kk} is the self-inductance of the k-circuit and L_{kr} $(k \neq r)$ is the mutual inductance between the k- and r-circuit. Now, the Lagrange function of the electromechanical system can be compiled in the following form

$$L = T(q_j, \dot{q}_j) - \Pi(q_j) + W_m(q_j, i_k) - W_e(q_j, e_k), \tag{36.1}$$

where $T(q_j, \dot{q}_j)$ and $\Pi(q_j)$ are the kinetic and potential energy of the system, respectively, $W_\mathrm{m}(q_j, i_k)$ and $W_\mathrm{e}(q_j, e_k)$ are magnetic and electrical energy stored in the system, respectively. In a case of stationary constraints, the kinetic energy of the system has the quadratic form such as

$$T = \frac{1}{2} \sum_i^n \sum_j^n a_{ij} \dot{q}_i \dot{q}_j, \tag{36.2}$$

where $a_{ij} = a_{ij}(\mathbf{q}, t)$ are coefficients of inertia, depending on the generalized coordinates. The potential energy Π is also the function of the generalized coordinates, namely,

$$\Pi = \Pi(q_1, \ldots, q_n). \tag{36.3}$$

The electrical energy stored between the electrodes of capacitors can be found by the following known equation

$$W_\mathrm{e} = \frac{1}{2} \sum_k^m \frac{e_k^2}{C_k}. \tag{36.4}$$

The magnetic energy stored by the system of m-loops with electrical currents is

$$W_\mathrm{m} = \frac{1}{2} \sum_k^m \sum_r^m L_{kr} i_k i_r. \tag{36.5}$$

Besides, the energy from the system is dissipated due to Joule heating and friction. This dissipation energy can be taken into account by introducing the following function, which sums up the dissipation occurring in electrical and mechanical parts of the system, such as

$$\Psi = \Psi_\mathrm{e}(i_k) + \Psi_\mathrm{mech}(q_j, \dot{q}_j). \tag{36.6}$$

Noting that the electrical dissipation function Ψ_e is independent of the generalized coordinates and the mechanical dissipation function Ψ_mech of the currents, thus it can be concluded that

$$\frac{\partial \Psi}{\partial i_k} = \frac{\partial \Psi_\mathrm{e}}{\partial i_k}; \quad \frac{\partial \Psi}{\partial \dot{q}_j} = \frac{\partial \Psi_\mathrm{mech}}{\partial \dot{q}_j}. \tag{36.7}$$

Using Lagrangian (36.1) and dissipation function (36.6), the set of the Lagrange-Maxwell equations of electromechanical system can be obtained

$$\begin{cases} \dfrac{\mathrm{d}}{\mathrm{d}t}\left(\dfrac{\partial L}{\partial \dot{e}_k}\right) - \dfrac{\partial L}{\partial e_k} + \dfrac{\partial \Psi}{\partial \dot{e}_k} = u_k;\ k = 1, \ldots, m; \\ \dfrac{\mathrm{d}}{\mathrm{d}t}\left(\dfrac{\partial L}{\partial \dot{q}_j}\right) - \dfrac{\partial L}{\partial q_j} + \dfrac{\partial \Psi}{\partial \dot{q}_j} = Q_j;\ j = 1, \ldots, n, \end{cases} \tag{36.8}$$

where Q_j is the generalized forces applied to the system. The obtained equations are called the Lagrange-Maxwell equations. Equation (36.8) is the set of $n+m$ ordinary differential equations of the second order with respect to the generalized coordinates and charges. Worth noting that methods of analytical mechanics were developed by two physicists, namely, Joseph Louis Lagrange (1736–1813) and William Rowan Hamilton (1805–1865) in eighteenth and nineteenth centuries. In particular, in 1873 using the Lagrange approach, James Clerk Maxwell (1831–1879) derived the equations describing electromechanical systems in his famous work "A Treatise on Electricity and Magnetism" [31]. In general, set (36.8) is nonlinear because of the terms, which are defined by

$$\sum_{j}^{n}\sum_{k}^{m}\frac{\partial L_{kr}}{\partial q_j}\dot{q}_j i_k, \tag{36.9}$$

representing the induced e.m.f by moving conductors with currents. Set (36.8) includes also ponderomotive forces, which are

$$Q_j^* = \frac{\partial}{\partial q_j}\left(W_{\mathrm{m}} - W_{\mathrm{e}}\right) = \frac{1}{2}\sum_{k}^{m}\sum_{r}^{m}\frac{\partial L_{kr}}{\partial q_j} i_k i_r + \frac{1}{2}\sum_{k}^{m}\frac{\partial C_k}{\partial q_j}\frac{e_k^2}{C_k^2}. \tag{36.10}$$

Formally, ponderomotive forces arise as a result of changing the electrical and magnetic energy with the generalized coordinates. The generalized coordinates q_j determine the positions of electrodes of capacitors and wires of conductors, as well as the distribution of magnetic permeability μ and dielectric constant ε in space. For this, the different types of ponderomotive forces are responsible for the force interaction, for instance, the force interaction between wires with currents, the force interaction between charged bodies, force acting on a body due to the difference between the magnetic permeability of the body and surrounding space, etc. However, in any case, equation for ponderomotive force (36.10) is still applicable. For some treatments, it is convenient to define the state of the electromechanical system through *the generalized momentum*, which is defined as follows

$$p_j = \frac{\partial L}{\partial \dot{q}_j}, \tag{36.11}$$

and *the generalized magnetic flux* such as

$$\phi_k = \frac{\partial L}{\partial \dot{e}_k}. \tag{36.12}$$

Using the generalized momentum and magnetic flux defined by (36.11) and (36.12), respectively, the *Hamiltonian* of the system can be explicitly obtained through the Legendre transform of the *Lagrangian* such as

$$H(\mathbf{p}, \boldsymbol{\phi}, \mathbf{q}, \mathbf{e}) = \mathbf{p}\dot{\mathbf{q}} + \boldsymbol{\phi}\mathbf{i} - L(\dot{\mathbf{q}}, \mathbf{q}, \mathbf{i}, \mathbf{e}). \tag{36.13}$$

Then $n+m$ Lagrange-Maxwell equations can be equivalently represented by the set of $2(n+m)$ first-order Hamilton's equations as follows

$$\begin{cases} \dfrac{\mathrm{d}}{\mathrm{d}t}e_k = \dfrac{\partial H}{\partial \phi_k};\ k = 1, \ldots, m; \\ \dfrac{\mathrm{d}}{\mathrm{d}t}\phi_k = u_k - \dfrac{\partial H}{\partial e_k}; \\ \dfrac{\mathrm{d}}{\mathrm{d}t}q_j = \dfrac{\partial H}{\partial p_j};\ j = 1, \ldots, n; \\ \dfrac{\mathrm{d}}{\mathrm{d}t}p_j = Q_j - \dfrac{\partial H}{\partial q_j}. \end{cases} \tag{36.14}$$

36.2.3 Dynamics of Electromagnetic Levitation Micro-Systems

Electromagnetic levitation is defined as the stable or indifferent equilibrium of a body without material contact to its surrounding environment, which is reached by means of stored electromagnetic energy inducing, in turn, the ponderamotive forces acting on the levitated body and equilibrating gravitational forces. Electromechanical systems implement the principle of electromagnetic levitation on a micro-scale is referred as electromagnetic levitation micro-systems or *levitation micro-systems*.

Levitation micro-systems offer a fundamental solution to overcome the domination of friction over inertial forces at the micro-scale. This fact makes levitation micro-systems to be very attractive for their applications in micro-inertial-sensors, micro-motors, switches, micro-accelerators, particle traps, digital micro-fluidics, nano-force sensors, micro-transporters, micro-bearings, etc. There are a number of techniques, which provide the implementation of electromagnetic levitation into a micro-system and can be classified according to using materials and the sources of the force fields as follows [11]:

- Electric levitation: force interaction between dielectric and conducting materials located into electric field;
- Magnetic levitation: force interaction between magnets and direct current (dc) or magnetic materials and dc ;
- Diamagnetic levitation: force interaction between diamagnetic materials and magnet;
- Superconducting levitation: force interaction between superconducting materials and magnet;
- Inductive levitation: force interaction between conducting materials and alternating current (ac);

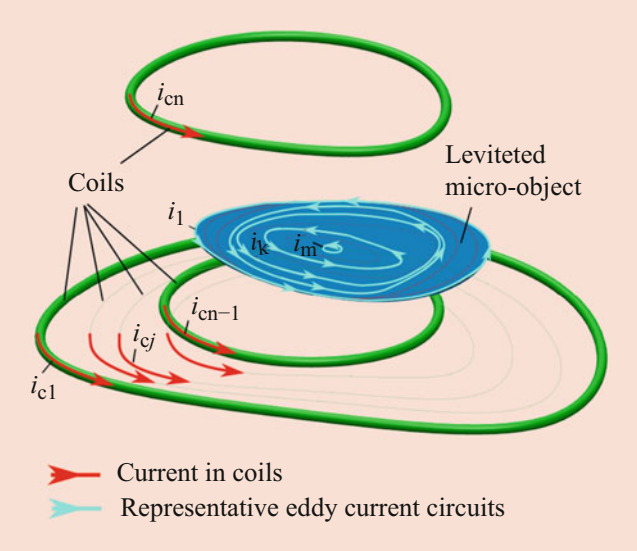


Fig. 36.2 Scheme of inductive levitation system with induced eddy current represented by the m eddy current circuits: YXZ is the fixed coordinate frame; g is the gravity acceleration directed along the Z axis; i_k is the eddy current in the k-th eddy current circuit; i_{cj} is the current in the j-coil

- Hybrid levitation: combination of different force fields.

The analysis of such levitation systems requires the application of the Maxwell equations. Although, these equations are universally applicable, but their application even for simple designs is extremely difficult task [29], which is not able to cover all required aspects of the behavior of a proposed design of the levitation system related to its stability or stable levitation and dynamics including nonlinear effects [30].

Let us consider the scheme of an inductive levitation system shown in Fig. 36.2, which consists of a system of n coils, and a levitated micro-object. Each j-th coil is fed by its own alternating current denoted by i_{cj} and generates a time-variable magnetic field in space. The alternating magnetic flux passes through the conducting micro-object and induces an eddy current. Since the density of eddy current induced within the levitated micro-object is not homogeneous, it can be assumed that the m eddy current circuits can be selectively chosen to represent the behaviour of the entire eddy current, as shown in Fig. 36.2. As seen from Fig. 36.2, i_k is the eddy current in the k-th eddy current circuit.

An equilibrium position of the levitated micro-object is characterized with respect to the fixed coordinate frame YXZ. The micro-object is considered as a rigid body. Hence its behaviour relative to the equilibrium position can be characterized in general by six generalized coordinates corresponding to three linear and three angular displacements, which can be denoted by q_l, $l = 1...6$. Let us define that coordinates, q_l, with indexes $l = 1, 2, 3$ are the generalized linear coordinates, while indexes $l = 4, 5, 6$ correspond to the generalized angular coordinates. Thus, the state of the levitation system can be described by m independent currents i_k and six independent displacements. Hence, instead of the field equations, the methods of analytical mechanics can be applied to study the system.

Adapting the generalized coordinates and the assumptions introduced above, the model of electromagnetic levitation system can be written by using the Lagrange-Maxwell equations as follows

$$\begin{cases} \dfrac{\mathrm{d}}{\mathrm{d}t}\left(\dfrac{\partial L}{\partial i_k}\right) + \dfrac{\partial \Psi}{\partial i_k} = 0; \ k = 1, \ldots, m; \\ \dfrac{\mathrm{d}}{\mathrm{d}t}\left(\dfrac{\partial L}{\partial \dot{q}_l}\right) - \dfrac{\partial L}{\partial q_l} + \dfrac{\partial \Psi}{\partial \dot{q}_l} = F_l; \ l = 1, 2, 3; \\ \dfrac{\mathrm{d}}{\mathrm{d}t}\left(\dfrac{\partial L}{\partial \dot{q}_l}\right) - \dfrac{\partial L}{\partial q_l} + \dfrac{\partial \Psi}{\partial \dot{q}_l} = T_l; \ l = 4, 5, 6, \end{cases} \tag{36.15}$$

where $L = T - \Pi + W_\mathrm{m}$ is the Lagrange function for the micro-object-coil system; $T = T(\dot{q}_1, \ldots, \dot{q}_6)$ is the kinetic energy of the system; $\Pi = \Pi(q_1, \ldots, q_6)$ is the potential energy of the system;$W_\mathrm{m} = W_\mathrm{m}(q_1, \ldots, q_6, i_{c1}, \ldots, i_{cn}, i_1, \ldots, i_m)$ is the energy stored in the electromagnetic field; $\Psi = \Psi(\dot{q}_1, \ldots, \dot{q}_6, i_1, \ldots, i_m)$ is the dissipation function; F_l ($l = 1, 2, 3$) and T_r ($l = 4, 5, 6$) are the generalized forces and torques, respectively, acting on the micro-object relative to the appropriate generalized coordinates. The kinetic energy is

$$T = \frac{1}{2}\sum_{l=1}^{3} M\dot{q}_l^{\,2} + \frac{1}{2}\sum_{l=4}^{6} J_l\dot{q}_l^{\,2}, \tag{36.16}$$

where M is the mass of the micro-object; J_l is its moment of inertia in terms of the appropriate generalized angular coordinates. The linear generalized coordinates, q_l, $l = 1, 2, 3$, are defined in the orthogonal coordinate frame. Assuming that the generalized coordinate q_3 is directed along the gravity acceleration g, as shown in Fig. 36.2, then the potential energy can be defined simply as follows

$$\Pi = Mgq_3. \tag{36.17}$$

The dissipation function is

$$\Psi = \frac{1}{2}\sum_{r=1}^{6} \mu_r\dot{q}_r^{\,2} + \frac{1}{2}\sum_{k=1}^{m} R_k i_k^2 \pm \sum_{k=1}^{m}\sum_{s=1, s\neq k}^{m} R_{ks} i_k i_s, \tag{36.18}$$

where μ_r is the damping coefficient corresponding to the appropriate generalized coordinates; R_k is the electrical resistance for the k-th eddy current circuit within the micro-object; R_{ks} is the resistance of a common circuit for k-th and s-th eddy current circuits (for example, this case is shown in Fig. 36.2 for eddy currents i_1, i_2, and i_3). For generality, it is assumed that the k-th eddy current may share a common path with the s-th eddy current. The plus-minus sign corresponds

to eddy currents having the same or opposite direction on the common circuit. The energy stored within the electromagnetic field can be written as

$$W_{\mathrm{m}}=\frac{1}{2}\sum_{j=1}^{n}\sum_{s=1}^{n}L_{js}^{\mathrm{c}}i_{\mathrm{c}j}i_{\mathrm{c}s}+\frac{1}{2}\sum_{k=1}^{m}\sum_{s=1}^{m}L_{ks}^{\mathrm{o}}i_k i_s+\frac{1}{2}\sum_{k=1}^{m}\sum_{j=1}^{n}M_{kj}i_k i_{\mathrm{c}j}, \tag{36.19}$$

where L_{jj}^{c} is the self inductance of the j-coil; L_{js}^{c}, $j \neq s$ is the mutual inductance between j- and s-coils; $L_{kk}^{\mathrm{o}} = L_{kk}^{\mathrm{o}}(q_1, \ldots, q_6)$ is the self inductance of the k-eddy current circuit; $L_{ks}^{\mathrm{o}} = L_{ks}^{\mathrm{o}}(q_1, \ldots, q_6)$, $k \neq s$ is the mutual inductance between k- and s-eddy current circuits; $M_{kj} = M_{kj}(q_1, \ldots, q_6)$ is the mutual inductance between the k-eddy current circuit and the j-coil.

The induced eddy currents i_k can be expressed in terms of coil currents $i_{\mathrm{c}j}$ under a particular condition discussed below. Assuming that for each coil, the current $i_{\mathrm{c}j}$ is a periodic signal with an amplitude of $I_{\mathrm{c}j}$ at the same frequency ω, we can write

$$i_{\mathrm{c}j} = I_{\mathrm{c}j}e^{\jmath\omega t}, \tag{36.20}$$

where $\jmath = \sqrt{-1}$. Taking the derivative of the Lagrange function with respect to the eddy current i_k, we have:

$$\frac{\partial L}{\partial i_k} = \frac{\partial W_m}{\partial i_k} = \sum_{s=1}^{m} L_{ks}^{\mathrm{o}} i_s + \sum_{j=1}^{n} M_{kj} i_{cj}, \tag{36.21}$$

or

$$\frac{\partial L}{\partial i_k} = \frac{\partial W_m}{\partial i_k} = L_{kk}^{\mathrm{o}} i_k + \sum_{s=1,\ s\neq k}^{m} L_{ks}^{\mathrm{o}} i_s + \sum_{j=1}^{n} M_{kj} i_{cj}. \tag{36.22}$$

Substituting (36.22) into (36.15), the first equation of set (36.15) becomes

$$\begin{aligned}\frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{\partial L}{\partial i_k}\right)+\frac{\partial \Psi}{\partial i_k} &= \sum_{r=1}^{6}\frac{\partial L_{kk}^{\mathrm{o}}}{\partial q_r}\frac{\mathrm{d}q_r}{\mathrm{d}t}i_k + L_{kk}^{\mathrm{o}}\frac{\mathrm{d}i_k}{\mathrm{d}t}\\ &+\sum_{s=1,\ s\neq k}^{m}\left(\sum_{r=1}^{6}\frac{\partial L_{ks}^{\mathrm{o}}}{\partial q_r}\frac{\mathrm{d}q_r}{\mathrm{d}t}i_s + L_{ks}^{\mathrm{o}}\frac{\mathrm{d}i_s}{\mathrm{d}t}\right)\\ &+\sum_{j=1}^{n}\left(\sum_{r=1}^{6}\frac{\partial M_{kj}}{\partial q_r}\frac{\mathrm{d}q_r}{\mathrm{d}t}i_{cj} + M_{kj}\frac{\mathrm{d}i_{cj}}{\mathrm{d}t}\right) + R_k i_k\\ &\pm\sum_{s=1,\ s\neq k}^{m} R_{ks}i_s = 0.\end{aligned} \tag{36.23}$$

Accounting for (36.20), the k-eddy current can be represented as

$$i_k = I_k \mathrm{e}^{\jmath\omega t}, \tag{36.24}$$

where I_k is the amplitude. Hence, Eq. (36.23) can be rewritten in term of the current amplitudes as follows

$$\begin{aligned}&\sum_{r=1}^{6}\frac{\partial L_{kk}^{\mathrm{o}}}{\partial q_r}\frac{\mathrm{d}q_r}{\mathrm{d}t}I_k + L_{kk}^{\mathrm{o}}\jmath\omega I_k\\ &+\sum_{s=1,\ s\neq k}^{m}\left(\sum_{r=1}^{6}\frac{\partial L_{ks}^{\mathrm{o}}}{\partial q_r}\frac{\mathrm{d}q_r}{\mathrm{d}t}I_s + L_{ks}^{\mathrm{o}}\jmath\omega I_s\right)\\ &+\sum_{j=1}^{n}\left(\sum_{r=1}^{6}\frac{\partial M_{kj}}{\partial q_r}\frac{\mathrm{d}q_r}{\mathrm{d}t}I_{\mathrm{c}j} + M_{kj}\jmath\omega I_{\mathrm{c}j}\right)\\ &+R_k I_k \pm\sum_{s=1,\ s\neq k}^{m} R_{ks}I_s = 0.\end{aligned} \tag{36.25}$$

Analysis of Eq. (36.25) shows that due to the velocities of generalized coordinates, $\mathrm{d}q_r/\mathrm{d}t$ the equation is nonlinear. However, the velocity of the levitated micro-object in microsystems is not essential factor and its value is as usually small enough that the velocity $\mathrm{d}q_r/\mathrm{d}t$ can be neglected. Moreover, the frequency ω is commonly larger than 1 MHz, which corresponds to $\sim 10^7$ rad/s. Hence, Eq. (36.25) can be rewritten [32] as follows

$$\left(L_{kk}^{\mathrm{o}}+R_k/(\jmath\omega)\right)I_k + \sum_{s=1,\ s\neq k}^{m}(L_{ks}^{\mathrm{o}} \pm R_{ks}/(\jmath\omega))I_s = -\sum_{j=1}^{n} M_{kj}I_{\mathrm{c}j}. \tag{36.26}$$

The later equation provides the linear relationship between coils and eddy currents. Solving Eq. (36.26) by the Cramer rule, set (36.15) of m+6 equations is reduced to six equations. Hence, the behavior of the suspension is defined only by the generalized coordinates of its mechanical part. Thus,

$$\begin{cases} M\ddot{q}_l + \mu_l\dot{q}_l - \dfrac{\partial W_{\mathrm{m}}}{\partial q_l} = F_l;\ \ l = 1, 2;\\ M\ddot{q}_3 + \mu_3\dot{q}_3 + mg - \dfrac{\partial W_{\mathrm{m}}}{\partial q_3} = F_3;\\ J_l\ddot{q}_l + \mu_l\dot{q}_l - \dfrac{\partial W_{\mathrm{m}}}{\partial q_l} = T_l;\ \ l = 4, 5, 6, \end{cases} \tag{36.27}$$

Assuming that the displacements are small, set (36.27) can be linearized near an equilibrium point. Hence, model (36.27) becomes

$$\begin{cases} M\ddot{q}_l + \mu_l\dot{q}_l + \sum\limits_{r}^{6}\bar{c}_{lr}q_r = F_l;\ \ l = 1, 2, 3;\\ J_l\ddot{q}_l + \mu_l\dot{q}_l + \sum\limits_{r}^{6}\bar{c}_{lr}q_r = T_l;\ \ l = 4, 5, 6, \end{cases} \tag{36.28}$$

where $\bar{c}_{l0}$ and $\bar{c}_{lr}$ $(l, r = 1, \ldots, 6)$ are complex coefficients analytically defined by expanding (36.19) into the Taylor series. Noting that the imaginary part of $\bar{c}_{lr}$ is due to the resistance, R, of the levitated micro-object. At the equilibrium point, the following coefficients must hold:

$$\bar{c}_{30} = -Mg;\ \ \bar{c}_{l0} = 0;\ \ l = 1, 2, 4, 5, 6. \tag{36.29}$$

The obtained dynamical model of a levitation system (36.28) based on the assumption of the discretization of the induced eddy current into a levitation object implements, on the one hand, naturally the concept of model order reduction (the details of the concept are provided below in Sect. 1.5). On the other hand, using Eq. (36.26) an optimization problem about the shape of the levitated object, which provides, for instance, the minimum value of the excitation current into the coils necessary for its levitation can be defined. At the same time the optimistation must be preformed under the constrains related to the condition of stability, which also is dependent on the shape of the excitation coils. Thus, the topology optimization problem (other details are given in Sect. 1.3) of the distribution material of the levitated object for a particular design of the excitation coils is arisen.

36.2.4 Stability of Electromagnetic Levitation Micro-Systems

Let us write linear model (36.28) in a matrix form as

$$\underline{A}\ddot{\underline{q}} + \underline{B}\dot{\underline{q}} + \left(\underline{R} + \jmath\underline{P}\right)\underline{q} = f, \tag{36.30}$$

where $\underline{q} = [\overline{q}_1 \ \ldots \ \overline{q}_6]^{\mathrm{T}}$ is the column-matrix of generalized coordinates, which are complex variables due to (36.28); $\underline{f} = [F_1 \ F_2 \ F_3 \ T_4 \ T_5 \ T_6]^{\mathrm{T}}$ is the column-matrix of generalized forces and torques applied to the micro-object; $\underline{A} = \mathrm{diag}[m \ m \ m \ J_4 \ J_5 \ J_6]$ is the diagonal matrix of the micro-object mass and its moments of inertia; $\underline{B} = \mathrm{diag}[\mu_1 \ \ldots \ \mu_6]$ is the diagonal matrix of damping coefficients; $\underline{R} = [\mathrm{Re}\{\overline{c}_{lr}\}]$ and $\underline{P} = [\mathrm{Im}\{\overline{c}_{lr}\}]$.

The physical meanings of matrices $\underline{A}$, $\underline{B}$ and $\underline{R}$ are obvious. While, matrix $\underline{P}$ presents the coefficients of *circulatory forces* (the nonconservative positional forces) due to the dissipation of eddy current. Equation (36.30) can be rewritten by using only real values, and at the equilibrium point the linear model is equivalent to

$$\left[\begin{array}{c|c} \underline{A} & \underline{0} \\ \hline \underline{0} & \underline{A} \end{array}\right]\left[\begin{array}{c} \ddot{\underline{q}} \\ \hline \ddot{\underline{q}}* \end{array}\right] + \left[\begin{array}{c|c} \underline{B} & \underline{0} \\ \hline \underline{0} & \underline{B} \end{array}\right]\left[\begin{array}{c} \dot{\underline{q}} \\ \hline \dot{\underline{q}}* \end{array}\right] + \left[\begin{array}{c|c} \underline{R} & -\underline{P} \\ \hline \underline{P} & \underline{R} \end{array}\right]\left[\begin{array}{c} \underline{q} \\ \hline \underline{q}* \end{array}\right] = 0, \tag{36.31}$$

where $[q|q*]^{\mathrm{T}}$ is the block column-vector of twelve variables; $q = \mathrm{Re}\{\overline{q}\}$, $q* = \mathrm{Im}\{\overline{q}\}$, $\underline{0}$ is a zero matrix and all block matrices have 12×12 elements. It is visible that

$$\left[\begin{array}{c|c} \underline{R} & -\underline{P} \\ \hline \underline{P} & \underline{R} \end{array}\right] = \left[\begin{array}{c|c} \underline{R} & \underline{0} \\ \hline \underline{0} & \underline{R} \end{array}\right] + \left[\begin{array}{c|c} \underline{0} & -\underline{P} \\ \hline \underline{P} & \underline{0} \end{array}\right], \tag{36.32}$$

and

$$\left[\begin{array}{c|c} \underline{0} & -\underline{P} \\ \hline \underline{P} & \underline{0} \end{array}\right] = -\left[\begin{array}{c|c} \underline{0} & -\underline{P} \\ \hline \underline{P} & \underline{0} \end{array}\right]^{\mathrm{T}} \tag{36.33}$$

is a skew-symmetric matrix which corresponds to the positional nonconservative forces.

Analysis of model (36.30) reveals the following general issues related to stability of inductive levitation micro-systems, which are in particular formulated in terms of three theorems.

Theorem 1 (Unstable Levitation I) *If a inductive levitation micro-system is subjected to only electromagnetic forces defined by (36.19) (without dissipation forces, so that $\underline{B} = 0$), then stable levitation in the micro-system is impossible.*

This theorem can be referred to the main feature of inductive levitation systems. However, if the levitating micro-object is a perfect conductor, then $\underline{P} = 0$. Hence, when matrix $\underline{R}$ is the positive definite matrix, stable levitation without dissipative forces becomes possible. Also another conclusion can be formulated in the following corollary.

Corollary 1.1 *If a micromachined inductive levitation system is subjected to only electromagnetic forces, and the potential part of the electromagnetic forces is absent ($\underline{R} = 0$), then stable levitation in the system is impossible.*

Even if the dissipative forces are added to such a system without potential forces, the stable levitation is still impossible, this fact can be formulated in the second theorem below.

Theorem 2 (Unstable Levitation II) *If a micromachined inductive levitation system is subjected to electromagnetic forces having only positional $\underline{P} \neq 0$ ($\underline{R} = 0$) and dissipative forces ($\underline{B} > 0$), then stable levitation is impossible.*

The stable inductive levitation can be only achieved by adding the dissipative force. Upon holding the following necessary and sufficient conditions given in the theorem below, the system can be asymptotically stable.

Theorem 3 (Asymptotically Stable Levitation) *By adding dissipative forces ($\underline{B} > 0$) to a micromachined inductive levitation system subjected to electromagnetic forces defined by (36.19) and having a positive definite matrix of potential forces ($\underline{R} > 0$), the system can be asymptotically stable.*

The necessary condition is that matrix $\underline{A}$, $\underline{B}$ and $\underline{R}$ should be positive definite. The condition follows from the statement of the theorem. According to Metelitsyn's inequality [33,34, page 32], a sufficient practical condition for asymptotically stable levitation for the present case becomes as follows

$$\mu_{\min} > p_{\max}\sqrt{a_{\max}/r_{\min}}, \tag{36.34}$$

where $\mu_{\min}$, and $r_{\min}$ are the respective minimum values of $\underline{B}$ and $\underline{R}$; $p_{\max}$ and $a_{\max}$ are the respective maximum values of $\underline{P}$ and $\underline{A}$.

Operating levitation micro-systems in air, inequality (36.34) automatically holds due to the fact that damping

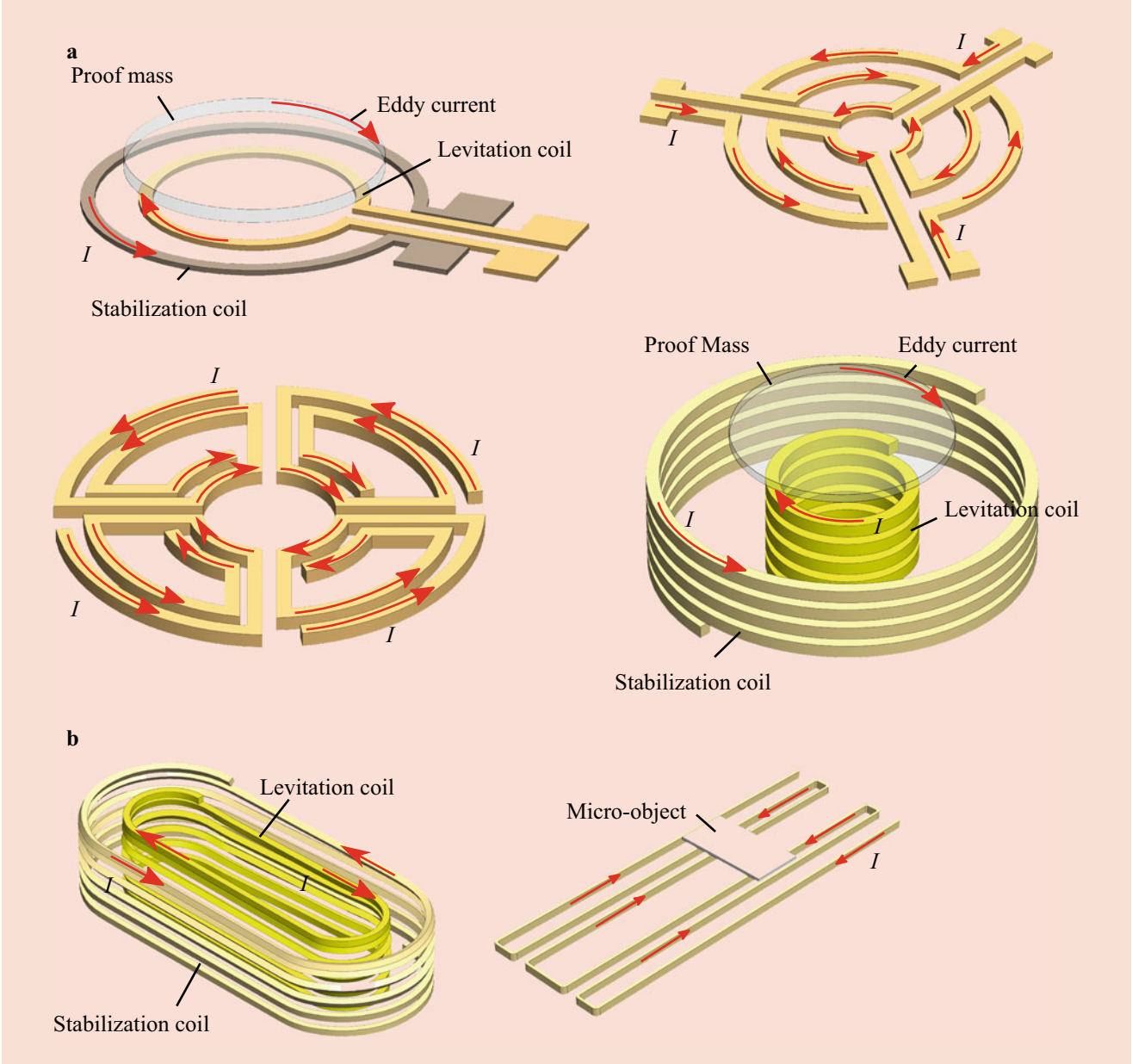


Fig. 36.3 Different designs based on planar and 3D micro-coils: (**a**) axially symmetric and (**b**) symmetric designs (I is the electric current)

forces dominate in the micro-world. Note that inequality (36.34) should be separately verified upon using levitation micro-systems in a vacuum environment.

Application

The analytical approach developed above can be applied to analyze the dynamics and stability of symmetric and axially symmetric designs of micromachined levitation micro-actuators as shown in Fig. 36.3. Due to the symmetry in the considered designs, the number of equations in set (36.28) can be reduced. Structures of their analytical models are obtained as shown in Table 36.1.

It can be proposed the following procedure for designing levitation micro-systems. If the system is intended for using in air, the application of the developed approach is reduced to the analysis of the coefficients of matrix $\underline{R} = (\mathrm{Re}\{\overline{c}_{lr}\})$, whose elements are defined in (36.29) as functions of the design parameters. A result of this analysis would be to find the domains of these design parameters where the matrix $\underline{R} > 0$ is positive definite, or to demonstrate that such domains do not exist ($\underline{R} < 0$ is everywhere negative definite). Additionally, for a vacuum environment, it becomes necessary to define the coefficients of the matrix $\underline{P} = (\mathrm{Im}\{\overline{c}_{lr}\})$, which give the required values of the damping coefficients, μ_{r}, in order to fulfill the condition for stable levitation as defined in Theorem 3.

Table 36.1 The structures of the analytical models of the levitation micro-systems as a function of design

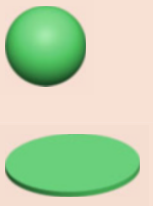
Design	Levitating micro-object	Model Structure
Axially symmetric		$\begin{cases} M\ddot{q}_v+\mu_v\dot{q}_v+\bar{c}_{vv}q_v=F_v; \\ M\ddot{q}_1+\mu_1\dot{q}_1+\bar{c}_{11}q_1=F_1. \end{cases}$ $\begin{cases} M\ddot{q}_v+\mu_v\dot{q}_v+\bar{c}_{vv}q_v=F_v; \\ M\ddot{q}_1+\mu_1\dot{q}_1+\bar{c}_{11}q_1+\bar{c}_{1\theta}\theta=F_1; \\ J_\theta\ddot{\theta}+\mu_\theta\dot{\theta}+\bar{c}_{\theta 1}q_1+\bar{c}_{\theta\theta}\theta=T_\theta. \end{cases}$
Symmetric		$\begin{cases} M\ddot{q}_v+\mu_v\dot{q}_v+\bar{c}_{vv}q_v=F_v; \\ M\ddot{q}_1+\mu_1\dot{q}_1+\bar{c}_{11}q_1+\bar{c}_{1\alpha}\alpha=F_1; \\ J_\alpha\ddot{\alpha}+\mu_\alpha\dot{\alpha}+\bar{c}_{\alpha l}q_l+\bar{c}_{\alpha\alpha}\alpha=T_\alpha; \\ J_\beta\ddot{\beta}+\mu_\beta\dot{\beta}+\bar{c}_{\beta\beta}\beta=T_\beta. \end{cases}$

Table 36.2 Comparison of suspension stiffness from modelling and experiment results

Stiffness component	Measured values reported in [35]	Modelling reported in [35]	Analytical modelling
Lateral, ($N{\cdot}m^{-1}$)	3.0×10^{-3}	3.0×10^{-3}	2.0×10^{-3}
Vertical, ($N{\cdot}m^{-1}$)	4.5×10^{-2}	4.2×10^{-2}	4.5×10^{-2}
Angular, ($m{\cdot}N{\cdot}rad^{-1}$)	1.5×10^{-8}	0.8×10^{-8}	1.4×10^{-8}

The micromachined levitation actuator design based on 3D micro-coils shown in Fig. 36.4a is analyzed. Let us assume that the actuator is operated in air. Hence, the elements of the matrix (see, Table 36.1) will be defined as functions of the design parameters [9, 10, 35]. Thus, d is the difference between the radius of the disk-shaped proof mass and the radius of the levitation coil, and h is the levitation height. The same design of 3D micromachined levitation actuator and the experimental parameters given in [35]: the radii of the stabilization and levitation coils are 1.9 mm and 1.0 mm, respectively; the pitch of coil winding is 25 μm ; the number of windings for the stabilization and levitation coils are 12 and 20, respectively; the radius of the proof mass is 1.6 mm are used.

For an excitation current of 109 mA in both coils, the maps of the stiffness coefficients are shown in Fig. 36.4. The results of the modelling are shown in Table 36.2 together with experimental ones published in [35] in order to enable the direct comparison. The analysis of Table 36.2 shows that the developed technique allows us to evaluate the stiffness with a good enough accuracy.

36.2.5 Phenomenological Model of Heat Transfer in Hard-Disk Air Bearing

To achieve higher areal density, a flying height of air bearing is required to be significantly reduced to a few nanometers. For instance, to support areal density 10 Tbit in^{-2}, the flying height has to be less than 4 nm. Thus, heat transfer processes between a slider and disk surface in hard disk drives (HDD) becomes an extremely important issue. Recently, the Thermal Fly-height Control (TFC) technology has been developed to provide such a nano-scale flying height [36, 37]. In TFC technology, a microheater embedded in-situ slider is used to control the protrusion and gap by means of measuring Joule heating current. Moreover, a nano-level slider-disk gap leads to a thermal deformation of the slider's air bearing surface as well as air bearing cooling affect which have a great influence on a performance of HDD [38, 39]. Thus, it becomes a very important to accurately describe heat transfer in hard-disk air bearing, in order to provide further HDD improvement.

To solve this issue, a number of models were developed and discussed in the literature. The analytical heat transfer model in a thin slider/disk air bearing based on the reduced Navier-Stokes equation with velocity slip and temperature jump boundary conditions was proposed by S. Zhang and D.B. Bogy as reported in [40]. Then the result of Zhang's work was extended by Chen et al. accounting for the pressure gradient and their model agreed well with experiment for the flying heights of air bearing between 80 and 100 nm [41].

Worth noting that in mentioned above studies, bulk values of thermal conductivity and viscosity were assumed to be constant. However, this fact is in contradiction with reality. This point was reflected in the continuum model based on the assumption of the nonlocal behavior in air molecule heat transport in the slider/disk interface developed by Poletkin and Kulish in [28, 42].

Nonlocal Behavior in Air Molecule: Governing Equation in Air Bearing

Schematic of slider/disk interface is shown in Fig. 36.5a. A part of disk moves with a linear speed, U, relative to the slider as shown in the scheme. The spacing between the head of slider and the surface of disk is defined by variable, s. In this analysis, the slider/disk interface can be idealized as a channel between two boundary plates, in which air flow moves along these plates. Assuming that the top plate is

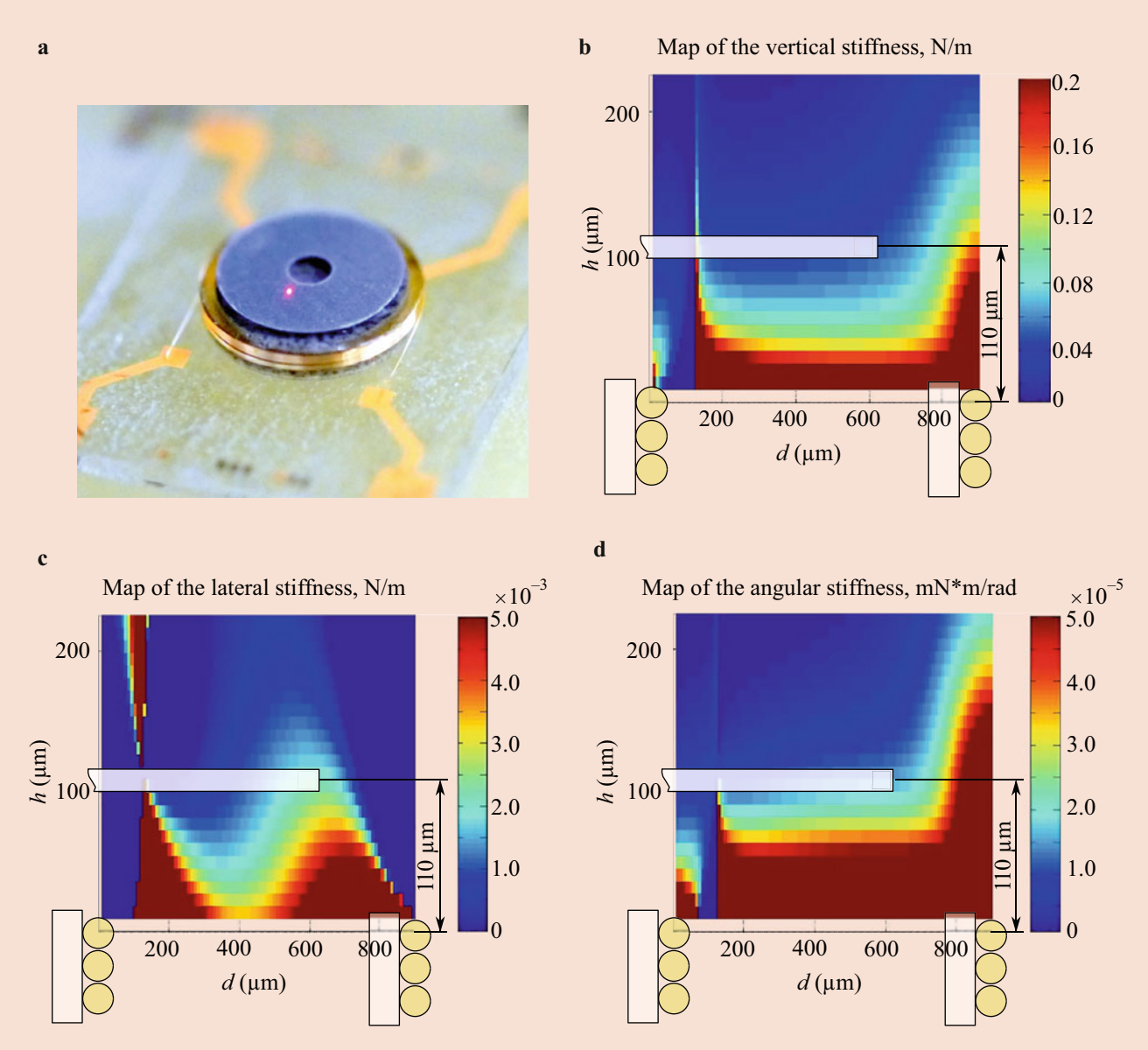


Fig. 36.4 (**a**) Axially symmetric 3D micromachined levitation actuator; (**b**) Map of angular stiffness as a function of d and levitation height, h; (**c**) Map of the vertical stiffness; (**d**) Map of the lateral stiffness

movable and a positive pressure gradient with respect to the y axis is applied as shown in Fig. 36.5b. We consider in this analysis a steady state; hence, time dependent terms in the related equations disappear. Assuming the nonlocal behavior (in space) in air molecular gas due to its scattering from the boundaries of the domain through which air flow is moved, we can write the following equations similar to the Fourier law along the x axis:

$$q''(s + l_q, x) = -k\frac{\partial T}{\partial x}, \tag{36.35}$$

and Newton's law of viscosity:

$$\varphi(s + l_\varphi, x) = \mu\frac{\partial u}{\partial x}, \tag{36.36}$$

where q'' is the heat flux, T is the temperature, l_q is the length measuring the nonlocality of the heat flux, k is the bulk value of the thermal conductivity of air, φ is the shearing stress, u is the y axis component of air flow velocity, μ is the bulk value of the dynamic viscosity of air, l_φ is the length measuring the nonlocality of the shearing stress, s is the size of the domain along the x axis through which air flow is moved. Equations (36.35) and (36.36) are the primary assumption.

The reduced Navier-Stokes equation [40] for two dimension problem can be written as follows:

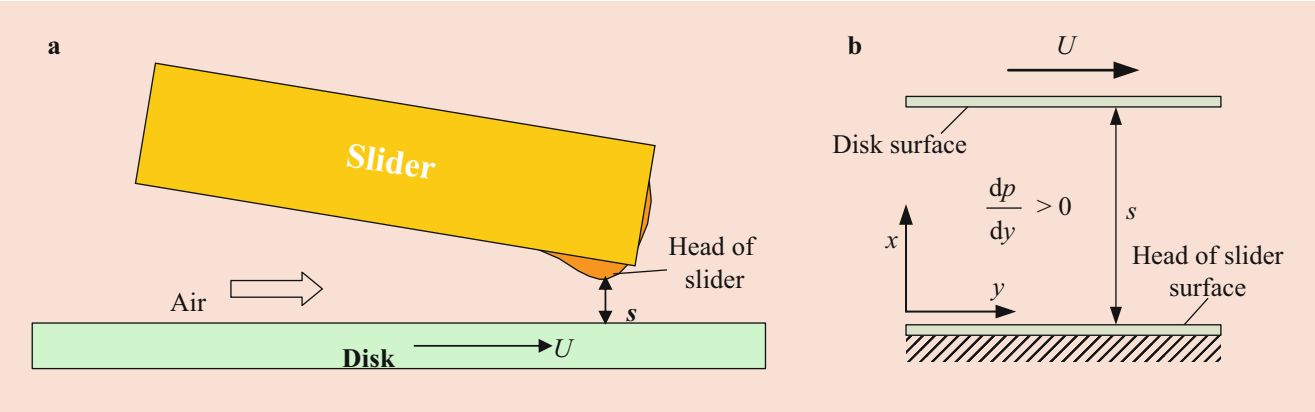


Fig. 36.5 (**a**) Schematic of slider/disk interface: U is the linear speed of the disk with regard to the slider; s is the spacing between the head of slider and the disk surface; (**b**) The slider/disk system idealization and coordinate

$$\frac{\mathrm{d}p}{\mathrm{d}y} = \frac{\partial \varphi}{\partial x}, \tag{36.37}$$

$$\frac{\mathrm{d}p}{\mathrm{d}x} = 0, \tag{36.38}$$

where p is the pressure. Using the result of analysis for the energy equation conducted in [40], and accounting for Eq. (36.36), the general form of the energy equation can be written as follows:

$$\frac{\partial q''_{\mathrm{v}}}{\partial x} + \varphi(s,x)\left(\frac{\partial u}{\partial x}\right) = 0, \tag{36.39}$$

where q''_{v} is the heat flux due to the viscous dissipation. Assuming that the nonlocal behavior in air molecular gas exists in the immediate vicinity of the interest point at s, hence Eqs. (36.35) and (36.36) can be expanded into the Taylor series containing the first order effects in l_{q} and l_{φ} are as follows

$$q''(s,x) + l_{\mathrm{q}}\frac{\partial q''(s,x)}{\partial s} = -k\frac{\partial T}{\partial x}, \tag{36.40}$$

$$\varphi(s,x) + l_{\varphi}\frac{\partial \varphi(s,x)}{\partial s} = \mu\frac{\partial u}{\partial x}. \tag{36.41}$$

Gradients of temperature and velocity are assumed to be constant against the change of the domain size, s. The physical meaning for this assumption can be supported by the following analysis of conservation laws applied to the one-dimensional case. For energy conservation, we have

$$-\frac{\partial q''(s+l_{\mathrm{q}},x)}{\partial x} = c_p\rho\frac{\partial T}{\partial t}, \tag{36.42}$$

where c_p is the specific heat, ρ is the density. Since we study the steady state process, the derivative of T with respect to time is eliminated. Hence, Eq. (36.42) can be rewritten as the deferential equation of the first order:

$$\frac{\partial q''(s+l_{\mathrm{q}},x)}{\partial x} = 0. \tag{36.43}$$

The solution of the last equation is

$$q''(s+l_{\mathrm{q}},x) = C, \tag{36.44}$$

where C is the constant. Assuming that l_{q} is small, Eq. (36.44) becomes

$$q''(s,x) + l_{\mathrm{q}}\frac{\partial q''(s,x)}{\partial s} = C. \tag{36.45}$$

Applying to (36.45) boundary condition $q''(0,x) = 0$, solution of Eq. (36.45) is

$$q''(s,x) = C\left(1 - \mathrm{e}^{-s/l_{\mathrm{q}}}\right). \tag{36.46}$$

On the other hand, substituting (36.35) into (36.44), we come to conclusion that $C = -k\dfrac{\partial T}{\partial x}$. Hence, heat transport due to the nonlocal behavior in air molecular gas becomes

$$q''(s,x) = -k\frac{\partial T}{\partial x}\left(1 - \mathrm{e}^{-s/l_{\mathrm{q}}}\right). \tag{36.47}$$

For momentum conservation law, we have

$$-\frac{\partial \varphi(s+l_{\varphi},x)}{\partial x} = \rho\frac{\partial u}{\partial t}. \tag{36.48}$$

Then, applying the same analysis conducted above to (36.48), we obtain the equation for shear stress in air due to the nonlocal behavior as follows

$$\varphi(s,x) = \mu\frac{\partial u}{\partial x}\left(1 - \mathrm{e}^{-s/l_{\varphi}}\right). \tag{36.49}$$

Now, let us define functions $k_{\mathrm{eff}}(s)$ and $\mu_{\mathrm{eff}}(s)$, as

$$k_{\text{eff}}(s) = k\left(1 - \mathrm{e}^{-s/l_{\text{q}}}\right), \tag{36.50}$$

$$\mu_{\text{eff}}(s) = \mu\left(1 - \mathrm{e}^{-s/l_{\varphi}}\right). \tag{36.51}$$

Taking into account (36.50) and (36.51), Eqs. (36.47) and (36.49) can be rewritten in the similar to the Fourier and Newton laws forms as

$$q''(s,x) = -k_{\text{eff}}(s)\frac{\partial T}{\partial x}, \tag{36.52}$$

$$\varphi(s,x) = \mu_{\text{eff}}(s)\frac{\partial u}{\partial x}, \tag{36.53}$$

where k_{eff} and μ_{eff} are size dependent the effective conductivity and dynamic viscosity. Thus, Eqs. (36.52) and (36.53) represent phenomenological models for heat transport and shear stress in assuming the nonlocal behavior (in space) in air molecular gas due to its scattering from the boundaries of the domain through which air flow is moved. Finally, combining Eq. (36.53) with (36.39), the energy equation can be rewritten as

$$\frac{\partial q''_{\text{v}}}{\partial x} + \mu_{\text{eff}}(s)\left(\frac{\partial u}{\partial x}\right)^2 = 0. \tag{36.54}$$

Let us consider the heat flux due to the viscous dissipation for the case of Couette and Poiseuille flows. In this case, the velocity distribution can be obtained by direct integrating reduced Navier-Stokes Eq. (36.37) with accounting for (36.53). For the following boundary conditions such as $u(s) = U$ and $u(0) = 0$, accounting for the pressure gradient $\mathrm{d}p/\mathrm{d}y$ is constant, the velocity distribution becomes

$$u = \frac{U}{s}x - \frac{s^2}{2\mu_{\text{eff}}}\left[\frac{x}{s} - \left(\frac{x}{s}\right)^2\right]\frac{\mathrm{d}p}{\mathrm{d}y}. \tag{36.55}$$

It is worth to note that Eq. (36.55) is the similar to classical result of velocity distribution due to Couette and Poiseuille flows between two parallel plates.

The net heat transfer between the two bounding surfaces, in particular, due to the Couette flow can be computed by subtracting viscous heating terms from the heat conduction term:

$$q''_{\text{n}} = \frac{k_{\text{eff}}}{s}\left(T_{\text{s}} - T_{\text{d}}\right) - \mu_{\text{eff}}\frac{U^2}{s}, \tag{36.56}$$

where T_{s} and T_{d} are surface temperatures of the slider and disk, respectively. Thus, Eq. (36.56) is the phenomenological model of heat transfer in hard-disk air bearing based on the nonlocal behavior in air molecular gas.

The nonlocal length, l_{q}, is corresponded to the back-scattering process of air molecules from the boundary surfaces of the plates [21]. At the same time, the energy transfer of this process has the wave nature, which can be defined by the propagation of thermal waves [43]. Hence, the nonlocal length becomes the same as the characteristic length traveled by the thermal wave [27]. Applying the same reasoning to define the nonlocal length, l_{φ}, via the wave nature of the energy transfer, the nonlocal lengths can by defined as

$$l_{\text{q}} = \frac{3k}{c_p\rho c} = 3\frac{\alpha}{c} = 3l, \tag{36.57}$$

$$l_{\varphi} = \frac{3\mu}{\rho c} = 3\frac{\nu}{c} = 3\frac{\text{Pr}\cdot\alpha}{c} = 3\text{Pr}\cdot l, \tag{36.58}$$

where c is the speed of sound in air, α is the air thermal diffusivity, ν is the air kinematic viscosity, Pr is the Prandtl number, l is the mean free path of air molecule.

Discussion

Let us compare the developed model (36.56) with known ones, namely, based on temperature jump theory by Znang and Bogy [40], kinematic theory by Shen and Chen [44], Monte Carlo simulation by Ju [45]. To do so, model (36.56) in the non-dimensional form is represented. Employing (36.57) and (36.58), and accounting for the relationship between conductivity and dynamic viscosity of air, $k = 15/4\ \mu R$, we have

$$Q_{\text{n}} = \frac{lq''_{\text{n}}}{k\Delta T} = \frac{1 - \exp\left(-\frac{D}{3}\right)}{D} - \frac{4}{15}\frac{1 - \exp\left(-\frac{D}{3\text{Pr}}\right)}{D}\widetilde{U}^2, \tag{36.59}$$

where $\Delta T = T_{\text{s}} - T_{\text{d}}$, $D = s/l$ is the inverse Knudsen number, $\widetilde{U} = U/\sqrt{R\Delta T}$, R is the gas constant, $\widetilde{p} = (lp)/(\mu\sqrt{R\Delta T})$, $\widetilde{y} = y/s$. Hence, the contribution in heat transfer between the slider and disk surface in HDD due to heat conduction is defined by

$$Q' = \frac{1 - \exp\left(-\frac{D}{3}\right)}{D}. \tag{36.60}$$

Consequently, the contribution in heat transfer between the slider and disk surface in HDD due to the viscous dissipation for Couette and Poiseuille flows are as follow

$$Q''_{\text{c}} = \frac{4}{15}\frac{1 - \exp\left(-\frac{D}{3\text{Pr}}\right)}{D}. \tag{36.61}$$

Results of comparison of the different models with nonlocal one are shown in Fig. 36.6a, b. Analysis of Fig. 36.6a, b reveals that the new model prediction for heat conduction agrees well with known models namely based on Boltzmann equation and the temperature jump theory. For the viscous dissipation due to Couette flow, the nonlocal model prediction qualitatively agrees with models base on Boltzmann equation and Monte Carlo simulation. The nonlocal model agrees quantitatively well with model based on Monte Carlo simulation, the difference is less than 7%.

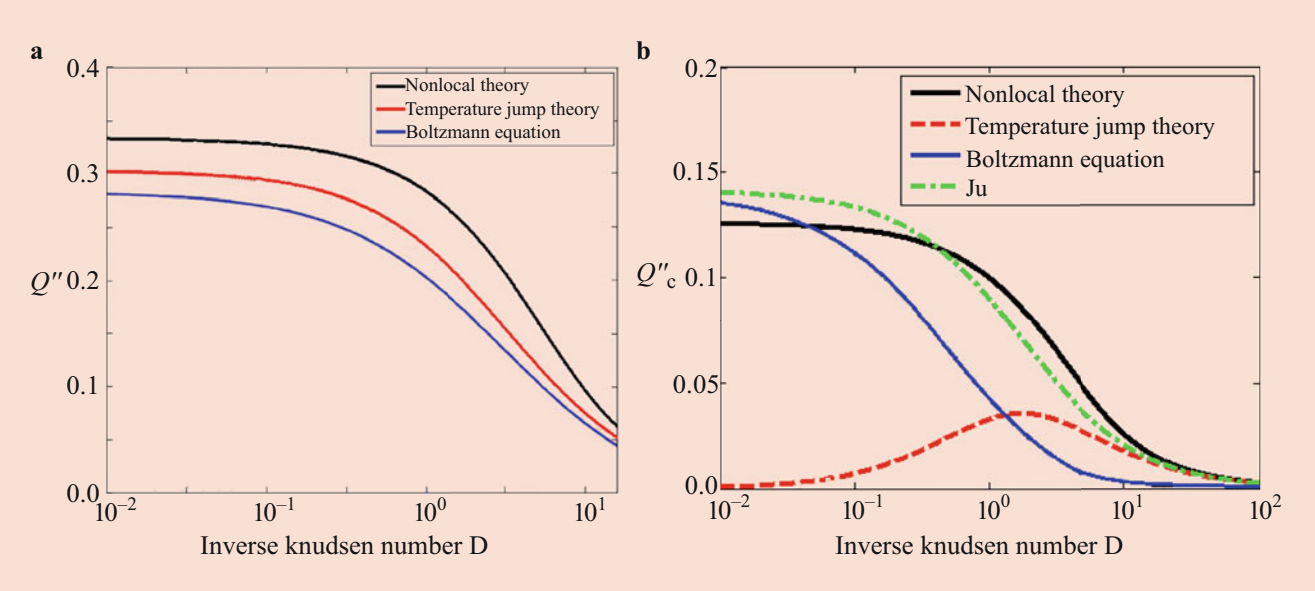


Fig. 36.6 (**a**) Comparison of Q'', representing heat conduction between two parallel plate obtained from nonlocal theory with other existing solutions; (**b**) Comparison of Q''_c, representing viscous dissipation due to Couette flow between two parallel plate obtained from nonlocal theory with other existing solutions

36.3 Topology Optimization

Topology optimization is currently regarded to be the most robust methodology for the inverse determination of material distribution in the structures that meet given structural performance criteria. It can provide a powerful approach for inverse design of micro-/nano-structures in the areas of and, with synthetically considering the device performance, scale effect and manufacturability. Therefore, this section focuses on the introduction of topology optimization in an abstract mathematical form and demonstration of its applications in the areas of microfluidics and nano-optics.

36.3.1 General Considerations in Topology Optimization

Layout optimization problems have attracted research interest of mathematicians and engineers for several decades [46, 47]. Usually, they are categorized into three types, i.e. size optimization, shape optimization and topology optimization. Those three types can be distinguished as demonstrated in Fig. 36.7, where the compliance of the cantilever shown in Fig. 36.7a is minimized respectively using the size optimization, shape optimization and topology optimization approaches. In size optimization, the structure is parameterized by the sizes and positions of geometrical characteristics, and the corresponding parameters are chosen to be the optimization variables; meanwhile, the shape optimization parameterizes the geometrical characteristics of structures using the spline interpolation [48, 49] etc, where the sample points are the optimization variables. After parameterization, the optimization variables are iteratively evolved in the preset feasible regions, using global optimization or gradient information-based optimization algorithm [50]. Size optimization and shape optimization are subjected to the inflexibility on changing the topology of the initial guesses of the structure, and hence have relatively strong dependence on the initial guesses of the optimization variables.

Being different from the size and shape optimization, topology optimization is a full-parameter method used to inversely determine the geometrical configuration, which represents distribution of materials in a structure [51]. It can be used to implement the structural design for the cases where the scale is large enough to ensure the reasonability for using physical parameters of materials fitting in with statistical or continuum hypothesis. In contrast to designing devices by tuning a handful of structural parameters in size and shape optimization, topology optimization utilizes the full-parameter space to design structures solely based on the user's desired performance specification. It is more flexible and robust, because of its low dependence on initial guess of structures and implicitly expression of the material distribution in structures. Therefore, topology optimization is currently regarded to be the most robust methodology for the inverse determination of material distribution in the structures that meet given structural performance criteria.

Structural topology was investigated as early as 1904 for trusses by Michell, and this resulted in structure types carrying his name [52]. The topology optimization method

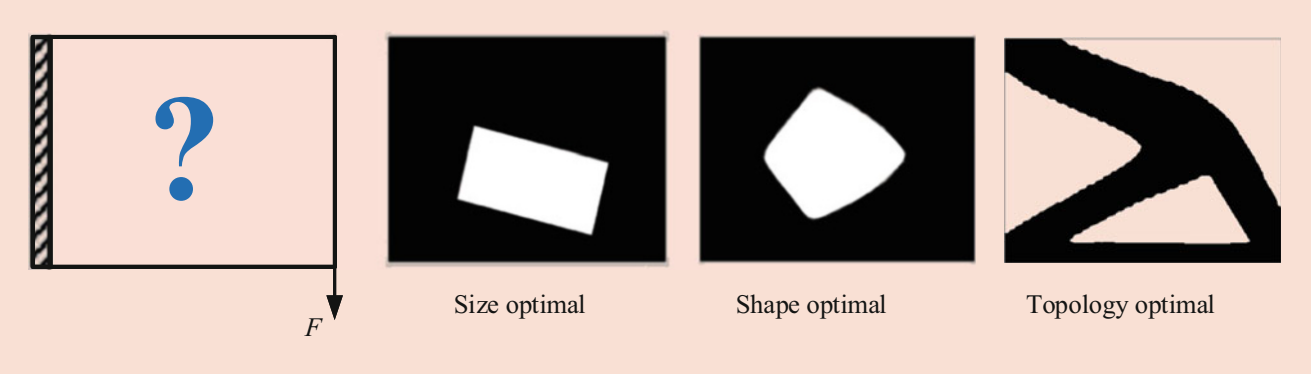


Fig. 36.7 Size optimization, shape optimization and topology optimization of a cantilever with minimizing compliance [111]

was pioneered by Bendsøe and and Kikuchi for elasticity in 1988 [53]; then, it was extended to a variety of application areas, e.g., acoustics, electromagnetics, fluid dynamics and thermodynamics [54–81], to list the most prominent. Currently, the density method [72, 73] and level set method [82–85] have been widely used to describe the material distribution in gradient-based topology optimization. Several other approaches have also been developed for the implementation of topology optimization, e.g., evolutionary techniques [86–88], moving morphable components [89, 90] and phase field method [92], to list the most prominent. In all those researches, the design variable used to represent the structure was usually defined on three-dimensional domains or reduced two-dimensional planes, with the deficiency on the general two-dimensional manifolds. To solve this deficiency, a topology optimization on two-dimensional manifolds has been developed recently [91].

The density method was firstly used to design stiffness and compliance mechanisms [53–55], and it has been extended to multiple physical problems, such as acoustic, electromagnetic, fluidic, optical and thermal problems [51, 56, 70, 71, 74, 75, 79]. The level set method, pioneered by Osher and Sethian [93], accomplishes a change of topology by evolving and merging the zero contour of the level set function, i.e., embedding the boundary in a higher dimension space. This method provides a general approach to track the implicit interface between two phases, and it has been applied to shape and topology optimization [77, 82–85, 94–96]. One of the major advantages of the level set method lies in expressing continuously moving interfaces, and abstracting the material domains that correspond to the structural topology. Compared to the level set method, the density method has the merits of rapid and robust convergency, weak dependence on the initial distribution of the design variable, and the ability to deal with multiple constraints. It is therefore our method of choice for this chapter.

Variational Problem and Regularization

The variational problem for topology optimization is typically in the mathematical form of optimization problem constrained by partial differential equations, and it can be written in the following abstract form

$$\text{find } \gamma \in \mathrm{K}_\gamma \text{ to minimize } J(y;\gamma), \text{ subject to } e(y;\gamma) = 0 \tag{36.62}$$

where $y \in \mathrm{Y}$ is the state variable which can be a scalar or vector; $\gamma \in \mathrm{V}$ is the design variable; y and γ are functionals defined on the open and bounded domain Ω with Lipschitz boundary; $J : \mathrm{Y} \times \mathrm{V} \to \mathbb{R}$ and $e : \mathrm{Y} \times \mathrm{V} \to \mathrm{Z}$ are bounded continuous mapping operator; Y, V and Z are Banach spaces; $\mathrm{K}_\gamma \subset \mathrm{V}$ is the feasible set of γ. A common situation is that $e : \mathrm{Y} \times \mathrm{V} \to \mathrm{Z}$ is continuously Fréchet differentiable and $e_y(y;\gamma) \in \mathcal{L}(\mathrm{Y}, \mathrm{Z})$ has the bounded inverse. Then, according to the implicit function theorem [97], the partial differential equation $e(y;\gamma) = 0$ locally defines a continuously Fréchet differentiable map $\gamma \mapsto y(\gamma)$, which has the following Fréchet derivative

$$y'(\gamma) = -e_y^{-1}(y;\gamma)\, e_\gamma(y;\gamma) \tag{36.63}$$

Therefore, the optimization problem in Eq. (36.62) is transformed into

$$\min \hat{J}(\gamma) = J(y(\gamma);\gamma);\ \gamma \in \mathrm{K}_\gamma \tag{36.64}$$

In density method-based topology optimization, the design variable is relaxed and bounded in a given interval, typically $[0, 1]$, where the values 0 and 1 respectively represent two different materials. Then the set of the feasible values of the design variable in Eq. (36.62) is $\mathrm{K}_\gamma = [0, 1]$. Based on the gradient information of the optimization problem, the design variable is penalized and evolved to the value 0 or 1 at a fixed point in the design domain. Based on the above

regularization, the optimization problem in Eq. (36.64) can be transformed furthermore

$$\min \hat{J}(\gamma) = J(y(\gamma); \gamma); \ \gamma \in [0, 1] \tag{36.65}$$

The gradient information of γ in Eq. (36.65) can be obtained after the adjoint analysis. Based on the gradient information, the variational problem for topology optimization can be solved using an iterative procedure.

Adjoint Analysis

Adjoint method is an efficient approach to derive the descent direction of the objective in the partial differential equation constrained optimization problem [98–100]. From the Gâteaux derivative of $\hat{J}$, one can obtain

$$\begin{aligned} &\left\langle \hat{J}', s \right\rangle_{\mathrm{V}^*,\mathrm{V}} \\ &= \langle J_y, y's \rangle_{\mathrm{Y}^*,\mathrm{Y}} + \langle J_\gamma, s \rangle_{\mathrm{V}^*,\mathrm{V}} \\ &= \langle y'^* J_y, s \rangle_{\mathrm{V}^*,\mathrm{V}} + \langle J_\gamma, s \rangle_{\mathrm{V}^*,\mathrm{V}} \\ &= \langle y'^* J_y + J_\gamma, s \rangle_{\mathrm{V}^*,\mathrm{V}} \\ &= \left\langle e_\gamma^* \left(-e_y^{-1}\right)^* J_y + J_\gamma, s \right\rangle_{\mathrm{V}^*,\mathrm{V}}; \ \forall s \in \mathrm{V} \end{aligned} \tag{36.66}$$

where $(\cdot)^*$ is the adjoint operator of $(\cdot)$; $\langle \cdot, \cdot \rangle$ represents the dual pairing of V^* and V. By setting

$$\lambda = \left(-e_y^{-1}\right)^* J_y = -\left(e_y^*\right)^{-1} J_y \tag{36.67}$$

one can obtain

$$\left\langle e_y^* \lambda, v \right\rangle_{\mathrm{Y}^*,\mathrm{Y}} = \langle -J_y, v \rangle_{\mathrm{Y}^*,\mathrm{Y}}, \ \forall v \in \mathrm{Y} \tag{36.68}$$

where $\lambda \in Z^*$ is the adjoint variable of y; e_y^* is the adjoint operator of e_y. And the Gâteaux derivative of $\hat{J}$ can be reduced to be:

$$\left\langle \hat{J}', s \right\rangle_{\mathrm{V}^*,\mathrm{V}} = \langle e_\gamma^* \lambda + J_\gamma, s \rangle_{\mathrm{V}^*,\mathrm{V}}, \ \forall s \in \mathrm{V} \tag{36.69}$$

If $\hat{J}$ is Fréchet differentiable, the adjoint equation

$$e_y^* \lambda = -J_y \tag{36.70}$$

and the adjoint derivative

$$\hat{J}' = e_\gamma^* \lambda + J_\gamma \tag{36.71}$$

can be obtained, where the adjoint derivative is utilized as the gradient information of the objective.

In engineering, the variational problem may need to be regularized furthermore by some integral constraints, e.g., volume constraint. The adjoint analysis of these integral constraints is the same as that for the objective. The variational problem in Eq. (36.62) usually has strong nonlinearity and it is difficult to solve the system directly. Therefore, the iterative approach is widely adopted. In the iterative approach, the descent direction can be defined based on the adjoint derivative, where the state and adjoint variables are respectively obtained by solving the partial differential equations and corresponding adjoint equations.

Numerical Implementation

The procedure for the iterative approach includes the following steps (Fig. 36.8):

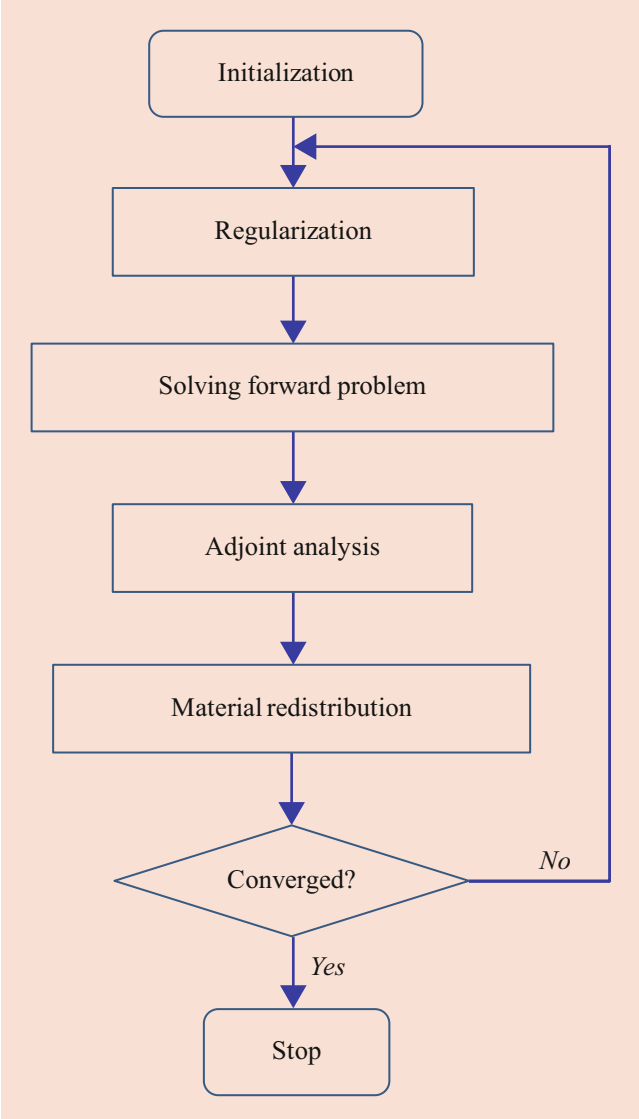


Fig. 36.8 Flowchart for the iterative solution of the optimization problem

1. the design variable is regularized by a PDE filter and threshold method [101–105];
2. the partial differential equations are solved with the regularized design variable;
3. the adjoint equations are solved based on the numerical solution of the partial differential equations;
4. the adjoint derivatives of the objective functional and integral constraint are computed;
5. the design variable is updated using the method of moving asymptotes (MMA), which can be used to deal with the optimization problem with multiple integral constraints and bound constraint of the design variable [107].

These steps are implemented iteratively until the stopping criteria are satisfied. The stopping criteria are usually specified as a maximal iterative number or the change of the objective values in 5 consecutive iterations satisfying

$$\sum_{i=0}^{4} |J_{k-i} - J_{k-i-1}| / |J_k| < \epsilon \tag{36.72}$$

in the k-th iteration, where J_k and γ_k are the objective value and the distribution of the design variable in the k-th iteration, respectively; ϵ is the tolerance typically chosen to be 1×10^{-3}. In the above iterative procedure, the partial differential equations and corresponding adjoint equations can be solved by reasonably chosen numerical methods. During the iterative procedure, the design variable can be filtered by the PDE filter [101, 102] to ensure the distribution smoothness, where the PDE filter is implemented by solving the following equation:

$$\begin{aligned} -r^2 \nabla \cdot \nabla \tilde{\gamma} + \tilde{\gamma} &= \gamma, \text{ in } \Omega \\ \mathbf{n} \cdot \nabla \tilde{\gamma} &= 0, \text{ on } \partial\Omega \end{aligned} \tag{36.73}$$

where r is the filter radius chosen based on numerical experiments [102]; $\tilde{\gamma}$ is the filtered design variable. To ensure the minimum scale length and remove the gray area in the obtained material topology, the filtered design variable is projected by the threshold method [103–105]:

$$\bar{\tilde{\gamma}}(\tilde{\gamma}) = \frac{\tanh(\beta\xi) + \tanh(\beta(\tilde{\gamma} - \xi))}{\tanh(\beta\xi) + \tanh(\beta(1 - \xi))} \tag{36.74}$$

where $\bar{\tilde{\gamma}}$ is the projected design variable called physical density representing the material topology [105]; $\xi \in [0, 1]$ and β are the threshold and projection parameters for the threshold projection, respectively. On the choice of the values of ξ and β, one can refer to [103, 106]. Because the design variable is filtered by the PDE filter, the filter equation is included in the partial differential equation constraints of the variational problem (Eq. 36.62). Then, $\tilde{\gamma}$ is regarded as one component of the state vector y. And the adjoint equation of the filter equation is included in the adjoint analysis.

36.3.2 Applications in Microfluidics and Nano-Optics

Topology optimization can provide a powerful approach for inverse design of structures in the area of MEMS and NEMS, with synthetically considering the device performance, scale effect and manufacturability. In this section, topology optimization of MEMS and NEMS are demonstrated respectively for microfluidics and nano-optics.

Topology Optimization for Microfluidics

Lab on a chip is a recent trend in analytical chemistry and the life sciences. In the past two decades, the lab-on-a-chip for fluid handling and analysis has emerged in the interdisciplinary research field of microfluidics [108, 109]. The use of microfluidics in these applications has attracted the interest of industry and academia, because of its potential and advantages, such as small amounts of sample and reagent, less time consumption, lower cost, and high throughput [110]. Miniaturization gives rise to the scale effects of microfluidics. Therefore, it is required to synthetically consider the microscale effects and manufacturability with achieving the desired microfluidic performance.

Two of the most important scale effects in microfluidics are the low Reynolds number and large surface-to-volume ratio. They result in the inefficient mass-transfer and dominance of the surface tension in microfluidics. Because of these specialities, the usually used design approaches encounter the problem on synthetically considering the microscale effects and manufacturability to achieve required microfluidic performance. Therefore, it was inspired to utilize the topology optimization method and implement the inverse design of microfluidics. Based on the topology optimization method, several researches on the inverse design of typical microfluidic components have been implemented [111]. To demonstrate the capability of such a synthetic method, passive micromixers are inversely designed to increase the mass-transfer efficiency, and the periodic microtextures are inversely designed to enhance the robustness of Cassie-Baxter mode of wetting behavior.

Low Reynolds-Number: Topology Optimization of Micromixers

The low-Reynolds-number effect of microfluidics results in the low mass-transfer efficiency. For this effect, passive micromixer is the most typical microfluidic component, where it is desired to enhance the chaotic advection of microflows based on the reasonable design of a microchannel; it is also an important microfluidic component, with wide chemical, biological and detection/analysis applications [112].

The passive micromixer implements the mixing of reagents for the steady flow. By the reasonable layout of the microchannel in a micromixer, the chaotic advection can be

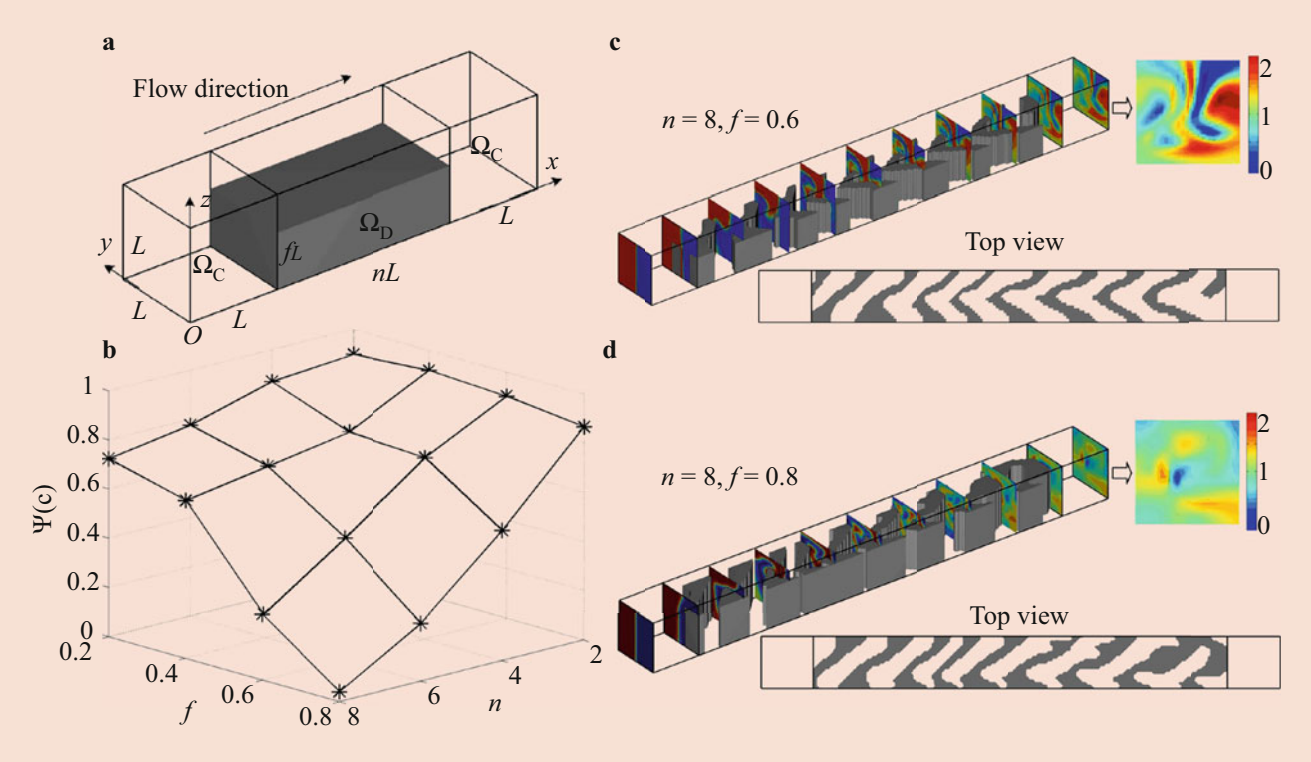


Fig. 36.9 (**a**) Design domain of the passive micromixer. Ω_C is the channels connected to the design domain Ω_D; the length and height of Ω_D are nL and fL, respectively; (**b**) plotting of the mixing measurement of the micromixers for design domains with different values of n and f; (**c**) layout of the micromixer with $n = 8, f = 0.6$, and the corresponding value of the mixing measurement is 0.267; (**d**) layout of the micromixer with $n = 8, f = 0.8$, and the corresponding value of the mixing measurement is 0.041. The characteristic length L is 400 μm; the Reynolds number and Péclet number are 10 and 10^3, respectively [113]

strengthened, and the mixing performance can be improved. In the cases of mixing two fluid streams with different concentration of solutions, the ideal concentration distribution of the solute at the outlet, is the average concentration. The mixing performance of the micromixer can be measured by $\Psi(c) = \int_{\Gamma_o} (c - c_a)^2 \, d\Gamma / \int_{\Gamma_i} (c_r - c_a)^2 \, d\Gamma$, where c_a is the ideal concentration distribution at the outlet Γ_o; c_r is the reference concentration distribution at the inlet Γ_i. A lower value of $\Psi(c)$ corresponds to better mixing performance. Therefore, the design task is to find the reasonable layout of a micromixer corresponding to the lowest value of the mixing measurement in a given design domain with designer specified inlet and outlet. Then a variational problem with the mixing measurement $\Psi(c)$ as the objective functional can be constructed for the inverse design of the micromixer in the specified design domain. The variational problem is solved using the topology optimization approach, with the model setting and results as shown in Fig. 36.9, where the soft lithography-like manufacturability of the micromixers is ensured by enforcing the quasi-3D dimension of the derived geometry [113].

Large Surface-to-Volume Ratio: Topology Optimization of Microtextures for Cassie-Baxter Wettability

Large surface-to-volume ratio results in the dominance of surface tension in microfluidics, and this is typically presented by the wetting behavior on a solid surface. Recent achievements in the construction of artificial surfaces for special wettability are widespread focused on superhydrophobicity, which means the contact angle of water larger than 150° for a hydrophobic solid substrate [114]. Because the wettability of the solid surface is commonly determined by its geometric morphology and surface free energy, creating microtextures on hydrophobic surfaces has been commonly used to design artificial surfaces with Cassie-Baxter wettability [115].

On a hydrophobic surface with microtextures, two different solid/liquid contact modes can exist. They are the Wenzel and Cassie-Baxter modes. The Cassie-Baxter mode corresponds to a stronger hydrophobicity. When the liquid is pressed physically, the solid/liquid contact mode can change from the Cassie-Baxter case to the Wenzel case, along with

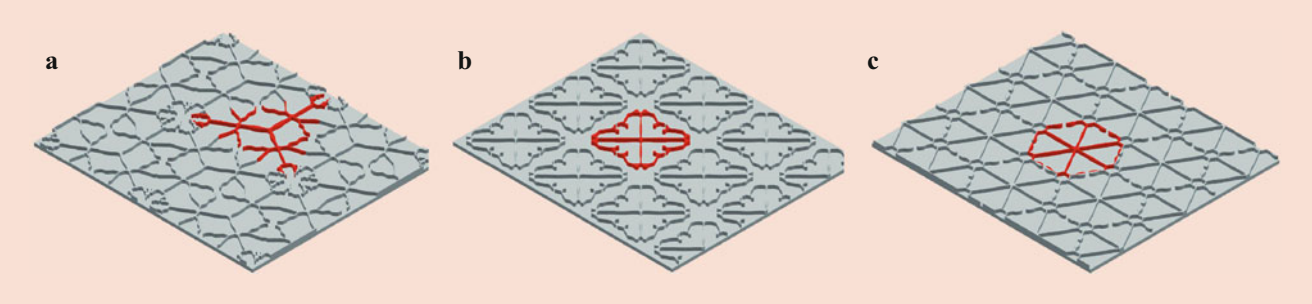


Fig. 36.10 Microtextures for Cassie-Baxter wettability derived by topology optimization method, respectively for the periodic tilling with regular-triangle, regular-quadrangle and regular-hexagon lattices. (**a**) Regular triangle. (**b**) Regular quadrangle. (**c**) Regular hexagon

a decrease of the hydrophobicity. Therefore, reasonable microtextures on a solid surface can keep the Cassie-Baxter mode from transition, and enhance the robustness of the hydrophobicity-like wetting behavior. The reasonability of a microtexture can be measured by the volume of the liquid bulges hold by the liquid/vapor interface, when a fixed static pressure is loaded. And smaller liquid-bulge volume corresponds to more robust Cassie-Baxter mode. Therefore, the microtexture on a solid surface can be inversely designed by minimizing the volume of the liquid bulges. Then, based on the topology optimization method, the microtextures in Fig. 36.10 are derived for the special periodicity with regular-triangle, regular-quadrangle and regular-hexagon lattices, which can respectively strew a flat surface [116, 117].

Topology Optimization for Nano-Optics

Control of optical waves is realized by the nanostructures with complicated geometrical configurations and preselected materials, where the Maxwell's equations are widely used to describe the electromagnetics of the corresponding wave propagation. For the complication of electromagnetics, physical intuition-based electromagnetic structure design has its limitations to achieve the desired performance. To overcome these bounds, several inverse design tests have been implemented based on the structural optimization methods [56–71, 118–122], in which topology optimization method is the one of the most employed.

This section provides the researches on inversely finding the optimal geometric topology of photonic nanostructures, with synthetically considering the performance and manufacturability. The optimal geometric configuration of the nanostructure is determined by the topology optimization approach including the geometric constraints (e.g. the feature size and geometric dimension) brought by the used fabrication process (e.g. ebeam lithography). The related researches have been implemented for both the dielectric and metal material-based nanostructures [123–126]. And those researches have permitted the one-shot design and prediction of nanostructures with satisfied performances in the area of photonics and wave optics, where nanostructures play the key role.

Dielectric Nanostructure: Topology Optimization of Metalens

Metalenses are able to achieve diffraction-limited focusing through localized phase modification of the incoming light beam [127–132]. Because these structures are ultrathin, less than a wavelength, this has the potential of achieving ultrathin optical elements, with a thickness limited mainly by the mechanical strength of the transparent substrate. Recently proposed metalenses are based on either dielectric nanofin arrays, or nanoparticles of large number, which leads to severe manufacturing challenges [133]. To overcome these challenges, a new type of metalens has been predicted with concentric-nanoring configuration, where the number and size of the nanorings are determined using an topology optimization method [123]. By focusing the electrical field energy at a specified position, the convex-like metalens is inversely predicted with desired numerical aperture and a diffraction-limited focal spot (Fig. 36.11a). The Poynting vector distribution found demonstrates the mechanism of the lensing function, in which optical vortices are generated in the nanorings to achieve a matching of the phase and impedance between the substrate and free space, and further, to form a spherical wavefront and enhance the transmission of the optical energy (Fig. 36.11b–d). This method can also be extended to predict an axicon-like metalens with focal beam. The improved manufacturability is concluded from the geometry of the concentric-nanoring configurations.

Metal Nanostructure: Topology Optimization for Localized Surface Plasmon Resonances

Localized surface plasmon resonances (LSPRs) are the strong interaction between metal nanostructures and visible light through the resonant excitations of collective oscillations of conduction electrons. In LSPRs, the local electromagnetic fields near the nanostructure can be many orders of magnitude higher than the incident fields, and the incident light around the resonant-peak wavelength is

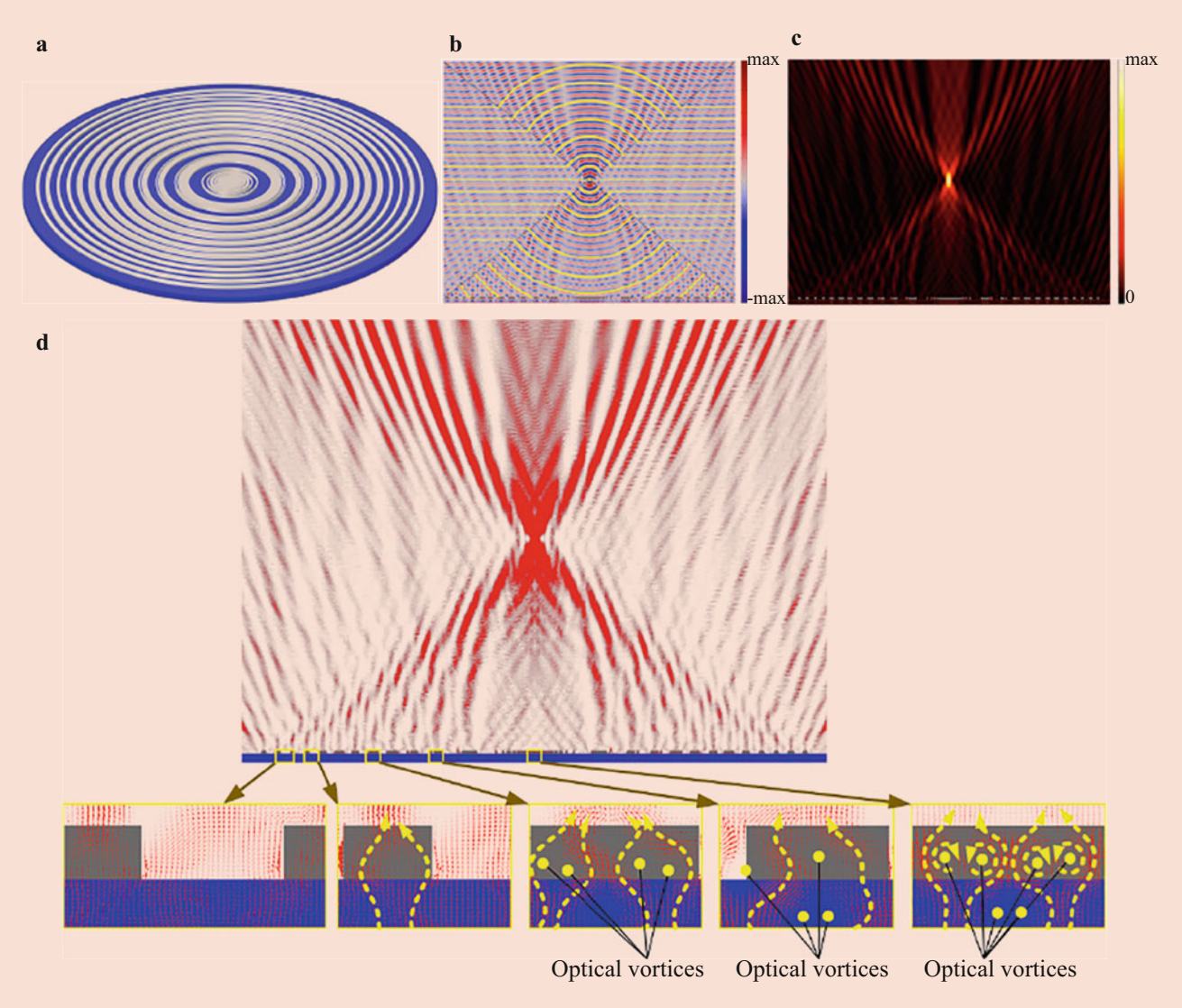


Fig. 36.11 (**a**) Convex-like metalens with ring thickness 200 nm for an incident wavelength of 700 nm; (**b**) real part distribution of the field in the metalens, with spherical phase distribution indicated by the yellow-colored circular arcs; (**c**) electric energy density distribution in the symmetrical plane of the metalens; (**d**) Poynting vector distribution in the metalens with incident wavelength 700 nm, ring thickness 200 nm, and NA = 0.8. The used material is titanium oxide [123]

scattered strongly. The enhanced electric fields are confined within only a tiny region of the nanometer length scale near the surface of the nanostructures and decay significantly thereafter [134].

Due to the deficiency on the inverse problem to find the optimized spatial distribution of metal material in air or dielectric to cater to the performance requirement, an inverse design methodology of metal nanostructures has been presented for LSPRs, based on the topology optimization approach [124,125]. Using the proposed method, determination of the metal distribution in nanostructures is implemented to maximize the enhancement factor of the electric field. The topologically optimized nanostructure was obtained with resonant peak at the specified incident wavelength (Fig. 36.12). Red or blue shift of the resonant peak can be controlled by specifying larger or smaller wavelength for the outlined topology optimization approach. Therefore, the outlined approach can be used to design metal nanostructure with resonant peak and improved enhancement factor at specified incident wavelength and control the shift of the resonant peak by topologically optimizing the nanostructure. This inverse design method for LSPRs can be further extended to other metal nanostructures, e.g. optical antenna and optical trapping.

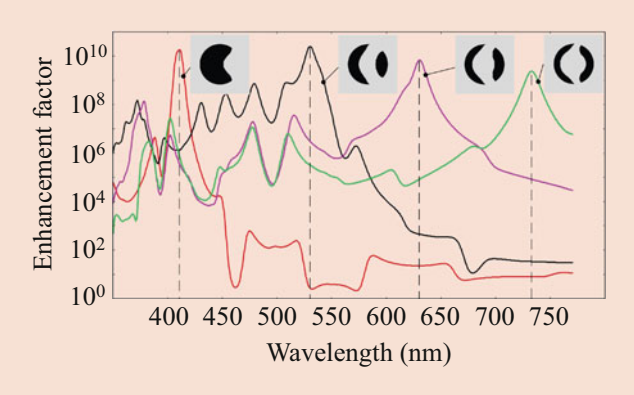


Fig. 36.12 Enhancement-factor spectra of the topologically optimized metal nanostructures. The four nanostructures respectively correspond to the incident wavelengths 410, 533, 633 and 733 nm, in which the resonant peak is red shifted by topology optimization implemented at larger incident wavelengths. The used material for the metal nanostrucutres is silver [124]

36.4 Model Order Reduction

The design domain in topology optimization is usually meshed finely in order to derive a design with accurate representation of the geometry; such fine mesh leads to a large-scale system with many degrees of freedom, especially in the design of three dimensional structures. Therefore, the optimization process is very time consuming due to the need of solving a large-scale system at each iteration. This also poses high demand for computational resources. Model order reduction (MOR) aims to construct a model with much smaller number of degrees of freedom, which gives rise to an approximate solution to the original large-scale system with acceptable error, and at the same time, preserves the key structure of the original large-scale system, so that the small system can play as a surrogate for the large-scale system in simulation. The original large-scale system is called full-order model (FOM) and the model with smaller degrees of freedom is named as the reduced order model (ROM).

Parametric model order reduction (pMOR) is especially useful in design, such as optimization, control, and uncertainty quantification, since the ROM preserves the parametric structure of the original system and is constructed to be accurate for every parameter variation happened during each query of the task.

In this section, we review the reduced basis method which is efficient for linear steady systems with a general parametric form; those systems may arise from topology optimization as discussed in the previous section. Since port-Hamiltonian systems are also very common in MEMS design, we review typical MOR methods for nonlinear port-Hamiltonian systems.

36.4.1 Reduced Basis Method for Steady Linear Parametric Systems

In this section, we review the reduced basis (RB) method for steady linear parametric systems.

$$A(\mu)x(\mu) = f(\mu, x(\mu)), \tag{36.75}$$

where, $\mu \in \mathbb{R}^d$ is the vector of parameters in the parameter domain $\mathcal{P} \subset \mathbb{R}^d$, $x(\mu) \in \mathbb{R}^N$ is the state vector, $f(\mu, x(\mu)) \in \mathbb{R}^N$ is the nonlinear vector. $A(\mu) \in \mathbb{R}^{N\times N}$ is the system matrix.

Such systems may arise from discretization of parametric partial differential equations (PDEs) in space, using finite difference, finite element or finite volume methods. The number of degrees of freedom N is usually large; MOR techniques are developed to find a system of reduced order $r \ll N$, that approximates the original FOM with acceptable accuracy.

If the solution to (36.75) lies in a low dimensional subspace, then it is possible to construct an orthogonal basis of the subspace, such that the solution can be approximated by the basis vectors. Then a ROM can be constructed via Galerkin projection as,

$$A_r(\mu)x_r(\mu) = f_r(\mu, x_r(\mu)), \tag{36.76}$$

where $A_r(\mu) = V^{\mathrm{T}}A(\mu)V \in \mathbb{R}^{r\times r}$ is the reduced system matrix; $x_r(\mu) \in \mathbb{R}^r$, is the reduced state vector; $f_r(\mu, x_r(\mu)) = V^{\mathrm{T}}f(\mu, Vx_r(\mu)) \in \mathbb{R}^r$ is the reduced nonlinear vector. The solution $x(\mu)$ can be recovered via the approximation: $x(\mu) \approx Vx_r(\mu)$.

Algorithm 1 Greedy algorithm for steady systems

Require: $\mathcal{P}_{\text{train}}$, tol_{RB}
Ensure: Projection matrix V representing the reduced basis.
1: Initialization: $V = [\,]$, $\mu^\star = \mu^1$, $\eta(\mu^\star)(> \text{tol}_{\text{RB}})$
2: **while** the error $\eta(\mu^\star) > \text{tol}_{\text{RB}}$ **do**
3: Solve (36.75) to get the solution $x(\mu^\star)$.
4: Update: $V :=$orth $[V, \mathbf{x}(\mu^\star)]$.
5: Find $\mu^\star := \arg\max_{\mu\in\mathcal{P}_{\text{train}}} \eta(\mu)$.
6: **end while**

The RB method for a linear parametric steady system (36.75) can be summarized as below

- Specify $\mathcal{P}_{\text{train}} := \{\mu^1, \ldots, \mu^m\}$, a training set of parameter samples.
- Specify an error estimator/indicator/bound $\eta(\mu)$.
- Use Greedy algorithm to compute the projection matrix V.
- Form the ROM (36.76).

The essence of the RB method is that performing limited number of full simulations of the original large-scale system, a ROM with sufficient accuracy at all possible samples of μ can be constructed, so that it can act as a surrogate of the FOM in the subsequent multi-query tasks.

For efficient simulating the ROM, it is required that the system matrix $A(\mu)$ is affine with the parameter μ, i.e.,

$$A(\mu) = A_1 h_1(\mu) + \ldots + A_q h_q(\mu),$$

where $h_1(\mu), \ldots, h_q(\mu)$ are scalar functions of the parameter vector μ and $A_1, \ldots, A_q$ are parameter independent matrices. If $A(\mu)$ is in the affine form of μ, then $A_r(\mu)$ can be efficiently computed as

$$A_r(\mu) = \big(V^{\mathrm{T}} \cdot A_1 \cdot V\big)h_1(\mu) + \ldots + \big(V^{\mathrm{T}} \cdot A_q \cdot V\big)h_q(\mu),$$

where $V^{\mathrm{T}} \cdot A_1 \cdot V, \ldots, V^{\mathrm{T}} \cdot A_q \cdot V$ can be precomputed and repeatedly called during solving the ROM. Ideally, the right-hand side $\mathbf{f}(\mu, x(\mu))$ is also affine with the parameter μ and is independent of the state vector $x(\mu)$, then $\mathbf{f}_r(\mu)$ can also be efficiently computed as

$$\mathbf{f}_r(\mu) = \big(V^{\mathrm{T}} \cdot \mathbf{f}_1\big)\tilde{h}_1(\mu) + \ldots + \big(V^{\mathrm{T}} \cdot \mathbf{f}_m\big)\tilde{h}_m(\mu),$$

where the parameter-independent vectors $V^{\mathrm{T}} \cdot \mathbf{f}_1, \ldots, V^{\mathrm{T}} \cdot \mathbf{f}_m$ can be precomputed and repeatedly called during solving the ROM. However, in many cases $\mathbf{f}(\mu, x(\mu))$ is non-affine and is also a nonlinear function of $x(\mu)$. In this case, we can use interpolation methods introduced in the next section to reduce the complexity of computing $\mathbf{f}_r$ in the ROM.

Reducing the complexity of $\mathbf{f}_r(\mu, x_r(\mu))$ in the ROM (36.76)

From (36.76), we observe that if the right-hand side $f(\mu, x(\mu))$ is not affine with the parameter μ, evaluating the nonlinear term $f_r(\mu, x_r(\mu))$ still depends on the dimension N of the FOM, since we need to first evaluate $f(\mu, Vx_r(\mu))$ and then multiply with V^{T}. Some interpolation techniques are proposed in the literature to reduce this complexity, such as the Empirical interpolation method (EIM) [135, 136], and the Discrete empirical interpolation method (DEIM) [137].

EIM is proposed associated with the reduced basis method. Both the interpolation indices and the interpolation basis vectors are chosen within the greedy algorithm. DEIM can be considered as a discrete version of EIM. The main difference of DEIM from EIM is in the interpolation basis construction. EIM computes the basis from the snapshots of the nonlinear vector, whereas DEIM constructs basis from the POD basis of the nonlinear snapshots.

Either EIM or DEIM considers approximation for the nonlinear term as below,

$$f(\mu, x(\mu)) \approx U_{\mathrm{f}} c(\mu),$$

where U_{f} is the matrix of interpolation basis vectors and $c(\mu)$ is the vector of parameter dependent coefficients. The approximation $U_{\mathrm{f}} c(\mu)$ interpolates $f(\mu)$ in the sense that it matches $f(\mu)$ at the selected interpolation points, i.e.

$$P^{\mathrm{T}} f(\mu, x(\mu)) = P^{\mathrm{T}} U_{\mathrm{f}} c(\mu),$$

where $P^{\mathrm{T}} = [e_{\wp_1}, e_{\wp_2}, \ldots, e_{\wp_\ell}]^{\mathrm{T}}$ is a row permutation matrix, and $e_{\wp_i}$ is the $\wp_i$-th unit vector. Here, $\wp_1, \ldots, \wp_\ell$ are the interpolation points (indices). To be self-contained, we list both algorithms as Algorithms 2 and 3.

Algorithm 2 EIM for steady systems

Input: Snapshots of $f(\mu, x(\mu)) : F = \{f^1, \ldots, f^m\}, f^k := f(\mu^k, x(\mu^k)), k = 1, \ldots m.$

Output: EI basis: $U = [u_1, \ldots, u_M]$ and indices: $\{\wp_1, \ldots, \wp_M\}$, index matrix: $P = [e_{\wp_1}, \ldots, e_{\wp_M}]$.

$P = [\,], U_{\mathrm{f}} = [\,]$.

$s = 1$, $\xi_1 := \arg\max_{f^k \in F} \|f^k\|_2$, $\wp_1 := \arg\max_{j \in \{1,\ldots,n\}} |\xi_{1,j}|$, $u_1 := \xi_1 / \xi_{1,\wp_1}$. $P = [P, e_{\wp_1}]$, $U_{\mathrm{f}} = [U_{\mathrm{f}}, u_1]$.

while $\|\xi_s\|_2 > \epsilon$ **do**

  $s := s + 1$. For each f^k, $k = 1, \ldots, m$: $f^k \approx \sum_{i=1}^{s-1} \beta_{ki} u_i$, i.e.

$$f^k \approx U_{\mathrm{f}} \beta_k, \beta_k = (\beta_{k1}, \ldots, \beta_{ks-1})^{\mathrm{T}}$$

  β_k is determined by interpolation:

$$P^{\mathrm{T}} f^k = P^{\mathrm{T}} U \beta_k,$$

  so that $\beta_k = (P^{\mathrm{T}} U_{\mathrm{f}})^{-1} P^{\mathrm{T}} f^k$.

  Let $f^{k^\star} := \arg\max_{f^k \in F} \|f^k - U_{\mathrm{f}} \beta_k\|_2$, $\xi_s = f^{k^\star} - U_{\mathrm{f}} \beta_{k^\star}$

  if $\|\xi_s\|_2 \le \epsilon$ **then**

    Stop and set $M = s - 1$.

  else

    Define $\wp_s := \arg\max_{j \in \{1,\ldots,N\}} |u_{s,j}|$, $u_s := \xi_s / \xi_{s,\wp_s}$.

    $P = [P, e_{\wp_s}]$, $U_{\mathrm{f}} = [U_{\mathrm{f}}, u_s]$.

  end if

end while

ROM After Applying EIM or DEIM Using either EIM or DEIM, the ROM in (36.76) is then formulated as,

$$A_r(\mu) x_r(\mu) = V^{\mathrm{T}} U_{\mathrm{f}} \big(P^{\mathrm{T}} U_{\mathrm{f}}\big)^{-1} P^{\mathrm{T}} f(\mu, Vx_r(\mu)). \tag{36.77}$$

The term $V^{\mathrm{T}} U_{\mathrm{f}} \big(P^{\mathrm{T}} U_{\mathrm{f}}\big)^{-1}$ in (36.77) can be precomputed. When evaluating $P^{\mathrm{T}} f(\mu, Vx_r(\mu))$, only a few terms (say, $\ell_{\mathrm{EI}} \ll N$ terms) of the function $f(\cdot, \cdot)$ need to be evaluated, so that the complexity of computing the nonlinear term of the ROM is reduced from $O(N)$ to $O(\ell_{\mathrm{EI}} \ll N)$. When the matrix $A(\mu)$ is also nonaffine with the parameter μ, then the matrix DEIM method [138] could be applied to obtain an affine approximation of $A(\mu)$, so that for each evaluation of $A_r(\mu)$,

Algorithm 3 Discrete empirical interpolation method (DEIM) [137]

Input: Snapshots of $f(\mu)$ at a set of parameter samples, $F = \{f^1, \ldots, f^m\}, f^k := f(\mu^k, x(\mu^k)), k = 1, \ldots m, \epsilon_{\text{svd}}$.
Output: DEIM basis vectors U_f, index matrix $P = [e_{\wp_1}, e_{\wp_2}, \ldots, e_{\wp_\ell}]$.
1: $U_f = [\,], P = [\,]$.
2: Apply SVD: $F \xrightarrow{\text{SVD}} U\Sigma Q^{\mathrm{T}}$, where $U := [u_1, u_2, \ldots, u_N]$, $\Sigma := \begin{bmatrix} D_f & 0 \\ 0 & 0 \end{bmatrix}$, $D_f := \text{diag}(\sigma_1, \sigma_2, \ldots, \sigma_{r_{\text{F}}})$.
3: Find ℓ, s.t., $\sum_{i=\ell+1}^{r_{\text{F}}} \sigma_i^f / \sum_{i=1}^{r_{\text{F}}} \sigma_i^f < \epsilon_{\text{svd}}$, r_{F} is the number of non-zero singular values of Σ.
4: Select the first interpolation index as the position of the row element with maximal magnitude in the first column of U: $\wp_1 = \arg \max_{j \in \{1,2,\ldots,N\}} |u_{1j}|$, where $u_1 = [u_{11}, u_{12}, \ldots, u_{1N}]^{\mathrm{T}}$.
5: $U_f \leftarrow u_1, P \leftarrow [e_{\wp_1}]$.
6: **for** $i = 2$ to ℓ **do**
7: Solve $(P^{\mathrm{T}} U_{\text{f}})c = P^{\mathrm{T}} u_i$, for c.
8: Compute the residual, $r_i = u_i - U_{\text{f}} c$.
9: $\wp_i = \arg \max_{j \in \{1,2,\ldots,N\}} |r_{ij}|$. Here, $r_i = [r_{i1}, r_{i2}, \ldots, r_{iN}]^{\mathrm{T}}$.
10: $U_{\text{f}} \leftarrow [U_{\text{f}}, u_i], P \leftarrow [P, e_{\wp_i}]$.
11: **end for**

the matrix $A(\mu)$ of full dimension needs not be evaluated, and only some terms which are independent of μ need be precomputed. Detailed analysis of the method can be found in [138] and the references therein. Algorithm 1 can be combined with either EIM or DEIM for MOR linear systems with right-hand side $f(\mu)$ being non-affinely dependent on the parameter. The interpolation basis are precomputed before the greedy loop starts. Algorithm 4 provides the Greedy-(D)EIM algorithm.

36.4.2 Structure Preserving MOR for Nonlinear Port-Hamiltonian Systems

In this section, we review a recently proposed structure preserving MOR method for nonlinear port-Hamiltonian systems [139]. Finite dimensional nonlinear port-Hamiltonian (NLPH) system is in the form of

$$\begin{aligned} \dot{\mathbf{x}} &= (J - R)g(\mathbf{x}) + Bu(t), \\ \mathbf{y} &= B^{\mathrm{T}} g(\mathbf{x}), \end{aligned} \tag{36.78}$$

Algorithm 4 Greedy algorithm with (D)EIM for steady systems

Input: Training set of parameter samples $\Xi \subset \mathcal{P}$, tolerance *tol*, snapshot matrix of $f(\mu, x(\mu))$: $F = [f^1, \ldots, f^{n_{\text{train}}})], f^k := f(\mu^k, x(\mu^k)), k = 1, \ldots n_{\text{train}}$, n_{train} is the number of samples in Ξ.
Output: Basis V.
1: (D)EIM interpolation basis obtained from Algorithm 2 or Algorithm 3.
2: Call Algorithm 1, where the ROM in (36.76) is replaced by the ROM in (36.77) at each iteration.

where $\mathbf{x} \in \mathbb{R}^n$ is the n-dimensional state vector; $g(\mathbf{x}) := \nabla_{\mathbf{x}} H(\mathbf{x})$; the scalar-valued function $H : \mathbb{R}^n \mapsto [0, \infty)$ is called the Hamiltonian, which is continuous and differentiable. It describes the internal energy of the system as a function of state. $J = -J^{a\mathrm{T}} \in \mathbb{R}^{n \times n}$ is the structure matrix describing the interconnection among energy storage elements in the systems; $R = R^{\mathrm{T}} \geq 0 \in \mathbb{R}^{n \times n}$ is the dissipation matrix describing energy loss in the system; and $B \in \mathbb{R}^{n \times O_l}$ is the port matrix describing how energy enters and exists the system. It is assumed that the Hamiltonian is bounded below and strictly positive, i.e., $H(\mathbf{x}) > 0, \forall \mathbf{x}$. Note that the method in [139] considers only non-parametric systems without parameter variations.

A ROM of the NLPH can be obtained using the above mentioned POD method based on Petrov-Galerkin projection, i.e.

$$\begin{aligned} W^{\mathrm{T}} \cdot V \cdot \dot{\mathbf{x}}_r &= W^{\mathrm{T}} \cdot (J - R) \cdot \mathbf{g}(V \cdot \mathbf{x}_r) + W^{\mathrm{T}} \cdot B \cdot u(t), \\ \mathbf{y} &= B^{\mathrm{T}} \cdot \mathbf{g}(V \cdot \mathbf{x}_r). \end{aligned} \tag{36.79}$$

Unfortunately, system in (36.79) does not preserve the Hamiltonian form and some properties of the Hamiltonian systems might be lost. Furthermore, if the Hamiltonian function $H(\cdot)$ is nonquadratic, then $\mathbf{g}(V \cdot \mathbf{x}_r)$ is a nonlinear vector-valued function, so that DEIM or EIM is necessary to reduce the cost of evaluating $\mathbf{g}(V \cdot \mathbf{x}_r)$.

In [139], a structure preserving method is proposed, so that the ROM is also a Hamiltonian system. It is based on the following heuristic assumption: the internal force $\mathbf{g}(\mathbf{x})$ approximately locates in the subspace spanned by the columns of W, so that $\mathbf{g}(\mathbf{x}) \approx W \cdot \mathbf{g}_r$, for some $\mathbf{g}_r \in \mathbb{R}^r$. Assume that $V^{\mathrm{T}} \cdot W = I$, which can be satisfied by many MOR methods, e.g., the structure-preserving POD method in Algorithm 5. From $\mathbf{x} = V \cdot \mathbf{x}_r$, we get $\mathbf{g}(\mathbf{x}) \approx \mathbf{g}(V \cdot \mathbf{x}_r)$. Since we have $\mathbf{g}(\mathbf{x}) \approx W \cdot \mathbf{g}_r$, then

$$\mathbf{g}(V \cdot \mathbf{x}_r) \approx \mathbf{g}(\mathbf{x}) \approx W \cdot \mathbf{g}_r. \tag{36.80}$$

Using $V^{\mathrm{T}} \cdot W = I$ and from (36.80), we can compute $\mathbf{g}_r$ as

$$\mathbf{g}_r \approx V^{\mathrm{T}} \cdot \mathbf{g}(V \cdot \mathbf{x}_r). \tag{36.81}$$

Finally, $\mathbf{g}(\mathbf{x})$ can be approximated as

$$\mathbf{g}(\mathbf{x}) \approx W \cdot \mathbf{g}_r \approx W \cdot V^{\mathrm{T}} \cdot \mathbf{g}(V \cdot \mathbf{x}_r).$$

Applying the approximation $\mathbf{x} \approx V \cdot \mathbf{x}_r$ and $\mathbf{g}(\mathbf{x}) \approx W \cdot V^{\mathrm{T}} \cdot \mathbf{g}(V \cdot \mathbf{x}_r)$ to the original Hamiltonian system (36.78), we obtain the ROM as below,

$$\begin{aligned} \dot{\mathbf{x}}_r &= (J_r - R_r) \cdot V^{\mathrm{T}} \cdot \mathbf{g}(V \cdot \mathbf{x}_r) + B_r \cdot u(t), \\ \mathbf{y} &= B_r^{\mathrm{T}} \cdot V^{\mathrm{T}} \cdot \mathbf{g}(V \cdot \mathbf{x}_r), \end{aligned} \tag{36.82}$$

Algorithm 5 Structure-preserving POD for NLPH systems

1: Snapshots $X = [\mathbf{x}(t_1), \mathbf{x}(t_2), \ldots, \mathbf{x}(t_K)]$: solution vector $\mathbf{x}(t)$ at discrete time instances $t_i, i = 1, \ldots, K$.
2: Simultaneously collect associated *force*(nonlinear) snapshots: $G = [\mathbf{g}(\mathbf{x}(t_0)), \mathbf{g}(\mathbf{x}(t_1)), \ldots, \mathbf{g}(\mathbf{x}(t_K))]$.
3: Perform $X \xrightarrow{\text{SVD}} U \cdot \Sigma \cdot Q^{\mathrm{T}}$ to get the projection matrix $V = U(:, 1 : r)$.
4: Perform $G \xrightarrow{\text{SVD}} U_g \cdot \Sigma_g \cdot Q_g^{\mathrm{T}}$ to get the projection matrix $W = U_g(:, 1 : r)$.
5: Biorthoganolize the two matrices such that $W^{\mathrm{T}} \cdot V = I$. This can be achieved by e.g., modified Gram-schmidt process.
6: Using W, V to obtain the ROM in (36.82).

where $J_r = W^{\mathrm{T}} \cdot J \cdot W$, $R_r = W^{\mathrm{T}} \cdot R \cdot W$, and $B_r = W^{\mathrm{T}} \cdot B$. Note that $J_r = -J_r^{\mathrm{T}}$ and $R_r = R_r^{\mathrm{T}} \geq 0$, so that (36.82) preserves the Hamiltonian structure and is a port-Hamiltonian system. In Algorithm 5, we review the structure preserving POD method for NLPH system proposed in [139].

Structure Preserving MOR with DEIM

To solve the ROM in (36.82), the nonlinear function $\mathbf{g}(V \cdot \mathbf{x}_r)$ must be computed at each time step. Directly computing $\mathbf{g}(V \cdot \mathbf{x}_r)$ needs evaluating a vector of length N, the complexity is not reduced. Therefore, interpolation methods, e.g., DEIM or EIM are useful for reducing the complexity of evaluating the nonlinear term. In [139], DEIM is applied to $\mathbf{g}(V \cdot \mathbf{x}_r)$, and the resulting ROM with DEIM still preserves the Hamiltonian structure.

In the following, we first present an algorithm of DEIM being applied to approximate the nonlinear function $\mathbf{g}(V \cdot \mathbf{x}_r)$, as shown in Algorithm 6. A straight-forward application of DEIM to the ROM in (36.82) is as following. Using $U_g := W$ computed from Algorithm 5 to obtain a DEIM approximation of $g(V\mathbf{x}_r)$, we get

$$g(V \cdot \mathbf{x}_r) \approx W(P^{\mathrm{T}} \cdot W)^{-1} \cdot P^{\mathrm{T}} \cdot g(V \cdot \mathbf{x}_r),$$

where the index matrix P can be computed from Algorithm 6 with SVD of G (Step 2) already being available from Algorithm 5. inserting the above DEIM approximation into (36.82), and using $V^{\mathrm{T}} \cdot W = I$, we obtain

$$\begin{aligned} \dot{\mathbf{x}}_r &= (J_r - R_r) \cdot (P^{\mathrm{T}} \cdot W)^{-1} \cdot P^{\mathrm{T}} \cdot g(V \cdot \mathbf{x}_r) + B_r \cdot u(t), \\ \mathbf{y} &= B_r^{\mathrm{T}} \cdot (P^{\mathrm{T}} \cdot W)^{-1} \cdot P^{\mathrm{T}} \cdot g(V \cdot \mathbf{x}_r). \end{aligned} \tag{36.83}$$

However, it is stated in [139] that the ROM in (36.83) is not port-Hamiltonian and might no longer be stable. A DEIM Hamiltonian method is proposed in [139] to produce a ROM which is still Hamiltonian. An algorithm of computing a structure preserving Hamiltonian ROM with DEIM can be found in [139].

Algorithm 6 Discrete empirical interpolation method (DEIM) for $g(\mathbf{x})$

Input: Snapshots of $g(\mathbf{x})$ at a set of time instances $t_i, i = 1, \ldots, K$, $G = [g(\mathbf{x}_1) \ldots, g(\mathbf{x}_K]$, $\mathbf{x}_i, i = 1, \ldots, K$ is the solution $\mathbf{x}$ at time instances t_i.
Output: DEIM basis U_g, index matrix $P = [e_{\wp_1}, e_{\wp_2}, \ldots, e_{\wp_\ell}]$.
1: $U_g = [\,], P = [\,]$.
2: Compute SVD of G: $G \xrightarrow{\text{SVD}} U\Sigma Q^{\mathrm{T}}$, where $U := [u_1, u_2, \ldots, u_N]$, $\Sigma := \begin{bmatrix} D_g & 0 \\ 0 & 0 \end{bmatrix}$, $D_g := \text{diag}(\sigma_1, \sigma_2, \ldots, \sigma_{r_G})$.
3: Find ℓ, s.t., $\sum_{i=\ell+1}^{r_G} \sigma_i^f / \sum_{i=1}^{r_F} \sigma_i^f < \epsilon_{\text{svd}}$, r_{G} is the number of non-zero singular values of Σ.
4: Select the first interpolation index as the position of the row element with maximal magnitude in the first column of U: $\wp_1 = \arg \max_{j \in \{1,2,\ldots,N\}} |u_{1j}|$, where $u_1 = [u_{11}, u_{12}, \ldots, u_{1N}]^{\mathrm{T}}$.
5: $U_g \leftarrow u_1, P \leftarrow [e_{\wp_1}]$.
6: **for** $i = 2$ to ℓ **do**
7: Solve $(P^{\mathrm{T}} U_g)c = P^{\mathrm{T}} u_i$, for c.
8: Form the residual, $r_i = u_i - U_g c$.
9: $\wp_i = \arg \max_{j \in \{1,2,\ldots,N\}} |r_{ij}|$. Here, $r_i = [r_{i1}, r_{i2}, \ldots, r_{iN}]^{\mathrm{T}}$.
10: $U_g \leftarrow [U_g, u_i], P \leftarrow [P, e_{\wp_i}]$.
11: **end for**

36.4.3 Application to Topology Optimization

Iterative approach is widely employed to solve the topology optimization problem in Sect. 36.3. At every iteration step, the discrete counterparts of $e(y, \gamma)$ and $e_y^* \cdot \lambda = -J_y$ need to be solved. Their discrete forms are

$$\begin{aligned} K(\gamma) \cdot \nu &= \mathbf{f}(\gamma), \\ K(\gamma) \cdot \boldsymbol{\lambda} &= \frac{\partial \Phi}{\partial \nu}, \end{aligned} \tag{36.84}$$

where ν and $\boldsymbol{\lambda}$ are the discrete physical variable and adjoint variable, respectively, $K(\boldsymbol{\gamma})$ is the global stiffness matrix, and it depends on the discrete design variable γ; Φ corresponds to the discretized design objective. Based on the above analysis, the computational cost in topology optimization is mostly spent on solving the linear systems in (36.84).

MOR could be applied to obtain ROM of the system in (36.84), so as to reduce the computational cost. Note that the system in (36.84) is a one-way coupled system of ν and $\boldsymbol{\lambda}$, where a possibly nonlinear function of ν appears on the right-hand side of the second system of $\boldsymbol{\lambda}$. From the literature [140], constructing a single ROM of (36.84) is usually no more efficient than constructing two ROMs for the systems of ν and $\boldsymbol{\lambda}$, respectively.

Consider the system of ν, it is a linear parametric system, which is of the same form as the system in (36.75), therefore the reduced basis method as discussed in Sect. 36.4.1 can be applied to construct the ROM, and the EIM or DEIM algorithm could be applied to reduce the complexity of the

right-hand side $\mathbf{f}(\gamma)$, if it is a non-affine or nonlinear function of γ. As for the second equation, once ν is solved from its ROM, it can be substituted into the right-hand side of the system of $\boldsymbol{\lambda}$, which then becomes a linear system of $\boldsymbol{\lambda}$ with right-hand side $\partial\Phi/\partial\nu$ being a function of γ, which can then be reduced using the reduced basis method combined with the EIM or DEIM method, in case $\partial\Phi/\partial\nu$ is non-affine with γ. For clarity we show the process of constructing the ROM of the coupled system (36.84) in Algorithm 7.

Algorithm 7 Greedy algorithm for the coupled system (36.84)

Input: $\mathcal{P}_{\text{train}}$: a set of samples of γ, tol_{RB}
Output: Projection matrix V_1 for MOR of the system of ν, V_2 for MOR of the system of $\boldsymbol{\lambda}$.
1: Initialization:$V_1 = [\,]$, $V_2 = [\,]$, $\gamma^\star = \gamma^1$, $\eta(\gamma^\star)(> \text{tol}_{\text{RB}})$
2: **while** the error $\eta(\gamma^\star) > \text{tol}_{\text{RB}}$ **do**
3: Solve $K(\gamma)\cdot\nu = \mathbf{f}(\gamma)$ to get the solution $\nu(\gamma^\star)$.
4: Substitute $\nu(\gamma^\star)$ into $K(\gamma)\cdot\boldsymbol{\lambda} = \partial\Phi/\partial\nu$, and solve for $\boldsymbol{\lambda}(\gamma^\star)$.
5: Update: V_1 :=orth $[V_1, \nu(\gamma^\star)]$, V_2 :=orth $[V_2, \boldsymbol{lambda}(\gamma^\star)]$
6: Find $\gamma^\star := \arg\max_{\gamma\in\mathcal{P}_{\text{train}}} \eta(\gamma)$.
7: **end while**

Once V_1 and V_2 are obtained from Algorithm 7, the ROM of system (36.84) can be constructed as below,

$$\begin{aligned}\left(V_1^{\mathrm{T}}\cdot K(\gamma)\cdot V_1\right)\cdot\nu_r &= V_1^{\mathrm{T}}\cdot f(\gamma),\\ \left(V_2^{\mathrm{T}}\cdot K(\gamma)\cdot V_2\right)\cdot\boldsymbol{\lambda}_r &= V_2^{\mathrm{T}}\cdot\frac{\partial\Phi}{\partial(V_1\cdot\nu_r)},\end{aligned}\qquad(36.85)$$

where $V_1^{\mathrm{T}}\cdot K(\gamma)\cdot V_1 \in \mathbb{R}^{r\times r}$ is a small matrix with $r \ll n$. If the right-hand side $\mathbf{f}(\gamma)$ or $\partial\Phi/\partial(V_1\cdot\nu_r)$ is non-affine with the parameter γ, then EIM or DEIM can be applied to obtain interpolation of $\mathbf{f}(\gamma)$ or $\partial\Phi/\partial(V_1\cdot\nu_r)$ and to reduce the computational complexity of evaluating $V_1^{\mathrm{T}}\cdot\mathbf{f}(\gamma)$ or $V_2^{\mathrm{T}}\cdot\partial\Phi/\partial(V_1\cdot\nu_r)$. During optimization, the small ROM in (36.85) can be used as a surrogate of the original large system in (36.84), which is aimed to produce accurate results not only at the samples of γ in the training set $\mathcal{P}_{\text{train}}$ but also at every other possible variation of the parameter γ.

36.5 Conclusions

This chapter brings together three diverse topics and seeks a single descriptive framework. These topics form, in one way or another, and with varying degrees of intensity, the necessary tasks that advance computational design and the digital twin. Much work must be done still to complete the consolidation process. In particular, if model order reduction and topology optimization can be consistently integrated (or merged), the task of finding optimal designs may one day be performed with the speed necessary for interactive design processes performed in real time. Furthermore, model order reduction as presented is applicable only to linear systems. Nonlinear problems, especially those of stability, are potentially complex enough that MOR cannot be applied with sufficient computational efficiency. Advancing this area is also one of the priorities for the future.

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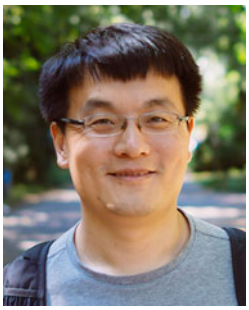

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Macroscopic Transport Models for Classical Device Simulation

37

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Contents

37.1 History of Classical Device Simulation 1336
37.1.1 Structure of the Review 1336

37.2 The Phenomenological Drift-Diffusion Model 1338
37.2.1 Poisson's Equation and the Continuity Equation 1338
37.2.2 Drift and Diffusion Current 1339
37.2.3 The Semiconductor Equations 1339
37.2.4 Parameter Modeling 1340

37.3 Microscopic Transport Modeling 1341
37.3.1 The Boltzmann Transport Equation 1341
37.3.2 The Band Structure 1342
37.3.3 Macroscopic Observables 1342
37.3.4 Analytical Distributions 1343
37.3.5 The Microscopic Relaxation Time Approximation 1344
37.3.6 Microscopic Generation and Recombination 1344

37.4 Macroscopic Transport Models 1345
37.4.1 The Method of Moments 1345
37.4.2 The Macroscopic Relaxation Time Approximation 1345
37.4.3 The Closure Problem 1346
37.4.4 Moment Equations for a Parabolic Band 1346
37.4.5 Hydrodynamic Models 1347

37.5 Energy Transport Models 1349
37.5.1 The Diffusion Approximation 1349
37.5.2 Diffusion Scaling 1350
37.5.3 Stratton's Approach 1350
37.5.4 Bløtekjær's Approach 1351
37.5.5 Relaxation Times and Carrier Mobilities 1353
37.5.6 Bløtekjær Versus Stratton Approach 1355

37.6 Limits of Validity for Drift-Diffusion and Energy Transport Models 1355
37.6.1 Critical Issues 1355
37.6.2 Non-Maxwellian Energy Distribution 1357
37.6.3 Numerical Evaluation 1359

37.7 Advanced Macroscopic Transport Models 1362
37.7.1 Ansatz-Based Approaches 1362
37.7.2 Higher-Order Moment Models 1364
37.7.3 Table-Based Parameter Modeling 1366

37.8 Applications 1367
37.8.1 n^+nn^+ Test Structures 1368
37.8.2 A Double-Gate MOSFET 1371
37.8.3 Modeling of Hot-Carrier Effects 1373

37.9 Summary and Conclusion 1376

References 1377

Abstract

We review macroscopic transport models as used in classical device simulation such as drift-diffusion, hydrodynamic, and energy transport models. Using a systematic approach, these transport models are derived from the semiclassical Boltzmann equation by applying the method of moments. The drift-diffusion model is based on the first two moments of the Boltzmann equation, while hydrodynamic and energy transport models consider three or four moments. Within the framework of the diffusion approximation, the convective terms in the hydrodynamic models can be neglected, resulting in the much simpler diffusive energy transport models. A discussion of the physical assumptions needed for the validity of these models is given.

In cases where the energy distribution is insufficiently described by a heated Maxwellian distribution, energy transport models give poor results. Based on the diffusion approximation, a six-moment model generalizing the energy transport model is presented. All model parameters can be extracted from fullband bulk Monte Carlo simulations. The six-moment model is applied for the simulation

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of devices with channel length in the deca-nanometer regime. Short-channel and hot-carrier effects for which the heated Maxwellian assumption introduces particularly large errors are studied. Comparing all models, it is demonstrated that the six-moment model can improve on the drift-diffusion and energy transport models.

Keywords

Macroscopic transport models · Device simulation · Classical device simulation · Bolzmann-transport equation · Drift diffusion · Hydrodynamic transport · Energy transport · Six-moments · Higher-order models · Semiconductor equations · Poisson equation

37.1 History of Classical Device Simulation

The success of microelectronic technology has been partly enabled and supported by sophisticated technology computer-aided design (TCAD) tools which are used to assist in development and engineering at practically all stages from process definition to circuit optimization. The modern technology development cost and time reduction from the use of TCAD has been estimated at around 40% [1].

At the early days of transistor technology, relatively simple compact models based on the drift-diffusion formalism, idealized doping profiles, and quasi-one-dimensional assumptions produced sufficiently accurate results. To reduce the costs of the chip manufacturing process, the number of devices on a chip has been continually increased by increasing the chip size and decreasing the size of the individual devices. For these devices, the simplifying assumptions valid before became increasingly violated, thus requiring a more rigorous description. Development of compact models, though still possible and of fundamental importance, became more complicated, requiring large development times and continuous modifications.

The drift-diffusion (DD) model was first presented by Van Roosbroeck in the year 1950 [2]. Instead of a closed-form compact model, the basic semiconductor equations can be solved directly for a given doping profile and geometry. The same model was later derived from the Boltzmann transport equation (BTE) by the method of moments [3] or from basic principles of irreversible thermodynamics [4, 5]. The self-consistent numerical solution of carrier transport models dates back to the famous seminal work of Scharfetter and Gummel [6, 7] and eliminates many of the assumptions required for compact models. Due to its simplicity and its excellent numerical properties, the drift-diffusion equations have become the workhorse for most applications in technology computer-aided design.

In the 1980s, the first tools appeared which offered a solution of the drift-diffusion equations on two-dimensional domains. The first monograph comprehensively covering aspects from modeling and discretization to applications was Selberherr [3], which was published in 1984. Since then, current transport models have been continuously refined and extended to more accurately capture transport phenomena occurring in state-of-the-art semiconductor devices.

The steady need for refinement and extension is caused by the ongoing feature size reduction in technology. As the supply voltages cannot be scaled accordingly without compromising the circuit performance, the electric fields inside the devices have increased. Large electric fields, which rapidly change over small length scales, give rise to nonlocal and hot-carrier effects which begin to dominate device performance. These phenomena are a concern for industrial applications, and an accurate description is required.

To deal with nonlocal and hot-carrier effects, extended models have been proposed which consider the carrier energy as an independent solution variable. The most prominent examples of such models are the hydrodynamic and energy transport (ET) models. These models are based on the work of Stratton [8] and Bløtekjær [9] who solved the BTE using the method of moments with three or four moments. Many variants of these models have been published, which are reviewed in [10]. However, detailed examinations in the deep submicron area show that using three or four moments is still not sufficient for specific problems which depend on high-energy tails. One method for improving the approximation is the six-moments (SM) model [11].

Figure 37.1 gives an overview of transport models in use for modern TCAD. The most accurate methods solve the Boltzmann equation directly, either by Monte Carlo methods or by the spherical harmonic expansion. Yet the computational costs of these methods are challenging even today, and in many cases, simpler moment-based methods are preferred. In addition, for the simulation of small state-of-the-art devices, quantum effects have to be included.

This handbook chapter is concerned with macroscopic transport models based on the method of moments as used in classical device simulation. Other chapters in the handbook specialize on modeling with spherical harmonic expansion, the Monte Carlo simulation method, and quantum transport modeling. Classical monographs on macroscopic transport models are [3] and [12]. A modern mathematical reference on macroscopic transport models is [13]. A review article about general classical device simulation is [5]. The limits of validity for classical macroscopic models and models for nanoscale device simulation beyond these limits are discussed in [14].

37.1.1 Structure of the Review

Following the historical notes in Sect. 37.1, we start our exposition in Sect. 37.2 with a phenomenological derivation

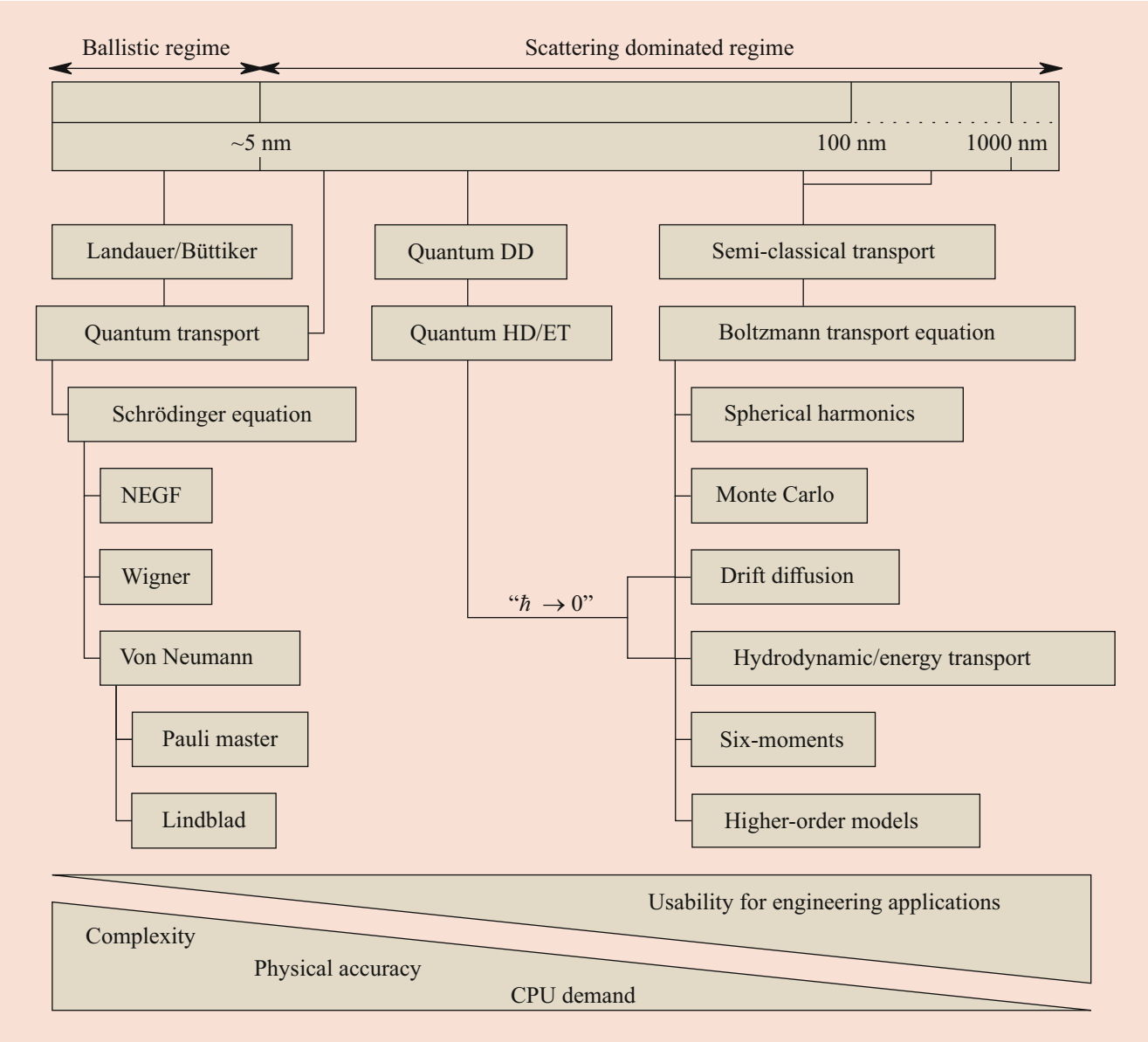

Fig. 37.1 Hierarchy of transport models

of the drift-diffusion model which is the simplest reasonable macroscopic transport model. The drift-diffusion model assumes an equilibrium between carrier energy and electric field, which however is no longer valid in modern electronic devices. Several assumptions are required for its validity to hold, and a heuristic derivation is instructive for a good physical understanding.

The theoretical cornerstone of classical device simulation is the Boltzmann equation which is discussed in Sect. 37.3. In classical device simulation, electron transport is dominated by the scattering operator. We introduce the relaxation time approximation in the Boltzmann equation which allows an analytical treatment of the scattering term.

Macroscopic transport models based on the Boltzmann equation are derived by the method of moments, which is a powerful approach to obtain a series of weighted balance and flux equations. This approach is studied in Sect. 37.4. To enable an analytical treatment, we assume parabolic bands and give the corresponding equations for the first four moments. Following Bløtekjær's approach, we derive a hydrodynamic model based on the first three moments by assuming an isotropic thermal energy tensor and a phenomenological closure for the heat flow.

In Sect. 37.5, we derive energy transport models starting from the hydrodynamic model by making additional simplifications, which are known as the diffusion approximation. To motivate the diffusion approximation, the drift-diffusion equations are derived from the Boltzmann equation using the method of moments. The assumptions necessary for the derivation are analyzed.

The validity of drift-diffusion and energy transport models is investigated theoretically and numerically in Sect. 37.6. Differences and common features of transport models can be understood by looking closely at the assumptions used in their derivation from the Boltzmann equation. Based on this analysis, we discuss critical issues for the validity of energy transport and hydrodynamic models. The highest-order even moment available in typical energy transport models is the temperature. Based on Monte Carlo simulation data, it is demonstrated that the energy distribution in n^+nn^+ test structures strongly deviates from a heated Maxwellian distribution below 100 nm channel length. We then compare results from drift-diffusion and energy transport models with Monte Carlo simulations.

A natural extension of energy transport and hydrodynamic models is the inclusion of higher-order moments. A transport model based on six moments of the distribution function is presented in Sect. 37.7. This model does not assume any particular shape of the distribution function. The additional even order moment, the kurtosis of the distribution function, is shown to contain fundamental information about the shape of the distribution function.

In Sect. 37.8, we present applications of higher-order transport models to n^+nn^+ test structures and double-gate MOSFETs. We compare results of the energy transport model and the six-moment model with Monte Carlo simulation results and discuss short-channel effects.

Finally, we close the review by summarizing our results in Sect. 37.9.

37.2 The Phenomenological Drift-Diffusion Model

In this section, the drift-diffusion current relations will be derived using a phenomenological approach. This set of equations has first been presented by van Roosbroeck in 1950 [2]. Together with the Poisson equation and the carrier continuity equations, these equations constitute the basic semiconductor equations, the simplest reasonable transport model possible [3]. The presentation in this section follows conceptionally [15].

37.2.1 Poisson's Equation and the Continuity Equation

The Poisson equation is a common constituent to all charge transport models for semiconductor devices and serves as the link between the electrostatic potential and the charge distribution within a semiconductor device.

In the eddy-current-free quasi-stationary case (electro-quasistatic model), which typically holds true for semiconductor devices [16–18], the electric field $\mathbf{E}$ is expressed as the gradient of a scalar potential ψ.

$$\mathbf{E} = -\nabla\psi \tag{37.1}$$

Using Gauss's law and the proper material equation for the quasi-stationary case one obtains the Poisson equation:

$$\nabla \cdot (\varepsilon \nabla\psi) = -\rho \tag{37.2}$$

ε is the dielectric permittivity (assumed to be scalar hereafter). In semiconductors, two separate particle systems are responsible for charge transport, namely, electrons (n) and holes (p). Neglecting defects and fixed charges, the total space charge density in semiconductors is primarily composed of the charges of electrons, the holes, and the ionized dopant atoms:

$$\rho = q\,(p + N_\mathrm{D}^+) - q\,(n + N_\mathrm{A}^-) = q\,(p - n + N) \tag{37.3}$$

In order to obtain a complete description, the Poisson equation has to be solved self-consistently with the transport equation system.

Charge transport is described by the current continuity equation which expresses local charge conservation:

$$\nabla \cdot \mathbf{J} + \partial_t \varrho = 0 \tag{37.4}$$

Like the Poisson equation, the continuity equation can be derived from Maxwell's equations. The conduction current density $\mathbf{J}$ can be written as the sum of two components:

$$\mathbf{J} = \mathbf{J}_\mathrm{n} + \mathbf{J}_\mathrm{p} \tag{37.5}$$

$\mathbf{J}_\mathrm{n}$ and $\mathbf{J}_\mathrm{p}$ are the electron and hole current density.

It is convenient to split up also the current continuity equation (37.4) into two equations by introducing a formal separation parameter R:

$$\nabla \cdot \mathbf{J}_\mathrm{n} - q\partial_\mathrm{t} n = qR \tag{37.6}$$

$$\nabla \cdot \mathbf{J}_\mathrm{p} + q\partial_\mathrm{t} p = -qR \tag{37.7}$$

R can be interpreted as the net recombination rate defined as:

$$R = R_\mathrm{n} - G_\mathrm{n} = R_\mathrm{p} - G_\mathrm{p} \tag{37.8}$$

where $R_\mathrm{n}/G_\mathrm{n}$ and $R_\mathrm{p}/G_\mathrm{p}$ are the recombination/generation rates for electrons and holes, respectively.

37.2.2 Drift and Diffusion Current

The simplest current transport model at hand is based on the so-called drift-diffusion assumption. This model distinguishes between two charge carrier transport mechanisms: the drift of charge carriers due to an electric field caused by a gradient in the electric potential and the diffusion of the charge carriers due to a spatial gradient in the charge carrier concentration.

Drift Current

The component of the current which is caused by the electric field is called drift current. From a macroscopic point of view, the current density and the electric field are related by Ohm's law:

$$\mathbf{J}^{\text{drift}} = \sigma\,\mathbf{E} \tag{37.9}$$

σ is the electric conductivity.

Semiconductors are in principle anisotropic due to their crystal structure. However, due to symmetry properties, especially in the case of germanium and silicon, the anisotropicity of the conductivity is very small, and the electric conductivity can be well approximated by a scalar.

From a microscopic point of view, the current density can be expressed as

$$\mathbf{J}^{\text{drift}} = q\,p\,\bar{\mathbf{v}}_{\text{p}} - q\,n\,\bar{\mathbf{v}}_{\text{n}} \tag{37.10}$$

where q is the elementary charge, n and p the electron and hole concentrations, and $\bar{\mathbf{v}}_{\text{n}}$ and $\bar{\mathbf{v}}_{\text{p}}$ the mean velocities of electrons and holes, respectively. The electric field accelerates the carriers, but due to various scattering mechanisms, the velocity of the carriers in a constant field is bounded and is proportional to the electric field:

$$\bar{\mathbf{v}}_{\text{n}} = -\mu_{\text{n}}(\mathbf{E})\,\mathbf{E} \tag{37.11}$$

$$\bar{\mathbf{v}}_{\text{p}} = \mu_{\text{p}}(\mathbf{E})\,\mathbf{E} \tag{37.12}$$

μ_{n} and μ_{p} are the respective mobilities of electrons and holes. In order to improve the applicability range of the drift current expression, a field-dependent mobility is generally used (see Sect. 37.2.4). By inserting these equations into (37.10), we get

$$\mathbf{J}^{\text{drift}} = q\,p\,\mu_{\text{p}}\,\mathbf{E} + q\,n\,\mu_{\text{n}}\,\mathbf{E}. \tag{37.13}$$

Comparing (37.13) with (37.9) and (37.5), the following relations are obtained:

$$\mathbf{J}_{\text{n}}^{\text{drift}} = \sigma_{\text{n}}\,\mathbf{E} \tag{37.14}$$

$$\mathbf{J}_{\text{p}}^{\text{drift}} = \sigma_{\text{p}}\,\mathbf{E} \tag{37.15}$$

The conductivities are are given as

$$\sigma_{\text{n}} = q\,n\,\mu_{\text{n}} \tag{37.16}$$

$$\sigma_{\text{p}} = q\,p\,\mu_{\text{p}}. \tag{37.17}$$

Diffusion Current

The component of the current which is caused by the thermal motion of the carriers is called diffusion current. It is driven by a gradient in the carrier concentration. The law of diffusion, which originally stems from the theory of dilute gases, defines the flux densities:

$$\mathbf{F}_{\text{n}} = -D_{\text{n}}\,\nabla n \tag{37.18}$$

$$\mathbf{F}_{\text{p}} = -D_{\text{p}}\,\nabla p \tag{37.19}$$

Here, D_{n} and D_{p} are the diffusion coefficients for electrons and holes. The particle flux densities $\mathbf{F}_{\text{n}}$ and $\mathbf{F}_{\text{p}}$ have to be multiplied by the charge of the particle to get the electric current densities:

$$\mathbf{J}_{\text{n}}^{\text{diffusion}} = -q\,\mathbf{F}_{\text{n}} \tag{37.20}$$

$$\mathbf{J}_{\text{p}}^{\text{diffusion}} = q\,\mathbf{F}_{\text{p}} \tag{37.21}$$

37.2.3 The Semiconductor Equations

Superposition of the current components yields the drift-diffusion current relations:

$$\mathbf{J}_{\text{n}} = q\,n\,\mu_{\text{n}}\mathbf{E} + q\,D_{\text{n}}\nabla n \tag{37.22}$$

$$\mathbf{J}_{\text{p}} = q\,p\,\mu_{\text{p}}\mathbf{E} - q\,D_{\text{p}}\nabla p \tag{37.23}$$

For conditions close to thermal equilibrium and for nondegenerate carrier systems where Boltzmann statistics are valid, the diffusion coefficients are related to the mobilities by the Einstein relation:

$$D_{\text{n}} = \mu_{\text{n}}\,\frac{k_{\text{B}}\,T_{\text{n}}}{q} \tag{37.24}$$

$$D_{\text{p}} = \mu_{\text{p}}\,\frac{k_{\text{B}}\,T_{\text{p}}}{q} \tag{37.25}$$

k_{B} is Boltzmann's constant, and T_{n} and T_{p} are the temperatures of electrons and holes.

Since no information about the carrier temperature is available, the carrier temperature is set equal to the lattice temperature T_{L}, assuming the thermal equilibrium approximation [19]. We finally write the equations for the electrons as:

$$\nabla\cdot\mathbf{J}_{\text{n}} = q\,(R + \partial_{\text{t}}\,n) \tag{37.26}$$

$$\mathbf{J}_{\text{n}} = \mu_{\text{n}}\,k_{\text{B}}\left(\nabla(n\,T_{\text{L}}) + \frac{\text{q}}{k_{\text{B}}}\,\mathbf{E}\,n\right). \tag{37.27}$$

The analogous equations for holes, namely

$$\nabla \cdot \mathbf{J}_\mathrm{p} = -q\,(R + \partial_\mathrm{t}\, p) \tag{37.28}$$

$$\mathbf{J}_\mathrm{p} = \mu_\mathrm{p}\, k_\mathrm{B} \left(-\nabla (p\, T_\mathrm{L}) + \frac{\mathrm{q}}{k_\mathrm{B}}\, \mathbf{E}\, p \right) \tag{37.29}$$

are added to complete the system. Together with Poisson's equation (37.2), the set of basic semiconductor equations is obtained.

The drift-diffusion scheme takes only local quantities into account. As such, it completely neglects nonstationary transport effects which occur in response to a sudden variation of the electric field, either in time or in space. A robust discretization of the drift-diffusion equations was proposed by Scharfetter and Gummel [6,7], which is still in use today.

As one of the basic limitations of the drift-diffusion model, it should be pointed out that the Einstein relations are only valid near equilibrium and the diffusivity relations are largely underestimated, if the lattice temperature rather than the carrier temperature is being used [20, p.145]. In order to account for hot-carrier effects, the average energy can be estimated via the homogeneous energy balance equation:

$$T_\mathrm{n} = T_\mathrm{L} + \frac{2}{3}\, \frac{q}{k_\mathrm{B}}\, \tau_\mathcal{E}\, \mu_\mathrm{n}\, E^2 \tag{37.30}$$

This equation can be derived from the homogeneous limit of an energy transport model based on the Boltzmann equation (see Sect. 37.5.4). However, for rapidly increasing electric fields, the average energy lags behind the electric field and can be considerably smaller than the one predicted by the homogeneous energy balance equation (37.30). Purely phenomenological approaches to describe heat transport in semiconductors are available [5], but are not further discussed here.

37.2.4 Parameter Modeling

Even though this set of basic semiconductor equations is complete, it cannot be solved without the further description of the material parameters for the mobilities μ_n and μ_p and the generation/recombination rate R.

Mobility

The carrier mobilities in semiconducting materials are determined by various physical mechanisms, because the charge carriers experience scattering events by thermal lattice vibrations, ionized impurities, neutral impurities, vacancies, interstitials, dislocations, surfaces, and with each other.

The engineering approach to take all this into account is to use fitted analytical models based on measurements or to extract parameters from sophisticated Monte Carlo simulations. Rigorous first principle models for the carrier mobilities exist, but they are complicated and hard to implement.

In the drift-diffusion equations, mobility models depending on the electric field are usually employed. Various models have been developed; examples can be found in [21–23]. For weak electric fields, the mobility is constant with respect to the field, and therefore the relation between the velocity and the electric field is linear. For large electric fields, the relationship begins to deviate from linear, and the velocity saturates for very high fields. The maximum velocity observed in bulk silicon measurements is the saturation velocity v_sat requiring the mobility to be of the form $\mu \to v_\mathrm{sat}/E$. In silicon, the value of v_sat is 10^7 cm/s [24]. Simulation tools commonly differentiate between low- and high-field mobilities and allow the user to select the models independently.

However, as will be shown below, the carrier mobility does not depend on E, but is a functional of the carrier distribution function. Mobility models in higher-order transport models can use more information from the distribution function. In energy transport models, for example, the carrier temperature can be used as a solution variable. As a consequence, effects like the velocity overshoot can be approximately described.

Carrier Generation and Recombination

The recombination rate R was formally introduced in the drift-diffusion equations (37.6) and (37.7) by splitting the continuity equation into two individual parts for electrons and holes. From a physical point of view, this term includes the generation and the recombination of electron-hole pairs.

Various physical mechanisms can cause the generation/recombination of an electron-hole pair. For instance, the absorption or emission of a photon, the absorption or emission of a phonon, three particle transitions, and transitions assisted by recombination centers can occur. The impact of these mechanisms depends on the operation conditions and the properties of the employed materials.

One important generation/recombination process is the well-known Shockley-Read-Hall (SRH) mechanism [25,26] which describes a two-step phonon transition. A trap level, which is energetically located within the bandgap and enables the electron to recombine with a hole, is utilized. Four partial processes can be separated: the capture and the emission of both, electrons and holes, on the trap level. Balance equations can be formulated for the trap occupancy function which leads to the Shockley-Read-Hall model. In the stationary limit, the rate dependence on the carrier concentration is described by the expression

$$\begin{aligned} R &= R_\mathrm{n} - G_\mathrm{n} = R_\mathrm{p} - G_\mathrm{p} \\ &= \frac{n\,p - n_i^2}{\tau_\mathrm{p}\,(n + n_1) + \tau_\mathrm{n}\,(p + p_1)} \end{aligned} \tag{37.31}$$

$$n_1 p_1 = n_i^2. \tag{37.32}$$

Here n_i denotes the intrinsic carrier concentration (constant). The auxiliary concentrations n_1 and p_1 depend on lattice temperature and the trap energy level. The parameters τ_n and τ_p are the lifetimes for electrons and holes depending on the lattice temperature. Various physical mechanisms may influence the recombination/generation process. A doping dependence of recombination lifetimes is experimentally observed in silicon technology.

In thermal equilibrium, the net recombination rate vanishes ($n_0 p_0 = n_i^2$). An excess number of carriers ($np > n_i^2$) lead to an increased recombination, and a low-carrier concentration ($np < n_i^2$) leads to an increased generation. Lifetimes can be modeled depending on trap concentration, temperature, and doping.

The carrier recombination process is critical for any device that involves both electron and hole flows. Generation/recombination phenomena are involved in many fundamental effects, like leakage current and device breakdown.

37.3 Microscopic Transport Modeling

Following a more rigorous approach, macroscopic transport equations used in semiconductor device simulation are normally derived from the Boltzmann transport equation (BTE), which determines the microscopic phase space distribution function $f = f(\mathbf{r}, \mathbf{k}, t)$ for a stochastic ensemble of particles of a single-carrier type. The unknown distribution function in the BTE is considered as a classical, everywhere positive, distribution function.

However, the Boltzmann transport equation requires information only accessible by quantum mechanical considerations [14]. These are the band structure, expressions for the scattering and generation/recombination rates, and the Pauli exclusion principle reflecting the Fermi statistics of carriers. In this section, we discuss the Boltzmann equation and simplified models for band structure, scattering, and generation/recombination processes, which are employed in the derivation of macroscopic transport models.

37.3.1 The Boltzmann Transport Equation

The BTE describing charge transport in semiconductors is an integro-differential equation in the seven-dimensional space $(\mathbf{r}, \mathbf{k}, t)$. Here $\mathbf{r}$ is the spatial variable, t is time, and the variable $\mathbf{k}$ is called the wave vector. Alternatively, one can use the crystal momentum $\mathbf{p} = \hbar\,\mathbf{k}$ as variable.

The BTE is a classical kinetic equation which reads for electrons [27]

$$\partial_t f + \mathbf{v}\cdot\nabla_{\mathbf{r}} f + \frac{\mathbf{F}}{\hbar}\cdot\nabla_{\mathbf{k}} f = C[f] - R[f]. \tag{37.33}$$

The operator C on the right-hand side is called the collision operator (see Sect. 37.3.5). In general, this operator is nonlinear and nonlocal in the variable $\mathbf{k}$. The operator R on the right-hand side describes generation/recombination terms and depends on the electron and hole distribution function (see Sect. 37.3.6). Mathematically, the operators C and R are integral operators nonlocal in k-space. Scattering and generation/recombination have an interpretation in terms of stochastic processes for classical point particles. In general, these operators depend also on any local impurities and material defects.

The quantity $\mathbf{v} = \mathbf{v}(\mathbf{r}, \mathbf{k})$ on the left-hand side in (37.33) is the group velocity of the carrier

$$\mathbf{v}(\mathbf{r}, \mathbf{k}) = \frac{1}{\hbar}\nabla_{\mathbf{k}}\mathcal{E}(\mathbf{r}, \mathbf{k}). \tag{37.34}$$

The energy of the carrier $\mathcal{E}(\mathbf{r}, \mathbf{k})$ is determined by the band structure of the material (see Sect. 37.3.2).

In (37.33), $\mathbf{F}$ is an external force exerted on the electrons, which in general depends on both $\mathbf{r}$ and $\mathbf{k}$. It is given as

$$\begin{aligned}\mathbf{F}(\mathbf{r}, \mathbf{k}) = &-\nabla_{\mathbf{r}} E_c(\mathbf{r}) \\ &-q\big(\mathbf{E}(\mathbf{r}) + \mathbf{v}(\mathbf{r}, \mathbf{k})\times\mathbf{B}(\mathbf{r})\big) \\ &-\nabla_{\mathbf{r}}\mathcal{E}(\mathbf{r}, \mathbf{k})\end{aligned} \tag{37.35}$$

where E_c is the conduction band minimum.

The Boltzmann equation is valid for general inhomogeneous materials with arbitrary band structure [28]. If the influence of the magnetic field is omitted and a homogeneous material is assumed, then $\mathbf{F}$ depends only on the local electric field as

$$\mathbf{F}(\mathbf{r}) = -q\,\mathbf{E}(\mathbf{r}). \tag{37.36}$$

Like in the drift-diffusion model (see Sect. 37.2.1), the electric field $\mathbf{E} = -\nabla\psi$ must be determined by Poisson's equation (37.2), where we have

$$\nabla\cdot(\varepsilon\nabla\psi) = q\,(n - p - N) \tag{37.37}$$

with N representing the net doping. The right-hand side contains the electron and hole concentrations, n and p. These are the zeroth-order moments of the distribution functions $f_n(\mathbf{r}, \mathbf{k}, t)$ and $f_p(\mathbf{r}, \mathbf{k}, t)$. For a complete description of the system of charge carriers, two Boltzmann equations with different physical parameters have to be solved self-consistently, one equation for the electron distribution f_n and a second one for the hole distribution f_p. The electron and hole ensembles

couple through the Poisson equation and through generation and recombination of electron-hole pairs. The coupling of the transport equations with the Poisson equation requires an iterative self-consistent solution procedure [6].

37.3.2 The Band Structure

For the evaluation of the transport equation, some information about the band energy $\mathcal{E}(\mathbf{r}, \mathbf{k})$ must be provided. The inverse effective mass tensor is defined by the second-order derivative of $\mathcal{E}(\mathbf{r}, \mathbf{k})$ as

$$\hat{\boldsymbol{m}}^{-1}(\mathbf{r}, \mathbf{k}) = \frac{1}{\hbar}\nabla_{\mathbf{k}} \otimes \mathbf{v}(\mathbf{r}, \mathbf{k}) \tag{37.38}$$

$$= \frac{1}{\hbar^2}\nabla_{\mathbf{k}} \otimes \nabla_{\mathbf{k}} \mathcal{E}(\mathbf{r}, \mathbf{k}) \tag{37.39}$$

where $\otimes$ denotes the tensor product.

A common assumption in macroscopic transport models is that the band structure is isotropic, that is, the kinetic energy depends only on the magnitude of the wave vector $\mathbf{k}$. Then, an isotropic effective mass approximation via the trace of the mass tensor is employed as [29]

$$m^{-1} = \frac{1}{3}\,\mathrm{tr}\,\langle \hat{\boldsymbol{m}}^{-1} \rangle. \tag{37.40}$$

The simplest isotropic model is given by a parabolic relationship between the energy and the crystal momentum $\mathbf{p} = \hbar\,\mathbf{k}$, which is assumed to be valid for energies close to the band minimum:

$$\mathcal{E} = \frac{p^2}{2m} \tag{37.41}$$

With increasing carrier energies, non-parabolic bands must be taken into account. A first-order non-parabolic relationship was given by Kane [30]. However, an analytical treatment of the corresponding carrier energy and group velocity is no longer possible.

In the parabolic case, we get for the group velocity

$$\mathbf{v} = \frac{\hbar\,\mathbf{k}}{m} = \frac{\mathbf{p}}{m} \tag{37.42}$$

and the band energy can be expressed in various equivalent ways as

$$\mathcal{E} = \frac{\hbar^2\,k^2}{2\,m} = \frac{p^2}{2\,m} = \frac{\mathbf{v}\cdot\mathbf{p}}{2} = \frac{m\,v^2}{2}. \tag{37.43}$$

Using the crystal momentum $\mathbf{p}$ as variable, the Boltzmann equation for electrons simplifies in the parabolic case for a homogeneous material to

$$\partial_t f + \frac{\mathbf{p}}{m}\cdot\nabla_{\mathbf{r}} f - q\,\mathbf{E}\cdot\nabla_{\mathbf{p}} f = C[f] - R[f] \tag{37.44}$$

where the left-hand side is the classical Liouville equation.

37.3.3 Macroscopic Observables

Rather than looking at the microscopic distribution function $f(\mathbf{r}, \mathbf{k})$ itself, a common simplification is to investigate only some macroscopic counterparts which are averages over $\mathbf{k}$-space. As a consequence, the moments no longer depend on $\mathbf{k}$ but only on $\mathbf{r}$. Macroscopic quantities are obtained by the integration of an according microscopic weight function multiplied by the distribution function f. A general moment of the distribution function can be defined as

$$\langle \Phi \rangle = \int \Phi f \; \mathrm{d}^3\mathbf{k} \tag{37.45}$$

with a suitable weight function $\Phi = \Phi(\mathbf{k})$. In the definition of the physical observables, we will use moments rescaled with a fixed constant:

$$\langle\!\langle \Phi \rangle\!\rangle = \frac{1}{4\pi^3}\langle \Phi \rangle \tag{37.46}$$

Here, the prefactor $1/(4\pi^3)$ incorporates the density of states in three-dimensional $\mathbf{k}$-space [31, p.26]. This factor is composed of the spin degeneracy which implies a factor of two; a further factor of $1/(2\pi)$ per degree of freedom results from the transition from discrete states to a continuum distribution function.

The moments contain information about the full microscopic distribution function, and they are used to define macroscopic observables or state variables. Some common physical observables (e.g., carrier temperature and velocity) are derived by additionally normalizing the moment with the local carrier concentration $n(\mathbf{r})$ (see table below). The angular bracket always denotes integration without normalization. As normalization of a distribution function is a nonlinear transformation, the models derived by the method of moments (see Sect. 37.4.1) are more naturally written in terms of (non-normalized) moments.

In the following, the group velocity $\mathbf{v}$ is separated into a random part $\mathbf{c}$ and the mean value $\bar{\mathbf{v}} = \langle\!\langle \mathbf{v} \rangle\!\rangle / \langle\!\langle 1 \rangle\!\rangle$ such that $\mathbf{c} = \mathbf{v} - \bar{\mathbf{v}}$. We then define the following symbols:

Electron density: $n = \langle\!\langle 1 \rangle\!\rangle$ (37.47)

Velocity: $\bar{\mathbf{v}} = \frac{1}{n}\langle\!\langle \mathbf{v} \rangle\!\rangle = -\frac{\mathbf{J}}{qn}$ (37.48)

Energy: $w = \frac{1}{n}\langle\!\langle \mathcal{E} \rangle\!\rangle$ (37.49)

$$\text{Thermal energy:}\quad w_{\mathrm{T}} = \frac{1}{n}\langle\!\langle \frac{m}{2}c^2 \rangle\!\rangle = \frac{3}{2}k_{\mathrm{B}}T_{\mathrm{n}} \tag{37.50}$$

$$\text{Energy flux:}\quad \mathbf{S} = \langle\!\langle \mathcal{E}\mathbf{v} \rangle\!\rangle \tag{37.51}$$

$$\text{Heat flux:}\quad \mathbf{Q} = \langle\!\langle \frac{m}{2}c^2\mathbf{c} \rangle\!\rangle. \tag{37.52}$$

Here T_{n} is the electron gas temperature and $\mathbf{J}$ the electron current density.

Macroscopic moments provide the link between the microscopic description in terms of a distribution function f and a phenomenological description such as described in Sect. 37.2. Using the method of moments (see Sect. 37.4), a system of equations for a given set of observables can be systematically derived from the Boltzmann equation.

37.3.4 Analytical Distributions

The Boltzmann equation can be solved approximately by making a suitable ansatz for the distribution function. An ansatz can also be used to derive closure relations for higher-order moment models (see Sect. 37.4.3). Important analytical classes of distribution functions are described below.

Fermi-Dirac and Maxwell-Boltzmann

The Fermi-Dirac and Maxwell-Boltzmann distribution functions (see Fig. 37.2) are frequently used to model the distribution of carriers in equilibrium which describes the case of a negligible applied electric field.

The Fermi-Dirac distribution is defined as

$$f(\mathbf{r},\mathbf{p}) = \frac{1}{1+\exp\left(\dfrac{E_{\mathrm{tot}}(\mathbf{r},\mathbf{p}) - E_{\mathrm{F}}}{k_{\mathrm{B}}T_{\mathrm{L}}}\right)} \tag{37.53}$$

$$E_{\mathrm{tot}}(\mathbf{r},\mathbf{p}) = E_{\mathrm{c}}(\mathbf{r}) + \mathcal{E}(\mathbf{r},\mathbf{p}). \tag{37.54}$$

For $E_{\mathrm{c}} \gg E_{\mathrm{F}}$, the Fermi-Dirac distribution (37.53) can be approximated by a Maxwell-Boltzmann distribution (see Fig. 37.3):

$$f(\mathbf{r},\mathbf{p}) = \exp\left(-\frac{E_{\mathrm{tot}}(\mathbf{r},\mathbf{p}) - E_{\mathrm{F}}}{k_{\mathrm{B}}T_{\mathrm{L}}}\right). \tag{37.55}$$

This is valid for nondegenerate, lowly doped semiconductors and corresponds to a neglect of the Pauli principle. While the assumption of lowly doped semiconductors is virtually never justified for semiconductor devices, the Maxwell-Boltzmann distribution is still preferentially used, since it gives closed-form results when integrated, for example, for the calculation of moments.

Rewriting the Maxwell distribution gives

$$\begin{aligned} f(\mathbf{r},\mathbf{p}) &= \exp\left(-\frac{E_{\mathrm{c}}(\mathbf{r}) + \mathcal{E}(\mathbf{r},\mathbf{p}) - E_{\mathrm{F}}}{k_{\mathrm{B}}T_{\mathrm{L}}}\right) \\ &= A\,\exp\left(-\frac{\mathcal{E}}{k_{\mathrm{B}}T_{\mathrm{L}}}\right). \end{aligned} \tag{37.56}$$

Here the prefactor A is given by

$$A = \exp\left(\frac{E_{\mathrm{F}} - E_{\mathrm{c}}(\mathbf{r})}{k_{\mathrm{B}}T_{\mathrm{L}}}\right) \tag{37.57}$$

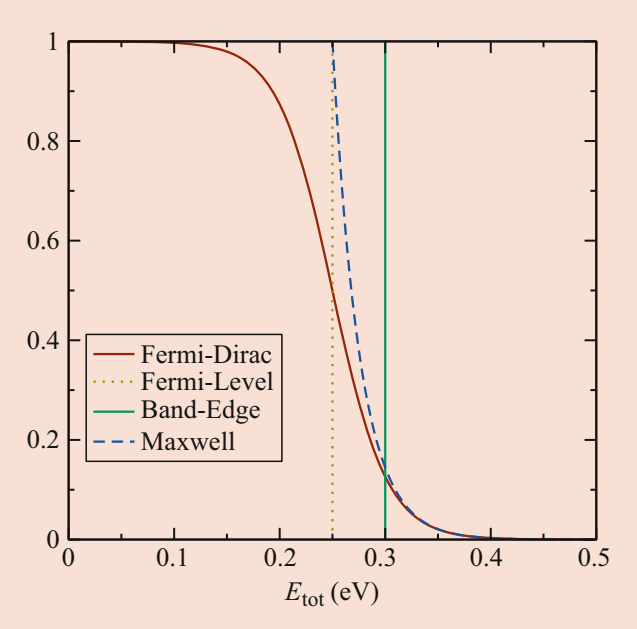

Fig. 37.2 Fermi-Dirac versus Maxwell-Boltzmann distribution

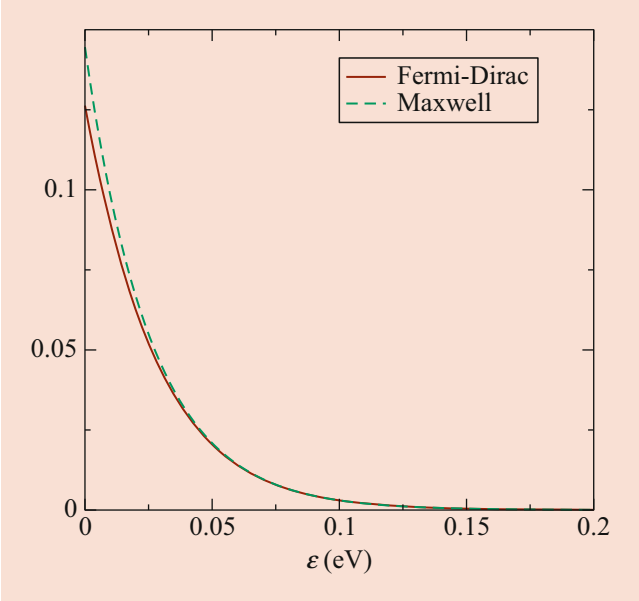

Fig. 37.3 In the limit $E_{\mathrm{c}} \gg E_{\mathrm{F}}$, the Fermi-Dirac distribution can be approximated by a Maxwell-Boltzmann distribution

and does not depend on **p**. For parabolic bands, we get

$$f(\mathbf{r},\mathbf{p}) = A\exp\Big(-\frac{\mathbf{p}^2}{2mk_{\mathrm{B}}T_{\mathrm{L}}}\Big). \tag{37.58}$$

which is often referred to as "cold Maxwellian," as the lattice temperature appears in it.

Heated Displaced Maxwellian

A heated displaced Maxwellian distribution function (also called shifted Maxwellian)

$$f_{\mathrm{sM}}(\mathbf{k}) = \exp\left(a + \mathbf{b}\cdot\mathbf{k} - c\,k^2\right) \tag{37.59}$$

is a frequently used ansatz for the distribution function in the Boltzmann equation. In terms of its moments (37.45), this distribution can be parameterized as

$$f(\mathbf{k}) = \frac{n_0}{(2\pi T_2)^{\frac{3}{2}}}\exp\Big(-\frac{(\mathbf{k}-\mathbf{k}_0)^2}{2T_2}\Big) \tag{37.60}$$

where

$$n_0 = \langle 1\rangle = \Big(\frac{\pi}{c}\Big)^{\frac{3}{2}}\exp\Big(a+\frac{b^2}{4c}\Big) \tag{37.61}$$

$$\mathbf{k}_0 = \frac{\langle\mathbf{k}\rangle}{n_0} = \frac{1}{2c}\,\mathbf{b} \tag{37.62}$$

$$T_2 = \frac{\langle(\mathbf{k}-\mathbf{k}_0)^2\rangle}{3\,n_0} = \frac{1}{2c}. \tag{37.63}$$

For $k_0 = 0$, we get a heated Maxwellian as a special case, while $k_0 \neq 0$ is required to result in a current density. Note, however, that a shifted Maxwellian has zero heat flow. Hence, this ansatz cannot represent solutions where the heat flow is physically relevant.

Diffusive Maxwellian

If the displacement **b** in (37.59) is small, then it is justified to approximate the shifted Maxwellian by a linearized shifted Maxwellian:

$$\begin{aligned} f(\mathbf{k}) &= \exp\left(a + \mathbf{b}\cdot\mathbf{k} - c\,k^2\right)\\ &= \exp\left(a - c\,k^2\right)\,\exp\left(\mathbf{b}\cdot\mathbf{k}\right)\\ &\approx f_{\mathrm{M}}(|\mathbf{k}|)\,(1+\mathbf{b}\cdot\mathbf{k}) = \tilde{f}(\mathbf{k}). \end{aligned} \tag{37.64}$$

Note that the distribution $\tilde{f}$ is no longer positive on all of $\mathbf{R}^3$. In terms of its moments (37.45), a linearized shifted Maxwellian can be parameterized as

$$\tilde{f}(\mathbf{k}) = \frac{n_0}{(2\pi M_2)^{\frac{3}{2}}}\exp\Big(-\frac{\mathbf{k}^2}{2M_2}\Big)\Big(1+\frac{\mathbf{k}\cdot\mathbf{k}_0}{M_2}\Big) \tag{37.65}$$

where

$$n_0 = \langle 1\rangle = \Big(\frac{\pi}{c}\Big)^{\frac{3}{2}}\exp(a) \tag{37.66}$$

$$\mathbf{k}_0 = \frac{\langle\mathbf{k}\rangle}{n_0} = \frac{1}{2c\,\mathbf{b}} \tag{37.67}$$

$$M_2 = \frac{\langle\mathbf{k}^2\rangle}{3\,n_0} = \frac{1}{2c}. \tag{37.68}$$

The expression "diffusive Maxwellian" stems from the fact that this distribution is implicitly used in the context of the diffusion approximation (see Sect. 37.5.1) to derive parabolic equation systems from the Boltzmann equation.

37.3.5 The Microscopic Relaxation Time Approximation

Electron transport is often dominated by the scattering operator. In a crude approximation, the collision term on the right-hand side of equation (37.33) represents the various scattering processes and can be approximately modeled as

$$C[f] \approx -\frac{f-f_0}{\tau} \tag{37.69}$$

which is commonly referred to as relaxation time approximation [32, p.144]. Here the index 0 represents the quasi-equilibrium distribution function $f_0(\mathbf{k})$. Depending on the type of model, both the distribution f_0 and the relaxation time τ can depend on the distribution function f or its moments. The relaxation time approximation can only be justified near quasi-equilibrium and even then only for specific types of scattering processes, i.e., elastic or isotropic. In contrast, energy relaxation by optical inter-valley scattering can hardly be accounted for by a relaxation time approximation.

One consequence of the relaxation time approximation is that the distribution decays exponentially toward its quasi-equilibrium value f_0 with the time constant τ, whenever it is disturbed from its quasi-equilibrium value. To allow for an easy analytic treatment, a Fermi-Dirac or a Maxwellian equilibrium distribution might be used. While this is a crude approximation, it allows for a straight forward numerical implementation. In a more rigorous way, scattering is modeled based on Fermi's golden rule and doping-dependent rates. A discussion on the validity of the relaxation time approximation is given in [31, p.139].

37.3.6 Microscopic Generation and Recombination

Similar to the relaxation time approximation for scattering, there are microscopic models for generation and recombina-

tion of electron-hole pairs. A simple model for generation/recombination is presented in [15].

The Shockley-Read-Hall model (see Sect. 37.2.4) has a microscopic formulation in terms of the distribution function f. The generation-recombination term $R[f]$ in the Boltzmann equation for electrons (37.33) is based on the assumption that generation-recombination occurs via a trap level E_t. Carriers in the valence and conduction band can be transferred to this trap level via phonon-assisted transitions. In k-space, the model reads

$$R[f] = \frac{1}{\tau_n}\left((1-f_t)f^e(k) - f_t \exp(-\tfrac{\mathcal{E}(k)-\mathcal{E}_t}{k_B T_L})\right). \quad (37.70)$$

Here f^e denotes the even part of the distribution function f, and f_t is the trap occupancy. The parameter $\mathcal{E}_t$ denotes the fixed trap level inside the semiconductor bandgap, while for the transition rates an energy-independent carrier lifetime τ_n is assumed. The simple model (37.70) allows for an analytical treatment under stationary conditions. Generation-recombination terms do not enter into the macroscopic flux equations, because $R[f]$ is an even function in k.

In general, generation/recombination terms depend on both, electron and hole distribution functions, in an integral, nonlocal manner [3]. This makes the task of solving the corresponding coupled transport equations for electrons and holes extremely difficult and represents a significant challenge [33].

37.4 Macroscopic Transport Models

To solve the Boltzmann equation deterministically by discretization of the differential and integral operators is computationally very expensive. A widely used stochastic method for solving the Boltzmann equation is the Monte Carlo method. The Monte Carlo method has been proven to give accurate results but may be computationally expensive, too. In particular, due to its stochastic nature, very large computation times are required for rare events. For instance, if the distribution of high energetic carriers is relevant or if the carrier concentration is very low in specific regions of the device, Monte Carlo simulations tend to produce high variance in the results.

An approximate deterministic solution method for the Boltzmann equation, which is often sufficient for TCAD demands, is the method of moments, which transforms the Boltzmann equation into a macroscopic transport model, i.e., a small system of partial differential equations in the four-dimensional space $(\mathbf{r}, t)$. The solution variables are a selected set of moments, which often correspond to macroscopic observables. In this section, we give the basic steps of this method.

37.4.1 The Method of Moments

The method of moments is characterized by multiplying the Boltzmann equation with weight functions and integrating the whole equation over $\mathbf{k}$-space. The moments of the distribution then become the unknowns of the equation system. The integration eliminates the coordinates in $\mathbf{k}$-space and leaves a set of partial differential equations in $(\mathbf{r}, t)$ space.

Generation and recombination processes are not considered in the following. Application of the method of moments to the Boltzmann equation gives the moment equations. For a general scalar Φ, we obtain a scalar equation:

$$\partial_t\langle\Phi_j\rangle + \nabla_{\mathbf{r}}\cdot\langle\mathbf{v}\,\Phi_j\rangle + q\,\mathbf{E}\cdot\langle\nabla_{\mathbf{p}}\Phi_j\rangle = \int \Phi_j\, C[f]\ \mathrm{d}^3\mathbf{k} \quad (37.71)$$

and for a vectorial $\mathbf{\Phi}$, we obtain a vectorial equation:

$$\partial_t\langle\mathbf{\Phi}_j\rangle + \nabla_{\mathbf{r}}\cdot\langle\mathbf{v}\otimes\mathbf{\Phi}_j\rangle + q\,\mathbf{E}\cdot\langle\nabla_{\mathbf{p}}\otimes\mathbf{\Phi}_j\rangle = \int \mathbf{\Phi}_j\, C[f]\ \mathrm{d}^3\mathbf{k} \quad (37.72)$$

where $\otimes$ denotes the tensor product [28]. In the derivation, partial integration for integrals over product terms of type $(\Phi\nabla_{\mathbf{p}} f)$ is used.

If we assume a parabolic band and a weight function Φ which is a (multivariate) polynomial in $\mathbf{p}$, then $\mathbf{v} = \frac{\mathbf{p}}{m}$, and the terms in the angular brackets on the left-hand side in the moment equations are polynomials again.

37.4.2 The Macroscopic Relaxation Time Approximation

In analogy to the microscopic relaxation time approximation, the collision term on the right-hand side of equations (37.71) and (37.72), which represents the various scattering processes, can be approximately modeled as

$$\int \hat{\mathbf{\Phi}}_j\, C[f]\ \mathrm{d}^3\mathbf{k} \approx -\frac{\langle\hat{\mathbf{\Phi}}_j\rangle - \langle\hat{\mathbf{\Phi}}_j\rangle_0}{\tau_{\hat{\mathbf{\Phi}}_j}} \quad (37.73)$$

which is commonly referred to as macroscopic relaxation time approximation [32, p.144]. Here the index 0 represents the average over the equilibrium distribution. Both the equilibrium moments and the relaxation times depend on moments of the distribution function f. In this approach, the moment decays exponentially toward its equilibrium value $\langle\hat{\mathbf{\Phi}}_j\rangle_0$ with the time constant $\tau_{\hat{\mathbf{\Phi}}_j}$ under homogeneous conditions. As we may have different time constants for each moment, the macroscopic relaxation time approximation is

in some way more general than the microscopic relaxation time approximation (37.69).

The equilibrium distribution function $f_0(\mathbf{k})$ is a symmetric function. Since the even weight functions are symmetric in $\mathbf{k}$ and the odd weight functions are antisymmetric in $\mathbf{k}$, only the even moments of the equilibrium distribution function will be nonzero, whereas the odd moments will vanish

$$\langle \mathbf{\Phi}_{j_{\text{odd}}} \rangle_0 = \int \mathbf{\Phi}_j(\mathbf{k}) f_0(\mathbf{k}) \, \mathrm{d}^3\mathbf{k} = 0. \tag{37.74}$$

Nonlinearity enters into the moment equations through the relaxation time approximation of the scattering operator, because both the equilibrium distribution f_0 (and hence its moments) and the relaxation time parameters τ depend on the distribution function f.

37.4.3 The Closure Problem

The weight functions for the moment method are usually chosen as being proportional to powers of increasing order of the wave vector $\mathbf{k}$ or equivalently (in the parabolic case) as powers of the momentum $\mathbf{p}$. Using polynomial weight functions of all orders, the method of moments transforms the parabolic band BTE into an infinite set of equations for the polynomial moments. To obtain a practically relevant model, the infinite hierarchy has to be truncated to a finite number of equations by restricting the set of weight functions to a finite number.

With this finite set of polynomial weight functions, an equation system containing only polynomial moments is obtained. The unknowns of the resulting system are the moments corresponding to the weight functions. However, in general, additional moments will show up, and the system will contain more unknowns than equations. The additional moments have to be expressed by the available moments. This is a nontrivial task and known as the closure problem.

A simple way to close the system of equations is to make a suitable ansatz for the shape of the distribution function. Then all moments can be calculated explicitly in terms of the ansatz parameters. With this kind of closure, the method of moments becomes equivalent to the Petrov-Galerkin method. This is a finite element method where the set of ansatz functions (e.g., shifted Maxwellians) and the set of test functions (e.g., polynomials) are not identical, in contrast to the usual Galerkin method. If the equation is linear and the ansatz is linear in the unknown parameters, we get a linear system of equations; else it is nonlinear (this would be the case for a shifted Maxwellian ansatz).

No form of the distribution function has to be assumed in the derivation of the moment equations, but in that case separate closure relations are needed. We can distinguish three types of closure relations:

- First, the highest-order moment closure. The equation of highest order contains the moment of the next order, which has to be suitably approximated using available information, typically the lower-order moments.
- Second, approximation of the tensors appearing in the equation system. They have to be expressed by the available scalar and vectorial moments in order to make the final equation system tractable.
- Finally, approximations for the moments of the scattering term. Practical implementations use the macroscopic relaxation time approximation and the closure problem consists in finding models for the mobilities and relaxation times. These parameters depend in general on all other moments.

37.4.4 Moment Equations for a Parabolic Band

Commonly used macroscopic models like hydrodynamic or energy transport models use polynomial moments up to order four. To derive a four-moment system, we use the following weight functions of even order:

$$\Phi_0 = 1 \tag{37.75}$$

$$\Phi_2 = \mathcal{E} = \frac{p^2}{2m} \tag{37.76}$$

while the weight functions for the odd orders are

$$\mathbf{\Phi}_1 = \mathbf{v} = \frac{\mathbf{p}}{m} \tag{37.77}$$

$$\mathbf{\Phi}_3 = \mathcal{E}\,\mathbf{v} = \frac{p^2}{2m}\frac{\mathbf{p}}{m}. \tag{37.78}$$

As will be seen, using these weight functions in the method of moments, the scalar weight functions will lead to the balance equations, whereas the vectorial weight functions will lead to the flux equations. The calculation of the gradients of the weight functions of even order is straightforward:

$$\nabla_{\mathbf{p}} \Phi_0 = 0 \tag{37.79}$$

$$\nabla_{\mathbf{p}} \Phi_2 = \mathbf{v} \tag{37.80}$$

while the gradients of the odd weight functions can be written as

$$\nabla_{\mathbf{p}} \otimes \mathbf{\Phi}_1 = \frac{\hat{\boldsymbol{\delta}}}{m} \tag{37.81}$$

$$\nabla_{\mathbf{p}} \otimes \mathbf{\Phi}_3 = \frac{\mathcal{E}}{m}\hat{\boldsymbol{\delta}} + \mathbf{v}\otimes\mathbf{v}. \tag{37.82}$$

Here $\hat{\boldsymbol{\delta}}$ is the unit matrix in three dimensions.

Applying the macroscopic relaxation time approximation and inserting the calculated gradients from the previous section into equations (37.71) and (37.72) lead to the equation set

$$\Phi_0: \quad \partial_t \langle 1\rangle + \nabla\cdot\langle\mathbf{v}\rangle = -\frac{\langle 1\rangle - \langle 1\rangle_0}{\tau_n} \tag{37.83}$$

$$\mathbf{\Phi}_1: \quad \partial_t \langle\mathbf{v}\rangle + \nabla\cdot\langle\mathbf{v}\otimes\mathbf{v}\rangle + \frac{q}{m}\mathbf{E}\cdot\langle\hat{\boldsymbol{\delta}}\rangle = -\frac{\langle\mathbf{v}\rangle}{\tau_v} \tag{37.84}$$

$$\Phi_2: \quad \partial_t \langle\mathcal{E}\rangle + \nabla\cdot\langle\mathbf{v}\,\mathcal{E}\rangle + q\,\mathbf{E}\cdot\langle\mathbf{v}\rangle = -\frac{\langle\mathcal{E}\rangle - \langle\mathcal{E}\rangle_0}{\tau_\mathcal{E}} \tag{37.85}$$

$$\mathbf{\Phi}_3: \quad \partial_t \langle\mathbf{v}\,\mathcal{E}\rangle + \nabla\cdot\langle\mathbf{v}\otimes\mathbf{v}\,\mathcal{E}\rangle + q\,\mathbf{E}\cdot\langle\frac{\mathcal{E}}{m}\hat{\boldsymbol{\delta}} + \mathbf{v}\otimes\mathbf{v}\rangle = -\frac{\langle\mathbf{v}\,\mathcal{E}\rangle}{\tau_S} \tag{37.86}$$

where τ_n, $\tau_m = \tau_v$, $\tau_\mathcal{E}$, and τ_S are the relaxation times for particle density, momentum/velocity, energy, and energy flux density, respectively.

Complementing the macroscopic observables already defined in Sect. 37.3.3, all moment equations will be written using the following observables [34]:

$$\text{Momentum:} \quad \bar{\mathbf{p}} = \frac{1}{n}\langle\!\langle\mathbf{p}\rangle\!\rangle \tag{37.87}$$

$$\text{Thermal tensor:} \quad \hat{\boldsymbol{T}} = \frac{1}{n}\langle\!\langle\frac{m}{2}\mathbf{c}\otimes\mathbf{c}\rangle\!\rangle \tag{37.88}$$

$$\text{Energy-like tensor:} \quad \hat{\boldsymbol{U}} = \frac{1}{n}\langle\!\langle\frac{1}{2}\mathbf{v}\otimes\mathbf{p}\rangle\!\rangle \tag{37.89}$$

$$\text{Fourth-order tensor:} \quad \hat{\boldsymbol{R}} = \frac{1}{n}\langle\!\langle\mathbf{v}\otimes\mathbf{p}\,\mathcal{E}\rangle\!\rangle. \tag{37.90}$$

In these definitions, the even moments w, $\hat{\boldsymbol{U}}$, $\hat{\boldsymbol{R}}$ are normalized, while the fluxes $\mathbf{J}$ and $\mathbf{S}$ are not. The energy tensor and thermal energy tensors are also known as stress and pressure tensor in fluid dynamics.

In the parabolic case, we get the following relations:

$$\bar{\mathbf{p}} = m\bar{\mathbf{v}} \tag{37.91}$$

$$w = \frac{1}{n}\langle\!\langle\mathcal{E}\rangle\!\rangle = \frac{1}{n}\langle\!\langle\frac{m}{2}v^2\rangle\!\rangle = \operatorname{tr}\hat{\boldsymbol{U}} \tag{37.92}$$

$$w_T = \frac{3}{2}k_B T_n = \frac{1}{n}\langle\!\langle\frac{m}{2}c^2\rangle\!\rangle = \operatorname{tr}\hat{\boldsymbol{T}} \tag{37.93}$$

Thus, the scalar values for the energy and the thermal energy are the traces of the corresponding tensors.

Average energy w and energy flux $\mathbf{S}$ are raw moments of second and third order. Temperature T_n and heat flux $\mathbf{Q}$ are (up to scaling) the corresponding central moments. In the parabolic case, central and raw moments are related by

$$w = w_T + \frac{m}{2}\bar{v}^2 \tag{37.94}$$

$$\hat{\boldsymbol{U}} = \hat{\boldsymbol{T}} + \frac{m}{2}\bar{\mathbf{v}}\otimes\bar{\mathbf{v}} \tag{37.95}$$

$$\mathbf{S} = \mathbf{Q} + 2n\hat{\boldsymbol{T}}\bar{\mathbf{v}} + nw_T\bar{\mathbf{v}} + n\frac{m}{2}\bar{v}^2\bar{\mathbf{v}}. \tag{37.96}$$

If we define convective energy as

$$w_{conv} = \frac{m}{2}\bar{v}^2, \tag{37.97}$$

the total energy is the sum of thermal and convective energy.

Introducing these state variables (moments) leads to the following form of the transport equations:

$$\Phi_0: \quad \partial_t n + \nabla\cdot n\bar{\mathbf{v}} = -\frac{n - n_0}{\tau_n} \tag{37.98}$$

$$\mathbf{\Phi}_1: \quad \partial_t(n\bar{\mathbf{v}}) + \frac{2}{m}\nabla\cdot n\hat{\boldsymbol{U}} + \frac{q}{m}n\,\mathbf{E} = -\frac{n\bar{\mathbf{v}}}{\tau_v} \tag{37.99}$$

$$\Phi_2: \quad \partial_t(nw) + \nabla\cdot\mathbf{S} - \mathbf{E}\cdot\mathbf{J} = -n\frac{w - w_0}{\tau_\mathcal{E}} \tag{37.100}$$

$$\mathbf{\Phi}_3: \quad \partial_t\mathbf{S} + \frac{1}{m}\nabla\cdot n\hat{\boldsymbol{R}} + q\,\mathbf{E}\Big(\frac{nw}{m} + 2\frac{n\hat{\boldsymbol{U}}}{m}\Big) = -\frac{\mathbf{S}}{\tau_S} \tag{37.101}$$

In three dimensions, this system consists of just eight equations (two scalar plus two vectorial) for the 19 unknowns $\{n, \bar{\mathbf{v}}, \hat{\boldsymbol{U}}, \mathbf{S}, \hat{\boldsymbol{R}}\}$. We also have to find models for the relaxation times. The limitations of the various possible moment models are a consequence of the closure problem and are discussed in the following.

37.4.5 Hydrodynamic Models

A hydrodynamic model for semiconductors was first introduced by Bløtekjær [9], who made several assumptions listed below to derive this system. Due to the hyperbolic nature and the resulting numerical challenges, hydrodynamic models are rarely used in macroscopic device simulation. However, hydrodynamic models are based on fewer assumptions than the energy transport models which actually can be derived from the hydrodynamic models by additional simplifications.

For this reason, the generic hydrodynamic transport model is discussed first. The energy transport models are discussed in Sect. 37.5.

We now consider only the first three moment equations (37.98)–(37.100) as originally done by Bløtekjær (see [9]). This system assumes a single effective parabolic energy band and consists of five equations (line $\mathbf{\Phi}_1$ is vectorial). The unknowns corresponding to the weight functions are $\{n, \bar{\mathbf{v}}, w\}$. Since we have $w = \frac{m}{2}\bar{v}^2 + \frac{3}{2}k_\mathrm{B}T_\mathrm{n}$, an equivalent set of unknowns is $\{n, \bar{\mathbf{v}}, T_\mathrm{n}\}$. All other moments appearing in the system have to be expressed through these unknowns.

Isotropic Symmetry

To reduce the number of unknowns, we use symmetry considerations for the thermal energy tensor. We can split the energy tensor according to (37.95):

$$\hat{\boldsymbol{U}} = \hat{\boldsymbol{T}} + \frac{m}{2}\bar{\mathbf{v}}\otimes\bar{\mathbf{v}} \tag{37.102}$$

The random component of the velocity has zero average, that is, $\langle \mathbf{c} \rangle = 0$. Under the assumption that the even part of the distribution of $\mathbf{c}$ is isotropic, the following relation can be derived:

$$\langle \mathbf{c}\otimes\mathbf{c} \rangle = \frac{1}{3}\langle c^2 \rangle \hat{\boldsymbol{I}} \tag{37.103}$$

This assumption is frequently considered to be justified because of the strong influence of scattering. With this assumption, we can represent the thermal energy tensor $\hat{\boldsymbol{T}}$ by a scalar temperature T_n:

$$\hat{\boldsymbol{T}} = \frac{w_T}{3}\hat{\boldsymbol{I}} = \frac{1}{2}k_\mathrm{B}T_\mathrm{n}\hat{\boldsymbol{I}} \tag{37.104}$$

With this assumption, (37.95) now becomes

$$\hat{\boldsymbol{U}} = \frac{1}{2}k_\mathrm{B}T_\mathrm{n}\hat{\boldsymbol{I}} + \frac{1}{2}m\bar{\mathbf{v}}\otimes\bar{\mathbf{v}} \tag{37.105}$$

and the six unknowns of the (symmetric) energy tensor $\hat{\boldsymbol{U}}$ are reduced to a single unknown T_n.

We employ the usual definition:

$$\mu = \frac{\mathrm{q}\,\tau_m}{\mathrm{m}} \tag{37.106}$$

where μ will be identified by the electron mobility in the drift-diffusion model, which is used in place of the momentum relaxation time.

With the isotropic approximations (37.104) and (37.105), the moment equations (37.98)–(37.100) can be written in the usual variables as [35]:

$$\nabla\cdot\mathbf{J} = \mathrm{q}\partial_\mathrm{t}n \tag{37.107}$$

$$\mathbf{J} - \frac{\tau_\mathrm{m}}{q}\nabla\cdot\left(\mathbf{J}\otimes\frac{\mathbf{J}}{n}\right) = \mu k_\mathrm{B}\nabla(nT_\mathrm{n}) + qn\mu\mathbf{E} - \tau_\mathrm{p}\partial_\mathrm{t}\mathbf{J} \tag{37.108}$$

$$\nabla\cdot\mathbf{S} = -\partial_\mathrm{t}(nw) + \mathbf{E}\cdot\mathbf{J} - n\frac{w-w_0}{\tau_\mathcal{E}}. \tag{37.109}$$

Note that we have set $n_0 = n$ in equation (37.98), i.e., we do not relax the carrier density. The equilibrium value w_0 is given as

$$w_0 = \frac{3}{2}k_\mathrm{B}T_\mathrm{L}. \tag{37.110}$$

Phenomenological Highest-Order Moment Closure

The third equation (37.109) needs to be closed in the energy flux $\mathbf{S}$. A suitable approximation for the energy flux $\mathbf{S}$ has to be found, and different approaches have been published. Assuming isotropic symmetry (37.104) and using definition (37.93), we can express $\mathbf{S}$ from equation (37.96) as

$$\mathbf{S} = (w + k_\mathrm{B}T_\mathrm{n})n\bar{\mathbf{v}} + \mathbf{Q} \tag{37.111}$$

which still contains the heat flux $\mathbf{Q}$ as unknown third-order moment.

A simple way to close the equation is to assume that f is a shifted Maxwellian. For a shifted Maxwellian, the heat flux $\mathbf{Q}$ vanishes which gives

$$\mathbf{S} = (w + k_\mathrm{B}T_\mathrm{n})n\bar{\mathbf{v}} = \left(\frac{5}{2}k_\mathrm{B}T_\mathrm{n} + \frac{m}{2}\bar{v}^2\right)n\bar{\mathbf{v}}. \tag{37.112}$$

By contrast, Bløtekjær [9] took a phenomenological approach and approximated the heat flux $\mathbf{Q}$ by Fourier's law as

$$\mathbf{Q} = -\kappa(T_\mathrm{n})\nabla T_\mathrm{n} \tag{37.113}$$

in which the thermal conductivity is given by the Wiedemann-Franz law as

$$\kappa(T_\mathrm{n}) = \left(\frac{5}{2} - p_\gamma\right)\left(\frac{k_\mathrm{B}}{q}\right)^2 q\mu n T_\mathrm{n} \tag{37.114}$$

where p_γ is an empirical correction factor.

Numerical Properties

Equations (37.107)–(37.109) yield the full hydrodynamic model for parabolic band structures. The system needs to be supplemented by Fourier's law (37.113) which is used in (37.111) to close the system. This equation system is similar to the Euler equations of fluid dynamics with the addition of a

heat conduction term and the collision terms. In the absence of electric fields and scattering terms, equations (37.107)–(37.109) together with the Maxwellian closure (37.112) correspond to the Euler equations of gas dynamics [13, p.201]. Mathematically, they constitute a quasilinear hyperbolic system of conservation laws since mass, momentum, and energy are conserved.

The hydrodynamic model describes the propagation of charge carriers in an electronic device as the flow of a compressible fluid. The electron gas has a sound speed of $v_c = \sqrt{k_B T_n / m^*}$, and the carrier flow may be either supersonic or subsonic. With $T_n = \xi T_L$ and $T_L = 300\,\mathrm{K}$, we have $v_c = \sqrt{\xi}\, 1.3 \times 10^7\,\mathrm{cm/s}$, while for $T_L = 77\,\mathrm{K}$, $v_c = \sqrt{\xi}\, 6.6 \times 10^6\,\mathrm{cm/s}$ [36]. Typical maximum carrier temperatures, which are observed experimentally inside electronic devices, give rise to sound speeds of about $5 \times 10^7\,\mathrm{cm/s}$ which is higher than the maximum velocities observed in typical simulations.

If the flow is supersonic, electron shock waves can occur inside the semiconductor device [36]. Such shock waves arise typically either at low temperatures or at a small length scale. In general, special numerical methods have to be applied, because the system of equations is hyperbolic [36–39]. For this type of system, the traditionally used Scharfetter-Gummel scheme [7] and its extension to the energy transport models [40–45] cannot be applied. A possible approximation consists in treating the convective term as a perturbation by freezing the dependence on the state variables at each step and using the values from the previous recursion [46]. However, in those cases where the temporal or spatial variation is important, this approach degrades the convergence [47]. In order to derive a numerically feasible spatial discretization, methods from fluid dynamics known as upwinding have been applied [47, 48]. In addition, the handling of the boundary conditions is more involved [39, 49].

These numerical properties make the hydrodynamic model challenging to solve, and the energy transport models discussed in the next section are virtually always preferred for practical device modeling.

37.5 Energy Transport Models

The hydrodynamic transport model introduced in Sect. 37.4.5 includes convective terms analogous to the differential equations in fluid dynamics. With these convective terms, we get a system of partial differential equations of hyperbolic type, which is difficult to solve with numerical methods. Therefore, in order to get rid of these inconvenient terms, the diffusion approximation is introduced. The resulting systems are of parabolic type which differs in the numerical properties from the original hyperbolic problem.

In the literature, there often is an arbitrary or synonymous use of the terms hydrodynamic transport and energy transport model. For the sake of consistency, the commonly employed three- or four-moment models incorporating the diffusion approximation should better be addressed as energy transport models [5]. Transport models based on the diffusion approximation are termed diffusive models, the prototypical example being the drift-diffusion model.

Assuming the validity of the diffusion approximation, we are now going to discuss two prototypical schemes to derive energy transport models from the Boltzmann equation which have been proposed by Stratton [8] and Bløtekjær [50], respectively. They use different variants of the method of moments and employ different strategies to close the system of equations.

37.5.1 The Diffusion Approximation

A heuristic way to motivate the diffusion approximation consists in analyzing the assumptions necessary for the derivation of the drift-diffusion model from the Boltzmann equation. We start with the first two equations of the hydrodynamic transport model:

$$\nabla \cdot \mathbf{J} = q \partial_t n \tag{37.115}$$

$$\mathbf{J} - \frac{\tau_m}{q} \nabla \cdot \left(\mathbf{J} \otimes \frac{\mathbf{J}}{n} \right) = \mu k_B \nabla (n T_n) + q n \mu \mathbf{E} - \tau_m \partial_t \mathbf{J} \tag{37.116}$$

This model assumes a parabolic band and an isotropic thermal energy tensor.

In order to derive the drift-diffusion model (37.26)–(37.27) from the hydrodynamic moment equations (37.115)–(37.116) for Φ_0 and $\mathbf{\Phi}_1$, we need two crucial assumptions which form the core of the diffusion approximation. Both assumptions can mathematically be justified in the framework of diffusion scaling [13, p.52].

First, we assume that the equation for the odd moment $\mathbf{J}$ is quasi-stationary. As signal frequencies are well below $1/(2\pi\tau_m) \approx 10^{12}\,\mathrm{Hz}$, the time derivative in (37.116) is neglected [51].

Second, the contribution of the drift kinetic energy to the carrier energy is frequently neglected:

$$w \approx \frac{3}{2} k_B T_n \tag{37.117}$$

This simplification is valid if the thermal energy is much larger than the convective energy (see Sect. 37.6.1 for a discussion of validity). Mathematically, we approximate the raw second-order moment by the central moment. The last assumption has an analogue for the energy tensor. We split the energy tensor according to equation (37.95):

$$\hat{\boldsymbol{U}} = \hat{\boldsymbol{T}} + \frac{m}{2}\bar{\mathbf{v}}\otimes\bar{\mathbf{v}} \tag{37.118}$$

and drop the convective tensor on the right-hand side, which gives

$$\hat{\boldsymbol{U}} \approx \frac{1}{2}k_{\mathrm{B}}T_{\mathrm{n}}\hat{\boldsymbol{I}}. \tag{37.119}$$

With this approximation, we can neglect the convective term:

$$\frac{\tau_{\mathrm{m}}}{\mathrm{q}}\nabla\cdot\left(\mathbf{J}\otimes\frac{\mathbf{J}}{n}\right) \tag{37.120}$$

in the current relation (37.108), and a parabolic equation system is obtained which only covers the subsonic flow regions. This is a very common approximation employed in virtually all device simulators, and we are not aware of any numerically robust scheme which can solve the HD model for realistic and relevant semiconductor devices.

With these simplifications, we still have the continuity equation (37.6) for Φ_0, and the equation (37.116) for $\boldsymbol{\Phi}_1$ turns into

$$\mathbf{J} = qn\mu\mathbf{E} + \mu k_{\mathrm{B}}\nabla(nT_{\mathrm{n}}). \tag{37.121}$$

This still differs from the drift-diffusion current relation:

$$\mathbf{J} = qn\mu\mathbf{E} + \mu k_{\mathrm{B}}T_{\mathrm{L}}\nabla n \tag{37.122}$$

with respect to the term inside the gradient operator. Only, if we assume that the carrier temperature T_{n} is in equilibrium with the lattice temperature T_{L} and that T_{L} is spatially homogeneous, then (37.121) and (37.122) are equivalent.

The derivation of the drift-diffusion model from the Boltzmann equation using the method of moments unmasks the assumptions behind the drift-diffusion model. The assumptions made above can be justified from a mathematical point of view in the sense that they follow consistently from appropriately scaling the BTE and taking the limit $\alpha \to 0$ of vanishing Knudsen number. This is discussed below.

37.5.2 Diffusion Scaling

The Knudsen number α appears as scaling parameter in the Boltzmann equation. It represents the mean free path $\tau_0 v_0$ relative to the device dimension [52]:

$$\alpha = \frac{\tau_0 v_0}{x_0} \tag{37.123}$$

τ_0 is the characteristic time between scattering events, v_0 denotes the velocity scale, and x_0 is given by the size of the simulation domain.

Macroscopic models assume that scattering is dominant in the sense that the mean free path is much smaller than the device dimension [13]. This means that a particle will undergo many collisions along its way through the device. Carriers in a semiconductor at room temperature can be considered a collision-dominated system, for which $\alpha \ll 1$.

The choice of the scaling – hydrodynamic or diffusive – depends on the equilibrium states associated with the collision operator [13, p.47]. Hydrodynamic scaling assumes the characteristic timescale of the system to be

$$t_0 = \frac{\tau_0}{\alpha}. \tag{37.124}$$

This means that we consider a timescale much larger than the collision time. Diffusion scaling assumes the characteristic timescale of the system to be even larger:

$$t_0 = \frac{\tau_0}{\alpha^2} \tag{37.125}$$

In diffusion scaling, the Boltzmann equation for electrons becomes (for parabolic bands)

$$\alpha^2\partial_t f + \alpha\left(\frac{\mathbf{p}}{m}\cdot\nabla_{\mathbf{r}}f - q\,\mathbf{E}\cdot\nabla_{\mathbf{p}}f\right) = C[f]. \tag{37.126}$$

The Boltzmann equation in diffusion scaling can be solved by a Hilbert expansion in the parameter α. This can be used to derive the drift-diffusion equations in a mathematically consistent way (see [13, p.106]). Using diffusion scaling (see [13, p.52]), one obtains that convective terms of the form $\langle\mathbf{v}\rangle\otimes\langle\mathbf{v}\rangle$ are negligible compared to $\langle\mathbf{v}\otimes\mathbf{v}\rangle$. Furthermore, in the diffusion approximation, the drift kinetic energy $\frac{1}{2}m\bar{v}^2$ is neglected against $\frac{3}{2}k_{\mathrm{B}}T_{\mathrm{n}}$, and in the flux equation, the time derivative is ignored. The validity of these assumptions for semiconductor devices is further discussed in Sect. 37.6.1.

37.5.3 Stratton's Approach

Historically, Stratton [8] performed one of the first derivations of an extended system of transport equations. This approach employs a parity decomposition, where the distribution function is split into even and odd parts:

$$f(\mathbf{r},\mathbf{k}) = f^{\mathrm{e}}(\mathbf{r},\mathbf{k}) + f^{\mathrm{o}}(\mathbf{r},\mathbf{k}) \tag{37.127}$$

Because of antisymmetry $f^o(\mathbf{r},-\mathbf{k}) = -f^o(\mathbf{r},\mathbf{k})$, it follows that $\langle f^o\rangle = 0$. Assuming a single microscopic relaxation time approximation for the collision operator

$$C[f] = -\frac{f - f_{\mathrm{eq}}}{\tau(\mathcal{E},\mathbf{r})} \tag{37.128}$$

the Boltzmann equation splits into two coupled equations which allows to express the odd part f^{o} as a function of f^{e} via

$$f^{\mathrm{o}} = -\tau(\mathcal{E}, \mathbf{r})\Big(\mathbf{v}\cdot\nabla_{\mathbf{r}} f^{\mathrm{e}} - \frac{\mathrm{q}}{\hbar}\mathbf{E}\cdot\nabla_{\mathbf{k}} f^{\mathrm{e}}\Big). \tag{37.129}$$

Stratton proposes a power law for the microscopic relaxation time;

$$\tau(\mathcal{E}) = \tau_0\Big(\frac{\mathcal{E}}{k_{\mathrm{B}}T_{\mathrm{L}}}\Big)^{-p_\nu} \tag{37.130}$$

Assuming that f^{e} is a heated Maxwellian distribution, the equation system below is obtained:

$$\nabla\cdot\mathbf{J} = q\partial_t n \tag{37.131}$$

$$\mathbf{J} = q\mu n\mathbf{E} + k_{\mathrm{B}}\nabla(n\mu T_{\mathrm{n}}) \tag{37.132}$$

$$\nabla\cdot\mathbf{S} = -\frac{3}{2}k_{\mathrm{B}}\partial_{\mathrm{t}}(nT_{\mathrm{n}}) + \mathbf{E}\cdot\mathbf{J} - \frac{3}{2}k_{\mathrm{B}}n\frac{T_{\mathrm{n}}-T_{\mathrm{L}}}{\tau_{\mathcal{E}}} \tag{37.133}$$

$$\mathbf{S} = -\Big(\frac{5}{2} - p_\nu\Big)\Big(\mu n k_{\mathrm{B}}T_{\mathrm{n}}\mathbf{E} + \frac{K_{\mathrm{B}}^2}{\mathrm{q}}T_{\mathrm{n}}\nabla(n\mu T_{\mathrm{n}})\Big). \tag{37.134}$$

The inclusion of mobility within the gradient operator in (37.132) is incorrect if doping is not homogeneous and mobility is doping-dependent. In his original paper [8], Stratton discussed a Schottky-barrier junction where doping was assumed to be uniform. This is probably why he included mobility within the gradient operator [53].

Equation (37.132) can be rewritten as

$$\mathbf{J} = q\mu\Big(n\mathbf{E} + \frac{k_{\mathrm{B}}}{q}T_{\mathrm{n}}\nabla n + \frac{k_{\mathrm{B}}}{q}n(1+\nu_{\mathrm{n}})\nabla T_{\mathrm{n}}\Big) \tag{37.135}$$

with

$$\nu_{\mathrm{n}} = \frac{T_{\mathrm{n}}}{\mu}\frac{\partial\mu}{\partial T_{\mathrm{n}}} = \frac{\partial\ln\mu}{\partial\ln T_{\mathrm{n}}} \tag{37.136}$$

which has to be considered a fitting parameter with common values in the range $[-1.0, -0.5]$, since no analytic expression for μ is known. Note that the thermal diffusion term vanishes for $\nu_{\mathrm{n}} = -1.0$.

A problem with the formulation (37.130) for τ is that p_ν has to be approximated in order to cover all scattering processes. Particularly, in the presence of impurity scattering, the parameter p_ν is in the range $[-1.5, 0.5]$, which depends on charge screening [54]. Hence, the average value is dependent on the applied field and on the doping profile, and it is not possible to give a unique value for p_ν.

37.5.4 Bløtekjær's Approach

Without requiring any assumptions on the form of the distribution function, Bløtekjær [9] derived conservation equations by taking the moments of the Boltzmann equation using the weight functions 1, $\hbar\mathbf{k}$, and $\mathcal{E}$, which define the moments of zeroth, first, and second order. The exposition in Sects. 37.4.4 and 37.4.5 is in line with Bløtekjær's approach. The resulting system of equations can be written as follows [34]:

$$\partial_{\mathrm{t}} n + \nabla\cdot(n\bar{\mathbf{v}}) = nC_{\mathrm{n}} \tag{37.137}$$

$$\partial_{\mathrm{t}}(n\bar{\mathbf{p}}) + \nabla\cdot(n\hat{\boldsymbol{U}}) - n\mathbf{F} = n\mathbf{C}_{\mathrm{m}} \tag{37.138}$$

$$\partial_{\mathrm{t}}(nw) + \nabla\cdot\mathbf{S} - n\bar{\mathbf{v}}\cdot\mathbf{F} = nC_{\mathcal{E}} \tag{37.139}$$

Under the assumption that the carrier mass is position-independent, these equations are valid for arbitrary band structures. In the case of a position-dependent mass, additional force terms have to be included in (37.137)–(37.139) [55].

Bløtekjær originally proposed the concept of macroscopic relaxation times introducing one relaxation time for each moment equation:

$$\mathbf{C}_{\mathrm{m}} = -\frac{\bar{\mathbf{p}}}{\tau_{\mathrm{m}}} \tag{37.140}$$

$$C_{\mathcal{E}} = -\frac{w - w_0}{\tau_{\mathcal{E}}} \tag{37.141}$$

which introduces the momentum and energy relaxation times τ_{m} and $\tau_{\mathcal{E}}$, respectively. A discussion of this approximation is given in [56]. Recombination processes are neglected here; thus, $C_{\mathrm{n}} = 0$.

Three-Moment Energy Transport Model

Bløtekjær's system of equations is not closed, because it contains more unknown moments than equations. In order to express the equations by the moments n, $\bar{\mathbf{v}}$, and w (or T_{n}), closure relations have to be introduced.

Customarily, parabolic bands are assumed, and the closure relations (37.91), (37.94), and (37.95) for $\bar{\mathbf{p}}$, $\hat{\boldsymbol{U}}$, and w can be used. In addition, Bløtekjær assumed an isotropic temperature tensor (37.105) and the same phenomenological closure for the highest-order moment as in his hydrodynamic model, i.e., an energy flux based on Fourier's law (37.113) and (37.114). Bløtekjær also used the diffusion approximation as discussed above for the drift-diffusion equation (Sect. 37.5.1). The resulting simplified equations are

$$\nabla\cdot\mathbf{J} = q\partial_t n \tag{37.142}$$

$$\mathbf{J} = \mu k_{\mathrm{B}}\nabla(nT_{\mathrm{n}}) + qn\mu\mathbf{E} \tag{37.143}$$

$$\nabla \cdot \mathbf{S} = -\frac{3}{2}k_\mathrm{B}\partial_\mathrm{t}(nT_\mathrm{n}) + \mathbf{E}\cdot\mathbf{J} - \frac{3}{2}k_\mathrm{B}n\frac{T_\mathrm{n}-T_\mathrm{L}}{\tau_\mathcal{E}} \tag{37.144}$$

$$\mathbf{S} = -\frac{5}{2}\frac{k_\mathrm{B}T_\mathrm{n}}{q}\mathbf{J} - \kappa(T_\mathrm{n})\nabla T_\mathrm{n} \tag{37.145}$$

Equations (37.142)–(37.145) form a typical three-moment model which has been closed using Fourier's law and is commonly known in the literature as energy transport model. Actually, this name is somewhat misleading as the model consists of the two conservation equations (37.142) and (37.144) and the two transport equations (37.143) and (37.145); the latter transport equation is empirical.

In the case of a homogeneous and stationary bulk silicon system, the energy balance equation (37.144) reduces to

$$n\frac{w-w_0}{\tau_\mathcal{E}} = \boldsymbol{E}\cdot\mathbf{J}. \tag{37.146}$$

With

$$w_0 = \frac{3}{2}k_\mathrm{B}T_\mathrm{L} \tag{37.147}$$

$$w = \frac{3}{2}k_\mathrm{B}T_\mathrm{n} \tag{37.148}$$

$$\mathbf{J} = q\mu\boldsymbol{E}n \tag{37.149}$$

one obtains from the homogeneous energy balance equation (37.146) the following relation between the carrier temperature and the electric field [10]:

$$T_\mathrm{n} = T_\mathrm{L} + \frac{2}{3}\frac{\mathrm{q}}{k_\mathrm{B}}\tau_\mathcal{E}\mu E^2 \tag{37.150}$$

The estimated temperature T_n is roughly proportional to the square of the electric field.

Four-Moment Energy Transport Model

To overcome the difficulties associated with the Fourier law closure (37.113) which is empirical and leaves κ undefined, an additional moment equation of the BTE can be taken into account [34]. From (37.101), we have

$$\partial_\mathrm{t}\mathbf{S} + \frac{1}{m}\nabla\cdot n\hat{\boldsymbol{R}} + q\mathbf{E}\Big(\frac{nw}{m} + 2\frac{n\hat{\boldsymbol{U}}}{m}\Big) = -\frac{\mathbf{S}}{\tau_\mathrm{S}}. \tag{37.151}$$

In this equation, the time derivative can be ignored using the same scaling argument that led to a neglect of the time derivative in (37.138). The energy flux mobility is defined in analogy to the mobility as

$$\mu_\mathrm{S} = \frac{q\tau_\mathrm{S}}{m}. \tag{37.152}$$

This gives

$$\mathbf{S} = -\frac{\mu_\mathrm{S}}{q}\Big(\nabla\cdot(n\hat{\boldsymbol{R}}) - qn\mathbf{E}(w+2\hat{\boldsymbol{U}})\Big). \tag{37.153}$$

A closure relation for $\hat{\boldsymbol{R}} = \frac{1}{n}\langle\mathbf{v}\otimes\mathbf{p}\,\boldsymbol{\mathcal{E}}\rangle$ has to be introduced, which can be obtained, for example, by assuming a heated Maxwellian distribution. This gives the Maxwellian closure

$$\hat{\boldsymbol{R}} = \frac{5}{2}k_\mathrm{B}^2T_\mathrm{n}^2\hat{\boldsymbol{I}}. \tag{37.154}$$

Together with the scalar isotropic diffusion approximation

$$(w+2\hat{\boldsymbol{U}}) \approx \frac{5}{2}k_\mathrm{B}T_\mathrm{n} \tag{37.155}$$

one obtains the closure for a four-moment model.

$$\mathbf{S} = -\frac{5}{2}k_\mathrm{B}\frac{\mu_\mathrm{S}}{q}\Big(\nabla(k_\mathrm{B}nT_\mathrm{n}^2) + qnT_\mathrm{n}\mathbf{E}\Big) \tag{37.156}$$

Discussion of Bløtekjær's Closure

The closure (37.156) should be compared with Bløtekjær's phenomenological closure:

$$\mathbf{S} = -\frac{5k_\mathrm{B}T_\mathrm{n}}{2q}\mathbf{J} - \kappa(T_\mathrm{n})\nabla T_\mathrm{n} \tag{37.157}$$

$$\kappa(T_\mathrm{n}) = \Big(\frac{5}{2}-p_\gamma\Big)\Big(\frac{k_\mathrm{B}}{q}\Big)^2 q\mu nT_\mathrm{n}. \tag{37.158}$$

For that purpose, one now rewrites in (37.156)

$$\nabla(nT_\mathrm{n}^2) = T_\mathrm{n}\big(\nabla(nT_\mathrm{n}) + n\nabla T_\mathrm{n}\big). \tag{37.159}$$

Using (37.121) and (37.159), one gets the following expression for the closure (37.156) of the four-moment model:

$$\mathbf{S} = -\frac{5}{2}k_\mathrm{B}T_n\frac{\mu_\mathrm{S}}{q}\Big(k_\mathrm{B}n\nabla T_\mathrm{n} + \frac{\mathbf{J}}{\mu}\Big) \tag{37.160}$$

The last form allows for a direct comparison with Bløtekjær's phenomenological closure. From (37.160), it follows that Bløtekjær's closure and the four-moment closure become identical if $\mu_\mathrm{S}/\mu = 1$ and $p_\gamma = 0$ in the three-moment model. However, Monte Carlo simulations show that the ratio μ_S/μ strongly depends on the average energy and shows a pronounced hysteresis, when plotted over the average energy as shown in Fig. 37.4a. Similar observations can be made for the electron mobility [34], which is shown in Fig. 37.4b. In essence, this implies that neither μ nor μ_S can be accurately expressed as a function of w or T_n.

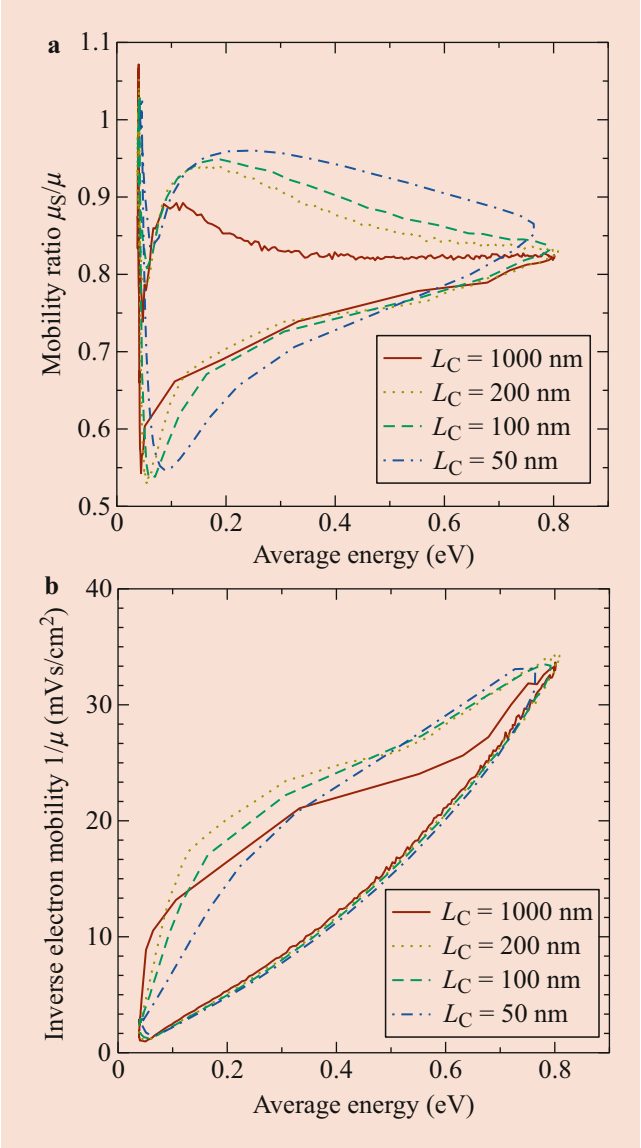

Fig. 37.4 (**a**) Ratio of μ_S and μ as a function of the carrier temperature inside the n^+nn^+ test structures obtained from Monte Carlo simulations. (**b**) Electron mobility inside n^+nn^+ test structures obtained from Monte Carlo simulations

37.5.5 Relaxation Times and Carrier Mobilities

Due to the scattering operator in Boltzmann's equation, the relaxation times and mobilities depend on the distribution function. Since the distribution function is not uniquely determined by the average energy, models only based on the average energy are bound to fail. Furthermore, the band structure can play a dominant role. Nevertheless, all models should be able to correctly reproduce the homogeneous limit for which there is a unique relationship between the electric field and the carrier temperature. Hence, the relaxation times and the mobilities are often derived from homogeneous field measurements or Monte Carlo simulations. In the following, the most commonly used analytical transport parameter models for silicon are discussed. Table-based parameter modeling is discussed later in Sect. 37.7.3.

Mobility

Two models for the energy dependence of the mobility are frequently used, the model after Baccarani and Wordeman [57]:

$$\frac{\mu(T_\mathrm{n})}{\mu_0} = \frac{T_\mathrm{L}}{T_\mathrm{n}} \tag{37.161}$$

and the one-dimensional model going back to Hänsch [58]:

$$\frac{\mu(T_\mathrm{n})}{\mu_0} = \left(1 - \frac{3}{2}\frac{\mu_0}{\tau_\mathcal{E} v_\mathrm{s}^2}\left(\frac{k_\mathrm{B}T_\mathrm{L}}{\mathrm{q}} - \frac{2}{5}\frac{nS}{J}\right)\right)^{-1}. \tag{37.162}$$

Here, μ_0 is the zero-field mobility.

Under homogeneous conditions, the energy flux is proportional to the particle current:

$$\mathbf{S} = \frac{5}{2}\frac{k_\mathrm{B}T_\mathrm{n}}{q}\mathbf{J} \tag{37.163}$$

which can be used to simplify (37.162) to

$$\frac{\mu(T_\mathrm{n})}{\mu_0} = \left(1 + \frac{3}{2}\frac{\mu_0 k_\mathrm{B}}{q\tau_\mathcal{E} v_\mathrm{s}^2}\left(T_\mathrm{n} - T_\mathrm{L}\right)\right)^{-1}. \tag{37.164}$$

As has been shown in [34,59], expression (37.164) reproduces the mobility quite well in the regions with increasing **E**. However, for decreasing **E**, equation (37.162) should be used [34, 60], which, unfortunately, is numerically very difficult due to the vector-valued fluxes **J** and **S**, particularly in two or three dimensions.

In Fig. 37.5, the three models are compared with parameters extracted from Monte Carlo simulation data. All models have been evaluated using the data from the Monte Carlo simulation for an n^+nn^+ test structure with $L_\mathrm{c} = 200\,\mathrm{nm}$, once with $E_\mathrm{max} = 100\,\mathrm{kV/cm}$ and once with $E_\mathrm{max} = 300\,\mathrm{kV/cm}$. For electric fields smaller than 100 kV/cm, equation (37.162) gives reasonable results but breaks down for larger electric fields. Equation (37.162) is the only model that captures the hysteresis properly and, shown in Fig. 37.5a, thus the mobility at the beginning of the drain region. The hysteresis in the other models stems from the doping dependence of μ_0.

Energy Relaxation Time

The simplest and most commonly used model for the energy relaxation time $\tau_\mathcal{E}$ is a constant value. Typically used values for electrons in silicon at room temperature are in the range [0.3, 0.4 ps], although values in the range [0.08, 0.68 ps] have been used [61]. A constant value is justified in view of the fact

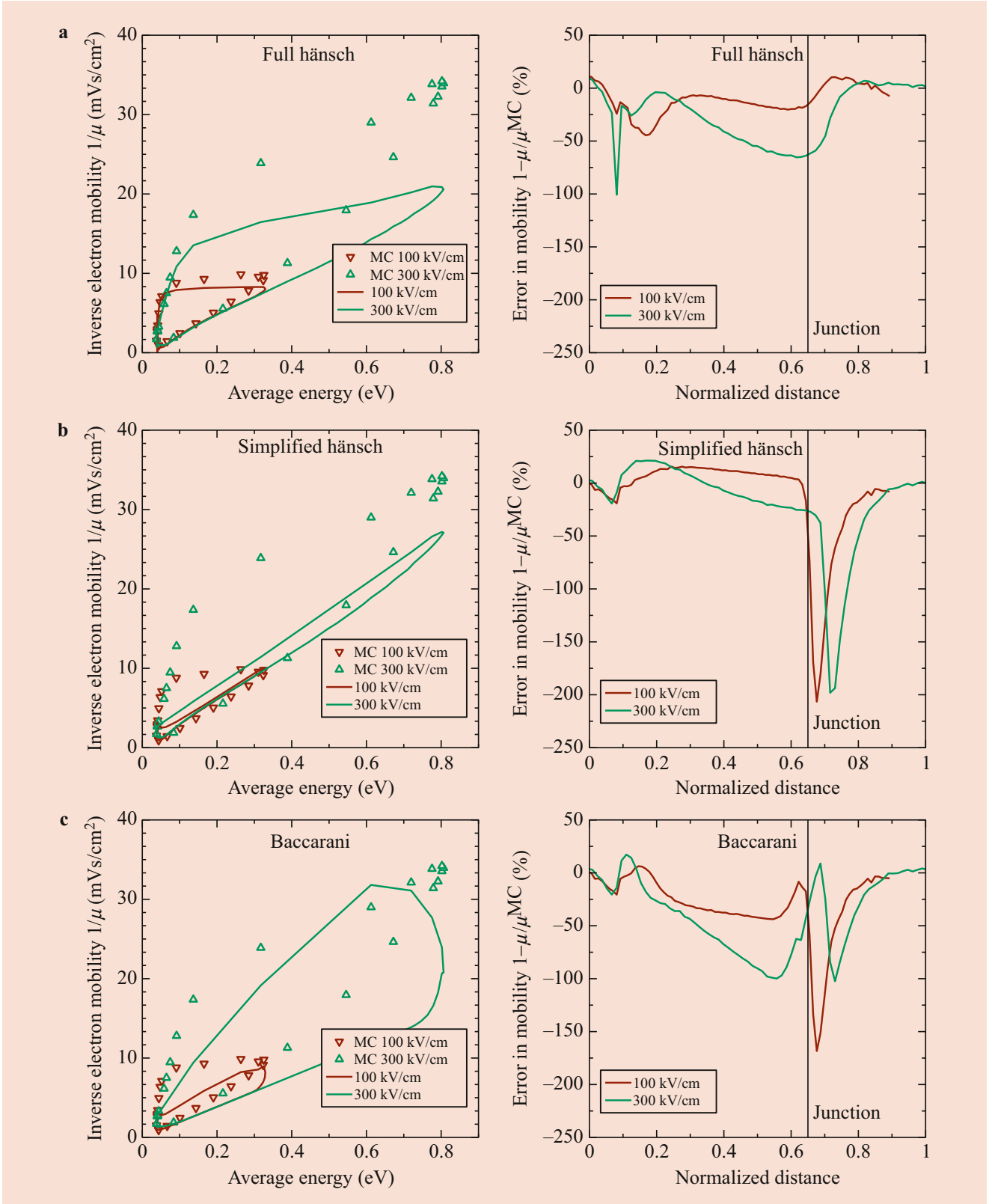

Fig. 37.5 Comparison of the full Hänsch model (**a**), simplified Hänsch model (**b**) and Baccarani mobility model (**c**). The three different mobility models (solid lines) are plotted in contrast to Monte Carlo simulation data (symbols). Only the full Hänsch model (37.162) covers the hysteresis appropriately, at least for lower fields

that Monte Carlo simulations show only a small hysteresis and a small energy dependence [62]. However, different energy dependencies have been published. The differences seem to originate from the different band structures employed in the various Monte Carlo simulation codes.

Based on theoretical considerations, Baccarani and Wordeman [57] proposed the expression

$$\tau_{\mathcal{E}}(T_\mathrm{n}) = \frac{3}{2}\frac{k_\mathrm{B}\mu_0}{qv_\mathrm{s}^2}\frac{T_\mathrm{n}T_\mathrm{L}}{T_\mathrm{n}+T_\mathrm{L}} + \frac{m\mu_0}{2q}\frac{T_\mathrm{n}}{T_\mathrm{L}} \tag{37.165}$$

which should be used together with (37.161) to correctly reproduce the homogeneous limit. Within Hänsch's approach, $\tau_{\mathcal{E}}$ is only required to be independent of the carrier temperature for (37.162) to correctly predict the homogeneous limit. When

$$\tau_{\mathcal{E}} = \frac{3}{2}\frac{k_\mathrm{B}\mu_0 T_\mathrm{L}}{qv_\mathrm{s}^2} \tag{37.166}$$

is used in the Hänsch mobility models (37.162) and (37.164), the models are equivalent to Baccarani's model in the homogeneous case.

37.5.6 Bløtekjær Versus Stratton Approach

Stratton's closure (37.134) is quite different from the four-moment closure (37.156), and it is not clear if both models can be made consistent with each other by a special choice of parameters. A thoroughly discussed difference between Bløtekjær's approach and Stratton's approach is the position of the mobility relative to the gradient in the current relation:

$$\begin{aligned}\text{Bløtekjær}: &\ \mu_1\nabla(nT_\mathrm{n})\\ \text{Stratton}: &\ \nabla(n\mu_2 T_\mathrm{n})\end{aligned}$$

Stratton himself has addressed this issue in [63], and it has also been discussed by Landsberg [64,65]. Further comparisons of the two formulations are given in [60,66–69]. In both formulations, the parameters μ_1 and μ_2 are called mobilities, but these parameters actually differ substantially in their definition. The formulations are compared in [60], and both approaches can be justified if the respective mobilities are modeled properly. The mobilities are equal in the case of bulk simulations and are suitably expressed using energy-dependent models [20,58]. However, in the nonhomogeneous case where the electric field changes abruptly, the mobilities are no longer a single-valued function of the temperature.

The formulation based on μ_1 has the advantage that it can be approximated by its bulk value for increasing values of the electric field, whereas the value of μ_2 is always different from the bulk case. Hence, μ_1 is more useful for numerical simulation as it can be approximately modeled as a function of the temperature. Using an empirical ansatz for $\mathbf{C}_\mathrm{m}$, namely

$$\mathbf{C}_\mathrm{m} = \mathbf{C}_\mathrm{m}^* + \lambda_\mathrm{p}\nabla\cdot\hat{\boldsymbol{U}} \tag{37.167}$$

where λ_p is a dimensionless transport coefficient and $\mathbf{C}_\mathrm{m}^*$ is the homogeneous component, Tang et al. [62] demonstrated that the formulation of Stratton is obtained from Bløtekjær's with $\lambda_\mathrm{p} = \eta_\mathrm{n}$, where

$$\eta_\mathrm{n} = -\frac{T_\mathrm{n}}{\mu^*}\frac{\partial\mu^*}{\partial T_\mathrm{n}}. \tag{37.168}$$

In this expression, $\mu^* = \mu^*(T_\mathrm{n})$ is the bulk mobility which is representable as a function of the temperature. The variable η_n, as given by (37.168), is analogous to $-\nu_\mathrm{n}$, given by (37.136) in the Stratton model. However, by comparing Monte Carlo simulation results, it has been demonstrated that $\lambda_\mathrm{p} \neq \eta_\mathrm{n}$ in the inhomogeneous case [70].

37.6 Limits of Validity for Drift-Diffusion and Energy Transport Models

The range of validity for macroscopic models such as drift-diffusion and energy transport models has been extensively examined [71,72]. When the critical dimensions of devices shrink below a certain value (around 200 nm for silicon at room temperature), Monte Carlo simulations reveal strong off-equilibrium transport effects such as velocity overshoot and nonlocality of important model parameters.

In this section, we start with a discussion of the simplifying assumptions used in the previous sections to derive numerically feasible transport models from the Boltzmann equation.

Then we study energy distribution functions for one-dimensional $\mathrm{n}^+\mathrm{nn}^+$ test structures. Energy transport models use up to four moments of the distribution function, while the highest even moment included is the temperature. Based on Monte Carlo simulation results, it is demonstrated that below 100 nm the energy distribution function strongly deviates from a Maxwellian shape in test structures.

Finally, we compare results from a drift-diffusion model and an energy transport model with Monte Carlo simulation data. In contrast to the drift-diffusion model, higher-order models such as the energy transport model can describe nonlocal effects such as the velocity overshoot as they can make use of the information available in the additional moments.

37.6.1 Critical Issues

The moment-based hydrodynamic and energy transport models given in the previous sections are based on various sim-

plifying assumptions and employ several approximations of different severity. These approximations are crucial to derive numerically feasible models, and they will be discussed in the following.

Non-parabolic Band Structure

Many employed models are based on the single effective parabolic band model. Due to its simplicity, a closed-form solution for the single effective parabolic band model exists, while, even for the relatively simple non-parabolicity correction model by Kane [30], it is not possible to obtain a closed-form representation of the moment equations. Non-analytic table-based correction-terms describing non-parabolicity can be added to macroscopic transport models [73, 74].

Tensor Quantities and Anisotropy

So far we have barely discussed the assumption of isotropic symmetry used in the approximation of tensors by scalar quantities like the carrier mass and temperature. This type of simplification is used in both hydrodynamic and energy transport models.

One-dimensional simulations carried out in [34] demonstrate that the transverse temperature component T_{yy} is smaller than the longitudinal temperature component T_{xx}. This is an indicator that there is an elongation of the distribution function in the direction of the electric field and hence the assumed isotropic symmetry of the energy tensor is not valid (Fig. 37.6). The rigorous approach taken in [75] models all components of the temperature tensor. For ballistic diodes and bipolar transistors, no substantial difference between the scalar temperature and the trace of the temperature tensor is found. In contrast, a difference of up to 15% in the linear region of the transfer characteristics is observed for aggressively scaled MOSFETs.

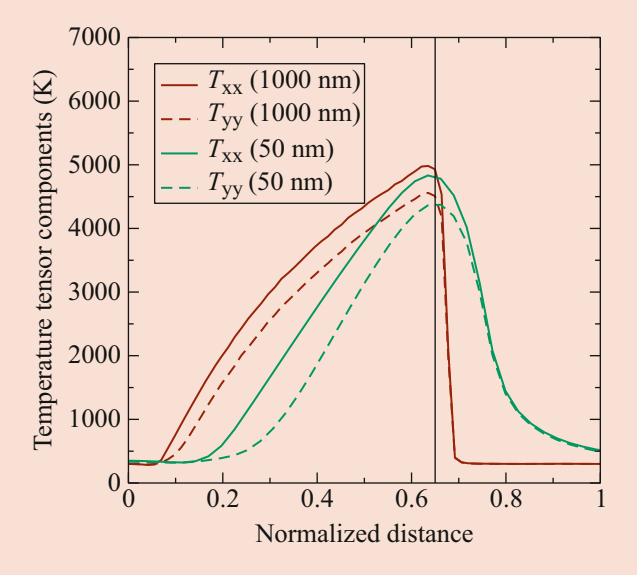

Fig. 37.6 Main components of the temperature tensor $\hat{\boldsymbol{T}}$ for two different n^+nn^+ test structures

Drift Energy Versus Thermal Energy

Another common approximation [76] is to neglect the drift kinetic energy in the average carrier energy:

$$w = \frac{1}{2}m\bar{v}^2 + \frac{3}{2}k_\mathrm{B}T_\mathrm{n} \approx \frac{3}{2}k_\mathrm{B}T_\mathrm{n}. \tag{37.169}$$

However, as has been pointed out by Baccarani and Wordeman [57], the convective energy can reach values comparable to the thermal energy. A plot of the ratio

$$\frac{\frac{1}{2}m\bar{v}^2}{\langle \mathcal{E} \rangle} \tag{37.170}$$

inside n^+nn^+ test structures is given in Fig. 37.7a. As can be seen, the error introduced by neglecting the kinetic energy can reach 30% at the beginning of the channel where the carrier temperature is still low and a velocity overshoot is observed. This effect has been studied in [57, 77].

When looking at the moment equations, it can be seen that not only the absolute value of the convective energy but also its gradient is important. A plot of the ratio

$$\frac{\nabla \frac{1}{2}m\bar{v}^2}{\nabla \langle \mathcal{E} \rangle} \tag{37.171}$$

based on one-dimensional data is given in Fig. 37.7b which indicates that this term becomes increasingly important for nanoscale devices. In particular, pronounced spikes are observed at both junctions.

Highest-Order Moment Closure

The equation of highest order contains the moment of the next order which has to be suitably approximated using available information, typically the lower-order moments. As the lower-order equations remain unchanged by this choice, it is worth noting that the whole information about the remaining higher-order equations has to be packed into this closure.

One approach to derive a suitable closure relation is to assume a distribution function and calculate the fourth-order moment. Typically, a heated Maxwellian distribution is assumed [10]. This assumption is problematic, because it only uses partial, and in general insufficient, information about the distribution function.

Mobilities and Relaxation Times

Particularly in the diffusion-dominant regime, the scattering operator is dominant in the Boltzmann equation and must be modeled with sufficient care [13]. The physical mecha-

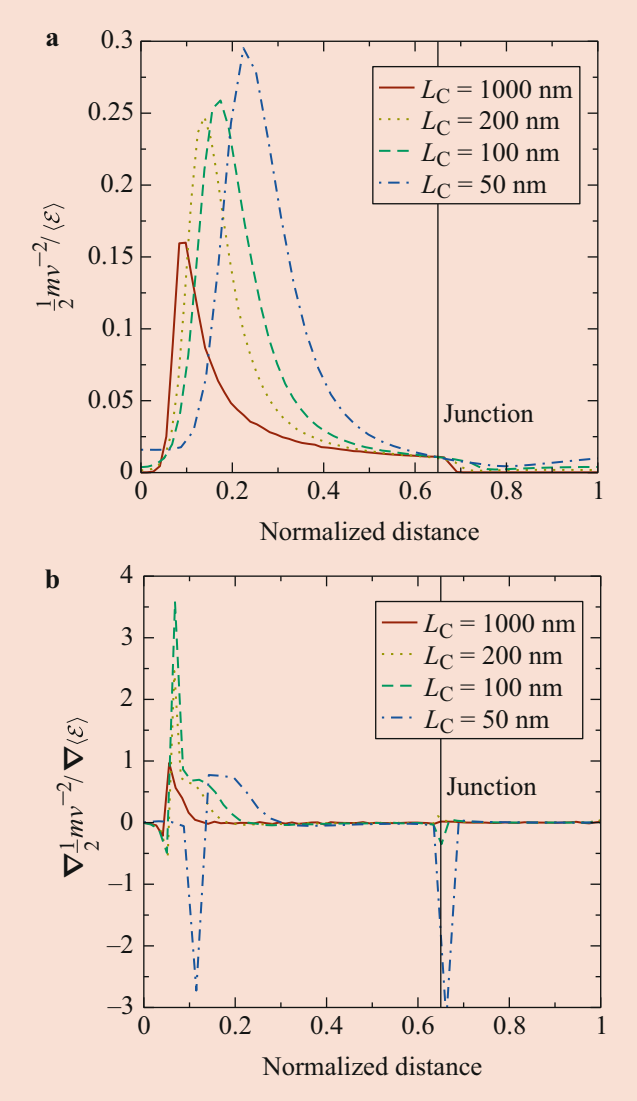

Fig. 37.7 The ratio of $m\bar{v}^2/2$ and $\langle\mathcal{E}\rangle$ and the ratio of the gradients for different n^+nn^+ test structures

nisms behind scattering are typically described using Fermi's golden rule. Using macroscopic transport models, scattering is approximated by transport parameters such as mobilities and relaxation times. From the Boltzmann equation, it is clear that these parameters depend on the full distribution function through the collision operator. Since the distribution function is not uniquely described by the average energy, models based solely on the average energy have limited validity particularly at the drain side of MOSFETs. However, from a practical perspective, this is the only viable option found so far. In order to increase their accuracy, table-based models depending on doping, temperature, and carrier energy can be extracted from bulk Monte Carlo simulations, which is discussed in Sect. 37.7.3.

Complexity of Models

Modeling of carrier transport is far more complex than can be described in this work. Accurate, but complex models for a lot of physical effects from different domains are available. To give just one example, we have hardly discussed the intricacies of carrier generation and recombination. But practical engineering approaches will often rely on fitted analytical models. Models must also be numerically feasible, and one has to compromise between numerical costs and physical sophistication. Handling the trade-off between model accuracy and numerical costs is the craft of technology computer-aided design.

37.6.2 Non-Maxwellian Energy Distribution

Test structures with n^+nn^+ topology exhibit similar features as a MOSFET or a bipolar transistor like, e.g., a distinctive velocity overshoot and a mixture of a hot and a cold distribution in the drain region. As such, given their simplicity, they have been very popular for the study of the basic behavior of macroscopic transport models for very small devices within n^+nn^+ structures without the additional levels of complexity introduced by two-dimensional MOS devices [73, 78].

Qualitative Analysis

Monte Carlo simulations indicate that the shape of the distribution function inside an n^+nn^+ test structure behaves qualitatively as shown in Fig. 37.8.

For cold carriers injected at the contacts, the Maxwellian shape provides a good description. In Region I, carriers diffuse against the built-in energy barrier. While moving along Region I, the amount of low-energy carriers in the distribution function decreases due to reflection at the energy barrier. Therefore, unlike predicted by the Maxwellian approximation, only the low-energy range of the energy distribution is filtered out, whereas nearly no changes in the high-energy tail are observed.

It is interesting to note that inside the channel the slope in the low-energy range is almost the same as at the end of the channel. However, the knee energy E_1, which is the energy of the kink between different slopes of the distribution function, changes. It shifts toward higher energies as the carriers travel through the channel in Region II.

In Region III, the small number of hot carriers from the channel meets the large pool of cold carriers in the drain, which is visible in the distribution function by a rapid increase of the low-energy part. Region III is very small, and there is little change in the high-energy tail. As the hot carriers travel through Region IV, the temperature of the high-energy tail relaxes to the equilibrium temperature.

It will be argued in Sect. 37.7.2 that the kurtosis β of the distribution function, which is defined as the fourth-

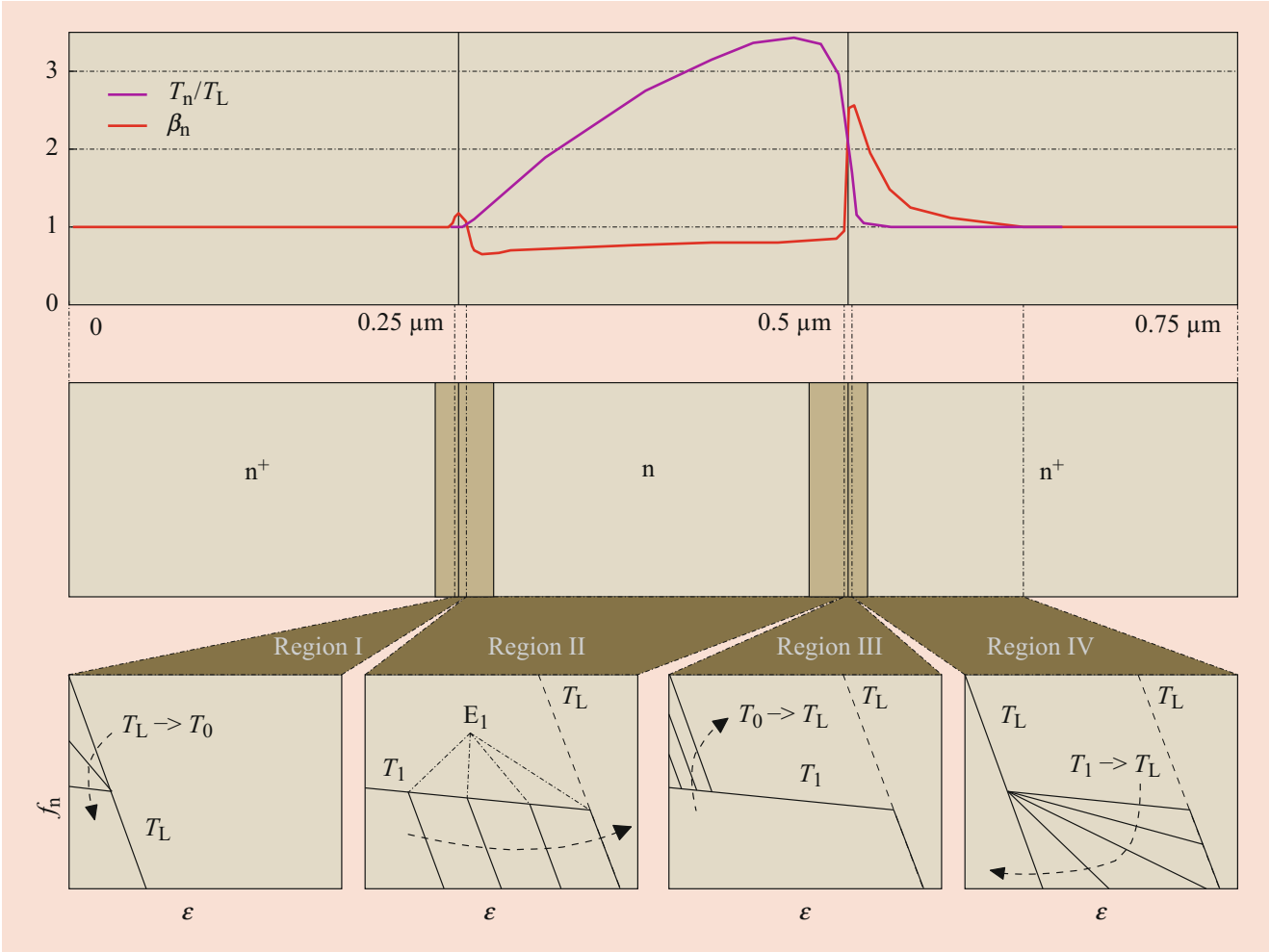

Fig. 37.8 Schematic evolution of the distribution function inside an n^+nn^+ test structure

order standardized moment, provides enough information to distinguish between different regions of the test structure. This provides the basis for the development of more accurate models.

Shape of the Distribution Function

The transport models discussed so far only contain moments up to, and including at most, the third order. In general, the distribution function is insufficiently described by these moments. The only even moments available are the zeroth- and the second-order moment which correspond to particle density and average energy. These moments are the parameters of a heated Maxwell distribution function which often gives only a poor approximation to the actual energy distribution.

This is demonstrated for an n^+nn^+ test structure with $L_c = 200\,\text{nm}$ in Fig. 37.9. Here, the energy distribution function, which is obtained from Monte Carlo simulations, is shown for four characteristic points inside the structure. For points A and C, which have the same average energy, the distribution function is completely different. In particular, the mixture of a cold and a hot-carrier population leads to an inadequate description via the average carrier energy. In such cases, the extension of the energy transport model to a six-moment transport model (see Sect. 37.7.2) increases the accuracy significantly.

A heated Maxwellian distribution neither captures the basic shape of the energy distribution function nor the change in the shape when the end of the channel is reached. This is shown in Fig. 37.10 where the failure of the Maxwellian approximation is obvious. The error is largest for high energetic carriers where the tail of the distribution function is severely either overestimated or underestimated.

The importance of the high-energy tail increases with decreasing channel length. This issue becomes crucial for modeling short-channel and hot-carrier effects, e.g., for gate tunneling or hot-carrier degradation, which will be discussed in Sect. 37.8.3.

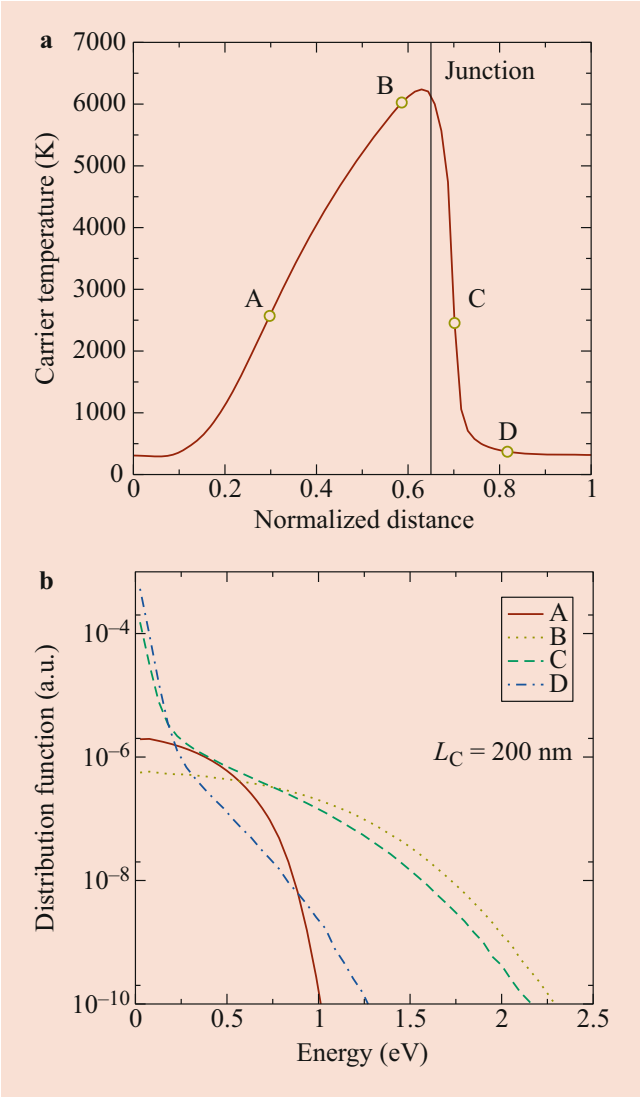

Fig. 37.9 Electron temperature (**a**) and distribution functions (**b**) at four characteristic points inside an n^+nn^+ test structure with L_c = 200 nm. The average energies at points A and C are the same, whereas the distribution function looks completely different. Note the high-energy tail at point D where the carrier temperature is 370 K

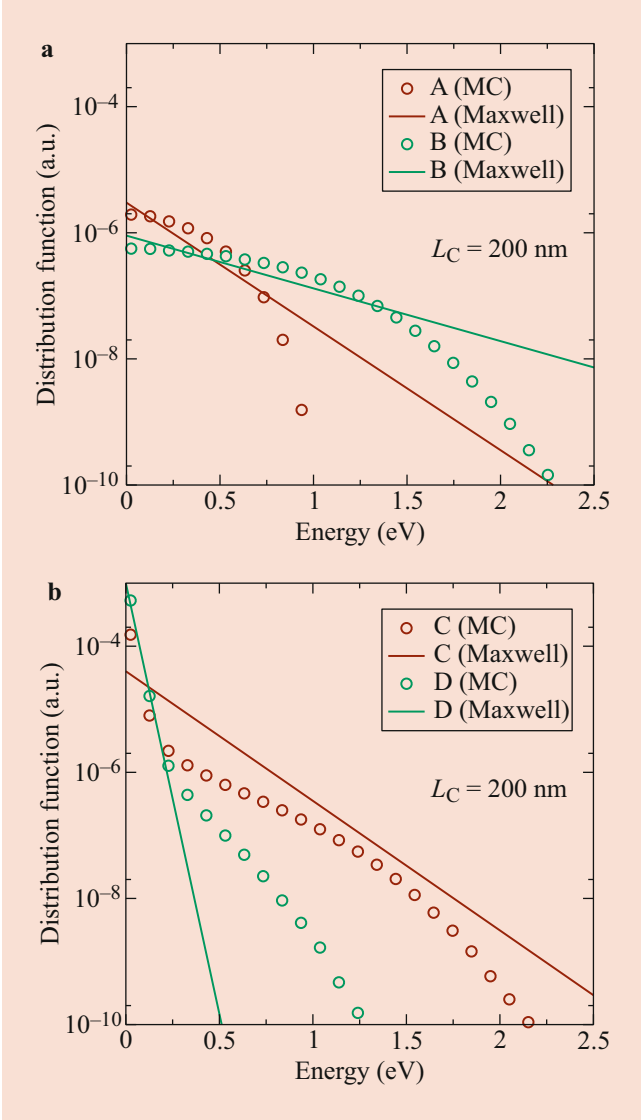

Fig. 37.10 The heated Maxwellian distribution approximation at the four characteristic points of Fig. 37.9. (**a**) Inside the channel, the number of hot electrons is dramatically overestimated because the Maxwell distribution cannot reproduce the thermal tail. (**b**) Inside the drain region, a cold and a hot population are visible, which cannot be resolved with a single Maxwell distribution

37.6.3 Numerical Evaluation

In order to check the validity of the drift-diffusion and energy transport models, we compare simulations of MOS transistors as a function of the channel length.

Modeling of Velocity Overshoot

The carrier velocity in most devices operating near room temperature and under modest bias condition is always limited by scattering. For constant or slowly varying electric fields, carriers cannot go beyond a certain saturation velocity $v_{sat} = 10^7$ cm/s. However, as demonstrated in Fig. 37.11, for short-channel devices, the situation is different. As the channel length decreases, the gradient of the electric field inside the device increases as well. Thus, the carriers will be accelerated without colliding with the lattice ($T_n = T_L$) for at least a few picoseconds. Therefore, the random component of the carrier velocity induced by scattering events is small, which leads to a maximum drift velocity in the range of 10^7 cm/s to 10^8 cm/s [79]. This is known as the velocity overshoot.

In the energy transport model, T_n is an independent solution variable, while in the drift-diffusion model, T_n is only estimated through a local relationship via the electric field. Neglecting diffusion, the velocity follows the mobility as $\bar{v} =$

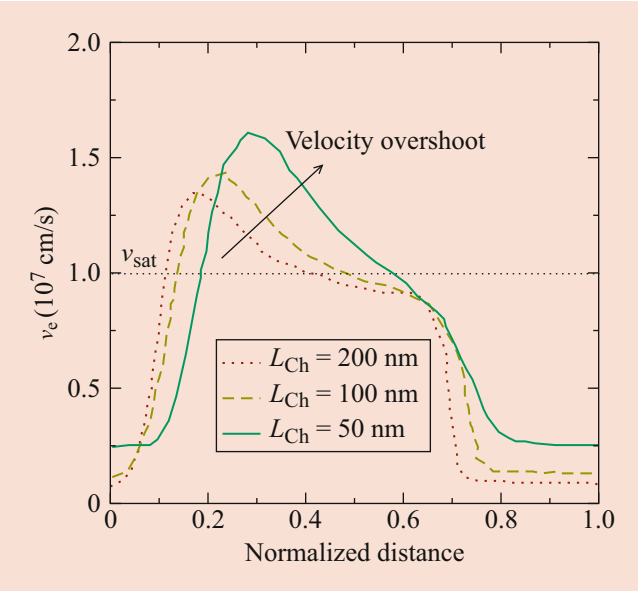

Fig. 37.11 Velocity profiles of a 50 nm, 100 nm, and 200 nm long n^+nn^+ structure calculated with the Monte Carlo method are presented after [10]. The velocity overshoot at the beginning of the lowly doped n-region is clearly visible

μE. Commonly used analytical models for carrier mobilities in the energy transport and drift-diffusion models are given as

$$\text{Energy transport model: } \mu = \mu_0 \frac{T_\mathrm{L}}{T_\mathrm{n}}$$

$$\text{Drift} - \text{diffusion model: } \mu = \mu_0 \frac{1}{1 + \frac{E}{E_\mathrm{crit}}}.$$

Here $E_\mathrm{crit} \approx 10\,\mathrm{kV/cm}$ is the critical field and μ_0 is the zero-field mobility. With this simple model, the velocity in the drift-diffusion model saturates at $v_\mathrm{sat} = \mu_0 E_\mathrm{crit}$.

The drift-diffusion mobility follows the field, while the energy transport mobility follows the temperature. Comparing models, we see that the drift-diffusion mobility model estimates the electron temperature via the electric field as

$$T_\mathrm{n} = T_\mathrm{L}(1 + E/E_\mathrm{crit}). \tag{37.172}$$

In reality, however, the response of the distribution f to the electric field is delayed, because carriers need time to pick up the energy from the field.

As a consequence, this can result in an overshoot in the carrier velocity for rapidly varying electric fields. The reason for this velocity overshoot is that the mobility depends on distribution function rather than on the electric field. As the mobility has not yet been reduced by the increasing temperature but the electric field is already high, an overshoot in the velocity $\bar{v} = \mu E$ is observed until the carrier energy comes into equilibrium with the electric field again. One of the first works dealing with this effect is [80]. Such nonlocal effects cannot be properly modeled using the common drift-diffusion transport model.

Limitations of the Drift-Diffusion Model

It was found in [71] through a comparison with Monte Carlo simulations that relaxation time-based models tend to overestimate nonstationary carrier dynamics, especially the energy distribution.

Figure 37.12 compares the drift-diffusion estimate for temperature with results from Monte Carlo simulations for various MOS transistors. The gate length varies from 1000 nm (Fig. 37.12a) down to 100 nm (Fig. 37.12d). These and other simulation results demonstrate that the drift-diffusion model is a good approximation down to a gate length of about 250 nm but becomes increasingly inaccurate below. At shorter gate lengths, the carrier energy does no longer directly follow the field. In most regions, the temperature is overestimated by the drift-diffusion model. In some parts, it is also underestimated.

For the same MOS transistors as before, we also compare the velocity between the drift-diffusion model and results from Monte Carlo simulations (see Fig. 37.13). The critical gate length for this example is $L_\mathrm{G} \approx 350\,\mathrm{nm}$ (Fig. 37.13b). At 100 nm (Fig. 37.13d), one can see a significant velocity overshoot in a large portion of the channel. This velocity overshoot is not modeled correctly by the drift-diffusion model where the velocity is bounded by v_sat.

Drift-Diffusion Versus Energy Transport

Banoo and Lundstrom [72] compared the results obtained by (37.142)–(37.145) with a drift-diffusion model and a solution of the BTE obtained by using the scattering matrix approach. They found that the used variant of the energy transport model dramatically overestimates both the drain current and the velocity inside the device.

Figure 37.14 shows the IV characteristics from drift-diffusion and energy transport models and compares them with Monte Carlo simulation results. For long-channel devices with $L_\mathrm{G} \approx 1\,\mu\mathrm{m}$, all models yield the same results (not shown here). At 250 nm (Fig. 37.14a), the models are still close. For submicron devices with $L_\mathrm{G} \approx 100\,\mathrm{nm}$ (Fig. 37.13b), the energy transport model is closer to Monte Carlo simulation results. For short-channel devices with $L_\mathrm{G} \approx 50\,\mathrm{nm}$ (Fig. 37.14c), the energy transport model overestimates the current. In Fig. 37.14d at a channel length of $L_\mathrm{G} \approx 25\,\mathrm{nm}$, the drift-diffusion is even better than the energy transport model.

To better understand this behavior, one may look at the distributed quantities inside the transistor, for instance, the velocity profile. Figure 37.15a shows the velocity profile for a channel length of 250 nm Fig. 37.15b, for 50 nm, and Fig. 37.15c for and 25 nm, respectively. While the velocity in

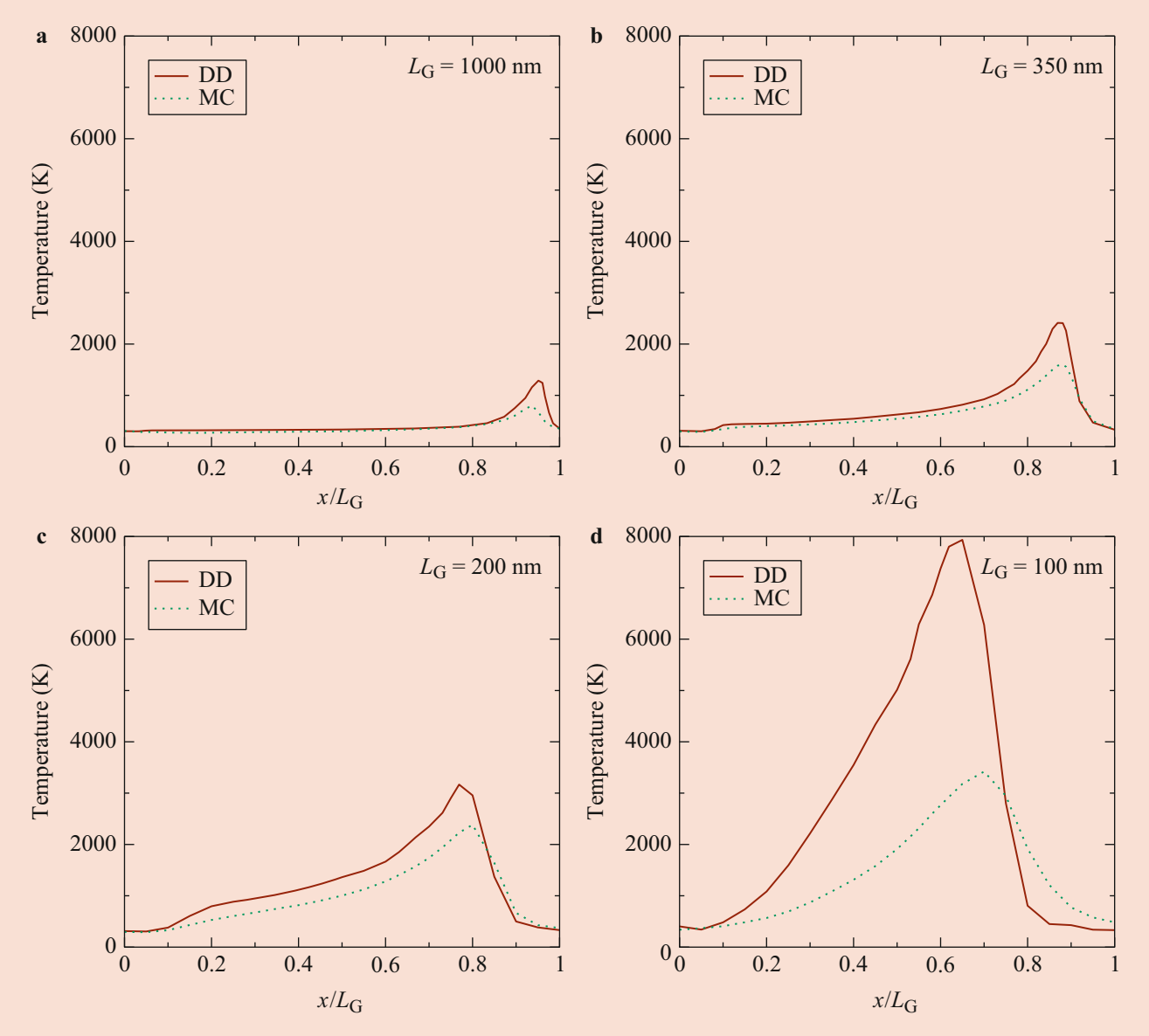

Fig. 37.12 Comparison of temperature approximated within the drift-diffusion model with Monte Carlo simulation results for MOSFETs with gate lengths of 1000 nm (**a**), 350 nm (**b**), 200 nm (**c**), and 100 nm (**d**). Drift-diffusion results provide a reasonable approximation till a gate length of 200 nm

the drift-diffusion model is always bounded, the Monte Carlo simulation results show a velocity overshoot. This is quite well matched in the energy transport model at 250 nm. However, at shorter-channel lengths, the velocity is overestimated in the energy transport model, and at 25 nm, the velocity profile of the energy transport model is far off from Monte Carlo simulation results.

Spurious Velocity Overshoot

Compared to drift-diffusion models, energy transport models have advantages concerning the modeling of velocity overshoot in the main channel region. However, when the electric field decreases rapidly, these models also tend to show a nonphysical (spurious) velocity overshoot. This is the case, for instance, at the end of the channel of a MOSFET. The same effect is more pronounced in n^+nn^+ test structures (see Sect. 37.8.1 for more simulation results). Models based on Bløtekjær's approach have been frequently associated with such nonplausible spikes in the velocity characteristics which do not occur in Monte Carlo simulations. Since the velocity overshoot at the end of the channel is not observed by Monte Carlo simulations, this effect is known as the spurious velocity overshoot (SVO) [81–83].

In [34], this spurious velocity overshoot is investigated using different mobility models. It is found that improved results are possible when proper mobility models are used.

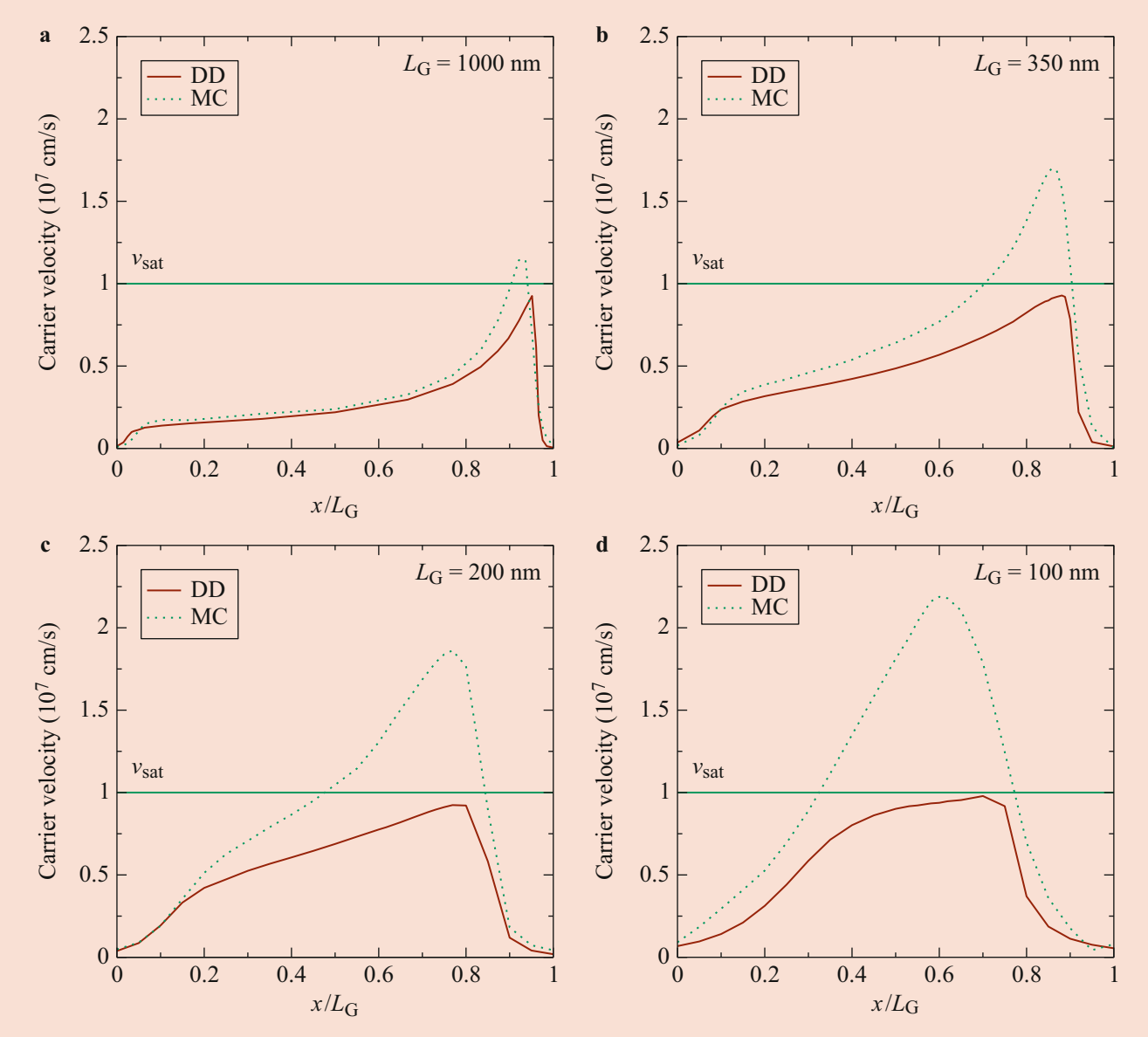

Fig. 37.13 Comparison of the velocity calculated by the drift-diffusion model with Monte Carlo simulation results for MOSFETs with varying gate lengths of 1000 nm (**a**), 350 nm (**b**), 200 nm (**c**), and 100 nm (**d**). At 350 nm and below, Monte Carlo simulation results show a velocity overshoot. Velocity in the drift-diffusion model stays bounded

For example, with Hänsch's mobility model (37.162), these spikes are strongly diminished but not completely removed. Unfortunately, Monte Carlo simulations show that (37.162) also overestimates the real velocity overshoot at the beginning of the channel.

37.7 Advanced Macroscopic Transport Models

As device geometries are further reduced without according reduction of the supply voltages, the electric fields occurring inside the devices increase rapidly. Furthermore, strong gradients in the electric field are observed. These highly inhomogeneous field distributions give rise to distribution functions which deviate significantly from the frequently assumed Maxwellian distribution.

37.7.1 Ansatz-Based Approaches

Various improved macroscopic transport models have been developed based on analytical descriptions of the distribution function, e.g., [84]. Unfortunately, the model from Liotta and Struchtrup [85] and the model from Nekovee [86], which are both discussed below, require a large number of moments, because the chosen ansatz functions converge slowly.

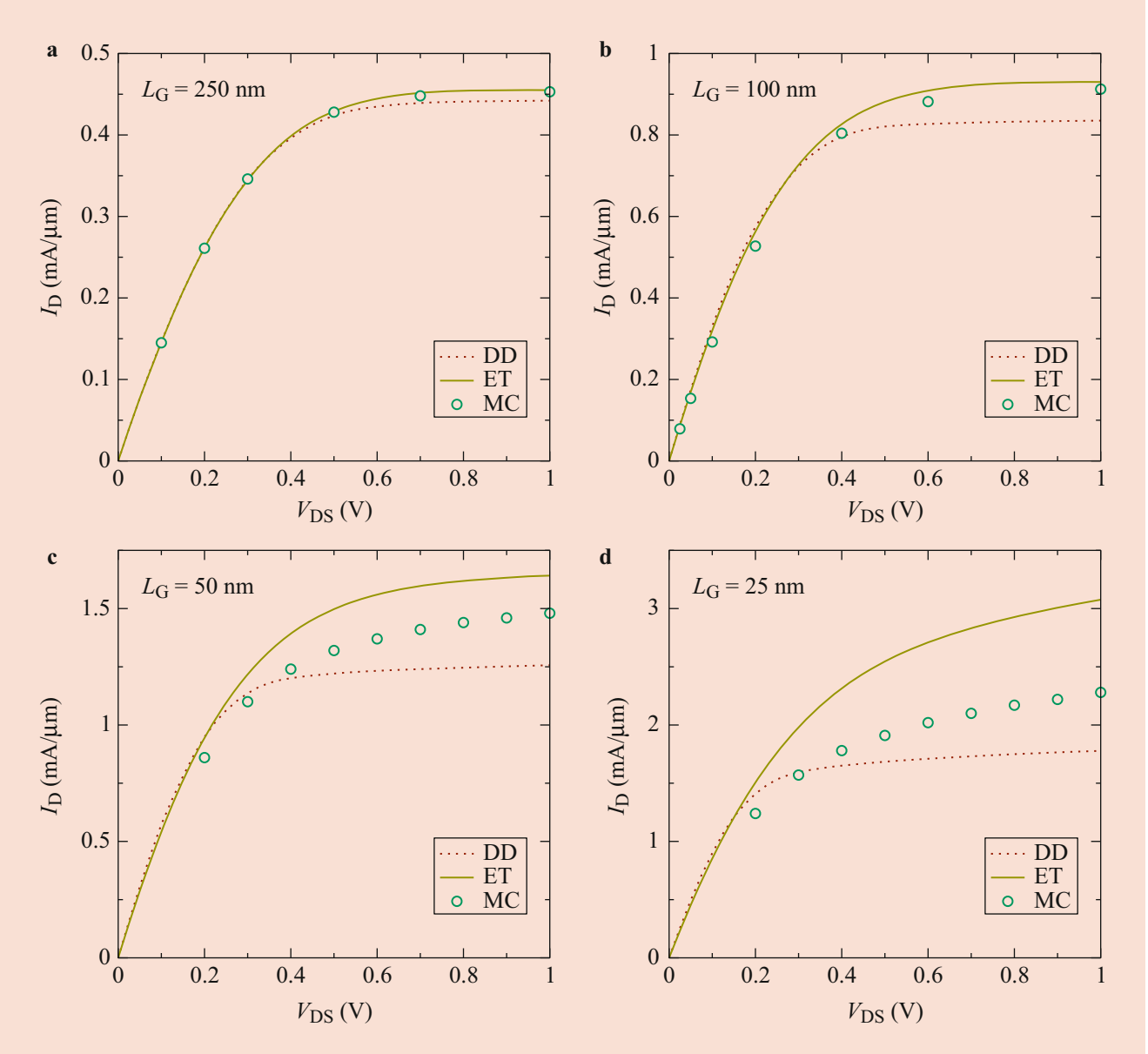

Fig. 37.14 Comparison of drain currents from the drift-diffusion and energy transport models with Monte Carlo simulation results for a doublegate MOSFET with a gate length of 250 nm (**a**), 100 nm (**b**), 50 nm (**c**), and 25 nm (**d**). The drift-diffusion model stays accurate down to a gate length of 250 nm. The energy transport model is accurate down to 100 nm

Liotta and Struchtrup [85] find that a hierarchy containing 12-moment equations is needed to reproduce simulation results obtained from an expansion in spherical harmonics. The proposed model uses an ansatz for the distribution function to calculate the closure relations which is less general than moment-based models with carefully derived closure relations.

A conclusion similar to Liotta and Struchtrup is drawn in [86] by Nekovee et al., who solve the Boltzmann equation using moment-based models. However, this "moment" model is based on an expression for the distribution function using a sum of Hermite polynomials multiplied by a Maxwellian shape. They find that the hierarchy of equations converges too slowly and the model fails to predict results for ballistic diodes. Instead of the moments, the parameters of the distribution function are considered in [86]. Hence, we feel that their conclusion is not applicable to moment-based models [10, 87].

Another approach [88–90] derives only the closure relations from an analytical distribution function model based on the maximum entropy principle. However, these models are difficult to handle numerically as they are hyperbolic.

An explicit ansatz for the distribution function can be avoided in the derivation of a higher-order moment-based

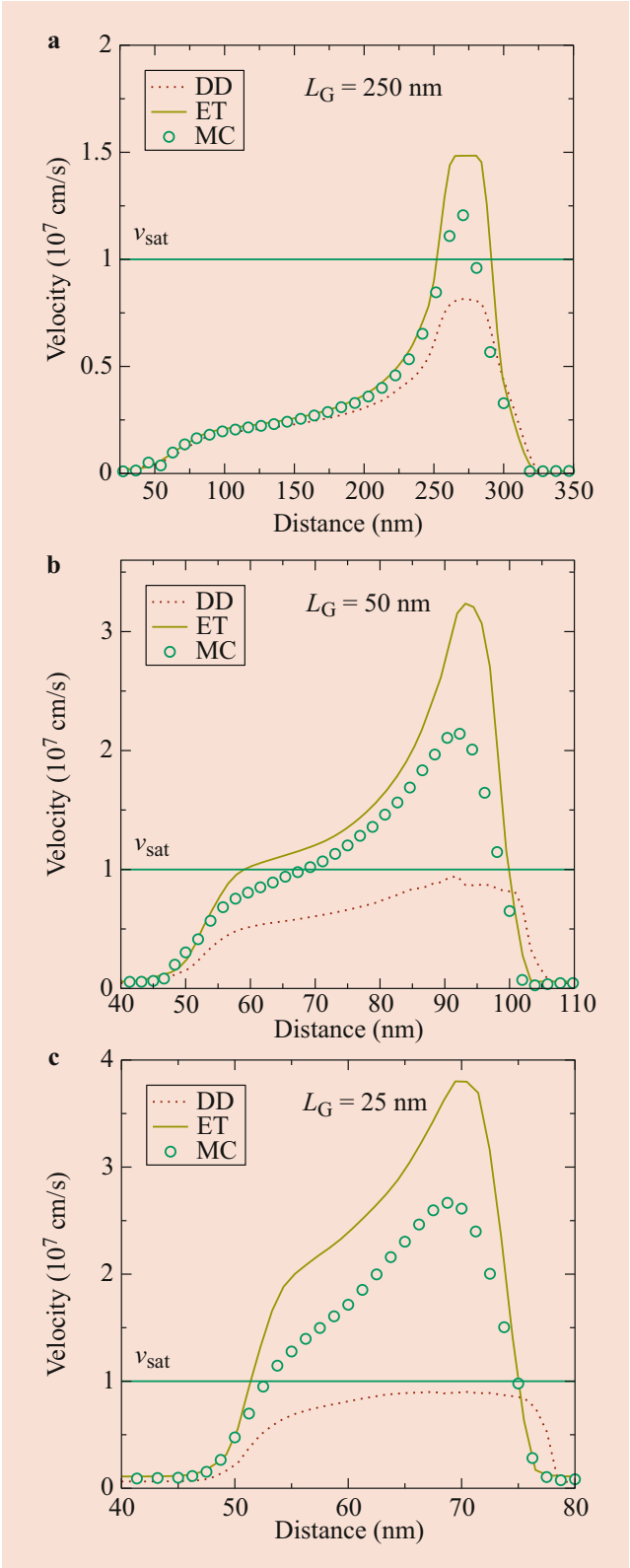

Fig. 37.15 Comparison of velocity profiles from a drift-diffusion and energy transport model with Monte Carlo simulation results for MOSFETs with varying gate lengths of 250 nm (**a**), 50 nm (**b**), and 25 nm (**c**). Down to 250 nm, the energy transport model matches the Monte Carlo simulation results quite well. At shorter gate lengths, the energy transport model overestimates the velocity

transport model. In particular, a macroscopic transport model has been proposed in [51] which considers the first six moments in the Boltzmann transport equation and closes the system using an empirical relation matched to Monte Carlo simulation results.

37.7.2 Higher-Order Moment Models

A natural extension of energy transport models which retains the basic structure of the equation system is to include higher-order moment equations. The only assumption made about the distribution function is the validity of the diffusion approximation in order to obtain a numerically tractable (parabolic) model [52]. Ignoring generation and recombination terms, the flux and balance equations of the six-moment model read for electrons:

$$\nabla \cdot \frac{\mathbf{J}}{q} = \partial_t n \tag{37.173}$$

$$\frac{\mathbf{J}}{q} = \frac{k_B}{q}\mu\left(\frac{\mathrm{q}}{k_B}\mathbf{E}\,n + \nabla(nT_n)\right) \tag{37.174}$$

$$\nabla \cdot \mathbf{S} = -\frac{3}{2}k_B\,\partial_t(nT_n) + \mathbf{E}\cdot\mathbf{J} - n\frac{3}{2}k_B\frac{T_n - T_L}{\tau_\varepsilon} \tag{37.175}$$

$$\mathbf{S} = -\frac{5}{2}\frac{k_B^2}{\mathrm{q}}\mu_S\left(\frac{\mathrm{q}}{k_B}\mathbf{E}\,n\,T_n + \nabla(n\,T_n^2\,\beta)\right) \tag{37.176}$$

$$\nabla \cdot \mathbf{K} = -\frac{15}{4}k_B^2\,\partial_t(n\,T_n^2\,\beta) - 2\,q\,\mathbf{E}\cdot\mathbf{S} - \frac{15}{4}k_B^2\,n\,\frac{T_n^2\,\beta - T_L^2}{\tau_\beta} \tag{37.177}$$

$$\mathbf{K} = -\frac{35}{4}\frac{k_B^3}{q}\mu_K\left(\frac{\mathrm{q}}{k_B}\mathbf{E}\,n\,T_n^2\,\beta + \nabla(n\,T_n^3\,\beta^3)\right) \tag{37.178}$$

The additional unknowns of the six-moment model are the kurtosis of the distribution function β and the kurtosis flux density $\mathbf{K}$, which are defined as

$$\beta = \frac{3}{5}\frac{\langle\mathcal{E}^2\rangle}{\langle\mathcal{E}\rangle^2} \quad \text{and} \quad \mathbf{K} = \langle\mathbf{v}\,\mathcal{E}^2\rangle. \tag{37.179}$$

This definition of the kurtosis is based on the diffusion approximation. The additional transport parameters are the kurtosis relaxation time τ_β and the kurtosis flux mobility μ_K. In terms of the kurtosis, the fourth-order moment is expressed as

$$\langle v^2 \boldsymbol{\mathcal{E}} \rangle = \frac{5{\cdot}3}{2} \frac{k_\mathrm{B}^2}{m} n T_\mathrm{n}^2 \beta. \tag{37.180}$$

In the six-moment model above, we have used an empirically found closure [51] for the sixth-order moment which depends on the third power of β:

$$\langle v^4 \boldsymbol{\mathcal{E}} \rangle = \frac{7 \cdot 5 \cdot 3}{2} \frac{k_\mathrm{B}^3}{m^2} n T_\mathrm{n}^3 \beta^3. \tag{37.181}$$

With this closure, the six-moment model is contained as a special case in the model hierarchy described by Jüngel in [13, p.187].

The first four equations are the same as for the energy transport model, except that the kurtosis β appears in the energy flux equation (37.176). As a consequence, the energy flux equation cannot be written in the form frequently used for energy transport models as proportional to the current density (cf. (37.156)) without producing additional terms. This modification makes the coupled equation system difficult to solve, and approximations have been used [51]. Note that the six-moment model reduces to a standard energy transport model when the equations containing $\mathbf{K}$ are dropped and a value of unity is assumed for β.

Discretization and numerical solution of the six-moment model are covered in [15]. A generalized Maxwellian closure for the sixth moment is proposed in [51], and a cumulant-based closure is discussed in [91, 92]. Correction terms for non-parabolicity are added to the six-moment model in [73, 74].

Properties of the Kurtosis

For a heated Maxwell distribution and parabolic bands, the kurtosis β_M is identical 1. Thus, a $\beta \neq 1$ quantifies the deviation from the heated Maxwellian shape. Note that a Maxwellian shape is never observed in Monte Carlo simulations, except for the contact regions where the carriers are still cold and the Pauli principle is neglected.

For the special case of a bulk semiconductor, the kurtosis can be expressed as a function of the carrier temperature. By considering the homogeneous six-moment model, the following expression is obtained [10]:

$$\beta_\mathrm{bulk}(T_\mathrm{n}) = \frac{T_\mathrm{L}^2}{T_\mathrm{n}^2} + 2 \frac{\tau_\beta}{\tau_\varepsilon} \frac{\mu_\mathrm{S}}{\mu_\mathrm{n}} \left(1 - \frac{T_\mathrm{L}}{T_\mathrm{n}}\right). \tag{37.182}$$

This is an analogy to the homogeneous energy transport equation used to estimate the carrier temperature from the electric field as discussed in Sect. 37.5.4. Since in inhomogeneous samples T_n already lags behind the field (for increasing $\mathbf{E}$), some nonlocality is also expected for beta, and an expression estimating β from T_n is preferable to one using $\mathbf{E}$. Figure 37.16a shows that the doping dependence

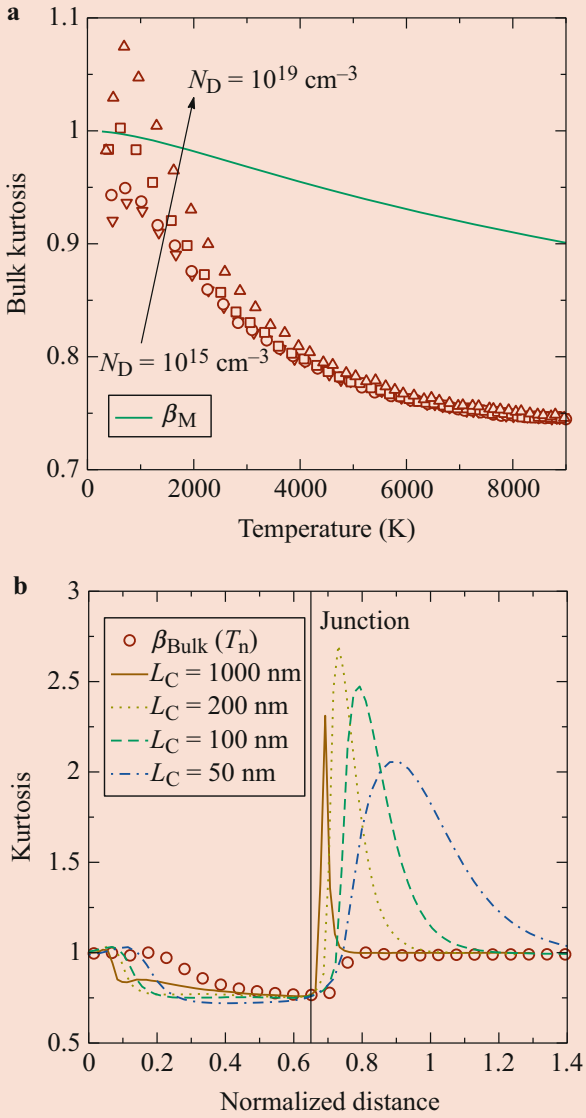

Fig. 37.16 The kurtosis for bulk (**a**) and for different n^+nn^+ test structures (**b**). Note the strong deviation from unity after the second junction

of the bulk kurtosis $\beta_\mathrm{bulk}(T_\mathrm{n})$ is only relevant at doping concentrations higher than 10^{16} cm^{-3} and for lower-carrier temperatures.

As shown in Fig. 37.16b, the kurtosis behaves quite differently in inhomogeneous samples than would be expected from the bulk relation $\beta_\mathrm{bulk}(T_\mathrm{n})$. While inside the channel β is typically below unity and reasonably close to the bulk relation, values larger than unity are observed at the end of the channel region. This deviation corresponds to the high-energy tail of the distribution function in Fig. 37.9. Typical values of the kurtosis β are in the range [0.75, 3] which indicates a strong deviation from a heated Maxwellian distribution.

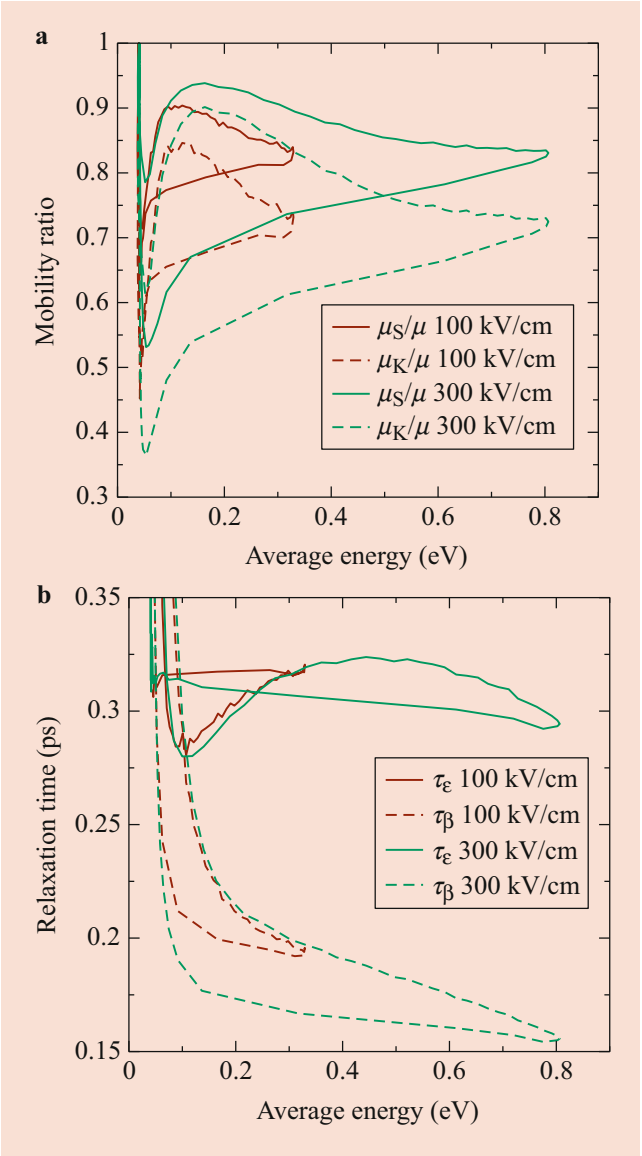

Fig. 37.17 (**a**) The ratio of the mobilities μ_S/μ and μ_K/μ for an n^+nn^+ test structure with $L_c = 200$ nm. (**b**) The energy and the kurtosis relaxation times $\tau_\mathcal{E}$ and τ_β

Modeling of the Transport Parameters

Modeling of the additional parameters μ_K and τ_β faces similar problems as discussed in Sect. 37.5.5. These parameters contain information on hot-carrier effects. Both parameters show a clear hysteresis when plotted over the average energy as shown in Fig. 37.17.

In the six-moment model, the interplay between the various parameters is highly complex and has a strong impact on the numerical stability of the whole transport model. Simple analytical models based on constant values as the ones used in [51] do not always deliver satisfactory results.

For an appropriate description of higher-order transport models, it is therefore important to model the transport parameters with as few simplifying assumptions as possible. To minimize uncertainties arising from this issue, all physical parameters might be extracted as a function of the doping concentration and the average energy from homogeneous Monte Carlo simulations. This is discussed below.

37.7.3 Table-Based Parameter Modeling

Modeling transport parameters like the mobilities μ, μ_S, and μ_K and the relaxation times $\tau_\mathcal{E}$ and τ_β is challenging, since they all depend on the actual shape of the distribution function, on the scattering rates, as well as on the band structure [74]. Having many adjustable parameters is an inconvenience inherent in many higher-order transport models based on analytical models for the mobilities and relaxation times [10]. In particular, a consistent comparison with Monte Carlo simulations is difficult, when the resulting transport models do not reproduce the Monte Carlo simulation results in the homogeneous case. For a meaningful comparison, the models should be consistent at least in the bulk case, which already is far from trivial.

In [93], a transport parameter model based on homogeneous fullband Monte Carlo tables has been introduced. By adjusting this method for the six-moment model, all higher-order transport parameters are extracted from bulk Monte Carlo simulations for different doping concentrations and for different driving forces. In the macroscopic models, the transport parameters are then considered as a function of doping and the average energy [73, 94]. In this way, the fullband structure of the material and scattering mechanisms such as phonon-induced scattering are inherently included in the model. Correction factors for non-parabolic band structures have also been obtained [74].

Since all model parameters are obtained from bulk Monte Carlo simulations, the transport models are free of fit parameters which leaves us with "no knobs to turn" [95]. Macroscopic models based on Monte Carlo simulation data improve on their counterpart models based on analytical models significantly, both in terms of numerical stability and in the agreement with Monte Carlo device simulations [74].

In Fig. 37.18, the extracted bulk mobility parameter set for higher-order macroscopic transport models is displayed. Here the carrier mobility μ (Fig. 37.18a) and higher-order mobilities μ_S (Fig. 37.18b) and μ_K (Fig. 37.18c) as a function of the electric field E_{abs} for different doping concentrations N_d are presented. As can be observed for each type of mobility, the values of the mobility are independent of the doping concentration for fields above 100 kV/cm, which is where $v = v_{sat}$ and $\mu = v_{sat}/E$. For low fields, the mobilities are much larger at low doping concentrations compared to high doping concentrations.

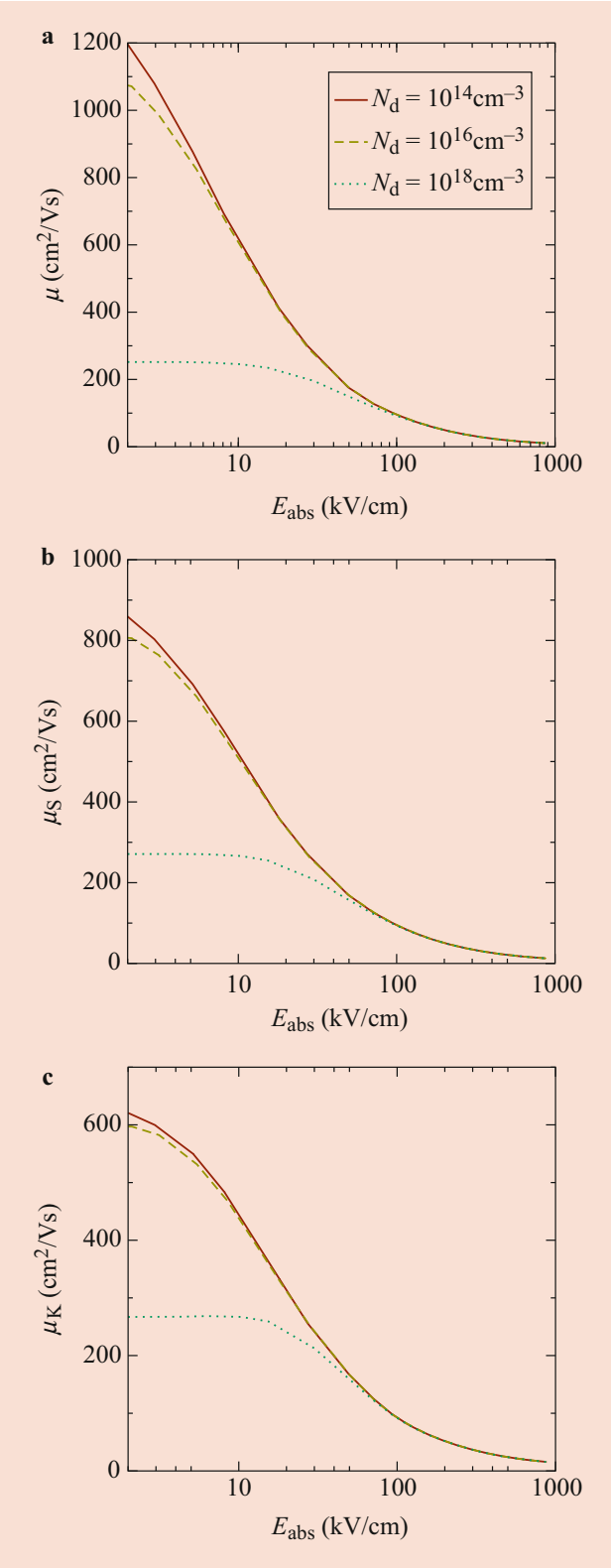

Fig. 37.18 Carrier mobility μ, (**a**) energy flux mobility μ_S, and (**b**) second-order energy flux mobility μ_K versus driving field for different doping concentrations. For fields higher than (**c**) 100 kV/cm, the mobilities are independent of the doping concentration. For low fields, the values of the mobilities are much larger at low doping than at high doping concentrations

The value of all three types of mobilities is comparable at high doping concentrations. For low doping concentrations and low fields, the energy flux mobility and the second-order flux mobility are smaller than the carrier mobility.

Figure 37.19 presents the relaxation times τ_ε and τ_β for different doping concentrations as a function of the kinetic energy of the carriers. As can be seen, for high energies, the relaxation times become doping-independent.

For a fixed energy, the Monte Carlo simulations predict lower relaxation times with higher N_d. In a certain field regime, where optical phonons can be neglected, the energy relaxation time τ_ε is approximately constant. However, for driving fields above 450 kV/cm, the energy relaxation time is no longer constant but decreases due to the increase of optical phonon scattering, which is an inelastic process.

The carrier velocity as a function of the lateral field and for different N_d is shown in Fig. 37.20. The saturation velocity of Si is reached at a driving field of 150 kV/cm.

In Fig. 37.21, the bulk carrier temperature as a function of the electric field calculated with the bulk fullband Monte Carlo method is presented. The quadratic dependence of the carrier temperature on the electric field (37.150) is a good approximation for fields lower than 200 kV/cm, while for fields up to 450 kV/cm a linear approximation

$$T_n = T_L + \tau_{const} \frac{2}{3} \frac{q}{k_B} v_{sat} E \,. \tag{37.183}$$

can be used assuming $\mu = v_{sat}/E$. However, for driving fields above 450 kV/cm, the linear approximation breaks down due to optical phonon scattering.

37.8 Applications

This section discusses applications of the six-moment model in the deca-nanometer regime. The channel length range of deca-nanometer devices is here defined approximately from 100 nm down to 20 nm.

In order to consider the high-field case as accurately as possible, a transport model based on fullband Monte Carlo tables is considered. The results of the Monte Carlo table-based higher-order transport models are benchmarked for n^+nn^+ test structures and double-gate MOSFETs against Monte Carlo simulations. Occasionally, the spherical harmonic expansion simulator is used as a reference, because the results are very close to those obtained by the Monte Carlo method, but the computational effort is considerably lower, particularly for rare events which determine, for example, the high-energy tail of the energy distribution function.

When the channel length is reduced to increase the operation speed and the number of components per chip, the so-called short-channel effects arise [96]. An adequate de-

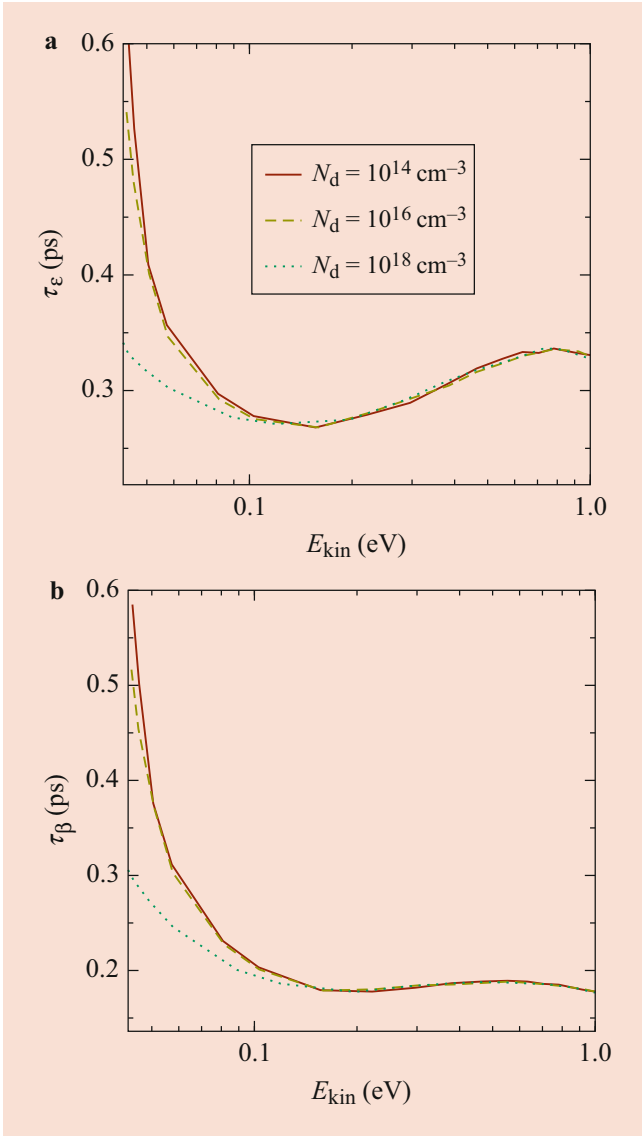

Fig. 37.19 Energy relaxation time $\tau_\mathcal{E}$ (**a**) and second-order energy relaxation time τ_β (**b**) extracted from bulk Monte Carlo simulations as a function of the kinetic energy for different bulk dopings. For very high energies, the relaxation times decrease due to the increase of optical phonon scattering

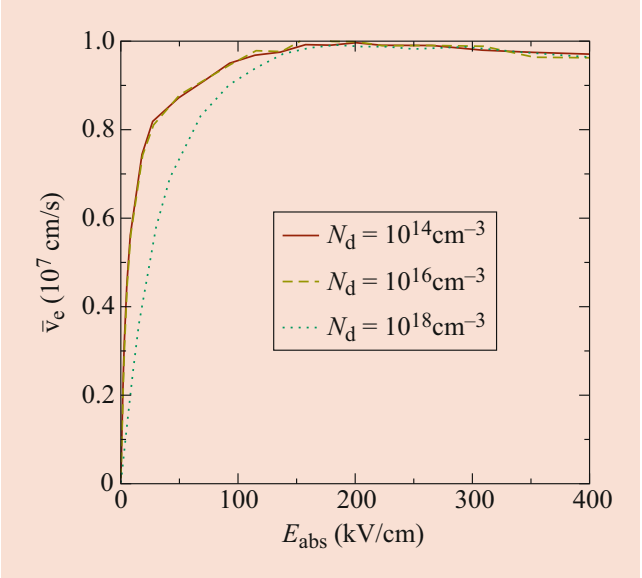

Fig. 37.20 Bulk velocity of electrons as a function of the driving field E_{abs} for a doping of 10^{14} cm^{-3}, 10^{16} cm^{-3}, and 10^{18} cm^{-3}. In the low-field regime, the electron velocity for high dopings is lower than the velocity of the low dopings, while the value of the velocity converges for high fields

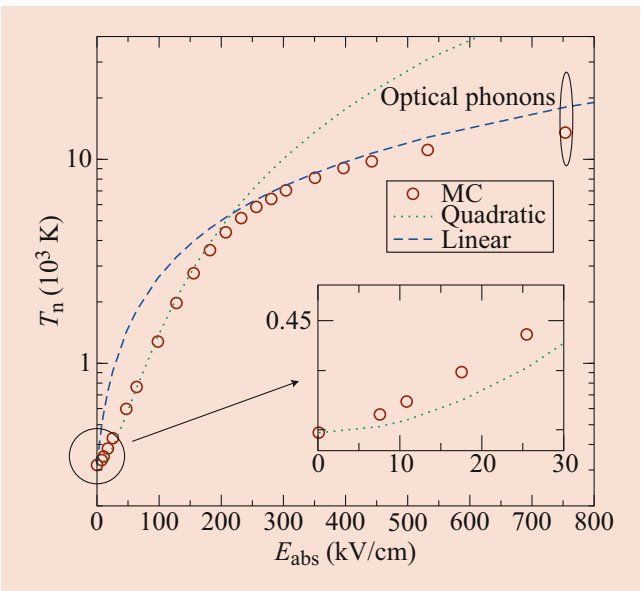

Fig. 37.21 Carrier temperature T_n as a function of the driving field in a homogeneous bulk simulation carried out with the fullband Monte Carlo method. For lower fields, the carrier temperature is a function of E^2, while for high fields, the temperature is closer to a linear dependence on the driving field

scription of these phenomena relies on a detailed description of the distribution function which is provided by the six-moment model [11, 74]. A variety of short-channel effects such as the velocity overshoot, the impact ionization, and the influence of hot electrons on the carrier distribution function are investigated.

37.8.1 n^+nn^+ Test Structures

We first investigate the validity of higher-order transport models on a series of the most popular test devices, one-dimensional n^+nn^+ structures. Due to the simplified one-dimensional structure and the requirement of only one carrier type, the influence of the various parameters on basic quantities like the velocity or the carrier temperature can be more easily separated and interpreted. However, as can be seen

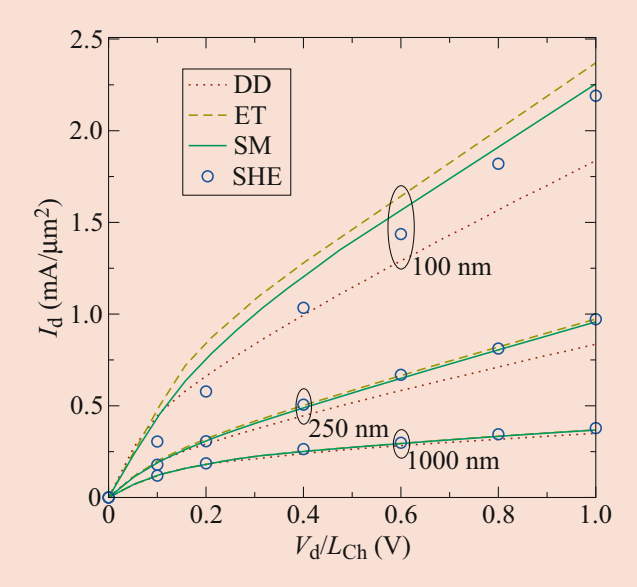

Fig. 37.22 Output currents for different n^+nn^+ structures calculated with DD, ET, and SM models. As a reference, spherical harmonic expansion simulations are used. For 1000 nm, all models predict the same current, while the DD model underestimates the current for a channel length of 100 nm

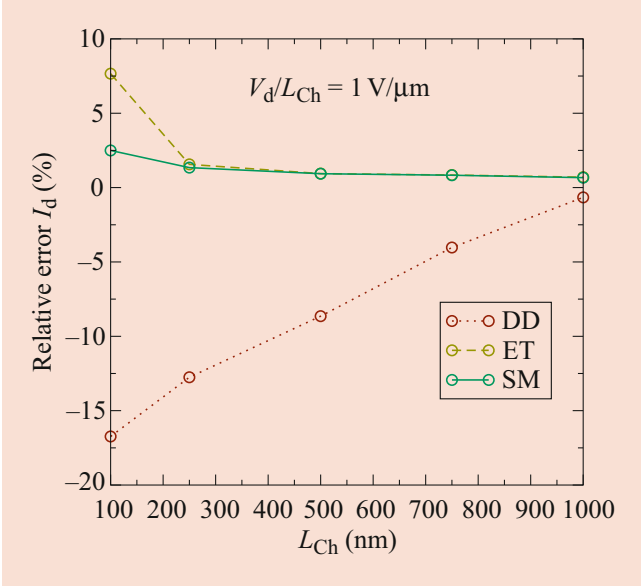

Fig. 37.23 Relative error of the current calculated with the DD, ET, and the SM model as a function of the channel length L_{Ch}. A voltage of 1 mV/nm × L_{Ch} has been applied. While the relative error in the ET and the SM model is always below 7.5%, the relative error in the DD model approaches 16% at a channel length of 100 nm

from the examples below, even for these simple structures, such an interpretation is far from trivial.

Model Check

As discussed in the previous sections, macroscopic transport models are based on many empirical assumptions. Hardly any of these can be justified theoretically below a channel-length of one micrometer. Hence, we choose 1000 nm as the calibration point, where all macroscopic transport models together with the spherical harmonic approach, which is the reference simulator here, should yield the same result.

Figure 37.22 shows the output currents of different n^+nn^+ structures for channel lengths of 100 nm, 250 nm, and 1000 nm calculated with the DD, ET, SM, and the spherical harmonic expansion model. For a channel length of 1000 nm, all models yield the same results with an error below 1% as can be observed in Fig. 37.23. While the error of the ET and SM model stays more or less constant below 2.5% for a channel length down to 250 nm, the error of the DD model continuously increases and reaches a value of −16% for a channel length of 100 nm. Therefore, simulating short-channel devices with the DD model gives only poor results. While the inaccuracy of the ET model starts to increase below 250 nm, the SM model still gives results very close to spherical harmonic expansion simulations.

Velocity Profile

In Fig. 37.24, the evolution of the velocity profile within several n^+nn^+ structures calculated with the DD, ET, SM, and the spherical harmonic expansion model as a reference is shown. The bias conditions were chosen in such a way to result in an electric field of 50 kV/cm in the middle of the intrinsic region (loosely referred to as channel region in the following) for each channel length. Overall, the SM model predicts a velocity profile closer to the spherical harmonic expansion data than the DD and the ET model. From this, we conclude that the closure relation of the SM model is improved compared to the ET model.

For long-channel devices, all models yield a similar velocity profile. For decreasing channel length below L_{Ch} = 250 nm, the spurious velocity overshoot in the ET model and the reduced one in the six-moment model are clearly visible. On the other hand, the DD model does not predict any velocity overshoot at all and stays always below the bulk saturation velocity v_{sat}.

In order to explain this effect, various theories have been put forward. Some authors have argued that there is a relation with non-parabolicity effects [97], whereas other theories relate it to the hysteresis in the mobility [98].

However, it was demonstrated in [99] that the SVO is caused by deficient models for the closure relation and the transport parameters. For higher-order transport models, the error in the SVO decreases. This can also be seen in Fig. 37.24 where the six-moment model is consistently better than the energy transport model.

Drain Current

The improved accuracy in the device characteristics obtained from higher-order moments is also reflected in the currents, which is demonstrated in Fig. 37.25. Here, the output characteristics of a 40 nm and 80 nm channel length n^+nn^+ structure calculated with the DD, ET, SM, and the reference spherical harmonic expansion model are shown.

While the relative error of the current calculated with the SM and the ET model stays small in long-channel devices (see Fig. 37.23), there is a significant deviation for short-channel devices as shown in Fig. 37.26. In the short-channel range, from 40 to 100 nm, the current calculated with the SM model is below an error of 10%. In contrast, at a channel length of 40 nm, the errors of the DD and the ET model are at −30% and 40%, respectively.

As has been pointed out, the ET model accurately describes current transport down to a channel length of about 80 nm, but a strong increase in the error of the current can be observed below 80 nm. Therefore, the ET model is a suitable transport model for devices down to 80 nm channel lengths

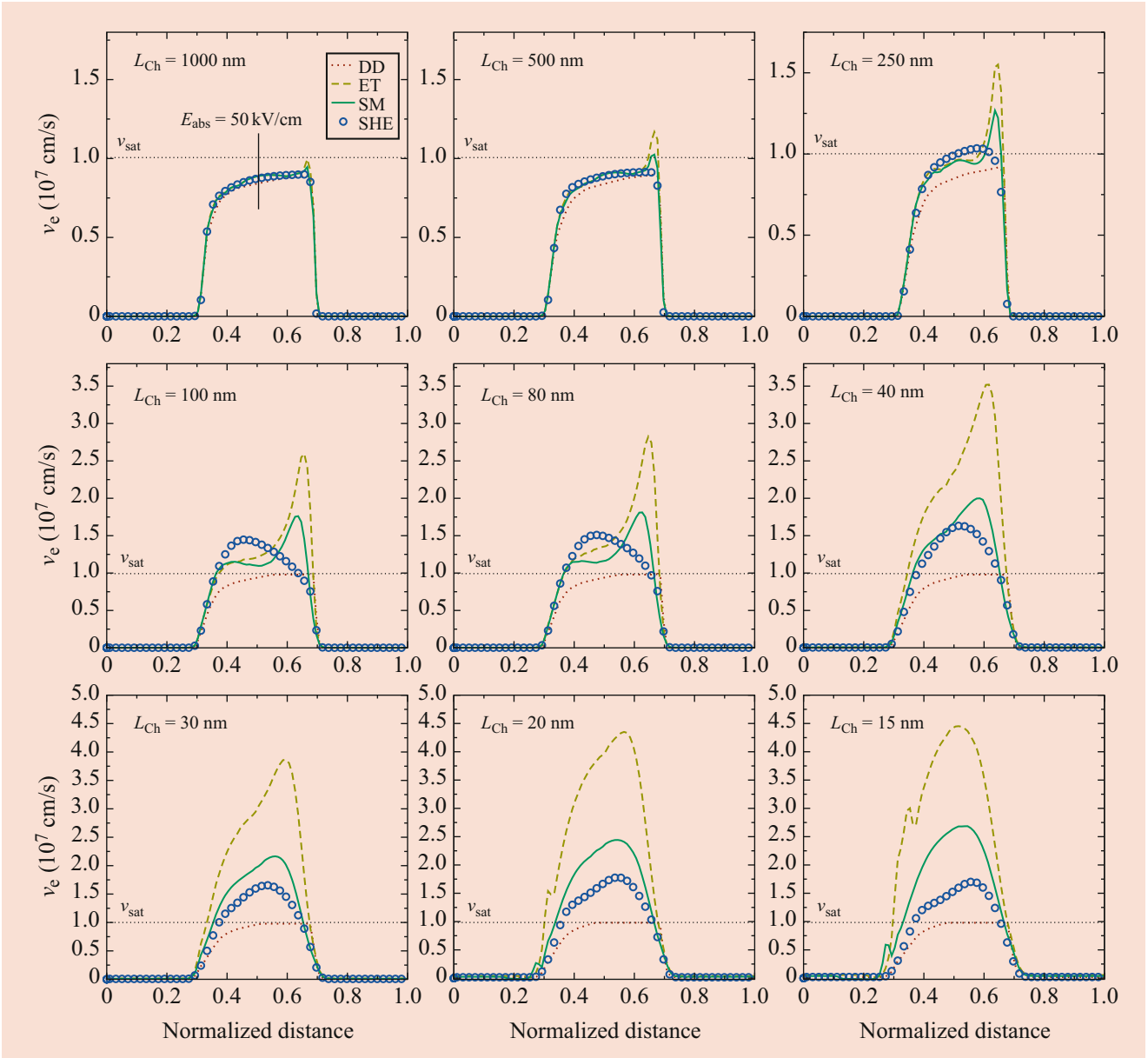

Fig. 37.24 Evolution of the carrier velocity profiles for decreasing channel lengths calculated with the DD, the ET, and the SM model. The velocities are compared to the results obtained from spherical harmonic expansion simulations. While the maximum velocity of the DD model is the saturation velocity v_{sat}, the spurious velocity overshoot at the end of the channel in the ET and the SM model is clearly visible. The velocity overshoot at the beginning of the channel can be quantitatively identified for devices smaller than 100 nm in the ET and the SM model

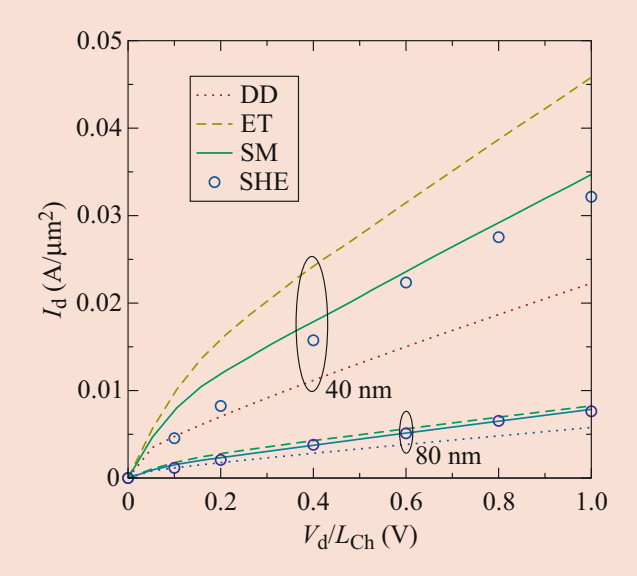

Fig. 37.25 Output currents of an 80 nm and a 40 nm channel length n^+nn^+ structure calculated with the DD, ET, SM, and spherical harmonic expansion model. The ET model overestimates the current at 40 nm, while the SM model yields the most accurate result

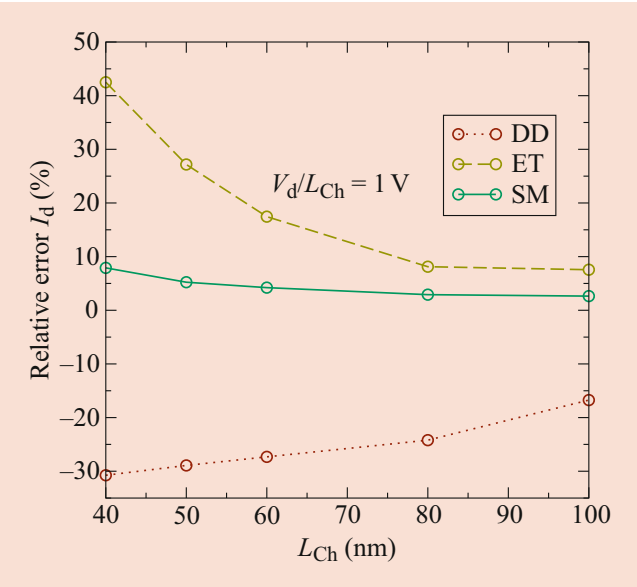

Fig. 37.26 Relative error in the current of the DD, the ET, and the SM model for an n^+nn^+ structure in the channel range from 100 nm down to 40 nm. At 40 nm the relative error of the SM model is below 6%, while the error of the DD and the ET model is at −30% and 40% respectively

only. For a channel length below 80 nm, the SM model appears to be the model of choice. One additional strength of the six-moment model is that it gives more information about the distribution function than the ET model.

37.8.2 A Double-Gate MOSFET

Previously, the transport models have been validated with n^+nn^+ structures. Although it has been frequently claimed that n^+nn^+ structures emulate the behavior of MOS transistors, the most important devices in silicon technology, this is only partly true.

Drain Current

In Fig. 37.27, we compare results from drift-diffusion, energy transport and six-moment model with Monte Carlo simulation results for double-gate MOSFETs. All models use consistent bulk parameters. For long-channel devices down to a gate length of 250 nm (Fig. 37.28a) all of the models yield consistent results for the drain current.

However, the DD model consistently underestimates the current, particularly in the saturation regime. The ET model starts to deviate from the Monte Carlo simulation data at 100 nm (Fig. 37.28b), while the SM model properly reflects the output characteristic down to 50 nm (Fig. 37.28c). For gate lengths below 50 nm, all macroscopic models fail to describe the reference current.

Velocity

For a detailed analysis, we make a comparison of distributed quantities. Among several quantities, we find that velocity profiles are the most critical. Getting the right velocity profiles is important for correct terminal currents. Velocity profiles are depicted in Fig. 37.28. As above, for 250 nm, all models give reasonable results (Fig. 37.28a). At 50 nm and below (Fig. 37.28b-c), the ET models overestimate the velocity. The results of the SM model stay closest to Monte Carlo simulations but is also off at 25 nm.

The energy transport models tend to overestimate the velocity overshoot and introduce a spurious velocity overshoot at the end of the channel region of n^+nn^+ structures. For MOS transistors, on the other hand, the SVO coincides with the velocity overshoot at the end of the channel and is therefore not explicitly visible.

Predictiveness

To compare the predictiveness of macroscopic models, we plot drain current and transit frequency as a function of the gate length in Fig. 37.29. In both figures, the error of the DD model is much higher. The six-moment model and the energy transport model show similar behavior. But the six-moment model is closer to the Monte Carlo simulation results as it utilizes more information about the distribution function.

Despite the apparent limitations, it is possible to use drift-diffusion transport models also for deca-nanometer devices [100, 101]. These drift-diffusion models use mobility models and saturation velocities which are inconsistent with bulk data [102] and can provide short-term fixes to available

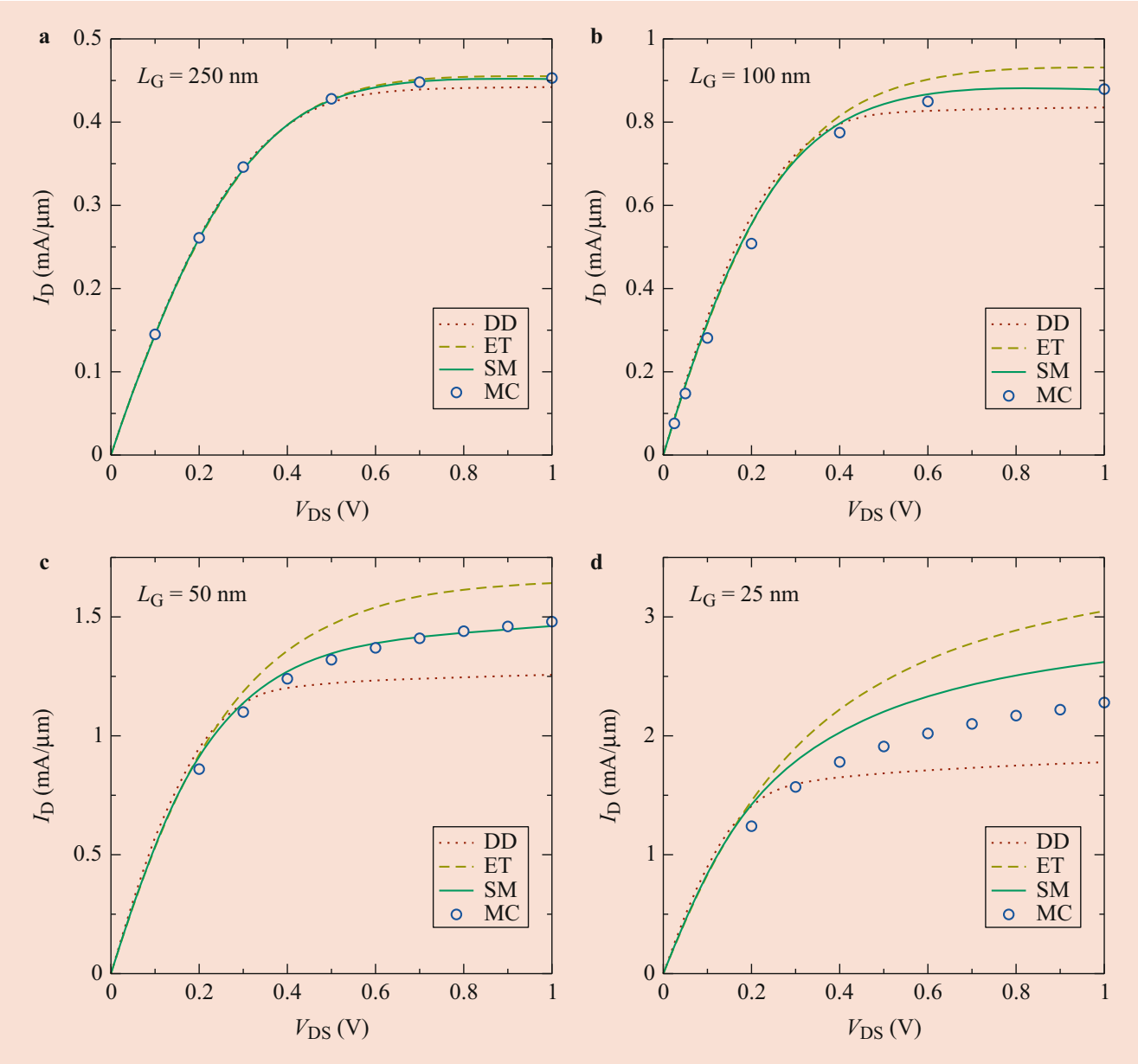

Fig. 37.27 Comparison of drain currents from the drift-diffusion, energy transport, and six-moment models with Monte Carlo simulation data for a double-gate MOSFET with varying gate lengths of 250 nm (**a**), 100 nm (**b**), 50 nm (**c**), and 25 nm (**d**). The six-moment model stays accurate down to a gate length of about 50 nm

models. This, obviously, is a fitting approach and has limited value for predictive simulations.

As a side note, we would like to mention that with shrinking device geometries quantum effects gain more importance and limit the validity of the BTE itself [103]. When the device dimensions are comparable to the carrier wave length, the carriers can no longer be treated as classical pointlike particles, and effects originating from the quantum mechanical nature of propagation begin to determine transport [104].

Numerical Properties

From a practical point of view, it has to be pointed out that convergence problems are an issue and inhibit the use of higher-order moment equations in everyday engineering applications. Unfortunately, simulation codes based on higher-order moment equations have never reached a robustness comparable to the drift-diffusion model. Several discretization schemes have been proposed [45], but no generally accepted discretization like the Scharfetter-Gummel scheme [7] for the drift-diffusion equations exists.

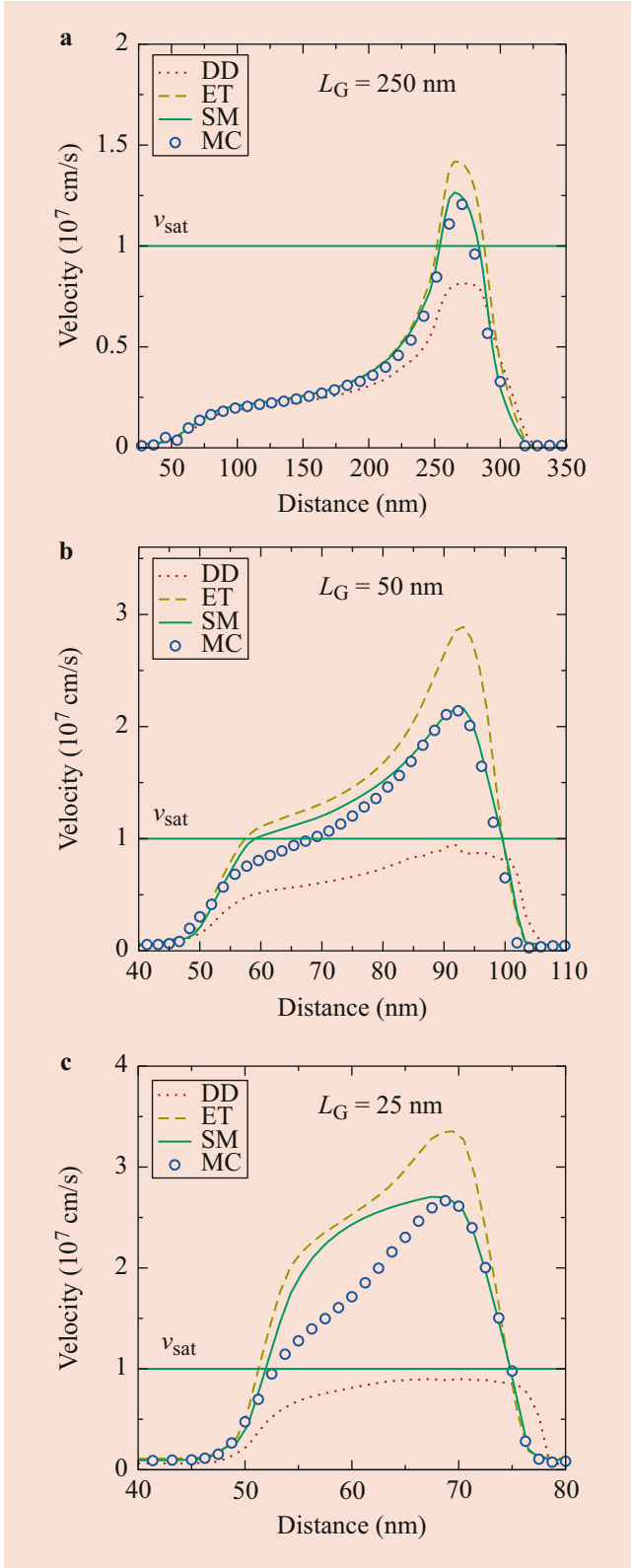

Fig. 37.28 Comparison of the velocity from the drift-diffusion, energy transport, and six-moment model with Monte Carlo simulation data for a double-gate MOSFET with gate length of 250 nm (**a**), 50 nm (**b**), and 25 nm (**c**). The spurious velocity overshoot is much less pronounced than for n^+nn^+ structures. The six-moment model stays closest to the Monte Carlo simulation results

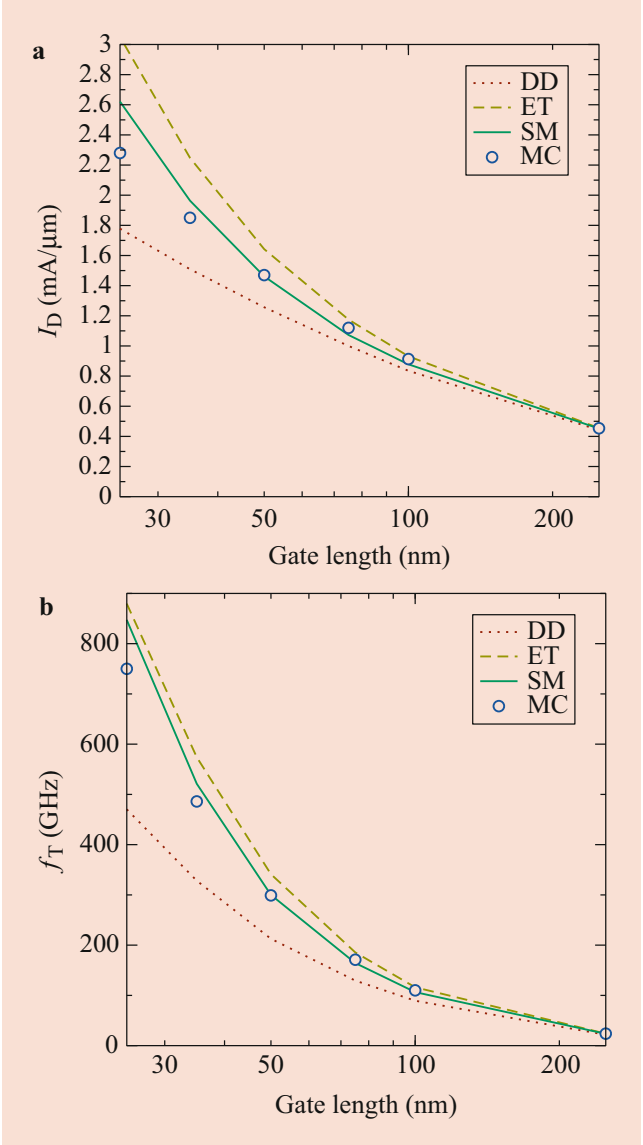

Fig. 37.29 Comparison of drain currents (**a**) and transit frequency (**b**) as a function of the gate length from the drift-diffusion, energy transport, and six-moment model with Monte Carlo simulation data for a double-gate MOSFET. The six-moment model is predictive down to 50 nm

37.8.3 Modeling of Hot-Carrier Effects

Hot carriers can lead to a number of interesting phenomena and are difficult to model in the drift-diffusion model, because too little information about the distribution function is available.

Within DD and ET, it is difficult to estimate the deviation of the energy distribution function from the Maxwellian shape. By contrast, the SM model provides the kurtosis, which has been shown to be crucial in that respect.

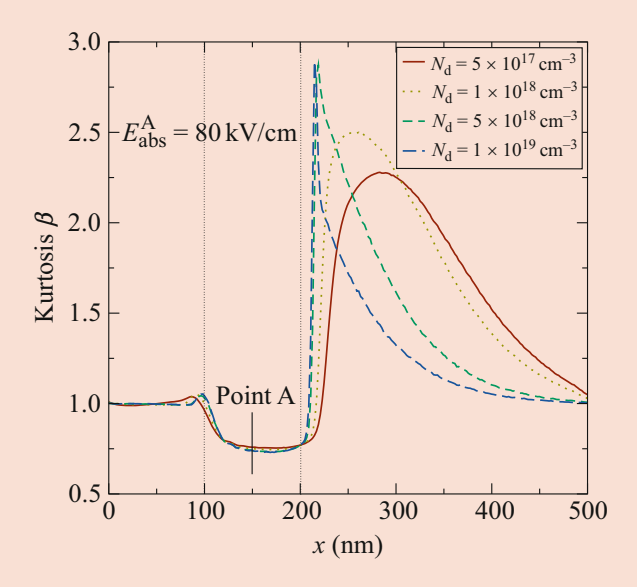

Fig. 37.30 Kurtosis calculated for different source and drain doping concentrations in an n^+nn^+ structure with a channel length of 100 nm. With increase in the doping concentrations, the peak of the kurtosis moves closer to the channel, as the cold carriers in the highly doped region strongly suppress the high-energy tail

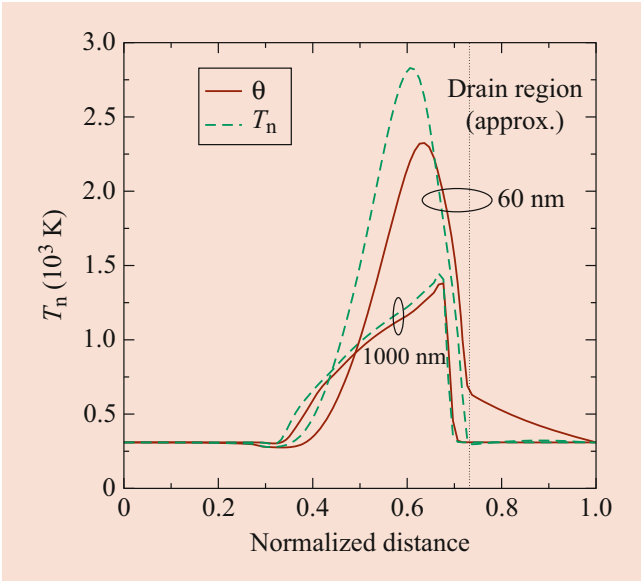

Fig. 37.31 Carrier temperature T_n together with the second-order temperature Θ for a 1000 nm and a 60 nm device. A bias leading to a maximum field of 50 kV/cm has been applied. While in the long-channel device a Maxwellian can be used, the high-energy tail in the short-channel device in the drain region increases

Kurtosis

As will be shown below, the kurtosis provides information to distinguish the channel region from the drain region [87]. The kurtosis of an n^+nn^+ structure with 100 nm channel length and a total length of 500 nm is visualized in Fig. 37.30 for different source and drain dopings. A constant channel doping of 10^{16} cm^{-3} is considered. As can be observed, for low doping, the maximum peak of the kurtosis is at 300 nm. For high doping, the maximum is at about 220 nm.

This can be explained as follows: Due to the higher concentration of cold electrons in the highly doped drain region, the relaxation of hot carriers is faster than in the low doped drain region. Hence, the maximum peak of β for the high doping concentration case is 25% higher than for low doping concentrations.

In Fig. 37.31, the second-order temperature Θ defined as

$$\Theta = \beta T_n \tag{37.184}$$

and the carrier temperature T_n are presented for a short- and a long-channel device. For the long-channel device, the hot distribution part can be neglected due to the small deviation of the second-order temperature Θ from T_n. Note that for cold carriers, where the energy distribution function follows a Maxwellian distribution for which $\beta = 1$, we also have $\Theta = T_n$.

Large field gradients strongly influence the kurtosis as shown in Fig. 37.32. Here, the kurtosis for fields of 5 kV/cm, 20 kV/cm, and 50 kV/cm for a 100 nm channel length structure is shown in the upper part of Fig. 37.32. The electric field has been calculated in the middle of the channel at Point A. As can be seen for a low field of 5 kV/cm, where the carrier temperature is low (see the lower part), a heated Maxwellian ($\beta_M = 1$) can be used, while for 20 kV/cm, an increase of the kurtosis at the beginning of the drain region is apparent. An overall significant increase of the kurtosis can be observed for high fields. As shown in the upper part of Fig. 37.32, the kurtosis starts to rise when the maximum of the carrier temperature decreases to the equilibrium value. This is the region where the hot electrons from the channel meet the large pool of cold electrons in the drain region, which quickly thermalizes the energy distribution function.

Velocity Overshoot

Within this work, the velocity overshoot has already been shown for n^+nn^+ test structures in Fig. 37.24 and for double-gate MOSFETs in Fig. 37.28. For a complete discussion, the velocity is given in Fig. 37.33 for the same type of structure which has been simulated in the previous figures. The ET transport model yields the same velocity profile in the low-field regime as the SM model, which is an indication that a Maxwellian is a good approximation at low fields. However, for high fields, the ET model overestimates the velocity profile of the DD and the SM model and exhibits a maximum at the end of the channel.

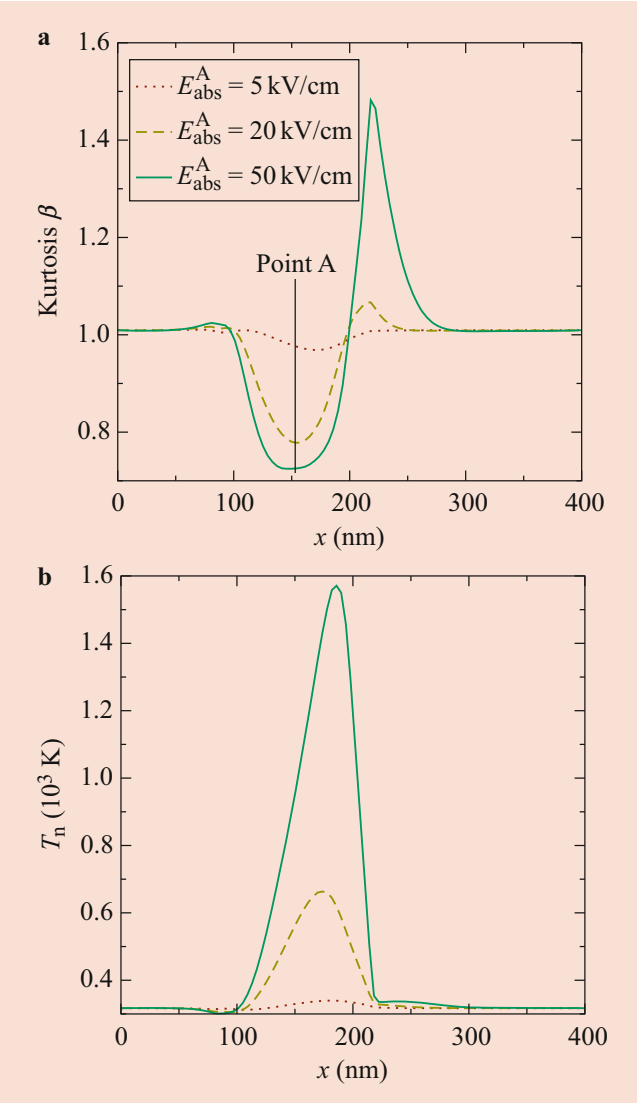

Fig. 37.32 Kurtosis β (**a**) and the carrier temperature (**b**) for electric fields of 5 kV/cm, 20 kV/cm, and 50 kV/cm through a 100 nm channel n^+nn^+ device (the value of the fields is calculated at Point A from Fig. 37.30). For high fields, the kurtosis increases at the beginning of the drain region, which means that the high-energy tail of the distribution function becomes very important. In the lower part of the figure, the carrier temperature profile for different electric fields is shown. The kurtosis exceeds unity in the region, where the carrier temperature drops down

Impact Ionization

Impact ionization due to high lateral fields occurs particularly in n-channel MOSFETs, because of the higher velocity of electrons compared to holes. The electrons in the conduction band collide with electrons in the valence band and generate electron-hole pairs. Hence, the probability of impact ionization for electrons in a strong field is determined by the probability that the electrons will acquire the ionization energy of the atoms from the field [105].

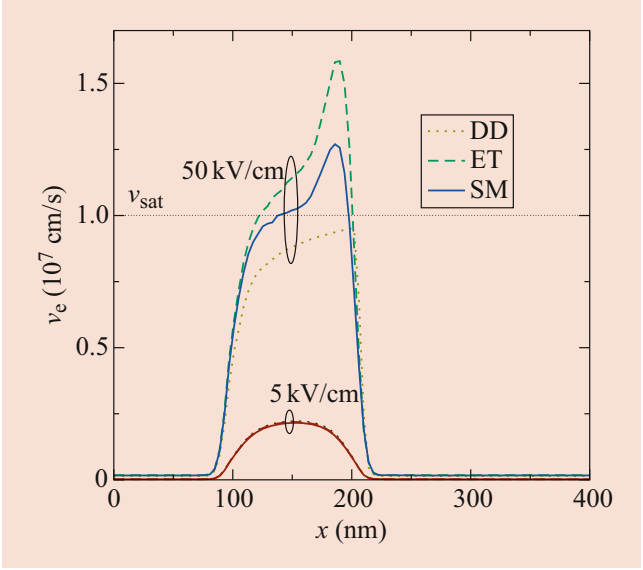

Fig. 37.33 The velocity profile for fields of 5 kV/cm and 50 kV/cm is shown for a MOSFET. For low fields, all models yield the same velocity profiles, which is an indication that the heated Maxwellian can be used. For high fields, a significant deviation of the velocity profiles can be observed

Figure 37.34 shows impact ionization rates of a 200 nm (Fig. 37.34a) and a 50 nm (Fig. 37.34b) channel device calculated with the DD, ET, and SM model and the Monte Carlo method. As can be observed, the impact ionization rate predicted by the SM model is closer to Monte Carlo simulation data than the ET and the DD model due to the better modeling of the distribution function in the SM model [106, 107].

Hot-Carrier Gate Currents

In the channel region of a MOSFET, the energy distribution deviates from the ideal shape implied by a heated Maxwellian. The carrier energy distribution influences tunneling processes which is important for modeling of gate leakage currents in turned-on devices. If a heated Maxwellian approximation is used for the description of hot-carrier tunneling, the gate current density is heavily overestimated. This effect is found to be especially pronounced for devices with short gate lengths. Some non-Maxwellian models are reviewed in [108], and it is found that a model which is based on the solution variables of a six-moment transport model accurately reproduces the Monte Carlo simulation results.

Hot-Carrier Degradation

Hot-carrier degradation is a major device reliability issue, particularly for MOSFETs. The degradation is commonly assumed to be driven by the generation of traps at or near the Si/SiO_2 interface.

Charge carriers in the channel can gain high kinetic energy and trigger the creation of defects at the Si/SiO_2 interface

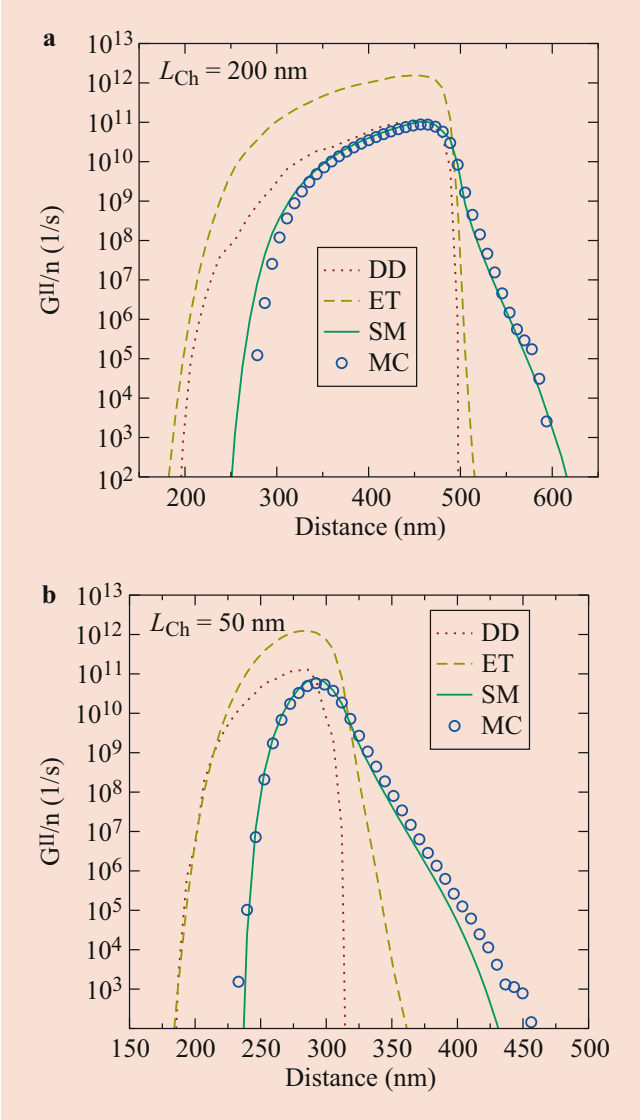

Fig. 37.34 The impact ionization rate calculated with Monte Carlo, the DD, ET, and the SM model for a 200 nm (**a**) and a 50 nm structure (**b**). Due to the better modeling of the distribution function in the SM model, the results are closer to the Monte Carlo simulation data than those of the DD and the ET model

[109, 110]. The driving force of this process is the energy deposited by charge carriers. For a proper physics-based description of this complex phenomenon, one again requires a detailed knowledge about the carrier transport in the targeted devices [111–116].

37.9 Summary and Conclusion

Macroscopic models for current transport in semiconductors can be formulated by following two approaches: phenomenologically, where the semiconductor equations are based on the laws of mass and energy conservation as well as the principles of irreversible thermodynamics, or systematically, where a set of equations is derived starting from the Boltzmann transport equation.

Transport models can be derived from the semiclassical Boltzmann equation using various methods. The method of moments can be considered the most general one as it does not require an explicit ansatz for the distribution function. Within the method of moments, the Boltzmann transport equation is multiplied with a polynomial weight function, and the whole equation is integrated over *k*-space. Each equation contains information about the next higher-order moment which yields an infinite number of coupled equations. To obtain a tractable equation set, this hierarchy has to be truncated at a certain order. The next higher-order moment has to be modeled as a function of the available lower-order moments which is referred to as the closure of the equation system.

When only the first two moments are considered, the drift-diffusion model is obtained, which is still predominantly used in engineering applications due to its simplicity and numerical stability. As the drift-diffusion model cannot capture nonlocal effects, which become increasingly important for miniaturized devices, its use becomes questionable. Therefore, higher-order equations have to be considered.

Inclusion of the first three or four moments of Boltzmann's equation results in hydrodynamic models which are, however, numerically too complicated to solve for everyday's use due to their hyperbolic nature. Within the framework of the diffusion approximation, the convective terms in the hydrodynamic models can be neglected, resulting in much simpler parabolic energy transport models, which are offered by the leading commercial device simulators in addition to the traditional drift-diffusion model.

A detailed study reveals some common problems observed in macroscopic transport models using only the first three or four moments. Most importantly, the energy distribution function is frequently modeled by a heated Maxwellian distribution. This distribution function model is then used to derive a closure relation. However, Monte Carlo simulations show that the energy distribution function is only poorly described by a heated Maxwellian distribution function, both for bulk and inhomogeneous devices. Another important issue is the modeling of the relaxation times and mobilities. Both quantities show a pronounced hysteresis when plotted over the average energy. This is insofar of importance as both quantities are often modeled as a single valued function of the average energy. A comparison with Monte Carlo simulation data reveals that this error in the mobilities and the error introduced in the closure relation cause a spurious overshoot in the velocity characteristics.

Based on the observations made during the evaluation of transport models including the first four moments of Boltzmann's transport equation, an extended model has been pro-

posed which includes the first six moments. The additional even order moment, the kurtosis of the distribution function, has been proven to be beneficial for device simulation and the modeling of hot-carrier effects.

Several interesting cases where the heated Maxwellian assumption introduces impermissibly large errors have been discussed, particularly impact ionization, hot-carrier gate currents, and hot-carrier degradation. Highly satisfactory results are obtained in all cases. The six-moment transport model, the six-moment impact ionization model, and the six-moment gate current model have been implemented in the device simulator MINIMOS-NT [117]. It has been demonstrated that the six-moment model can improve on the drift-diffusion and energy transport models and still has the advantage of vastly reduced numerical costs in relation to Monte Carlo simulations [11,74].

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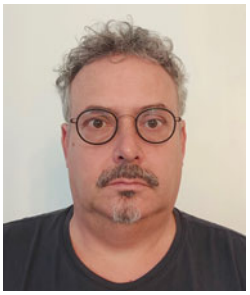

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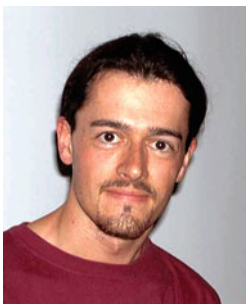

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Grid Generation and Algebraic Solvers

38

Aurelio Giancarlo Mauri, Benedetta Morini, Simona Perotto, and Fiorella Sgallari

Contents

38.1 Introduction and Motivations 1383

38.2 Modeling Semiconductor Devices 1385
38.2.1 The Scaled Dimensionless DD Model 1386

38.3 The Gummel Map 1386
38.3.1 Toward the Numerical Solution of the Gummel Map . . . 1388
38.3.2 The Discretization of the Gummel Map 1389

38.4 The Fully Coupled Newton Approach 1390

38.5 Grid Generation: The Basics 1391
38.5.1 Structured Meshes 1392
38.5.2 Unstructured Meshes 1392
38.5.3 Hybrid Meshes 1393
38.5.4 Advanced Techniques: Mesh Adaptation 1393
38.5.5 Meshes for Semiconductor Devices 1396

38.6 Algebraic Solvers 1398
38.6.1 Nonlinear Solvers 1398
38.6.2 Linear Solvers 1401

38.7 The n-MOSFET Test Case 1402
38.7.1 Comparison of Sparse Solution Techniques 1403
38.7.2 Numerical Assessment 1406

References 1407

Abstract

This work focuses on some of the most relevant numerical issues in the solution of the drift-diffusion model for semiconductor devices. The drift-diffusion model consists of an elliptic and two parabolic partial differential equations which are nonlinearly coupled. A reliable numerical approximation of this model unavoidably leads to choose a suitable tessellation of the computational domain as well as specific solvers for linear and nonlinear systems of equations. These are the two main issues tackled in this work, after introducing a classical discretization of the drift-diffusion model based on finite elements. Numerical experiments are also provided to investigate the performances both of up-to-date and of advanced numerical procedures.

Keywords

Finite elements · Gummel map · Hybrid meshes · Mesh adaptivity · Sparse solvers · Preconditioning · Newton methods · Linesearch method

38.1 Introduction and Motivations

Partial differential equations (PDEs) can be used to model a wide variety of phenomena, ranging from sound propagation, heat transfer, diffusion processes, electrostatics, electrodynamics, fluid dynamics, elasticity, or quantum mechanics. A PDE model generally coincides with an equation (or with a system of equations) of the form

$$\mathcal{P}\left(x_1, \ldots, x_d, t, u, \frac{\partial u}{\partial t}, \frac{\partial u}{\partial x_1}, \ldots, \frac{\partial u}{\partial x_d}, \ldots, \frac{\partial^{k_t+k_1+\ldots+k_d} u}{\partial^{k_t} t\, \partial^{k_1} x_1 \cdots \partial^{k_d} x_d}, f\right) = 0, \tag{38.1}$$

with $\mathbf{x} = (x_1, \ldots, x_d)^{\mathrm{T}} \in \Omega \subset \mathbb{R}^d$ and $t \in I \subset \mathbb{R}$ the independent variables, $u = u(\mathbf{x}, t)$ the unknown function, f

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the set of data, and where $\mathcal{P}$ mathematically translates the (mass, momentum, energy) conservation laws involved by the phenomenon at hand [1–3]. The law $\mathcal{P}$ is defined in the space-time domain $Q = \Omega \times I$, and it may be linear or nonlinear with respect to u and the involved derivatives, homogeneous or nonhomogeneous according to the presence or the absence of a source term feeding the system.

Model (38.1) has to be completed with initial and boundary conditions. Initial data specify the starting configuration of the modeled system. Boundary conditions constrain the problem evolution at the boundary, $\partial\Omega$, of the physical domain, by tuning, for instance, the value of the solution (Dirichlet conditions) or of the flux of the solution (Neumann conditions), or of a weighted combination of u and its flux (Robin conditions).

A classification at least for the second-order linear PDEs, which are the most frequently encountered in applications, is well-established. It is based on the *discriminant*, $\mathcal{D}$, of the differential operator, which combines the coefficients (here assumed constant) of the highest order derivatives, so that one can distinguish among elliptic ($\mathcal{D} < 0$), parabolic ($\mathcal{D} = 0$), and hyperbolic ($\mathcal{D} > 0$) PDEs. This classification gives an insight on the smoothness of the solution and on how it does depend on the initial and on the boundary conditions. In particular, when dealing with hyperbolic PDEs, the smoothness of the solution depends on the smoothness of the initial and of the boundary conditions (e.g., a discontinuity in the data propagates as a shock in the solution while, if the equation is nonlinear, shocks may occur even though the data are smooth). In contrast, the solution of an elliptic PDE is smooth although the initial and boundary conditions are rough. Parabolic PDEs are associated with time-dependent processes. Solutions are smooth in space but may exhibit singularities during the time window.

The modeling of the physical mechanisms occurring in modern semiconductor devices involves several aspects, such as the electrical transport, the thermal generation, mechanical stresses, the atomic migration, and chemical reactions. The most recurrent PDE problem to model the carrier transport in semiconductors is represented by the drift-diffusion model [4], which describes the electronic and the hole current flow in terms of a drift and a diffusion contribution. From a modeling viewpoint, the drift-diffusion equations coincide with an elliptic and two parabolic PDEs which are nonlinearly coupled and deserve an ad hoc theoretical as well as numerical investigation [5–7].

In practical problems, the integral to the PDE model (38.1) is generally not available, so that the solution u is approximated by numerical methods. The numerical solution of PDEs requires the replacement of the continuous differential equations with a discrete counterpart. This step is known as *discretization*. The specific features of the PDE affect the choice of the discretization. Essentially, we can distinguish between two main settings, namely, when the discretization takes place at discrete points or over discrete cells. The former approach coincides with a *finite difference* (FD) discretization (see, e.g., [8]), where the derivatives in the PDE are approximated at specific points by difference quotients obtained via the Taylor series expansion. The second approach considers the integral (weak) form of the PDE to represent the solution over discrete cells in terms of selected functions and then to integrate these functions analytically over the volume (*finite element* (FE) discretization, see, e.g., [9]), or to balance the fluxes through the cell sides (*finite volume* (FV) discretization, see, e.g., [10]). This chapter primarily focuses on the FE method. Independently of the adopted discretization, the key role to move from a continuous to a discrete setting is played by the generation of the computational mesh which provides a discrete representation of the physical domain Ω. Grid generation is the practice of creating a tessellation of a continuous geometric space into discrete cells [11–14]. The actual goal is to create a mesh that accurately describes the domain geometry and that, possibly, follows the main features of the solution, to better model the phenomenon under investigation. In particular, tessellations ensuring this last property are known as adapted meshes [11,12,15,16]. Ideally, the number of the cells should be the smallest possible to ensure a certain discretization accuracy and to make computations affordable. As an alternative, one could be interested in setting the number of mesh elements while maximizing the accuracy of the discretization. Generating a good computational grid becomes an important issue, especially in the presence of problems characterized by complex trends, such as singularities or boundary/internal layers, which pose additional challenges in the numerical solution. This is, for instance, the case of any semiconductor device. The presence of regions with a different type of doping requires ad hoc meshes to accurately describe the doping variation across the junctions. Moreover, the presence of material interfaces (e.g., between the silicon and the silicon oxide) or the use of polycrystalline materials induces complex physical mechanisms in correspondence with these interfaces that deserve to be carefully computed. This demands for meshes closely refined in such areas [17,18].

Concerning the time discretization, numerical methods can be divided into explicit and implicit algorithms. Among the most widely employed schemes, we mention the θ-method (which includes the well-known Euler and Crank-Nicolson algorithms), the backward differentiation formulas (BDF), and the Runge-Kutta schemes [19]. Implicit methods require an extra computation with respect to explicit schemes. However, for a wide class of problems (e.g., when dealing with stiff problems), explicit methods require impractical small time steps to ensure numerical stability, so that implicit schemes become the choice since allowing much

larger time steps [19]. Thus, the time partition is, in general, driven by stability considerations. Although less recurrent than the spatial one, adaptivity in time turns out to be a useful tool, especially when the modeled phenomena exhibit strong temporal heterogeneities. In semiconductor modeling, a standard approach to discretize the time dependence combines BDF schemes with the θ-method [20].

As the last step, the discretization of a model leads to solve a system of equations which may be linear or nonlinear according to the PDE involved and, in general, of large scale when tackling real-life problems. There exists a large variety of solvers for these systems. Among the most efficient linear solvers, we cite the preconditioned Krylov subspace methods [21]. Similar concepts can be used for nonlinear systems, where different nonlinear solvers can be combined to significantly improve the computational efficiency.

The chapter is organized as follows. Section 38.2 is devoted to the drift-diffusion model which is introduced both in the standard and in the scaled form. In Sect. 38.3 we introduce the Gummel map, which represents a very well-known tool to solve the drift-diffusion system. In particular, we provide the corresponding weak form and FE discretization, in order to obtain the algebraic counterpart of the Gummel map. Section 38.4 introduces the fully coupled Newton method which represents an alternative to the Gummel map to deal with the drift-diffusion model. The focus is mainly on the solvers to deal with the nonlinear systems characterizing such an approach. Sections 38.5 and 38.6 represent the core of the chapter. The former offers a rich survey about standard and advanced techniques for grid generation, by including examples of different types of meshes for a n-MOSFET semiconductor device. Section 38.6 focuses both on nonlinear and linear solvers to deal with the algebraic counterpart of the procedures in Sects. 38.2 and 38.4. Finally, the last Sect. 38.7 provides a numerical assessment of the methodological part when applied to a n-MOSFET device, with a specific attention to the role played by the selected computational grid and by the adopted solver in order to improve the accuracy and the efficiency of the simulations based on the drift-diffusion model.

38.2 Modeling Semiconductor Devices

In this section, we shortly review the drift-diffusion (DD) model, together with the associated initial and boundary conditions. For more details, we refer the reader, for instance, to [6,7].

The DD model is currently the most used approach to model the transport in semiconductors. DD equations were introduced by W. Van Roosbroeck in 1950 as a conservation system for electron and hole carriers, along with the electric field [4]. From a geometric viewpoint, a standard

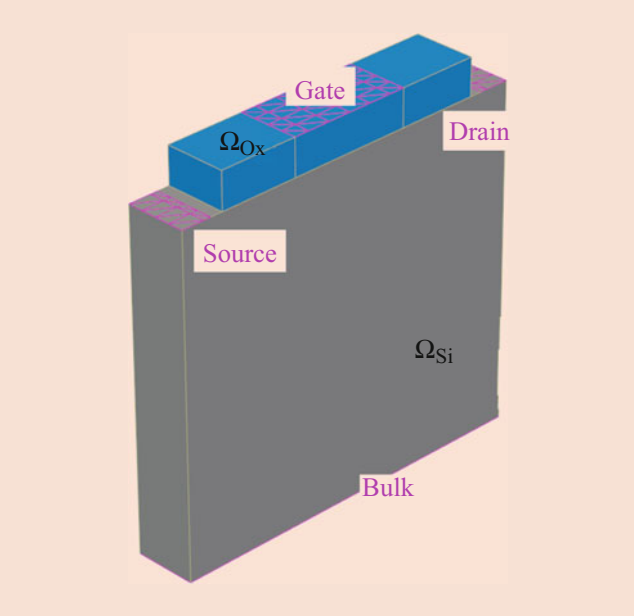

Fig. 38.1 Sketch of the geometry for a 3D MOSFET: the purple areas represent the electrical terminals (drain, source, gate, and bulk), where the boundary conditions of the DD system are assigned. Domains Ω_{Si} and Ω_{Ox}, of dimension $0.3 \times 0.05 \times 0.27\,\mu m^3$ and $0.22 \times 0.05 \times 0.01\,\mu m^3$, respectively, are highlighted

semiconductor device coincides with a bounded and simply connected domain $\Omega \subset \mathbb{R}^d$ ($d = 1, 2, 3$), which consists of a semiconductor part, Ω_{Si}, and, in the case of a metal-oxide-semiconductor (MOS), of a portion of thin oxide, Ω_{Ox}, which is adjacent to Ω_{Si}, so that $\bar{\Omega} = \bar{\Omega}_{Si} \cup \bar{\Omega}_{Ox}$ (see Fig. 38.1 for a sketch). The DD model is provided by the system

$$\begin{cases} \nabla \cdot \mathbf{D} = q(p - n + \bar{N}) \ \text{ with } \ \mathbf{D} = -\varepsilon \nabla\varphi = \varepsilon \mathbf{E} & \text{in } \mathbf{Q} \\ \dfrac{\partial n}{\partial t} - \dfrac{1}{q} \nabla \cdot \mathbf{J}_n = -R & \text{with } \ \mathbf{J}_n = q\mu_n n \mathbf{E} + qD_n \nabla n \ \text{ in } \mathbf{Q}_{Si} \\ \dfrac{\partial p}{\partial t} + \dfrac{1}{q} \nabla \cdot \mathbf{J}_p = -R & \text{with } \ \mathbf{J}_p = q\mu_p p \mathbf{E} - qD_p \nabla p \ \text{ in } \mathbf{Q}_{Si}, \end{cases} \tag{38.2}$$

whose unknowns coincide with the electrostatic potential, φ; the electron concentration, n; and the hole concentration, p, being $\mathbf{Q} = \Omega \times (0, t_f)$ and $\mathbf{Q}_{Si} = \Omega_{Si} \times (0, t_f)$, with t_f the final time of the considered time window. In particular, $\mathbf{D}$ models the electric displacement; $\mathbf{E}$ is the electric field; q is the positive electron charge; ε denotes the dielectric constant of the material; μ_n, μ_p and D_n, D_p are the mobilities and the diffusion coefficients of n and p, respectively; R is the net recombination/generation rate; $\bar{N} = N_D^+ - N_A^-$ is the net doping profile resulting from the sum of donors, N_D^+, and acceptors, N_A^-; $\mathbf{J}_n$ is the electron current density; and $\mathbf{J}_p$ is the hole current density.

Exploiting the explicit expression for $\mathbf{D}$, $\mathbf{J}_n$, and $\mathbf{J}_p$, we obtain a system of elliptic equations. In particular, the first

equation leads to the standard Poisson problem for the scalar variable φ, being

$$-\nabla\cdot(\varepsilon\nabla\varphi)=q(p-n+\bar{N})\ \text{ in } \mathbf{Q}. \tag{38.3}$$

The two remaining equations coincide with a nonlinear advection-diffusion-reaction model for n and p, respectively, and can be rewritten as

$$\begin{cases}\dfrac{\partial n}{\partial t}+\dfrac{1}{q}\nabla\cdot(q\mu_{\mathrm{n}}n\nabla\varphi-qD_{\mathrm{n}}\nabla n)=-\left(np-n_i^2\right)\mathcal{F}(n,p) & \text{in } \mathbf{Q}_{\mathrm{Si}}\\ \dfrac{\partial p}{\partial t}-\dfrac{1}{q}\nabla\cdot(q\mu_{\mathrm{p}}p\nabla\varphi+qD_{\mathrm{p}}\nabla p)=-\left(np-n_i^2\right)\mathcal{F}(n,p) & \text{in } \mathbf{Q}_{\mathrm{Si}}\end{cases} \tag{38.4}$$

with n_i the intrinsic concentration of the semiconductor material, representing the number of electrons and holes available for the electric conduction if $\bar{N}=0$ (see [22, Chapter 1]). For the rate R, we adopt the general form $(np-n_i^2)\mathcal{F}(n,p)$, which can model several recombination/generation mechanisms, by properly setting $\mathcal{F}$.

Concerning the boundary conditions completing the DD model, we have to distinguish between the Dirichlet, $\partial\Omega_{\mathrm{D}}$, and the Neumann, $\partial\Omega_{\mathrm{N}}$, portions of the boundary $\partial\Omega$ of Ω. With reference to the device in Fig. 38.1, $\partial\Omega_{\mathrm{D}}$ includes the MOSFET electrical terminals (drain, source, gate, and bulk) which are assumed to be ideal Ohmic contacts, while $\partial\Omega_{\mathrm{N}}$ coincides with the remaining portion of the boundary, i.e., $\partial\Omega_{\mathrm{N}}=\partial\Omega\setminus\partial\Omega_{\mathrm{D}}$. On $\partial\Omega_{\mathrm{D}}$, we assign nonhomogeneous data to all the unknowns, namely,

$$\varphi=\varphi_{\mathrm{D}},\quad n=n_{\mathrm{D}},\quad p=p_{\mathrm{D}}, \tag{38.5}$$

while we impose homogeneous data on $\partial\Omega_{\mathrm{N}}$ (i.e., we require that the fluxes of the electric field and of the current densities vanish across $\partial\Omega_{\mathrm{N}}$). To determine φ_{D}, n_{D}, and p_{D}, we enforce the thermodynamical equilibrium and charge neutrality conditions [22].

As far as the initial values is concerned, conditions $n=n_0$, $p=p_0$ are assigned consistently with the doping profile $\bar{N}$ and according to the Maxwell-Boltzmann distribution [22], whereas the initial value $\varphi=\varphi_0$ is obtained by prolongating the bias applied to the contacts into the whole domain (for more details, we refer to [5]).

Finally, we remark that the DD model actually consists of three nonlinear equations. Indeed, the electron and the hole concentrations are related to the potential φ via the Maxwell-Boltzmann statistics, being

$$n=n_i\exp\left(\frac{\varphi-\varphi_{\mathrm{n}}}{V_{\mathrm{th}}}\right),\quad p=n_i\exp\left(\frac{\varphi_{\mathrm{p}}-\varphi}{V_{\mathrm{th}}}\right), \tag{38.6}$$

where φ_{n} and φ_{p} are the electrochemical potentials and $V_{\mathrm{th}}=K_{\mathrm{B}}T/q$ is the thermal potential, with K_{B} the Boltzmann constant and T the device temperature. Thus, the Poisson equation (38.3) turns out to be nonlinear with respect to φ. In practice, the nonlinearity characterizing the DD model is tackled by resorting to two alternative strategies, i.e., the decoupling Gummel approach or the fully coupled Newton approach which will be tackled in Sects. 38.3 and 38.4, respectively.

38.2.1 The Scaled Dimensionless DD Model

Models (38.3) and (38.4) depend on quantities characterized by a different physical dimension. It is advisable to reformulate such a model in a dimensionless form, in order to reduce possible numerical oscillations (see Sect. 38.4). One possibility consists in scaling the potential by the thermal voltage, V_{th}; the concentration by the intrinsic concentration, n_i; and the length by the characteristic Debye length, $L_{\mathrm{D}}=\sqrt{\varepsilon V_{\mathrm{th}}/(qn_i)}$ [23]. Another option leads to scale the potential by the thermal voltage, V_{th}, the concentration by the maximum value of $\bar{N}$ over the whole domain, and the length by a characteristic device dimension [7, 24]. By adopting, for simplicity, the same notation for the unscaled and scaled unknowns, we can write the scaled dimensionless DD model as

$$\begin{cases}-\lambda^2\nabla\cdot(\varepsilon\nabla\varphi)=p-n+\bar{N} & \text{in } \mathbf{Q}\\ \dfrac{\partial n}{\partial t}+\nabla\cdot(\mu_{\mathrm{n}}(n\nabla\varphi-\nabla n))=-R & \text{in } \mathbf{Q}_{\mathrm{Si}}\\ \dfrac{\partial p}{\partial \hat{t}}-\nabla\cdot\left(\mu_{\mathrm{p}}(p\nabla\varphi+\nabla p)\right)=-R & \text{in } \mathbf{Q}_{\mathrm{Si}}\end{cases} \tag{38.7}$$

being

$$D=-\varepsilon\nabla\varphi,\ \mathbf{J}_{\mathrm{n}}=\mu_{\mathrm{n}}(-n\nabla\varphi+\nabla n),\ \mathbf{J}_{\mathrm{p}}=-\mu_{\mathrm{p}}(p\nabla\varphi+\nabla p) \tag{38.8}$$

and where λ^2 is a scalar depending on the adopted scaling. We refer to [25, p. 326] for a complete list of possible choices for the scaling factors. Clearly, the scaling has to be applied also to the boundary and to the initial conditions.

In the sequel, we will essentially refer to formulations (38.3) and (38.4), although in some context the dimensionless model plays a crucial role [26].

38.3 The Gummel Map

To simplify the discussion, we neglect the time dependence in (38.3) and (38.4). Actually, the Gummel map is an iterative algorithm originally proposed in [27] to solve this stationary problem, although it can be extended to a time-dependent setting in a straightforward way. The basic idea is to preserve the nonlinearity only for the Poisson equation (38.3), while linearizing the continuity equation for the electrons and for

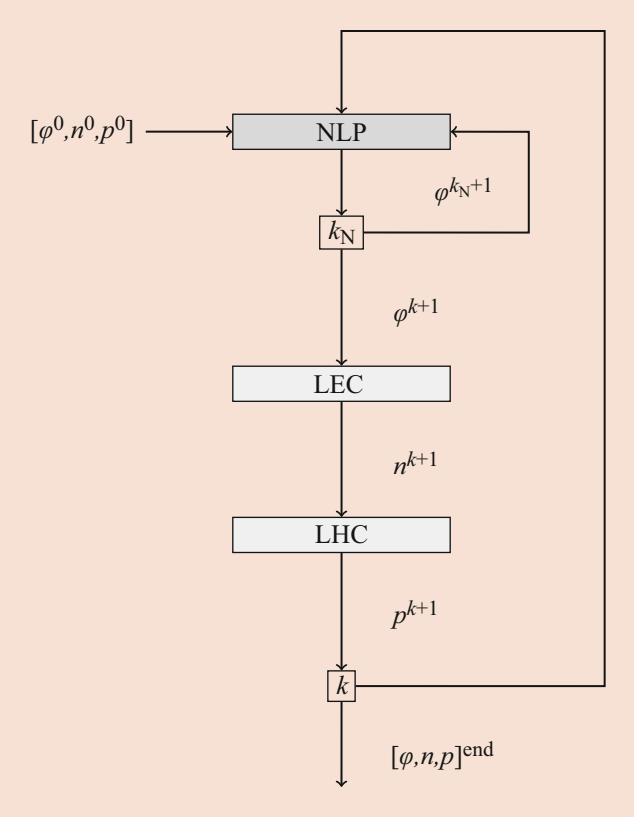

Fig. 38.2 Flowchart of the Gummel map

the holes. In particular, we tackle the nonlinearity in (38.3) by resorting to the standard Newton method (in this section, we limit to a plain use of this algorithm, while referring to Sect. 38.6.1 for all the details and for more sophisticated variants of it). The whole decoupling Gummel algorithm is outlined in Fig. 38.2, where NLP stands for nonlinear Poisson problem, whereas LEC and LHC denote the linearized electron and hole continuity equations. We distinguish between the Gummel iterations, identified by index k, and the Newton iterations, identified by index k_N.

At the generic iteration, $k+1$, of the Gummel map, first we approximate the electrostatic potential φ via φ^{k+1}, where φ^{k+1} denotes the value Newton algorithm converges to. In more detail, at the generic iteration, k_N+1, of the Newton method, we compute the approximation φ^{k_N+1} for φ^{k+1} such that

$$\varphi^{k_N+1} = \varphi^{k_N} + \delta\varphi^{k_N},$$

where the update $\delta\varphi^{k_N}$ is the solution to the problem

$$\begin{cases} \nabla\cdot(-\varepsilon\nabla\delta\varphi^{k_N}) + \sigma^{k_N}\delta\varphi^{k_N} = -f^{k_N} & \text{in } \Omega \\ \delta\varphi^{k_N} = 0 & \text{on } \partial\Omega_D \\ \varepsilon\nabla\delta\varphi^{k_N}\cdot\mathbf{n} = 0 & \text{on } \partial\Omega_N, \end{cases} \tag{38.9}$$

with $\mathbf{n}$ the unit outward normal vector to the boundary, and with

$$\sigma^{k_N} = \begin{cases} \dfrac{qn_i}{V_{th}}\left(\exp\left(\dfrac{\varphi_p-\varphi^{k_N}}{V_{th}}\right)+\exp\left(\dfrac{\varphi^{k_N}-\varphi_n}{V_{th}}\right)\right) & \text{in } \Omega_{Si} \\ 0 & \text{in } \Omega_{Ox} \end{cases} \tag{38.10}$$

and

$$f^{k_N} = \begin{cases} \nabla\cdot(-\varepsilon\nabla\varphi^{k_N}) - qn_i\left(\exp\left(\dfrac{\varphi_p-\varphi^{k_N}}{V_{th}}\right)-\exp\left(\dfrac{\varphi^{k_N}-\varphi_n}{V_{th}}\right)\right) - q\tilde{N} & \text{in } \Omega_{Si} \\ \nabla\cdot(-\varepsilon\nabla\varphi^{k_N}) & \text{in } \Omega_{Ox}. \end{cases}$$

Then, we linearize equations (38.4). With this aim, we replace φ with φ^{k+1}, and we compute the right-hand side of Eqs. $(38.4)_1$ and $(38.4)_2$, here denoted by R_n^{k+1} and R_p^{k+1}, respectively, as

$$\begin{aligned} R_n^{k+1} &= -\left(n^{k+1}p^k - n_i^2\right)F(n^k,p^k), \\ R_p^{k+1} &= -\left(n^k p^{k+1} - n_i^2\right)F(n^k,p^k). \end{aligned} \tag{38.11}$$

If other recombination/generation mechanisms are considered, the same type of linearization can be adopted in a straightforward way. Thus, we obtain LEC and LHC equations which read

$$\begin{cases} \nabla\cdot\left(q\mu_n^{k+1}n^{k+1}\nabla\varphi^{k+1} - qD_n^{k+1}\nabla n^{k+1}\right) = qR_n^{k+1} & \text{in } \Omega_{Si} \\ n^{k+1} = n_D & \text{on } \partial\Omega_{D,Si} \\ \nabla n^{k+1}\cdot\mathbf{n} = 0 & \text{on } \partial\Omega_{N,Si} \end{cases} \tag{38.12}$$

and

$$\begin{cases} -\nabla\cdot\left(q\mu_p^{k+1}p^{k+1}\nabla\varphi^{k+1} + qD_p^{k+1}\nabla p^{k+1}\right) = qR_p^{k+1} & \text{in } \Omega_{Si} \\ p^{k+1} = p_D & \text{on } \partial\Omega_{D,Si} \\ \nabla p^{k+1}\cdot\mathbf{n} = 0 & \text{on } \partial\Omega_{N,Si}, \end{cases} \tag{38.13}$$

respectively with $\partial\Omega_{D,Si} = \partial\Omega_D \cap \partial\Omega_{Si}$, $\partial\Omega_{N,Si} = \partial\Omega_N \cap \partial\Omega_{Si}$. Notice that the mobilities as well as the diffusion coefficients might depend on φ, n, and p, so that they have to be updated throughout Gummel iterations. The idea is to compute these quantities by exploiting the same linearization as in (38.11) in order to preserve the linearity of Eqs. (38.12) and (38.13).

Finally, problems (38.12) and (38.13) are solved with respect to the carrier densities, n^{k+1} and p^{k+1}, respectively, which are successively used to compute the quasi-Fermi potentials, φ_n and φ_p, in (38.10) via the formulas (38.6), before restarting the Gummel iterations.

Suitable stopping criteria clearly control both the Gummel and Newton loops. Standard choices are based on the residual (to stop NLP iterations) and on the increment (to stop LEC and LHC iterations). Moreover, we remark that the current definition of R_n^{k+1} and R_p^{k+1} in (38.11) allows us to solve LEC

and LHC problems in parallel, in the spirit of a Jacobi solver. As an alternative, one can modify the definition of R_{p}^{k+1} by replacing n^k with n^{k+1}, this leading to a sequential Gauss-Seidel-like solver.

38.3.1 Toward the Numerical Solution of the Gummel Map

The numerical solution of the Gummel map moves from the weak formulation of the corresponding differential problems and the associated well-posedness analysis. In the sequel, we adopt standard notation for the function spaces involved in this analysis [28]. For the sake of simplicity, we remove any dependence on the indices associated with the Gummel and Newton iterations throughout the whole section.

Let us first consider Eq. (38.9), whose weak form reads: find $\delta\varphi \in V = H^1_{0,\partial\Omega_{\mathrm{D}}}(\Omega)$ such that

$$a_{\mathrm{NLP}}(\delta\varphi, v) = F_{\mathrm{NLP}}(v) \quad \forall v \in V, \tag{38.14}$$

whose bilinear and linear forms, $a_{\mathrm{NLP}} : V \times V \to \mathbb{R}$ and $F_{\mathrm{NLP}} : V \to \mathbb{R}$, are defined by

$$\begin{aligned} a_{\mathrm{NLP}}(u, v) &= \int_\Omega \varepsilon \nabla u \cdot \nabla v \, \mathrm{d}\Omega + \int_\Omega \sigma u v \, \mathrm{d}\Omega, \\ F_{\mathrm{NLP}}(v) &= \int_\Omega -f v \, \mathrm{d}\Omega, \end{aligned} \tag{38.15}$$

respectively for any $u, v \in V$. The boundary conditions in (38.9) are exploited to choose space V and to erase the boundary contributions yielded by the integration by parts of the diffusive term.

The well-posedness of problem (38.14) is analyzed by resorting to the Lax-Milgram lemma [1, 28]. The continuity of $a_{\mathrm{NLP}}(\cdot,\cdot)$ is proved by combining Hölder with Cauchy-Schwarz inequalities and by exploiting the definition of the norm in V. This leads to the upper bound

$$\begin{aligned} \left|a_{\mathrm{NLP}}(u, v)\right| &\le \|\varepsilon\|_{L^\infty(\Omega)} \|\nabla u\|_{L^2(\Omega)} \|\nabla v\|_{L^2(\Omega)} \\ &\quad + \|\sigma\|_{L^\infty(\Omega)} \|u\|_{L^2(\Omega)} \|v\|_{L^2(\Omega)} \\ &\le \left[\|\varepsilon\|_{L^\infty(\Omega)} + \|\sigma\|_{L^\infty(\Omega)}\right] \|u\|_V \|v\|_V, \end{aligned} \tag{38.16}$$

after assuming $\varepsilon, \sigma \in L^\infty(\Omega)$, with $M = \|\varepsilon\|_{L^\infty(\Omega)} + \|\sigma\|_{L^\infty(\Omega)}$ the continuity constant of the bilinear form. (We can relax the regularity assumption on σ, by choosing $\sigma \in L^2(\Omega)$. By exploiting inequality $\|uv\|_{L^2(\Omega)} \le \|u\|_{L^4(\Omega)} \|v\|_{L^4(\Omega)}$ and the Sobolev immersion theorem, we have $\left|a_{\mathrm{NLP}}(u, v)\right| \le [\|\varepsilon\|_{L^\infty(\Omega)} + \|\sigma\|_{L^2(\Omega)}] \|u\|_V \|v\|_V$, i.e., the continuity property with $M = \|\varepsilon\|_{L^\infty(\Omega)} + \|\sigma\|_{L^2(\Omega)}$.) The coercivity of $a_{\mathrm{NLP}}(\cdot,\cdot)$ is guaranteed by requiring $\varepsilon(\mathbf{x}) \ge \varepsilon_{\mathrm{m}} > 0$ a.e. in Ω and $\sigma(\mathbf{x}) \ge 0$ a.e. in Ω, so that we have, for any $v \in V$,

$$a_{\mathrm{NLP}}(v, v) \ge \varepsilon_{\mathrm{m}} \left\|\nabla v\right\|^2_{L^2(\Omega)} \ge \frac{\varepsilon_{\mathrm{m}}}{1 + C_{\mathrm{P}}^2} \|v\|^2_V, \tag{38.17}$$

with $\alpha = \varepsilon_{\mathrm{m}}/(1 + C_{\mathrm{P}}^2)$ the coercivity constant of the bilinear form and where C_{P} denotes the Poincaré constant. Finally, the continuity of $F_{\mathrm{NLP}}(\cdot)$ is ensured by selecting $f \in L^2(\Omega)$. Indeed, the Cauchy-Schwarz inequality together with the definition of the norm in V leads to the bound

$$\left|F_{\mathrm{NLP}}(v)\right| \le \|f\|_{L^2(\Omega)} \|v\|_{L^2(\Omega)} \le \|f\|_{L^2(\Omega)} \|v\|_V \tag{38.18}$$

for any $v \in V$, so that $\tilde{C} = \|f\|_{L^2(\Omega)}$ represents the continuity constant for the linear form.

Now we consider Eq. (38.12). After simplifying q throughout all the terms, we rewrite the LEC problem as an advection-diffusion-reaction problem (in conservative form), namely, as

$$\begin{cases} -\nabla \cdot (D_{\mathrm{n}} \nabla n) + \nabla \cdot (\boldsymbol{\beta}_{\mathrm{n}} n) + \sigma_{\mathrm{n}} n = f_n & \text{in } \Omega_{\mathrm{Si}} \\ n = n_{\mathrm{D}} & \text{on } \partial\Omega_{\mathrm{D,Si}} \\ \nabla n \cdot \mathbf{n} = 0 & \text{on } \partial\Omega_{\mathrm{N,Si}} \end{cases} \tag{38.19}$$

with $\boldsymbol{\beta}_{\mathrm{n}} = \mu_{\mathrm{n}} \nabla\varphi$, $\sigma_{\mathrm{n}} = p\tilde{F}$, $f_{\mathrm{n}} = n_i^2 \tilde{F}$ and where we have denoted function $F(n^k, p^k)$ in (38.11) by $\tilde{F}$, made computable thanks to the performed linearization.

The weak form of the LEC equations is generally stated after rewriting (38.19) in terms of the so-called Slotboom variable [29]

$$u_n = n_i \exp\left(-\frac{\varphi_{\mathrm{n}}}{V_{\mathrm{th}}}\right), \tag{38.20}$$

so that n and u_n are related by

$$n = \exp\left(\frac{\varphi}{V_{\mathrm{th}}}\right) u_{\mathrm{n}}.$$

Notice that

$$\nabla u_{\mathrm{n}} = \exp\left(-\frac{\varphi}{V_{\mathrm{th}}}\right) \nabla n - \exp\left(-\frac{\varphi}{V_{\mathrm{th}}}\right) \frac{n}{V_{\mathrm{th}}} \nabla\varphi$$

and thanks to Einstein's relation, $D_{\mathrm{n}} = \mu_{\mathrm{n}} V_{\mathrm{th}}$. Thus, it follows

$$\begin{aligned} \nabla \cdot \left(-D_{\mathrm{n}} \exp\left(\frac{\varphi}{V_{\mathrm{th}}}\right) \nabla u_{\mathrm{n}}\right) &= \nabla \cdot (-D_{\mathrm{n}} \nabla n + \mu_{\mathrm{n}} n \nabla\varphi) \\ &= \nabla \cdot \left(-D_{\mathrm{n}} \nabla n + \boldsymbol{\beta}_{\mathrm{n}} n\right). \end{aligned}$$

Exploiting this relation in (38.19) and the boundary conditions for the potential on $\partial\Omega_{\mathrm{N}}$, we obtain

$$\begin{cases} \nabla \cdot \left(-D_{\mathrm{n}} \exp\left(\dfrac{\varphi}{V_{\mathrm{th}}}\right) \nabla u_{\mathrm{n}}\right) + \sigma_{\mathrm{n}} \exp\left(\dfrac{\varphi}{V_{\mathrm{th}}}\right) u_{\mathrm{n}} = f_{u_{\mathrm{n}}} & \text{in } \Omega_{\mathrm{Si}} \\ u_{\mathrm{n}} = n_{\mathrm{D}} \exp\left(-\dfrac{\varphi}{V_{\mathrm{th}}}\right) & \text{on } \partial\Omega_{\mathrm{D,Si}} \\ \nabla u_{\mathrm{n}} \cdot \mathbf{n} = 0 & \text{on } \partial\Omega_{\mathrm{N,Si}}, \end{cases} \tag{38.21}$$

where $f_{u_{\mathrm{n}}}$ coincides with function f_{n} in (38.19) properly rewritten in terms of the Slotboom variable.

To provide the weak form of Eq. (38.21), we pick the space $W = H^1_{0,\partial\Omega_{\mathrm{D,Si}}}(\Omega_{\mathrm{Si}})$, so that, we have: find $u_{\mathrm{n}} \in W$ such that

$$a_{\mathrm{LEC}}(u_{\mathrm{n}}, w) = F_{\mathrm{LEC}}(w) \quad \forall w \in W, \tag{38.22}$$

where the bilinear and linear forms, $a_{\mathrm{LEC}} : W \times W \to \mathbb{R}$ and $F_{\mathrm{LEC}} : W \to \mathbb{R}$, are defined by

$$\begin{aligned} a_{\mathrm{LEC}}(u, w) &= \int_{\Omega_{\mathrm{Si}}} D_{\mathrm{n}} \exp\left(\frac{\varphi}{V_{\mathrm{th}}}\right) \nabla u \cdot \nabla w \, d\Omega_{\mathrm{Si}} \\ &\quad + \int_{\Omega_{\mathrm{Si}}} \sigma_{\mathrm{n}} \exp\left(\frac{\varphi}{V_{\mathrm{th}}}\right) uw \, d\Omega_{\mathrm{Si}}, \\ F_{\mathrm{LEC}}(w) &= \int_{\Omega_{\mathrm{Si}}} f_{u_{\mathrm{n}}} w \, d\Omega_{\mathrm{Si}} - a_{\mathrm{LEC}}(R_{u_{\mathrm{n}}}, w), \end{aligned} \tag{38.23}$$

respectively for any $u, w \in W$, and where $R_{u_{\mathrm{n}}} \in H^1(\Omega_{\mathrm{Si}})$ denotes the lifting of the nonhomogeneous Dirichlet data in (38.21), so that, $R_{u_{\mathrm{n}}}\big|_{\partial\Omega_{\mathrm{D,Si}}} = n_{\mathrm{D}} \exp(-\varphi/V_{\mathrm{th}})$.

We exploit the Lax-Milgram lemma to investigate the well-posedness of problem (38.22). By adopting the notation $\gamma_{\mathrm{n}} = D_{\mathrm{n}} \exp(\varphi/V_{\mathrm{th}})$, $\delta_{\mathrm{n}} = \sigma_{\mathrm{n}} \exp(\varphi/V_{\mathrm{th}})$, we can repeat computations in (38.16) and (38.17), so that we can ensure the continuity and the coercivity of the bilinear form $a_{\mathrm{LEC}}(\cdot,\cdot)$ under the hypotheses $\gamma_{\mathrm{n}}, \delta_{\mathrm{n}} \in L^\infty(\Omega_{\mathrm{Si}})$, $\gamma_{\mathrm{n}}(\mathbf{x}) \geq \gamma_{\mathrm{n,m}} > 0$ a.e. in Ω_{Si}, $\delta_n(\mathbf{x}) \geq 0$ a.e. in Ω_{Si}, with $M_{\mathrm{n}} = \|\gamma_{\mathrm{n}}\|_{L^\infty(\Omega_{\mathrm{Si}})} + \|\delta_{\mathrm{n}}\|_{L^\infty(\Omega_{\mathrm{Si}})}$ and $\alpha_{\mathrm{n}} = \gamma_{\mathrm{n,m}}/(1 + C_{\mathrm{P}}^2)$ the continuity and coercivity constant, respectively. As far as the continuity of $F_{\mathrm{LEC}}(\cdot)$ is concerned, following (38.18) and by exploiting the continuity of $a_{\mathrm{LEC}}(\cdot,\cdot)$, we have

$$\left|F_{\mathrm{LEC}}(w)\right| \leq \|f_{u_{\mathrm{n}}}\|_{L^2(\Omega_{\mathrm{Si}})} \|w\|_W + M_{\mathrm{n}} \|R_{u_{\mathrm{n}}}\|_W \|w\|_W$$

for any $w \in W$, so that, for $f_{u_{\mathrm{n}}} \in L^2(\Omega_{\mathrm{Si}})$, we can guarantee the continuity of the linear form. The well-posedness of (38.22) thus follows.

Problem (38.13) can be addressed analogously to LEC equation, by introducing the corresponding Slotboom variable $u_{\mathrm{p}} = n_i \exp(\varphi_{\mathrm{p}}/V_{\mathrm{th}})$ [29]. This completes the well-posedness analysis for the weak form of the Gummel map.

38.3.2 The Discretization of the Gummel Map

To provide the discrete counterpart of the Gummel map, we have first to define a discretization $\mathcal{T}_h = \{K\}$ of the computational domain. The choice of $\mathcal{T}_h$ is not a trivial task, in particular when dealing with complex phenomena such as the modeling of semiconductor devices. For this reason, we devote the whole Sect. 38.5 to furnish some hints for the generation of a good computational mesh.

Concerning the adopted discretization scheme, we focus on a FE approach as implemented in [30], although instances of FV discretizations are available in commercial codes (e.g., in [26, 31]). To this aim, we introduce the discrete space,

$$X_h^1(\Omega) = \left\{v_h \in C^0(\bar{\Omega}) : v_h|_K \in \mathbb{P}_1(K), \forall K \in \mathcal{T}_h\right\},$$

of the continuous piecewise linear finite elements, associated with the tessellation $\mathcal{T}_h$. Thus, the discrete form of the nonlinear Poisson problem reads: find $\delta\varphi_h \in V_h$, with $V_h = V \cap X_h^1(\Omega)$, such that

$$a_{\mathrm{NLP}}(\delta\varphi_h, v_h) = F_{\mathrm{NLP}}(v_h) \quad \forall v_h \in V_h, \tag{38.24}$$

where the bilinear and linear forms, $a_{\mathrm{NLP}}(\cdot,\cdot)$ and $F_{\mathrm{NLP}}(\cdot)$, are defined exactly as in (38.15). We now introduce a Lagrangian basis, $\{\psi_j\}_{j=1}^{N_h}$, of the space V_h, with $N_h = \dim(V_h)$. This allows us to expand the discrete solution $\delta\varphi_h$ to (38.24) in terms of this basis as

$$\delta\varphi_h(\mathbf{x}) = \sum_{j=1}^{N_h} \delta\varphi_j \, \psi_j(\mathbf{x}), \tag{38.25}$$

and to pick the test function v_h in (38.24) as the generic basis function ψ_i, with $i = 1, \ldots, N_h$, so that we reduce the discrete problem (38.24) to the N_h identities

$$\sum_{j=1}^{N_h} \delta\varphi_j \, a_{\mathrm{NLP}}(\psi_j, \psi_i) = F_{\mathrm{NLP}}(\psi_i) \quad \text{with } i = 1, \ldots, N_h.$$

These relations identify the algebraic counterpart of the NLP problem, namely, the linear system

$$\mathbf{A}_{\mathrm{NLP}} \delta\boldsymbol{\varphi} = \mathbf{b}_{\mathrm{NLP}}, \tag{38.26}$$

where the stiffness matrix, $\mathbf{A}_{\mathrm{NLP}} \in \mathbb{R}^{N_h \times N_h}$, and the right-hand side, $\mathbf{b}_{\mathrm{NLP}} \in \mathbb{R}^{N_h}$, are defined by

$$[\mathbf{A}_{\mathrm{NLP}}]_{ij} = a_{\mathrm{NLP}}(\psi_j, \psi_i), \quad [\mathbf{b}_{\mathrm{NLP}}]_i = F_{\mathrm{NLP}}(\psi_i),$$

respectively, with $i, j = 1, \ldots, N_h$, while vector $\delta\boldsymbol{\varphi} \in \mathbb{R}^{N_h}$ collects the (unknown) coefficients $\{\delta\varphi_j\}_{j=1}^{N_h}$ characterizing the discrete solution $\delta\varphi_h$.

In a similar way, we introduce the discrete space $W_h = W \cap X_h^1(\Omega_{\rm Si})$, with basis $\{\theta_k\}_{k=1}^{M_h}$ and $M_h = \dim(W_h)$, where we look for an approximation

$$n_h(\mathbf{x}) = \sum_{k=1}^{M_h} n_k\, \theta_k(\mathbf{x})$$

of the electron concentration. This leads to solve the linear system

$$\mathbf{A}_{\rm LEC}\mathbf{N} = \mathbf{b}_{\rm LEC}, \tag{38.27}$$

with $\mathbf{A}_{\rm LEC} \in \mathbb{R}^{M_h \times M_h}$ and $[\mathbf{A}_{\rm LEC}]_{lk} = a_{\rm LEC}(\theta_k, \theta_l)$, $\mathbf{b}_{\rm LEC} \in \mathbb{R}^{M_h}$ and $[\mathbf{b}_{\rm LEC}]_l = F_{\rm NLP}(\theta_l)$, $\mathbf{N} \in \mathbb{R}^{M_h}$ and $[\mathbf{N}]_k = n_k$, for $l, k = 1, \ldots, M_h$, and where $a_{\rm LEC}(\cdot,\cdot)$ and $F_{\rm NLP}(\cdot)$ are defined as in (38.23).

Finally, the same procedure is applied to the hole concentration, p, to yield the associated linear system,

$$\mathbf{A}_{\rm LHC}\mathbf{P} = \mathbf{b}_{\rm LHC}. \tag{38.28}$$

The solver adopted for systems (38.26), (38.26), and (38.28) has to be carefully chosen. We refer the reader to Sect. 38.6 for an overview on possible solvers.

Remark 38.1 The Slotboom variables play a crucial role when proving the well-posedness of the Gummel map, as checked in Sect. 38.3.1. Nevertheless, the practical implementation of the Gummel map moves from the linearized equations (38.12) and (38.13). These equations may be troublesome from a numerical viewpoint, due to the occurrence of spurious oscillations, in particular when the drift component is dominant. A possible remedy is represented by a (global) mesh refinement, although this choice generally leads to an unaffordable computational cost, especially for 3D simulations. As an alternative, one can resort to suitable stabilization schemes for the FE discretization, such as the upwind technique [32], the Scharfetter-Gummel method [33], or the edge-averaged FE (EAFE) approach [34]. The employment of ad hoc adapted meshes represents a third possible solution to numerical instabilities which still deserves to be properly investigated.

Remark 38.2 Gummel map is applied in a stationary setting. When dealing with an unsteady configuration, the NLP problem remains unchanged, while the linearized equations (38.12) and (38.13) are embedded into a time-advancing loop, after being properly modified to include the contributions due to the time discretization (we refer the interested reader to [5] for more details). In the context of semiconductor modeling, the approximation in time is generally performed via the TRBDF2 method [20], i.e., a composite scheme which combines the trapezoidal rule (TR) with the second-order backward difference formula (BDF2) in a two-step method, to contemporary benefit of the accuracy of TR and of the stability properties of the BDF2 scheme.

38.4 The Fully Coupled Newton Approach

This procedure represents an alternative to the Gummel map to tackle the DD model [35]. To simplify the discussion, we exemplify such an approach on the scaled system (38.7), after neglecting the time dependence analogously to what done in Sect. 38.3, so that we have

$$\begin{cases} \mathcal{F}_1(\varphi, n, p) = -\lambda^2 \nabla \cdot (\varepsilon \nabla \varphi) - p + n - \bar{N} = 0 & \text{in } \mathbf{Q} \\ \mathcal{F}_2(\varphi, n, p) = \nabla \cdot (\mu_n (n \nabla \varphi - \nabla n)) + R(\mathbf{E}, n, p) = 0 & \text{in } \mathbf{Q}_{\rm Si} \\ \mathcal{F}_3(\varphi, n, p) = -\nabla \cdot \big(\mu_p (p \nabla \varphi + \nabla p)\big) + R(\mathbf{E}, n, p) = 0 & \text{in } \mathbf{Q}_{\rm Si}, \end{cases} \tag{38.29}$$

where we have highlighted the dependence of the net recombination/generation rate term, R, on the electric field and on the electron and the hole concentrations. We rewrite (38.29) in a matrix form, as

$$\mathbf{F}(\mathbf{U}) = \mathbf{0}, \tag{38.30}$$

with $\mathbf{F}(\mathbf{U}) = [\mathcal{F}_1(\mathbf{U}), \mathcal{F}_2(\mathbf{U}), \mathcal{F}_3(\mathbf{U})]^{\rm T}$, $\mathbf{U} = [\varphi, n, p]^{\rm T}$ and $\mathbf{0} = [0, 0, 0]^{\rm T}$.

We resort to the standard Newton method to solve system (38.29). As remarked in Sect. 38.3, the Newton algorithm is here meant as a simple tool to manage the nonlinearity of the problem, while referring to Sect. 38.6.1 for details and improvements of the basic setting. The update of the generic $k_{\rm N}$ iteration is performed via the standard rule

$$\mathbf{U}^{(k_{\rm N}+1)} = \mathbf{U}^{(k_{\rm N})} + \delta\mathbf{U}^{(k_{\rm N})}, \tag{38.31}$$

with $\mathbf{U}^{(k_{\rm N})} = [\varphi^{(k_{\rm N})}, n^{(k_{\rm N})}, p^{(k_{\rm N})}]^{\rm T}$. The update $\delta\mathbf{U}^{(k_{\rm N})} = [\delta\varphi^{(k_{\rm N})}, \delta n^{(k_{\rm N})}, \delta p^{(k_{\rm N})}]^{\rm T}$ is the solution to the system

$$\mathbf{F}'(\mathbf{U}^{(k_{\rm N})})\delta\mathbf{U}^{(k_{\rm N})} = -\mathbf{F}(\mathbf{U}^{(k_{\rm N})}) \tag{38.32}$$

with $\mathbf{F}'(\mathbf{U}^{(k_{\rm N})})$ the Jacobian matrix associated with the $k_{\rm N}$-th iteration. The generic entry $[\mathbf{F}'(\mathbf{U}^{(k_{\rm N})})]_{ij}$ of the Jacobian matrix coincides with the Frèchet derivative of the i-th row of $\mathbf{F}(\mathbf{U})$ with respect to the j-th variable in $\mathbf{U}$. For instance, the first row of $\mathbf{F}'(\mathbf{U}^{(k_{\rm N})})$ involves the derivatives of $\mathcal{F}_1(\mathbf{U})$, being

$$[\mathbf{F}'(\mathbf{U}^{(k_{\rm N})})]_{11} = \frac{\partial \mathcal{F}_1(\mathbf{U}^{(k_{\rm N})})}{\partial \varphi}\delta\varphi^{(k_{\rm N})} = -\lambda^2 \nabla \cdot \left(\varepsilon \nabla \delta\varphi^{(k_{\rm N})}\right),$$

$$[\mathbf{F}'(\mathbf{U}^{(k_{\rm N})})]_{12} = \frac{\partial \mathcal{F}_1(\mathbf{U}^{(k_{\rm N})})}{\partial n}\delta n^{(k_{\rm N})} = \delta n^{(k_{\rm N})},$$

$$[\mathbf{F}'(\mathbf{U}^{(k_{\rm N})})]_{13} = \frac{\partial \mathcal{F}_1(\mathbf{U}^{(k_{\rm N})})}{\partial p}\delta p^{(k_{\rm N})} = -\delta p^{(k_{\rm N})}.$$

The dependence of the mobilities, μ_n, μ_p, and of the net recombination/generation rate term, R, on the unknowns φ, n, and p explicitly affects the definition of the Jacobian entries $[\mathbf{F}'(\mathbf{U}^{(k_N)})]_{ij}$, for $i = 2, 3$.

We proceed now by discretizing each block of the Jacobian matrix. Consistently with Sect. 38.3, we resort to a FE discretization. Thus, at the generic k_N-th iteration, we are led to solve the algebraic system

$$\begin{bmatrix} \mathbf{A}_{11}^{(k_N)} & \mathbf{A}_{12}^{(k_N)} & \mathbf{A}_{13}^{(k_N)} \\ \mathbf{A}_{21}^{(k_N)} & \mathbf{A}_{22}^{(k_N)} & \mathbf{A}_{23}^{(k_N)} \\ \mathbf{A}_{31}^{(k_N)} & \mathbf{A}_{32}^{(k_N)} & \mathbf{A}_{33}^{(k_N)} \end{bmatrix} \begin{bmatrix} \delta\varphi^{(k_N)} \\ \delta n^{(k_N)} \\ \delta p^{(k_N)} \end{bmatrix} = \begin{bmatrix} -\mathbf{F}_1(\mathbf{U}^{(k_N)}) \\ -\mathbf{F}_2(\mathbf{U}^{(k_N)}) \\ -\mathbf{F}_3(\mathbf{U}^{(k_N)}) \end{bmatrix}, \tag{38.33}$$

where $\mathbf{A}_{ij}^{(k_N)}$ is the matrix associated with the FE discretization of $[\mathbf{F}'(\mathbf{U}^{(k_N)})]_{ij}$, while $\mathbf{F}_i(\mathbf{U}^{(k_N)})$ denotes the discrete counterpart of $\mathcal{F}_i(\mathbf{U}^{(k_N)})$, for $i, j = 1, 2, 3$.

To simplify the computation, we consider a discretization of the domain Ω only, and we set to zero the values taken by n and p at the dofs in $\Omega \backslash \Omega_{Si}$. Thus, each block $\mathbf{A}_{ij}^{(k_N)}$ in (38.33) coincides with a matrix of order N_h, with N_h the dimension of the FE space employed to discretize the Poisson problem, consistently with the notation adopted in Sect. 38.3.2. Thus, the order of the system involved by the Newton iterations in the fully coupled approach is higher compared with the one used at the NLP step of the Gummel algorithm ($3N_h$ versus N_h), with a consequent larger demand in terms of computational burden.

The choice of the initial guess to start Newton iterations in (38.31) is far from being trivial. Very often, the Gummel map is employed for this purpose, in the spirit of a predictor-corrector technique [5]. The increment represents the criterion usually adopted to stop Newton algorithm (we refer to Sect. 38.6.1 for more details).

Moreover, we remark that the complex definition often assumed by mobilities μ_n and μ_p makes the Jacobian, in general, an ill-conditioned matrix. This demands to resort to suitable scaling and balancing techniques, in order to avoid possible problems related to the round-off error propagation.

Finally, considerations analogous to the ones in Remark 38.2 hold when generalizing the fully coupled approach to a time-dependent framework.

38.5 Grid Generation: The Basics

The choice of the computational mesh represents a challenging task. Actually, grid generation cannot be identified with a unique process for a fixed domain. In this direction, we quote the statement "Mesh is not a data but an unknown of the problem" which clearly frames the grid generation issue [36].

Given a domain Ω, the first step toward mesh generation consists in a suitable discretization of the boundary, $\partial\Omega$, of Ω. This process, known as *boundary rectification*, is straightforward in the presence of Cartesian geometries, while unavoidably introduces an error (known as geometric error) when dealing with domains characterized by a complex shape. Grid nodes are expected to sharply approximate the original geometry, so that boundary conditions can be accurately imposed.

Successively, the problem turns into the construction of a tessellation of the internal part, $\mathring{\Omega}$, of Ω. Given a polygonal domain $\Omega \subset \mathbb{R}^3$ (so that the geometric error is null), a grid (or a mesh or a tessellation), $\mathcal{T}_h = \{K\}$, of Ω is such that:

(H1) $\overline{\Omega} = \bigcup_{K \in \mathcal{T}_h} K$;

(H2) $\mathring{K} \neq \emptyset$, for any cell (or element) $K \in \mathcal{T}_h$;

(H3) $\mathring{K}_1 \cap \mathring{K}_2 = \emptyset$, for any cells $K_1, K_2 \in \mathcal{T}_h$ with $K_1 \neq K_2$,

$\overline{\omega}$ and $\mathring{\omega}$ denoting the closure and the internal part of the generic set ω, respectively. Moreover, a mesh satisfying the additional condition

(H4) if $\mathcal{I} = K_1 \cap K_2 \neq \emptyset$, then $\mathcal{I}$ coincides with a vertex, an edge or a face in $\mathcal{T}_h$, for any cells $K_1, K_2 \in \mathcal{T}_h$ with $K_1 \neq K_2$,

is classified as *conformal* mesh [28]. In the sequel, we focus on conformal tessellations of Ω. The *grid size* is identified by the number of cells (i.e., the mesh cardinality) or of cell vertices, while the *cell size* coincides with the maximum length of the cell edges. In particular, when dealing with standard finite elements, the size of the cell K coincides with the diameter $h_K = \max_{\mathbf{x},\mathbf{y} \in K} |\mathbf{x} - \mathbf{y}|$.

The adopted discretization as well as the PDE to be solved have a direct impact on the construction of the tessellation $\mathcal{T}_h$. Actually, the shape of the elements K depends on the adopted discretization, on the geometry of Ω and on the PDE at hand. In general, in a 3D setting, tetrahedra, hexahedra, or prisms are adopted. Historically, finite differences are associated with Cartesian grids, since such regular lattice structures allow one to easily identify the points to be used in the representation of derivatives. On the contrary, general pattern tessellations are well suited to fill arbitrarily shaped regions and are usually related to a FE discretization. More recently, polytopal meshes have been employed in several settings (see, e.g., [37]), this topic being beyond the goal of the present work.

Computational grids can be categorized driven by different criteria. In the sequel, we consider the standard classification into structured, unstructured, and hybrid meshes, before considering more sophisticated techniques to generate grids customized to the considered problem.

38.5.1 Structured Meshes

The basic difference between structured and unstructured meshes lies in the data structure which most appropriately describes the grid. In particular, in the structured case, the connectivity of the grid is implicitly taken into account, while for unstructured grids, it has to be explicitly described through an appropriate data structure (see Sect. 38.5.2). For instance, a structured 3D mesh of quadrilateral cells consists of a set of coordinates and connectivities that naturally map into the elements of a 3D matrix. Neighboring points in the mesh are associated with neighboring elements in the mesh matrix. Thus, a 3D array, $X(i, j, k)$, can be used to store the coordinates of the mesh vertices, indices i, j, and k describing the position of points along the x-, y-, and z-direction, respectively. The idea generalizes in a straightforward way to structured meshes with arbitrarily shaped cells.

Among structured grids, the simplest ones are the Cartesian meshes obtained by the intersection of the Cartesian coordinates in Ω and whose cells are rectangular parallelepipeds in 3D (or rectangles in 2D). The basic idea, characterizing all the structured mesh generation methods, starts from a partition of $\partial\Omega$, fitting the physical boundary of the domain the best way as possible, and successively extends the computational mesh from the boundary to the interior of Ω. Following [14,38,39], we can distinguish essentially among three different methods to generate the internal mesh:

(a) *Algebraic methods*: the interior points of the grid are computed through transfinite interpolation [40]. These methods are very simple. However, they can lead to a degenerate tessellation (with overlapped or reversed elements) when applied to complex geometries.
(b) *Differential methods*: these approaches are ideal to deal with domains characterized by arbitrary shapes. To generate the internal mesh in Ω, a partial differential equation problem is solved on a reference domain. Solution to this problem will be the vertex coordinates of the grid in Ω. In particular, elliptic equations are employed when these coordinates are specified on the whole boundary. Vice versa, when the coordinates are specified only on a part of $\partial\Omega$, parabolic or hyperbolic problems are solved. Elliptic equations are widely employed since they ensure several good properties to the grid (e.g., grid orthogonality close to the boundary, smoothness and equal spacing of the coordinate lines according to the boundary curvature, no propagation of boundary discontinuities inside Ω).
(c) *Variational methods*: the internal mesh generation is driven by the optimization of different grid properties (e.g., non-degeneracy, smoothness, uniformity, near-orthogonality) which are imposed through special functionals defined on a set of smooth discrete transformations. A compromise grid, with properties close the desired ones, is thus obtained for a suitable combination of these functionals.

As we will see in Sect. 38.5.5, alternative techniques can be used to generate structured grids, especially in the presence of complex problems, such as in the modeling of semiconductor devices.

38.5.2 Unstructured Meshes

Unstructured grids are considered as the most efficient solution to deal with realistic geometries and complex solution features. In such a case, points and connectivities do not have any global structure. On the one hand, this allows one to add and delete nodes and elements according to the geometry or the solution, making these meshes the ideal setting where to perform mesh adaptation. On the other hand, for any vertex in $\mathcal{T}_h$, the connection with other points must be defined explicitly via the connectivity matrix. Standard information provided by such an array are the number of vertices, the number of elements, the coordinates for each vertex, and the vertices identifying each cell, sometimes completed by data related to the boundary discretization (e.g., the number of the edges constituting $\partial\Omega$ together with the vertices associated with these edges). The connectivity matrix clearly plays a role when dealing with the numerical solution of PDEs, leading to an additional computational effort. Actually, numerical algorithms based on an unstructured grid topology are the most costly in terms of operations per time step and memory per grid point.

In contrast to the generation of structured grids, algorithms to build unstructured meshes are usually driven by geometric criteria. Among the most widespread techniques, we mention:

(d) *The octree approach*: spatial decomposition methods were applied to mesh generation about three decades ago [41]. An octree procedure (quadtree in 2D) yields a hierarchical tree structure which is used to simplify the geometry of the grid. First, Ω is enclosed in a bounding box (one cell, the root). The domain is then approximated with a union of disjoint, variably sized cells, representing a partition of the domain. In particular, each cell is analyzed and recursively subdivided so as to determine whether it conforms to a stopping criterion (e.g., based on the curvature of the domain or supplied by an error estimate). If not, it is subdivided into eight (four in 2D) cells of identical size. A covering up of a spatial region enclosing the root is thus obtained. Each cell is finally further decomposed into tetrahedra, leading to a suitable unstructured mesh of the domain Ω. The

main drawback of the octree approach is the inability to match a prescribed boundary discretization, the grid on the surface being identified by the intersection of the irregular volume cells with the surface itself.

(e) *The Delaunay criterion*: (The basic geometric concept behind this approach has been discussed already by Dirichlet in 1850 [42].) this approach connects a specified set of nodes to form tetrahedra so that the circumsphere through the four vertices of a tetrahedral cell does not contain any other point (in-sphere (in-circle in 2D) criterion). For a given set of points, there exists a unique Delaunay triangulation [43]. The main limit of this technique is that it does not preserve the boundary integrity. To recover such a property, improvements of the basic approach have been proposed, such as the constrained and the conforming Delaunay triangulations (see, e.g., [44, 45]).

(f) *The advancing front method*: this procedure does not exploit geometric criteria. The main idea is to construct the mesh, element by element, starting from an initial front which coincides with a discretization of the domain boundary. An entity of the front is selected and a mesh element is generated by connecting this entity to an existing or to a newly created point in order to form a new cell. For each new element, the front is updated so that it dynamically evolves. The process stops when the domain is entirely meshed [46, 47]. In general, the marching direction for the front takes into account the normals to the surface. Limits of advancing front methods include the selection of the front entity and of the marching step size and the capability to prevent the front from intersecting.

The techniques above are often combined to overcome, for instance, the limits exhibited by approaches (d)–(e) in managing surfaces and interfaces. A possibility is to resort to the advancing front on the external parts of the domain and to apply the Delaunay criterion to generate the internal mesh (see Sect. 38.5.5). Moreover, we remark that approaches (d)–(f) can be adopted to generate also structured meshes. Finally, it is very recurrent to apply, after generation, a smoothing of the unstructured mesh (e.g., by a Laplacian-type smoother) in order to enhance the quality of the mesh [11, 13, 14].

38.5.3 Hybrid Meshes

Hybrid meshes combine structured with unstructured grids [48, 49], meshes with elements characterized by a different shape (triangles/tetrahedra with squares/parallelepipeds), or grids generated via different approaches (e.g., by alternating an octree with a Delaunay criterion, see Sect. 38.5.5). This combination is meant to benefit of the good properties characterizing the different grid types, for instance, the computational efficiency of structured meshes and the geometric flexibility of unstructured tessellations. In general, the advantages of one approach are the disadvantages of the other one. Hybrid meshes find a large employment when dealing with phenomena where the presence of boundary layers demands for ad hoc meshes. This occurs, for instance, when modeling semiconductor devices in correspondence with Si/SiO2 interfaces [50–52], or high Reynolds number turbulent flows with immersed bodies in aero- and hydro-dynamics [53, 54]. In particular, when unstructured grids are used, boundary layers require very small spacing, resulting either in very long skewed cells or in a prohibitively large number of small cells. The practical solution implemented in a structured/unstructured hybrid mesh resorts to very thin structured grids along layers immersed into an unstructured grid. Anisotropic meshes represent an alternative smart solution to manage boundary or internal layers (see Remark 38.4).

38.5.4 Advanced Techniques: Mesh Adaptation

The choice of ad hoc meshes can significantly enhance the accuracy of the computed solution together with the computational cost and time, especially in the modeling of complex systems. The generation of tessellations customized to the problem at hand represents the main goal of mesh adaptation. The idea is to cluster the grid points in regions where solution exhibits a problematic trend, thus providing a local finer resolution. Actually, without grid clustering, some important features are missed, and the accuracy of the solution degrades. The benefit led by an adapted mesh can be in terms of accuracy, for a fixed size of the mesh, or vice versa, in terms of mesh size, for a desired accuracy on the discrete solution. The alternative to an adapted grid is a uniform refinement in the whole domain which, however, turns out to be very costly, especially for multidimensional computations.

Two are the main ingredients required to adapt a computational mesh, namely, an estimation for the discretization error to identify the regions where the mesh has to be modified and a procedure to modify the grid starting from this information. We will focus on these two topics in the next sections, separately.

Evaluation of the Discretization Error

Typically, the areas of the domain where a high resolution is demanded (e.g., the location of the junction breakdown in semiconductor simulations) are not known a priori. This issue is generally accomplished by defining an error quantifier for the problem at hand. There exists an extensive choice of criteria to quantify the discretization error in the different areas

of Ω, which are mainly categorized into heuristic information and rigorous mathematical tools. In the former case, we deal with an *error indicator*, $\boldsymbol{\mathcal{I}}$. Standard examples include the comparison between the computational stencils involved by the approximation of different order for the differential operators, the comparison of the same derivatives on different (finer and coarser) meshes, the Hessian or the gradient of the numerical solution, physical features (e.g., stagnation points, vortices, layers, carrier generation, and multiplication), or geometric information (e.g., corners, interfaces) relevant for the considered problem. More rigorous approaches lead to define an *error estimator*, $\boldsymbol{\mathcal{S}}$, which can be classified as a priori or a posteriori. The common goal is to provide a control for a certain norm, $\|\cdot\|_*$, of the discretization error.

To simplify the exposition, we denote the (weak) solution to the PDE problem of interest by u and the corresponding (e.g., FE) discretization by u_h. An estimator for the discretization error, $e_h = u - u_h$, takes the form

$$\|e_h\|_* \leq C\,\boldsymbol{\mathcal{S}} = C\left(\sum_{K\in\mathcal{T}_h} \eta_K^2\right)^{1/2}, \tag{38.34}$$

with $\boldsymbol{\mathcal{S}}$ and η_K the global and the local error estimator, respectively, and $C > 0$ a constant. In more detail, an a priori error analysis leads to a local estimator of the form

$$\eta_K = \eta_K(u, h_K) = h_K^{\alpha}\,\|u|_K\|_{\beta},$$

while, with an a posteriori error analysis, we have

$$\eta_K = \eta_K(u_h, h_K) = h_K^{\gamma}\,\|R(u_h|_K)\|_{\delta},$$

for certain powers, α and γ, of the cell diameter, h_K, and for suitable norms, $\|\cdot\|_{\beta}$ and $\|\cdot\|_{\delta}$, where $R(u_h|_K)$ denotes a quantity (e.g., the residual) depending on the discrete solution. The elementwise structure of the global estimator $\boldsymbol{\mathcal{S}}$ is crucial in order to localize the areas of the domain where the approximation has to be improved (i.e., the elements characterized by the highest estimated error) and vice versa. The same property is demanded for an error indicator.

A posteriori error estimators are directly computable in contrast to a priori estimates which, in general, require to replace u with a computable quantity, before being employed to drive mesh adaptation. Standard examples of a priori results are the interpolation and the convergence estimates. Concerning the a posteriori error estimators, they differ essentially for the controlled quantity and can be distinguished into the following categories [55–57]:

(g) *Residual-based error estimators*: the norm $\|\cdot\|_*$ in (38.34) coincides with the $H^1(\Omega)$- or with the $L^2(\Omega)$-norm, while the local estimator depends on the internal and on the boundary residuals associated with u_h in K. The main drawback for these estimators is that the constant C in (38.34) is, in general, not explicitly computable;

(h) *Goal-oriented error estimators*: the quantity controlled now coincides with an error functional, $J(u - u_h)$, where $J(\cdot)$ models a goal quantity of interest [56], for instance, the convective or diffusive flux across a portion of the boundary, the current density in a semiconductor device, the lift or the drag in fluid dynamic applications, pointwise values, and the stress of an elastic body. The control of $J(u)$ via the computable quantity $J(u_h)$ is achieved by solving an auxiliary problem, the dual problem, whose source term is strictly related to J. The extra computational cost associated with the dual problem (in particular, in an unsteady setting) represents the main limit of a goal-oriented approach;

(j) *Recovery-based error estimators*: these estimators are widely employed in practice because of the good properties they exhibit, e.g., the independence from the problem and from the adopted discretization, the computational cheapness, and the implementation easiness [58,59]. The $H^1(\Omega)$-seminorm replaces norm $\|\cdot\|_*$ in (38.34), whereas the local estimator coincides with the recovered error, $\|\nabla^* u_h - \nabla u_h\|^2_{L^2(K)}$, where $\nabla^* u_h$ denotes the recovered gradient, namely, an approximation for ∇u, in general, more accurate than the discrete gradient, ∇u_h [60]. The main weak point of these estimators is the limited theoretical investigation;

(k) *Local error estimators*: this analysis is based on the solution of local problems. The challenge is the choice of the corresponding boundary conditions [55].

The Adaptive Procedure

We exemplify a possible procedure to commute an error estimator $\boldsymbol{\mathcal{S}}$ (or, analogously, an error indicator, $\boldsymbol{\mathcal{I}}$) into an adapted mesh. Our goal is to ensure a user-defined accuracy, TOL, on the error (i.e., on the error estimator) so that $\|e_h\|_* \leq C\,\boldsymbol{\mathcal{S}} \leq$ TOL, and to equidistribute the error across the grid cells so that $\eta_K \leq \mathrm{TOL}/\#(\boldsymbol{\mathcal{T}}_h)$, with $\#(\boldsymbol{\mathcal{T}}_h)$ the mesh cardinality. At each step, $i \geq 0$, starting from a background grid, $\boldsymbol{\mathcal{T}}_h^{(0)}$:

1. We compute the discrete solution u_h and the corresponding error estimator $\boldsymbol{\mathcal{S}}$ on the actual mesh, $\boldsymbol{\mathcal{T}}_h^{(i)}$;
2. We identify the operations to be performed on $\boldsymbol{\mathcal{T}}_h^{(i)}$;
3. We generate the new mesh $\boldsymbol{\mathcal{T}}_h^{(i+1)}$.

Notice that the initial mesh cannot be too coarse, so that $\boldsymbol{\mathcal{S}}$ has enough information about the local accuracy of the current approximation. The stopping criterion for the adaptive

procedure coincides with the check on the accuracy to be equidistributed on the mesh, sometimes combined with additional controls (e.g., on the stagnation of mesh cardinality between consecutive adaptive loops [61]).

Let us focus now on step 2. We classify the possible different operations into three main classes:

(l) *Mesh refinement/coarsening*: all the cells K where the local error estimator is larger than a certain threshold, i.e., such that

$$\eta_K \geq \frac{C_1 \mathrm{TOL}}{\sqrt{\#(\mathcal{T}_h^{(i)})}}, \tag{38.35}$$

are marked for refinement. Vice versa, cells where the local error estimator is smaller than a certain threshold, i.e., such that

$$\eta_K < \frac{C_2 \mathrm{TOL}}{\sqrt{\#(\mathcal{T}_h^{(i)})}}, \tag{38.36}$$

are marked for coarsening. Inequalities (38.35) and (38.36) are meant to ensure the desired accuracy, TOL, together with the error equidistribution. Constants C_1 (>1) and C_2 (<1) confine mesh refinement and coarsening to the cells characterized by the largest and the smallest (estimated) error, respectively.

Elements marked for refinement are then subdivided into 2, 3, or 4 parts, according to a green, blue, or red refinement, respectively [57]. These techniques can be combined, depending on whether one is interested in conforming or non-conforming meshes.

Refinement of unstructured grids is readily implemented, whereas it is not so straightforward on structured grids, especially when dealing with conforming meshes. Indeed, the addition of new elements breaks the regular data structure characterizing structured meshes, due to the creation of vertices with a different number of connections to the neighboring points.When dealing with non-conforming structured meshes, hanging nodes are allowed during the refinement phase, and this requires modifications to the solver. Conversely, the addition of new cells in an unstructured mesh involves only a local reconnection of the elements, with a consequent update of the connectivity matrix, and the original solver can be preserved.

Unlike refinement, coarsening does not apply to a single cell. In particular, if all the cells belonging to the patch of elements, $\Delta_{\mathbf{v}} = \{K \in \mathcal{T}_h^{(i)} : K \ni \mathbf{v}\}$, associated with a node, $\mathbf{v}$, are marked for coarsening, vertex $\mathbf{v}$ is removed and the area covered by $\Delta_{\mathbf{v}}$ is remeshed.

From a practical point of view, an efficient adaptive procedure alternates mesh refinement and coarsening with regularization operations, such as edge swapping and node smoothing (see, e.g., [62]), to improve the mesh quality (see Remark 38.3);

(m) *Node movement*: the equidistribution of the desired accuracy is pursued through the migration of the mesh vertices from regions characterized by a small error to areas with a large error, so that the number of vertices remains fixed. Algorithms to move points are, in general, driven by a weight function which combines an error estimator with desired geometric properties (e.g., smoothness, orthogonality). Node movement can be applied both to structured and unstructured grids [15];

(n) *Remeshing*: a discrete function is derived from the error estimator/indicator computed on $\mathcal{T}_h^{(i)}$, to predict the element-size spacing $\mathcal{M}$ (i.e., the *metric* [12]), which identifies the new mesh $\mathcal{T}_h^{(i+1)}$. In more detail, function $\mathcal{M}$ is defined in Ω and specifies the size (for isotropic meshes) together with the directional features (for anisotropic meshes) that must be conformed to by the mesh elements (see Remark 38.4). In practice, metric $\mathcal{M}$ is assigned at the vertices of the background mesh, $\mathcal{T}_h^{(i)}$, to predict the new grid, $\mathcal{T}_h^{(i+1)}$. The derivation of $\mathcal{M}$ usually involves the resolution of local constrained optimization problems, thus leading to a computational overhead, especially for 3D configurations. However, impressive demonstrations of the effectiveness of remeshing are available in the literature, primarily on unstructured grids (see, for instance, [16,63,64]).

Mesh refinement/coarsening, node movement, and remeshing can be distinguished into global and local procedures. Remeshing is a global approach since, at each iteration, it reconstructs the whole mesh. On the contrary, mesh refinement/coarsening and node movement are local procedures, since they usually involve only a confined portion of the mesh. The adaptivity performed according to (l) and (n) is called *h-adaptivity*, while adaptivity driven by node movement (m) is called *r-adaptivity* (actually, there exists a third kind of adaptivity, the *p-adaptivity*, where the solution is improved by locally tuning the accuracy of the discretization scheme [65]).

The choice among the adaptive techniques in (l)–(n) is always affected by the available mesh generator. Mesh generators usually include local modification procedures, while only few provide metric-based routines. Finally, approaches (l)–(n) can be combined to maximize the benefits led by the individual procedures.

Remark 38.3 (Mesh Quality) There exist different ways to certify the quality of an adapted grid (see, e.g., [11,66,67]). A first possibility is to introduce geometric quantities which characterize the shape of the cells [68]. When dealing with a finite element approximation, a good mesh is the one which, for a certain mesh size, leads to the best possible numerical

accuracy or, vice versa, for a certain accuracy, minimizes the mesh cardinality. When dealing with an element-size spacing $\mathcal{M}$, the good quality of a mesh is ensured by making the length of each side in $\mathcal{T}_h^{(i+1)}$ the closest as possible to unit with respect to $\mathcal{M}$, since a triangle with unit edge lengths is necessarily a good quality triangle [12].

Remark 38.4 (Isotropic Versus Anisotropic Meshes) Meshes can be classified also into isotropic and anisotropic. In the former case, elements share the same length in all the directions and the cell diameter, h_K, is the only information demanded to characterize the grid. On the contrary, anisotropic meshes admit deformed cells, so that the elements are uniquely identified by supplying the shape and the orientation of K, in addition to the size h_K. The cell deformation can be quantified, for instance, through the aspect ratio (i.e., the ratio of the longest to shortest edge) or the angles between the cell edges, whereas the grid deformation is measured by the change rate of the geometric features across adjacent cells.

With reference to Sect. 38.5.2, Delaunay triangulations are, by construction, isotropic. The advancing front method can generate deformed elements, although of low quality. Actually, anisotropic meshes are generated via specific procedures, e.g., via a map that changes an isotropic reference cell into a distorted element in the physical space [69, 70]. The demand for extra information to characterize anisotropic meshes turns into a more involved error analysis as well as into a more complex definition of the metric $\mathcal{M}$. Moreover, stretched cells lead often to ill-conditioned systems, for instance, when dealing with a FE discretization (see [68]). Despite these drawbacks, anisotropic meshes have been successfully employed in several contexts. The computational advantages obtained by replacing isotropic with anisotropic meshes have been numerically checked, in particular when modeling phenomena with intrinsic directionalities (e.g., boundary or internal layers, shocks, stagnation points, vortices) such as in fluid dynamics, combustion, solid mechanics, and wave propagation [61, 63, 71–80].

38.5.5 Meshes for Semiconductor Devices

Three-dimensional mesh generation for semiconductor device simulations still leaves room for much innovation due to the complex phenomena often involved in such a modeling (e.g., silicon crystallization, ion precipitation, stoichiometry variation). Difficulties are experienced dealing with the boundaries and the interfaces (for instance, between semiconductor materials and dielectric or a cross p-n junction), in particular to strike a balance between a sharp fitting of these features and an optimal mesh density distribution [81].

Among the available techniques, we mention the Cartesian-based approach employed by the mesh generator OMEGA, which implements octree decomposition techniques, improved with the possibility to tessellate the Cartesian cells into Delaunay tetrahedra and more anisotropic cells [82].

Advancing front methods are sometimes used since they ensure good point placement properties. Indeed, elements are grown from the boundary so that they are well aligned with it. Some attempts are available in two dimensions [83–85], while it remains an issue how to effectively apply such methods to the complexity of a three-dimensional semiconductor device. An alternative approach in three dimensions is provided by hybrid meshes [50, 51]. In particular, we cite the hybrid mesh generator MESHise [52], which constitutes a further development of OMEGA.

Delaunay triangulations represent another viable choice for semiconductor simulations [86–89]. Also for this procedure, the most challenging context remains the three-dimensional case due to the difficulty in effectively integrating boundaries into a three-dimensional Delaunay mesh. Specific algorithms are demanded to generate an unstructured Delaunay mesh coherent with boundaries and interfaces, for instance, when dealing with an extremely thin oxide layer on top of a comparatively big silicon block.

Finally, some examples of adapted meshes for semiconductor devices are available in the literature, for Raviart-Thomas mixed finite elements [90] and in the context of a finite difference or a finite element discretization (see, e.g., [91–93]). Moreover, we refer to [94] for a first attempt of anisotropic mesh adaptation. Here, the authors apply the DD model to a p-n junction diode device and propose a goal-oriented error estimator to drive an anisotropic adaptation of the mesh via a metric-based procedure.

Among the mesh generators which are currently most widely employed in the modeling of semiconductor devices, we mention Gmsh, an open-source 3D finite element mesh generator with a built-in CAD engine and post-processor [95]; ViennaMesh, a mesh library which covers both mesh generation and adaptation in 2D and 3D [96]; Victory Mesh by Silvaco, to mesh and refine both existing and new 2D and 3D TCAD structures [97]; and Synopsys a tool suite which allows constructing device structures, meshing, simulation, visualization of electrical characteristics, plotting of various curves, and extraction of performance parameters [26]. In the examples provided below, we resort to the last mesh generator. This choice is motivated by the fact that Synopsys is one of the most widely used mesh suites for industrial applications. Moreover, it is compatible with the solver adopted in the numerical assessment (see Sect. 38.7).

Synopsys includes three mesh generators, i.e., Mesh, Noffset3D, and Sentaurus Mesh. In particular, we will employ Sentaurus Mesh to build an example of structured

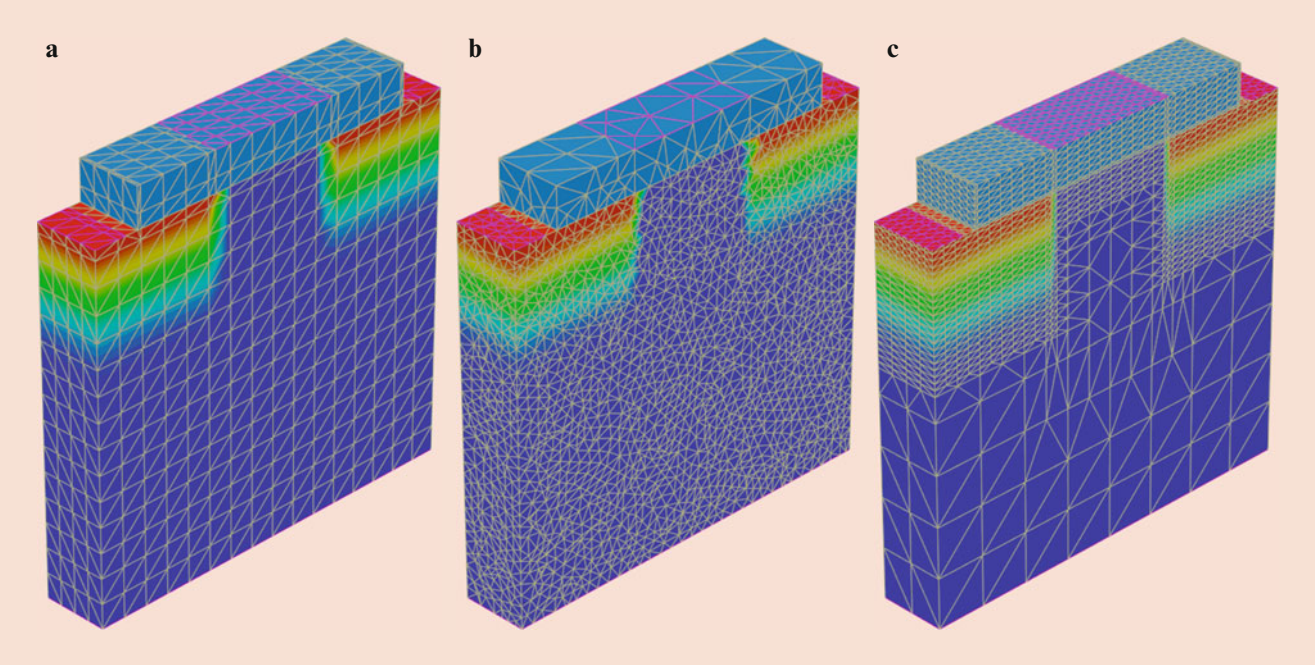

Fig. 38.3 n-MOSFET device: example of (**a**) structured, (**b**) unstructured, and (**c**) hybrid tetrahedral mesh (the colormap refers to the doping)

and hybrid mesh and Noffset3D to generate an unstructured grid. Sentaurus Mesh incorporates a tensor product mesh generator to produce hexahedral (or rectangular) elements and an axis-aligned grid generator where the octree (quadtree) technique is adopted to discretize the device domain via tetrahedra (triangles), in combination with the Delaunay criterion, which ensures high-quality conforming grids. Sentaurus Mesh performs also local mesh refinements, by using the doping or specific information prescribed by the user (see the example below). Noffset3D is a mesh generator that employs triangles and rectangles in 2D and tetrahedra in 3D to provide a fully unstructured tessellation of the computational domain. Noffset3D uses an advancing front method starting from specified surfaces and interfaces, to create anisotropic layers of elements, and fills the remainder of the domain with an isotropic mesh, by resorting to different meshing algorithms which can be arbitrarily selected by the user. Except for some special cases, the default series of algorithms produces very good results in terms of mesh quality. Moreover, meshes can be adapted to the geometry of a device by creating layers along certain interfaces or to suit other data such as refining p-n junctions.

Now, we focus on a specific semiconductor device, and we provide some examples of possible grids. We consider an n-type MOSFET (n-MOSFET), characterized by a constant p-type (Boron) channel doping of 10^{17} (cm^{-3}), and by symmetric source/drain junctions characterized by a Gaussian n-type (Arsenic) profile, with a peak value equal to 10^{18} (cm^3) at the top surface of Ω_{Si} (see Fig. 38.1 for a sketch). The gate is of n-type, with a thickness of 30 (nm) and a length of 100 (nm).

For this device, we show an example of structured mesh in Fig. 38.3a, which consists of 1560 vertices and 6600 cells. The grid has been generated with Sentaurus Mesh, which resorts to an octree recursive space decomposition technique to discretize the device domain. As previously remarked, methods devoted to unstructured meshes can be adopted also to generate structured tessellations.

For the same device, in Fig. 38.3b we show an example of unstructured mesh generated by Noffset3D. Two of the techniques in Sect. 38.5.2 are here combined to yield the desired grid, namely, the advancing front method to track the external surface and the interfaces and the Delaunay criterion to fill the internal part of the domain. The grid consists of 65,838 vertices and 12,240 tetrahedra.

Figure 38.3c shows an example of tetrahedral hybrid mesh for the n-MOSFET device, where hybrid is meant as a combination of different techniques to generate the tessellation of the domain. The grid consists of 30,866 vertices and 6442 elements. It has been generated with Sentaurus Mesh, which enriches the standard octree algorithm, here employed with two different step sizes, with a Delaunay criterion. The two different types of mesh can be easily distinguished in the hybrid grid.

It is also interesting to compare the three meshes in Fig. 38.3 in terms of vertices and elements.

We consider now the advanced techniques in Sect. 38.5.4. In Fig. 38.4, we provide two examples of adapted mesh for

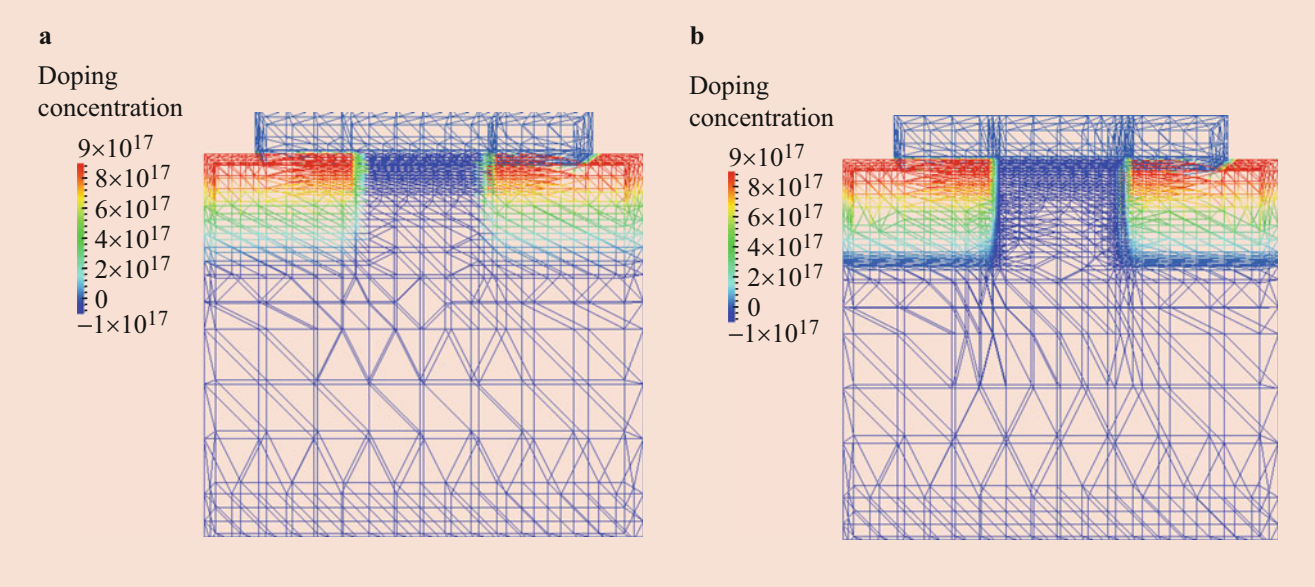

Fig. 38.4 n-MOSFET device: adapted mesh driven (**a**) by geometric and (**b**) by geometric plus physical information

the n-MOSFET device. The two grids are generated with Sentaurus Mesh, driven by heuristic considerations and by resorting to a mesh refinement/coarsening procedure. The mesh on the left consists of 2389 vertices and 10,284 cells. It has been obtained starting from the structured mesh in Fig. 38.3a and following a geometric indicator, namely, by refining the region under the channel where the inversion layer is induced by the bias applied to the gate. The mesh on the right, constituted by 4438 vertices and 19,888 tetrahedra, is obtained by enriching the geometric indicator with the value of the gradient of the doping profile. This allows us to better define the source and drain junctions inside the n-MOSFET bulk region. The twofold source of information driving mesh adaptation justifies the finer mesh, and it makes us expect a higher accuracy in terms of device modeling (see Sect. 38.7).

38.6 Algebraic Solvers

The numerical procedures introduced in the previous sections lead to solve both linear and nonlinear systems of equations. We discuss here suitable solvers for these systems, with a particular emphasis on a large-scale setting. In particular, to make the discussion more general, we do not confine the presentation to the specific systems associated with the DD model, and we consider a generic framework.

38.6.1 Nonlinear Solvers

Both the approaches in Sects. 38.3 and 38.4 involve the Newton algorithm to manage a nonlinearity. We generically denote a nonlinear system of equations by

$$F(\boldsymbol{U}) = \boldsymbol{0}, \tag{38.37}$$

with $F : \mathbb{R}^N \to \mathbb{R}^N$, $\boldsymbol{U} \in \mathbb{R}^N$, and $\boldsymbol{0} = [0, \ldots, 0]^{\mathrm{T}} \in \mathbb{R}^N$.

Several iterative procedures are available to solve system (38.37), which essentially differ for the linearized model employed at each iteration. Among the others, we mention Newton-based and quasi-Newton methods [98]. In the context of semiconductor modeling, it is common to resort to Newton-based schemes. The standard Newton method applied to (38.37) employs the linear model

$$F'(\boldsymbol{U}_{\mathtt{k}})(\boldsymbol{U} - \boldsymbol{U}_{\mathtt{k}}) + F(\boldsymbol{U}_{\mathtt{k}}) = 0, \tag{38.38}$$

with $\boldsymbol{U}_{\mathtt{k}}$ the $\mathtt{k}$-th iteration and with $F'(\boldsymbol{U}_{\mathtt{k}}) \in \mathbb{R}^{N\times N}$ the associated Jacobian matrix. The corresponding algorithm can be thus itemized:

Algorithm 38.1 Newton method

Input : $\boldsymbol{U}_0 \in \mathbb{R}^N$, $\mathtt{TOL} < 1$, $\mathtt{ESTIM}_0 > \mathtt{TOL}$, $\mathtt{kmax}$.

1: Set: $\mathtt{k} = 0$;
2: **while** $\mathtt{ESTIM}_{\mathtt{k}} > \mathtt{TOL}$ & $\mathtt{k} < \mathtt{kmax}$ **do**
3: Solve $F'(\boldsymbol{U}_{\mathtt{k}})\Delta\boldsymbol{U}_{\mathtt{k}} = -F(\boldsymbol{U}_{\mathtt{k}})$;
4: Compute $\boldsymbol{U}_{\mathtt{k}+1} = \boldsymbol{U}_{\mathtt{k}} + \Delta\boldsymbol{U}_{\mathtt{k}}$;
5: Compute $\mathtt{ESTIM}_{\mathtt{k}}$;
6: $\mathtt{k} = \mathtt{k}+1$;
7: **end while**

The termination of the iterative process is based on the estimator $\mathtt{ESTIM}_{\mathtt{k}}$ combined with a control on the maximum number, $\mathtt{kmax}$, of the iterations. The estimator typically coincides with the residual, $F(\boldsymbol{U}_{\mathtt{k}})$, and/or with the difference $\boldsymbol{U}_{\mathtt{k}+1} - \boldsymbol{U}_{\mathtt{k}}$ between two consecutive iterations. For instance, standard stopping criteria are

$$\|F(\boldsymbol{U}_{\mathtt{k}})\|_\infty \leq \tau_1 + \tau_2 \|F(\boldsymbol{U}_0)\|_\infty, \tag{38.39}$$

and

$$\|\boldsymbol{U}_{\mathtt{k}+1} - \boldsymbol{U}_{\mathtt{k}}\|_\infty \leq \tau_1 + \tau_2 \|\boldsymbol{U}_{\mathtt{k}}\|_\infty, \tag{38.40}$$

with $\|\cdot\|_\infty$ the infinite norm and where τ_1 and τ_2 are fixed tolerances on the absolute and on the relative error, respectively. The employment of the infinite norm is motivated by the large dimension of the vectors involved. Alternatively, if we resort to the Euclidean norm, it is advisable to properly scale the norms in (38.39) and (38.40) (e.g., by $1/\sqrt{N}$) and to rewrite the stopping criteria in terms of these scaled quantities.

Newton method is locally convergent, namely, the sequence $\{\boldsymbol{U}_{\mathtt{k}}\}$ converges to the solution $\boldsymbol{U}^*$ of (38.37) if the initial guess $\boldsymbol{U}_0$ is sufficiently close to such a solution. To enhance the convergence, Newton-based methods can be embedded into a *globalization* strategy, i.e., a procedure such that, for any initial value, either $\|F(\boldsymbol{U}_{\mathtt{k}})\|$ converges to zero or the iteration $\boldsymbol{U}_{\mathtt{k}}$ fails to converge and the ways which the sequence can fail to converge are well understood [99]. A possible globalization strategy is represented by a line search along the Newton step, $\Delta\boldsymbol{U}_{\mathtt{k}}$, leading to the so-called Damped Newton method (or Newton method with line search) [98–100]. This globalization strategy relies on the minimization problem

$$\min_{\mathbf{U}\in\mathbb{R}^N} \psi(\boldsymbol{U}) \quad \text{with } \psi(\boldsymbol{U}) = \|F(\boldsymbol{U})\|_2$$

and $\|\cdot\|_2$ the Euclidean norm and, given $\boldsymbol{U}_{\mathtt{k}}$ and $\Delta\boldsymbol{U}_{\mathtt{k}}$, computes the new iteration as

$$\boldsymbol{U}_{\mathtt{k}+1} = \boldsymbol{U}_{\mathtt{k}} + \lambda\, \Delta\boldsymbol{U}_{\mathtt{k}},$$

with $0 < \lambda \leq 1$ and $\psi(\boldsymbol{U}_{\mathtt{k}+1}) < \psi(\boldsymbol{U}_{\mathtt{k}})$. The existence of λ is guaranteed since the Newton step is a descent direction for ψ at $\boldsymbol{U}_{\mathtt{k}}$ (see [99, Proposition 3.3]). Typically, the step length λ is chosen via a backtracking approach. The idea is to start with $\lambda = 1$ and then to backtrack it, i.e., to reduce λ until $\|F\|_2$ is sufficiently reduced. A possible implementation of the damped Newton method is provided in the following

Algorithm 38.2 Damped Newton method

Input : $\boldsymbol{U}_0 \in \mathbb{R}^N$, $\mathtt{TOL} < 1$, $\mathtt{ESTIM}_0 > \mathtt{TOL}$, $\mathtt{kmax}$, α, $\sigma \in (0, 1)$

1: Set: $\mathtt{k} = 0$;
2: **while** $\mathtt{ESTIM}_{\mathtt{k}} > \mathtt{TOL}$ & $\mathtt{k} < \mathtt{kmax}$ **do**
3: Solve $F'(\boldsymbol{U}_{\mathtt{k}})\Delta\boldsymbol{U}_{\mathtt{k}} = -F(\boldsymbol{U}_{\mathtt{k}})$;
4: Set: $\lambda = 1$;
5: **while** $\|F(\boldsymbol{U}_{\mathtt{k}} + \lambda\, \Delta\boldsymbol{U}_{\mathtt{k}})\|_2 > (1 - \alpha\lambda)\|F(\boldsymbol{U}_{\mathtt{k}})\|_2$ **do**
6: Compute $\lambda = \sigma\lambda$;
7: **end while**
8: Compute $\boldsymbol{U}_{\mathtt{k}+1} = \boldsymbol{U}_{\mathtt{k}} + \lambda\Delta\boldsymbol{U}_{\mathtt{k}}$;
9: Compute $\mathtt{ESTIM}_{\mathtt{k}}$;
10: $\mathtt{k} = \mathtt{k}+1$;
11: **end while**

We remark that the backtracking phase (lines 5–6) has a finite termination [100]. Parameter α is known as Armijo constant, and it is usually set to 10^{-4}, while typical values for σ are 0.5 and 0.1 [99]. Concerning the choice of λ, the simple update in line 6 allows one to progressively reduce λ by a fixed factor. Alternatively, λ is selected by using a polynomial model for the scalar function $\psi(\boldsymbol{U}_{\mathtt{k}} + \lambda\Delta\boldsymbol{U}_{\mathtt{k}})$ and looking for the minimum of this polynomial as the next step length [99,100]. Finally, we cite the Bank-Rose strategy, where λ is first set to one and then updated as $\lambda = 1/(1 + \rho\|F(\boldsymbol{U}_{\mathtt{k}})\|_2)$, $\rho \geq 1$ being progressively increased to fulfill a sufficient reduction on ψ [101].

The main computational issue characterizing Newton method is represented by the solution, at each iteration, of the linear system in line 3 of both Algorithms 38.1 and 38.2. A direct solver is generally employed when dealing with small or medium size systems or with large dimension problems characterized by a sparse Jacobian matrix, whereas, in case of huge dimension systems, it is advisable to resort to an iterative linear solver. When the linear systems are solved approximately and in some unspecified manner, the resulting procedure is denoted by inexact Newton method [102], and it can be itemized as follows:

Algorithm 38.3 Inexact Newton method

Input : $\boldsymbol{U}_0 \in \mathbb{R}^N$, $\eta_{\max} \in (0, 1)$, $\mathtt{TOL} < 1$, $\mathtt{ESTIM}_0 > \mathtt{TOL}$, $\mathtt{kmax}$

1: Set: $\mathtt{k} = 0$;
2: **while** $\mathtt{ESTIM}_{\mathtt{k}} > \mathtt{TOL}$ & $\mathtt{k} < \mathtt{kmax}$ **do**
3: Choose $\eta_{\mathtt{k}} \in [0, \eta_{\max}]$;
4: Find $\Delta\boldsymbol{U}_{\mathtt{k}}$ such that $\|F(\boldsymbol{U}_{\mathtt{k}}) + F'(\boldsymbol{U}_{\mathtt{k}})\Delta\boldsymbol{U}_{\mathtt{k}}\|_2 \leq \eta_{\mathtt{k}}\|F(\boldsymbol{U}_{\mathtt{k}})\|_2$;
5: Compute $\boldsymbol{U}_{\mathtt{k}+1} = \boldsymbol{U}_{\mathtt{k}} + \Delta\boldsymbol{U}_{\mathtt{k}}$;
6: Compute $\mathtt{ESTIM}_{\mathtt{k}}$;
7: $\mathtt{k} = \mathtt{k}+1$;
8: **end while**

The so-called forcing term, $\eta_{\mathtt{k}}$, is employed to control the level of accuracy when solving the linear system (38.38), and it strongly influences the efficiency of the algorithm. If $\eta_{\mathtt{k}} = 0$ for all $\mathtt{k} \geq 0$, the inexact procedure reduces to the standard Newton method. Actually, the inexact Newton method is locally convergent [102]. In particular, if F' is Lipschitz continuous in a neighborhood of $\boldsymbol{U}^*$, $F'(\boldsymbol{U}^*)$ is nonsingular, $\boldsymbol{U}_0$ is sufficiently close to $\boldsymbol{U}^*$, and $\eta_{\mathtt{k}}$ is uniformly bounded away from one for any $\mathtt{k} \geq 0$ (i.e., $\eta_{\mathtt{k}} \leq \eta_{\max} < 1$, as in Algorithm 38.3), then the sequence $\{\boldsymbol{U}_{\mathtt{k}}\}$ converges linearly to $\boldsymbol{U}^*$ with respect to the norm $\|\cdot\|_*$, with $\|\mathbf{v}\|_* = \|F'(\boldsymbol{U}^*)\mathbf{v}\|$ for any $\mathbf{v} \in \mathbb{R}^N$ and with $\|\cdot\|$ a generic norm, i.e.,

$$\|\boldsymbol{U}_{\mathtt{k}\ +1} - \boldsymbol{U}^*\|_* \leq \nu\|\boldsymbol{U}_{\mathtt{k}} - \boldsymbol{U}^*\|_*$$

with $\nu \in (0, 1)$. If $\lim_{\mathtt{k}\to\infty} \eta_{\mathtt{k}} = 0$, then convergence is superlinear, i.e.,

$$\lim_{k\to\infty} \frac{\|\boldsymbol{U}_{k+1} - \boldsymbol{U}^*\|}{\|\boldsymbol{U}_k - \boldsymbol{U}^*\|} = 0.$$

Finally, if $\eta_k \leq \xi \|F(\boldsymbol{U}_k)\|^2$ for some $\xi > 0$, then convergence is quadratic, being

$$\|\boldsymbol{U}_{k+1} - \boldsymbol{U}^*\| \leq \tilde{\nu} \|\boldsymbol{U}_k - \boldsymbol{U}^*\|^2,$$

with $\tilde{\nu}$ a positive constant. Besides controlling local convergence rate, a proper choice of the forcing term avoids the so-called *oversolving* phenomenon. This means that system $F'(\boldsymbol{U}_k)\Delta\boldsymbol{U}_k = -F(\boldsymbol{U}_k)$ is approximately solved, with an accuracy that is far beyond what is needed to obtain a sufficient reduction in the norm of F. In particular, the computation of an accurate $\Delta\boldsymbol{U}_k$, when far from a solution, may yield either a marginal improvement or no progress toward an actual solution because of the significant mismatch between the linear model, $F(\boldsymbol{U}_k) + F'(\boldsymbol{U}_k)\Delta\boldsymbol{U}_k$, and the updated value, $F(\boldsymbol{U}_k + \Delta\boldsymbol{U}_k)$. Vice versa, a less accurate solution of system $F'(\boldsymbol{U}_k)\Delta\boldsymbol{U}_k = -F(\boldsymbol{U}_k)$ can be both more effective in reducing the norm of F and more convenient from a computational view point. Smart choices for the forcing term allows us to avoid oversolving in the early iteration phase and to achieve fast local convergence during the late iteration stage. Two choices that fulfill these requirements are provided in [103, 104]. Given $\eta_0 \in [0, 1)$ ($\eta_0 = 0.5$ is a standard default value), the first choice selects

$$\eta_k = \frac{\left|\|F(\boldsymbol{U}_k)\| - \|F(\boldsymbol{U}_{k-1}) + F'(\boldsymbol{U}_{k-1})\Delta\boldsymbol{U}_{k-1}\|\right|}{\|F(\boldsymbol{U}_{k-1})\|} \quad k \geq 1,$$

while the second choice leads us to pick

$$\eta_k = \frac{\|F(\boldsymbol{U}_k)\|}{\|F(\boldsymbol{U}_{k-1})\|} \quad k \geq 1.$$

Very frequently, Krylov subspace projection methods [21] are used as iterative linear solvers in inexact Newton methods, leading to the so-called Newton-Krylov algorithms [102, 104]. These methods, which will be discussed more in detail in Sect. 38.6.2, do not require the explicit computation of the Jacobian $F'(\boldsymbol{U}_k)$. On the contrary, they focus only on the "action" of $F'(\boldsymbol{U}_k)$ on a generic vector $\boldsymbol{V} \in \mathbb{R}^N$. In particular, if the nonzero entries of $F'(\boldsymbol{U}_k)$ are available, the product $F'(\boldsymbol{U}_k)\boldsymbol{V}$ can be computed analytically with a computational cost which depends on the sparsity of the Jacobian. Alternatively, product $F'(\boldsymbol{U}_k)\boldsymbol{V}$ is approximated by a finite difference scheme, i.e., as

$$F'(\boldsymbol{U}_k)\boldsymbol{V} \sim \frac{F(\boldsymbol{U}_k + \zeta\boldsymbol{V}) - F(\boldsymbol{U}_k)}{\zeta}, \tag{38.41}$$

with $\zeta > 0$ a properly selected scalar, this leading to a so-called "matrix-free" procedure [102, 104]. In this case, the cost for evaluating $F'(\boldsymbol{U}_k)\boldsymbol{V}$ reduces to a single function evaluation (i.e., $F(\boldsymbol{U}_k + \zeta\boldsymbol{V})$), $F(\boldsymbol{U}_k)$ being already available. The parameter ζ in (38.41) is commonly fixed as

$$\zeta = \begin{cases} \sqrt{\texttt{eps}}\,\dfrac{\|\boldsymbol{U}_k\|}{\|\boldsymbol{V}\|} & \text{if } \|\boldsymbol{U}_k\| \neq 0 \\ \sqrt{\texttt{eps}} & \text{otherwise,} \end{cases}$$

with `eps` the unit round-off. This choice, although heuristic, ensures a balance between floating point and truncation error [100, §5.4.4].

Globalization strategies consisting in a line search along the inexact Newton step, $\Delta\boldsymbol{U}_k$, have been widely investigated (see, e.g., [100, 103–106]), giving rise to the damped inexact Newton method (or inexact Newton method with line search). An effective implementation of the damped inexact Newton is provided in the following

Algorithm 38.4 Damped Inexact Newton method

Input : $\boldsymbol{U}_0 \in \mathbb{R}^N$, $\eta_{\max} \in (0, 1)$, `TOL` < 1, $\texttt{ESTIM}_0 >$ `TOL`, `kmax`, $\alpha, \sigma \in (0, 1)$

1: Set: `k = 0`;
2: **while** $\texttt{ESTIM}_k >$ `TOL` & `k` $<$ `kmax` **do**
3: Choose $\eta_k \in [0, \eta_{\max}]$;
4: Find $\Delta\boldsymbol{U}_k$ such that $\|F(\boldsymbol{U}_k) + F'(\boldsymbol{U}_k)\Delta\boldsymbol{U}_k\|_2 \leq \eta_k\|F(\boldsymbol{U}_k)\|_2$;
5: Set: $\lambda = 1$;
6: **while** $\|F(\boldsymbol{U}_k + \lambda\,\Delta\boldsymbol{U}_k)\|_2 > (1 - \alpha(1 - \eta_k))\|F(\boldsymbol{U}_k)\|_2$ **do**
7: Compute $\lambda = \sigma\lambda$;
8: Compute $\eta_k = 1 - \sigma(1 - \eta_k)$;
9: **end while**
10: Compute $\boldsymbol{U}_{k+1} = \boldsymbol{U}_k + \lambda\Delta\boldsymbol{U}_k$;
11: Compute $\texttt{ESTIM}_k$;
12: `k = k+1`;
13: **end while**

The backtracking phase (lines 6–8) has a finite termination [100]. It can be checked that the selected step, $\lambda\,\Delta\boldsymbol{U}_k$, coincides with an inexact Newton step corresponding to the forcing term $1 - \lambda(1 - \eta_k^*)$, with η_k^* the initial value of η_k (i.e., the forcing term selected in line 3). A typical value for α is 10^{-4} [99]. Concerning the choice of λ, the simple update in line 7 allows one to progressively reduce λ by a fixed factor, where typical values for σ are 0.5 and 0.1, as for Algorithm 38.2 [99]. As an alternative, λ is selected by using a polynomial model for the scalar function $\psi(\boldsymbol{U}_k + \lambda\Delta\boldsymbol{U}_k)$, and choosing the minimum of such a polynomial as the next step length [99, 100].

Finally, the Bank-Rose method can be adopted also in this case, by exploiting exactly what remarked for Algorithm 38.2 [101].

A Fortran implementation of the damped inexact Newton method based on Algorithm 38.4 and called NITSOL is pro-

posed in [104] and made freely accessible at the webpage https://users.wpi.edu/~walker/NITSOL/. This code can be easily employed as a template for a translation in other programming languages. Matlab codes for Newton method, inexact Newton method, and damped versions are accessible through the webpage https://ctk.math.ncsu.edu/newtony.html and are documented in [100].

38.6.2 Linear Solvers

Both the Gummel map and the fully coupled Newton approach involve the numerical solution of linear systems,

$$\mathbf{Az} = \mathbf{b}, \tag{38.42}$$

which are typically *sparse*. A rigorous definition of sparse matrix is not available. Informally, a sparse matrix is characterized by a sufficiently large number of zero entries such that this can be advantageously exploited [21, 107].

The efficient solution of sparse linear systems can be pursued by either direct or iterative methods. Direct methods for sparse linear systems overcome the drawback characterizing standard factorizations, i.e., the presence of entries that, during the factorization, change their value from zero to nonzero. This phenomenon is known as *fill-in*. A sparse factorization of matrix $\mathbf{A}$ consists of three steps [107]. The first one performs a reordering (with permutations of rows and/or columns) of $\mathbf{A}$ to reduce the fill-in induced by the factorization, with respect to the one associated with the original matrix. The reordering is driven by efficient heuristics, since minimizing the fill-in coincides with an NP-hard problem. Well-known ordering algorithms are provided by the approximate minimum degree, the Cuthill-McKee, and the column permutation methods [107]. The second step coincides with the LU factorization of the reordered matrix. Finally, the third step involves triangular solvers for sparse matrices.

The reordering of $\mathbf{A}$ can be performed without introducing instabilities in the associated LU factorization, as shown in [108]. In this case, it can be found a sparsity-preserving column permutation matrix, $\mathbf{Q}$, which reduces the fill-in induced by any row permutation associated with the *LU* factorization with partial pivoting of matrix $\mathbf{AQ}$. This finally yields the factorization $\mathbf{PAQ} = \mathbf{LU}$, where $\mathbf{P}$ is a permutation matrix selected independently of the sparsity, while $\mathbf{L}$ and $\mathbf{U}$ are a lower and an upper triangular matrix, respectively. This reordering is *symbolic*, namely, it is performed by using only the position of the nonzero entries of $\mathbf{A}$. Symbolic factorization is much more convenient in terms of time and memory than the numerical factorization. Actually, it can be reused for matrices characterized by the same sparsity pattern, such as those arising during Newton iterations and in the time stepping. In Sect. 38.7, we will provide some examples of reordering applied to the matrix yielded by the discretization of the drift-diffusion model for the MOS device in Fig. 38.1.

Concerning the softwares related to sparse direct solvers, we cite SUITESPARSE (`faculty.cse.tamu.edu/davis/suitesparse.html`.) and, specifically, function COLAMD. Both parallel and sequential implementations of sparse direct solvers are also available in the package MUMPS (http://mumps.enseeiht.fr/.) (MUltifrontal Massively Parallel Sparse solver) [109, 110] and PARDISO (https://www.pardiso-project.org/.) (PARallel DIrect sparse SOlver interface) [111, 112]. Finally, we point out that the MATLAB command\automatically resorts to linear solvers for sparse matrices if matrix $\mathbf{A}$ is allocated as a sparse array.

Krylov subspace methods constitute a class of very successful iterative algorithms for solving linear systems. As anticipated in the previous section, these methods require only the product of $\mathbf{A}$ times a vector. In the context of Newton-Krylov methods, *transpose-free* solvers are generally preferred. The reason is twofold. First of all, if the Jacobian is available, it is stored in a sparse compact format which allows one for an efficient row-column matrix-vector product. Secondly, if the Jacobian is not available, products involving the transpose of the Jacobian cannot be performed by resorting to finite difference schemes. Transpose-free methods commonly used are the GMRES (Generalized Minimal RESidual) [113], the BICGSTAB (Bi-Conjugate Gradient STABilized method) [114], and the TFQMR (Transpose-Free Quasi-Minimal Residual) [115] algorithms, although it is well-known that it is not possible to rank iterative solvers for non-symmetric linear systems [116].

GMRES is a breakdown-free iterative method suited to solve indefinite systems of linear equations [113]. When applied to system (38.42), given the initial guess $\mathbf{z}^0$, the m-th GMRES iteration, $\mathbf{z}^m$, with $m \geq 1$, solves the least-squares problem

$$\min_{\mathbf{z} \in \mathbf{z}^0 + K_m} \|\mathbf{Az} - \mathbf{b}\|_2, \tag{38.43}$$

where

$$K_m = \text{span}\left\{\boldsymbol{r}_{\text{k}}^0, \mathbf{A}\boldsymbol{r}_{\text{k}}^0, (\mathbf{A})^2\boldsymbol{r}_{\text{k}}^0, \ldots, (\mathbf{A})^{m-1}\boldsymbol{r}_{\text{k}}^0\right\}, \tag{38.44}$$

is the m-th Krylov subspace, and $\boldsymbol{r}_{\text{k}}^0 = (\mathbf{Az}^0 - \mathbf{b})$ is the initial linear residual. Ideally, the GMRES method finds the solution to the linear system in a number of iterations, at most, equal to the order of the system, since it minimizes the residual in increasing subspaces [113]. In practice, due to the accumulation of the rounding error, this is not the case and GMRES is implemented as an iterative algorithm and stopped when the residual becomes sufficiently small.

Using an orthonormal basis for the Krylov subspaces, K_m, the residual $\boldsymbol{r}_{\mathrm{k}}^m = \mathbf{A}\mathbf{z}^m - \mathbf{b}$ can be computed without deriving explicitly $\mathbf{z}^m$ [113].

Although from (38.43), the residual norm, $\|\boldsymbol{r}_{\mathrm{k}}^m\|$, is non-increasing with m, GMRES may stagnate, i.e., the residual norm may remain constant for a certain number of iterations [21]. Moreover, from a practical viewpoint, the basis of the Krylov subspaces has to be stored to perform GMRES iterations. This requirement becomes prohibitive when the order of the system is large. Typically a maximum value, ℓ, of GMRES iterations is fixed. If, after ℓ iterations, the desired accuracy is not reached, then GMRES is *restarted* with initial guess, $\mathbf{z}^0$, equal to $\mathbf{z}^\ell$. The convergence of such a procedure is not always guaranteed. Restarting may degrade performances but, in general, the idea works well in practice [113]. Small values of ℓ are usually chosen, such as $l = 10,\ 20,\ 50$. An alternative to restarted GMRES is represented by the QUASI-GMRES method [117].

BICGSTAB and TFQMR constitute useful alternatives to GMRES, since storage requirements do not increase during the successive iterations. Nevertheless, for these methods, the residual does not decrease monotonically and two matrix-vector products are required at each iteration. Although there does not exist a rigorous convergence theory for the BICGSTAB method, and the TFQMR algorithm may break down, both these procedures can be competitive with GMRES when matrix-vector products are cheap and GMRES convergence is slow.

Iterative methods may exhibit lack of robustness, unlike direct methods, or of efficiency [21, 118]. *Preconditioning* techniques can improve both these properties. They commute the original system into an equivalent one which turns out to be easier to solve via iterative methods. A preconditioner coincides with a non-singular matrix, $\mathbf{M}$, satisfying the following properties: it is, somehow, close to $\mathbf{A}$; solving linear systems with $\mathbf{M}$ as coefficient matrix is numerically affordable; the preconditioned system can be solved more efficiently (i.e., with a faster convergence) than the original one. Moreover, we remark that, if an effective preconditioner is available, the solution of the preconditioned system is less sensitive to the choice of the linear solver.

Now, if the preconditioner is applied on the left, the linear system in (38.42) becomes

$$\mathbf{M}^{-1}\mathbf{A}\mathbf{z} = \mathbf{M}^{-1}\mathbf{b}, \tag{38.45}$$

while, when it is applied on the right, we obtain

$$\mathbf{A}\mathbf{M}^{-1}\widetilde{\mathbf{z}} = \mathbf{b} \quad \text{with } \mathbf{z} = \mathbf{M}^{-1}\widetilde{\mathbf{z}}. \tag{38.46}$$

It follows that, if now we apply GMRES, in the former case we minimize the residual $\mathbf{M}^{-1}(\mathbf{A}\mathbf{z} - \mathbf{b})$, while, in the latter case, we minimize the residual associated with the original system. Thus, right preconditioning is often preferred to the left one since allowing to track, through the iterations, the residual we are interested in.

A common way to build the preconditioner $\mathbf{M}$ is to perform a threshold incomplete LU (ILUT) factorization of $\mathbf{A}$ [119]. ILUT factorization has sparse lower and upper triangular factors and is meant to approximate $\mathbf{A}$ at a low computational cost. One of the simplest ways to apply ILUT is to impose that factors $\mathbf{L}$ and $\mathbf{U}$ share the same sparsity pattern as $\mathbf{A}$. Nevertheless, the resulting incomplete factorization, named ILUT(0), is often a crude approximation to the original matrix. Alternatively, the incomplete factorization can be computed so that the entries smaller than a fixed tolerance are dropped from factors $\mathbf{L}$ and $\mathbf{U}$ during factorization. Clearly, the lower the tolerance, the more accurately the ILUT preconditioner approximates $\mathbf{A}$ as well as the denser the triangular factors become, thus increasing the computational effort of the direct triangular solvers [21].

38.7 The n-MOSFET Test Case

We numerically solve the drift-diffusion system (38.3)–(38.4) applied to the n-MOSFET device in Fig. 38.1 in a steady setting. In particular, we are interested in investigating the dependence of the transfer characteristics (i.e., the drain current as function of the gate voltage) on the adopted grid. For this purpose, we resort to the FEMOS-MP (Finite Element Modeling-Oriented Simulator for Multi-Physics simulations) platform [30, 120]. FEMOS-MP is a general-purpose modular code based on the Galerkin FE method to model complex interplaying multiphysics phenomena in semiconductor and biophysics, including both 2D and 3D geometric configurations.

To improve the mathematical and numerical description of the physics occurring in the n-MOSFET device, we consider the Shockley-Read-Hall (SRH) and the Auger mechanisms as the recombination/generation law on the right-hand side of (38.2) (for more details, we refer to [22]). Moreover, it is well-known that, in real semiconductors, the carrier bulk mobility exhibits a strong dependence on several mechanisms (e.g., the doping or the interface scattering). For this reason, we compute the carrier mobilities by considering the contribution of the doping (Masetti's model [121]) and of the electric field (Canali's model [122]), while neglecting the interface scattering and the short channel-related effects.

Due to the simplest choice allowed for the initial guess, we adopt the Gummel method in Sect. 38.3 as a decoupling scheme, while resorting to Algorithm 38.2 to solve the system associated with the nonlinear Poisson equation, as in [123]. Concerning the computational mesh, we identify $\mathcal{T}_h$ with the grids in Figs. 38.3 and 38.4, and we apply the EAFE discretization scheme (see Remark 38.1). Finally, we will

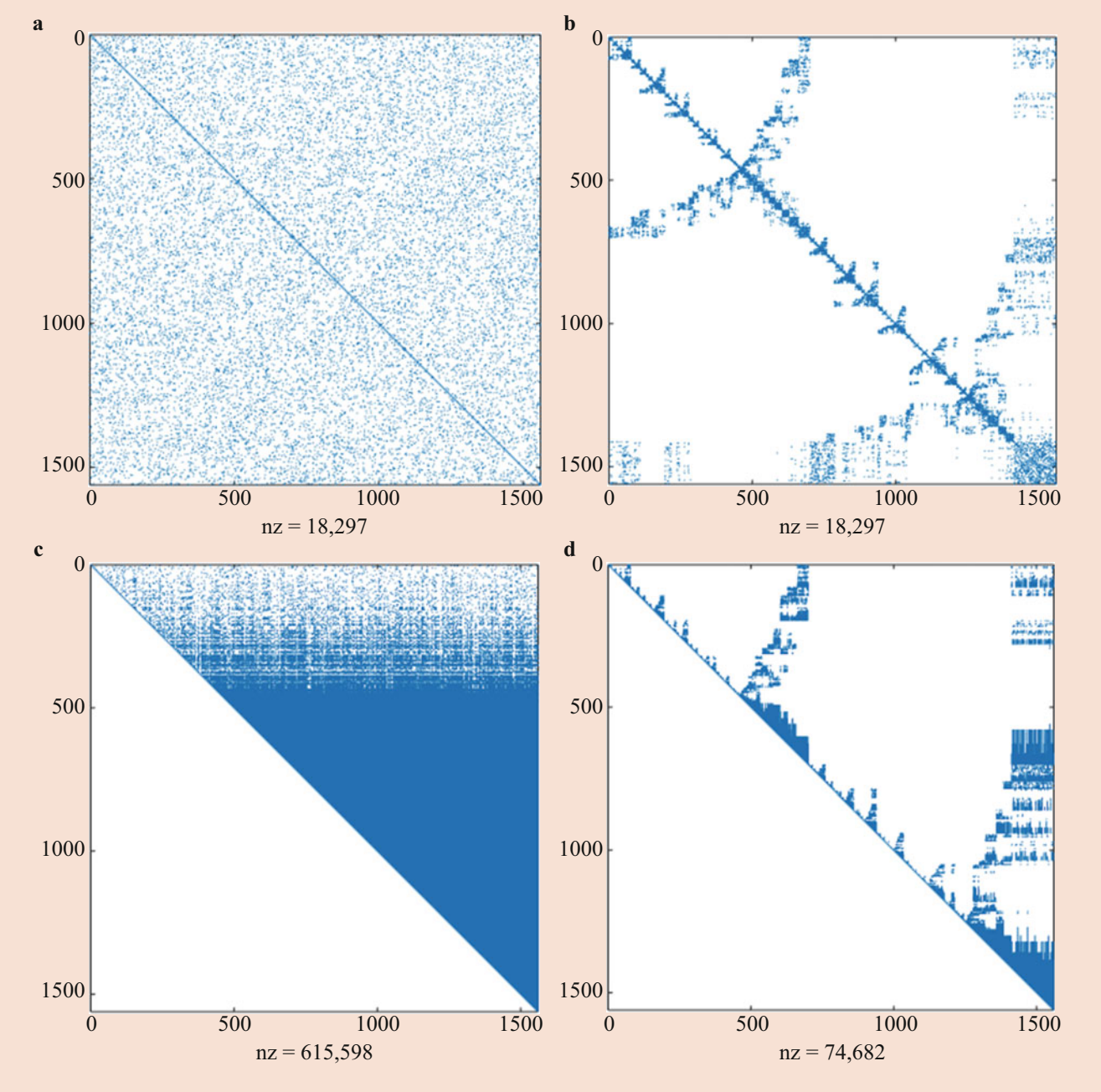

Fig. 38.5 Structured mesh: (**a**) sparsity pattern of matrix $\mathbf{A}_{\mathrm{NLP}}$ and (**b**) of the corresponding Cholesky factor, (**c**) before and (**d**) after the AMD reordering

compare the performances of some of the solvers available in FEMOS-MP to deal with systems (38.26)–(38.28).

38.7.1 Comparison of Sparse Solution Techniques

We focus here on the matrix associated with the FE discretization of the nonlinear Poisson equation (38.3) on the three meshes in Fig. 38.3.

In particular, in Figs. 38.5, 38.6, and 38.7a, we show the sparsity pattern of the matrix $\mathbf{A}_{\mathrm{NLP}}$ in (38.26), after the assignment of the boundary conditions and for the three choices of the grid, the number of nonzero entries being denoted by `nz`. The pattern associated with the structured mesh is very uniform, with a completely full diagonal. This is due to the fact that tetrahedra evenly cover the whole domain, without distinguishing any particular area from the others. On the contrary, the corresponding panels in Figs. 38.6 and 38.7 exhibit the presence of block substructures.

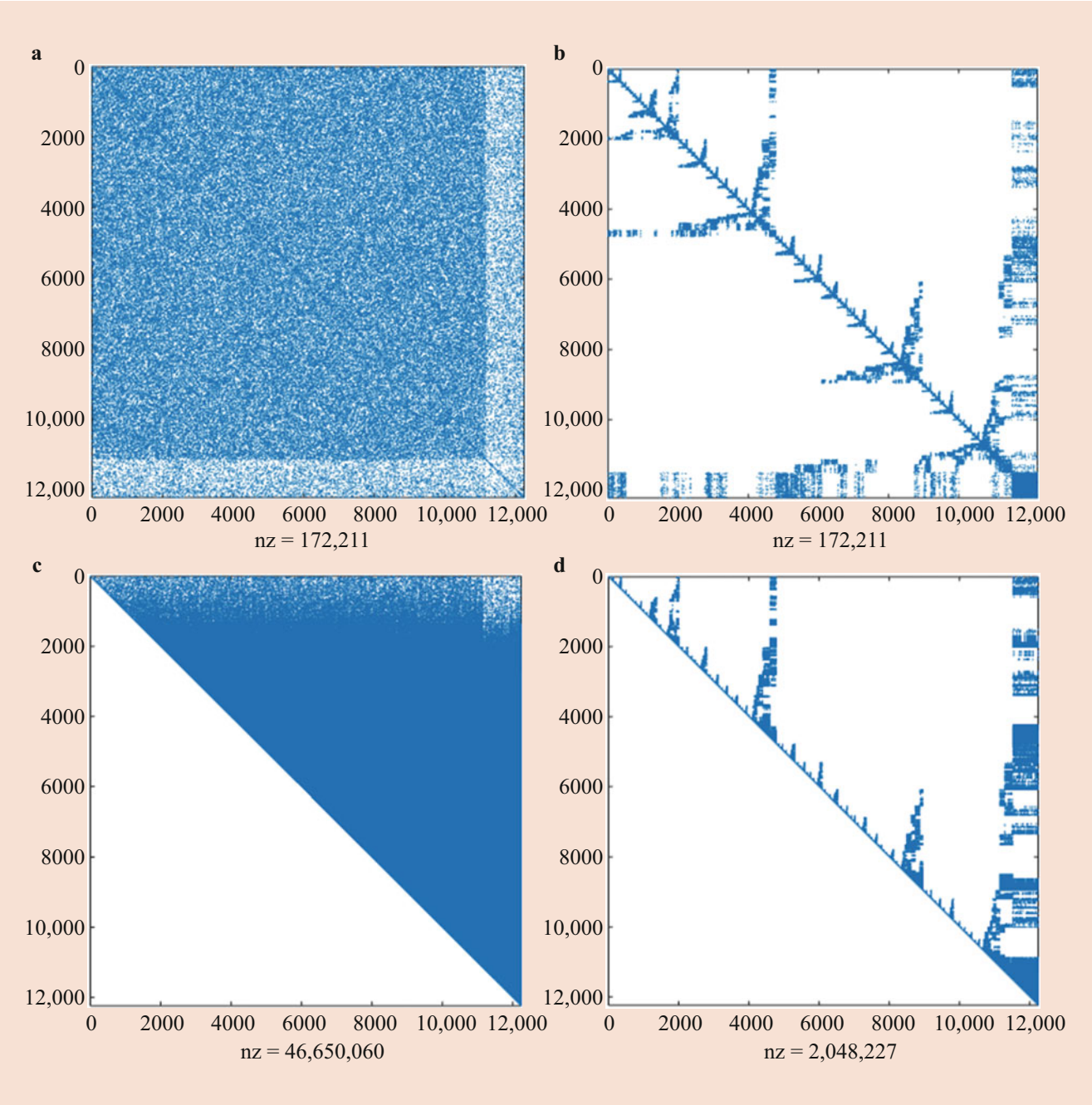

Fig. 38.6 Unstructured mesh: (**a**) sparsity pattern of matrix $\mathbf{A}_{\mathrm{NLP}}$ and (**b**) of the corresponding Cholesky factor, (**c**) before and (**d**) after the AMD reordering

The dimension, N_h, of matrix $\mathbf{A}_{\mathrm{NLP}}$ increases when moving from the structured ($N_h = 1580$) to the hybrid ($N_h = 6442$) and to the unstructured ($N_h = 12,240$) mesh, while the matrix density, identified by the ratio $\mathtt{nz}/N_h^2$, increases as expected, being $7 \cdot 10^{-3}$, $5 \cdot 10^{-4}$ and 10^{-3}, respectively.

To efficiently solve system (38.26) via a direct method, it is advisable to employ a reordering algorithm (see Sect. 38.6.2). Figures 38.5, 38.6, and 38.7b show how the sparsity pattern of matrix $\mathbf{A}_{\mathrm{NLP}}$ modifies after applying the `Matlab` function `AMD` which implements the approximate minimum degree (AMD) reordering [124]. In the same figures, we also provide the sparsity pattern for the Cholesky (upper triangular) factor, before (bottom left) and after (bottom right) the reordering. The effect of the reordering is evident both on the original matrix and the Cholesky factor. In particular, the difference in terms of the sparsity pattern among the three different meshes reduces after the reordering, independently of the value for N_h.

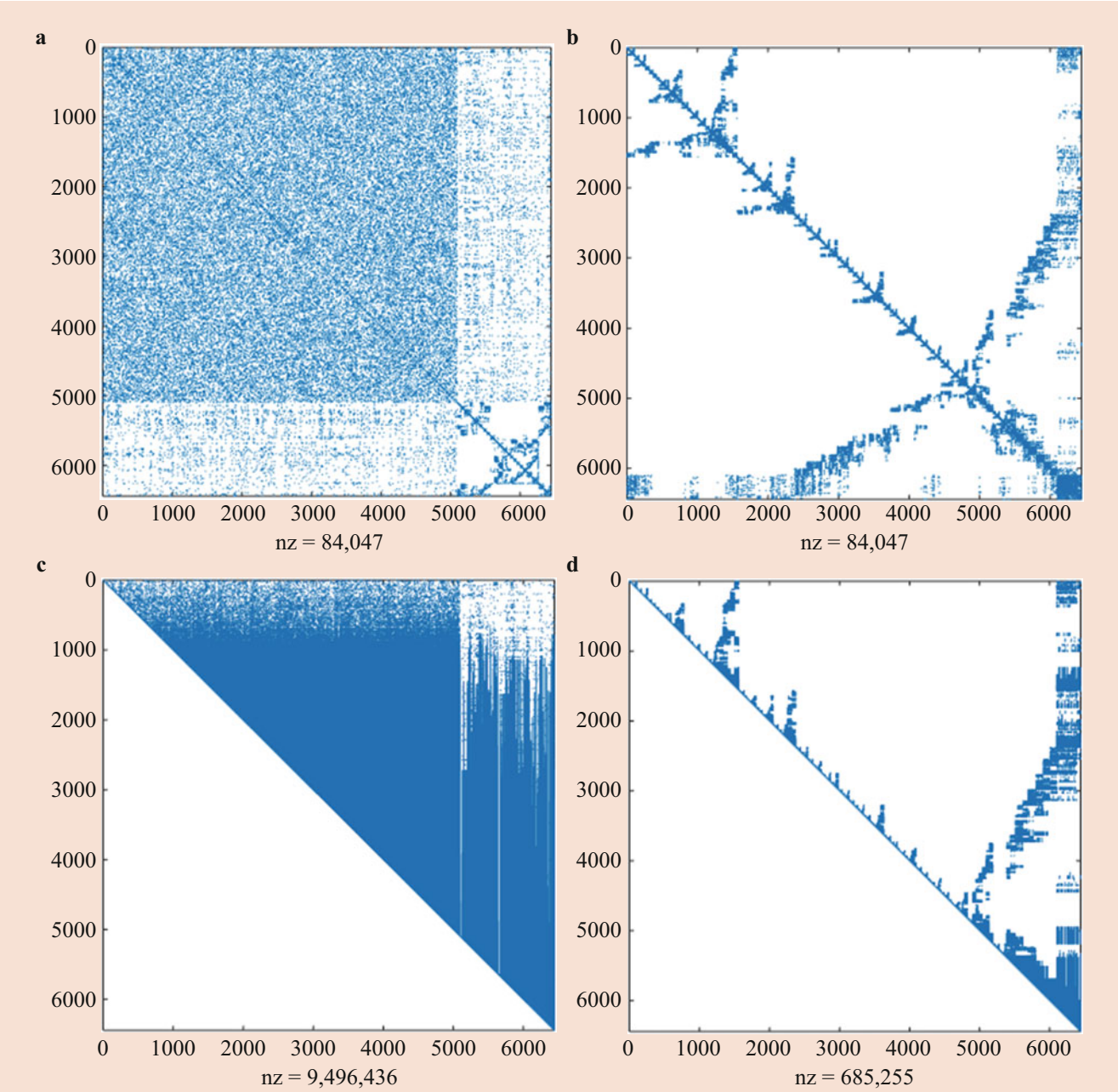

Fig. 38.7 Hybrid mesh: (**a**) sparsity pattern of matrix $\mathbf{A}_{\mathrm{NLP}}$ and (**b**) of the corresponding Cholesky factor, (**c**) before and (**d**) after the AMD reordering

In Table 38.1, we investigate the effectiveness of direct methods for sparse linear systems. We compare SUPERLU [125], MUMPS [109, 110], and UMFPACK [107] libraries in terms of CPU time (in seconds) (The computations have been run on a portable PC equipped with INTEL i5 processor 2.4 GHz and 8 GB of RAM.). In particular, we measure the time actually demanded by the solver, while neglecting the matrix assembling phase. All the libraries involved in this comparison employ LU-based factorizations combined with the AMD reordering. As an alternative, we resort to a SParse QR (SPQR) factorization [107]. Nevertheless, this turns out to be the most expensive algorithm both on the structured and unstructured grids and fails on the hybrid mesh. Actually, QR factorization efficiently works only for highly ill-conditioned systems. In all the other cases, the orthogonal matrix Q is characterized by many nonzero entries, thus becoming unpractical.

For the sake of comparison, in Table 38.1 we furnish also the CPU time associated with the BCG-NR [126] and the BCG-EIGEN [127] iterative methods that we run without

preconditioning and by adopting the default options. The performances of BCG-NR are fully comparable with the ones of MUMPS and UMFPACK. Nevertheless, to have reliable solutions, we have set a very high accuracy. Moreover, these methods are, in general, enriched by suitable preconditioners (see Sect. 38.6.2), whose choice, unfortunately, represents a problem-dependent issue.

Thus, to sum-up, we can state that LU-based direct solvers (enriched with reordering algorithms) represent the ideal tool to solve sparse systems, provided that memory requirements and CPU time remain contained. If this is not the case, we can resort to iterative methods, after an ad hoc selection of a preconditioner.

38.7.2 Numerical Assessment

We investigate here the electrical properties characterizing the discretization performed in the previous section, with a particular emphasis on the possible influence of the computational mesh. We adopt the MUMPS solver for all the assessments throughout performed.

Table 38.1 NLP system, CPU time [s]: comparison among solvers and for different meshes

Solver	Structured mesh	Unstructured mesh	Hybrid mesh
Superlu	$1.8573 \cdot 10^{-2}$	$1.6730 \cdot 10^{0}$	$2.6797 \cdot 10^{-1}$
mumps	$2.6008 \cdot 10^{-2}$	$5.2267 \cdot 10^{-1}$	$2.0729 \cdot 10^{-1}$
umfpack	$1.2558 \cdot 10^{-2}$	$4.6721 \cdot 10^{-1}$	$1.3596 \cdot 10^{-1}$
spqr	$3.5664 \cdot 10^{-2}$	$2.1753 \cdot 10^{0}$	FAILURE
bcg-nr	$2.2140 \cdot 10^{-2}$	$4.2618 \cdot 10^{-1}$	$1.5783 \cdot 10^{-1}$
bcg-eigen	$3.2930 \cdot 10^{-2}$	$1.1702 \cdot 10^{0}$	$3.3415 \cdot 10^{-1}$

In particular, Fig. 38.8a compares the n-MOSFET transfer characteristics, for the different computational meshes in Fig. 38.3. We observe a mismatch among the three curves when the gate voltage is low. This can be ascribed to the electron density, whose gradient strongly influences the drift-diffusion current. Figure 38.9 highlights the difference among the three meshes in terms of electron density concentration. In particular, the structured grid results in the highest current, i.e., in the highest electron concentration in the region under the gate. From a modeling viewpoint, the simulations associated with the unstructured and the hybrid grids better describe the electron generation in the region delimited by the source and the drain junctions. On the contrary, the employment of the structured mesh leads to an overestimation of this mechanism, due to the limited number of dofs in such a region.

Figure 38.8b shows the Id-Vg transfer curves associated with the adapted grids in Fig. 38.4. The characteristics are essentially overlapped, with a slight mismatch when the gate voltage is low, analogously to Fig. 38.8a. This very small difference does not allow to easily compare the two simulations in terms of electron density. In this case, it is more convenient to consider the SRH contribution (see Fig. 38.10, where higher SRH (red colors) mean higher recombination). It turns out that the SHR mechanism is correctly captured along the whole junction profile when employing the grid adapted via the geometric plus the physical criterion, whereas, in the purely geometric case, the profile exhibits some interruptions caused by the nonoptimal mesh. Thus, the choice of a computational mesh able to follow the features of the problem turns out to be crucial in terms of modeling accuracy (besides of convergence properties of the numerical algorithms).

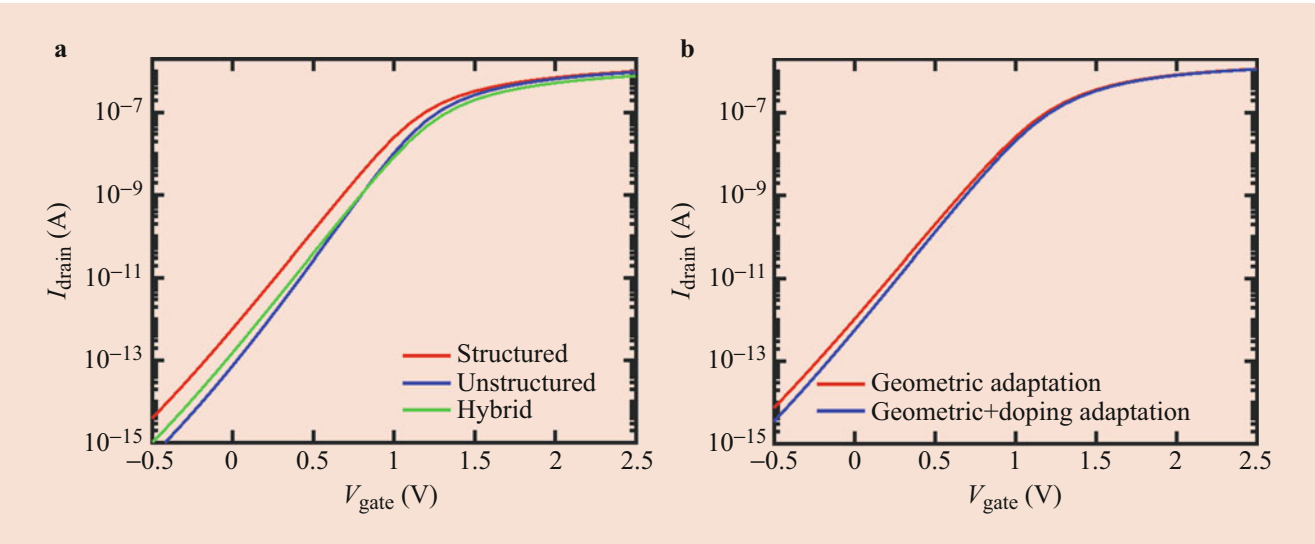

Fig. 38.8 n-MOSFET device: $I_d - V_g$ transfer characteristics in logarithmic scale for the grids in Fig. 38.3a and Fig. 38.4b

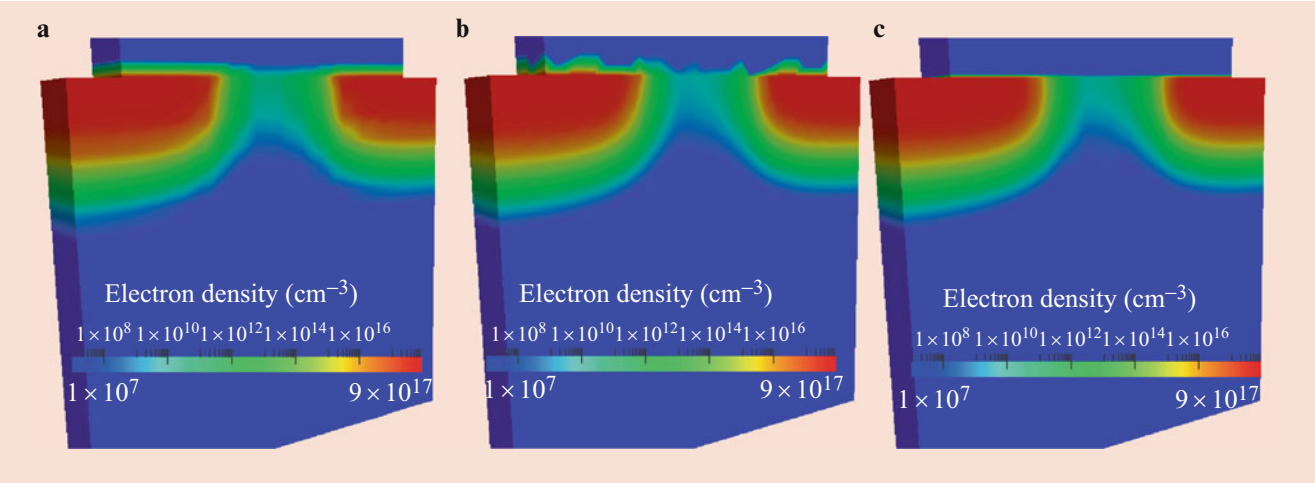

Fig. 38.9 n-MOSFET device: color plot of the electron density concentration at $V_{\text{Drain}} = 0.1$ (V) and $V_{\text{Gate}} = 0.0$ (V) on the (**a**) structured, (**b**) unstructured, and (**c**) hybrid mesh

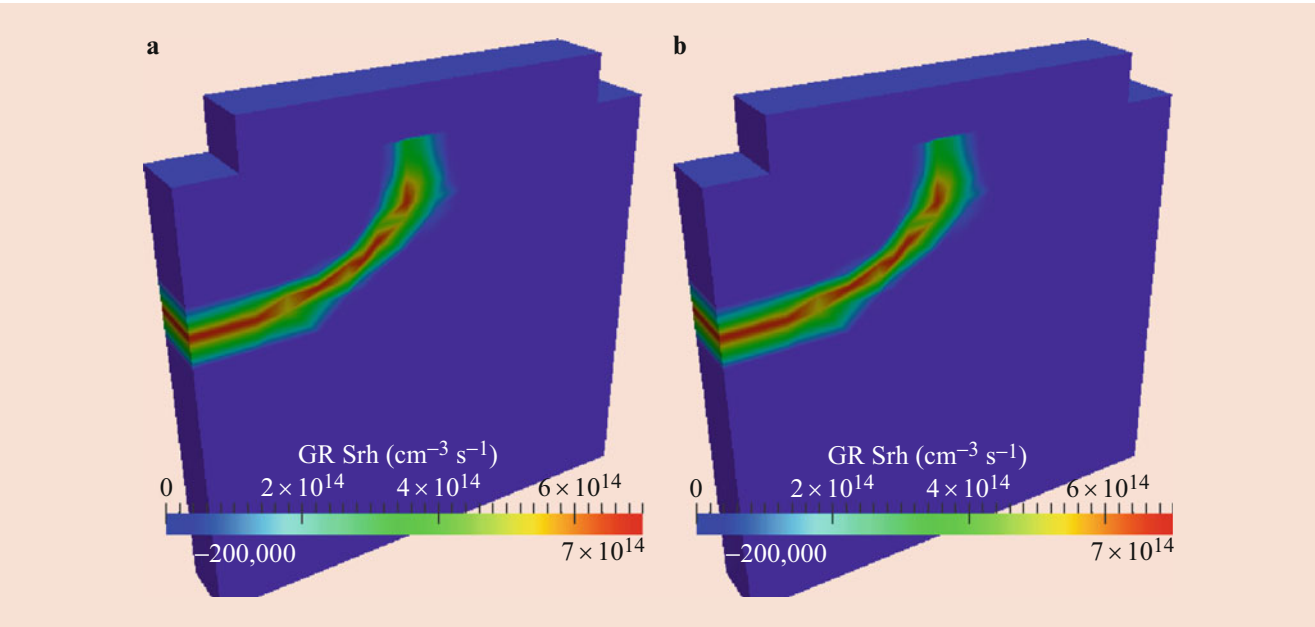

Fig. 38.10 n-MOSFET device: color plot of the SRH net production term at $V_{\text{Drain}} = 0.1$ (V) and $V_{\text{Gate}} = 0.0$ (V) on the (**a**) geometric and (**b**) geometric+doping adapted mesh

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Spherical Harmonics Expansion and Multi-Scale Modeling

39

Bernd Meinerzhagen and Christoph Jungemann

Contents

39.1 Introduction 1413

39.2 The Spherical Harmonic Expansion Method 1414
39.2.1 The Boltzmann Transport Equation 1414
39.2.2 Spherical Harmonics Expansion 1416
39.2.3 Results 1419

39.3 Multi-Scale Modeling 1426
39.3.1 Sequential Multi-Scale Modeling 1426
39.3.2 Concurrent Multi-Scale Modeling 1432

39.4 Numerical Solution of the Drift-Diffusion Model: Some Historical Remarks 1437

39.5 Conclusion 1445

References 1446

Abstract

By far, most numerical device simulations are still based on the drift-diffusion (DD) model, owing to its versatility, numerical efficiency, and robustness. However, the DD model is of limited physical accuracy for nanoscale devices and hot carrier effects. Advanced physical modeling in the regime of semi-classical transport must therefore be based on the Boltzmann transport equation (BTE), and the typical solution method for this equation is a Monte-Carlo (MC) algorithm owing to its small memory requirements. Unfortunately, this popular solution method makes the BTE model much less versatile than the DD approach, as, for example, no AC and noise analysis in the small-signal framework based on the Jacobian of the numerical model is available if the MC method is used. Moreover, evaluating the complete transport of carriers in a device by the BTE model is always several orders of magnitude less efficient in terms of CPU time than the application of the DD model. Thus, there is a clear demand to increase the versatility of the BTE model and to enhance the physical accuracy of the DD model without compromising its numerical efficiency and robustness. Solving the BTE model with the spherical harmonic expansion (SHE) method allows the calculation of the full Jacobian of the discrete system and to establish AC and noise analysis in the small-signal framework, thus making the BTE model much more versatile. Moreover, sequential and concurrent multi-scale methods using microscopic models such as the BTE model where necessary and macroscopic models such as the DD model otherwise are well suited to enhancing the physical accuracy of the DD model without compromising its efficiency and robustness. In addition, using the SHE method allows many of the discretization methods and principles previously developed for the DD model to be applied for the discretization of the BTE model. Therefore, a short overview of the historic development of discretization methods and principles, finally making the DD model as efficient and robust as it is today, is added as well.

Keywords

Multi-scale simulation · Boltzmann transport equation · Spherical harmonics expansion · Monotonicity-preserving discretization · Hierarchical drift-diffusion · Hydrodynamic equations

39.1 Introduction

In the semi-classical framework electron and hole motion in semiconductors is described by Newton's classical laws,

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whereas scattering rates and band structures are calculated by quantum mechanical methods [1]. The most fundamental transport equation in this framework is the BTE, which was derived by Ludwig Boltzmann to model the dynamics of an ideal gas, and was later applied to electrons and holes in semiconductors [2]. It describes the temporal evolution of the distribution function and the density in the single-particle phase space, which spans the real space and the k-space (KS) [3]. The BTE, which is an integro-differential equation, can be solved by the MC method, which is used to calculate hot-electron phenomena in the case of strong non-equilibrium [4–8]. Owing to its simplicity and low memory requirements, the stochastic MC algorithm is the method of choice for solving the BTE, and, for example, numerically calculated band structures (full bands) can be easily included [9–12]. It is inherently transient and in the case of the physical MC method electronic noise can be simulated [13]. On the other hand, the transient and stochastic nature of the MC technique can lead to problems. It is difficult to obtain very accurate solutions, because the variance of the estimated values is inversely proportional to the CPU time [14–17]. In the case of processes with very different time scales or rare events, CPU times might become too long to be feasible. This shows clearly that the numerical properties of the MC method are very different from the robust and versatile methods used in the case of other technology computer-aided design (TCAD) models (e.g., the drift-diffusion [DD] model), making the numerical effort needed for the TCAD models much less dependent on the bias conditions and the required numerical accuracy. Thus, alternative deterministic methods for the solution of the BTE were developed (e.g., [18–20]). The most important one is the spherical harmonics expansion (SHE) method, which has its origin in semi-analytical solutions of the BTE [21–23]. Application of this method to device simulation was only possible with the advent of large computer memories and the development of stable numerical algorithms [24]. Although SHE is numerically much more difficult to handle than the MC method, it has distinct advantages [25]. It can be solved directly for the stationary case, AC and noise simulations are possible in the small-signal framework in contrast to the MC method [26–28], and the numerical effort depends only weakly on bias conditions and the required numerical accuracy. The SHE approach can be easily extended in the case of lower-dimensional particle gases, which occur in systems that are confined perpendicular to the transport direction (e.g., inversion channel of a MOSFET). For example, in the case of a quasi-2D particle gas, instead of spherical coordinates, polar coordinates are used and the angular dependencies are expanded into a Fourier series (Fourier harmonic expansion) [29–31].

The models based on direct solutions of the BTE are not only used to simulate devices. As simpler lower-level transport models (e.g., DD and hydrodynamic (HD) models) can be derived from the BTE, their transport and noise parameters (mobilities, relaxation times, etc.) can be generated by bulk simulations with the BTE [12] (see also Sect. 39.3.1). In the case of new materials, it is often not possible to measure transport parameters for all material compositions in the design space and the more fundamental model can be used to generate the transport parameters. For example, in the case of strained SiGe, the transport and noise parameters for the HD and DD models were generated by solving the BTE for a large range of temperatures, Ge contents, doping concentrations, various strain configurations, and crystal orientations, and were stored in a table model [32]. In an investigation of the performance limits of SiGe heterojunction bipolar transistors (HBTs), BTE device simulations were even used to generate certain parameters of a compact model [33]. In addition, the models at the higher level are used to assess the accuracy of the models at a lower level by comparison of results for benchmark devices [12]. Moreover, hot carrier or tunneling-related effects can be modeled by higher-level models based on the results of lower-level models, thus improving the overall modeling accuracy without influencing the computational efficiency too much (see Sect. 39.3.2).

Despite its limited accuracy the DD model is still the numerical device model used most often for device simulations. This is largely because of the accurate, robust, versatile, and computationally efficient numerical methods that are applied for the simulations and which are very similar for the different DD simulation programs mostly applied today. The situation was very different when the solution methods for the DD model were developed about 50 years ago. In particular, many different discretization methods were applied in the beginning and it took about two decades to develop the method, which is still used today. As much can be learned from the historic development of the numerical DD model and the principles and insights leading to the advanced numerical device models used today, a brief outline is added at the end of this chapter.

39.2 The Spherical Harmonic Expansion Method for the Solution of the Boltzmann Transport Equation

39.2.1 The Boltzmann Transport Equation

The distribution function $f^{\nu}(\boldsymbol{r}, \boldsymbol{k}, t)$ is the density in the six-dimensional single-particle phase space of band or valley ν at position $\boldsymbol{r}$ and wave vector $\boldsymbol{k}$ at time t. The particle number in the infinitesimal volume $\mathrm{d}^3k\mathrm{d}^3r$ is given by [3, 34]

$$\mathrm{d}N^{\nu}(\boldsymbol{r}, \boldsymbol{k}, t) = \frac{2}{(2\pi)^3} f^{\nu}(\boldsymbol{r}, \boldsymbol{k}, t)\mathrm{d}^3r\mathrm{d}^3k \,. \tag{39.1}$$

The factor $2/(2\pi)^3$ takes into account spin degeneracy and the minimum phase space volume of a particle [2]. To reduce the notational clutter, only the case for electrons is discussed. With the distribution function and a microscopic quantity $X^\nu(\boldsymbol{k})$, a macroscopic density (generalized moment of the distribution function) can be calculated by integration over the KS

$$x(\boldsymbol{r},t) = \frac{2}{(2\pi)^3}\sum_\nu \int X^\nu(\boldsymbol{k}) f^\nu(\boldsymbol{r},\boldsymbol{k},t)\mathrm{d}^3k\,. \tag{39.2}$$

The sum runs over all valleys of the conduction bands. $X^\nu(\boldsymbol{k}) = 1$ yields the electron density

$$n(\boldsymbol{r},t) = \frac{2}{(2\pi)^3}\sum_\nu \int f^\nu(\boldsymbol{r},\boldsymbol{k},t)\mathrm{d}^3k\,. \tag{39.3}$$

The particle current density

$$\boldsymbol{j}(\boldsymbol{r},t) = \frac{2}{(2\pi)^3}\sum_\nu \int \boldsymbol{v}_\nu(\boldsymbol{k}) f^\nu(\boldsymbol{r},\boldsymbol{k},t)\mathrm{d}^3k \tag{39.4}$$

is obtained with the group velocity

$$\boldsymbol{v}_\nu(\boldsymbol{k}) = \frac{1}{\hbar}\nabla_{\boldsymbol{k}}\varepsilon_\nu(\boldsymbol{k})\,, \tag{39.5}$$

where $\varepsilon_\nu(\boldsymbol{k})$ is the band energy, which is assumed to be position independent, and $\hbar$ is the reduced Planck constant. The more general case of a position-dependent band structure is not discussed here and is described in Jungemann and Meinerzhagen [12, 30] and the references therein. If only the band or valley minima depend on the position, this dependence can be easily included by adding the corresponding potential energy to the quasi-stationary potential [12].

The distribution function is the solution of the BTE [8,34]

$$\left\{\frac{\partial}{\partial t} - \frac{e}{\hbar}\boldsymbol{E}\cdot\nabla_{\boldsymbol{k}} + \boldsymbol{v}\cdot\nabla_{\boldsymbol{r}}\right\} f = \mathcal{W}\,. \tag{39.6}$$

e is the magnitude of the electron charge and $\boldsymbol{E}(\boldsymbol{r},t)$ the electric field. The scattering integral

$$\begin{aligned}\mathcal{W}^\nu(\boldsymbol{r},\boldsymbol{k},t) = \frac{\Omega_{\mathrm{sys}}}{(2\pi)^3}\sum_\eta\sum_{\nu'}\int &\left[1 - f^\nu(\boldsymbol{r},\boldsymbol{k})\right] \\ &\times W_\eta^{\nu,\nu'}(\boldsymbol{r},\boldsymbol{k},\boldsymbol{k}') f^{\nu'}(\boldsymbol{r},\boldsymbol{k}') \\ &- \left[1 - f^{\nu'}(\boldsymbol{r},\boldsymbol{k}')\right] W_\eta^{\nu',\nu}(\boldsymbol{r},\boldsymbol{k}',\boldsymbol{k}) f^\nu(\boldsymbol{r},\boldsymbol{k})\,\mathrm{d}^3k'\end{aligned} \tag{39.7}$$

describes the scattering of particles into the state $\nu,\boldsymbol{k}$ and out of it. Ω_{sys} is the system volume and $W_\eta^{\nu,\nu'}(\boldsymbol{r},\boldsymbol{k},\boldsymbol{k}')$ the transition rate for scattering from state $\nu',\boldsymbol{k}'$ into $\nu,\boldsymbol{k}$ owing to scattering process η, of which the rate is calculated by Fermi's golden rule [2, 8].

The BTE is a partial differential equation that requires boundary conditions. At the surfaces of the semiconductor region, which belong to contacts, the distribution function of the inflowing particles is given by the equilibrium distribution function [35]. If $\boldsymbol{r}_i^{\mathrm{cont}}$ is a vector in the surface region of the ith contact and $\boldsymbol{n}$ a vector, which is normal to the surface and points into the semiconductor region, the condition

$$\boldsymbol{n}\left(\boldsymbol{r}_i^{\mathrm{cont}}\right)\cdot\boldsymbol{v}_\nu(\boldsymbol{k}_\nu) > 0 \tag{39.8}$$

selects all wave vectors, which represent states of inflowing particles. Only for these wave vectors is the distribution function given by the equilibrium distribution function, and the total flux through the boundary $\boldsymbol{n}\cdot\boldsymbol{J}$ is given by

$$\begin{aligned}&\boldsymbol{n}\left(\boldsymbol{r}_i^{\mathrm{cont}}\right)\cdot\boldsymbol{J}^\nu\left(\boldsymbol{r}_i^{\mathrm{cont}},\boldsymbol{k},t\right) \\ &\quad= \boldsymbol{v}_\nu(\boldsymbol{k}) f^\nu\left(\boldsymbol{r}_i^{\mathrm{cont}},\boldsymbol{k},t\right)\Theta\left[-\boldsymbol{n}\left(\boldsymbol{r}_i^{\mathrm{cont}}\right)\cdot\boldsymbol{v}_\nu(\boldsymbol{k})\right] \\ &\qquad+\boldsymbol{v}_\nu(\boldsymbol{k}) f^{\mathrm{eq},\nu}\left(\boldsymbol{r}_i^{\mathrm{cont}},\boldsymbol{k}\right)\Theta\left[\boldsymbol{n}\left(\boldsymbol{r}_i^{\mathrm{cont}}\right)\cdot\boldsymbol{v}_\nu(\boldsymbol{k})\right]\,.\end{aligned} \tag{39.9}$$

$\Theta(x)$ is the Heaviside function. The first part of the right-hand side (RHS) is the flux leaving the device, which depends on the distribution function within the device, and the second term describes the flux entering the device owing to a contact at equilibrium [30, 35]. At equilibrium the current density should be zero in the whole device and the Fermi levels of the distribution functions of the inflowing particles are chosen accordingly. On all other parts of the semiconductor surface, it is assumed that the particle flux through the surface is zero.

The electric field $\boldsymbol{E}(\boldsymbol{r},t)$ is the gradient of the quasi-stationary potential $\Psi(\boldsymbol{r},t)$

$$\boldsymbol{E} = -\nabla_{\boldsymbol{r}}\Psi\,, \tag{39.10}$$

which is the solution of the Poisson equation (PE) [36]

$$\nabla_{\boldsymbol{r}}\cdot\left[\kappa\nabla_{\boldsymbol{r}}\Psi\right] = -e\left(p - n + N_{\mathrm{D}} - N_{\mathrm{A}}\right)\,. \tag{39.11}$$

κ is the permittivity, p the hole density, N_{D} the donor concentration, and N_{A} the acceptor concentration. On all interfaces the potential and the normal electric flux density must be continuous. On contacts, Dirichlet boundary conditions are applied to the potential

$$\Psi = V_i + \Phi_{\mathrm{MS}}\,. \tag{39.12}$$

V_i is the bias applied to the ith contact and Φ_{MS} the metal–semiconductor work function difference [37]. On all other parts of the surface of the device, the component of the electric flux density perpendicular to the surface must vanish.

39.2.2 Spherical Harmonics Expansion

The phase space has six dimensions and is difficult to discretize directly. If the problem is translation-invariant in the real space for one or two dimensions, the dimensionality can be reduced accordingly. But even a problem with five or four dimensions requires a very large number of grid nodes. By expanding the angular dependence of the distribution function in the KS into a spherical harmonics series, the dimensionality can be reduced further [23, 38, 39]. In many cases this expansion converges rapidly and it can be truncated at a low order [39, 40].

A real spherical harmonic of degree $l \geq 0$ and order m with $-l \leq m \leq l$ is given by [41]

$$Y_{l,m}(\theta,\phi) = \begin{cases} c_{l,m} P_{l,m}(\cos\theta)\cos(m\phi) & \text{for } m \geq 0 \\ c_{l,m} P_{l,m}(\cos\theta)\sin(|m|\phi) & \text{for } m < 0 \end{cases} \tag{39.13}$$

with

$$c_{l,m} = \begin{cases} \sqrt{\frac{(2l+1)}{4\pi}} & \text{for } m = 0 \\ \sqrt{\frac{(2l+1)(l-|m|)!}{2\pi(l+|m|)!}} & \text{for } m \neq 0 \end{cases} . \tag{39.14}$$

The associated Legendre polynomial

$$P_{l,m}(x) = \left(1-x^2\right)^{\frac{m}{2}} \frac{\mathrm{d}^m}{\mathrm{d}x^m} P_l(x) \tag{39.15}$$

is related to the Legendre polynomial

$$P_l(x) = \frac{1}{2^l l!} \frac{\mathrm{d}^l}{\mathrm{d}x^l} \left(x^2-1\right)^l . \tag{39.16}$$

The first four spherical harmonics are

$$Y_{0,0} = \frac{1}{\sqrt{4\pi}} \tag{39.17}$$

$$Y_{1,1} = \sqrt{\frac{3}{4\pi}} \sin\theta\cos\phi \tag{39.18}$$

$$Y_{1,-1} = \sqrt{\frac{3}{4\pi}} \sin\theta\sin\phi \tag{39.19}$$

$$Y_{1,0} = \sqrt{\frac{3}{4\pi}} \cos\theta \tag{39.20}$$

The spherical harmonics form a complete set of orthonormal functions with respect to integration over the unit sphere

$$\oint Y_{l,m}(\theta,\phi) Y_{l',m'}(\theta,\phi)\mathrm{d}\Omega \tag{39.21}$$

$$\begin{aligned} &= \int_0^{2\pi}\int_0^{\pi} Y_{l,m}(\theta,\phi) Y_{l',m'}(\theta,\phi)\sin\theta \mathrm{d}\theta\mathrm{d}\phi \\ &= \delta_{l,l'}\delta_{m,m'} . \end{aligned}$$

$\delta_{i,j}$ is the Kronecker symbol.

A function that depends on the two angles of the spherical coordinates, can be projected onto spherical harmonics by

$$X_{l,m} = \oint X(\theta,\phi) Y_{l,m}(\theta,\phi)\mathrm{d}\Omega . \tag{39.22}$$

The corresponding SHE of the function is

$$\begin{aligned} X(\theta,\phi) &= \sum_{l=0}^{\infty}\sum_{m=-l}^{m=l} X_{l,m} Y_{l,m}(\theta,\phi) \\ &\approx \sum_{l=0}^{l_{\max}}\sum_{m=-l}^{m=l} X_{l,m} Y_{l,m}(\theta,\phi) , \end{aligned} \tag{39.23}$$

which is truncated at the maximum expansion order $l_{\max}$.

With $X(\theta,\phi) = Y_{l,m}(\theta,\phi) Y_{l',m'}(\theta,\phi)$ products of spherical harmonics can be expanded

$$a^{l,m}_{l',m',l'',m''} = \oint Y_{l,m} Y_{l',m'} Y_{l'',m''}\mathrm{d}\Omega . \tag{39.24}$$

The basis vector in radial direction of the KS can be expressed with spherical harmonics

$$\begin{aligned} \boldsymbol{e}_r(\theta,\phi) &= \begin{pmatrix} \sin\theta\cos\phi \\ \sin\theta\sin\phi \\ \cos\theta \end{pmatrix} \\ &= \sqrt{\frac{4\pi}{3}} \begin{pmatrix} Y_{1,1}(\theta,\phi) \\ Y_{1,-1}(\theta,\phi) \\ Y_{1,0}(\theta,\phi) \end{pmatrix} \end{aligned} \tag{39.25}$$

and its product with two spherical harmonics

$$\boldsymbol{a}^{l,m}_{l',m'} = \oint \boldsymbol{e}_r Y_{l,m} Y_{l',m'}\mathrm{d}\Omega = \boldsymbol{a}^{l',m'}_{l,m} \tag{39.26}$$

can be calculated by (39.24). The vector remains the same when the indices are interchanged. Another useful vector is obtained with the basis vectors in θ and ϕ directions

$$\boldsymbol{b}^{l,m}_{l',m'} = \oint \left(\boldsymbol{e}_\theta \frac{\partial Y_{l,m}}{\partial\theta} + \frac{\boldsymbol{e}_\phi}{\sin\theta} \frac{\partial Y_{l,m}}{\partial\phi} \right) Y_{l',m'}\mathrm{d}\Omega \tag{39.27}$$

with $\boldsymbol{b}^{0,0}_{l',m'} = 0$ for all l', m'. The two vectors satisfy [30]

$$2\boldsymbol{a}^{l,m}_{l',m'} = \boldsymbol{b}^{l,m}_{l',m'} + \boldsymbol{b}^{l',m'}_{l,m} . \tag{39.28}$$

Both vectors vanish for $|l - l'| \neq 1$. Thus, an even l couples only to an odd l' and vice versa.

For the boundary conditions of the BTE on contacts (39.10), two more expressions are required [30]:

$$D^{l,m}_{l',m'} = \oint \boldsymbol{e}_r \cdot \boldsymbol{n} \Theta(-\boldsymbol{e}_r \cdot \boldsymbol{n}) Y_{l,m} Y_{l',m'} \mathrm{d}\Omega$$
$$E^{l,m}_{l',m'} = \oint \boldsymbol{e}_r \cdot \boldsymbol{n} \Theta(\boldsymbol{e}_r \cdot \boldsymbol{n}) Y_{l,m} Y_{l',m'} \mathrm{d}\Omega \,. \quad (39.29)$$

$\boldsymbol{n}$ is a unit vector, which is perpendicular to the contact surface and points into the device.

For the sake of simplicity and legibility, it is assumed that the band structure is isotropic and depends only on the magnitude of the wave vector, where some full-band effects are included [42]:

$$\varepsilon_\nu(\boldsymbol{k}) = \varepsilon_\nu(k) \,. \quad (39.30)$$

Ellipsoidal valleys can be easily transformed into isotropic valleys by the Herring–Vogt transformation [43]. (The general case of full bands is discussed in Kosina et al., Jungemann et al., and Hong et al. [30, 40, 44, 45].) Assuming a monotonic relationship between the magnitude of the wave vector and the energy, a unique inversion of the relation is possible:

$$\boldsymbol{k} = \boldsymbol{k}_\nu(\varepsilon, \theta, \phi) = k_\nu(\varepsilon) \boldsymbol{e}_r(\theta, \phi) \quad (39.31)$$

and the energy can be used as a coordinate instead of the magnitude of the wave vector, where the two angles remain the same [44].

The distribution function is projected on the spherical equi-energy surfaces onto spherical harmonics [40]:

$$Z_\nu(\varepsilon) f^\nu_{l,m}(\boldsymbol{r}, \varepsilon, t) \quad (39.32)$$
$$= \frac{2}{(2\pi)^3} \int \delta(\varepsilon - \varepsilon_\nu(k)) Y_{l,m}(\theta, \phi) f^\nu(\boldsymbol{r}, \boldsymbol{k}, t) \mathrm{d}^3 k$$
$$= Z_\nu(\varepsilon) \oint Y_{l,m}(\theta, \phi) f^\nu(\boldsymbol{r}, \boldsymbol{k}_\nu(\varepsilon, \theta, \phi), t) \mathrm{d}\Omega$$

with the reduced density of states

$$Z_\nu(\varepsilon) = \frac{2}{(2\pi)^3} k^2_\nu(\varepsilon) \frac{\mathrm{d}k_\nu(\varepsilon)}{\mathrm{d}\varepsilon} \,. \quad (39.33)$$

This definition does not contain the usual integration over the unit sphere and is therefore smaller by a factor of 4π. The distribution function defined over the six-dimensional phase space is thus replaced by a generalized energy distribution function $Z_\nu(\varepsilon) f^\nu_{l,m}(\boldsymbol{r}, \varepsilon, t)$, which is defined over a four-dimensional space of energy and position and which has a finite number of components.

The macroscopic densities (39.2) are given with the energy distribution function by

$$x(\boldsymbol{r}, t) = \sum_{\nu,l,m} \int_0^\infty X^\nu_{l,m}(\varepsilon) Z_\nu(\varepsilon) f^\nu_{l,m}(\boldsymbol{r}, \varepsilon, t) \mathrm{d}\varepsilon \,. \quad (39.34)$$

The electron density is obtained with $X = 1 = \sqrt{4\pi} Y_{0,0}$ and $X_{l,m} = \sqrt{4\pi} \delta_{l,0} \delta_{m,0}$:

$$n(\boldsymbol{r}, t) = \sqrt{4\pi} \sum_\nu \int_0^\infty Z_\nu(\varepsilon) f^\nu_{0,0}(\boldsymbol{r}, \varepsilon, t) \mathrm{d}\varepsilon \quad (39.35)$$

and depends only on the lowest order of the distribution function, whereas the current density obtained with $X = \boldsymbol{v} = v\boldsymbol{e}_r$ involves only the first-order distribution functions:

$$\boldsymbol{j}(\boldsymbol{r}, t) = \sqrt{\frac{4\pi}{3}} \quad (39.36)$$
$$\times \sum_\nu \int_0^\infty v_\nu(\varepsilon) Z_\nu(\varepsilon) \begin{pmatrix} f^\nu_{1,1}(\boldsymbol{r}, \varepsilon, t) \\ f^\nu_{1,-1}(\boldsymbol{r}, \varepsilon, t) \\ f^\nu_{1,0}(\boldsymbol{r}, \varepsilon, t) \end{pmatrix} \mathrm{d}\varepsilon \,.$$

This is because of the assumption of a spherical band structure [40, 42].

The BTE is projected in a similar fashion

$$\frac{2}{(2\pi)^3} \int \delta(\varepsilon - \varepsilon_\nu(k)) Y_{l,m}(\theta, \phi) \{\mathrm{BTE}\} \mathrm{d}^3 k \,, \quad (39.37)$$

where arguments are suppressed as far as possible to improve legibility. The first term on the left-hand side (LHS) of Eq. (39.6) is given by

$$\frac{2}{(2\pi)^3} \int \delta(\varepsilon - \varepsilon_\nu(k)) Y_{l,m} \frac{\partial f^\nu}{\partial t} \mathrm{d}^3 k = \frac{\partial Z_\nu f^\nu_{l,m}}{\partial t} \,. \quad (39.38)$$

Integration by parts yields for the second term of the BTE

$$\frac{2}{(2\pi)^3} \int \delta(\varepsilon - \varepsilon_\nu(k)) Y_{l,m} \frac{e}{\hbar} \boldsymbol{E} \cdot \nabla_{\boldsymbol{k}} f^\nu \mathrm{d}^3 k$$
$$= e\boldsymbol{E} \cdot \oint \left[\frac{\partial \boldsymbol{v}_\nu Z_\nu f^\nu}{\partial \varepsilon} Y_{l,m} \right.$$
$$\left. - \frac{Z_\nu}{\hbar k_\nu} \left(\boldsymbol{e}_\theta \frac{\partial Y_{l,m}}{\partial \theta} + \frac{\boldsymbol{e}_\phi}{\sin\theta} \frac{\partial Y_{l,m}}{\partial \phi} \right) f^\nu \right] \mathrm{d}\Omega$$
$$= e \frac{\partial \boldsymbol{E} \cdot \boldsymbol{J}^\nu_{l,m}}{\partial \varepsilon} - \Gamma^\nu_{l,m} \quad (39.39)$$

with

$$\boldsymbol{J}^\nu_{l,m}(\varepsilon) = v_\nu(\varepsilon) Z_\nu(\varepsilon) \sum_{l',m'} \boldsymbol{a}^{l,m}_{l',m'} f^\nu_{l',m'}(\varepsilon) \quad (39.40)$$

and

$$\Gamma^{\nu}_{l,m}(\varepsilon) = \frac{e\boldsymbol{E}Z_{\nu}(\varepsilon)}{\hbar k_{\nu}(\varepsilon)} \cdot \sum_{l',m'} \boldsymbol{b}^{l,m}_{l',m'} f^{\nu}_{l',m'}(\varepsilon) \; . \tag{39.41}$$

The third term can be calculated along similar lines:

$$\frac{2}{(2\pi)^3} \int \delta\left(\varepsilon - \varepsilon_{\nu}(k)\right) Y_{l,m} \boldsymbol{v}_{\nu} \cdot \nabla_{\boldsymbol{r}} f^{\nu} \mathrm{d}^3 k = \nabla_{\boldsymbol{r}} \cdot \boldsymbol{J}^{\nu}_{l,m}. \tag{39.42}$$

For the scattering integral it is assumed in this chapter that the transition rate depends only on the scattering angle and not on all angles of the initial and final states. In addition, the energy transfer should be constant. This is the case, for example, for the scattering processes presented in Brunetti et al. [46] for silicon, which are widely used. The general case is discussed in Hong et al. [30]. With these assumptions the transition rate can be simplified:

$$\begin{aligned} W^{\nu,\nu'}(\boldsymbol{r},\boldsymbol{k},\boldsymbol{k}') = \frac{1}{\Omega_{\mathrm{sys}}} c^{\nu,\nu'}_{\eta}\left(\boldsymbol{r}, \varepsilon_{\nu}(\boldsymbol{k}), \cos\angle(\boldsymbol{k},\boldsymbol{k}')\right) \\ \times \delta(\varepsilon_{\nu}(\boldsymbol{k}) - \varepsilon_{\nu'}(\boldsymbol{k}') - \hbar\omega_{\eta}) \end{aligned} \tag{39.43}$$

where $\hbar\omega_{\eta}$ is the constant energy transfer of the ηth scattering process. The cosine of the scattering angle is given by

$$\begin{aligned} \cos\angle(\boldsymbol{k},\boldsymbol{k}') &= \boldsymbol{e}_r(\theta,\phi) \cdot \boldsymbol{e}_r(\theta',\phi') \\ &= \cos\theta\cos\theta' + \sin\theta\sin\theta'\cos(\phi-\phi') \; . \end{aligned} \tag{39.44}$$

With the addition theorem, the transition rate can be expressed by products of spherical harmonics [47]:

$$\begin{aligned} &c^{\nu,\nu'}_{\eta}\left(\boldsymbol{r}, \varepsilon_{\nu}(\boldsymbol{k}), \cos\angle(\boldsymbol{k},\boldsymbol{k}')\right) \\ &= \sum_{l=0}^{\infty} c^{\nu,\nu'}_{\eta,l}\left(\boldsymbol{r}, \varepsilon_{\nu}(\boldsymbol{k})\right) \sum_{m=-l}^{m=l} Y_{l,m}(\theta,\phi) Y_{l,m}(\theta',\phi') \end{aligned} \tag{39.45}$$

and

$$c^{\nu,\nu'}_{\eta,l}(\boldsymbol{r},\varepsilon) = 2\pi \int_{-1}^{1} P_l(x) c^{\nu,\nu'}_{\eta}(\boldsymbol{r},\varepsilon,x)\,\mathrm{d}x \tag{39.46}$$

is given by a projection onto Legendre polynomials.

The scattering integral is split into in- and out-scattering:

$$\mathcal{W}^{\nu}(\boldsymbol{r},\boldsymbol{k},t) = \mathcal{W}^{\mathrm{in},\nu}(\boldsymbol{r},\boldsymbol{k},t) - \mathcal{W}^{\mathrm{out},\nu}(\boldsymbol{r},\boldsymbol{k},t) \; . \tag{39.47}$$

Projection of in-scattering yields

$$\begin{aligned} \mathcal{W}^{\mathrm{in},\nu}_{l,m}(\boldsymbol{r},\varepsilon,t) = \sum_{\eta,\nu'} \Big[Z_{\nu}(\varepsilon) c^{\nu,\nu'}_{\eta,l}(\boldsymbol{r},\varepsilon) \\ \times Z_{\nu'}(\varepsilon - \hbar\omega_{\eta}) f^{\nu'}_{l,m}\left(\boldsymbol{r}, \varepsilon - \hbar\omega_{\eta}, t\right) \Big] \; , \end{aligned} \tag{39.48}$$

and for out-scattering the result is

$$\begin{aligned} \mathcal{W}^{\mathrm{out},\nu}_{l,m}(\boldsymbol{r},\varepsilon,t) &= \sum_{\eta,\nu'} \Big[Z_{\nu'}(\varepsilon + \hbar\omega_{\eta}) \\ &\quad \times c^{\nu',\nu}_{\eta,0}\left(\boldsymbol{r}, \varepsilon + \hbar\omega_{\eta}\right) Z_{\nu}(\varepsilon) \Big] f^{\nu}_{l,m}(\boldsymbol{r},\varepsilon,t) \\ &= S_{\nu}(\boldsymbol{r},\varepsilon) Z_{\nu}(\varepsilon) f^{\nu}_{l,m}(\boldsymbol{r},\varepsilon,t) \; , \end{aligned} \tag{39.49}$$

where the Pauli principle has been neglected for the sake of brevity. Inclusion of the Pauli principle is described in Hong et al. [30]. Scattering into and out of traps (e.g., Shockley–Read–Hall recombination) can be easily included in this formalism and is described in Jungemann, Piazza et al., and Rupp et al. [25, 48, 49].

The combination of all terms yields balance equations for the energy distribution function $Z_{\nu}(\varepsilon) f^{\nu}_{l,m}(\boldsymbol{r},\varepsilon,t)$:

$$\begin{aligned} \frac{\partial Z_{\nu} f^{\nu}_{l,m}}{\partial t} - e\boldsymbol{E} \cdot \frac{\partial \boldsymbol{J}^{\nu}_{l,m}}{\partial \varepsilon} + \Gamma^{\nu}_{l,m} \\ + \nabla_{\boldsymbol{r}} \cdot \boldsymbol{J}^{\nu}_{l,m} + S_{\nu} Z_{\nu} f^{\nu}_{l,m} = \mathcal{W}^{\mathrm{in},\nu}_{l,m} \; , \end{aligned} \tag{39.50}$$

where the different spherical harmonics couple owing to the sums in Eqs. (39.40) and (39.41) of the free-streaming operator, whereas the scattering integral does not lead to coupling because the Pauli principle was neglected.

The balance equations contain derivatives with respect to energy and position, which makes it difficult to stabilize the equations in the case of a device simulation. Different methods have been proposed (e.g., [39, 40]) and the most successful stabilization is based on a transformation onto the total energy (H-transform) [23, 24].

$$H_{\nu}(\boldsymbol{k},\boldsymbol{r},t) = \varepsilon_{\nu}(\boldsymbol{k}) - e\Psi(\boldsymbol{r},t) \; . \tag{39.51}$$

It changes the gradient with respect to position in the real space:

$$\nabla_{\boldsymbol{r}} \cdot \boldsymbol{J}(\boldsymbol{r},\varepsilon) = \nabla_{\boldsymbol{r}} \cdot \boldsymbol{J}(\boldsymbol{r},H) - e\nabla_{\boldsymbol{r}}\Psi \cdot \frac{\partial \boldsymbol{J}(\boldsymbol{r},H)}{\partial H} \tag{39.52}$$

and the time derivative [31]

$$\frac{\partial f(\varepsilon,t)}{\partial t} = \frac{\partial f(H,t)}{\partial t} - e\frac{\partial \Psi}{\partial t}\frac{\partial f(H,t)}{\partial H} \; . \tag{39.53}$$

This makes it possible to remove the derivative with respect to energy in the balance equations:

$$\begin{aligned} \frac{\partial Z_{\nu} f^{\nu}_{l,m}}{\partial t} - e\frac{\partial \Psi}{\partial t}\frac{\partial Z_{\nu} f^{\nu}_{l,m}}{\partial H} + \Gamma^{\nu}_{l,m} \\ + \nabla_{\boldsymbol{r}} \cdot \boldsymbol{J}^{\nu}_{l,m} + S_{\nu} Z_{\nu} f^{\nu}_{l,m} = \mathcal{W}^{\mathrm{in},\nu}_{l,m} \end{aligned} \tag{39.54}$$

at the cost of a new time derivative. All quantities now depend via $f^{\nu}_{l,m}(\boldsymbol{r}, H, t)$ on the total energy H, which is the new independent variable. In the case of a stationary system, the first two terms vanish and the free-streaming operator contains only a derivative with respect to position. The free-streaming term can be transformed with

$$\frac{\mathrm{d}v_\nu Z_\nu}{\mathrm{d}\varepsilon} = \frac{2Z_\nu}{\hbar k_\nu} \tag{39.55}$$

and (39.28) into

$$\nabla_{\boldsymbol{r}} \cdot \boldsymbol{J}^{\nu}_{l,m} + \Gamma^{\nu}_{l,m} = v_\nu Z_\nu \sum_{l',m'} \boldsymbol{a}^{l',m'}_{l,m} \cdot \nabla_{\boldsymbol{r}} f^{\nu}_{l',m'} \tag{39.56}$$
$$- \frac{e\boldsymbol{E}Z_\nu}{\hbar k_\nu} \cdot \sum_{l',m'} \boldsymbol{b}^{l',m'}_{l,m} f^{\nu}_{l',m'} \; .$$

The formula on the LHS is used in the case of an even l and the RHS in the case of an odd l [45]. This maximizes the dissipation of entropy [30], which means that the system of balance equations derived from the BTE is well posed [50].

The boundary conditions on the contacts describe the flux flowing into the device through the surface area of the contacts. Projection of (39.10) yields for the flux density at the contact

$$\boldsymbol{n} \cdot \boldsymbol{J}^{\nu}_{l,m} = v_\nu Z_\nu \sum_{l',m'} D^{l,m}_{l',m'}(\boldsymbol{n}) f^{\nu}_{l',m'} \tag{39.57}$$
$$+ v_\nu Z_\nu E^{l,m}_{0,0}(\boldsymbol{n}) f^{\mathrm{eq},\nu}_{0,0} \; .$$

As the unit vector $\boldsymbol{n}$, which is perpendicular to the surface, depends on the position on the surface, the coefficients $D^{l,m}_{l',m'}$ and $E^{l,m}_{0,0}$ have to be evaluated for the local $\boldsymbol{n}$.

The balance equations are mapped onto a grid in real and H space by the finite volume method (box integration) [51] (see also Sect. 39.4). This is described in detail in Hong et al. [30] and not repeated here. The SHE is terminated at a maximum order to obtain a system of equations with a finite size. The truncation error depends on the problem that is simulated and can be easily estimated by running simulations with different maximum expansion orders. In the case of quasi-ballistic transport, a rather high number of spherical harmonics is required, whereas strong scattering leads to a low value. As scattering depends on energy and the electric field on position, the necessary expansion order varies over phase space. In Rupp et al. [25] an adaptive scheme is presented, which minimizes the number of variables in the system by a truncation order that depends on the position in phase space.

The solution of the BTE must always be non-negative ($f^{\nu}(\boldsymbol{r}, \boldsymbol{k}, t) \geq 0$) and certain properties of the balance equations should reflect this. Owing to projection onto spherical harmonics, of which only the lowest order is non-negative, only the zeroth-order component of the distribution function $f^{\nu}_{0,0}(\boldsymbol{r}, H, t)$ has this property. The solution of the balance equations should also have this property. This is shown in Hong and Jungemann and Hong et al. [30,52] for the stationary case, an expansion up to the first order in spherical harmonics, and velocity randomizing scattering ($c^{\nu,\nu'}_{\eta,l}(\boldsymbol{r}, \varepsilon) = 0$ for $l > 0$). It turns out that this property, which is only shown for a first-order expansion, also improves the stability in the case of a higher-order expansion as shown by numerical experiments. On the other hand, certain important inelastic scattering processes (e.g., polar optical phonon scattering) are not velocity randomizing, and in this case it is no longer guaranteed that the zeroth-order SHE component is non-negative resulting in a less robust system of equations.

In contrast to the MC method, the SHE approach can be solved directly for the stationary case. The usual TCAD approaches (e.g., Gummel loop and Newton–Raphson iteration (see also Sect. 39.4) can be used to obtain a self-consistent solution of the BTE and PE. As the Jacobian matrix is available, extension to small-signal and noise analysis is straightforward [27,28,30], if the time derivative in (39.53) is treated as described in Ruić and Jungemann [31].

39.2.3 Results

Simulation results are presented for a homogeneous GaAs bulk system (0D real space), a silicon N^+NN^+ structure (1D real space), and a SiGe HBT (2D real space).

GaAs Bulk

Bulk simulations are used to investigate transport and noise properties of materials and to generate parameters for moments-based models (see also Sect. 39.3.1). In this case, a system homogeneous in the real space is assumed, with a constant electron density and electric field. The H-transform is not necessary in this case and a staggered grid in energy is used [40].

As an example, GaAs is investigated and the model is based on a band structure with three valley types (Γ, L, and X) with nonparabolic analytical dispersion relations and scattering by phonons, including polar optical ones, whereas impurity scattering is neglected, assuming a low donor concentration [53]. In Fig. 39.1 the total energy distribution function summed over all valleys

$$Zf(\varepsilon) = \sum_{\nu} Z_\nu(\varepsilon) f^{\nu}_{0,0}(\varepsilon) \tag{39.58}$$

is shown. The two humps in the energy distribution functions are due to the L and X valleys, which begin at higher energies

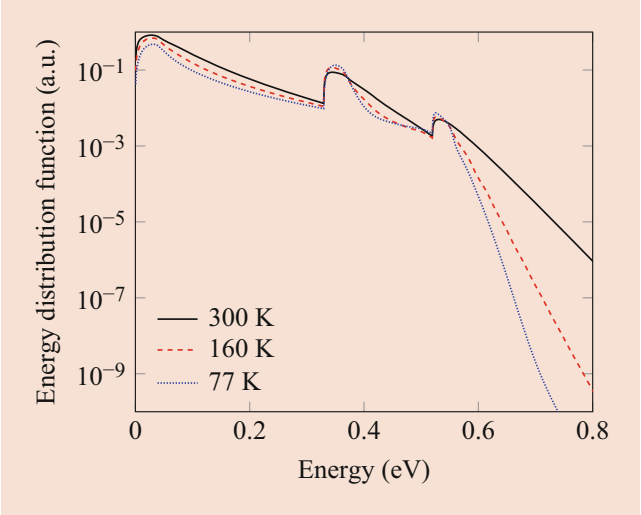

Fig. 39.1 Energy distribution function for GaAs at 77 K, 160 K, and 300 K and an electric field of 3 kV/cm

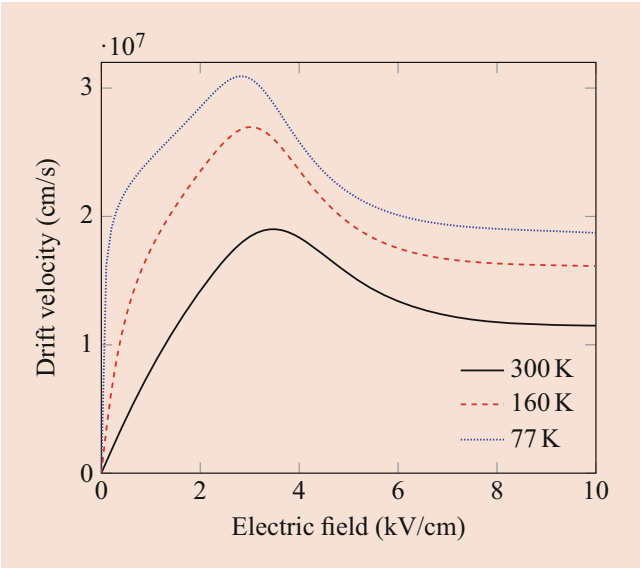

Fig. 39.2 Absolute value of the drift velocity in GaAs at different temperatures

than the Γ valley (0.33 eV and 0.52 eV respectively). The results show that with SHE, low values of the distribution function can be easily simulated, in contrast to MC.

In Fig. 39.2 the drift velocity is shown for GaAs in the limit of a low donor concentration. The drift velocity shows the usual stationary velocity overshoot due to transfer of electrons from the Γ valley into the L valleys (see Fig. 39.1), which have a higher mass [54].

A big advantage of the SHE method is that it can be easily extended to the case of small-signal analysis. With SHE the small-signal BTE can even be solved for plane waves as required for the analysis of plasma oscillations [55]. The small-signal distribution function is assumed to be harmonic in its dependence on time and position

$$\delta f^{\nu}(\boldsymbol{r},\boldsymbol{k},t) = \mathrm{Re}\left\{\underline{f}^{\nu}(\underline{\boldsymbol{q}},\boldsymbol{k},\underline{\omega})\exp\left(\mathrm{j}\underline{\omega}t - \mathrm{j}\underline{\boldsymbol{q}}\cdot\boldsymbol{r}\right)\right\} \quad (39.59)$$

$\underline{\omega}$ is the complex angular frequency, $\underline{\boldsymbol{q}}$ the complex wave vector, and $\underline{f}$ the phasor of the distribution function. Similar expressions are used for all other time- and position-dependent quantities. Under bulk conditions the small-signal BTE is given by

$$\left\{\mathrm{j}\underline{\omega} - \frac{e}{\hbar}\boldsymbol{E}_{\mathrm{DC}}\cdot\nabla_{\boldsymbol{k}} - \mathrm{j}\underline{\boldsymbol{q}}\cdot\boldsymbol{v}\right\}\underline{f} - \mathcal{W}\{\underline{f}\} \quad (39.60)$$
$$= \frac{e}{\hbar}\underline{\boldsymbol{E}}\cdot\nabla_{\boldsymbol{k}} f_{\mathrm{DC}}\,,$$

where $\boldsymbol{E}_{\mathrm{DC}}$ is the stationary electric field, f_{DC} the solution of the stationary BTE, and $\underline{\boldsymbol{E}}$ the phasor of the small-signal electric field. As the scattering integral is linear, the distribution function can be replaced by its phasor without any additional changes. The small-signal BTE can be projected onto spherical harmonics in the same way as the BTE. For the sake of simplicity it is assumed that the electric field and the wave vector are parallel:

$$\boldsymbol{E}_{\mathrm{DC}} = E_{\mathrm{DC}}\boldsymbol{n}\,,\quad \underline{\boldsymbol{E}} = \underline{E}\boldsymbol{n}\,,\quad \underline{\boldsymbol{q}} = \underline{q}\boldsymbol{n}\,. \quad (39.61)$$

In this case, the small-signal current is parallel to the electric field and a scalar small-signal mobility can be defined by

$$\underline{j} = en_{\mathrm{DC}}\underline{\mu}(\underline{\omega},\underline{q})\underline{E}\,. \quad (39.62)$$

This mobility definition corresponds at zero frequency and wave number to $\underline{\mu}(0,0) = -\mathrm{d}v/\mathrm{d}E$. In Fig. 39.3 the small-signal mobility is shown as a function of the real frequency and zero wave number at three electric fields and room temperature. For zero electric field the mobility can be described by a simple model with a single pole:

$$\underline{\mu}(\omega,0) \approx \frac{\underline{\mu}(0,0)}{1+\mathrm{j}\omega\tau_v}\,, \quad (39.63)$$

where τ_v is the macroscopic relaxation time of velocity. At higher electric fields transport is much more complex owing to the involvement of the different valleys and can no longer be described by a single pole. For an electric field of 3.47 kV/cm, the velocity peaks at room temperature (Fig. 39.2) and the small-signal mobility at zero frequency vanishes. At 5 kV/cm the derivative of the velocity-field relation is negative and the mobility is negative as well at zero frequency. This negative real part of the mobility could lead to instabilities (e.g., Gunn oscillations [56]). The

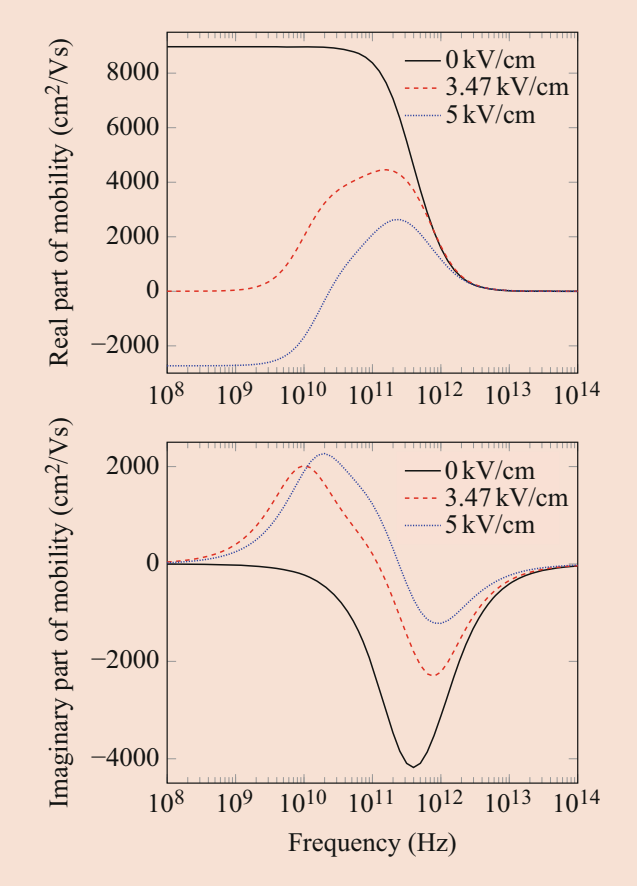

Fig. 39.3 Small-signal mobility for zero wave number ($q = 0$) and three electric fields at 300 K

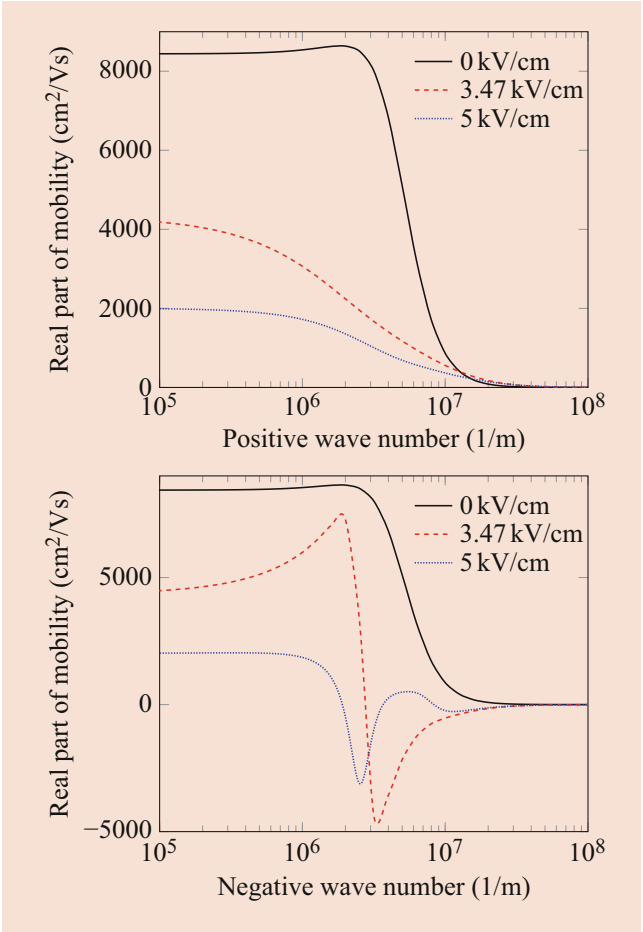

Fig. 39.4 Small-signal mobility for a frequency of 94 GHz and three electric fields at 300 K (upper graph, upstream; lower graph, downstream)

results clearly show that it is possible to cover the full range of technically relevant frequencies with SHE without any problems. Even zero frequency is feasible and very slow processes (e.g., deep traps) can be investigated [48,49].

In the case of a nonzero wave number, the mobility depends on the direction of the plasma wave. As electrons move into the negative direction of the electric field, a wave with a negative wave number travels into the same direction as the electrons, which is called "downstream." In the case of a positive wave number, it is "upstream." In Fig. 39.4 both cases are shown for a real frequency of 94 GHz and the real part of the mobility as a function of the wave number is different for positive and negative values. Only in the case of zero electric field, for which there is no electron flow, is the same result obtained. In the downstream case, negative real parts occur for nonzero electric field. This difference in the up- and downstream cases might induce instabilities in gated 2D plasmas with asymmetric boundary conditions [57]. In this case, both the frequency and the wave number are complex, which is extremely difficult to handle by the MC method and has not yet been attempted. This possibility of investigating the small-signal behavior in the complex frequency domain makes SHE the ideal tool for studying instabilities [58].

N^+NN^+ Structure

Transport in a silicon N^+NN^+ structure is investigated, where the six lowest minima of the conduction band (valleys) are considered by an analytical nonparabolic band structure and the phonon scattering processes described in Brunetti et al. [46] are included in the simulations. Scattering by ionized impurities is accounted for by the model presented in Brookes [59], where the scattering rate is modified in such a way that the measured mobility is reproduced at high donor concentrations [12].

In Fig. 39.5 the donor profile of the N^+NN^+ structure is shown, together with the electron density and potential at a bias of 0.5 V and room temperature. The donor concentration in the region between 200 and 300 nm is negligible and the contact regions are 200 nm long to ensure that the boundary conditions of the BTE have no impact

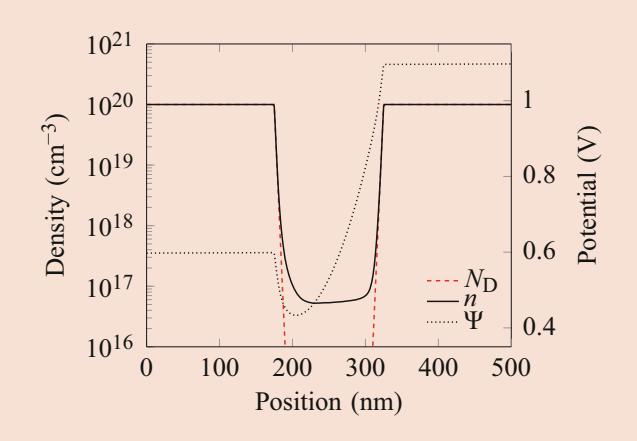

Fig. 39.5 Donor profile, electron density, and potential for the N^+NN^+ structure at a bias of 0.5 V

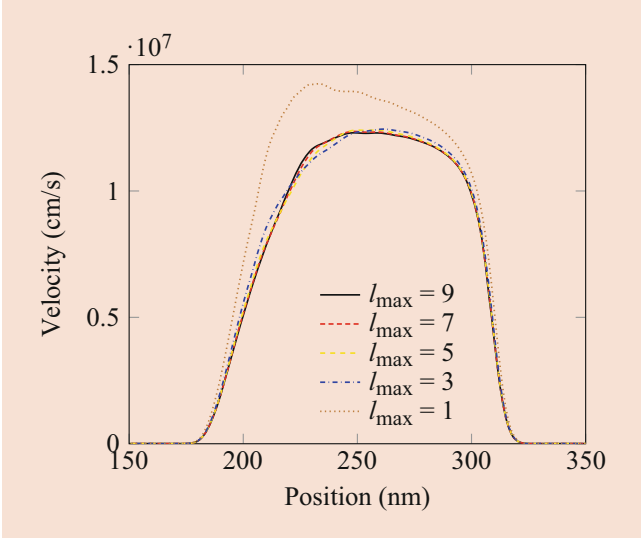

Fig. 39.6 Electron velocity for the N^+NN^+ structure at a bias of 0.5 V for different maximum expansion orders

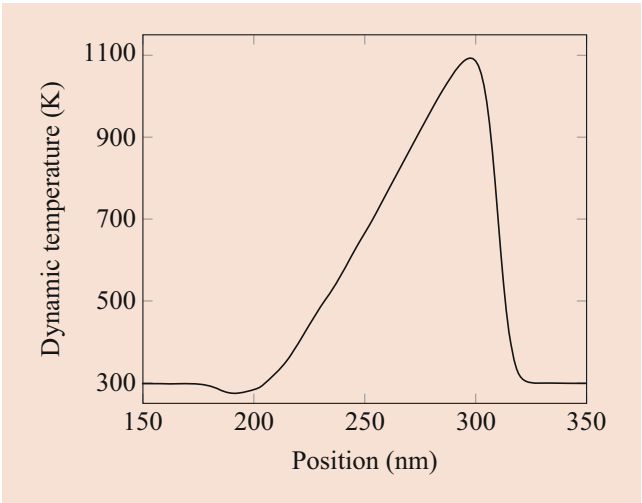

Fig. 39.7 Dynamic temperature for the N^+NN^+ structure at a bias of 0.5 V and a temperature of 300 K

on the results. An equidistant grid of 1.25 nm is used in the one-dimensional real space, and the energy grid has a fixed spacing of 5.17 meV and spans 1.24 eV. As transport in the ⟨100⟩ direction is simulated, two different sets of valleys (four degenerate valleys with the transverse mass in transport direction and two with the longitudinal ones) are considered. Owing to rotational symmetry with respect to the transport direction, only spherical harmonics with $m = 0$ are considered. For a SHE up to seventh order this results in 770,321 variables (401 grid nodes times 240 points in energy times 2 valley types times $(7+1)/2$ spherical harmonics plus 401 points for potential) and the CPU time is about 4000 s on a single core of a current processor. The simulation was started with a potential obtained by a DD model, and five Newton steps without any damping were sufficient to reduce the change in potential to 10^{-13} V. This small value shows that the combined BTE and PE are well-conditioned in this case.

The number of variables is proportional to the maximum expansion order and it should be as small as possible to save CPU time. In Fig. 39.6 the drift velocity is shown for different maximum orders of the SHE. The SHE clearly converges in this case and is by no means inferior to the MC method with respect to solving the BTE. Although an expansion up to first order introduces a large error, a third order seems to be sufficiently accurate compared with a ninth-order SHE. The error in current is for the third-order SHE 5.94%. To reduce this error below 1%, a seventh-order expansion is necessary (0.46%). The CPU efficiency of the SHE approach is much better than that of the MC method, even if the error due to the discrete energy grid is taken into account [48]. This is especially the case for internal variables (density, drift velocity, etc.). The high doping concentrations near the contacts do not lead to problems, in contrast to the MC method and no artificial heating of the particle gas is observed in Fig. 39.7, where the dynamic temperature is shown, which equals the lattice temperature near the contacts. The SHE simulations resolve without any problems in the electron gas cooling, when the electrons diffuse against the electric field before they pass the potential barrier at position 205 nm (see Fig. 39.5).

Transport models derived from the BTE by projection on moments of the distribution function require transport parameters. As an example the most basic transport parameters, the local mobility and diffusion constant, are discussed. With the microscopic relaxation time $\tau_\nu(\boldsymbol{k})$, which is the solution of the following integral equation [12, 60, 61]

$$\boldsymbol{v}_\nu(\boldsymbol{k}) = \frac{\Omega_{\mathrm{sys}}}{(2\pi)^3} \sum_\eta \sum_{\nu'} \int W_\eta^{\nu,\nu'}(\boldsymbol{r}, \boldsymbol{k}, \boldsymbol{k}') \times \left[\tau_\nu(\boldsymbol{k})\boldsymbol{v}_\nu(\boldsymbol{k}) - \tau_{\nu'}(\boldsymbol{k}')\boldsymbol{v}_{\nu'}(\boldsymbol{k}')\right] \mathrm{d}^3k' \,, \quad (39.64)$$

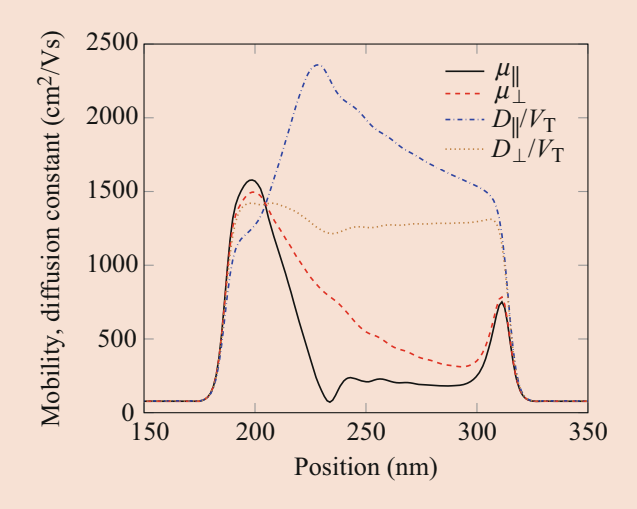

Fig. 39.8 Longitudinal and transverse mobilities and diffusion constants for the N^+NN^+ structure at a bias of 0.5 V and a temperature of 300 K. The diffusion constants are divided by the thermal voltage $V_T = 25.85\,\text{mV}$

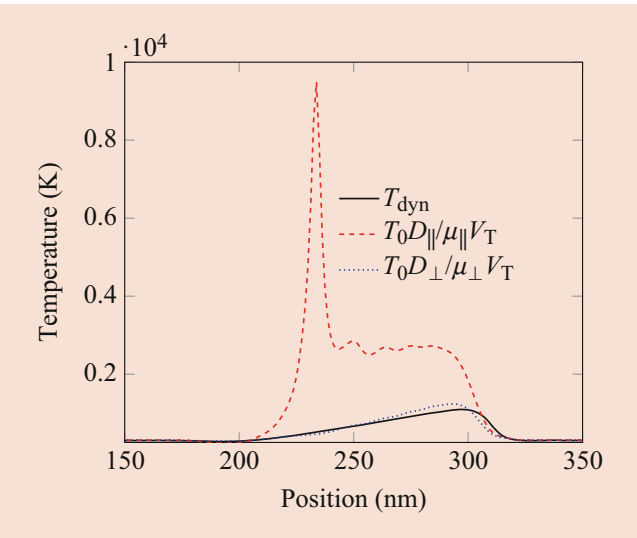

Fig. 39.9 Temperatures derived from the Einstein relation and the dynamic temperature for the N^+NN^+ structure at a bias of 0.5 V and a temperature of 300 K

the local mobility tensor can be exactly calculated:

$$\hat{\mu}(\boldsymbol{r},t) = \frac{1}{n(\boldsymbol{r},t)}\frac{2}{(2\pi)^3}\frac{e}{\hbar} \times \sum_\nu \int \nabla_{\boldsymbol{k}}\left[\tau_\nu(\boldsymbol{k})\boldsymbol{v}_\nu^{\mathrm{T}}(\boldsymbol{k})\right] f^\nu(\boldsymbol{r},\boldsymbol{k},t)\mathrm{d}^3k. \quad (39.65)$$

The diffusion tensor is obtained by

$$\hat{D}(\boldsymbol{r},t) = \frac{1}{n(\boldsymbol{r},t)}\frac{2}{(2\pi)^3} \times \sum_\nu \int \tau_\nu(\boldsymbol{k})\boldsymbol{v}_\nu(\boldsymbol{k})\boldsymbol{v}_\nu^{\mathrm{T}}(\boldsymbol{k}) f^\nu(\boldsymbol{r},\boldsymbol{k},t)\mathrm{d}^3k\,. \quad (39.66)$$

Both tensors are symmetric and in this one-dimensional case they have only two distinct elements, the longitudinal component for transport parallel to the transport direction and the transverse component for the perpendicular directions. They are shown in Fig. 39.8. In the regions with a very high electron density transport is close to equilibrium, the transport parameters are isotropic, and the Einstein relation between the diffusion constant and mobility holds. When the doping concentration drops, the mobilities and diffusion constants increase because of the reduced ionized impurity scattering. In the adjacent region with low electron density, the particle gas is in a strong non-equilibrium state and transport becomes anisotropic. Furthermore, the Einstein relation fails for longitudinal transport and the temperature defined by $D_\parallel/\mu_\parallel$ is very different from the dynamic temperature (Fig. 39.9), whereas for the transverse direction the Einstein relation roughly holds. In addition, the distribution function deviates very much from the simple form assumed to calculate the closure relation of the moments-based equations (e.g., drifted and heated Maxwellian), as shown in Fig. 39.10. Although near the left contact at 50 nm the energy distribution function is given by a Boltzmann distribution, it is very different at the position where the longitudinal temperature peaks (234 nm). At the peak of the dynamic temperature (297 nm), the distribution is very broad. Nevertheless, at high energies (>0.4 eV) the distribution function approaches the slope of the equilibrium distribution function and the distribution cannot be characterized by a single temperature. In the right contact region at 325 nm, the usual combination of a distribution of many cold electrons and a few hot ones is found.

The distribution of the electrons over the valleys is shown in Fig. 39.11. At equilibrium, each valley contains a fraction of 1/6 of all particles. When the electrons get hot, the energy gain in the valleys with the transverse mass parallel to the electric field is larger owing to the lower mass in this direction and the electrons scatter into the other valley type reducing the occupancy of these valleys. The mean free path of the electrons

$$\lambda(\boldsymbol{r},t) = \frac{1}{n(\boldsymbol{r},t)}\frac{2}{(2\pi)^3} \times \sum_\nu \int \tau_\nu(\boldsymbol{k})\,|\boldsymbol{v}_\nu(\boldsymbol{k})|\, f^\nu(\boldsymbol{r},\boldsymbol{k},t)\mathrm{d}^3k \quad (39.67)$$

must be small compared with the device dimensions for moments-based models to work. Owing to the strong scatter-

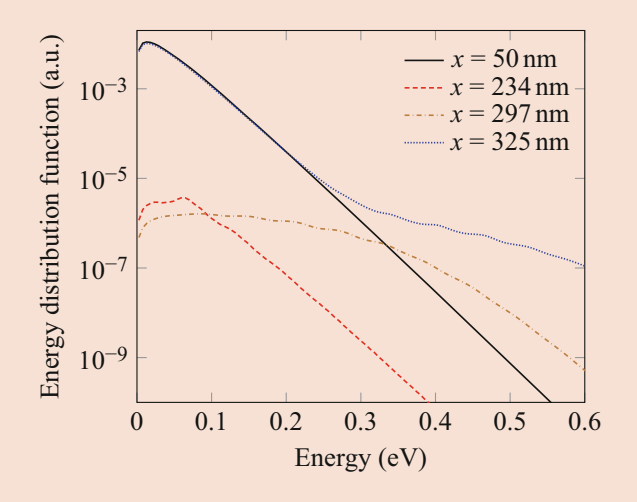

Fig. 39.10 Energy distribution function $Z_\nu(\varepsilon) f^\nu_{0,0}(\boldsymbol{r}, \varepsilon)$ for the valleys with longitudinal mass parallel to the transport direction for the N^+NN^+ structure at a bias of 0.5 V and a temperature of 300 K

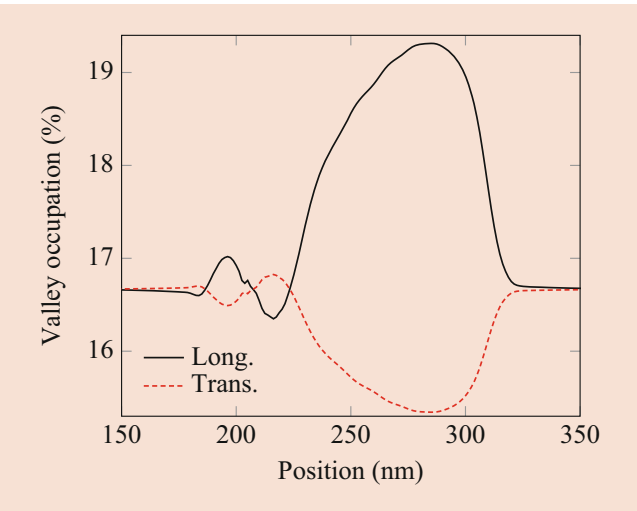

Fig. 39.11 Fraction of electrons in the valleys with longitudinal mass parallel to the transport direction and for the transverse direction for the N^+NN^+ structure at a bias of 0.5 V and a temperature of 300 K

ing by ionized impurities, this is the case near the contacts, but in the region with the low donor concentration, the mean free path becomes very large and of the same order as the length of the region. These results clearly show why it is difficult to model transport in nanoscale devices by moments-based models (Fig. 39.12).

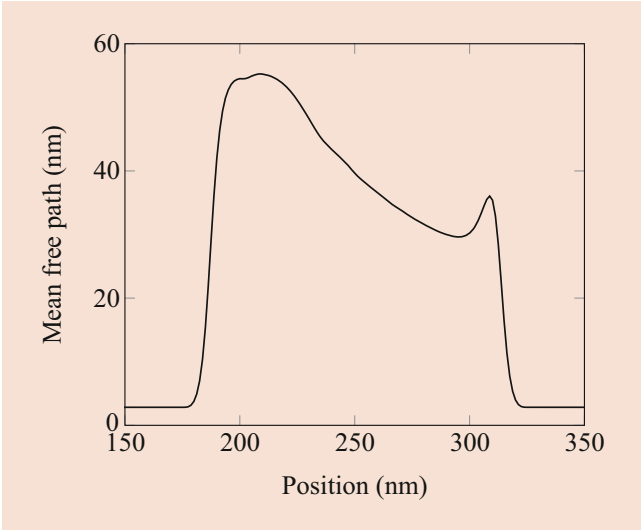

Fig. 39.12 Mean free path for the N^+NN^+ structure at a bias of 0.5 V and a temperature of 300 K

SiGe HBT

SiGe HBTs are a cost-efficient alternative to III–V transistors, which can be fabricated by silicon technologies and even integrated into CMOS circuits [62]. The fastest SiGe HBTs have cutoff and maximum oscillation frequencies above 500 GHz [63]. In Fig. 39.13 the doping and Ge profiles of an ultimate SiGe HBT are shown [33]. A corresponding symmetric 2D CBEBC structure with an emitter window of 50 nm in width is simulated at room temperature and self-heating effects are neglected [64]. The metallurgical base is about 7 nm thick and the peak acceptor concentration is $2.4 \cdot 10^{20}/\mathrm{cm}^3$. The Ge profile increases linearly from the emitter to the base to avoid an abrupt barrier in the out-of-plane valleys of the conduction band [30]. The peak Ge content is 30%. The 2D device structure is discretized by a non-uniform grid with 149 grid nodes in the vertical direction and 20 in the lateral direction. Owing to the assumption of translational invariance in the third dimension, only spherical harmonics with a non-negative m have to be considered in the fifth-order SHE. Three different sets of valleys are included in the simulation for the conduction band, whereas holes are simulated by a DD model. Scattering by phonons, ionized impurities, alloy fluctuations, and impact ionization are included in the simulations [30]. The BTE for electrons, the DD model for holes, and the PE are solved self-consistently by the Newton–Raphson method.

The Gummel plot of the transistor is shown in Fig. 39.14. Currents can be calculated over more than 12 orders of magnitude by SHE. The current gain is above 100 for base/emitter voltages below 0.95 V, at which the cutoff frequency peaks ($V_{\mathrm{CE}} = 1.0\,\mathrm{V}$). With SHE the ideality factor of the collector current can be calculated at a fixed collector/emitter bias by

$$n_{I_\mathrm{C}} = \frac{I_\mathrm{C}}{Y_{\mathrm{CB}}(0) V_\mathrm{T}} \,. \tag{39.68}$$

$Y_{\mathrm{CB}}(0) = \partial I_\mathrm{C}/\partial V_{\mathrm{BE}}$ is the collector/base admittance at zero frequency. At low base/emitter bias, the ideality factor is not

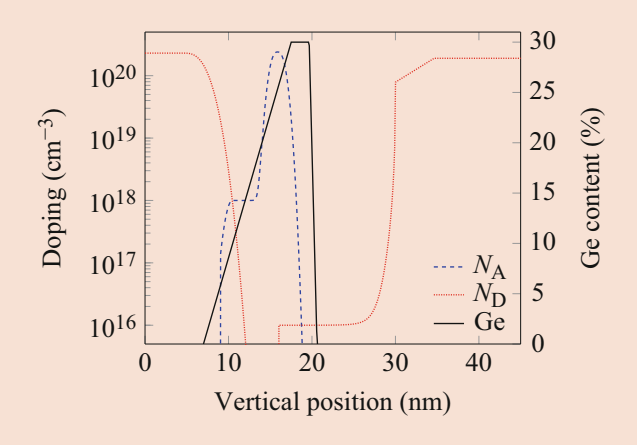

Fig. 39.13 Donor, acceptor, and Ge profiles along the vertical symmetry line of the SiGe HBT

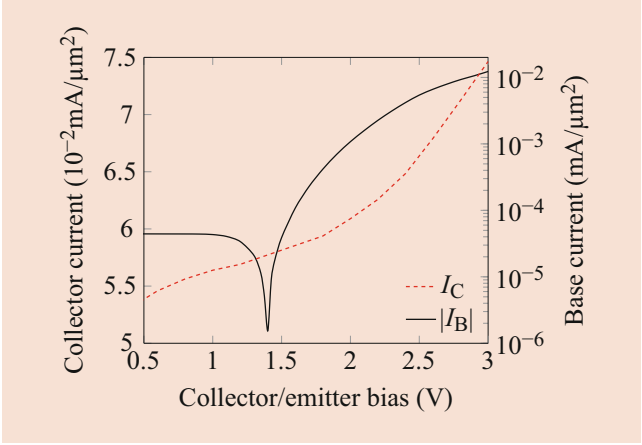

Fig. 39.15 Collector and base currents of the SiGe HBT at a base/emitter bias of 0.7 V

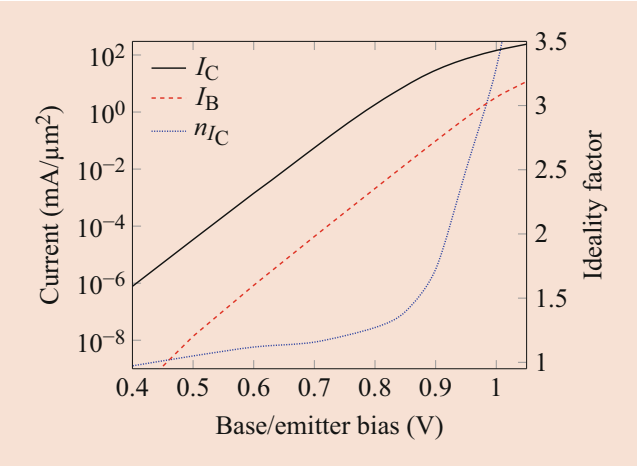

Fig. 39.14 Collector and base currents of the SiGe HBT at a collector/emitter bias of 1.0 V and the ideality factor

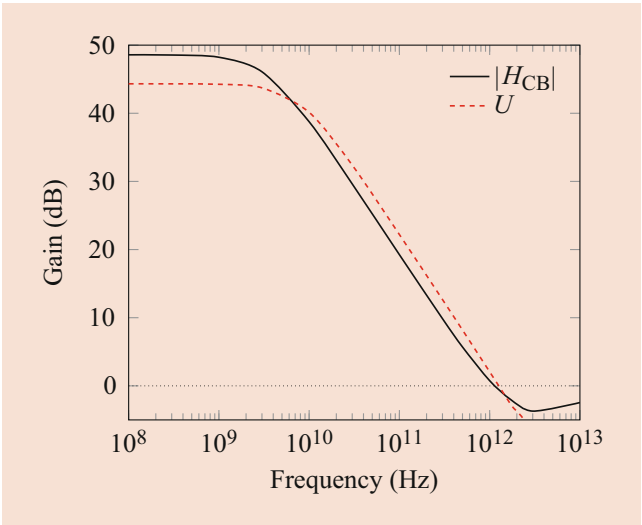

Fig. 39.16 Small-signal current gain (H_{CB}) and unilateral gain (U) at $V_{CE} = 1.0\,V$, $V_{BE} = 0.88\,V$

constant owing to the position-dependent band structure [65]. This quantity is very difficult to calculate using the MC method. Stochastic heating will lead to a reduced slope of the collector current and the stochastic error will make it very difficult to calculate the derivative at the required low current levels.

The collector and base currents at a base/emitter bias of 0.7 V are shown in Fig. 39.15 as a function of the collector/emitter voltage. The base current is positive up to $V_{CE} = 1.4\,V$ and then negative owing to the generation of holes by impact ionization. The collector/emitter breakdown voltage is defined as the bias for which the base current vanishes. In this case the breakdown voltage is $BV_{CE0} = 1.4\,V$, which is rather low and due to the thin low-doped collector. A thicker low-doped collector would increase the breakdown voltage at the cost of a lower cutoff frequency. The corresponding increase in the collector current due to feedback from the base current can lead to instability and is a major concern for the design of the safe operating area. The early voltage calculated at $V_{CE} = 1.0\,V$, $V_{BE} = 0.7\,V$ is $V_A = 16.7\,V$.

The cutoff frequency is defined as the frequency for which the magnitude of the small-signal current gain at a short-circuited output becomes one. In the common-emitter configuration, the small-signal gain is given by the hybrid parameter H_{CB}, which is shown in Fig. 39.16. At sufficiently high frequencies the gain drops with 20 dB/dec and the cutoff frequency can be estimated by extrapolation from its value at 300 GHz. Similarly, the maximum oscillation frequency can be calculated by extrapolation of the unilateral power gain. By this procedure, the cumbersome search for the frequency at which unit gain is obtained is avoided. The cutoff and maximum oscillation frequencies are shown in Fig. 39.17.

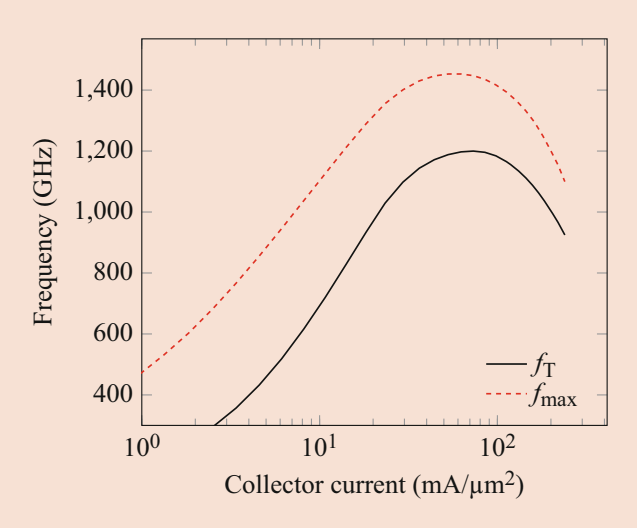

Fig. 39.17 Cutoff and maximum oscillation frequencies at $V_{CE} = 1.0\,V$

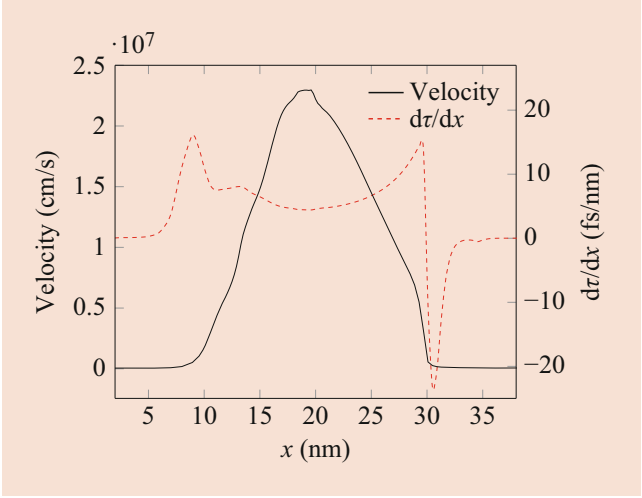

Fig. 39.18 Electron drift velocity and local contribution to the transit time ($d\tau/dx$) at $V_{CE} = 1.0\,V$, $V_{BE} = 0.885\,V$

The cutoff frequency peaks at 1.2 THz ($V_{BE} = 0.95\,V$) and the maximum frequency of oscillation at 1.45 THz.

The SHE approach allows the internal distributions to be investigated, and the drift velocity of the electrons is shown in Fig. 39.18. A strong velocity overshoot in the base of more than 100% is observed. This means that the thin base layer does not contribute much to the electron transit time of the device, which can be defined in the quasi-stationary limit and is inversely proportional to the cutoff frequency [66,67]. The local contribution to the transit time by the electrons is low in the base owing to the high velocity (Fig. 39.18) and the biggest contribution is due to the emitter/base space charge region. The large values at the junction between the low- and high-doped collector regions cancel to a certain degree. Thus, with SHE it is possible to get a detailed understanding of the processes that limit the speed of the transistor.

39.3 Multi-Scale Modeling

Multi-scale modeling is a vast field and remains very large, even if only applications for semiconductor devices are considered. Moreover, it is a scientific discipline with very fuzzy boundaries. Therefore, it is impossible to cite and describe all the methods that may fit within this framework. Consequently, this chapter relies mostly on the authors' experience and concentrates on methods that at least in the authors' opinion deserve to be named multi-scale models for semiconductor devices and which the authors helped to develop, at least to some extent. Concerning the defining terms in the field of multi-scale models, please refer to Weinan [68].

39.3.1 Sequential Multi-Scale Modeling

Sequential multi-scale modeling, as described in Weinan [68], typically starts with multi-scale analysis, which establishes a firm link between the models on the more microscopic scale, such as the BTE, and the models on the more macroscopic scale, such as the DD and HD equations. A typical example of a sequential multi-scale analysis is given below. At first, balance equations resulting from the BTE are derived, and HD and DD models are subsequently developed based on these balance equations. In this chapter, only the principles of such a derivation shall be shown. Therefore, the derivation is restricted to the case of electrons with a position-independent band structure. A generalization to the case of position-dependent band structures can be found in Jungemann and Meinerzhagen [12].

Balance Equations

Balance equations describe the behavior of macroscopic quantities $x(\boldsymbol{r}, t)$ as introduced in (39.2), which are averages over the KS, such as the electron density (39.3) or electron particle current density (39.4) [3,69–71]. These macroscopic quantities are closely related to expectation values introduced by the following equation for a scalar microscopic quantity X^ν:

$$x(\boldsymbol{r}, t) = n(\boldsymbol{r}, t)\,\langle X\rangle_{\boldsymbol{k}}\,(\boldsymbol{r}, t)\,, \tag{39.69}$$

where $n(\boldsymbol{r}, t)$ is the electron density and the subscript of the expectation value $\langle..\rangle_{\boldsymbol{k}}$ indicates that it is calculated over the KS (including the sum over the conduction bands). These expectation values are normalized because $\langle 1\rangle_{\boldsymbol{k}} = 1$. In the following the arguments ν, $\boldsymbol{r}$, $\boldsymbol{k}$, and t will be dropped as far as possible. In general, the current density $\boldsymbol{j}_X$ corresponding to the macroscopic quantity x reads

$$\boldsymbol{j}_X = n \langle X \boldsymbol{v} \rangle_{\boldsymbol{k}} \ , \tag{39.70}$$

where the microscopic quantity $\boldsymbol{v}_\nu$ is the group velocity, as introduced in (39.5). The balance equation for a given scalar microscopic quantity X^ν is obtained by integrating the BTE (39.6) multiplied by the microscopic quantity X^ν over the KS, as is done in (39.2) for X^ν alone. The first term on the left-hand side of the BTE (39.6) yields

$$\frac{2}{(2\pi)^3} \sum_\nu \int X^\nu(\boldsymbol{k}) \frac{\partial f^\nu(\boldsymbol{r}, \boldsymbol{k}, t)}{\partial t} \mathrm{d}^3 k = \frac{\partial x}{\partial t} \ . \tag{39.71}$$

The second term on the left-hand side is reformulated by the divergence theorem of Gauss based on the assumption that the distribution function is so small at the boundary of the KS that the integral along the boundary can be neglected:

$$\begin{aligned} &- \frac{2}{(2\pi)^3} \sum_\nu \int X^\nu(\boldsymbol{k}) \boldsymbol{E}(\boldsymbol{r}, t) \cdot \frac{e}{\hbar} \nabla_{\boldsymbol{k}} f^\nu(\boldsymbol{r}, \boldsymbol{k}, t) \mathrm{d}^3 k \\ &\quad = n \left\langle \boldsymbol{E} \cdot \frac{e}{\hbar} \nabla_{\boldsymbol{k}} X \right\rangle_{\boldsymbol{k}} \ . \end{aligned} \tag{39.72}$$

The last term on the left-hand side yields

$$\frac{2}{(2\pi)^3} \sum_\nu \int X^\nu(\boldsymbol{k}) \boldsymbol{v}_\nu(\boldsymbol{k}) \cdot \nabla_{\boldsymbol{r}} f^\nu(\vec{r}, \vec{k}, t) \mathrm{d}^3 k \ = \ \nabla_{\boldsymbol{r}} \cdot \boldsymbol{j}_X \ . \tag{39.73}$$

For the scattering integral on the right-hand side, the Pauli exclusion principle is neglected, resulting in

$$\begin{aligned} &\frac{2}{(2\pi)^3} \sum_\nu \int X^\nu(\boldsymbol{k}) \frac{\Omega_{\mathrm{sys}}}{(2\pi)^3} \\ &\quad \sum_\eta \sum_{\nu'} \int \left(W_\eta^{\nu,\nu'}(\boldsymbol{r}, \boldsymbol{k}, \boldsymbol{k}', t) f^{\nu'}(\boldsymbol{r}, \boldsymbol{k}', t) \right. \\ &\quad \left. - W_\eta^{\nu',\nu}(\boldsymbol{r}, \boldsymbol{k}', \boldsymbol{k}, t) f^{\nu}(\boldsymbol{r}, \boldsymbol{k}, t) \right) \mathrm{d}^3 k' \mathrm{d}^3 k \\ &= -n \left\langle \frac{\Omega_{\mathrm{sys}}}{(2\pi)^3} \sum_\eta \sum_{\nu'} \int W_\eta^{\nu',\nu}(\boldsymbol{r}, \boldsymbol{k}', \boldsymbol{k}, t) \left(X^\nu(\boldsymbol{k}) - X^{\nu'}(\boldsymbol{k}') \right) \mathrm{d}^3 k' \right\rangle_{\boldsymbol{k}} \ . \end{aligned} \tag{39.74}$$

With the abbreviation

$$S\{X\} = \frac{\Omega_{\mathrm{sys}}}{(2\pi)^3} \sum_\eta \sum_{\nu'} \int W_\eta^{\nu',\nu}(\boldsymbol{r}, \boldsymbol{k}', \boldsymbol{k}, t) \left(X^\nu(\boldsymbol{k}) - X^{\nu'}(\boldsymbol{k}') \right) \mathrm{d}^3 k' \tag{39.75}$$

the final balance equation is obtained:

$$\frac{\partial x}{\partial t} + n \boldsymbol{E} \cdot \left\langle \frac{e}{\hbar} \nabla_{\boldsymbol{k}} X \right\rangle_{\boldsymbol{k}} + \nabla_{\boldsymbol{r}} \cdot \boldsymbol{j}_X = -n \langle S\{X\} \rangle_{\boldsymbol{k}} \ . \tag{39.76}$$

Each balance equation of the type (39.76) not only contains the density $x(\boldsymbol{r}, t)$ but also the corresponding current density $\boldsymbol{j}_X(\boldsymbol{r}, t)$. Moreover, for an exact calculation of the expectation values the complete knowledge of the distribution function is typically required. Therefore, it is not possible to derive a finite set of balance equations with the property of having a unique solution without introducing further simplifying assumptions. In particular, the exact calculation of the expectation of the collision integral requires the full information of the distribution function. In the case of certain balance equations, the latter problem can be circumvented with the microscopic relaxation time [69]. However, for the general case, the macroscopic relaxation time approximation has to be used:

$$\langle S\{X\} \rangle_{\boldsymbol{k}} \approx \frac{\langle X \rangle_{\boldsymbol{k}} - \langle X \rangle_{\boldsymbol{k}}^{\mathrm{eq}}}{\tau_X} \ , \tag{39.77}$$

where $\langle \rangle_{\boldsymbol{k}}^{\mathrm{eq}}$ is the expectation in the case of thermodynamic equilibrium. The collision integral and the above approximation both vanish at thermodynamic equilibrium. Therefore, without further restrictions concerning the macroscopic relaxation time τ_X, the above equation could even be exact. The approximation is introduced by the fact that the macroscopic relaxation times are assumed to be functions of a finite set of macroscopic densities only [71].

Hierarchical Hydrodynamic Model

The solution of the BTE is very CPU intensive, irrespective of the solution algorithm (MC or SHE) used. Therefore, less accurate but more CPU-efficient numerical models based on balance equations have been developed. The most widely used models of this type are the DD and the hydrodynamic (HD) models [37,69–79]. Both models are derived by applying different degrees of approximation to balance equations of the type (39.76). Owing to the integration over the $\boldsymbol{k}$-space, the dimensionality of the problem is reduced and the CPU efficiency improves by orders of magnitude. For the HD model, four different balance equations are considered, which result from the four microscopic quantities 1, $\boldsymbol{v}$, ε, and $\varepsilon \boldsymbol{v}$, and relate on the macroscopic level to the electron density, electron particle current density, electron energy density, and the electron energy current density:

$$n = n \langle 1 \rangle_{\boldsymbol{k}} \ , \tag{39.78}$$

$$\boldsymbol{j}_{\mathrm{n}} = n \langle \boldsymbol{v} \rangle_{\boldsymbol{k}} \ , \tag{39.79}$$

$$w_{\mathrm{n}} = n \langle \varepsilon \rangle_{\boldsymbol{k}} \ , \tag{39.80}$$

$$\boldsymbol{s}_{\mathrm{n}} = n \langle \varepsilon \boldsymbol{v} \rangle_{\boldsymbol{k}} \ . \tag{39.81}$$

Such a reduced set of equations still enables the simulation of nonlocal effects, such as the velocity overshoot, that have a strong impact on the behavior of modern devices with

nanometer dimensions. The remaining model derivation presented in this section leads to the generalized HD model and follows closely the arguments outlined in [71]. First, the HD model for electrons is derived and then the results for the hole model are added. With Eq. (39.76) and $X = 1$ the electron continuity equation is obtained without approximations:

$$\nabla_{\boldsymbol{r}} \cdot \boldsymbol{j}_{\mathrm{n}} + \frac{\partial n}{\partial t} = 0 \,. \tag{39.82}$$

Here, generation-recombination processes are neglected for the sake of brevity.

The balance equation for the electron particle current density is derived with the macroscopic relaxation time approximation (39.77) and by choosing $X = v_x$, $X = v_y$, and $X = v_z$, where v_x, v_y, and v_z are the components of $\boldsymbol{v}$ in a Cartesian coordinate system. Combining the resulting three scalar equations into one vector equation yields the balance equation for the current density

$$\frac{\partial \boldsymbol{j}_{\mathrm{n}}}{\partial t} + e\, n \left\langle \hat{m}^{-1} \right\rangle_{\boldsymbol{k}} \boldsymbol{E} + \left(\nabla_{\boldsymbol{r}}^{\mathrm{T}} \left[n \left\langle \boldsymbol{v} \boldsymbol{v}^{\mathrm{T}} \right\rangle_{\boldsymbol{k}} \right] \right)^{\mathrm{T}} = -\frac{\boldsymbol{j}_{\mathrm{n}}}{\tau_{j_{\mathrm{n}}}}, \tag{39.83}$$

where the inverse mass tensor is given by

$$\hat{m}_{\nu}^{-1}(\boldsymbol{k}) = \frac{1}{\hbar^2} \nabla_{\boldsymbol{k}} \nabla_{\boldsymbol{k}}^{\mathrm{T}} \varepsilon_{\nu}(\boldsymbol{k}) \,. \tag{39.84}$$

The last balance equation contains two tensor quantities, which are replaced by scalar approximations.

$$\left\langle \hat{m}^{-1} \right\rangle_{\boldsymbol{k}} \approx \frac{\mathrm{Tr} \left\langle \hat{m}^{-1} \right\rangle_{\boldsymbol{k}}}{3} \hat{I} \,, \tag{39.85}$$

$$\left\langle \boldsymbol{v} \boldsymbol{v}^{\mathrm{T}} \right\rangle_{\boldsymbol{k}} \approx \frac{\left\langle \boldsymbol{v}^2 \right\rangle_{\boldsymbol{k}}}{3} \hat{I} \,, \tag{39.86}$$

where $\hat{I}$ is the unity tensor. Owing to the symmetry properties of the dispersion relations and the distribution function for situations close to thermodynamic equilibrium, these approximations are nearly exact close to equilibrium for typical semiconductor materials such as unstrained silicon. Moreover, the dynamic electron temperature $T_{\mathrm{n}}^{\star}$ is introduced by

$$\frac{3}{2} k_{\mathrm{B}} T_{\mathrm{n}}^{\star} = \frac{1}{2} m_{\mathrm{n}}^{\star} \left\langle \boldsymbol{v}^2 \right\rangle_{\boldsymbol{k}} \,, \tag{39.87}$$

where the mass $m_{\mathrm{n}}^{\star}$ is calculated for thermodynamic equilibrium

$$\frac{1}{m_{\mathrm{n}}^{\star}} = \frac{\left\langle \boldsymbol{v}^2 \right\rangle_{\boldsymbol{k}}^{\mathrm{eq}}}{3 k_{\mathrm{B}} T_0} \,, \tag{39.88}$$

and T_0 is the lattice temperature. Thus, under equilibrium conditions the dynamic temperature equals the lattice temperature. In addition, the approximation of the inverse mass tensor is absorbed by the introduction of a new relaxation time $\tau_{j_{\mathrm{n}}}^{*}$:

$$\frac{\mathrm{Tr} \left\langle \hat{m}^{-1} \right\rangle_{\boldsymbol{k}}}{3} \tau_{j_{\mathrm{n}}} = \frac{\tau_{j_{\mathrm{n}}}^{*}}{m_{\mathrm{n}}^{\star}}. \tag{39.89}$$

With these approximations, the final current balance equation is obtained:

$$\boldsymbol{j}_{\mathrm{n}} + \tau_{j_{\mathrm{n}}} \frac{\partial \boldsymbol{j}_{\mathrm{n}}}{\partial t} = -n \frac{e\, \tau_{j_{\mathrm{n}}}^{*}}{m_{\mathrm{n}}^{\star}} \boldsymbol{E} - \frac{\tau_{j_{\mathrm{n}}}}{m_{\mathrm{n}}^{\star}} \nabla_{\boldsymbol{r}} \left(n k_{\mathrm{B}} T_n^{\star} \right) . \tag{39.90}$$

Thus, the diffusion constant is given by a generalized Einstein relation [71]:

$$D = \frac{\tau_{j_{\mathrm{n}}} k_{\mathrm{B}} T_{\mathrm{n}}^{\star}}{m_{\mathrm{n}}^{\star}} = \underbrace{\frac{e \tau_{j_{\mathrm{n}}}^{*}}{m_{\mathrm{n}}^{\star}}}_{=\mu} \frac{\tau_{j_{\mathrm{n}}}}{\tau_{j_{\mathrm{n}}}^{*}} \underbrace{\frac{k_{\mathrm{B}} T_{\mathrm{n}}^{\star}}{e}}_{=V_{T_{\mathrm{n}}^{\star}}} = \mu V_{T_{\mathrm{n}}^{\star}} \frac{\tau_{j_{\mathrm{n}}}}{\tau_{j_{\mathrm{n}}}^{*}}, \tag{39.91}$$

where the thermal voltage is evaluated with the dynamic temperature of the particle gas instead of the lattice temperature. At equilibrium, the generalized Einstein relation reduces to the standard one.

The balance equation for the electron energy density results with $X = \varepsilon$

$$\frac{\partial w_{\mathrm{n}}}{\partial t} + e\, \boldsymbol{j}_{\mathrm{n}} \cdot \boldsymbol{E} + \nabla_{\boldsymbol{r}} \cdot \boldsymbol{s}_n = -n \frac{\langle \varepsilon \rangle - \langle \varepsilon \rangle^{\mathrm{eq}}}{\tau_{w_n}} \,. \tag{39.92}$$

Considering the relation between the expectation value $\langle \varepsilon \rangle$ and the dynamic temperature by introducing the new energy relaxation time $\tau_{w_{\mathrm{n}}}^{\star}$

$$\frac{\langle \varepsilon \rangle - \langle \varepsilon \rangle^{\mathrm{eq}}}{\tau_{w_{\mathrm{n}}}} = \frac{3 k_{\mathrm{B}}}{2} \frac{T_{\mathrm{n}}^{\star} - T_0}{\tau_{w_{\mathrm{n}}}^{\star}} \tag{39.93}$$

the final equation reads

$$\nabla_{\boldsymbol{r}} \cdot \boldsymbol{s}_{\mathrm{n}} + \frac{\partial w_{\mathrm{n}}}{\partial t} = -e\, \boldsymbol{j}_{\mathrm{n}} \cdot \boldsymbol{E} - n \frac{3 k_{\mathrm{B}}}{2} \frac{T_{\mathrm{n}}^{\star} - T_0}{\tau_{w_{\mathrm{n}}}^{\star}} \,. \tag{39.94}$$

The balance equation for the energy current density results from the three scalar balance equations for $X = \varepsilon v_x$, $X = \varepsilon v_y$, and $X = \varepsilon v_z$, which combined yield the vector balance equation :

$$\begin{aligned} \frac{\partial \boldsymbol{s}_{\mathrm{n}}}{\partial t} &+ e\, n \left\langle \hat{m}^{-1} \varepsilon + \boldsymbol{v} \boldsymbol{v}^{\mathrm{T}} \right\rangle_{\boldsymbol{k}} \boldsymbol{E} \\ &+ \left(\nabla_{\boldsymbol{r}}^{\mathrm{T}} \left[n \left\langle \varepsilon \boldsymbol{v} \boldsymbol{v}^{\mathrm{T}} \right\rangle_{\boldsymbol{k}} \right] \right)^{\mathrm{T}} = -\frac{\boldsymbol{s}_{\mathrm{n}}}{\tau_{\boldsymbol{s}_{\mathrm{n}}}} \,. \end{aligned} \tag{39.95}$$

The first tensor quantity in the equation above is again approximated in such a manner that close to equilibrium, and for typical unstrained semiconductors such as silicon the approximation is well justified:

$$\left\langle \hat{m}^{-1}\varepsilon + \boldsymbol{v}\boldsymbol{v}^{\mathrm{T}} \right\rangle_{\boldsymbol{k}} \approx \left[\frac{\mathrm{Tr}\left\langle \varepsilon\, \hat{m}^{-1} \right\rangle_{\boldsymbol{k}}}{3} + \frac{\left\langle \boldsymbol{v}^2 \right\rangle_{\boldsymbol{k}}}{3} \right] \hat{I}\,. \tag{39.96}$$

Moreover, this approximation is simplified by the introduction of the additional relaxation time $\tau^*_{s_\mathrm{n}}$.

$$\left[\frac{\mathrm{Tr}\left\langle \varepsilon\, \hat{m}^{-1} \right\rangle_{\boldsymbol{k}}}{3} + \frac{\left\langle \boldsymbol{v}^2 \right\rangle_{\boldsymbol{k}}}{3} \right] \tau_{s_\mathrm{n}} = \frac{5}{6} \left\langle \boldsymbol{v}^2 \right\rangle_{\boldsymbol{k}} .\tau^*_{s_\mathrm{n}} \tag{39.97}$$

The second tensor quantity in (39.95) is of the highest order, and a stronger approximation, which relates this term to the lower-order quantity $\left\langle \boldsymbol{v}^2 \right\rangle_{\boldsymbol{k}}$, is applied to close the set of equations.

$$\left\langle \varepsilon \boldsymbol{v}\boldsymbol{v}^{\mathrm{T}} \right\rangle_{\boldsymbol{k}} \approx \frac{5\left\langle \boldsymbol{v}^2 \right\rangle^2_{\boldsymbol{k}}}{6\mathrm{Tr}\left\langle \hat{m}^{-1} \right\rangle_{\boldsymbol{k}}} \hat{I}\,. \tag{39.98}$$

The approximation above is exact for a Maxwell–Boltzmann distribution function in conjunction with a parabolic band structure. Also, the gradient of the expected value of the inverse mass is neglected:

$$\nabla_{\boldsymbol{r}} \frac{1}{\mathrm{Tr}\left\langle \hat{m}^{-1} \right\rangle_{\boldsymbol{k}}} \approx 0\,. \tag{39.99}$$

The evaluation of the relaxation times has finally revealed [71] that the following simplifying assumption is well justified:

$$\tau^*_{s_\mathrm{n}} \approx \tau_{s_\mathrm{n}} \tag{39.100}$$

In summary, these approximations result in the final equation for the energy current density:

$$\begin{aligned} \boldsymbol{s}_\mathrm{n} + \tau^*_{s_\mathrm{n}} \frac{\partial \boldsymbol{s}_\mathrm{n}}{\partial t} &= -e\, n \frac{5 k_\mathrm{B} T^\star_\mathrm{n} \tau^*_{s_\mathrm{n}}}{2 m^\star_\mathrm{n}} \boldsymbol{E} \\ &\quad - \frac{5\tau^*_{s_\mathrm{n}} \tau_{j_\mathrm{n}}}{2 m^\star_\mathrm{n} \tau^*_{j_\mathrm{n}}} \nabla_{\boldsymbol{r}} \left[n \left(k_\mathrm{B} T^\star_\mathrm{n} \right)^2 \right]\,. \end{aligned} \tag{39.101}$$

Equations (39.90), (39.94), and (39.101) contain first-order derivatives with respect to time. Considering these derivatives leads to a strong influence of plasma oscillations with frequencies in the THz regime on the transient response of the final device model. This makes the initial value problem very stiff and creates a large amount of unnecessary numerical effort. However, plasma oscillations are not important for most applications. Therefore, these time derivatives are typically neglected. As a consequence, plasma oscillations are suppressed, and as the relaxation times are typically smaller than 1 ps, this approximation is considered to be valid as long as only time constants much larger than 1 ps are relevant for the application under consideration. Moreover, the interband transition of carriers has been neglected so far. These transitions are typically related to processes such as Shockley–Read–Hall recombination, Auger recombination, impact ionization, or band-to-band tunneling (BBT) [37]. These processes are typically considered only in the continuity equations for electrons and holes by a generation term G. Taking this into account, the final equation set of the generalized HD model reads as follows for electrons:

$$\nabla_{\boldsymbol{r}} \cdot \boldsymbol{j}_\mathrm{n} + \frac{\partial n}{\partial t} = G\,, \tag{39.102}$$

$$\boldsymbol{j}_\mathrm{n} = -e\, n \frac{\tau^*_{j_\mathrm{n}}}{m^\star_\mathrm{n}} \boldsymbol{E} - \frac{\tau_{j_\mathrm{n}}}{m^\star_\mathrm{n}} \nabla_{\boldsymbol{r}} \left[n k_\mathrm{B} T^\star_\mathrm{n} \right]\,, \tag{39.103}$$

$$\nabla_{\boldsymbol{r}} \cdot \boldsymbol{s}_\mathrm{n} = -e \boldsymbol{j}_\mathrm{n} \cdot \boldsymbol{E} - n \frac{3 k_\mathrm{B}}{2} \frac{T^\star_\mathrm{n} - T_0}{\tau^\star_{w_\mathrm{n}}}\,, \tag{39.104}$$

$$\boldsymbol{s}_\mathrm{n} = -e\, n \frac{5 k_\mathrm{B} T^\star_\mathrm{n} \tau^*_{s_\mathrm{n}}}{2 m^\star_\mathrm{n}} \boldsymbol{E} - \frac{5\tau^*_{s_\mathrm{n}} \tau_{j_\mathrm{n}}}{2 m^\star_\mathrm{n} \tau^*_{j_\mathrm{n}}} \nabla_{\boldsymbol{r}} \left[n \left(k_\mathrm{B} T^\star_\mathrm{n} \right)^2 \right]\,. \tag{39.105}$$

With the same chain of arguments as above, the following equation set of the generalized HD model for holes can be derived as well:

$$\nabla_{\boldsymbol{r}} \cdot \boldsymbol{j}_\mathrm{p} + \frac{\partial p}{\partial t} = G\,, \tag{39.106}$$

$$\boldsymbol{j}_\mathrm{p} = e\, p \frac{\tau^*_{j_\mathrm{p}}}{m^\star_\mathrm{p}} \boldsymbol{E} - \frac{\tau_{j_\mathrm{p}}}{m^\star_\mathrm{p}} \nabla_{\boldsymbol{r}} \left[p k_\mathrm{B} T^\star_\mathrm{p} \right]\,, \tag{39.107}$$

$$\nabla_{\boldsymbol{r}} \cdot \boldsymbol{s}_\mathrm{p} = e \boldsymbol{j}_\mathrm{p} \cdot \boldsymbol{E} - p \frac{3 k_\mathrm{B}}{2} \frac{T^\star_\mathrm{p} - T_0}{\tau^\star_{w_\mathrm{p}}}\,, \tag{39.108}$$

$$\boldsymbol{s}_\mathrm{p} = e\, p \frac{5 k_\mathrm{B} T^\star_\mathrm{p} \tau^*_{s_\mathrm{p}}}{2 m^\star_\mathrm{p}} \boldsymbol{E} - \frac{5\tau^*_{s_\mathrm{p}} \tau_{j_\mathrm{p}}}{2 m^\star_\mathrm{p} \tau^*_{j_\mathrm{p}}} \nabla_{\boldsymbol{r}} \left[p \left(k_\mathrm{B} T^\star_\mathrm{p} \right)^2 \right]\,. \tag{39.109}$$

The particle and energy current densities are eliminated from the HD model by inserting Eqs. (39.107), (39.109), (39.103), and (39.105) into Eqs. (39.106), (39.108), (39.102), and (39.104). Including PE (39.11) and keeping in mind (39.10), five equations remain for the unknown variables p, $T^\star_\mathrm{p}$, n, $T^\star_\mathrm{n}$, and Ψ. These are

$$(39.106) + (39.107) \;\rightarrow F_{\dot{\mathrm{p}}}(p, T^\star_\mathrm{p}, n, T^\star_\mathrm{n}, \Psi) + \frac{\partial p}{\partial t} = 0\,, \tag{39.110}$$

$$(39.108) + (39.107) + (39.109) \rightarrow F_{\dot{w}_\mathrm{p}}(p, T^\star_\mathrm{p}, n, T^\star_\mathrm{n}, \Psi) = 0\,, \tag{39.111}$$

$$(39.102) + (39.103) \;\rightarrow F_{\dot{\mathrm{n}}}(p, T^\star_\mathrm{p}, n, T^\star_\mathrm{n}, \Psi) + \frac{\partial n}{\partial t} = 0\,, \tag{39.112}$$

$$(39.104) + (39.103) + (39.105) \rightarrow F_{\dot{w}_\mathrm{n}}(p, T^\star_\mathrm{p}, n, T^\star_\mathrm{n}, \Psi) = 0\,, \tag{39.113}$$

$$(39.11) \;\rightarrow F_\Psi(p, n, \Psi) = 0\,, \tag{39.114}$$

where F_α with $\alpha = \dot{p}, \dot{w}_\mathrm{p}, \dot{n}, \dot{w}_\mathrm{n}, \Psi$ are abbreviations including all relevant terms besides the derivatives in time. The final set of Eqs. (39.110)–(39.114) contains four macroscopic relaxation times for holes ($\tau^*_{j_\mathrm{p}}$, τ_{j_p}, $\tau^\star_{w_\mathrm{p}}$, $\tau^*_{s_\mathrm{p}}$) and four for electrons ($\tau^*_{j_\mathrm{n}}$, τ_{j_n}, $\tau^\star_{w_\mathrm{n}}$, $\tau^*_{s_\mathrm{n}}$).

In order to generate a sequential multi-scale model, the assumption is introduced that these relaxation times depend only locally on the hole or electron dynamic temperature respectively for a predefined lattice temperature and doping level. This assumption allows a precalculation of these parameters under homogeneous bulk conditions with a given lattice temperature, a constant doping level, and a constant electric field $\boldsymbol{E}$ by SHE or single-particle MC simulations. Combining (39.79)–(39.81), (39.89), (39.103)–(39.105) and introducing the simplifications resulting from the assumption of homogeneous material and electric field yield

$$\tau^*_{j_\mathrm{n}} = \frac{m^\star_\mathrm{n} \langle \boldsymbol{v} \rangle_\mathrm{hom} \cdot \boldsymbol{E}}{e\boldsymbol{E}^2}\,, \tag{39.115}$$

$$\tau_{j_\mathrm{n}} = \frac{3\tau^*_{j_\mathrm{n}}}{m^\star_\mathrm{n} \mathrm{Tr} \langle \hat{m}^{-1} \rangle_\mathrm{hom}}\,, \tag{39.116}$$

$$\tau^\star_{w_\mathrm{n}} = \frac{3k_\mathrm{B}(T^\star_\mathrm{n} - T_0)}{2e \langle \boldsymbol{v} \rangle_\mathrm{hom} \cdot \boldsymbol{E}}\,, \tag{39.117}$$

$$\tau^*_{s_\mathrm{n}} = \frac{2m^\star_\mathrm{n} \langle \varepsilon \boldsymbol{v} \rangle_\mathrm{hom} \cdot \boldsymbol{E}}{5ek_\mathrm{B}T^\star_\mathrm{n}\boldsymbol{E}^2}\,. \tag{39.118}$$

Please note that the dynamic temperature corresponding to a given homogeneous bulk condition with a constant electric field $\boldsymbol{E}$ is calculated following (39.87) by

$$T^\star_\mathrm{n} = \frac{m^\star_\mathrm{n}}{3k_\mathrm{B}} \langle \boldsymbol{v}^2 \rangle_\mathrm{hom}\,. \tag{39.119}$$

Similar equations can be derived for holes. Please note that for unstrained silicon close to room temperature, the dependence of the above transport parameters and carrier temperatures on the orientation of the electric field is weak and can safely be neglected [80]. However, for other situations, especially strained semiconductor materials that show a non-isotropic transport behavior even close to equilibrium, it is advisable to choose the field orientation for the calculation of the transport parameters that best reflects the predominant transport direction in the device problem that should be simulated at least as long as scalar transport parameters should still be used [81]. For further details about the efficient evaluation of the relaxation times, please refer to Jungemann and Meinerzhagen [12].

The transport parameters are precalculated and stored together with the dynamic temperature in lookup tables as a function of discrete values of the electric field, doping, and lattice temperature. For device simulations they are interpolated with appropriate methods [81], and the relation between the carrier temperature and the modulus of the electric field (39.119) is applied to evaluate the correct parameter values for the device simulation based on the local carrier temperatures in the device simulator. The application of this table model-based sequential multi-scale approach does not impair the CPU efficiency of the HD model compared with models based on analytical expressions for the transport parameters.

Metal–semiconductor contacts typically have a highly doped semiconductor layer underneath the metal layer. This contact situation is typically modeled by the ideal ohmic contact model assuming charge neutrality in the highly doped semiconductor region and a local quasi-thermodynamic equilibrium between the metal and the highly doped semiconductor region. In order to understand this contact model properly, the relation between the carrier densities and the electrostatic potential at thermodynamic equilibrium must be reviewed first. At equilibrium the distribution function is given by the Fermi distribution function, which is known as soon as the temperature T_0 and the Fermi energy $E_{\mathrm{F},0}$ are given. Both quantities do not depend on the space coordinate. Assuming that the Fermi distribution function can be well approximated by the Boltzmann distribution function for the calculation of the carrier densities, these densities are given by Madelung [2]

$$n(\boldsymbol{r}) = N_\mathrm{C} \exp\left(-\frac{E_\mathrm{C} - e\Psi(\boldsymbol{r}) - E_{\mathrm{F},0}}{k_\mathrm{B}T_0}\right)\,, \tag{39.120}$$

$$p(\boldsymbol{r}) = N_\mathrm{V} \exp\left(\frac{E_\mathrm{V} - e\Psi(\boldsymbol{r}) - E_{\mathrm{F},0}}{k_\mathrm{B}T_0}\right)\,.$$

E_C and E_V are the energy levels of the conduction band and the valance band edges for vanishing electrostatic potential respectively. Moreover, the effective density of state N_C is given by

$$N_\mathrm{C} = \int_0^\infty D(\epsilon) \exp\left(-\frac{\epsilon}{k_\mathrm{B}T_0}\right) \mathrm{d}\epsilon\,, \tag{39.121}$$

where the density of states function $D(\epsilon)$ for the conduction bands is given by

$$D(\epsilon) = \sum_\nu \frac{2}{(2\pi)^3} \int_{\varepsilon_\nu(\boldsymbol{k})=\epsilon} \frac{\mathrm{d}^2k}{|\nabla_{\boldsymbol{k}}\varepsilon_\nu(\boldsymbol{k})|}\,. \tag{39.122}$$

The sum in the above equation extends over all conduction bands ν specified by the dispersion relations $\varepsilon_\nu(\boldsymbol{k})$ already introduced in (39.5) and the integral is a surface integral over all states $\boldsymbol{k}$ within the conduction band ν, having a band energy $\varepsilon_\nu(\boldsymbol{k}) = \epsilon$. Analog equations hold for N_V and

the valence bands. For the densities at equilibrium given in (39.120)

$$n(\boldsymbol{r})p(\boldsymbol{r}) = n_i^2 = N_\mathrm{C}N_\mathrm{V}\exp\left(\frac{E_\mathrm{V}-E_\mathrm{C}}{k_\mathrm{B}T_0}\right) \tag{39.123}$$

holds and this defines the intrinsic density n_i. Introducing the Fermi potential Φ by

$$-e\Phi = E_{\mathrm{F},0} - E_{\mathrm{F},i}\,, \tag{39.124}$$

where $E_{\mathrm{F},i}$ does not depend on $\boldsymbol{r}$ and is given by

$$E_{\mathrm{F},i} = \frac{1}{2}\left(E_\mathrm{V} + E_\mathrm{C} + k_\mathrm{B}T_0\,\ln\frac{N_\mathrm{V}}{N_\mathrm{C}}\right)\,, \tag{39.125}$$

yields the following more symmetric representation for the densities at equilibrium:

$$\begin{aligned} n(\boldsymbol{r}) &= n_i\,\exp\left(\frac{\Phi-\Psi(\boldsymbol{r})}{V_{T_0}}\right)\,,\\ p(\boldsymbol{r}) &= n_i\,\exp\left(\frac{\Psi(\boldsymbol{r})-\Phi}{V_{T_0}}\right)\,. \end{aligned} \tag{39.126}$$

Here, V_{T_0} is the thermal voltage for T_0 as defined already in (39.91) in an analog manner for $T_\mathrm{n}^\star$. Owing to the local quasi-thermodynamic equilibrium between the metal and the highly doped semiconductor region, it can be assumed that both regions share the common temperature T_0 and a common Fermi potential Φ_M that is independent of $\boldsymbol{r}$ in the contact region. Moreover, assuming charge neutrality means

$$p - n + N_\mathrm{D} - N_\mathrm{A} = 0\,, \tag{39.127}$$

where N_D and N_A are the densities of ionized donator and acceptor atoms. Using the last equation, (39.126) and $\Phi = \Phi_\mathrm{M}$ finally yield the boundary conditions of an ideal ohmic contact for the electrostatic potential

$$\Psi = \Phi_\mathrm{M} + V_{T_0}\,\sinh^{-1}\left(\frac{N_\mathrm{D}-N_\mathrm{A}}{n_\mathrm{i}}\right)\,, \tag{39.128}$$

the particle densities

$$p = -\frac{N_\mathrm{D}-N_\mathrm{A}}{2} + \sqrt{\left(\frac{N_\mathrm{D}-N_\mathrm{A}}{2}\right)^2 + n_\mathrm{i}^2}\,, \tag{39.129}$$

$$n = \frac{N_\mathrm{D}-N_\mathrm{A}}{2} + \sqrt{\left(\frac{N_\mathrm{D}-N_\mathrm{A}}{2}\right)^2 + n_\mathrm{i}^2}\,, \tag{39.130}$$

and the temperatures

$$T_\mathrm{p}^\star = T_0\,, \tag{39.131}$$

$$T_\mathrm{n}^\star = T_0\,. \tag{39.132}$$

The Fermi potentials at the metal contacts are typically specified by setting $\Phi_\mathrm{M} = 0\,\mathrm{V}$ at one reference contact and by applying voltages between this reference contact and the other contacts.

On all other surfaces, Neumann-type boundary conditions are typically applied for the electric field, the particle current, and energy current densities. For more information about boundary conditions, and in particular, for a more realistic boundary condition for minority carriers at ohmic contacts, please refer, for example, to Engl et al. [75].

Hierarchical Drift-Diffusion Model

The DD model is obtained by applying the following additional approximations to the HD model:

$$\tau_{j_\mathrm{n}} \approx \tau_{j_\mathrm{n}}^*\,, \tag{39.133}$$

$$T_\mathrm{n}^\star \approx T_0\,, \tag{39.134}$$

which imply the classical Einstein relation

$$D = V_{T_0}\mu\,. \tag{39.135}$$

Equation (39.90) now reads

$$\boldsymbol{j}_\mathrm{n} + \tau_{j_\mathrm{n}}^*\frac{\partial \boldsymbol{j}_\mathrm{n}}{\partial t} = -en\frac{\tau_{j_\mathrm{n}}^*}{m_\mathrm{n}^\star}\boldsymbol{E} - \frac{k_\mathrm{B}T_0\tau_{j_\mathrm{n}}^*}{m_\mathrm{n}^\star}\nabla_{\boldsymbol{r}} n\,, \tag{39.136}$$

and Eqs. (39.94) and (39.101) can be dropped, because the particle gas temperature is assumed to be equal to the lattice temperature. The final DD model for holes and electrons is obtained, neglecting again the derivative in time in the balance equations for the current densities

$$\nabla_{\boldsymbol{r}}\cdot\boldsymbol{j}_\mathrm{p} + \frac{\partial p}{\partial t} = G\,, \tag{39.137}$$

$$\boldsymbol{j}_\mathrm{p} = e\,p\frac{\tau_{j_\mathrm{p}}^*}{m_\mathrm{p}^\star}\boldsymbol{E} - \frac{k_\mathrm{B}T_0\tau_{j_\mathrm{p}}^*}{m_\mathrm{p}^\star}\nabla_{\boldsymbol{r}} p\,, \tag{39.138}$$

$$\nabla_{\boldsymbol{r}}\cdot\boldsymbol{j}_\mathrm{n} + \frac{\partial n}{\partial t} = G\,, \tag{39.139}$$

$$\boldsymbol{j}_\mathrm{n} = -e\,n\frac{\tau_{j_\mathrm{n}}^*}{m_\mathrm{n}^\star}\boldsymbol{E} - \frac{k_\mathrm{B}T_0\tau_{j_\mathrm{n}}^*}{m_\mathrm{n}^\star}\nabla_{\boldsymbol{r}} n\,. \tag{39.140}$$

The boundary conditions for the electrostatic potential, the particle densities, the electric field, and the particle current densities are the same as for the HD model.

Quasi-Fermi potentials Φ_p and Φ_n for holes and electrons can be defined by the relations

$$p = n_\mathrm{i} \exp\left(\frac{\Phi_\mathrm{p} - \Psi}{V_\mathrm{T}}\right) \tag{39.141}$$

and

$$n = n_\mathrm{i} \exp\left(\frac{\Psi - \Phi_\mathrm{n}}{V_\mathrm{T}}\right), \tag{39.142}$$

where n_i is the intrinsic particle density. This definition of the quasi-Fermi potentials is consistent with (39.126). This implies that in regions where the carrier distribution is close to equilibrium, these quasi-Fermi potentials still have a thermodynamic relevance. With these quasi-Fermi potentials the current continuity equations read

$$\boldsymbol{j}_\mathrm{p} = -p\frac{e\,\tau^*_{j_\mathrm{p}}}{m^\star_\mathrm{p}}\nabla_{\boldsymbol{r}}\Phi_\mathrm{p} = -p\mu_\mathrm{p}\nabla_{\boldsymbol{r}}\Phi_\mathrm{p} \tag{39.143}$$

and

$$\boldsymbol{j}_\mathrm{n} = n\frac{e\,\tau^*_{j_\mathrm{n}}}{m^\star_\mathrm{n}}\nabla_{\boldsymbol{r}}\Phi_\mathrm{n} = n\mu_\mathrm{n}\nabla_{\boldsymbol{r}}\Phi_\mathrm{n}. \tag{39.144}$$

Thus, the driving force is given by the gradient of the quasi-Fermi potential, of which the modulus $|\nabla_{\boldsymbol{r}}\Phi|$ is used to parameterize the mobility in order to account for non-equilibrium effects such as velocity saturation in the DD model [37, 75]. Moreover, under homogeneous material and field conditions

$$|\nabla_{\boldsymbol{r}}\Phi|_\mathrm{hom} = E \tag{39.145}$$

holds. This allows a sequential multi-scale DD model to be established by using the same transport parameter table as for the HD equation, by evaluating τ^*_j based on the local gradient of the quasi-Fermi potential and (39.145). Using this approach with an identical transport parameter table for the HD and DD models guarantees that the HD and DD models yield the same results as the BTE, which has been applied for calculating the transport parameter table, under homogeneous material and field conditions.

The balance equations of the current densities (39.138) and (39.140) are eliminated from the DD model similar to the HD case, and the final DD model for the variables p, n, and Ψ reads

$$(39.137) + (39.138) \;\rightarrow F_\mathrm{\dot{p}}(p, n, \Psi) + \frac{\partial p}{\partial t} = 0\,, \tag{39.146}$$

$$(39.139) + (39.140) \;\rightarrow F_\mathrm{\dot{n}}(p, n, \Psi) + \frac{\partial n}{\partial t} = 0\,, \tag{39.147}$$

$$(39.11) \;\rightarrow F_\Psi(p, n, \Psi) = 0\,. \tag{39.148}$$

The sequential multi-scale method just demonstrated for the case of silicon can be extended to other semiconductor materials such as SiGe and devices with heterojunctions such as SiGe HBTs [82]. The results for electron or hole transport resulting from the BTE and hierarchical HD and DD transport equations are identical for homogeneous material and field conditions. Thus, these models are ideally suited to study of the modeling differences at the level of inhomogeneous devices owing to the simplifying assumptions introduced for deriving the HD and DD equations. Therefore, these hierarchical models have been applied in [71, 83] to examine the accuracy of the DD and HD models for MOS transistors with nanometer dimensions and in [84] for advanced SiGe HBTs. Moreover, the sequential multi-scale methods have been extended to the efficient modeling of noise, where the noise in the HD and DD models is traced back to the microscopic scattering processes of the BTE [12, 32, 85]. In Jungemann et al. [86] it is verified that this approach to modeling noise yields excellent results for modern MOS transistors. Moreover, in the same paper it was also shown that the drain current noise in n-channel MOS transistors is predominantly due to the rather cool electrons near the source and not to the hot electrons near the drain, as was previously thought.

39.3.2 Concurrent Multi-Scale Modeling

Sequential multi-scale modeling typically tries to enhance the solution accuracy of macroscopic models (e.g., HD and DD models) by calculating transport parameters such as relaxation times or noise models sequentially in a preprocessing step based on models that consider effects on a more microscopic scale such as the BTE. However, there are many cases for which such a method is not applicable or just too much effort owing to the large amount of different cases that need to be considered in the preprocessor and stored in tables. In the case of semiconductor transport, such cases are typically related to an improved modeling of carrier generation or recombination both in the bulk or at the interfaces. Although the Shockley–Read–Hall and Auger recombinations can be well modeled based on the local quantities available in an HD and DD simulator such as the carrier densities or the electric field, local models for hot carrier or tunneling-related processes such as impact ionization (II), oxide injection, and BBT, tend to be very poor, especially for devices with submicron dimensions. These effects depend in a strongly nonlocal manner on the space-dependent solution variables of the HD and DD models and typically require for really accurate modeling details that can only be provided by models that access the microscopic scale, such as the BTE or Schrödinger's equation. In order to enhance the accuracy of the computationally efficient DD and HD models, this missing information related to nonlocal and/or microscopic effects is provided on-the-fly and incorporated in real time into the DD and HD simulations. Therefore, such methods are typically addressed as concurrent multi-scale

models [68]. Very often the additional information concerning nonlocal and/or microscopic effects is only needed in a very restricted region of the total simulation domain, so that concurrent multi-scale models can be very efficient.

William Shockley [87] showed that with his rather simple lucky electron ansatz, a wide variety of hot carrier-related experiments can be explained. This means that under favorable circumstances this simple model can provide useful quantitative information about the energy distribution function, which is normally only available after the solution of the BTE, already based on DD or HD models. This makes the lucky electron ansatz very interesting for concurrent multi-scale modeling. At the time of Shockley's publications, device dimensions were still so large that quantities such as densities and fields could typically be assumed to be spatially homogeneous and of only one-dimensional orientation for interpreting experiments. Therefore, as device dimensions shrank and these assumptions were no longer valid, it remained unclear how to generalize the lucky electron ansatz for inhomogeneous and multi-dimensional situations. For example, field lines of the electrostatic field and current lines of the electric current densities coincide for 1D but typically not for 2D or 3D situations. The solution to this problem became apparent when Tak Ning and coworkers showed that their experimental data of optical enhanced hot-electron injection could be nicely interpreted by a nonlocal lucky electron ansatz [88]. Based on the results of this paper, a new concurrent multi-scale model for impact ionization and oxide injection in silicon n-channel MOSFETs was developed consisting of a HD model [79] and a field line-based lucky electron model that exploited both the spatial electron density and the electrostatic potential distributions resulting from the HD model in a nonlocal manner [89, 90]. With only three different constants (one for each experiment), it is demonstrated in Meinerzhagen and Meinerzhagen and Engl [89, 90] that substrate current, drain-induced oxide injection, and optically triggered oxide injection can be modeled accurately by this new model in a consistent manner for many different devices and bias conditions. Moreover, it is demonstrated that the application of the HD model is mandatory for this success. None of the models published before typically combining a DD diffusion model and a nonlocal lucky electron ansatz based on current lines [91,92] could demonstrate a comparable predictive capability. The concurrent multi-scale hot-electron model first presented in Meinerzhagen and Meinerzhagen and Engl [89, 90] is therefore well suited to the modeling of flash memory devices, as demonstrated in Hagenbeck et al. [93]. Later the nonlocal lucky electron model for II in silicon was improved by replacing the hard threshold energy for impact ionization of the original model by a soft threshold model based on an energy-dependent impact ionization probability derived from full-band data [94, 95]. Moreover, a soft threshold model for the impact ionization triggered by holes was provided as well. The predictive capability of this improved model for substrate current simulations is verified in Jungemann et al. [96, 97] for a wide variety of different NMOS transistors and bias conditions. First, the nonlocal models for hot carrier effects were used in a postprocessing step [89, 90], but with a sufficiently smooth implementation of these models, a self-consistent solution is possible as well. Owing to the nonlocal nature of the lucky electron ansatz, a complete consideration of these models in the Jacobian matrices generates a large amount of additional entries typically changing the properties of the Jacobian matrices completely. Therefore, these nonlocal models are often embedded in the nonlinear relaxation schemes (e.g., [98]) updating the generation term G within every nonlinear iteration without generating Jacobian entries. The convergence of these iteration schemes may be slow if impact ionization dominates, but it is typically reliable enough to estimate the solution accuracy [99] and to simulate even the breakdown characteristic of a bipolar transistor with open base [100]. The nonlocal soft threshold model for impact ionization is used by many device simulation groups worldwide and is available in commercial TCAD tools [101].

In order to profit from the wealth of hot carrier-related information inherent to the energy distribution function, which results from the solution of the BTE, the classical DD and HD device models have also been directly coupled with the BTE resulting in another concurrent multi-scale model. In the beginning, the BTE was typically solved using the MC method and thus this new method is mostly addressed as non-self-consistent MC simulation (NSC-MC, [12]). The spatial distribution of the electrostatic potential is given for this method, mostly resulting from a DD or HD model. The NSC-MC method for hot carrier simulations was first described in Sangiorgi et al. and Higman et al. [102, 103]. In order to enhance the efficiency of this simulation method, the solution region of the BTE is typically substantially smaller than the solution region of the DD or HD models. The carriers within the MC simulation are injected at some part of the boundary of the MC simulation region or inside the simulation region based on information from the HD or DD simulations and absorbed at other parts of the boundary as described, for example, in Sangiorgi et al., Higman et al., and Jungemann and Meinerzhagen [12, 102, 103] and for the NAND-Flash memory simulation presented later in this section. The injection method depends on the purpose of the MC simulation and may require a profound understanding of the device behavior, as will be explained as well later in this section. The NSC-MC method was first verified for hot carrier effects in Sangiorgi et al. and Higman et al. [102, 103] and later on a much broader experimental basis for substrate current calculations in Bude and Mastrapasqua and Jungemann et al. [96, 104]. Moreover, in Jungemann et al. [96] it is shown that the NSC-MC method is predictive, as it does not require any calibration

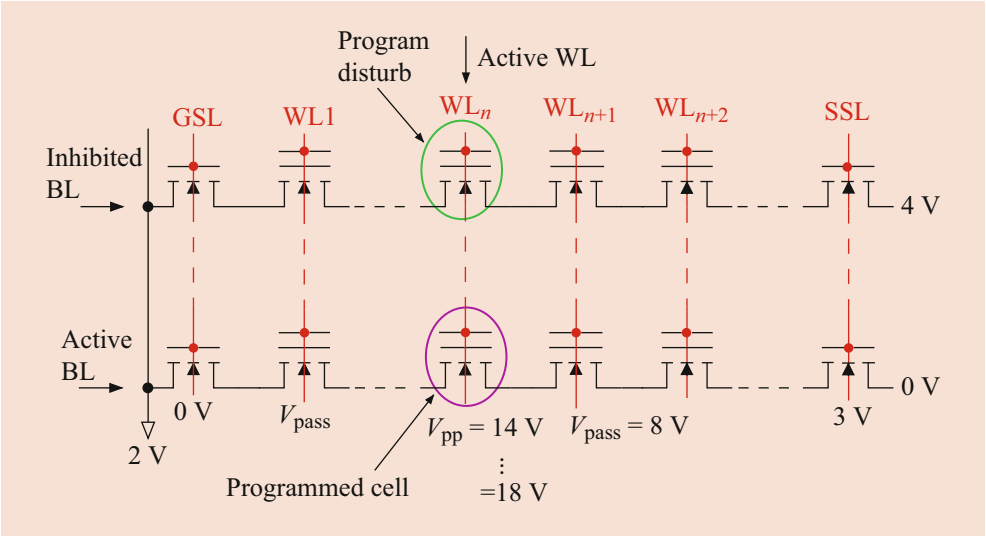

Fig. 39.19 Schematic of NAND strings with bias conditions during programming and the location of the program disturb

on the device level for modeling substrate currents with high accuracy over a wide range of devices and bias conditions. In addition it is shown in Jungemann et al. [96] that NSC-MC simulations are two to three orders of magnitude more efficient for substrate current calculations than self-consistent MC simulations, without compromising accuracy. The NSC-MC method presented in Jungemann et al. [96] is verified for an even wider variety of different MOSFETs in Jungemann et al. [97]. Thus, it can be concluded that the NSC-MC method is well suited to modeling hot carrier effects and this will be confirmed in Sect. 39.3.2. Although used for this purpose in a number of publications (e.g., Cheng et al. [105]), the NSC-MC method is not well suited to simulating drain currents and drain current noise. This is carefully examined and shown in Jungemann and Meinerzhagen [12, 106].

Probably the first nonlocal model for BBT in silicon MOSFETs and bipolar transistors was published and verified in Bergner et al. and Schwerin et al. [107–109]. The model describes the tunneling probabilities in a nonlocal manner based on the spatial distribution of the electrostatic potential following the early work of Keldysh. Provided that the nonlocal tunneling models are implemented in a sufficiently smooth manner, self-consistent simulations with these nonlocal models are possible [110]. Similar to the nonlocal II models described above, the easiest way to yield self-consistent simulations is to embed these models in one of the nonlinear relaxation schemes for DD or HD equations and to update the generation term G within each nonlinear iteration based on the nonlocal model. Again the convergence of these iteration schemes may be slow if the tunnel effect dominates, but it is typically reliable enough to estimate the solution accuracy [99]. In Carrillo-Nunez et al. [111] a nonlocal band-to-band tunnel model for heterostructure tunnel-FETs was developed and verified by simulation based on a full-band and atomistic quantum transport simulator. Meanwhile, a variety of different nonlocal tunneling models can be used, even in commercial TCAD tools [101].

Concurrent Multi-Scale Simulation of Program Disturb in NAND-Flash Memories

In this chapter it is shown that even very difficult problems can be simulated accurately and efficiently by a concurrent multi-scale model. Such a problem is the program disturb in NAND flash memory technologies. Program disturb is one effect that may ultimately limit the scalability of these technologies [112].

For the application of a concurrent multi-scale model, it is important to clearly understand the physical origin of this problem. Therefore, the effect itself is explained first. The results outlined in this section have been previously published in Nguyen et al. and Kuligt et al. [110, 113].

In Fig. 39.19 the scheme of a NAND memory block is shown, including all relevant bias voltages applied during the programming mode. The memory block consists of a number of bit line (BL) strings. Each string is composed of a number of memory cells and two select transistors at each end of the string. All cells and transistors in a BL string are of NMOS type and electrically connected by sharing common source/drain regions. The control gates of the memory cells are accessed by word lines (WLs) and the gates of the select transistors are accessed by the ground select line (GSL) and the string select line (SSL) respectively. The programming of the memory cell selected by the active WL and the active BL is intended. However, cells in other BLs sharing the active WL may also change their stored charge owing to the high programming voltage V_{pp} of the active WL. In order to inhibit programming in the non-active BLs, the string of memory cells in these lines is first isolated by switching the select

transistors connected to the SSL in these BLs into the off-state. This is achieved by applying a bias of 3 V to the SSL and a bias of 4 V to the source/drain regions of these select transistors that are accessible at the boundary of the memory block. Please note that during programming, because of the voltages applied, all select transistors connected to the GSL operate in the off-state and all memory cells operate in the on-state. Moreover, the select transistor connected to the SSL in the active BL operates in the on-state, as its contact accessible at the boundary is grounded, causing the electrostatic potential within the channels of the memory cells within the active BL to remain close to 0 V too. The undesired programming of a memory cell in an inhibited non-active BL is referred to as program disturb and depends strongly on the voltage V_{pass} applied to all nonactive WLs. This voltage increases (boosts) the channel potential in the inhibited BLs during programming owing to the capacitive coupling of the gate electrodes and the isolated electron charges in the inhibited BLs. As a consequence, the programming of the memory cells by electron injection is strongly reduced in the inhibited BLs. Program disturb is typically strongly enhanced for the memory cells neighboring the select transistors and depends critically on the distance between the memory cell and the closest select transistor (SL-WL separation) [114]. In Lee et al. [114] this enhanced program disturb is explained by BBT, which occurs in inhibited lines for programming bias conditions predominantly close to the silicon surface near the select transistors with the lower gate bias provided by the GSL. This BBT generates electrons and in Lee et al. [114] the enhanced program disturb is explained by the subset of these electrons that get hot enough to overcome the oxide barrier and increase the electron injection responsible for the programming of the cells. However, by far the most important reason for the enhanced program disturb is not mentioned in Lee et al. [114] and this is because of the holes that are generated by BBT. Owing to the large potential difference between the channel and the substrate in the inhibited BLs resulting from the boosting by V_{pass}, these holes generated close to the silicon/oxide interface are accelerated toward the substrate. Close to the bottom boundary of the substrate space charge region, the accelerated holes cause impact ionization (II). The electrons generated by this II are accelerated toward the silicon surface, and because of the same large potential difference, they can easily gain enough energy to overcome the oxide barrier leading to a significant increase in electron injection. Because the enhanced program disturb is clearly caused by hot electrons, it cannot be described by the program disturb model published in Torsi et al. [112], as this model neglects hot-electron injection.

Below, the feasibility, accuracy, and predictive capability of a new concurrent multi-scale simulation model for program disturb in general, and the enhanced disturb close to the select transistors in particular, are demonstrated by means of a comprehensive experimental verification. The disturb mechanism is investigated using a 48-nm TANOS 32-bit NAND string architecture as an example.

For the simulation a simplified 2D TANOS NAND string is considered consisting of the ground select, string select, and three WL cell transistors with lateral dimensions typical for a 48-nm NAND technology. The simulated structure is shown in Fig. 39.20. Program disturb is most pronounced for inhibited WL1 cells when the WL1 bias is equal to the programming voltage. Therefore, this situation is chosen for the simulation. Complete programming pulses of 20 µs in length are simulated by the transient DD simulator GALENE III [85], including self-consistently the nonlocal models for BBT [109] and II [94] for the electron and holes mentioned before. As all transistors in the string are either in the deep subthreshold or linear region, there is no difference if the DD or the HD model is used for simulating impact ionization. Therefore, the more CPU-efficient DD model is used for the simulation. The programming and inhibit pulses applied to the WLs have a trapezoidal shape with a length of about 22 µs and a maximum applied voltage of V_{pp} and V_{pass} respectively. The dominant mechanism allowing electrons to leak from the isolated inversion layer in the inhibited cell transistors is clearly BBT. Therefore, spatial distributions of electrostatic potential and the BBT generation rate for holes resulting from the transient DD simulations are transferred to the full-band Monte-Carlo (MC) simulator ELWOMIS [12] at equidistant time sampling points (every 2.5 µs in this example). Based on very CPU-time-efficient post-processor frozen-field MC simulations [12] using the BBT rate distribution for carrier injection and considering hole and electron-initiated II [12] in the full-band simulator, the energy distribution function for electrons is evaluated at the Si surface. The coupling of the DD and MC simulators is similar to the methods published in [115] and [96]. For every time step of the MC simulator, holes are injected into the MC simulation region and the total charge of the injected holes is equal to the integral of the BBT generation rate over the MC simulation region times the time step. The spatial injection probability density is given by the spatial BBT generation rate divided by the total integrated rate. The state of the injected hole in k-space is randomly chosen with a Maxwell–Boltzmann distribution. The carriers are reflected at the silicon/oxide boundary and removed out of the simulation at all other boundaries. The MC simulation region is selected large enough so that most hot carriers are included. The stochastic error control described in [12] is applied to control the numerical effort of the MC simulations. The oxide injection current density is calculated based on the energy distribution function resulting from the MC simulation underneath the WLs at the silicon/oxide interface. To calculate this current density both tunneling and direct over-the-barrier mechanisms are considered [1]. For this

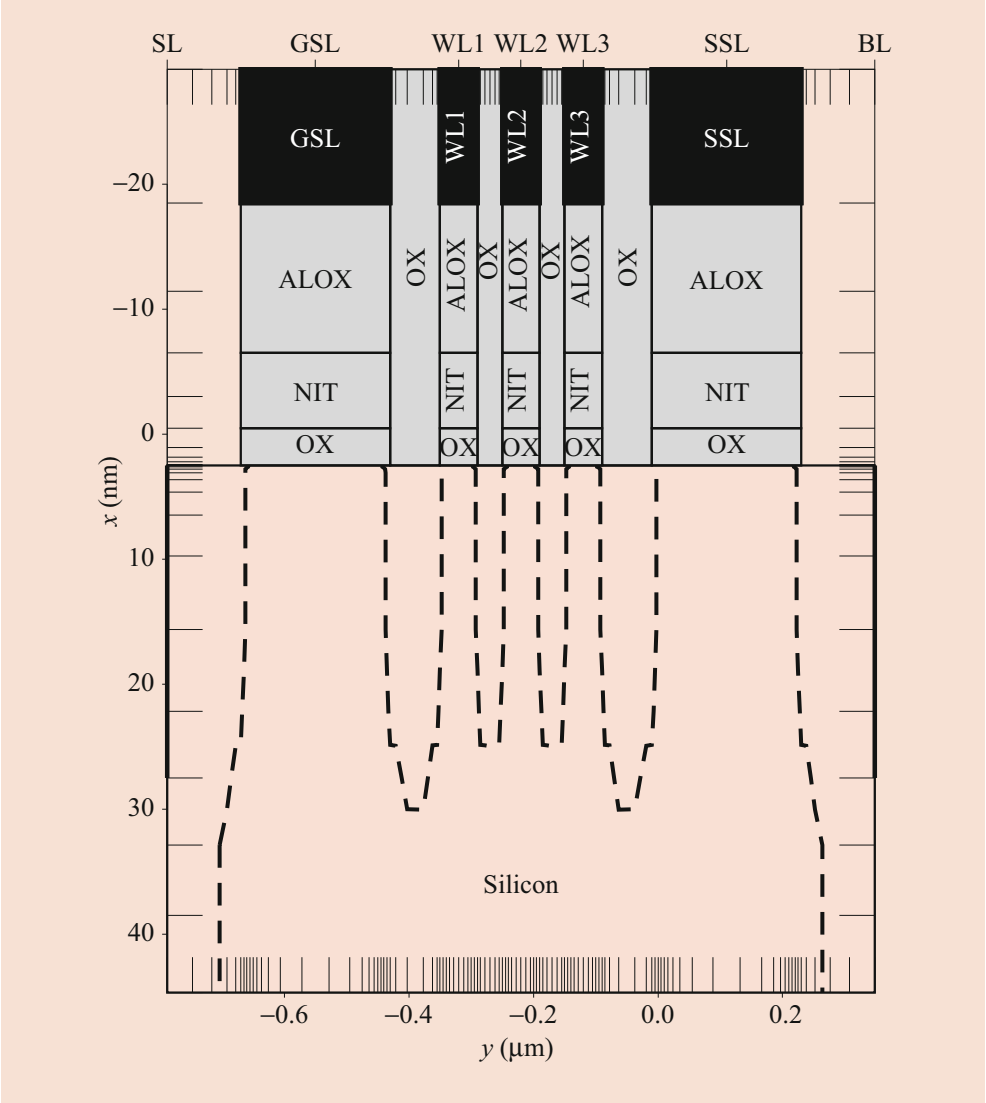

Fig. 39.20 Simplified 2D NAND string used in the simulations

example the latter mechanism was dominant. It is assumed that all injected electrons are finally trapped in the nitride layer. The injected charge per sampling time point or MC simulation is calculated as the injection current for each cell times the sampling time interval times the number of programming pulses NP for which the charge injection is calculated using the same transient DD simulation. After NP pulses, the injected charge, which is the sum over the injected charges per MC simulation (8 in this example), is fed back to the DD simulator by adding it to the charge considered in the nitride regions of the cells, and the DD and MC simulations are continued with the updated charge within the nitride layer. None of the physical models used in the simulations has been fitted or calibrated for these program disturb simulations. The model parameters applied have been either taken from the literature [12] or in the case of the BBT model have been extracted long ago based on experimental data from much older standard MOS technologies.

Figure 39.21 shows typical transient DD results for the surface potential in the middle of the channels of the cell transistors WL1–WL3 for 80 and 140 nm GSL-WL1 separation respectively. The decay of the potential after the initial programming pulse ramp-up is predominantly due to the BBT leakage current.

Figure 39.22 shows typical spatial BBT and II rate distributions from GALENE III and ELWOMIS respectively in an inhibited line for a typical programming situation in the middle of a programming pulse. Please note the much higher hole-initiated II rate for the small GSL-WL1 separation. The simulation time depends linearly on the number of DD and MC simulations necessary for an accurate simulation of the threshold voltage versus programming time characteristics.

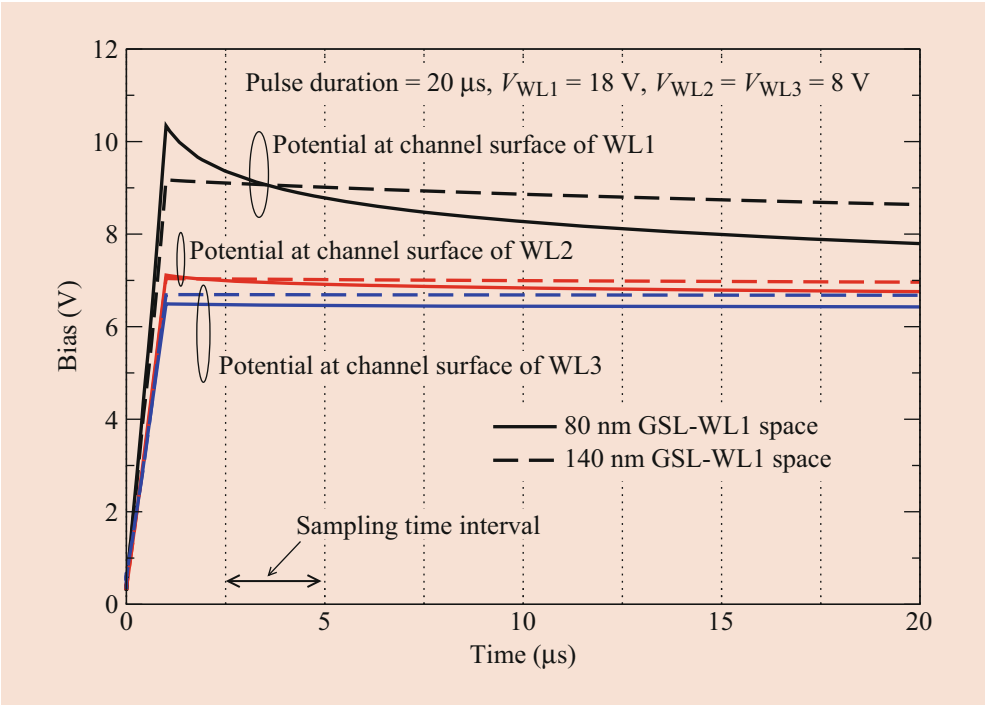

Fig. 39.21 Transient simulation results for the surface potential in the middle of the channel of the different cells for 80 nm and 140 nm GSLWL1 separation. The time sampling points for the MC simulations are marked by the dotted vertical lines

Figure 39.23 demonstrates that an update of the stored charge after NP = 5 pulses (or a total programming time increment of 0.1 ms) is sufficient to get accurate results. For NP = 5 the simulated threshold voltage increment versus programming time characteristics is shown in Fig. 39.24 for the inhibited WL1 cells, all programming voltages, and the most critical GSL-WL1 separation. Please note the large influence of the programming voltage on the program disturb. Figures 39.25, 39.26, 39.27, and 39.28 show a comparison between the simulated (big dots) and measured threshold voltages in the inhibited WL1 cells as a function of programming voltage for all four considered GSL-WL1 separations after a total programming time of 2 ms (100 pulses). The drawn lines in these figures represent the distribution of 15 measured samples. The horizontal lines indicate from bottom to top the minimum, quartile $Q_{0.25}$, median, quartile $Q_{0.75}$, and maximum of the distribution. Taking into consideration the complicated physics of program disturb, the simplified 2D structure used in the simulations and the fact that none of the physical models has been calibrated for these simulations, the agreement between the simulated and measured threshold voltage shifts is very impressive. The important influence of programming voltage and GSL-WL1 separation on WL1 threshold voltage is accurately represented by the new simulation model. This proves that the most important physical mechanisms governing program disturb are well represented by the simulation model in a predictive manner. Compared with the measured characteristics, the simulated threshold voltages increase somewhat faster with increasing programming voltage. This is most probably due to the neglect of charge leakage from the nitride layer between programming pulses in the simulations.

The demonstrated comprehensive comparison between simulation and experiment shows that the dependence of program disturb on WL-SL separation and programming voltage can be accurately described by a concurrent multi-scale model without fitting any model parameters.

39.4 Numerical Solution of the Drift-Diffusion Model: Some Historical Remarks

In the following, the development of the numerical solution methods for the DD equations will be reviewed, as much can be learned from this development for comparable tasks in the future. Aspects covered well in the literature will be only briefly mentioned by citing the appropriate references. Other aspects that are very important as well but rarely mentioned in the literature or even nearly forgotten today will be highlighted. In particular, the aspect of preserving the inherent "stability" of the underlying differential equations in terms of monotonicity properties during the discretization process will be carefully examined. The general flow of arguments presented here follows closely those outlined in Meinerzhagen [116]. Several details have also been previ-

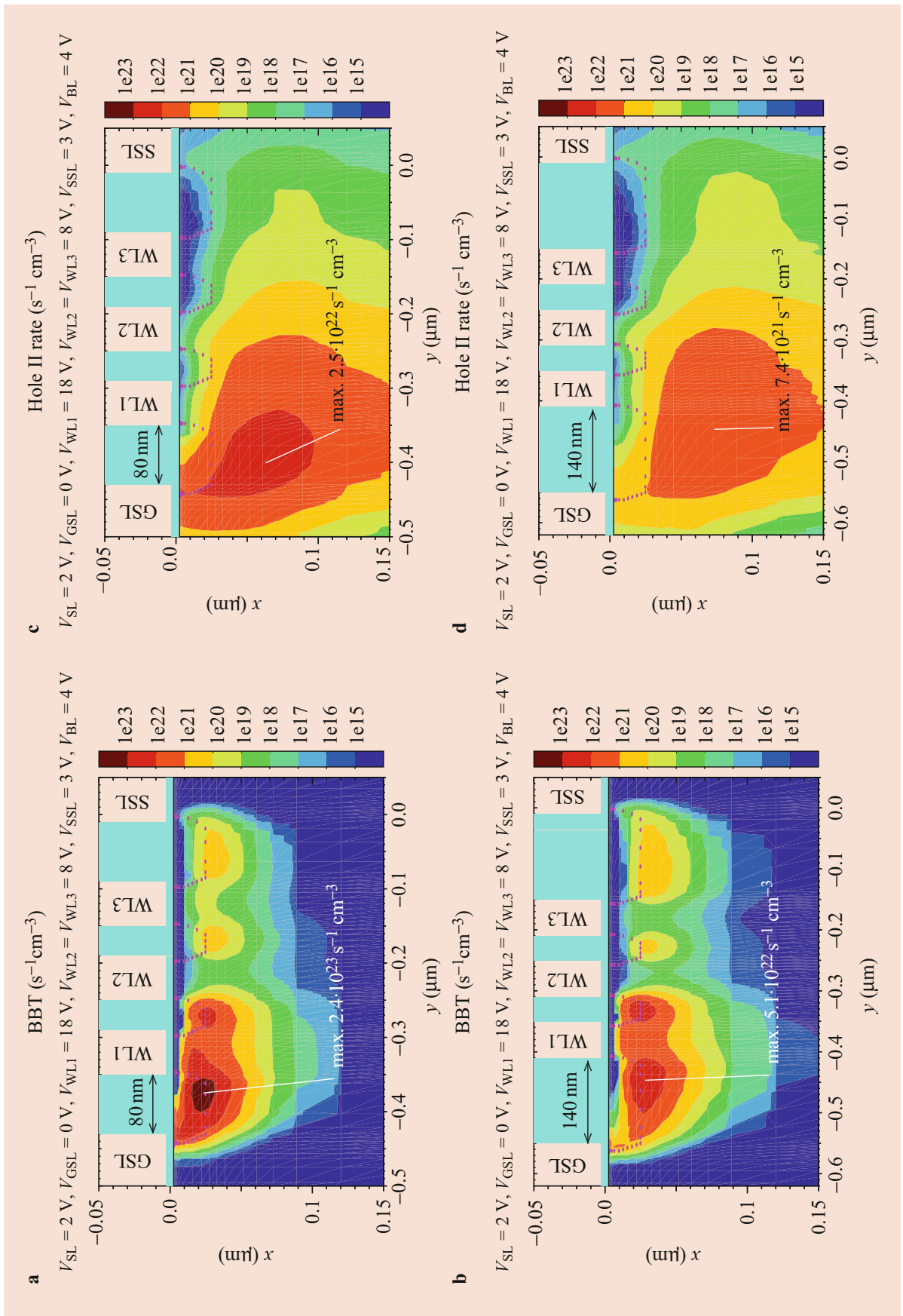

Fig. 39.22 Spatial distribution of the hole generation rate due to BBT for (**a**) 80 nm and (**b**) 140 nm GSL-WL1 separation. Spatial distribution of the hole-initiated II rate (**c**) for 80 nm and (**d**) 140 nm GSL-WL1 separation (scale on the right [s^{-1} cm^{-3}])

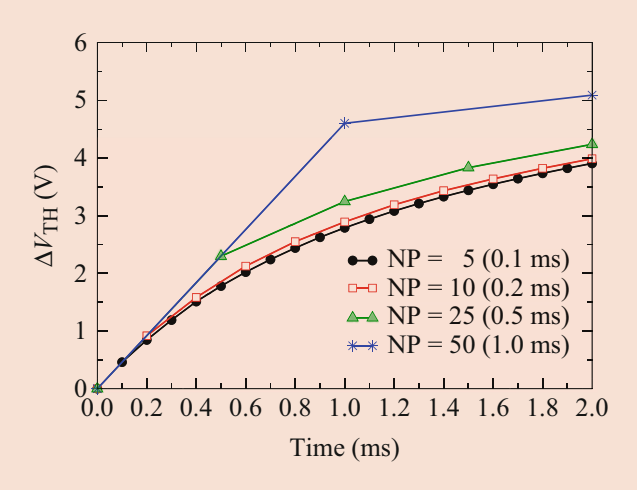

Fig. 39.23 Influence of NP on the accuracy of the threshold voltage increment versus programming time characteristic for 80 nm GSL-WL1 separation and 18 V programming voltage

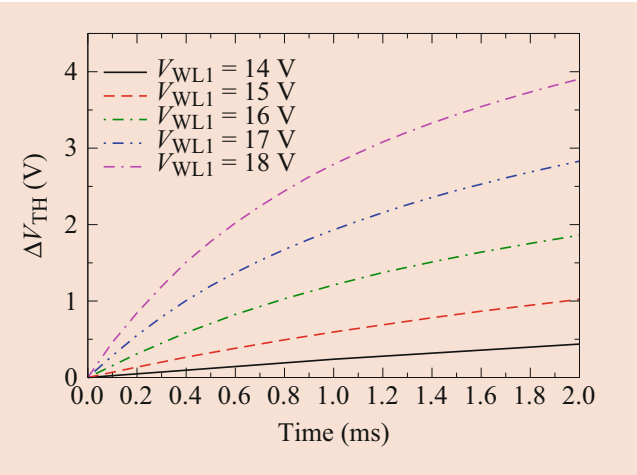

Fig. 39.24 Simulated threshold voltage increment (ΔV_{TH}) versus programming time characteristics for 80 nm GSL-WL1 separation

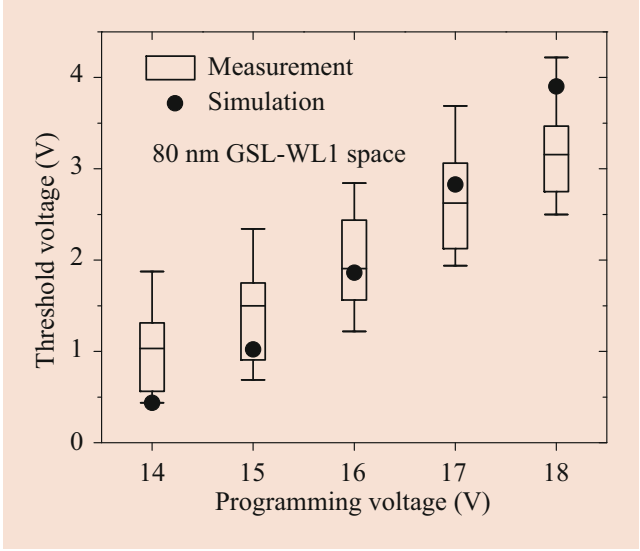

Fig. 39.25 Threshold voltage as a function of programming voltage after a total programming time of 2 ms for 80-nm GSL-WL1 separation; comparison of simulation and measurement

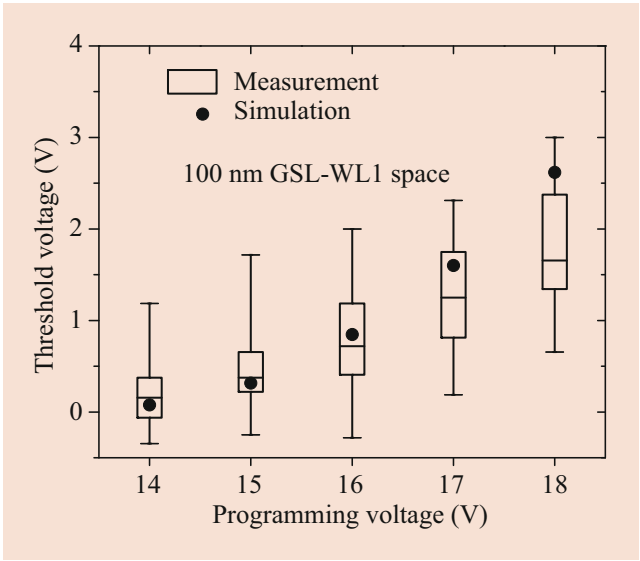

Fig. 39.26 Threshold voltage as a function of programming voltage after a total programming time of 2 ms for 100-nm GSL-WL1 separation; comparison of simulation and measurement

ously published in Engl et al. and Bank et al. [75,117]. Some hints concerning the HD model will be given at the end.

As the potentials Φ_n and Φ_p cover a much smaller range of numerical values than do the densities n, p, intermediate and final solutions of the DD system of equations are typically saved by storing Ψ, Φ_n, and Φ_p instead of Ψ, n, and p. Moreover, formulating the DD equations in the new set of variables makes it much easier to introduce the solution algorithms that are typically applied. Substituting p and n in the time-independent version of (39.146)–(39.148) by (39.141) and (39.142) and using the alternative expressions for the particle current densities (39.143) and (39.144) result in the following alternative forms of the stationary DD equations:

$$TP(\Psi, \Phi_p, \Phi_n) := -\nabla_{\boldsymbol{r}} \cdot [\kappa \nabla_{\boldsymbol{r}} \Psi]$$

$$+ e\left(n_i\left(\exp\left(\frac{\Psi - \Phi_n}{V_T}\right) - \exp\left(\frac{\Phi_p - \Psi}{V_T}\right)\right) - N_D + N_A\right) = 0 \qquad (39.149)$$

$$TH(\Psi, \Phi_p, \Phi_n) \qquad (39.150)$$

$$:= -\nabla_{\boldsymbol{r}} \cdot \left(n_i \exp\left(\frac{\Phi_p - \Psi}{V_T}\right) \mu_p \nabla_{\boldsymbol{r}} \Phi_p\right) - G$$

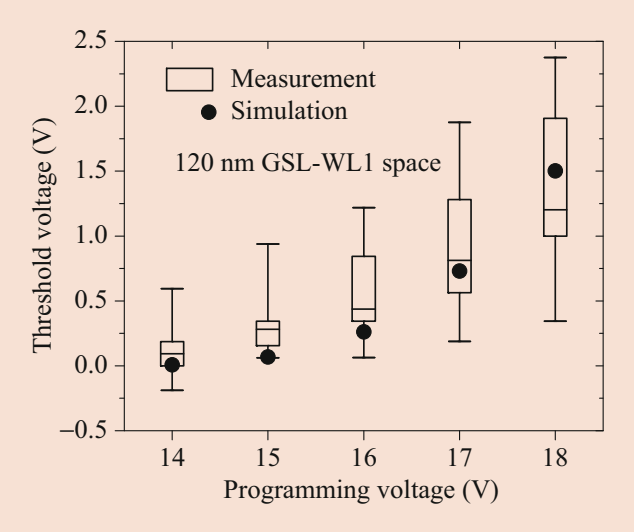

Fig. 39.27 Threshold voltage as a function of programming voltage after a total programming time of 2 ms for 120-nm GSL-WL1 separation; comparison of simulation and measurement

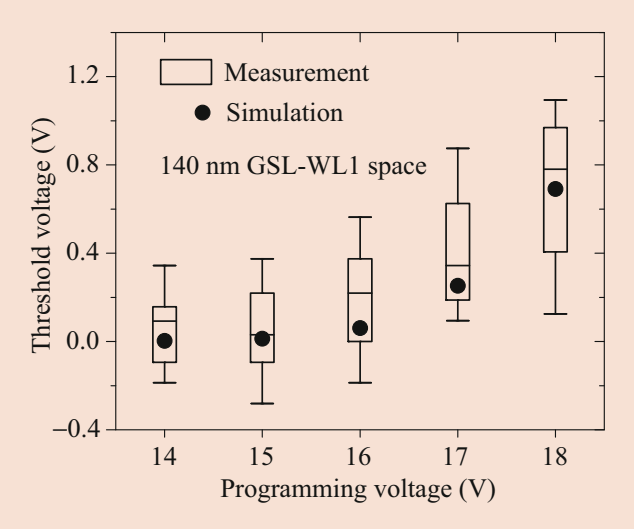

Fig. 39.28 Threshold voltage as a function of programming voltage after a total programming time of 2 ms for 140-nm GSL-WL1 separation; comparison of simulation and measurement

$$
\begin{aligned}
&= -\nabla_{\boldsymbol{r}} \cdot \left(n_{\mathrm{i}} \exp\left(\frac{-\Psi}{V_{\mathrm{T}}}\right) V_{\mathrm{T}} \mu_{\mathrm{p}} \nabla_{\boldsymbol{r}} \exp\left(\frac{\Phi_{\mathrm{p}}}{V_{\mathrm{T}}}\right)\right) - G \\
&=: \hat{TH}\left(\Psi, \exp\left(\frac{\Phi_{\mathrm{p}}}{V_{\mathrm{T}}}\right), \Phi_{\mathrm{n}}\right) = 0
\end{aligned}
$$

$$
\begin{aligned}
&TE(\Psi, \Phi_{\mathrm{p}}, \Phi_{\mathrm{n}}) \qquad (39.151) \\
&:= -\nabla_{\boldsymbol{r}} \cdot \left(n_{\mathrm{i}} \exp\left(\frac{\Psi - \Phi_{\mathrm{n}}}{V_{\mathrm{T}}}\right) \mu_{\mathrm{n}} \nabla_{\boldsymbol{r}} \Phi_{\mathrm{n}}\right) + G \\
&= +\nabla_{\boldsymbol{r}} \cdot \left(n_{\mathrm{i}} \exp\left(\frac{\Psi}{V_{\mathrm{T}}}\right) V_{\mathrm{T}} \mu_{\mathrm{n}} \nabla_{\boldsymbol{r}} \exp\left(\frac{-\Phi_{\mathrm{n}}}{V_{\mathrm{T}}}\right)\right) + G \\
&=: -\hat{TE}\left(\Psi, \Phi_{\mathrm{p}}, \exp\left(\frac{-\Phi_{\mathrm{n}}}{V_{\mathrm{T}}}\right)\right) = 0 \,.
\end{aligned}
$$

The boundary conditions remain unchanged, which means that at ideal ohmic contacts $\Phi_{\mathrm{p}} = \Phi_{\mathrm{n}} = \Phi_{\mathrm{M}}$ hold. It can be shown that the above system of differential equations has a unique solution provided a number of reasonable assumptions are fulfilled, especially for the generation term G. Please refer to Ladyshenskaya and Uraltseva [118] for a general theory and to Mock and Seidmann [119, 120] for special results concerning the DD set of equations. Moreover, there is an important property that deserves special attention.

I. All above operators TP - TE are in divergence from and result in important conservation laws if integrated over a finite volume and after the application of the divergence theorem.

For example, integrating $TE + TH$ over the simulation domain results in Kirchhoff's law for the stationary terminal currents of the device under consideration. If a numerical device model is used inside a circuit simulator, it is absolutely mandatory that this law is exactly reproduced by the numerical model. Therefore, it is very important to maintain the validity of such conservation laws in some sense during the discretization process.

The most important solution algorithm for the DD system is an iterative method often addressed as Gummel's nonlinear relaxation method [121]. Assuming that the result Ψ_k, $\Phi_{\mathrm{p},k}$, $\Phi_{\mathrm{n},k}$ after iteration k is known, this method evaluates the new approximate solution after iteration $k+1$ by solving the three boundary value problems (39.149)–(39.151) successively as follows:

$$
\begin{aligned}
TP(\Psi_{k+1}, \Phi_{\mathrm{p},k}, \Phi_{\mathrm{n},k}) &= 0 \,, \qquad (39.152) \\
TH(\Psi_{k+1}, \Phi_{\mathrm{p},k+1}, \Phi_{\mathrm{n},k}) &= 0 \,, \\
TE(\Psi_{k+1}, \Phi_{\mathrm{p},k+1}, \Phi_{\mathrm{n},k+1}) &= 0
\end{aligned}
$$

For the above partial differential equations, it is always assumed that the variable with the highest number of derivatives in the equation is updated and the other variables are kept unchanged. The individual nonlinear equations in (39.152) are typically solved by Newton's method, which converges very fast and robust, even for bad initial solutions, if the underlying equation is nearly linear. Therefore, Newton's method is typically applied for the operators $\hat{TH}$ and $\hat{TE}$ defined in (39.150) and (39.151) and not for the operators TH and TE, as $\hat{TH}$ and $\hat{TE}$ are nearly linear in the new variables:

$$
\zeta_{\mathrm{p}} := \exp\left(\frac{\Phi_{\mathrm{p}}}{V_{\mathrm{T}}}\right) \,, \quad \zeta_{\mathrm{n}} := \exp\left(\frac{-\Phi_{\mathrm{n}}}{V_{\mathrm{T}}}\right) \,, \qquad (39.153)
$$

provided that carrier generation G has no dominant influence. These new variables are often addressed as Slotboom variables because they were first introduced in Slotboom [122] and the advantages they have for generating "stable" discretization schemes were probably mentioned in Slotboom [123] for the first time. Nevertheless, it is still possible to calculate the Newton updates based on the numerically more convenient Jacobians TH and TE and the variables Φ_p and Φ_n. The only modification necessary for performing the Newton iterations for the more linear operators is to modify the Newton update itself as shown below for the hole continuity equation and the solution variable before ($\Phi_{p,b}$) and after ($\Phi_{p,a}$) one Newton step.

$$\Phi_{p,a} = \Phi_{p,b} + \delta\Phi_p \;\rightarrow \qquad (39.154)$$
$$\Phi_{p,a} = \Phi_{p,b} + V_T \ln\left(1 + \frac{\delta\Phi_p}{V_T}\right)$$

$\delta\Phi_p$ is the Newton update calculated using the Jacobian of TH for the variable ϕ_p. For a general report on using alternative solution variables for enhancing convergence, please refer to Bach et al. [124].

In order to understand which criteria in addition to the mandatory consistency criterion should be considered for the discretization of the continuous operators TP, TH and TE, it is very useful to look at the Jacobians of TP, $\hat{T}H$, and $\hat{T}E$, which are necessary for performing Gummel's nonlinear relaxation method based on Newton's method. These Jacobians are typically evaluated for some existing intermediate solution Ψ_b, $\Phi_{p,b}$, and $\Phi_{n,b}$, and operate on the functions $\delta\Psi$, $\delta\zeta_p$, and $\delta\zeta_n$. If in addition for the calculation of the Jacobians the dependence of the mobilities on the solution variables is neglected, these Jacobians have the following form:

$$\frac{\partial}{\partial\Psi} TP(\Psi_b, \Phi_{p,b}, \Phi_{n,b})[\delta\Psi] := -\nabla_{\boldsymbol{r}} \cdot [\kappa\nabla_{\boldsymbol{r}}\delta\Psi] \qquad (39.155)$$
$$+e\left(n_i\left(\exp\left(\frac{\Psi_b - \Phi_{n,b}}{V_T}\right) + \exp\left(\frac{\Phi_{p,b} - \Psi_b}{V_T}\right)\right)\right)\delta\Psi$$

$$\frac{\partial}{\partial\zeta_p}\hat{T}H(\Psi_b, \zeta_{p,b}, \Phi_{n,b})[\delta\zeta_p] \qquad (39.156)$$
$$:= -\nabla_{\boldsymbol{r}} \cdot \left(n_i \exp\left(\frac{-\Psi_b}{V_T}\right) V_T\mu_{p,b}\nabla_{\boldsymbol{r}}\delta\zeta_p\right)$$
$$-\frac{\partial}{\partial\zeta_p}G(\Psi_b, \zeta_{p,b}, \zeta_{n,b})\delta\zeta_p$$

$$\frac{\partial}{\partial\zeta_n}\hat{T}E(\Psi_b, \Phi_{p,b}, \zeta_{p,n})[\delta\zeta_n] \qquad (39.157)$$
$$:= -\nabla_{\boldsymbol{r}} \cdot \left(n_i \exp\left(\frac{\Psi_b}{V_T}\right) V_T\mu_{n,b}\nabla_{\boldsymbol{r}}\delta\zeta_n\right)$$
$$-\frac{\partial}{\partial\zeta_n}G(\Psi_b, \zeta_{p,b}, \zeta_{n,b})\delta\zeta_n.$$

All above partial derivatives with respect to solution variables are assumed to be Frećhet derivatives on suitable function spaces [125]. If only direct recombination and Shockley–Read–Hall recombination [37] are considered for the Frećhet derivative of the carrier generation G

$$-\frac{\partial}{\partial\zeta_p}G(\Psi_b, \zeta_{p,b}, \zeta_{n,b}) > 0 \qquad (39.158)$$
$$-\frac{\partial}{\partial\zeta_n}G(\Psi_b, \zeta_{p,b}, \zeta_{n,b}) > 0$$

holds. With this additional condition, all Jacobians (39.155)–(39.157) have important properties that again deserve special attention. They are:

II. Self-adjoint
III. Positive definite
IV. Of monotone type

if appropriate boundary conditions are assumed for the function spaces considered [125]. In particular, property IV is very important, as it means that for all these Jacobians monotonicity theorems hold [125, chapter 23.5], which restrict, for example, the possible form of the update functions $\delta\Psi$, $\delta\zeta_p$, and $\delta\zeta_n$ during the Newton iterations required for Gummel's nonlinear relaxation method very much and enhance the robustness and convergence properties of this solution method decisively.

The mathematical properties of the model after discretization should be as similar as possible to the properties of the continuous model! If this is fulfilled, the discrete model is an analogon of the continuous model, even if only coarse grids can be afforded, which is typically the case. This property is very important for the discretization error control on coarse grids. Therefore, discretization methods that are able to conserve conditions I–IV in some discrete sense are preferred.

The first 2D DD simulations used a rectangular solution domain and tensor product grids [123, 126] so that standard finite difference discretization methods for tensor product grids could be applied, which conserved most of the conditions mentioned above. However, many device cross sections were not rectangular, so that at least at the beginning of multi-dimensional numerical semiconductor device modeling, many groups developed discretization methods (see Barnes and Lomax, Buturla et al., Hachtel et al., Bank et al., Bürgler et al., and Mole [117, 127–132] and citations therein) for nonrectangular solution domains based on the

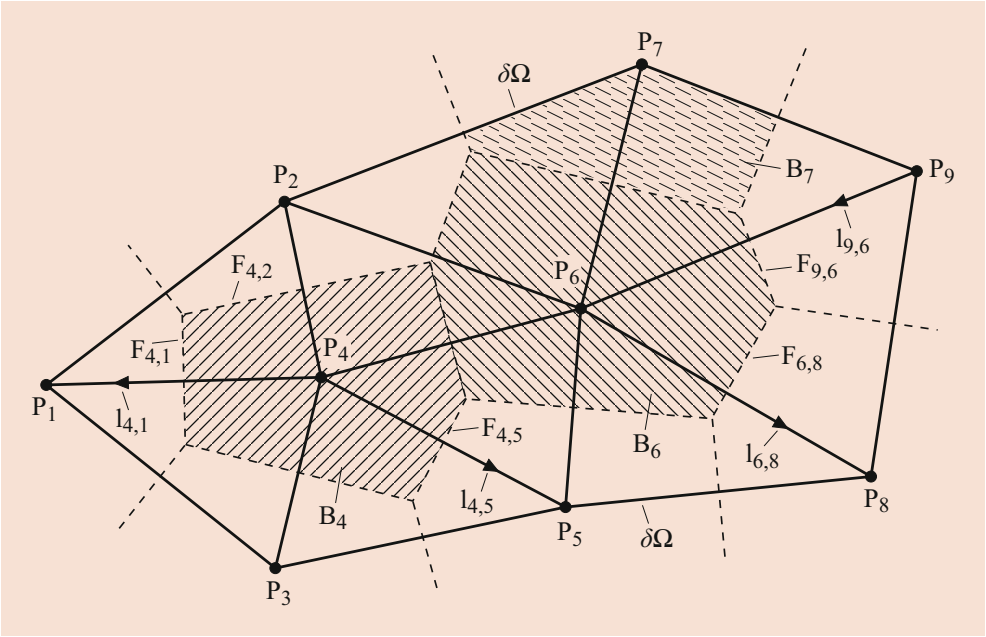

Fig. 39.29 Voronoi diagram (dashed lines) and Delaunay tessellation (thick drawn lines) for a 2D example with nine grid points

finite element approach [133], but it turned out that general finite element methods typically have problems conserving conditions I–IV [117, 128, 134, 135]. Finally, even for solution domains with complicated polygonal boundaries that cannot be discretized efficiently by a tensor product grid, the method of choice used today by the vast majority of DD and HD simulators is a straightforward generalization of the integration method published in Varga [51, chapter 6] for 2D tensor product grids. This method is able to conserve conditions I–IV, as will be shown below. This generalization for 2D problems was already briefly mentioned in Varga [51] using the early work of MacNeal [136] as a guideline. This general method is addressed as box integration method in Engl et al. [75] and as box method in Bank et al. [117] and today often named finite volume method [137]. An especially well-documented example of this historical development from the application of general finite element methods to the final exclusive application of the finite volume method is the development of numerical device modeling codes at IBM research. There, two groups independently developed two general numerical device modeling codes: one group with a clear focus on the application of general finite element methods [129,130,134] and the other group shifting more and more from hybrid finite element/finite volume discretization methods to the exclusive application of the finite volume method [128,138]. Both codes were developed over a decade until the beginning of the 1980s. Ten years later the finite element code development is no longer mentioned at all in a comprehensive review paper about TCAD development at IBM with more than 200 citations [139].

Possibly the first mathematical analysis of the general box integration method for the DD model in 3D is attributed to Sever [140]. The box integration method can be interpreted as a finite element method [117], but the grid elements for this method (e.g., triangles) cannot be considered as the basis from which the discretization method proceeds, as is the case for a general finite element method [133], but instead the elements are constructed in a unique way based on the predefined grid points. The method is based on the construction of two dual grids: the Voronoi diagram and the Delaunay tessellation. The early work of two Russian mathematicians M.G. Voronoi [141] and B.N. Delone [142] is typically cited in this context but the method in 2D is even older and has been rediscovered various times. Figure 39.29 is used to explain the basic principles of this method. The n grid points P_k ($n = 9$ in this example) with the coordinates $\boldsymbol{r}_k$ are considered as given. In a first step for each point with index k, its Voronoi volume V_k is constructed as the set of all points in space that are closer to P_k than to any other grid point.

$$V_k := \left\{\boldsymbol{r} | \parallel \boldsymbol{r} - \boldsymbol{r}_k \parallel \leq \parallel \boldsymbol{r} - \boldsymbol{r}_j \parallel, j = 1, \ldots, n, j \neq k\right\} \tag{39.159}$$

Moreover, for each grid point P_k its environment S_k is defined by

$$S_k := \left\{j | \mathcal{M}(V_k \cap V_j) \neq 0, j = 1, \ldots, n, j \neq k\right\}. \tag{39.160}$$

$\mathcal{M}$ indicates the 1D Lebesgue measure $\mathcal{M}_1$ for 2D problems and the 2D Lebesgue measure $\mathcal{M}_2$ for 3D problems. With this environment, the boundary of V_k is given by

$$\delta V_k := \bigcup_{j \in S_k} (V_k \cap V_j). \tag{39.161}$$

The union of all Voronoi volume boundaries defines the Voronoi diagram. Based on this diagram the dual grid structure of the Delaunay grid is defined by defining the set of edges D for this grid by the straight lines $l_{i,k}$ between the points P_i and P_k for which $\mathcal{M}(V_k \cap V_i) \neq 0$ and i and k vary between 1 and n with $i \neq k$. Please note that the $l_{i,k}$ are oriented curves starting at P_i and ending at P_k. If only the edges of the Delaunay grid without orientation are important, $l_{i,k}$ and $l_{k,i}$ can be considered equal. The typical elements in such a Delaunay grid are triangles for 2D problems and tetrahedra for 3D problems. But 2D and 3D rectangular tensor product grids are special cases for this method and fit perfectly into this framework. The DD and HD problems are typically formulated as boundary value problems on some finite region Ω, and in order to incorporate Neumann-type boundary conditions into the framework of box integration in a natural manner, the boundary $\delta\Omega$ is typically assumed to be composed of edges (faces in 3D) of the Delaunay grid elements. In the given example in Fig. 39.29 $\delta\Omega$ is the closed polygonal line composed of $l_{1,3}$, $l_{3,5}$, $l_{5,8}$, $l_{8,9}$, $l_{9,7}$, $l_{7,2}$, and $l_{2,1}$, and Ω is the interior of this closed polygonal line. The Voronoi volumes for the grid points on $\delta\Omega$ are typically unbounded, but for box integration, bounded boxes are mandatory. This leads to the following definitions:

$$B_k = V_k \cap (\Omega \cup \delta\Omega) \tag{39.162}$$

$$F_{k,j} = \delta V_k \cap \delta V_j \cap \Omega \tag{39.163}$$

Clearly, $\mathcal{M}(F_{k,j}) \geq 0$ and $F_{k,j}$ is only relevant if $l_{k,j}$ is part of the Delaunay grid. If no additional constraints are fulfilled, it can happen that $\mathcal{M}(F_{k,j}) = 0$ for some edge of the Delaunay grid. This is typically not good for the consistency of the discretization method and mostly avoided by constructing the grid in such a manner that, for 2D problems such as the given example, the Delaunay triangles that have some common boundary edge with $\delta\Omega$ have all their interior angles smaller than 90 degrees. Such triangles are called acute or non-obtuse. See, for example, Baker et al. [143], for algorithms generating grids in such a manner. If this additional condition is fulfilled, $\mathcal{M}(F_{k,j}) > 0$ for all edges of the Delaunay grid holds and only the boxes B_k of grid points on the boundary $\delta\Omega$ share some boundary with $\delta\Omega$ such as B_7 for the given example. Similar additional conditions with comparable consequences are considered for 3D problems as well [140]. For the box integration process presented here, it is not necessary for all triangles to be non-obtuse for preserving condition **IV**, but for finite element discretization schemes, this condition must be fulfilled [117, 143].

The boundary value problems TP, $\hat{T}H$, and $\hat{T}E$ defined in (39.149)–(39.151) and considered as individual problems that are solved separately have the following common form:

$$-\nabla_{\boldsymbol{r}} \cdot (a(\boldsymbol{r}, \nabla_{\boldsymbol{r}} u, u) \nabla_{\boldsymbol{r}} u) + f(\boldsymbol{r}, \nabla_{\boldsymbol{r}} u, u) = 0 \tag{39.164}$$

where $u(\boldsymbol{r})$ is the solution variable. Therefore, u is either Ψ or ζ_{p} or ζ_{n}. Moreover, $a(\boldsymbol{r}, \nabla_{\boldsymbol{r}} u, u) > 0$ always holds. The dependence of a and f on $\nabla_{\boldsymbol{r}} u$ and u considers the typical physical models for the mobilities and the generation rate and their dependence on the solution variables [37]. The first step always performed for the box method is to integrate (39.164) over the box B_k for each grid point P_k, which is not determined by a Dirichlet boundary condition. Moreover, the divergence theorem is used to transform the suitable parts of the integral over B_k into integrals over δB_k. This yields:

$$-\sum_{j \in S_k} \int_{F_{k,j}} a(\boldsymbol{r}, \nabla_{\boldsymbol{r}} u, u)(\nabla_{\boldsymbol{r}} u \cdot \boldsymbol{v}_{k,j}) \, \mathrm{d}F + \int_{B_k} f(\boldsymbol{r}, \nabla_{\boldsymbol{r}} u, u) \, \mathrm{d}V = 0. \tag{39.165}$$

$\boldsymbol{v}_{k,j}$ is a unit vector that has the same orientation as $l_{k,j}$. The above formulation is for the 3D case, where the first integrals integrate fluxes over an area and the remaining part is a volume integral. In the 2D case, the first integrals are line integrals and the second part is an area integral. If $\mathcal{M}(B_k \cap \delta\Omega) \neq 0$, it can typically be assumed that for this part of the boundary $(B_k \cap \delta\Omega)$, a Neumann-type boundary condition holds such that the flux through this part of the boundary is zero. This applies for instance to B_7 in the example, if for P_7 no Dirichlet boundary condition is given. It is clear that

$$\int_{F_{k,j}} a(\boldsymbol{r}, \nabla_{\boldsymbol{r}} u, u)(\nabla_{\boldsymbol{r}} u \cdot \boldsymbol{v}_{k,j}) \, \mathrm{d}F = -\int_{F_{j,k}} a(\boldsymbol{r}, \nabla_{\boldsymbol{r}} u, u)(\nabla_{\boldsymbol{r}} u \cdot \boldsymbol{v}_{j,k}) \, \mathrm{d}F \,, \tag{39.166}$$

where the first integral is related to P_k and the box integration over B_k, whereas the second integral is related to the point P_j and the box integration over B_j. During the discretization process the integrals in (39.165) are typically approximated independently by difference approximations and quadrature rules such that a consistent discrete approximation is generated. For conserving property **I** it is important that (39.166) holds exactly after discretization. If this is the case the discretized formulas for two points P_j and P_k with $k \in S_j$ (such as P_4 and P_6 in the example) can be summed, leading to an expression where the sum of the

discretized integrals over B_k and B_j is represented by the discretized flux integrals over the boundary of $B_k \cup B_j$, which is $\left((\cup_{i\in S_k} F_{k,i}) \cup (\cup_{i\in S_j} F_{j,i}) \cup ((B_k \cup B_j) \cap \delta\Omega)\right) \backslash F_{k,j}$. The resulting expression can be interpreted as a discrete version of the divergence theorem for $B_k \cup B_j$ and its boundary. If the discretized problem is solved exactly, this discretized version of the integral theorem holds exactly and does not depend on any discretization error. Relations of this kind are very helpful for checking the global numerical accuracy and the consistent calculation of, for instance, terminal currents.

In order to study how to preserve properties **II**–**IV** during the discretization process, Eq. (39.164) is simplified again by neglecting the dependence of a on the solution variable u and considering only the dependence of direct and SRH generation on the solution variable. Thus, (39.164) simplifies to

$$-\nabla_{\boldsymbol{r}} \cdot (a(\boldsymbol{r})\nabla_{\boldsymbol{r}} u) + f(\boldsymbol{r}, u) = 0 \tag{39.167}$$

and $\frac{\partial}{\partial u} f(\boldsymbol{r}, u) > 0$ always holds. If the discretization preserves property **I**, the discretized integral over $F_{k,j}$ in (39.165) can be considered as a function $\mathcal{F}(l_{k,j})$. This implies that $\mathcal{F}$ also depends on everything clearly connected to $l_{k,j}$ such as P_k and P_j. As (39.166) shall be preserved $\mathcal{F}(l_{k,j}) = -\mathcal{F}(-l_{k,j}) = -\mathcal{F}(l_{j,k})$ must hold. Let us assume that the discrete solution is represented by a vector $\boldsymbol{u}$ with n entries u_j and each u_j is the discrete approximation of the function u at the point P_j. The Jacobian of the equation system after discretization should be self-adjoint (symmetric). This requires the condition $\frac{\partial}{\partial u_j}\mathcal{F}(l_{k,j}) = \frac{\partial}{\partial u_k}\mathcal{F}(l_{j,k})$. There are not too many alternatives left if these above two conditions must be fulfilled simultaneously. One discretization formula, for which both conditions hold, is

$$\mathcal{F}(l_{k,j}) = -\frac{\mathcal{M}(F_{k,j})}{\mathcal{M}_1(l_{k,j})}\overline{a}(l_{k,j})(u_j - u_k). \tag{39.168}$$

Here, $\overline{a}(l_{k,j})$ is a suitable mean value of $a(\boldsymbol{r})$ that can be considered as a function of $l_{k,j}$ and for which $\overline{a}(l_{k,j}) = \overline{a}(l_{j,k}) > 0$ must be satisfied. If in addition the integral over the box B_k in (39.165) is discretized using the simplest quadrature formula

$$\int_{B_k} f(\boldsymbol{r}, u)\,\mathrm{d}V \approx \mathcal{V}(B_k) f(\boldsymbol{r}_k, u_k), \tag{39.169}$$

the strict diagonal dominance of the Jacobian matrix of the discrete system is guaranteed as well. $\mathcal{V}$ indicates the 2D Lebesgue measure for 2D problems and the 3D Lebesgue measure for 3D problems. So far, only the discretization for all points that are not given by a Dirichlet boundary condition has been studied. The set of indices of these points should be given by S_B. Moreover, S_D contains all indices of points that are given by a Dirichlet condition. The Jacobian entries for the latter points are simply 1 for the main diagonal and 0 for the other entries. In summary, the Jacobian of the discretized boundary value problem (39.167) is strictly diagonal dominant, all main diagonal elements are strictly positive, and all other elements are negative or zero. Such matrices are positive definite and M-matrices as well, which means that their inverse matrix has only elements that are positive or zero [51]. These properties are very beneficial for a large number of solution algorithms solving linear equations involving matrices. The convergence of iterative methods such as the Jacobi or Gauss–Seidel methods is guaranteed [51], semi-iterative methods such as conjugated gradient algorithms work well [144], and even Gaussian elimination profits, because a pivot element search is not necessary and the accumulation of the rounding error during elimination is well controlled. Finally, and probably most importantly, the discrete system introduced above is of the monotone type, which means that important stability inequalities can even be derived for the maximum norm, which is the most important norm for practical applications. For example, in Samarskij [145, chapter 4.2.2] the following is proven. If for all $k \in S_\mathrm{B}$

$$\sum_{j\in S_k} -\frac{\mathcal{M}(F_{k,j})}{\mathcal{M}_1(l_{k,j})}\overline{a}(l_{k,j})(\delta u_j - \delta u_k) + \mathcal{V}(B_k)\frac{\partial}{\partial u} f(\boldsymbol{r}_k, u_{k,b})\delta u_k = R_k \tag{39.170}$$

and $\delta u_k = b_k$ for all $k \in S_\mathrm{D}$, then the following stability inequality holds for the discrete solution:

$$\max_{1\le k\le n} |\delta u_k| \le \max_{k\in S_\mathrm{D}} |b_k| + \max_{k\in S_\mathrm{B}} \frac{|R_k|}{\mathcal{V}(B_k)\frac{\partial}{\partial u} f(\boldsymbol{r}_k, u_{k,b})} \tag{39.171}$$

This inequality is directly applicable for the estimation of the maximum Newton correction if the Jacobian on the left-hand side of (39.170) is used to solve the discretized nonlinear problem (39.167) by Newton's method. Moreover, such stability inequalities are very useful for evaluating upper bounds for the discretization error, even for the nonlinear problem (39.167). In Rafferty et al. [135] an excellent example is given demonstrating clearly how bad the discretization error is controlled if the off-diagonal elements of the Jacobian of the discretized electron continuity equation have both signs. Moreover, it is also shown in Rafferty et al. [135] for the same problem that the discrete solution becomes much more accurate and very well controlled by the applied voltages if all off-diagonal elements of the Jacobian always become negative or zero after a modification of the grid. The underlying reason is not as falsely stated in Bürgler et al. [131] that the original grid had one obtuse triangle but

that the original grid was not the Delaunay grid constructed on the basis of the Voronoi diagram, whereas the modified grid is the Delaunay grid. As already pointed out earlier, a Delaunay grid may contain obtuse triangles!

Another advantage of the discretization scheme presented above is that it allows a straightforward incorporation of the Scharfetter–Gummel discretization formula for the balance equations, which was originally developed for rectangular grids [75, 117, 146]. The application of this discretization formula is mandatory for achieving accurate simulation results on coarse grids. For general finite element schemes, it is typically very difficult to incorporate this formula, but for the scheme described above, it is easily done by choosing $\overline{a}(l_{k,j})$ as follows:

For holes:

$$\overline{a}(l_{k,j}) = n_{\mathrm{i}}\overline{\mu_{\mathrm{p}}}(l_{k,j})V_{\mathrm{T}}\frac{\Psi_j - \Psi_k}{\exp\left(\frac{\Psi_j}{V_{\mathrm{T}}}\right) - \exp\left(\frac{\Psi_k}{V_{\mathrm{T}}}\right)}. \quad (39.172)$$

For electrons:

$$\overline{a}(l_{k,j}) = n_{\mathrm{i}}\overline{\mu_{\mathrm{n}}}(l_{k,j})V_{\mathrm{T}}\frac{\Psi_k - \Psi_j}{\exp\left(\frac{-\Psi_j}{V_{\mathrm{T}}}\right) - \exp\left(\frac{-\Psi_k}{V_{\mathrm{T}}}\right)}. \quad (39.173)$$

$\overline{\mu_{\mathrm{n,p}}}(l_{k,j})$ are appropriate mean values of the mobilities that can be regarded as a function of the edge $l_{k,j}$. Results concerning the consistency and convergence of the discretization scheme described above for the balance equations can be found in Sever [140].

Gummel's nonlinear relaxation method (39.152), performed in such a manner that the relevant discrete Jacobian matrices fulfill conditions **II**–**IV**, which typically means that derivatives with respect to the solution variables are neglected for the mobilities and impact ionization, nearly always converges even for very bad initial solutions. One of the rare counterexamples is given in Bach et al. [124]. The convergence is typically slow for high current applications, but is very predictable; thus, the solution accuracy can be estimated very reliably during the iteration process [99]. This allows to switch to more coupled methods, like a simultaneous Newton method, as soon as the numerical solution accuracy is so high that the simultaneous Newton method is within the range where it converges quadratically. Of course, after switching all derivatives should be considered in the Jacobian matrix of the fully simultaneous Newton method. The availability of this combination of solution methods for the DD model featuring high robustness even for bad initial solution and high accuracy at the same time is possibly one reason why the DD model is still the numerical device model that is applied by far the most, even for nanoscale devices, where its physical accuracy is certainly questionable [83]. The above comments concerning the beneficial effect on robustness of neglecting the derivatives of the mobilities and impact ionization also apply to other nonlinear relaxation methods [124, 147] and are even valid for the fully coupled Newton method outside the range of quadratic convergence.

It is rather straightforward to extend the box integration method, including a Scharfetter–Gummel-type discretization for the energy flux densities to the HD model [79]. A nonlinear relaxation method with convergence properties that are coparable to Gummel's method has been published in Meinerzhagen et al. [98] and evaluated in Apanovich et al. [148] for the HD model. For this method and the numerical solution algorithms of the HD model in general, convergence robustness also increases significantly if certain derivatives with respect to mobilities and impact ionization are turned off in order to enhance the "stability" of the discretized equations.

39.5 Conclusion

The SHE method for the solution of the BTE is presented. This method enhances the applicability and versatility of the BTE model very much compared with typical MC solutions. This is shown in three examples: the calculation of plasma waves in GaAs bulk material, the detailed investigation of strong non-equilibrium transport in a one-dimensional nanoscale silicon N^+NN^+ structure, and the calculation of small-signal high-frequency figures of merit such as the maximum frequency of oscillation for an ultimately scaled silicon germanium heterojunction bipolar transistor. Sequential multi-scale DD and HD transport models for silicon are derived from the BTE. Owing to this derivation, called multi-scale analysis, it is possible to calculate the transport and noise parameters for these DD and HD models based on the solution of the BTE model under homogeneous material and field conditions in a consistent manner. Thus, the accuracy of the computationally more efficient DD and HD models is significantly enhanced. This is of paricular importance as it is typically impossible to evaluate the full set of transport and noise parameters experimentally. The historical development of the DD or the HD model-based concurrent multi-scale models for the efficient and accurate modeling of hot carrier or BBT effects is outlined. Moreover, it is demonstrated that the program disturb effect in modern NAND-Flash memories can be modeled accurately and efficiently using a concurrent multi-scale model based on the DD model, a nonlocal BBT model, and a post-processor MC model for modeling hot electrons and holes. Finally, based on the historic development of the spatial discretization of the DD model, it is shown how important it is for the control of the discretization error on coarse grids to preserve the monotonicity properties of the underlying partial differential equations in the final discretized model. The authors believe that this observation

should serve as a guideline for the development of discretization methods for transport models in the future.

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Charge Transport Models for Amorphous Chalcogenides

40

Rossella Brunetti and Massimo Rudan

Contents

40.1 Amorphous Semiconductors 1452

40.2 Atomic Structure and Electronic States 1454
40.2.1 Atomic Structure of Amorphous and Crystalline Chalcogenides 1454
40.2.2 Electron States in Amorphous and Crystalline Chalcogenides 1456
40.2.3 Resistance Drift 1457

40.3 Physical Models and Numerical Approaches to Charge Transport 1458

40.4 Microscopic Models 1461
40.4.1 A Hydrodynamic Approach to Trap-Limited Transport 1461
40.4.2 Inclusion of Dispersive Band States 1464
40.4.3 Detrapping Due to Electron-Electron Interaction 1467
40.4.4 3D Simulation on a Random Network 1469
40.4.5 Inter-Trap Transitions 1472
40.4.6 Ab Initio Quantum Transport Models for Ultrascaled Chalcogenide Devices 1473

40.5 Macroscopic Models 1476
40.5.1 Macroscopic Modeling of PCM Oscillations 1478
40.5.2 Measuring PCM Characteristics in the Amorphous Phase 1479
40.5.3 Thermal Analysis of the PCM 1481
40.5.4 Comparison with Experiments 1482
40.5.5 Stability Analysis of PCM Oscillations 1482

40.6 Open Challenges in Modeling: A Brief Outline 1485

References 1486

Abstract

The chapter addresses the issue of transport models applied to the amorphous chalcogenides which, in the last decades, have acquired importance in the design and manufacture of solid-state memories. After an introductory part where the main properties of the materials are outlined, ab initio atomistic, and semiclassical computational approaches for the study of the atomic structure and the features of electronic states of chalcogenides are briefly illustrated. This part is concluded by a description of the resistance-drift phenomenon and of how the simulation approaches contributed to the comprehension of the underlying physics.

The successive section summarizes a variety of physical models and numerical methods useful for describing charge transport in the materials. The issue is developed in the two subsequent sections, dealing with microscopic and macroscopic models, respectively. The first section of the pair addresses the trap-limited transport model in the hydrodynamic form and discusses a 3D network of randomly placed traps. Specific issues, like detrapping due to electron-electron interaction and the probability of inter-trap transitions, are addressed here. Finally, ab initio quantum models for ultrascaled devices are illustrated.

The last section deals with measuring schemes for the negative-slope branch of the $I(V)$ characteristic of the amorphous chalcogenide and with a method suitable for describing the instability due to this branch; the section is concluded by a macroscopic thermal analysis of a PCM. A brief outline of open problems and challenges in modeling transport in amorphous chalcogenides closes the chapter.

Keywords

Amorphous semiconductors · Chalcogenides · Atomic structure of chalcogenides · Electron states in chalcogenides · Microscopic transport models for

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chalcogenides · Ovonic switching · Phase-change memories (PCM) · Macroscopic transport models of PCM · Hydrodynamic model

40.1 Amorphous Semiconductors

Even though the majority of conventional electronic and optical devices exploit the physical properties of semiconductor materials in their crystalline form, amorphous semiconductors, like amorphous Silicon (a-Si) and related materials, together with chalcogenide alloys, have also been variously employed, albeit to a lesser extent, in technological applications, like solar cells, thin-film transistors, light sensors, and optical memory devices, just to quote some examples [1–5]. A recent compact and clear review on the fundamental concepts about structural, optical, and electrical properties of amorphous semiconductors is found in [6].

The first relevant scientific and technological focus was on light-induced phenomena, in particular the dark conductivity and photoconductivity in the a-Si:H material: both properties exhibit a decrease of their values after long illumination of band-gap light [3]. These effects have been studied in view of the associated performance degradation of the optoelectronic devices based on these materials. Details about the use of amorphous semiconductor materials for the realization of solar cells and sensors are found in [4] and, in this book, in Chaps. ▶ 19 by S. Goodnick and C. Honsberg, and ▶ 21 by J. Li and M. Östling. Furthermore, the tunable optical properties of a class of chalcogenide alloys, ranging over several orders of magnitude from the amorphous to the crystalline phase, gave impulse to the industrial exploitation, that is today a mature technology, for rewritable optical data storage and display devices [7]. In the last years, chalcogenide-based photonics has emerged as a new research topic, where the extremely efficient switching of chalcogenide phase-change materials under short optical pulses is exploited to implement light engineering. The interested reader can refer to [7] and references therein for a recent review on the subject.

As for the electrical properties of amorphous semiconductors, the pioneer literature published from the 1960s to mid-1980s established that both band and hopping conduction contribute to determine the material response to an external bias. The temperature dependence of the Ohmic conductivity σ is the "fingerprint" of the prevalent effect:

$$\sigma \propto \exp\left(-\frac{E_a}{kT}\right) \tag{40.1}$$

for band conduction in undoped amorphous semiconductors (with E_a the activation energy, k the Boltzmann constant, T the temperature), and

$$\sigma \propto \exp\left(-\frac{B}{T^{1/4}}\right) \tag{40.2}$$

for (nearest-neighbor and variable-range) hopping, with B a coupling parameter [1]. The former mechanism dominates at room temperature; the latter prevails at low temperature.

A renewed interest of the scientific community and the electronic industries on the extremely tunable nonequilibrium electrical properties of chalcogenides has been observed in the last 20 years, due to the foreseen range of applications [8–11]. This strong focus on the topic brought about a wide-range exploration of possible materials to be employed, an increasing control of the growing techniques, and a decrease in the dimensions of the material layers. Some performance limitations of the experimental characterization equipments have been overcome in order to meet the new issues brought about by this quickly expanding field; new alloys were grown, and their properties were tailored for specific purposes; thinner active regions were considered to the purpose of improving the device performances. The increasingly important role of metallic contacts has been explored down to the atomic level, in order to define the miniaturization limit at which the functionality of the devices is still preserved.

Innovative device architectures based on these materials, both in the amorphous and crystalline phase, have been proposed for memory elements, and their scaling to the nanometer range opened the way to the realization of 2D and 3D arrays with potentially new fields of application [12]. The process technology involved in the realization of these devices is extensively described in [8] and, in this book, in Chap. ▶ 2 by P. Fantini et al.; an overview of phase-change memory device physics can be found in [13], while new possible applications of chalcogenide-based memory devices are found in [12].

Another emerging field where chalcogenide materials are foreseen to play a relevant role is neuromorphic computing. Here, chalcogenides are employed to design memristive devices, i.e., devices that integrate memory and elaboration functions. The subject is treated in detail in this book in Chap. ▶ 32 by D. Ielmini. This topic is still rapidly evolving and is, so far, the most innovative and "trendy" one as for architecture design and modeling.

The impressive scientific and technological driving force described above brought about new challenges in the field of material and device modeling. Many different approaches have been adopted, ranging from compact models down to atomistic simulations. On the basis of the arguments discussed above, the present chapter will review the modeling approaches applicable to the analysis of the electrical properties of amorphous chalcogenides for device applications. The same approaches can be applied to the study of other amorphous semiconductors that share similar structural properties and electronic states.

Generally speaking, while a deep theoretical understanding of the most fundamental aspects related to electronic states and charge-transport properties of crystalline semiconductors and devices has been reached, many open issues still remain about the same topics as far as amorphous semiconductors are concerned, despite the huge amount of experimental and theoretical literature of the last years.

As for all amorphous materials, the electronic properties of amorphous semiconductors are difficult to study with the experimental techniques commonly applied to crystalline materials, since broken symmetries in the atom distribution of the disordered network make the spectral lines to broaden. For the same reasons, mathematical and numerical modeling of the atomic arrangement and of the electronic states, at the basis of any transport approach, is a formidable task also for amorphous chalcogenides; among several issues under debate, we quote two very basic questions, still open: (1) to what extent the "extended" band states influence the transport process in the amorphous phase? and (2) what is the microscopic origin of the trapping and recombination centers?

Focusing now on the charge-transport issues, the peculiar effects characterizing the amorphous phase of most chalcogenides can be summarized as follows:

(a) The $I(V)$ characteristic exhibits a linear dependence near the origin, followed by an exponential behavior.
(b) At a threshold field, mainly determined by the type of chalcogenide at hand, a sudden increase in conductivity (often of several orders of magnitude) sets in, while the material is still in the amorphous phase. The phenomenon is called "OTS".
(c) The transition from low- to high-conductivity state is an ultrafast phenomenon, taking place in the picosecond/-subpicosecond timescale.
(d) If, after the OTS, the external bias is reduced below a given value called *holding voltage*, in absence of memory switching, the amorphous chalcogenide returns to the initial conductivity state.
(e) The OTS behavior is maintained when the amorphous chalcogenide cell geometry is scaled down to the nanometer size.
(f) A slow increase of the electrical resistance of the amorphous phase with time (referred to as *resistance drift*) is observed for most amorphous chalcogenides.

Point (b) above is by far the most relevant one for the applications. The process described in it is referred to, in the literature, as "Ovonic threshold switching" or "OTS," and the $I(V)$ characteristic becomes S-shaped (equivalently, the $V(I)$ characteristic is N-shaped). In many cases, OTS is followed by a phase change to a crystalline state. Since such a transformation is exploited in the phase-change memory (PCM) technology, this second change is sometimes called "memory threshold switching" or "MTS." In some cases, instead, OTS is not followed by a phase change; however, when phase change occurs, it is favored by OTS, since the increase in conduction increases the Joule power absorbed by the material, thus favoring the temperature rise necessary for the phase change. When chalcogenide materials are used as PCM, the amorphous-to-crystal transition induced by a suitable electric pulse is called *set*; the opposite transition is called *reset*.

It must be remarked that OTS may occur or not, depending on the details of the carrier energy states within the specific amorphous material. The physical origin of the electrical bistability observed in some amorphous semiconductors is still a matter of debate, as discussed in this chapter and its references. However, no matter what the invoked explanation is (viz., electrical, thermal, or electrothermal, as extensively discussed in the chapter), in all cases the effect is strictly related to the extended and/or localized distribution of the electronic states in the amorphous material. Chalcogenides seem to possess two "key" ingredients, namely, a wide band gap and a distribution of more or less localized states in the band gap. To clarify this point, Buscemi et al. [14] analyzed the abovementioned bistability by an analytical approach; they found that the electric snapback may occur only when the energy separation between the electron localized and free states is larger than $4\,k\,T_\circ$, where k is the Boltzmann constant and $T_\circ$ the lattice temperature. This clarifies why bistability is generally not observed in the most popular elemental and compound semiconductors, where a high density of localized states deep in the gap is not present.

A recent concise review on the measured transport properties, their technological relevance, and the physical effects possibly influencing transport in chalcogenides is found in [15]. Extensive experimental investigations produced an impressive amount of data for a large number of chalcogenide alloys that have been used to test and validate the simulation models.

The contents of the chapter are organized as follows. In Sect. 40.2 we present a short review of the most relevant theoretical concepts and computational approaches about the atomic structure and electronic states of the amorphous chalcogenides, selected from about 20 years of advanced basic and applied research. In Sect. 40.3 and in the following ones, we present an overview of the physical models and the numerical approaches proposed by the scientific community to study the transport properties of amorphous chalcogenide materials and devices, ranging from the microscopic transport models, including atomistic ab initio simulations (Sect. 40.4), to macroscopic models solved by finite-element numerical techniques (Sect. 40.5). The theoretical predictions will be validated against experimental results for state-of-the-art devices. A number of still open questions

on the fundamental physics at the origin of the electrical performances of amorphous chalcogenides, along with some future trends for the modeling methodologies, will be drawn in Sect. 40.6, based on the present research achievements.

40.2 Atomic Structure and Electronic States

Understanding the atomic structure and the distribution of electronic states of amorphous chalcogenide materials is of fundamental importance for any study of charge transport and for device applications. In fact, the knowledge of the atomic structure is crucial for understanding, and possibly tailoring, the phase change and the consequent memory switching of chalcogenides; in turn, the distribution of the electronic states crucially influences the charge-transport properties of the amorphous phase, in particular the OTS phenomenon.

In the following sections, the two topics will be briefly reviewed on the basis of the most recent theoretical, experimental, and computational achievements appeared in the literature, with the purpose of providing the reader with the basic concepts used to discuss transport features of amorphous chalcogenides in the rest of the chapter.

40.2.1 Atomic Structure of Amorphous and Crystalline Chalcogenides

Owing to the lack of long-range order, the structure of amorphous materials is usually studied in terms of short- and medium-range properties. Statistical quantities, such as form factors, correlation functions, and coordination numbers, contribute to the identification of some characteristic units or building blocks which describe the short-range structural properties of the amorphous phase. From the experimental side, the above properties can be studied by means of neutron scattering, Raman scattering, X-ray diffraction (XRD), far IR absorption, photoemission, or extended X-ray absorption fine structure (EXAFS) (see, e.g., [5, Ch. 46]), which yield information on the space distribution of constituent atoms. However, the experimental analysis of the amorphous chalcogenide materials is particularly difficult, since they quickly switch to the crystalline state without stabilizing themselves to a solid glass, being this rapid phase change the property that makes these materials so interesting for memory applications [8].

In the last two decades, a strong effort has been devoted to obtain information on the structural properties and the electronic states of amorphous chalcogenides, using computational approaches based on atomistic models (the interested reader is referred to [16] for an extensive review on the subject). The numerical findings about the space distribution and

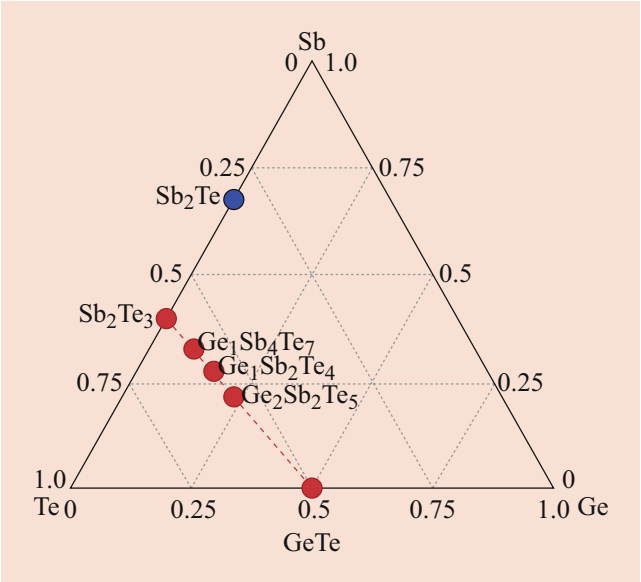

Fig. 40.1 Pseudo-binary alloys of GeTe and Sb_2Te_3. (Reprinted with permission from [23]; copyright ©2010 American Chemical Society)

the bonding features can be validated against experimental observations by means of the statistical quantities mentioned above (for further details, see, e.g., [17, 18]).

Calculations have been performed for several materials, but the most studied chalcogenide compounds are GeTe (the simplest phase-change material), Sb_2Te_3 and ternary materials, such as $Ge_2Sb_2Te_5$ (GST–225) and $Ge_1Sb_2Te_4$ [17, 19–22]. Among them, GST–225 is the material most used for memory applications, since it provides a good compromise between a high speed of the phase transition and a good stability of the amorphous phase. Moreover, many GeSbTe ternary alloys have been studied. They are regarded as pseudo-binary alloys of the compounds GeTe and Sb_2Te_3. In Fig. 40.1 three examples are shown, namely, $Ge_1Sb_2Te_4$, which is considered as $(GeTe)_1(Sb_2Te_3)_1$; then, $GeSb_4Te_7$, which is considered as $(GeTe)_1(Sb_2Te_3)_2$; and finally, $Ge_2Sb_2Te_5$, which is considered as $(GeTe)_2(Sb_2Te_3)_1$. In recent years, ab initio molecular dynamics has been the most advanced numerical method applied to predict or test the atomic distribution in amorphous (and crystalline) chalcogenides. Details on the fundamentals of this simulation technique are found in [8] and in Chap. ▶ 42 by M. Fischetti et al. Focusing on GeTe and GST–225, results show [17] that both compounds in the amorphous phase, obtained by quenching from the liquid phase, display two different types of short-range order: about 30% of the Ge atoms show tetrahedral sp^3 bonds promoted by the presence of Ge-Ge bonds, as in elemental or III-V semiconductors; the remaining Ge atoms, linked to Sb and/or Te chalcogen atoms, tend to form 3-coordinated or 4-coordinated defective octahedral orthogonal p bonds. The three corresponding

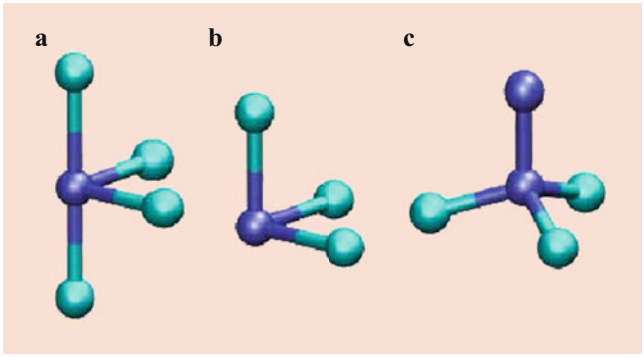

Fig. 40.2 Building blocks of a-GeTe (blue spheres represent Ge, light-blue spheres represent Te): (**a**) defective octahedra, (**b**) pyramids, and (**c**) tetrahedra with Ge-Ge bond. (After [22])

building blocks are shown in Fig. 40.2. The tendency of Ge atoms to form octahedral environments, reminiscent of the cubic crystalline phase, can be understood by noting that the main difference between the complex atomic structures of chalcogenide alloys with respect to that of the most common and well-known semiconductors of group IV or III–V is that, in the latter, a strong sp_3 hybridization of orbitals is present, whereas it is absent in the chalcogenide alloys. In fact, sp_3 hybridization is forbidden due to the large energy difference between the *s* and *p* orbitals produced by the stronger Coulomb attraction of the nuclei of group VI. Therefore, the bond is provided by the *p* orbitals, while *s* orbitals do not participate [24, 25]. This bond configuration favors the octahedral, rather than tetrahedral, structure. The crystalline octahedral structure, however, is not stable in GeTe and ternary alloys: it is followed by a Peierls distortion that generates a more stable trigonal symmetry. The energy gained by the Peierls distortion is larger than the elastic energy necessary to maintain the distortion (Fig. 40.3).

Furthermore, simulations in [20] reported for the amorphous phase a long-range order of Te atoms and an important structural motif consisting of four-membered ABAB squares, where A stands for atoms of Ge and Sb, and B stands for Te. A detailed analysis of possible bonds in Ge-Te-Sb alloys, on the basis of the electronic configurations of the atoms involved, is given in [5, Ch. 46]. This analysis suggests that the fast crystallization and high cyclability between amorphous and crystalline phases are related to small atomic displacements producing ordering (disordering) of pre-existing four-membered rings, with preservation of the covalent backbone. The concentration of vacancies in GST–225 is found to be larger than in GeTe. The reduction of imperfections in an amorphous chalcogenide favors the phase transition to the crystal, since vacancies provide the necessary space for atomic readjustment. This explains why phase-change performance in GST–225 is better. A combination of various experimental results with theoretical

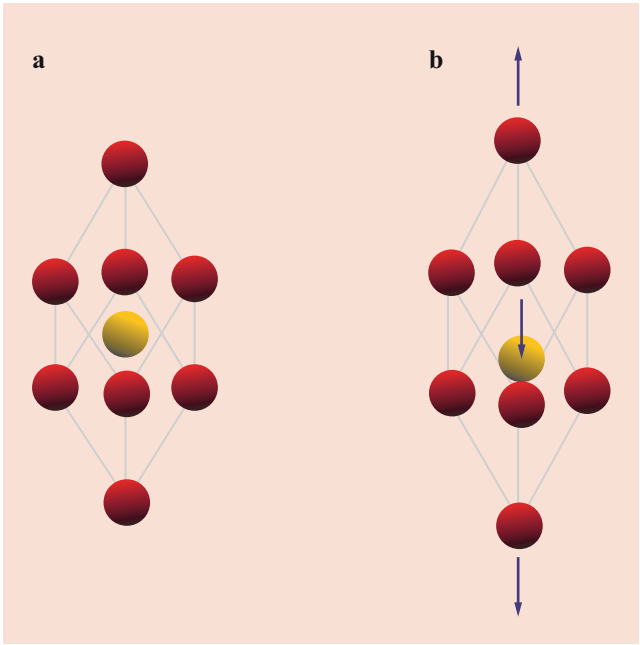

Fig. 40.3 Rock-salt structure (**a**) and trigonal structure (**b**) of GeTe in the primitive unit cell. The trigonal structure is obtained by stretching the rock-salt cell along the ⟨111⟩ direction and shifting the central atom. (Reprinted with permission from [23]; copyright ©2010 American Chemical Society)

interpretations by means of reverse Monte Carlo calculations [18, 26] confirmed that a variety of local motifs are present, without a predominance of tetrahedral $GeTe_4$, as previously suggested by [27]. Furthermore, EXAFS spectra proved that Ge-Te and Sb-Te bonds are shorter for the amorphous phase, even though the density of the latter is about 5% lower than that of the crystalline phase; this suggests that a significant change occurs in the local structure from the amorphous to the crystalline phase [5, Ch. 46].

As it regards the transition from the amorphous to the crystalline phase, recent experimental and theoretical findings [28] evidenced that, contrary to the case of the amorphous phase characterized by ordinary covalent bonding, the bonding mechanism in crystalline phase-change materials cannot be classified according to the conventional bonding theory: a novel bonding structure, named "metavalent bonding" [29, 30], has been suggested.

As far as symmetry properties are concerned, crystalline GeTe exhibits a stable rock-salt crystalline structure (Fig. 40.3a) at temperatures above about 400 °C. One sublattice is occupied by Te atoms and the other by Ge atoms. At lower temperatures, below about 200 °C, a phase transition occurs to a still rock-salt crystalline structure, which is unstable and relaxes to the trigonal structure (referred to above as Peierls distortion, Fig. 40.3b). Furthermore, a shift of the central atom along the [111] direction is present, generating alternating short and long

bonds; finally, in this stable structure, a large number of Ge vacancies are present [31]. Several authors suggested that vacancies stabilize the structure by decreasing the total energy of the system; they are not electronic defects but are an intrinsic feature of the atomic structure. This is the case, for example, of the GST–225 rock-salt structure ([27], [5, Ch. 46] and references therein). EXAFS studies [27] proved that the local structure around the Ge species is very similar to that of the binary Ge-Te, which possesses a rhombohedral structure with subsets of free-shorter and free-longer bonds. Peierls distortions are also present in GST–225. The stable structure of these ternary alloys is a layered trigonal structure. One sublattice is occupied by Te atoms, while the other is occupied by Ge atoms, Sb atoms, and vacancies [8]. A large vacancy concentration has been observed in several pseudo-binary alloys along the GeTe $-$ Sb_2Te_3 line. For the case of $GeSb_2Te_4$, e.g., the stacking order suggested in [32, 33], consists of alternating blocks of GeTe and Sb_2Te_3 (see also [8]).

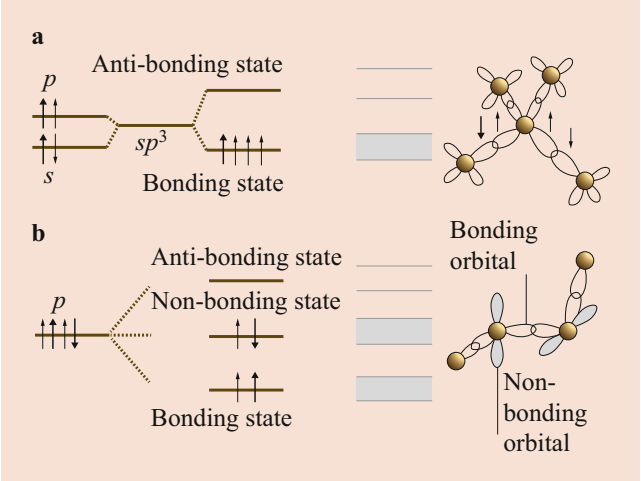

Fig. 40.4 Schematic description of atomic, hybridized orbitals and bands (**a**) for tetrahedrally coordinated amorphous semiconductors (e.g., a-Si) and for (**b**) amorphous chalcogenides (e.g., Se). (After [6])

40.2.2 Electron States in Amorphous and Crystalline Chalcogenides

In crystalline semiconductors, the electron energy structure consists of energy bands and gaps; the corresponding energy wave functions are Bloch states, extending over the whole crystal. Localized electron states in highly ordered systems are usually associated with donor or acceptor dopants, impurities, or structural defects and introduce discrete energy levels within the semiconductor band gap. In disordered semiconductors, like amorphous chalcogenide alloys, extended and localized states still exist, but the electron energy distribution has different features. Usually, electronic states in amorphous semiconductors are described by means of a tight-binding, Hartree-Fock approach, with the introduction of spatial fluctuations of the bond arrangement (e.g., length and angle). In the particular case of chalcogenides, starting from p-type atomic orbitals, which produce hybridized bonding, non-bonding, and anti-bonding states, the valence band is generated by the non-bonding state, while the conduction band arises from the anti-bonding state (Fig. 40.4). The energy gaps of amorphous materials are usually larger than those of crystals. The spatial fluctuation of the bond energy leads to a broadening of the edges of the conduction and valence bands and introduces energy levels associated to localized states; the latter reduce, or completely fill, the energy gap (Fig. 40.5). In general, the energy density of states (DOS) of electrons and holes decreases moving toward the mid-gap, generating energy tails commonly referred to as "Urbach tails." The energy that separates the extended from the localized states is called "mobility edge." Electron (hole) states above (below) the mobility edge are extended states, while electron (hole) states below (above) the mobility edge are spatially localized. The mobility gap of amorphous materials is defined as the minimum energy separation between the extended states of the valence and conduction bands ($\varepsilon_c - \varepsilon_v$ in Fig. 40.5).

Furthermore, in amorphous semiconductors the coordination number of constituent atoms deviates from that of the ideal random network. In chalcogenide glasses this number is 2. Onefold- and threefold-coordinated chalcogen atoms are called *valence-alternation pairs* (VAP, Fig. 40.6); they constitute structural defects with associated electron energy levels within the band-gap region. Moreover, donor- and acceptor-like trap states may be present in the amorphous materials as well.

The knowledge of the energy spectrum of amorphous chalcogenides is, of course, of extreme relevance for any charge-transport analysis. A large number of experimental techniques based on optical and electrical measurements have been applied [6] and confirmed the general features discussed above for a large number of amorphous chalcogenides. As an example, measurements of steady-state photocurrent (SSPC), modulated photocurrent (MPC), and Seebeck effect for the case of a-GeTe have been performed in [35]; from an elaborate analysis of the experimental results, an electron DOS for the samples under investigation, shown in Fig. 40.7, was calculated and found consistent with the obtained experimental data. However, in many cases the experimental information about the energy spectrum and the (extended or localized) nature of the electron wave functions close to the mobility edges and within the mobility gap is not accurate enough to provide reliable grounds for a transport theory.

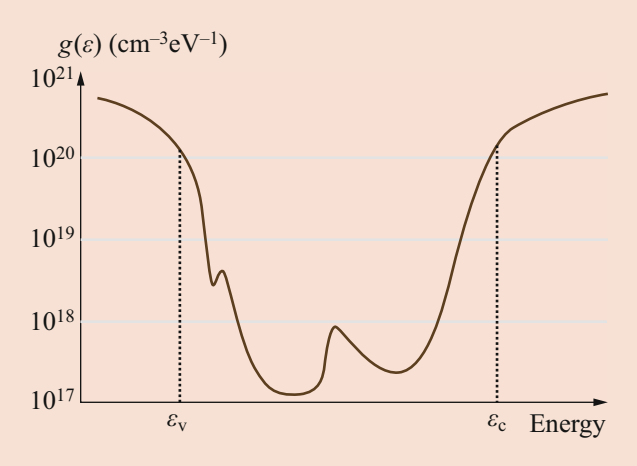

Fig. 40.5 Sketch of a typical energy density of states for a disordered semiconductor; here, ε_c and ε_v indicate the conduction and valence mobility edges, respectively (see text). (After [34])

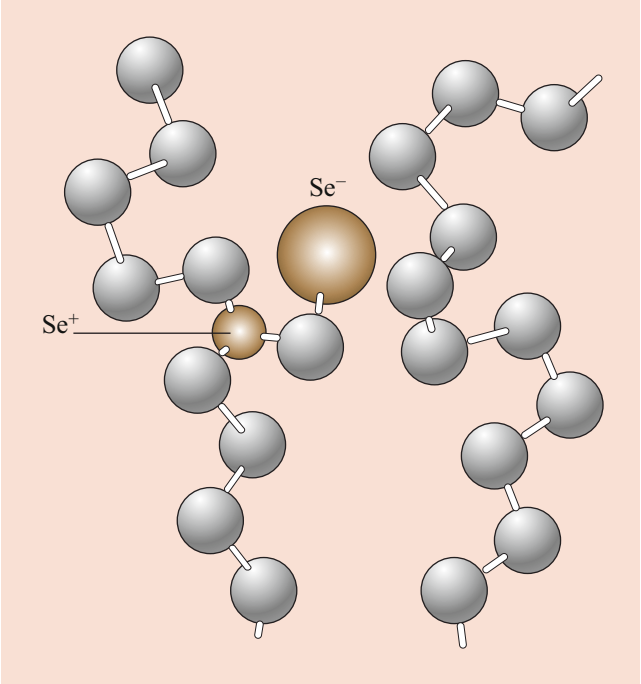

Fig. 40.6 Sketch of onefold-coordinated (negatively charged) chalcogen atom and threefold-coordinated (positively charged) chalcogen atom. The case of Se has been considered. (After [6])

Atomistic calculations are also very challenging, since the high accuracy in the determination of the DOS, necessary for investigating transport phenomena, requires large cells and a huge number of atoms, resulting in very heavy computational loads. Simulations of GeTe in [36] showed that localized states inside the gap in phase-change materials mostly come from band tails and are due to Te atoms; they also confirmed that the Fermi energy for these materials is located at mid-gap, in agreement with experimental findings.

Among chalcogenides, a-GeTe has extensively been studied by many groups; DFT and classical MD simulations in [37, 38] suggest that most of the localized states in the band gap of this chalcogenide alloy are introduced by defective groups of Ge atoms, in which at least one Ge atom is over- or under-coordinated. During the structural relaxation following a fast quenching, a slow time evolution of the bond spatial arrangement has been observed toward lower-energy structures, having a nearest-neighbor distribution similar to that of the crystalline phase, with a reduction of the localized states. For the same chalcogenide, a distribution of defect states in the gap, whose localization decreases as the energy of the states gets closer to the band edges, has been obtained [22]. Such states are connected with chains of Ge-Ge homopolar bonds.

40.2.3 Resistance Drift

An outstanding example of how atomistic, physics-based approaches can successfully be applied to analyze, and possibly overcome, technological limitations in semiconductor device design is provided by the resistance-drift effect.

The technology of PCM devices exploits the resistance difference between the crystalline and amorphous phase of chalcogenide materials; while the former is characterized by a stable resistance, the amorphous phase is characterized by a time instability of the resistance, due to two different phenomena: crystallization at high applied fields and the so-called *resistance drift* (RD) [39–41] at low fields. The latter effect is an irreversible phenomenon, present in amorphous chalcogenide materials, by which the electric resistance R of an amorphous sample slowly increases with time; RD is of course very relevant from the technological point of view: it is in fact a detrimental phenomenon for the memory applications of chalcogenides, particularly for multilevel-storage devices [42].

The phenomenological formula that accounts for the resistance change with time is

$$R(t) = R_0 \left(\frac{t}{t_0}\right)^{\nu}, \tag{40.3}$$

where $R_0 = R(t_0)$ and ν are material parameters. Even though the physical origin and dynamics of RD are not fully understood yet, there is a consensus that the effect must depend on changes in the atomic and electronic structures of the amorphous phase that take place in time. As a consequence, different atomistic approaches have been applied to the purpose of explaining the RD effect, and the study of RD has often merged with the study of atomic structures, being the RD experimental data a validation check of the adopted atomistic model.

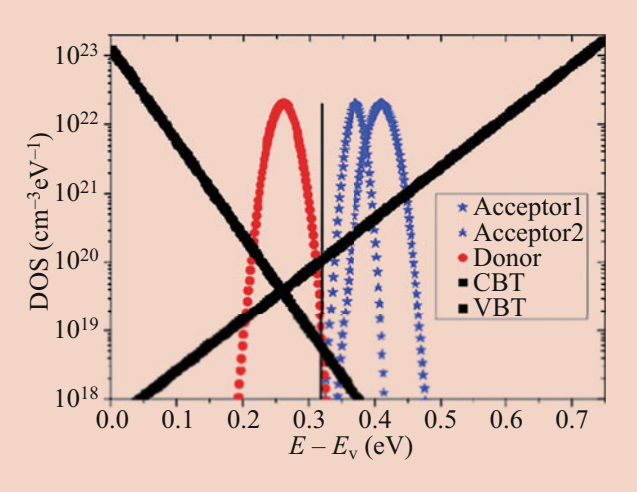

Fig. 40.7 Density of states as a function of energy for a-GeTe films obtained from numerical calculations reproducing experimental results. (After [35])

The first atomistic studies linked the origin of RD to a time-dependent, structural relaxation effect related to the stress in PCM systems after the reset operation, also depending on the sample history [43, 44] (the reset operation is defined in Sect. 40.1). However, stress has not been confirmed to be present in all chalcogenides, and RD has been found also in systems where stress is not present [45]. Furthermore, RD cannot be ascribed to partial crystallization taking place while devices are operated, since crystallization would bring a decrease, not an increase, of resistance.

Recently, a number of independent analyses based either on ab initio or classical potential molecular dynamics agreed in identifying the physical origin of RD as structural aging, i.e., a structural relaxation with time of the nonequilibrium, metastable amorphous materials, independent of the presence of stress [39, 46–49]. In particular, according to the theoretical model in [47], the structural relaxation process to a lower-energy, still amorphous phase, is associated with the decay of metastable defects during structural relaxation, with a consequent enhancement of the electron activation energy for conduction; this effect produces an increase of the resistance with time. The hypothesis, evidenced by atomistic structural calculations, was validated by comparing the theoretically predicted power exponent ν of RD in (40.3) with experimental data. An additional confirmation of this idea came from time-dependent ellipsometric measurements in a-GST [49], which have shown that RD is correlated to a band-gap widening, supporting its origin as due to a structural relaxation with atomic rearrangements of the amorphous material. In particular, such a relaxation determines an increase of the energy gap and a reduction of the number of localized states within the gap. Both these occurrences contribute to an increase of the resistance.

For the sake of completeness, it must be mentioned that a different explanation of this effect has been given assuming that RD is related to material changes induced by an external electric bias, rather than an intrinsic structural effect ([42] and refs. therein). In a first study based on amorphous GST, the increase of resistance with time was ascribed to a parallel increase of the density of a class of charged, coupled, and localized defects of the chalcogen atom (Te)—the *valence alternation pairs*, or VAP, mentioned above—induced by the drift phenomenon [39]. However, atomistic simulations based on molecular dynamics proved that atomic configurations associated with gap defects in amorphous chalcogenides are not simple VAP point-like defects, being instead spatially extended and with different energy shifts when occupied by electrons.

In a recent study, RD of amorphized GST line cells has been studied as a function of the sample temperature, from room temperature down to 125 K, where structural relaxation effects are expected to be much smaller than at room temperature; RD was detected in the full range of temperatures [50]. In the same study, the time evolution of RD of illuminated and non-illuminated samples was compared. The photoexcitation effect taking place under light exposure gives rise to a clearly observable change in resistance and to lower drift coefficients, suggesting that photoexcited carriers give a significant contribution to conductance at low temperatures. Experiments with periodic exposure to light evidence the existence of two different responses, one fast and one slow. The timescale of the slow response (about 10 min at 150 K) suggests that slow trap-to-trap charge exchanges have a significant impact on electrical conductivity and that the resistance can be stabilized under light exposure within each cycle; this seems to confirm that RD, at least in amorphous GST, is predominantly an electronic process.

In Ref. [42] the intrinsic electronic mechanism for RD is identified with the long-time, deep-trap release and subsequent recombination of charge carriers following electron-hole injection during the reset pulse; the phenomenon is also believed to be responsible for the long-time photocurrent decay in amorphous semiconductors, such as hydrogenated amorphous silicon. The effect is controlled by the energy width of the (localized) valence and conduction band tails in the vicinity of the band gap.

40.3 Physical Models and Numerical Approaches to Charge Transport

The first general microscopic theory of charge transport in amorphous materials was developed by Mott in the late 1960s (see, e.g., [1,51]). It represents a milestone in the field and has been widely and successfully applied, since then, to a variety of amorphous materials.

On the other hand, the Mott theory, being based on the hypothesis of hopping conduction, does not fully explain the peculiar features of transport in some chalcogenide glasses: specifically, a reversible electrical switching behavior, i.e., a sudden change in resistivity by several orders of magnitude when a threshold field is reached, with no transition to the crystalline phase. This effect was first evidenced by Goryunova and Kolomiets in 1955 [52], but only in 1968 Stanford Ovshinsky brought it to the attention of the international scientific community [53]. For this reason the phenomenon is commonly referred to as "Ovonic threshold switching" (OTS). In the last 30 years, the switching behavior of the amorphous state of chalcogenide materials proved to be of great interest for the technology of phase-change memories (PCM) [54], so that the study of electron transport in the amorphous state and the associated computational implementations raised renewed interest.

The theoretical approaches can be grouped on the basis of the prevailing mechanism used to describe the Ovonic swiching [55]. Several mechanisms have been proposed, and some of them can possibly be present at the same time with different relative importance in different materials and experimental conditions.

The first systematic study was presented by Adler in the late 1970 [56, 57]. Both electrons and holes are considered as mobile carriers, and charged trapping centers are included. When the threshold field is approached, extra pairs of carriers are generated via impact ionization, which are captured by the majority of traps and make them neutral. Since carriers are generated throughout the whole sample, some enter the external circuit instead of filling a trap and produce a significant current. The latter, in turn, can produce filamentation prior to the switching transition. Highly conductive micrometer-size filaments are thus created, which constitute privileged pathways for the electric conduction that dramatically decrease the electric resistance of the material.

The nucleation model proposed in [58, 59] is based on the assumption that a high electric field lowers the energy barrier to the point that the formation of a crystal nucleus becomes possible. A number of crystalline grains are then created within the amorphous matrix because of local energy dissipation; they do not alter the conductivity properties as long as they are far away from each other. A strong electric field and/or an external heat source enhance the formation of these grains so that, under suitable conditions, a conductive filament connecting the contacts is formed. This low-resistivity path produces the Ovonic switching observed in the $I(V)$ characteristic of the amorphous material. This hypothesis is supported, on one hand, by the fact that the conductivity of such materials, being thermally activated, increases exponentially with temperature; on the other hand, this mechanism is too slow to account for the experimental observations of the typical switching speed. Furthermore, the complexity of the reaction kinetics and the dimensions of the filaments are not compatible with the performances of the present-day Ovonic devices. Thus, new models were considered.

In the model proposed in [60], states with negative correlation energy are supposed to play a key role in determining the electric switching (the correlation energy is the sum of the electron positive-repulsion Coulomb energy and the negative energy interaction with the lattice). These states are usually referred to as *U-centers* and are modeled as defects in glassy semiconductors. Electric switching results from multiphonon tunneling ionization of U-centers, due to the electric field and Joule heating [55]; a high concentration of such centers is in fact present in chalcogenide glasses.

In [61], a thermally assisted, threshold-switching behavior is described by means of a modeling approach consisting of a feedback between electric transport and thermal models based on phenomenological equations. Using a field- and temperature-dependent subthreshold-conductivity model coupled with thermal feedback, a thermally assisted, threshold-switching dynamics is demonstrated in nanometer-scale devices. In fact, the high thermal efficiency and fast thermal dynamics of chalcogenide devices at the nanometer scale support the idea that a self-heating mechanism can trigger the electric response.

Other approaches assume purely electric phenomena. Pirovano et al. [62] departed from the common framework for charge transport in semiconductors and tried to describe the Ovonic switching by assuming the existence of trap states in the energy gap of the amorphous chalcogenides. These states favor transitions between the valence and conduction bands (band-to-band impact ionization is, instead, a very improbable process due to the width of the gap). The generation process increases at increasing biases, while the recombination rate is only weakly dependent on the applied field. As a consequence, when generation prevails over recombination, a net increase of the high-mobility carriers produces a drastic change in the electric behavior. Even with the assistance of intermediate trap states, however, the energy required by the carriers in order to impact ionize is still very high and incompatible with the estimated carrier mean free path in chalcogenide glasses, even though the inclusion of a cooperative electron-electron interaction can mitigate the problem (Sect. 40.4.3 and [63]). Furthermore, the impact ionization mechanism cannot correctly account for the experimentally demonstrated existence of an activation energy.

In [64, 65], electrical transport in chalcogenide glasses is analyzed by means of numerical estimates. In the presence of a large concentration of localized states in the energy gap, three electron transport processes involving localized states can take place (Fig. 40.8). Tunneling through the energy barrier between two localized states, without entering the

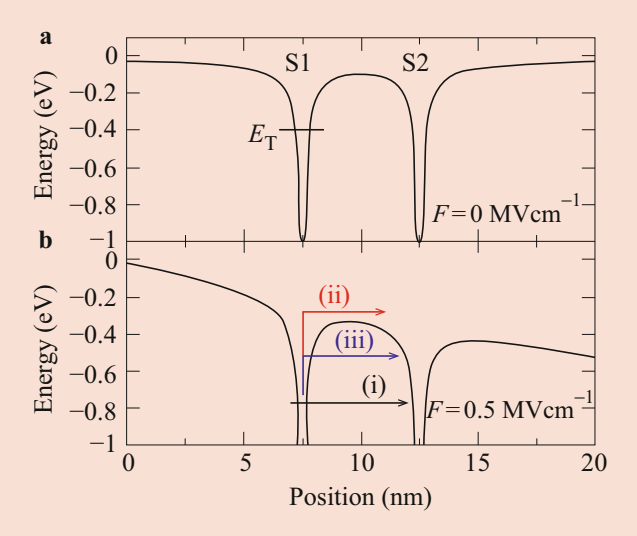

Fig. 40.8 (**a**) Profile of the electron potential energy along the minimum path between two localized states S1 and S2 in absence (*upper part of the figure*) and (**b**) presence (*lower part*) of an electric field. In the lower part, three different transport processes are sketched, namely, (**i**) direct and (**iii**) thermally assisted tunneling through the energy barrier between the two localized states, (**ii**) trap-limited transport. (After [65])

conduction band (process (i) in the figure), happens under the assumptions that (a) traps are spatially very close to each other, and (b) the energy barrier between two localized states is much smaller than the energy difference between the trap level and the bottom of the conduction band. Furthermore, field-assisted emission over the energy barrier with activation of band transport (process (ii) in the figure) and thermally assisted tunneling through the energy barrier (process (iii)) can take place as well.

Numerical estimates of the three mechanisms described above proved that tunneling is practically negligible as compared to thermally assisted tunneling and field-assisted emission over the barrier. Moreover, it has been shown by Monte Carlo simulations that transitions between two localized centers generate successive back and forth jumps between the two centers, which contribute to the high-frequency noise, but do not contribute significantly to transport: the two centers behave de facto as a single trap [66]. The contributions of the last two processes are, instead, comparable for typical trap levels and energy gaps in amorphous chalcogenides. The two mechanisms are treated with a unified theoretical approach, and they have been referred to as "thermally assisted hopping" [65] or "trap-limited conduction" [64,67,68] when carriers transfer to band states between successive capture events. In any case, carriers transfer from one trap to another in a time which is much shorter than the time they spend within the trap. At equilibrium, detrapping events in any direction are equally probable; when an electric field is applied, the energy profile around each trap is modified, and the transition probability for some transitions is exponentially enhanced or decreased. At high electric fields, an almost one-directional carrier flux is eventually observed with the formation of a heated carrier distribution, since the energy gained from the external field is not fully dissipated to the lattice. The mobility increase associated to the heating effect produces the observed Ovonic switching from a low- to a high-conductance state. The above-described assumptions have been included in a continuum-medium 1D analytical model which successfully predicts the Ovonic switching effect. The original model of [64] applies to a steady-state transport condition.

Based on the model of [64], Piccinini et al. [67] investigated the same problem by numerically solving a set of equations provided by a hydrodynamic model coupled with the Poisson equation, suitable to describe local nonuniformities which can be relevant to determine the Ovonic effect. Diffusion effects are thus taken into account, and the carrier energy distribution is self-consistently evaluated with the local concentration and average energy of the carriers, along with the charge and energy fluxes. The two abovementioned features make it possible to implement numerical simulations for real devices in steady-state conditions.

An interesting alternative approach to the continuum-medium models for trap-limited transport discussed above has been introduced by Cappelli et al. [69, 70], who simulated the microscopic time evolution preceding the onset of the Ovonic effect, and possible crystallization, through a disordered network of localized states. They considered that, due to the structure of the chalcogenide material in the amorphous phase, it is reasonable to suppose a trap-limited conduction mechanism, where electrons travel in extended states above the mobility edge between two successive capture events. The localized states are assumed to be nodes of a 3D network. The application of a strong electric field reduces the barrier to be overcome by the trapped electrons to reach the extended states (Poole [71] or Poole-Frenkel [72] effects), thus increasing the chalcogenide conductivity. The model couples the self-consistent solution of the charge-transport and energy-transport equations with that of the Poisson and Fourier heat-transport equations, thus including both electrical and thermal effects into the final results. The validation of the model against experimental data evidences that both Ovonic switching and crystallization take place after the formation of hot-carrier conduction paths inside the disordered network. This numerical approach is suitable for the study of few-carrier phenomena in small devices, or the analysis of the statistical dependence of the electrical properties on the degree of disorder of the amorphous matrix.

Based on the trap-limited transport hypothesis encoded in a set of space- and time-dependent balance equations for the

carrier charge, current, and energy, self-consistently solved with the Poisson equation for the local electric potential, Buscemi et al. proposed analytical and numerical models of increasing complexity [14, 73, 74], all including both trapped and (dispersionless) band states. Eventually, in [75] the approach has been generalized to include a band with parabolic dispersion; the last approach can be integrated into standard tools for device simulation.

As stated in Betti Beneventi et al. [76], both the Pool and Poole-Frenkel approaches include thermal emission and thermal-assisted tunneling into the transport description. In the Poole approach, traps are supposed to be strongly interacting, while in the Poole-Frenkel approach, traps are assumed not to interact. The choice of any of the two approaches is, of course, justified by the knowledge of the localized-state spatial concentration and energy distribution which, unfortunately, is not known for most of the chalcogenide materials. Furthermore, both models assume an exponential dependence of the electric current upon the barrier lowering at high fields (even if the dependence on the electric potential is different in the two cases), which seems to be a key feature of the $I(V)$ curve when the threshold field is approached. The Poole model correctly accounts for the Ohm law at low fields, while the Poole-Frenkel model seems to work better at high fields; to exploit both benefits, a combination of the two approaches is proposed in [76]. In [75], the most used Poole approach has been used in absence of reliable information about the spatial trap distribution.

Besides the microscopic models listed so far, a number of macroscopic approaches, aimed at formulating compact models suitable for inclusion into device simulation frameworks, have also been developed. These approaches complement the microscopic description, trying to "lump" the complex physics into few simple equations featuring a small number of parameters.

All the abovementioned theoretical and computational approaches can be tested on an increasingly higher quantity of experimental data for a variety of chalcogenide alloys, both in transient and steady-state conditions, for devices with different configurations, where the active layer of Ovonic material ranges from the micrometer to the nanometer scale. Since each transport theory includes several fitting parameters, only the interpretation of a large number of measurements of the electric properties in different conditions can validate a given model. In the following, we provide a more detailed description of some of the microscopic and macroscopic computational approaches just introduced, being forced by space reasons to focus on a selection of recent references in the field. To explore a wider scenery, the interested reader may avail herself of the references listed at the end of the chapter.

40.4 Microscopic Models

We describe here how the models of [64, 65] have evolved to include self-consistency between the local carrier concentration and electric potential. This continuum description of the transport process in amorphous chalcogenides follows a procedure commonly used in standard semiconductor theory when the Boltzmann equation holds, encoded in a hydrodynamic-like approach [77].

40.4.1 A Hydrodynamic Approach to Trap-Limited Transport

The model unknowns are the local carrier concentration and the charge and energy fluxes, which are calculated by a suitable integration over the energy region filled with trap states within the energy gap of the amorphous chalcogenide [67]; to this purpose, a nonequilibrium Fermi-like distribution function $f_F(E_F, T_e)$ is used, including a nonequilibrium Fermi energy E_F and a carrier temperature T_e. Due to the complexity of the mathematical problem at hand, a very accurate approximation of the Fermi distribution, which still makes analytical integrations possible, has been used [67]. The quantities of interest are assumed to depend on the coordinate parallel to the current flow (here the z coordinate).

As for the trap-energy distribution, an energy range ΔE_T around the equilibrium Fermi energy at mid-gap is considered, which can eventually span the entire band gap $\Delta E_G = E_C - E_V$ (E_C and E_V being the energies of the conduction and valence band edges, respectively). The energy range ΔE_T is an input parameter of the model and must be fixed, for the material at hand, from experimental data and/or first-principle calculations on the amorphous structure, able to describe the defectiveness of the matrix [20, 78, 79]. A flat density of states $\gamma = n_T/\Delta E_T$ is assumed within ΔE_T, where n_T is the trap concentration; in [67], ΔE_T is equal to the band gap. Following [64], the average escape time of a carrier belonging to a trap located at z with energy E is given by

$$\tau_{\rightleftharpoons}(E, z) = \tau_0 \exp\left[\frac{E_C - E \pm q\,F(z)\,\Delta z/2}{k\,T}\right]. \qquad (40.4)$$

In (40.4), τ_0 is a characteristic time constant, q, k, and T are the absolute value of the carrier charge, the Boltzmann constant and the temperature of the amorphous matrix, respectively. In turn, F is the electric field and Δz is the average distance between two traps. The escape times in the two directions of motion, indicated by the arrows at the l.h.s. of (40.4), are different because of the presence of the field.

In a transport phenomenon dominated by hopping, the escape process is (by orders of magnitude) the slowest process in the conduction chain; thus, the carrier velocity during a

transition can be approximated by the ratio between Δz and the escape time $\tau_{\rightleftharpoons}(E, z)$ of (40.4):

$$v_{\rightleftharpoons}(E, z) = \frac{\Delta z}{\tau_{\rightleftharpoons}(E, z)} = \frac{\Delta z}{\tau_0} \exp\left[-\frac{E_C - E \pm q F(z)\,\Delta z/2}{k T}\right]. \tag{40.5}$$

The moments of the distribution function that are included in the model are:

(i) Carrier concentration (zero-order moment)

$$n(z) = \int_{\Delta E_T} \gamma f_F(E, z)\, \mathrm{d}E\,, \tag{40.6}$$

(ii) Average carrier velocity (first-order moment)

$$\langle v_{\rightleftharpoons}(z)\rangle = \frac{1}{n(z)} \int_{\Delta E_T} \gamma f_F(E, z)\, v_{\rightleftharpoons}(E, z)\, \mathrm{d}E\,, \tag{40.7}$$

(iii) Average carrier energy (second-order moment)

$$\langle E(z)\rangle = \frac{1}{n(z)} \int_{\Delta E_T} \gamma f_F(E, z)\, (E - E_V)\, \mathrm{d}E\,, \tag{40.8}$$

(iv) Average energy flux (third-order moment)

$$\langle P_{\rightleftharpoons}(z)\rangle = \frac{1}{n(z)} \int_{\Delta E_T} \gamma f_F(E, z)\, (E - E_V)\, v_{\rightleftharpoons}(E, z)\, \mathrm{d}E\,. \tag{40.9}$$

The two even-order moments depend on two unknowns, the nonequilibrium Fermi energy $E_F(z)$ and the carrier temperature $T_e(z)$. The odd-order moments contain also a third unknown, the electric field $F(z)$, through the carrier velocity, and can be combined together to yield the transport equations. In this way, a set of three differential equations can be written, to be solved for the triplet $F(z)$, $n(z)$, and $\langle E(z)\rangle$; the differential equations read [67]:

1. *Poisson equation*

$$\frac{\mathrm{d}F(z)}{\mathrm{d}z} = -\frac{q}{\varepsilon}\,[n(z) - n_{eq}]\,, \tag{40.10}$$

where ε is the permittivity of the material and n_{eq} the equilibrium carrier concentration. Under equilibrium conditions, the system is neutral for all z.

2. *Carrier flux equation*

$$\frac{J}{q} = -n(z)\,[\langle v_{\rightarrow}(z)\rangle - \langle v_{\leftarrow}(z)\rangle] + \frac{\Delta z}{2}\frac{\mathrm{d}}{\mathrm{d}z}\left\{n(z)\,[\langle v_{\rightarrow}(z)\rangle + \langle v_{\leftarrow}(z)\rangle]\right\} \tag{40.11}$$

In a current-driven situation, appropriate for studying the typical S-shaped $I(V)$ characteristics of Ovonic materials, the l.h.s. of (40.11) is known a priori; in turn, the r.h.s. consists of two terms: the former stems from drift conduction, and the latter represents the diffusive contribution to the current, being related to the nonuniformity of the carrier concentration and velocity.

3. *Energy balance equation*

$$\frac{\mathrm{d}}{\mathrm{d}z}\left\{n(z)\,[\langle P_{\rightarrow}(z)\rangle - \langle P_{\leftarrow}(z)\rangle]\right\} - \frac{\Delta z}{2}\frac{\mathrm{d}^2}{\mathrm{d}z^2}\left\{n(z)\,[\langle P_{\rightarrow}(z)\rangle + \langle P_{\leftarrow}(z)\rangle]\right\} = J F(z) - \frac{n(z)\,[\langle E(z)\rangle - \langle E_{\circ}(z)\rangle]}{\tau_R}\,. \tag{40.12}$$

This equation is derived in the first-order approximation of the energy relaxation through a relaxation time constant τ_R and a "target energy" $\langle E_{\circ}(z)\rangle$, namely, the energy that the population $n(z)$ would have if it was at thermal equilibrium with the lattice at temperature T.

The analytical derivation of these equations is reported in [67] assuming that the trap-energy states fill the band gap. Some relevant results obtained from the theory outlined above, using the parameters of GST–225, are shown in Figs. 40.9 (black curve), 40.10, and 40.11 (dotted line). Figure 40.9 displays the $I(V)$ characteristics obtained by a numerical solution of (40.10, 40.11, 40.12). All standard features of the conduction in Ovonic materials, i.e., an Ohmic region at the lowest current, followed by an exponential regime, are reproduced. When the electric field reaches a threshold value, a voltage snapback occurs. In the subthreshold region, the profiles of the electric field and carrier temperature are essentially uniform, consistent with the fact that very small heating effects are detected (see Fig. 40.10). As a consequence, the carrier concentration is constant; any increase in the input current leads simply to a spatially uniform growth of the electric field.

When the threshold condition is approached, the spatial uniformity of the three profiles is lost in a region close to the injecting contact (here referred to as "off" region), where the quantities of interest vary appreciably. What happens in this region determines the switching effect: the intense electric field transfers to the carriers a large amount of energy, which is only partially relaxed to the lattice by the energy-dissipative mechanisms. As a consequence, carriers are heated up while they move from the injecting to the collecting contact. As their average energy (thus temperature) increases, carriers move faster, and, to keep the current equal to the prescribed value, the carrier concentration $n(z)$ decreases. Furthermore, hotter carriers can overcome energy

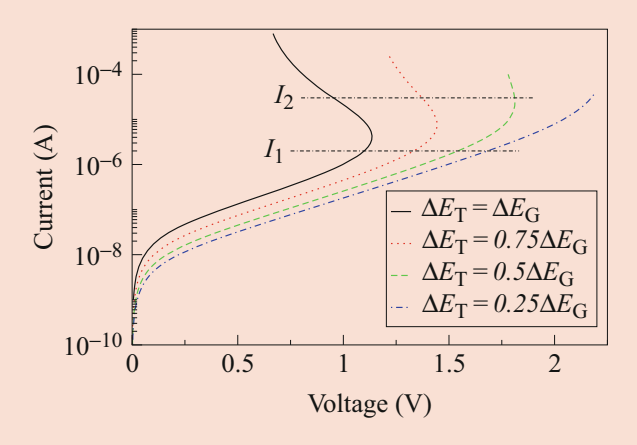

Fig. 40.9 $I(V)$ characteristics of a 40-nm-long device with a 1000 nm^2 cross-sectional area, for different values of ΔE_T ranging from ΔE_G down to 0.25 ΔE_G, with $\Delta E_G = 0.68$ eV. (After [68]). The parameters used in the numerical calculations are $\Delta z = 7$ nm, $\tau_0 = 1.2 \cdot 10^{-14}$ s, $\tau_R = 7.8 \cdot 10^{-14}$ s, $n_T = 6.8 \cdot 10^{19}$ cm^{-3}, and $T_0 = 300$ K. The *two horizontal lines* indicate the currents $I_1 = 2 \cdot 10^{-6}$ A and $I_2 = 3 \cdot 10^{-5}$ A, for which the profiles of $F(z)$, $T_e(z)$, and $n(z)$ are shown in Fig. 40.11

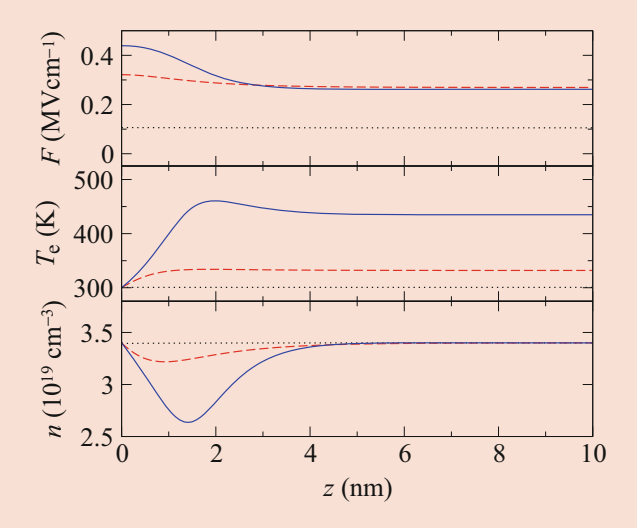

Fig. 40.10 Profiles of $F(z)$ (*top panel*), $T_e(z)$ (*middle panel*), and $n(z)$ (*bottom panel*) in the region of the device from 0 to 10 nm for the black curve of Fig. 40.9 evaluated at three selected currents: $1 \cdot 10^{-7}$ A (*dotted lines*), $2 \cdot 10^{-6}$ A (*dashed lines*), and $1 \cdot 10^{-5}$ A (*solid lines*). (After [68])

barriers more easily, and a lower field is required to sustain the current. In turn, lower fields transfer less energy so that, for a sufficiently high carrier temperature, the energy relaxation balances again the energy gain from the field. When this regime is attained, the spatial uniformity of the field, of carrier temperature and carrier concentration, is restored. This "on" region is much longer than the "off" region, close to the injecting contact, where carriers are heated up. The value of the field in the "on" region is thus assumed as representative of the whole device; this assumption is justified when the total device length is larger than the "off" region. While the field close to the injecting contact always increases with the current, the field in the "on" region increases at a slower rate at bias conditions close to the subthreshold region and eventually decreases, giving origin to the threshold-switching effect. The onset of the steady-state situation described above is crucially dependent on the interplay between energy gain and energy relaxation at a microscopic level.

The above analysis is influenced by the value of the energy range ΔE_T of the trap levels. To test this effect, four $I(V)$ characteristics are shown in Fig. 40.9, obtained by progressively reducing ΔE_T at a fixed spatial concentration n_T of the traps. It clearly appears that, at decreasing ΔE_T, the conductivity in the subthreshold region decreases and the threshold voltage and current increase. While the suppression of the very deep states does not alter significantly the results (as the contribution of these states to transport is substantially negligible), the lower conductivities found for smaller energy ranges can be attributed to the suppression of the shallow states within the band gap. According to (40.4), (40.5), if the trap energies are farther away from the bottom of the conduction band, the escape time is longer and the carrier velocity lower.

To complete the transport picture provided by the theory, in Fig. 40.11 the profiles of the electric field $F(z)$, carrier temperature $T_e(z)$, and carrier concentration $n(z)$ are shown as functions of the position along the device for two currents around the threshold value. A reduction by a factor 2 of the range of the trap-energy levels (solid line vs dashed line in Fig. 40.9) moves the threshold point roughly from $I_1 = 2 \cdot 10^{-6}$ A to $I_2 = 3 \cdot 10^{-5}$ A.

The lower conductivities obtained from reduced energy ranges imply that a given current is sustained only if the energy barriers between traps are further reduced by the action of a higher electric field. Since the field is almost constant along the device, but for a narrow region close to the injecting contact, higher overall potential drops are found, as seen in Figs. 40.9 and 40.11. In the "off" region, the average energy of the carriers is increased by the prevalence of energy gain over relaxation. In the absence of shallow energy levels in the band gap, larger threshold currents and voltages occur: the carrier average energy necessary for the switching event is established only at higher fields and currents, able to strongly increase the temperature of the carriers whose energies are close to the Fermi energy; this is visible in Fig. 40.11. In summary, the physical model and the numerical approach presented in this section are applicable to the study of electron transport in Ovonic materials when the current is dominated by hopping between localized states [64, 67]. Experimental data are well reproduced below and around the switching point.

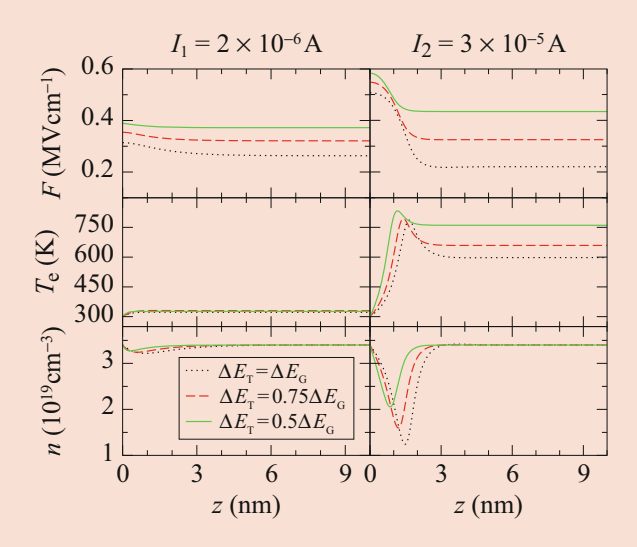

Fig. 40.11 Profiles of $F(z)$ (*top panels*), $T_e(z)$ (*middle panels*), and $n(z)$ (*bottom panels*), in the region of the device from 0 to 10 nm, when $\Delta E_T = \Delta E_G$ (*dotted line*), $\Delta E_T = 0.75 \cdot \Delta E_G$ (*dashed line*), and $\Delta E_T = 0.5 \cdot \Delta E_G$ (*solid line*), as in Fig. 40.9. For longer z's all curves keep their saturation values. (After [68])

40.4.2 Inclusion of Dispersive Band States

In the last years, many experiments have focused on the time-resolved electric response of nanometer scale layers of chalcogenide alloys inserted in high-performance electric setups; the aim was to assess the impact of the material choice on the read, write, and reset times of nonvolatile memories for advanced computation [80, 81]. The reduction of parasitic effects allows one to test the ultimate speed of threshold switching in different materials. On the modeling side, the first proposed time-dependent approach [82] is based on hopping transport and extends the analytical approach of [64] to transient conditions.

Then, a simulative approach merging the circuit equation with a set of differential equations of the hydrodynamic type, describing a trap-limited, time-dependent transport process for an Ovonic chalcogenide, has been applied to test how the transport time of the Ovonic material and the characteristic time of the external circuit interfere to determine the response to a time-variable voltage on different time scales [74, 83]. This approach was eventually extended to include, for the first time, a dispersion of the energy band states [75].

In the following we will describe this last development in detail. In order to focus on the effect of the band-state dispersion on transport, a very simple device structure is considered (as in the experiments used for validation purposes): a homogeneous chalcogenide layer with nanometer dimensions placed between two planar contacts; the latter are included into the physical model as boundary conditions for the model equations. As in previous models [14, 73, 74, 83], all relevant transport quantities depend upon the coordinate along the field direction (here denoted as z), while homogeneity is assumed in the perpendicular (x, y) plane; for simplicity, unipolar electron conduction is assumed.

Two types of electron energy states are considered. A set of localized states (referred to as "traps" in the following), all having the same energy E_T, are located in the middle of the gap (assumed to be the energy reference, $E_T = 0$), with g_T states per unit volume and carrier density $n_T(z, t)$; they have null mobility and do not contribute directly to the transport process. A parabolic band with minimum at energy Δ, effective mass m, and energy density of states per unit volume $g(E)$ describes the mobile extended states. The density of carriers in the band is $n_B(z, t)$; the band-state mobility μ is assumed to be independent of field and energy.

At equilibrium at temperature $T_\circ$, the total density of electrons $n_\circ$ is neutralized by an equal density of opposite fixed charges. Furthermore, the densities of carriers in the trap and mobile states are given by

$$n_{T_\circ} = \frac{g_T}{1 + \exp[(E_T - E_{F_\circ})/(k\,T_\circ)]}\,,$$
$$n_{B_\circ} = \int_\Delta^\infty \frac{g(E)\ \mathrm{d}E}{1 + \exp[(E - E_{F_\circ})/(k\,T_\circ)]}\,, \qquad (40.13)$$

where $E_{F_\circ}$ is the equilibrium Fermi energy and the second integral is evaluated over the band states. Densities $n_{B_\circ}$ and $n_{T_\circ}$ are homogeneous for a homogeneous distribution of traps, as supposed here.

Out of equilibrium, the occupation probability of an energy state is still taken as a Fermi distribution with an electron temperature T_e. Furthermore, the carrier energy necessary to reach the bottom of the conduction band is reduced by the amount gained from the electric field according to the Poole formula: $\Delta' = \Delta - \gamma\,|F|$. For a given electron temperature and Fermi energy E_F, the stationary position-dependent densities of carriers in the trap and mobile states are given by

$$\tilde{n}_T = \frac{g_T}{1 + \exp[(E_T - E_F)/(k\,T_e)]}\,,$$
$$\tilde{n}_B = \int_{\Delta'}^\infty \frac{g(E)\ \mathrm{d}E}{1 + \exp[(E - E_F)/(k\,T_e)]}\,. \qquad (40.14)$$

According to experimental evidence [84], we assume that the nonequilibrium Fermi energy E_F is well below the band edge, so that $E - E_F \gg k\,T_e$ and $\tilde{n}_B$ in (40.14) can be written as

$$\tilde{n}_B = \exp[E_F/(k\,T_e)] \int_{\Delta'}^\infty g(E)\ \exp[-E/(k\,T_e)]\ \mathrm{d}E\,. \qquad (40.15)$$

Assuming for $g(E)$ the standard form of a parabolic band [85], after straightforward calculations, one gets

$$\tilde{n}_\mathrm{B} = g_\mathrm{B}(T_\mathrm{e})\, \exp[-(\Delta' - E_\mathrm{F})/(k\,T_\mathrm{e})]\,,$$
$$g_\mathrm{B}(T_\mathrm{e}) = \frac{M}{\sqrt{2}} \left(\frac{m\,k\,T_\mathrm{e}}{\pi\,\hbar^2}\right)^{3/2}. \tag{40.16}$$

Coefficient M accounts for the possible concurrence of many bands to the determination of the energy density of states. The Fermi energy is analytically obtained as a function of the electron temperature T_e by imposing the normalization constraint to the density of carriers n:

$$\tilde{n}_\mathrm{T} + \tilde{n}_\mathrm{B} = n\,. \tag{40.17}$$

Replacing (40.14) and (40.16) in (40.17), an algebraic equation is obtained to be solved for the unknown $E_\mathrm{F}(T_\mathrm{e})$, which is position-dependent in nonequilibrium conditions.

Following the approach of [74, 75], particle- and energy-continuity equations along with the Poisson equation are solved with given boundary/initial conditions. The particle-continuity equation reads

$$\frac{\partial n}{\partial t} = \frac{1}{q}\,\frac{\partial J}{\partial z}\,, \tag{40.18}$$

where $n = n_\mathrm{B} + n_\mathrm{T}$ and the electron-current density J includes the drift and diffusion contributions:

$$J = q\,n_\mathrm{B}\,\mu\,F + \mu\,\frac{\partial}{\partial z}\,(n_\mathrm{B}\,k\,T_\mathrm{e})\,. \tag{40.19}$$

In the above equation, a generalized Einstein relation $D = \mu\,k\,T_\mathrm{e}/q$ is assumed in terms of the carrier temperature T_e. Owing to the asymmetry of the contacts present in real structures, the boundary conditions considered in the calculations are asymmetric as well. At the boundary with the source contact ($z = 0$), n is maintained constant and equal to the equilibrium value at any time, i.e., the contact is assumed to constantly inject the electrons that are necessary to maintain electrical neutrality right inside the device:

$$n(0,t) = n_\circ\,, \qquad \frac{\partial n(0,t)}{\partial t} = 0\,, \qquad T_\mathrm{e}(0,t) = T_\circ\,. \tag{40.20}$$

Elsewhere in the device, the transport dynamics determines a position-dependent value $n(z,t)$ of the carrier concentration, and the Poisson equation is used to evaluate the electric field $F(z,t)$.

At the exit contact ($z = L$), the condition $\partial n(z,t)/\partial z|_{z=L} = 0$ at any time is assumed; the value of n, in turn, is provided by the solution of the transport-Poisson equations. While moving across the device, the carriers redistribute themselves between band and trap states so that, at each z, the following equation holds

$$\frac{\partial n_\mathrm{B}}{\partial t} = \frac{\partial n}{\partial t} - \frac{n_\mathrm{B} - \tilde{n}_\mathrm{B}}{\tau_\mathrm{n}}\,, \tag{40.21}$$

where τ_n is the band-concentration relaxation time. In a time-dependent situation, $\tilde{n}_\mathrm{B}$ is the "tendential" stationary value of the mobile carrier concentration after a time variation of the electric field, i.e., $\tilde{n}_\mathrm{B}$ is the steady-state electron band population, given by (40.16), corresponding to the instantaneous values of F and T_e.

The rate of change of the total energy density w is obtained from the energy provided by the field, the spatial variation of the energy flux, including the energy lost in recombination processes, and the carrier energy loss to the phonon bath, assuming a relaxation time approximation:

$$\frac{\partial w}{\partial t} = -J\,F - \frac{\partial}{\partial z}(w\,v_\mathrm{B}) - \frac{w - w_\circ}{\tau_\mathrm{w}}\,. \tag{40.22}$$

where v_B is the average velocity of the band electrons at z. Combining the above equations yields the energy-continuity equation [75]:

$$\frac{\partial}{\partial t}\,(k\,T_\mathrm{e}) = \frac{2}{3\,n_\mathrm{B}}\left[-J\,F + \frac{3}{2}\,\frac{J}{q}\,\frac{\partial}{\partial z}\,(k\,T_\mathrm{e}) - \frac{k\,T_\mathrm{e} - k\,T_\circ}{\tau_\mathrm{wB}\,[k\,T_\circ/(k\,T_\mathrm{e})]}\,n_\mathrm{B} - \frac{k\,T_\mathrm{e} - k\,T_\circ}{\tau_\mathrm{wT}}\,n_\mathrm{T} + \frac{n_\mathrm{B} - \tilde{n}_\mathrm{B}}{\tau_n}\left(\Delta' + \frac{3}{2}\,k\,T_\mathrm{e}\right)\right], \tag{40.23}$$

with w_B the energy of the bottom of the band. The energy relaxation to the lattice, consistently with the assumption of Fermi-like distributions of carriers in trap and band states, is described through the carrier temperature relaxation, with contributions from both trapped (relaxation time τ_wT) and mobile (relaxation time τ_wB) states. In (40.23), the temperature relaxation time for band electrons is multiplied by the factor $k\,T_\circ/(k\,T_\mathrm{e})$ to phenomenologically account for faster relaxation of more energetic electrons. The particle- and energy-continuity equations are coupled to the Poisson equation (40.10). Since $n(0,t) = n_\circ$, then $\partial F(0,t)/\partial z = 0$ at any time. Furthermore, an integral condition on the field is imposed in terms of the applied bias $V(t)$:

$$V(t) = -\int_0^L F(z,t)\,\mathrm{d}z\,. \tag{40.24}$$

In summary, Eqs. (40.21), (40.23), and (40.10), along with the particle-continuity equation and the initial/boundary conditions, describe the transport process. They are numerically solved for the unknowns n, n_B, F, and T_e; other quantities like, e.g., j, $\tilde{n}_\mathrm{B}$, and $\tilde{n}_\mathrm{T}$ are calculated from them.

The model has been solved here through the Euler method; in fact, the inclusion of the Poole effect contribution to

the band population and of the steady-state projection $\tilde{n}_B$ makes it much more complex to implement methods like exponential fitting for space integration or Gear-like methods for time integration.

Numerical results obtained with the above-described model are shown here for different chalcogenide materials, which have been experimentally studied in view of their relevance for technological applications, namely, GST–225 [65], AIST [81], and $Zn_{0.35}Te_{0.65}$ [86]. Above threshold, phase change can possibly take place in the considered experiments. Since the model does not include the phase-change effect, the simulated characteristics are interrupted at threshold. Figures 40.12, 40.13, and 40.14 show the current flowing across chalcogenide layers of different thicknesses as a function of the applied voltage. Different layer thicknesses have been considered for each material, namely, 10, 20, and 40 nm; in addition, a thickness of 80 nm has also been considered for AIST. The reported experimental results are from [65] for a 40 nm GST–225 layer, from [81] for an 80 nm AIST layer, and from [86] for a 10 nm $Zn_{0.35}Te_{0.65}$ layer. In all cases the computed $I(V)$ curves show very good agreement with the experiments; a common feature of the three chalcogenides considered here is the overlap of the current curves when data are reported as functions of the mean applied field V/L.

Thus, in the considered range of device thicknesses, the computational approach confirms (see Fig. 40.15) that the threshold voltage scales linearly with the device thickness (i.e., the average electric field at threshold is independent of the device thickness); this is consistent with the findings of [65,87,88]. The result is also consistent with the microscopic

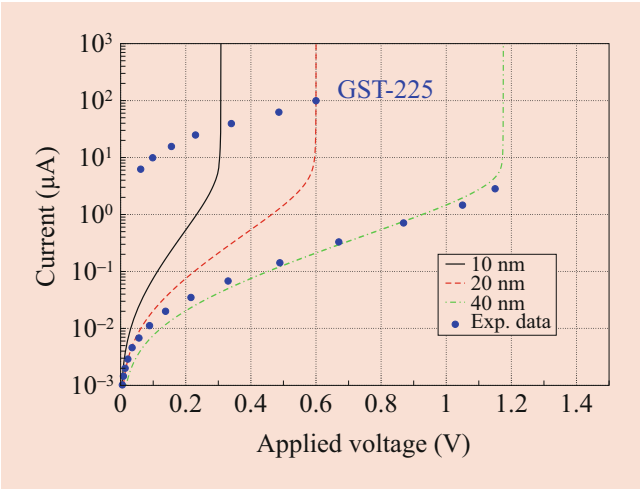

Fig. 40.12 Current flowing across GST–225 layers of different thicknesses as a function of the applied voltage. (After [75]). Experimental data from [65] refer to a 40 nm layer. The above-threshold measurements, which are outside the predictivity range of the present model, have been reported for the sake of completeness

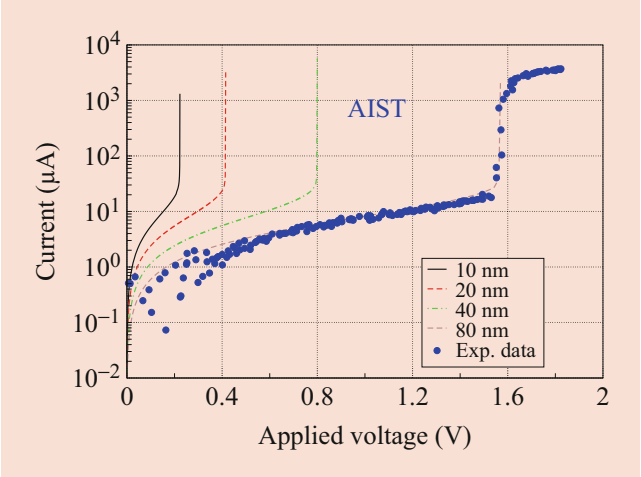

Fig. 40.13 Current flowing across AIST layers of different thicknesses as a function of the applied voltage. (After [75]). Experimental data from [81] refer to an 80 nm layer. The above-threshold measurements, which are outside the predictivity range of the present model, have been reported for the sake of completeness

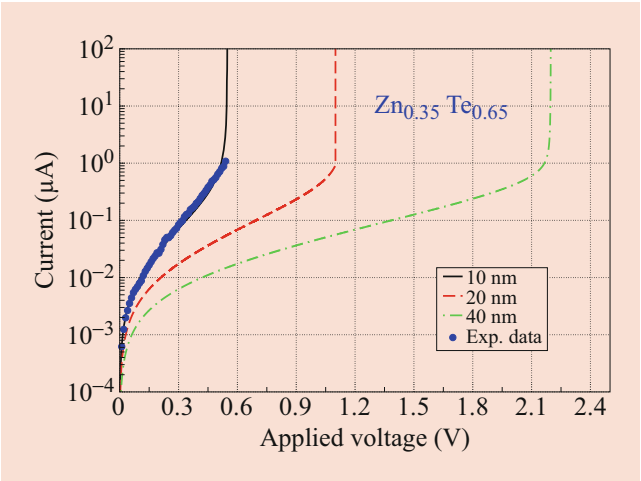

Fig. 40.14 Current flowing across $Zn_{0.35}Te_{0.65}$ layers of different thicknesses as a function of the applied voltage. (After [75]). Experimental data from [86] for a 10 nm layer are shown here up to the threshold voltage, due to the very high on/off current ratio

picture of the transport process at the origin of the switching effect provided by the present approach, already proposed in the literature from other theoretical models [65, 67, 74] and confirmed experimentally for chalcogenide layers larger than 10 nm [89]: in such cases, in fact, the device is large enough to allow carriers to gain the energy required to transfer from localized to extended states. Due to the Poole effect, this energy is actually lower than the bottom of the conduction band.

Experiments performed with chalcogenide layers below 10 nm [89] evidenced a constant voltage scaling with a minimum voltage value close to Δ/q; this has been justified

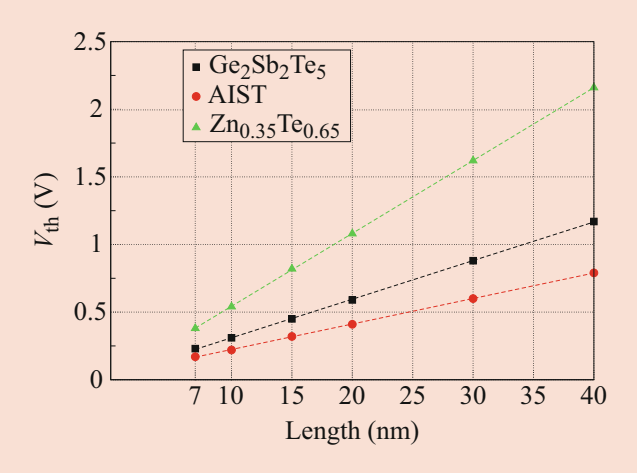

Fig. 40.15 Threshold voltage as a function of the chalcogenide layer thickness for the three materials considered in Sect. 40.4.2. (After [75])

as a consequence of the fact that in short samples electrons cannot relax energy to the phonon bath. Thus, when the energy gain from the external field is eventually enough to promote electrons to the mobile states, the switch takes place. This experimental evidence indicates that the present model is not applicable to devices whose thickness is smaller than a few nanometers.

40.4.3 Detrapping Due to Electron-Electron Interaction

As discussed above, carrier transport in chalcogenide materials typically includes two contributions, namely, that of band electrons (carrier motion in extended states) and hopping via traps (localized states). The sharpness of the trap-to-band transition mechanism is considered as the origin of the snapback event typical of these materials [90]. There may be different causes for the transition; among them is impact ionization which, however, is not frequent near threshold for the typical operating conditions of the devices; another cause is field emission which, by itself, is not able to provide the feedback mechanism necessary to produce the negative differential resistance; a third mechanism is the cooperative influence of the band electrons onto the trapped electrons, which is similar to impact ionization but involves also the lower-energy electrons of the band. The process has been investigated from first principles in [91] and has been included in a macroscopic model in [63], using a generation rate induced by the Coulomb interaction of trap electrons with band electrons. The first-principle analysis of the trap-to-trap transitions is shown here, based on the numerical solver for the time-dependent Schrödinger equation presented in [92].

The starting point is a flow of independent band electrons, having the same energy. The Coulomb interaction of such electrons with a trapped electron is described as the succession of electron-electron scattering events, each amenable to a two-particle analysis; given the number of band electrons at a given energy, the detrapping probability is found in terms of the band electron flow. It is assumed that the trapped electron is initially in the ground state E_0 of a potential well; in turn, the free-propagating band electrons belong initially to the energy state E_k (Fig. 40.16). A rectangular well is considered for simplicity; it is assumed that each band electron interacts with the trap electron only after the previous scattering event is over, so that one scattering event at the time is examined. It follows that the Hamiltonian is of the two-particle type:

$$\mathscr{H}(x_1, x_2) = \mathscr{H}_0(x_1) + \mathscr{H}_0(x_2) + \frac{q^2}{4\,\pi\,\varepsilon\,s}\,,$$
$$\mathscr{H}_0(x) = -\frac{\hbar^2}{2m^*}\,\frac{\partial^2}{\partial x^2} + V_T(x)\,, \qquad (40.25)$$

with V_T the potential energy of the well, m^* the effective mass of the material, and $s = |x_1 - x_2|$.

The trapped electron is initially in the ground state $\chi_0(x_2)$ of the single-particle Hamiltonian $\mathscr{H}_0$ with energy $-E_0$; the incoming electron is described by a Gaussian wave packet $w(x_1)$ with energy $E_k = \hbar^2 k^2/(2\,m^*)$: the center of the Gaussian is initially placed at a large distance from the well to make the interaction negligible at $t = 0$. The two-particle wave function of the system at $t = 0$ reads $\psi(x_1, x_2, 0) = w(x_1)\,\chi_0(x_2)$. The Schrödinger equation for ψ

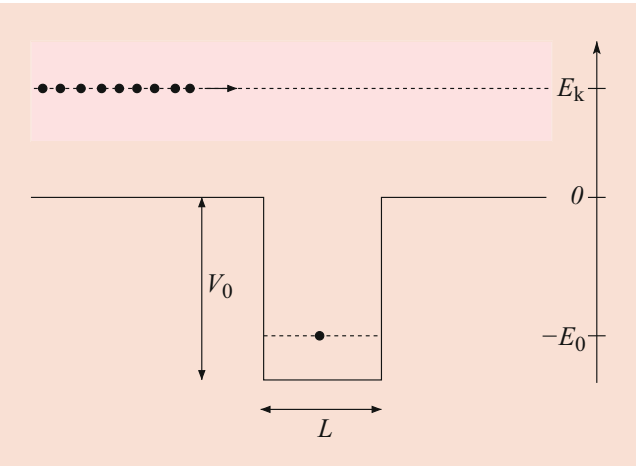

Fig. 40.16 Free-propagating band electrons at an initial energy E_k interact with an electron initially in the ground state E_0 of a rectangular well. (After [91]). The parameters used here are $V_0 = 350$ meV, $E_0 = 189$ meV, and $L = 1$ nm. The band electrons are described by a wave packet having a 5-nm standard deviation

$$i\hbar\frac{\partial}{\partial t}\psi(x_1, x_2, t) = \mathscr{H}(x_1, x_2)\,\psi(x_1, x_2, t)\,, \qquad (40.26)$$

yields a spatial wave function for each time step. To better understand the dynamics of the scattering event, the solution of (40.26) is used here to evaluate the single-particle probability density $\int |\psi(x_1, x_2, t)|^2\,\mathrm{d}x_1$ of the trapped electron before, during, and after the scattering (Fig. 40.17); one finds that, due to the electron-electron interaction, the band electron shares part of its energy with the trapped one, which initially belongs to the ground state χ_0 of the single-particle Hamiltonian (40.25).

It may happen that the trapped electron increases in energy and transits to non-bound states; as a consequence its spatial-density probability, which at $t = 0$ was peaked within the well, broadens up, and becomes non negligible also in regions far away from the well: the detrapping process is thus marked by the broadening of the trap-electron wave packet. Assume that at $t = t_\mathrm{f}$ the interaction is again negligible; then, the analysis of the wave functions provides information about the probability of detrapping: the latter occurs when both electrons are found in an extended state.

The duration of the electron-electron scattering is a few hundred fs; for this reason, one may neglect the relaxation to the ground level of the trapped electron; thus, when a scattering event takes place, the trapped electron is described by superposition of states of the form

$$\psi(x_1, x_2, t_\mathrm{f}) = \sum_{n=0}^{N} \alpha_n\,\varphi_n(x_1)\,\chi_n(x_2)\,, \qquad (40.27)$$

with $\chi_n(x_2)$ the n-th eigenstate of the single-particle Hamiltonian $\mathscr{H}_0$ and $\varphi_n(x_1)$ a freely propagating state associated to the incoming electron after scattering.

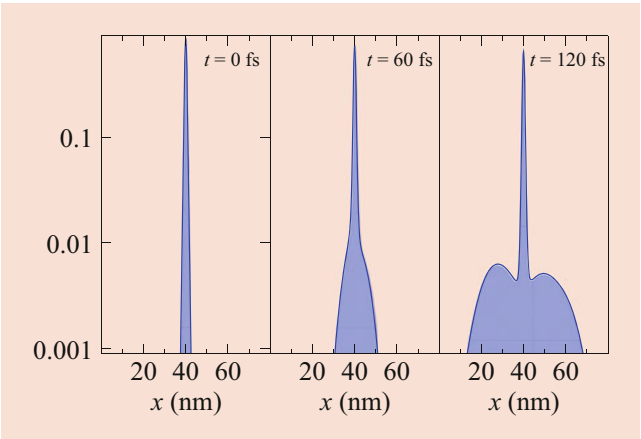

Fig. 40.17 Single-particle probability density of the trapped electron at different time steps. (After [91]). The probability density at $t = 0$ is $|\chi_0(x_2)|^2$, and its peak coincides with center of the potential well ($x_0 = 40\,\mathrm{nm}$). In this simulation, the initial kinetic energy of the incoming carrier is $E_\mathrm{k} = 50\,\mathrm{meV}$

Equation (40.26) has been solved here by the Crank-Nicholson scheme also used in [92, 93] to describe electron systems in semiconductor nanostructures. A one-dimensional, 80-nm-long region has been considered, discretized with a 640-point grid having a $\Delta x = 0.125\,\mathrm{nm}$ resolution [91]. The probability due to a single scattering event is evaluated at $t = t_\mathrm{f}$ from (40.27); for the problem in hand, and with reference to (40.25), χ_0 is the only eigenfunction of the single-particle Hamiltonian $\mathscr{H}_0$ corresponding to a bound state that describes a trapped electron. As a consequence, the square modulus of coefficient α_0 in (40.27) is the probability that, after a single scattering event with a band electron injected at energy E_k, the trapped electron is found in the ground state.

The detrapping probability due to successive interactions is also found from α_0; specifically, after the first two-particle collision is over, the electron described by a superposition of bound and extended states undergoes another Coulomb interaction with an incoming electron, again described by a Gaussian wave packet w. The scattering between w and the extended states of the other particle does not make the latter to relax; in turn, the interaction of w with state χ_0 has an $|\alpha_0|^2$ probability of leaving the latter state unchanged. Assuming independent scattering events, the probability that after n collision the trapped electron is still in the ground state is $|\alpha_0|^{2n}$; it follows that the probability that multiple electron-electron scatterings bring the initially trapped electron into an extended state is

$$P_\mathrm{D} = 1 - |\alpha_0|^{2n}\,. \qquad (40.28)$$

The dependence of P_D on the number n of injected electrons is shown in Fig. 40.18 for different values of the injection energy E_k; as expected, $|\alpha_0|$ decreases when E_k increases. When, instead, E_k is fixed, P_D increases with n and approaches unity within a few tens of interactions; this happens also when E_k is of the order of the thermal energy: such energies of the band electrons are realistic in amorphous GST–225 switching devices, near threshold or in the snapback regime, because the voltage drop across the device is relatively small. It follows from the considerations above that the increase of the device current that takes place in the snapback regime could be ascribed to the larger number of band electrons rather than to an increased velocity of the latter [90]. As the drift velocity of the band electrons is prescribed by their energy E_k, the current density is proportional to n; thus, the form of P_D in (40.28) indicates that the process of electron extraction from the traps has a sharp dependence on the current density. The exponential dependence of probability P_D on n and, therefore, on the current density, originates the function

$$r(I_\mathrm{n}) = 1 - \exp(-I_\mathrm{n}/I_\mathrm{A}) \qquad (40.29)$$

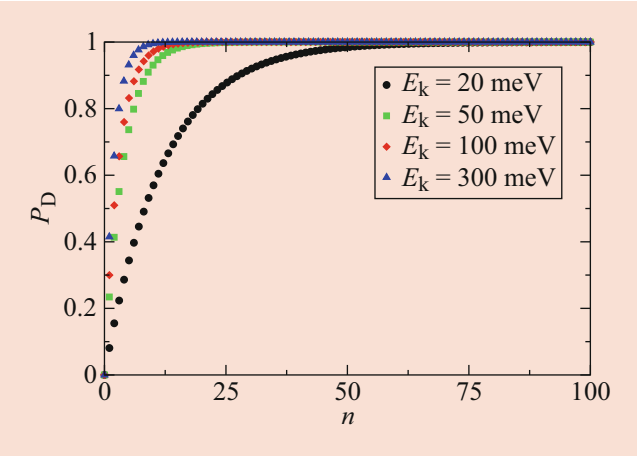

Fig. 40.18 Probability P_D of a detrapping event in terms of the number n of injected electrons; the curves correspond to the different injection energies shown in the inset. (After [91])

used in [63] as a macroscopic model describing the generation rate of the band electrons as a function of the band electron-current I_n, with I_A a constant. The sharpness of the dependence of r on I_n is essential for producing the negative differential resistance in the $I(V)$ curve of amorphous chalcogenides. It is therefore reasonable to conclude that, for the snap back to occur, the mechanism promoting an initially trapped electron to the conduction band must depend strongly on the current density: when this happens, the voltage increase across the device induced by the increasing current is overcome by a competitive effect, that is, the voltage decrease induced by the sudden increase in conductivity. The competitive effect produces the negative differential resistance observed in the amorphous GST–225 devices.

40.4.4 3D Simulation on a Random Network

An attempt to go beyond continuous-medium analytical models for the simulation of transport properties, in both OTS and PCM devices, has been carried out by Cappelli et al. [69, 70], by means of a random network approach that disposes of the one-dimensional limitation and allows one to couple the Fourier heat equation with the constitutive carrier-transport equations; in this way, both electric and thermal effects are accounted for self-consistently. Furthermore, this approach is suitable for describing local nonuniformities and few-carrier phenomena, both relevant in ultrascaled nanodevices.

In [69, 70] an amorphous chalcogenide layer, sandwiched between two conductive surfaces, is modeled as a three-dimensional network of N randomly placed nodes. At two opposite edges, two planar equipotential nodes (0 and $N+1$) play the role of contacts. The electrostatic potential φ_i and the carrier concentration n_i are associated to the i-th node; the average energy E_i is attributed to all members of the population sitting at node i. Following the concept of trap-limited conduction and considering for simplicity only the case of electrons, carrier motion comprises three stages: emission of a carrier from the i-th node to a traveling state with energy just above the conduction band mobility edge E_C, propagation toward the j-th node, and, finally, recapture by the j-th node. To represent the overall process the transition rate is assumed as

$$S_{ij} = \frac{f(r_{ij})}{\tau_0} \exp\left(-\frac{E_C - E_i}{k\,T}\right) \exp\left[-\frac{q\,(\varphi_i - \varphi_j)\,\eta}{r_{ij}\,k\,T}\right], \tag{40.30}$$

where τ_0 is the characteristic time of the transition process, T the lattice temperature, and r_{ij} the distance between nodes i and j. Term $f(r_{ij})$ in (40.30) is a function of the internode distance r_{ij}, describing propagation and recapture. For simplicity it is assumed $f(r_{ij}) = 0$ when r_{ij} is larger than a cutoff distance r_{cut}, and $f(r_{ij}) = 1$ otherwise. Furthermore, the two exponentials in (40.30) account for the thermally activated nature of the excitation process [64, 94]. The first one accounts for the energy barrier in the absence of field; the second one is a correction given by the average electric field $F = -(\varphi_j - \varphi_i)/r_{ij}$ between nodes i and j at a characteristic distance $\eta \le r_{cut}$; following [76], when $r_{ij} < 2\,\eta$ the correction is evaluated at $\eta = r_{ij}/2$.

The connections among nodes define a network of transition rates; given any pair of nodes (i, j), the current between them is $I_{ij} = -q\,(n_i\,S_{ij} - n_j\,S_{ji})$. To find the steady-state value of the node variables (φ_i, E_i, n_i), charge- and energy-flux balances are imposed at each node. As for the latter, three contributions are taken into account: the energy lost at the node site due to outgoing carriers, the energy gained from the incoming carriers (corrected by the effect of the field experienced during the transition), and the energy transferred to the lattice via phonon scattering with a relaxation time τ_R. Neglecting higher order terms, for a given current I the two balance conditions [69] yield

$$-\frac{I}{q}\,\delta_{0,i} + \sum_j n_i\,S_{ij} = \sum_j n_j\,S_{ji} - \frac{I}{q}\,\delta_{N+1,i}\,, \tag{40.31}$$

$$\sum_j n_j\,S_{ji}\,[E_j - q\,(\varphi_j - \varphi_i)] - \frac{I}{q}\,E_i\,\delta_{0,i} = E_i\left[\sum_j n_i\,S_{ij} - \frac{I}{q}\,\delta_{N+1,i}\right] + n_i\,\frac{E_i - E_i^{eq}}{\tau_R}, \tag{40.32}$$

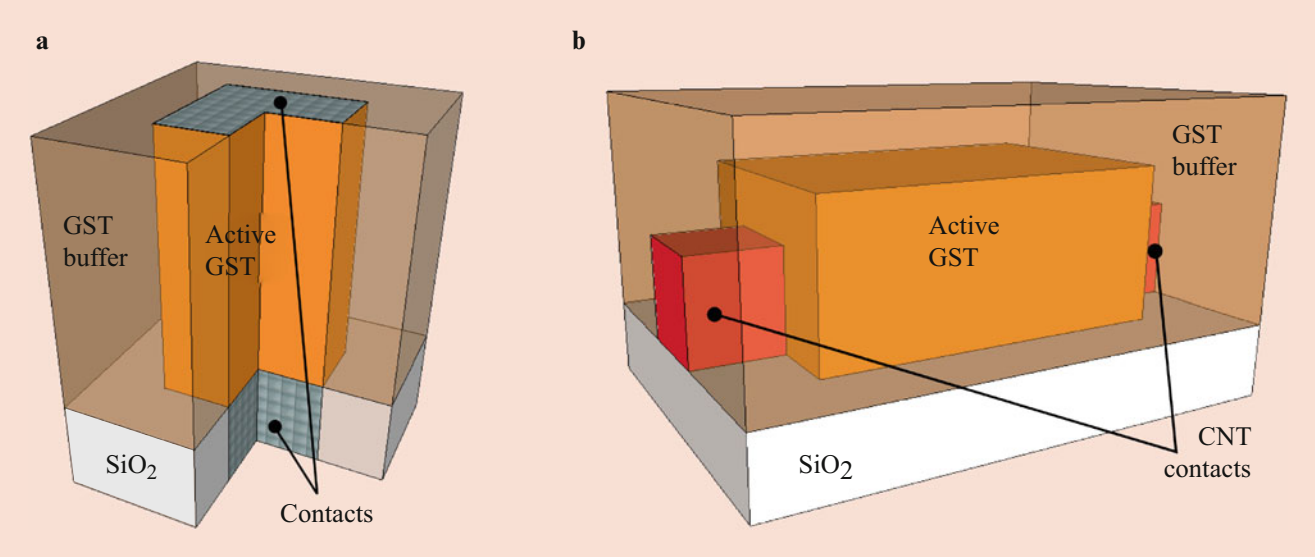

Fig. 40.19 (**a**) Schematics of the simulated devices. (After [70]): a traditional "mushroom-like" cell and (**b**) the novel device of [95] using carbon nanotubes as contacting leads

with $i = 0, 1, \ldots, N+1$. Since the device is current driven, the two equations for nodes 0 and $N + 1$ embed the fluxes from and to the external circuit through Kronecker's $\delta_{0,i}$ and $\delta_{N+1,i}$. The two sets of nonlinear equations (40.31) and (40.32) are solved along with the Poisson and the Fourier heat equations:

$$-\,\mathrm{div}(\varepsilon\,\mathrm{grad}\varphi) = Q_j\,, \qquad -\mathrm{div}(\kappa\,\mathrm{grad}T) = W_{ij}\,, \quad (40.33)$$

where $Q_j = -q\,(n_j - n_i^{\mathrm{eq}})$ at the scattering centers ($Q_j = 0$ otherwise) and $W_{ij} = q\,(n_i\,S_{ij} - n_j\,S_{ji})\,[E_i - E_j - q\,(\varphi_i - \varphi_j)]$ uniformly distributed along the line connecting the i and j centers ($W_{ij} = 0$ otherwise). In (40.33), κ is the thermal conductivity of the material.

The unknowns φ_i, E_i, n_i, and T_i are self-consistently evaluated at all nodes of the network, using a Newton-Raphson scheme coupled with a finite-element procedure. Given the network configuration, the algorithm leads to an $I(V)$ curve, with $V = \varphi_{N+1} - \varphi_0$.

Figure 40.19 provides a schematic view of the simulated devices: a traditional "mushroom-like" cell (left) [54] and a nanostructure with carbon nanotubes as contacting leads (right) [95]; the case of GST–225 has been considered. The SiO_2 bottom layer is kept at 300 K in both cases, and adiabatic boundary conditions are assumed at the sides [70]. The interplay among energy relaxation time of the carriers, local electric field, and local lattice temperature determines three different conditions, depending on the energy relaxation time constant τ_R and thermal conductivity κ (Fig. 40.20). When the energy gained from the electric field is efficiently dissipated to the lattice via phonon scattering, Joule heating and phase change prevail over other nonlinear effects. When, instead, the energy transfer to the lattice is low, the energy

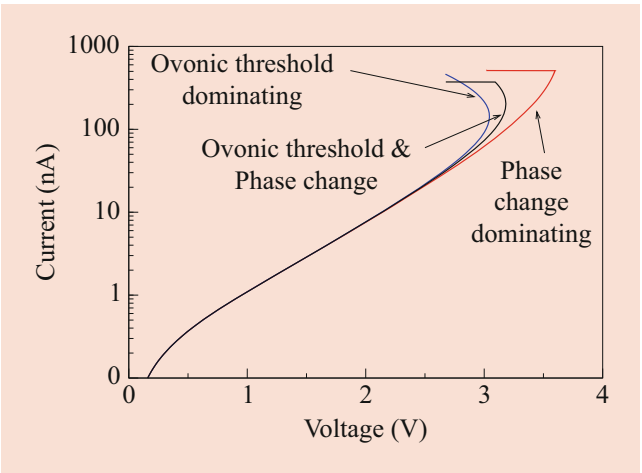

Fig. 40.20 Different threshold events evidenced in the $I(V)$ curve, depending on the values of thermal conductivity κ and energy relaxation time constant τ_R. (After [70])

gained from the electric field produces a hot-carrier distribution; under these conditions, the OTS event takes place. In intermediate cases, hot-carrier effects are limited, and the phase-change event may or may not be preceded by the OTS, depending on the transition temperature T_c.

The experimental device of [95] is analyzed in Fig. 40.21, showing the outcome of a microscopic simulation where preferential pathways for conduction are progressively created as the current is increased. In the figure, three frames of a ball-and-stick animation [70] from a single network configuration are shown, representing the mean energies E_i at the nodes and the normalized currents I_{ij}/I for the three points (a), (b) and, (c) of the $I(V)$ curve of Fig. 40.22. In the Ohmic

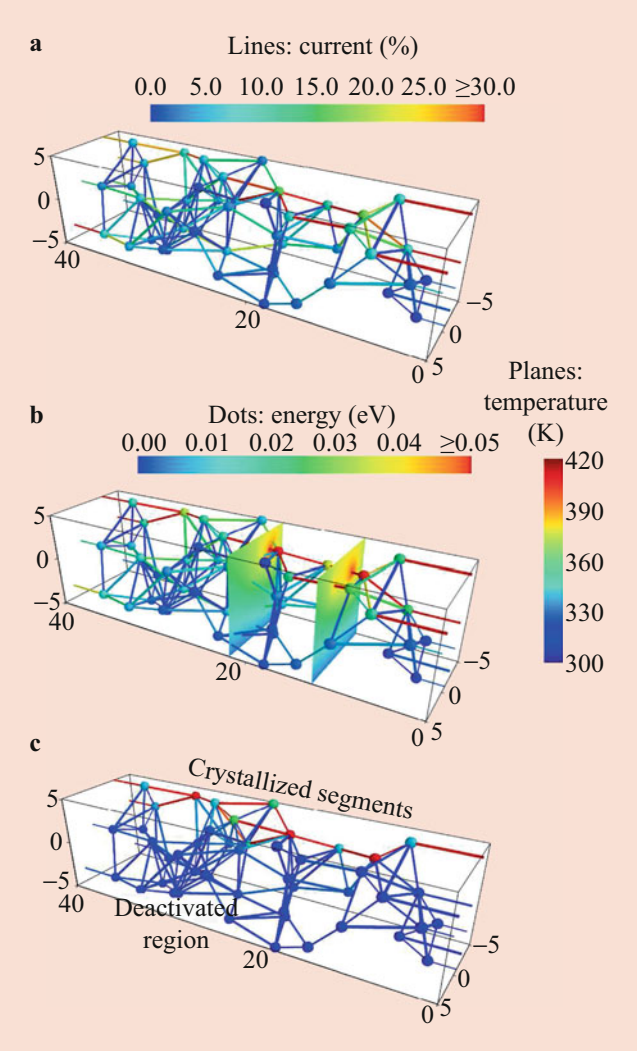

Fig. 40.21 Snapshots of the preferential path creation for conduction and first crystallization events when both (**a**) OTS) and (**b**) MTS are present. (After [70]). Panel (**c**) refers to a post-MTS condition. Note the high temperature along the preferential path

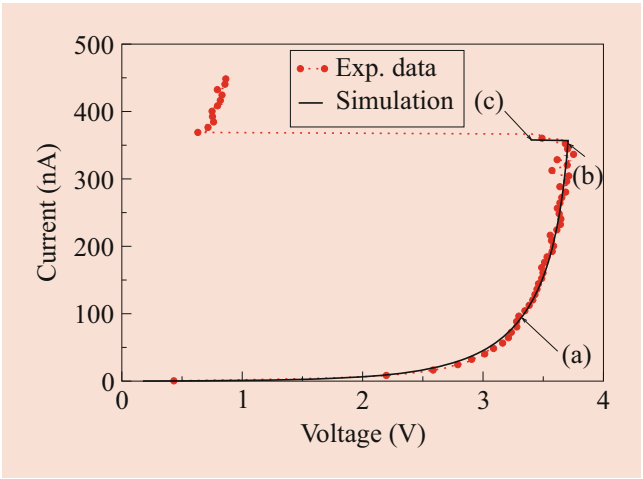

Fig. 40.22 $I(V)$ characteristic of a CNT test device ($10 \times 10 \times 40\,\text{nm}^3$) compared to experimental data. (After [70])

and exponential conduction regimes, the current is initially almost evenly distributed over several paths; heat transfer to the lattice is negligible or moderate. When the exponential conduction turns into the super-exponential regime, the small differences in the resistances among paths, due to local disorder, start to play a role: the current is progressively gathered along a single path, populated by slightly heated carriers. Due to current concentration, a significant Joule heating occurs. When OTS is present, as in Fig. 40.21, carrier heating near the OTS point enhances the creation of a preferential path. The outcome of the process is the positive feedback needed to trigger the switching event: more current implies more heating and faster transition rates and so on. Such a loop determines a steady-state condition where one or a few highly conductive paths connect the contacts (Fig. 40.22c) carrying most of the prescribed current; in turn, the lower resistance of the paths makes the voltage across the device to decrease. This generates a few negative differential-resistance regions featuring hot carriers with high mobility, while all other paths in the device become inactive; as a consequence, a large current can be sustained by a moderate electric field, until the crystallization of the preferential paths eventually takes place.

The concept of filamentation was introduced by Adler and coworkers [57] for large samples (see also p. 28). However, the size of the filaments predicted in this case does not appear compatible with nanoscale devices [96]: although the effect on the $I(V)$ characteristic is similar, the preferential paths identified by the model described here have a different origin than the filaments of Adler's model: in the present case, they are associated with nonequilibrium energy transport, not with a change in the quality or charge of the traps. The paths just indicate preferred sequences of connected nodes without any reference to the filament size.

The configuration-dependent nature of the model allows one to study the impact of intrinsic disorder on the threshold conditions. Figure 40.23 shows a set of one hundred $I(V)$ curves, differing only in the node positions; the statistical analysis of the corresponding threshold voltages V_{th} and currents I_{th} shows variations of up to ∼15% for V_{th} and ∼ 40% for I_{th}, with respect to the corresponding average values $\langle V_{\text{th}} \rangle$ and $\langle I_{\text{th}} \rangle$. Despite quantitative differences, the three known conduction regimes identified by the analytical models [65, 67]—Ohmic, exponential and super-exponential—are recovered in all curves, together with the onset of the voltage snapback. To validate the model against experimental data, a "theoretical" $I(V)$ curve has been constructed, for a given set of parameters, by averaging the potential drops of 30 simulations with random configurations. The standard

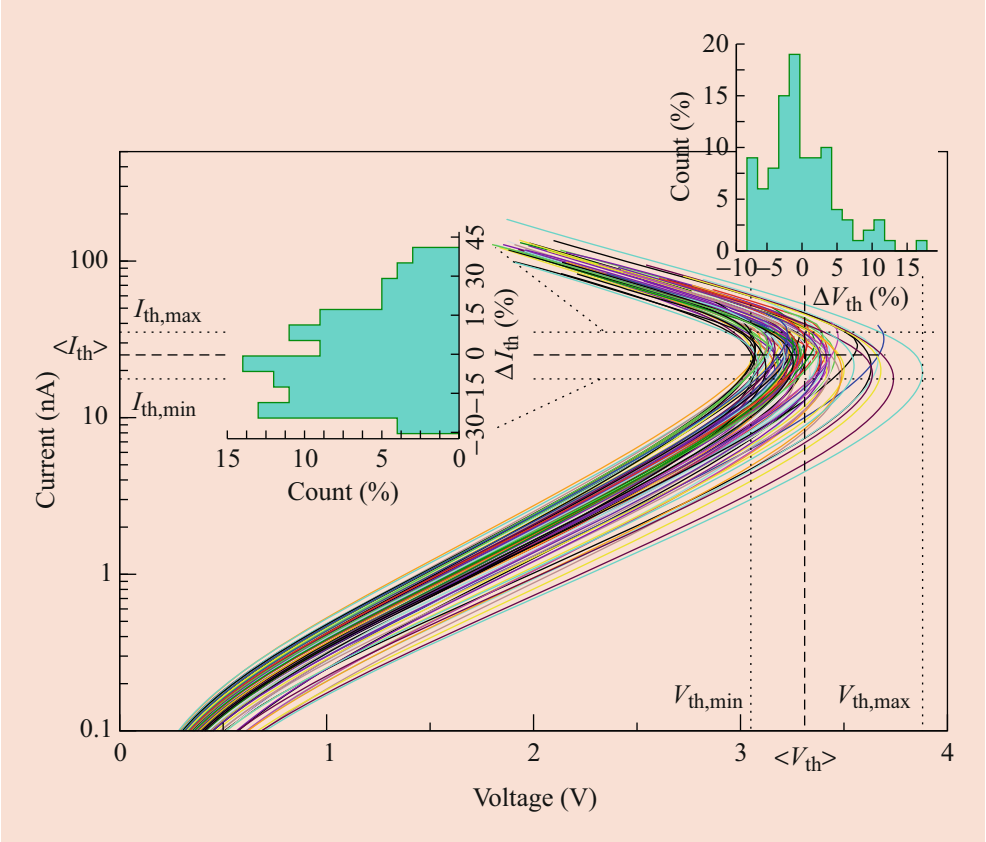

Fig. 40.23 Statistical fluctuations in the $I(V)$ curves for different spatial configurations of the network. (After [69]). The *dashed* and the *dotted lines* show the average and the minimum and maximum values for V_{th} and I_{th}, respectively. The two insets report the frequency analysis for the occurrence of the deviations from the average values $\langle V_{th}\rangle$ and $\langle I_{th}\rangle$. The analysis has been performed on a test device of $10 \times 10 \times 40\,\text{nm}^3$, using $\tau_0 = 10^2$ fs, $\tau_R = 10^3$ fs, $r_{cut} = 6$ nm, $\eta = 2$ nm, and a node concentration $1.2 \times 10^{19}\,\text{cm}^{-3}$

deviation of the potential drops provides an estimate of the expected variability. In Fig. 40.24, the calculated average curves and standard deviations best fitting three experimental $I(V)$ curves of memory devices are shown. In the subthreshold region, the agreement is good; the experimental points lie within the dispersion range, this confirming that the fitting parameters are reasonable. The onset of the threshold switching in the theoretical curve, i.e., the point where $\mathrm{d}V/\mathrm{d}I \approx 0$, corresponds quite accurately to the experimental threshold point. The abrupt voltage drop of the experimental curves above threshold eventually involves the crystallization of the system, which is not addressed by the model [97]. The sensitivity of the threshold condition to the particular location of the nodes is significantly reduced for longer cutoff distances, becoming of the order of ∼1% for V_{th} and of ∼13% for I_{th} in the limit of large r_{cut} (the latter is of the order of 12 nm).

40.4.5 Inter-Trap Transitions

Expression (40.30) of the inter-trap transition rate, or other expressions like (40.36) below, to be used in the balance equations (40.31 and 40.32), embed euristic parameters. An alternative expression, based on a first-principle derivation, is proposed in [98] and reads

$$S_{ij}^{0+} = \int_{E_m}^{\infty} F_{ij}\, n_i^{\text{ph}}\, (n_j^{\text{ph}} + 1)\, \mathrm{d}E\,,$$
$$S_{ji}^{0+} = \int_{E_m}^{\infty} F_{ji}\, n_j^{\text{ph}}\, (n_i^{\text{ph}} + 1)\, \mathrm{d}E\,. \qquad (40.34)$$

In (40.34), S_{ij}^{0+} is the probability per unit time that an electron transits from a filled trap belonging to site i to an empty trap belonging to site j (labels "0" and "+" indicate the charge state of the trap); in turn, n_i^{ph} is the phonon average occupation number at site i, $F_{ij} = F_{ji}$ a coefficient embedding the inter-trap transmission coefficient T_{ij} and E_m the bottom of the conduction band of the contact leads [98]. An analytical approximation of (40.34) is possible, that reads

$$S_{ij}^{0+} = \nu_{ij}^{0+} \left[T_{ij}\, n_i^{\text{ph}}\, (n_j^{\text{ph}} + 1) \right]_{E_{\text{av}}},$$
$$S_{ji}^{0+} = \nu_{ji}^{0+} \left[T_{ji}\, n_j^{\text{ph}}\, (n_i^{\text{ph}} + 1) \right]_{E_{\text{av}}}, \qquad (40.35)$$

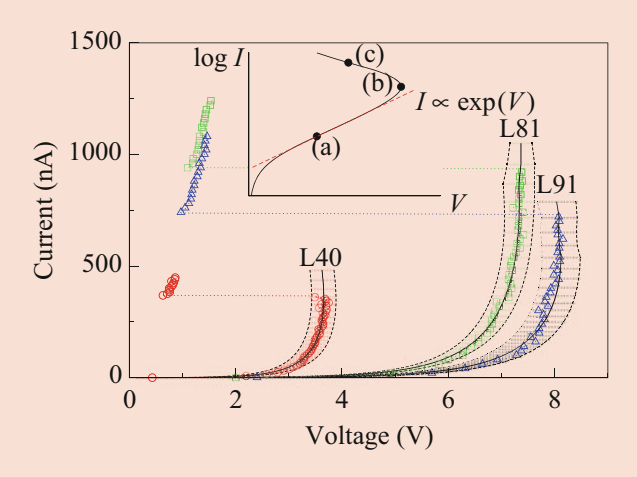

Fig. 40.24 Experimental $I(V)$ characteristics of three different CNT-GST–225 devices. (After [96]), whose estimated lengths are [69] 40 nm (*red circles*), 81 nm (*green squares*), and 91 nm (*blue triangles*). The *black solid lines* and the *dashed sides* show, up to the threshold region, the simulated average characteristics and the standard deviations obtained running a set of 30 simulations in each case. The *inset* shows a typical $I(V)$ characteristic in a semilog scale; the *dashed line* identifies the exponential regime. Points (**a**), (**b**), and (**c**) used in the microscopic analysis of Fig. 40.21 are also highlighted [70]

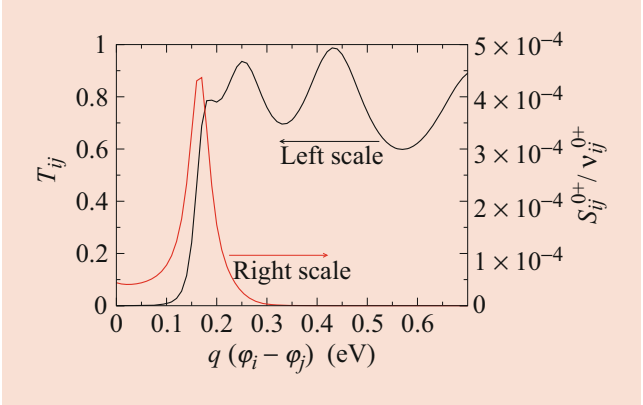

Fig. 40.25 Transmission coefficient T_{ij} (*left scale*) and normalized probability per unit time $S_{ij}^{0+}/\nu_{ij}^{0+}$ (*right scale*), at $T_L = 300$ K, in terms of the difference $q\,(\varphi_i - \varphi_j)$ of the potential energy between two traps. (After [98]). The calculation has been carried out by considering a 4-nm-thick rectangular barrier, with $\varphi_j = 0$. The simulation parameters are such that, depending on the value of $q\,\varphi_i$, both the oscillatory and real-exponential behavior of T_{ij} occur

with $E_{av} = (E_{ni} + E_{nj})/2$. Symbols E_{ni}, E_{nj} indicate the nonequilibrium Fermi energies at sites i, j; these values are available in a TCAD simulation because they are extracted at each iteration of the solution scheme from the electric potential and carrier concentration of the site. In turn, $\nu_{ij}^{0+} = \nu_{ji}^{0+}$ is the attempt-to-escape frequency, which is expressible in terms of the material properties [98]. Using (40.35) one calculates the normalized probability per unit time $S_{ij}^{0+}/\nu_{ij}^{0+}$; the latter is shown in Fig. 40.25 (right scale) in terms of the energy difference $q\,(\varphi_i - \varphi_j)$ between two neighboring traps, for a 4-nm-thick barrier with $\varphi_j = 0$. The same figure also reports the transmission coefficient T_{ij} (left scale); the calibration of parameters was such as to obtain both the real-exponential and the oscillatory behavior of T_{ij}.

The ratio $S_{ij}^{0+}/\nu_{ij}^{0+}$ has a peak at the transition between the real-exponential and oscillatory behavior of T_{ij}; on the right of the peak, $S_{ij}^{0+}/\nu_{ij}^{0+}$ drops quickly due to the vanishing of $n_i^{ph} = 1/\{\exp[(E_N + q\,\varphi_i)/(k\,T)] - 1\}$ that prevails over the oscillatory behavior of T_{ij} (E_N is a constant energy that depends on the form of the trap). In turn, the form of $S_{ij}^{0+}/\nu_{ij}^{0+}$ on the left of the peak is due to the competition between the decreasing exponential within n_i^{ph} and the increasing exponential that characterizes T_{ij} when $q\,\varphi_i$ becomes small. To summarize, Eq. (40.34), supplemented with the expression of F_{ij}, provides a first-principle derivation of the coefficients; the latter is rendered in terms of the local potential φ and the properties of the traps. A closed-form simplification of (40.34) is given by (40.35).

It is interesting to compare the behavior of S_{ij}^{0+} given by this model with that of [99], that reads

$$S_{ij}^{0+} = \nu_0 \exp[-r_{ij}/r_0 - q\,(\varphi_i - \varphi_j + |\varphi_i - \varphi_j|)/(2\,k\,T)]\,, \tag{40.36}$$

with r_{ij} the distance between sites i and j and r_0 a normalization factor that depends on the energy barrier between the two sites; due to the form of the exponent, the electric potential in (40.36) plays a role only when $\varphi_i > \varphi_j$. The normalized probability per unit time calculated with (40.35) and (40.36) is shown in Fig. 40.26 for different thicknesses of the barrier and different values of the ratio r_{ij}/r_0; the curves differ substantially: in fact, in (40.36) the effect of the local potential disappears when $\varphi_j > \varphi_i$ (this is equivalent to setting the probability of a phonon emission that brings the electron into the destination site, equal to unity). Another difference is in the real-exponential dependence on r_{ij} used in (40.36); such a dependence is, in fact, applicable only in a specific range of the final energy of the absorption event. In contrast, (40.35) does not suffer from such limitations: it considers both the absorption and emission probabilities, and the transmission coefficient T_{ij} accounts for the propagation at constant energy in both the oscillatory and real-exponential cases.

40.4.6 Ab Initio Quantum Transport Models for Ultrascaled Chalcogenide Devices

The transport approaches discussed so far are based on balance equations that assume diffusive transport and include a number of tunable parameters not directly connected to

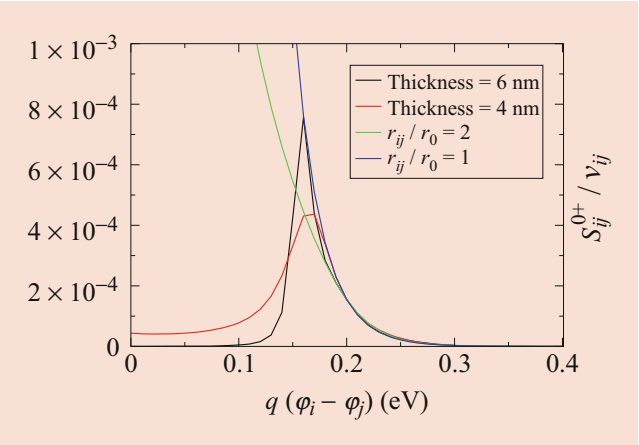

Fig. 40.26 Normalized probability per unit time, Eq. (40.35), calculated for two different thicknesses of a rectangular barrier (*black and red lines*). (After [98]). The same probability calculated following the theory of [99], reported here in Eq. (40.36), is shown by the *green and blue lines* for different values of the ratio r_{ij}/r_0

measurable quantities. Furthermore, as PCM devices scale down to the nanometer dimensions, new technological opportunities and modeling challenges open up [100]. In particular, for chalcogenide layers well below 10 nm, a small number of localized states are present in the atomic structure, which introduce an intrinsic granularity in the description of transport, and quantum effects become relevant when the de Broglie wavelength of the charge carrier becomes comparable with the layer length.

An attempt to deal with such effects relies on a first-principle quantum approach to the microscopic charge-transport process based, e.g., on the density functional theory (DFT), the nonequilibrium Green function (NEGF) method, or quantum hydrodynamics (QHD) [101–104]; for the basic concepts of the theoretical approach, the interested reader may refer, in this book, to Chaps. "▶ 42" by M. Fischetti et al., "▶ 43" by Ph. Dollfus and J. M. Sellier, "▶ 44" by S. Datta et al., and "▶ 45" by G. Klimeck and T. Boykin, and to [104] and references therein for more technical details about the application of the methods to the case of chalcogenides, the simulation packages used, and the input parameters of the calculations. Even though the atomistic approach cannot be applied to the simulation of complex devices due to the heavy computational load, it certainly provides the best tool for obtaining a unified understanding of the peculiar electrical properties of chalcogenides at the atomic scale, and clarifying what is the ultimate size PCM films can be scaled to, still retaining the crystalline-to-amorphous conductance ratio required by the technological applications.

The ab initio approaches, applicable to both amorphous and crystalline structures, in principle require, as input parameters, the lattice structure for the crystalline phase and the mass density for the amorphous one. As for the amorphous phase, the atomic structure is obtained from ab initio molecular dynamics (AIMD) starting from the liquid phase; then, the liquid is suitably quenched and, finally, relaxed to generate the amorphous structure. By means of a simulated annealing, an implementation of the AIMD procedure starting from the amorphous phase, at a temperature lower than the melting temperature and higher than the crystallization temperature, provides the recrystallised phase. Due to the small size of the samples, the procedure must be repeated to make different amorphous configurations available. The comparison between the computed and measured pair distribution functions provides a check about the reliability of the final result. Figure 40.27 shows some results of such a calculation for the case of GeTe [104]. In order to carry out the simulation of a transport process, the nanometer scale chalcogenide structure must be completed with the inclusion of two metal layers working as electrodes, to form a very simple device. In order to achieve a realistic structure at the metal-chalcogenide interfaces, all atoms are allowed to relax within a fixed region at the two interfaces. Open-source simulation packages are commonly used to implement the DFT-based, conjugate-gradient method and the AIMD; the results shown in [104] have been obtained with package SIESTA [105].

GeTe has been analyzed as case study [101] since binary PCM is found to maintain phase-change properties down to the smallest nanometer scale, probably due to the simple stoichiometry and small crystalline unit cell. Furthermore, TiN has been used to simulate metal contacts due to its wide experimental use, justified by the optimal thermal and mechanical properties at the interface with chalcogenide materials. The first calculations were performed for equilibrium electron transport [101]; the approach has then been extended to the nonzero bias case in the subthreshold regime under the assumption of ballistic transport [102]. The role of inelastic electron-phonon scattering in electron quantum transport has been assessed by using the Born approximation [103]. The results indicate that less than 4% of the energy carried by the electrons injected by the source contact is transferred to the lattice before carriers are collected at the drain contact. The main effect is a broadening of the calculated current density peaks (not shown in the figures), which has little influence on the quantitative shape of the $I(V)$ characteristic of the device.

In view of these results, the general quantum methodology to calculate electron transport quantities is outlined below for the ballistic case. The typical structure used for transport simulation at the atomic level is shown in Fig. 40.28. A combination of DFT, NEGF, and QHD approaches is applied starting from the lattice structure previously generated, which constitutes an input information (see the original literature [104] and the chapters of this book referred to at p. 1474 for a detailed description of the methodologies). The appli-

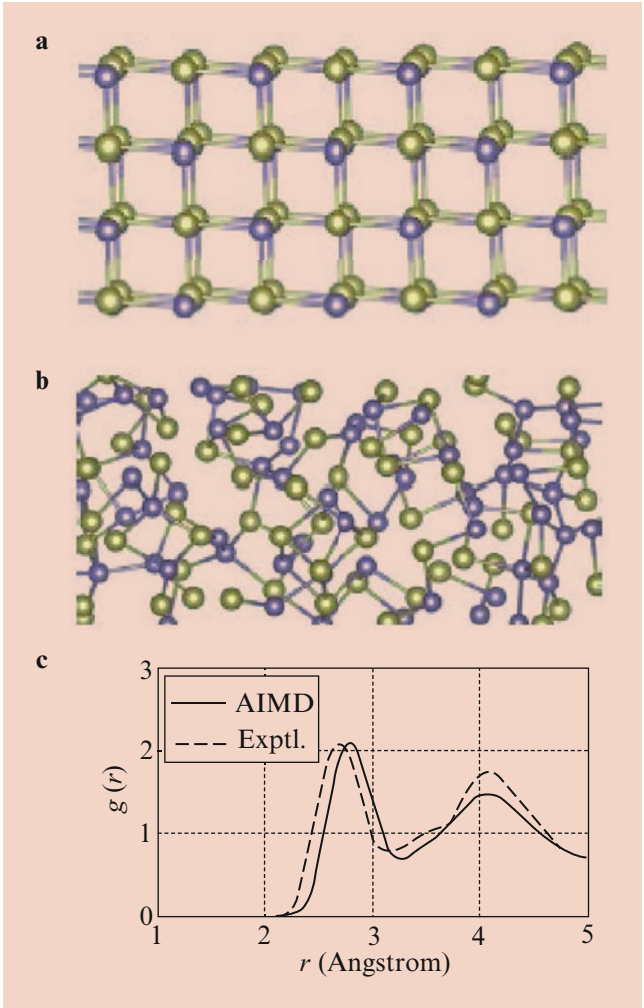

Fig. 40.27 Atomic structure of (**a**) crystalline and (**b**) amorphous GeTe; in (**c**) a comparison between computed and measured pair distribution function of amorphous GeTe is shown. (After [104])

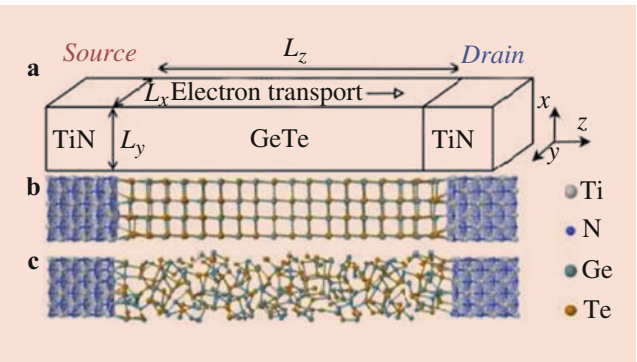

Fig. 40.28 Structure of the device used for simulations of transport at the atomic scale (*upper part*); crystalline (*middle part*) and amorphous (*lower part*) layers of GeTe chalcogenide within two layers of TiN acting as electrodes. (After [102]). Typical dimensions are $L_z = 6\,\text{nm}$, $L_x = L_y \approx 1.2\,\text{nm}$

cation of DFT to the device structure at zero bias provides the Hamiltonian matrix **H** and the overlap matrix **S**, which contain the ab initio equilibrium electronic structure. Then, an external bias V is applied, and the electron density is calculated in the pseudoatomic orbital (PAO) representation using an iterative self-consistent field solution:

$$n(\mathbf{r}) = \sum_{\mu\,\sigma} \mathbf{D}_{\mu\,\sigma}\,\phi_\mu(\mathbf{r})\,\phi^*_\sigma(\mathbf{r})\,, \tag{40.37}$$

where ϕ is the PAO basis function and **D** the density matrix:

$$\mathbf{D} = \frac{1}{2\,\pi\,\mathrm{i}} \int \mathbf{G}^<(E)\,\mathrm{d}E\,. \tag{40.38}$$

The lesser Green function $\mathbf{G}^<$ of (40.38) is computed as

$$\mathbf{G}^< = \mathbf{G}^+\,\mathbf{\Sigma}^<\,\left(\mathbf{G}^+\right)^\dagger\,, \tag{40.39}$$

where the retarded Green function $\mathbf{G}^+$ and the lesser self energy $\mathbf{\Sigma}^<$ are given by

$$\mathbf{G}^+ = \left(E\,\mathbf{S} - \mathbf{H} - \mathbf{H}_\mathrm{V} - \mathbf{\Sigma}^+_\mathrm{L} - \mathbf{\Sigma}^+_\mathrm{R}\right)^{-1}\,, \tag{40.40}$$

$$\mathbf{\Sigma}^< = -2\,\mathrm{i}\,\left(\mathrm{Im}\{\mathbf{\Sigma}^+_\mathrm{L}\}f_\mathrm{L} + \mathrm{Im}\{\mathbf{\Sigma}^+_\mathrm{R}\}f_\mathrm{R}\right)\,. \tag{40.41}$$

As mentioned above, **H** and **S** are the equilibrium Hamiltonian matrix and the overlap matrix; in turn, $\mathbf{H}_\mathrm{V}$ is the Hamiltonian term due to the external bias, E is the electron energy, $\mathbf{\Sigma}^+_{\mathrm{L,R}}$ is the retarded self-energy of the left/right electrodes (computed by means of the iterative surface Green-function algorithm [104]), and $f_{\mathrm{L/R}}$ the Fermi function of the left/right electrode:

$$f_{\mathrm{L/R}} = \left\{1 + \exp\left[(E - E_\mathrm{F} \pm q\,V/2)/(k\,T_\circ)\right]\right\}^{-1}\,. \tag{40.42}$$

In (40.42), E_F is the Fermi energy and $T_\circ$ the lattice temperature.

The self-consistent electric field solution inside the device for each external bias V is obtained by the iterative solution of (40.37) for the electron density and Poisson equation. Then, after the calculation of (a) the L/R electrode self-energy matrices $\mathbf{\Sigma}^+_{\mathrm{L,R}}$ [106], (b) the retarded Green function $\mathbf{G}^+$, and (c) the lesser Green function $\mathbf{G}^<$ [107, 108], the electron transport properties can be obtained; in particular, the analysis of the energy-resolved transmission coefficients $T(E)$ and current density $\mathbf{J}(\mathbf{r})$ evidences the microscopic origin of the peculiar electron transport properties below threshold for amorphous chalcogenides.

The energy-resolved transmission coefficient $T(E)$ provides a quantitative information about the probability that an electron with energy E propagates from the injecting contact to the drain contact: a low value of T means a high electron

backscattering in the device. In turn, the current density is evaluated as the sum of two terms: a local, conventional part $\mathbf{j}_c(\mathbf{r}, E)$ and a nonlocal term $\mathbf{j}_{nl}(\mathbf{r}, E)$, which guarantees the current-continuity condition in presence of a nonlocal potential in the DFT Hamiltonian [109]:

$$\mathbf{J}(\mathbf{r}) = \int \mathbf{j}(\mathbf{r}, E)\, \mathrm{d}E = \int \left[\, \mathbf{j}_c(\mathbf{r}, E) + \mathbf{j}_{nl}(\mathbf{r}, E) \,\right] \mathrm{d}E\,. \tag{40.43}$$

The average current density is defined from (40.43) as

$$J_{av} = \frac{1}{S_0} \int \mathbf{J}(\mathbf{r}) \cdot \mathrm{d}\mathbf{S}_0\,, \tag{40.44}$$

where $\mathbf{S}_0$ is the cross section perpendicular to the electron transport direction and S_0 is its area [104]. The theoretical predition for the case of GeTe, shown in Fig. 40.29, well compares with the experimental results. At voltages around $V = 0.2\,\mathrm{V}$ or lower, the ratio between the crystalline vs amorphous current densities is about 10^2–10^3 (see the C_1 and A_1 points in Fig. 40.29). This marked difference is well understood by considering the bias-dependent transmission coefficients, shown in Fig. 40.30. The amorphous case exhibits an empty band gap, while the crystalline case has metal-induced gap states near the Fermi energy, which bring about a large transmission through the device. A detailed microscopic analysis of the above quantities [104] evidences that a full explanation of the linear, exponential, and S-shaped $I(V)$ characteristic in the amorphous phase comes from a microscopic balance between (i) bias-dependent quantum dynamics of current swirls that set in at the Å scale due to the presence of defect-induced electron backscattering and localization and (ii) electron delocalization along the device produced by the external bias. Due to the large density of defects of the amorphous phase, the transmission effect is considerably reduced at low bias. As the applied voltage is increased, the field-induced progressive electron delocalization enhances the carrier drift along the electric force direction, and swirl localization is progressively destroyed. Figure 40.31 evidences the evolution of the current swirl localization pattern in the linear (A) and exponential (B) regions of the current-voltage characteristic of the a-GeTe layer through local 2D slices of the normalised, space-resolved scaled current density; the latter is defined as

$$\mathbf{D}(\mathbf{r}) = \frac{1}{J_{av}} \int \mathbf{j}(\mathbf{r}, E)\, \mathrm{d}E\,. \tag{40.45}$$

with J_{av} given by (40.44). The swirl patterns, well confined in the Å scale and separated from each other, are progressively destroyed when the external bias approaches the Ovonic switching field.

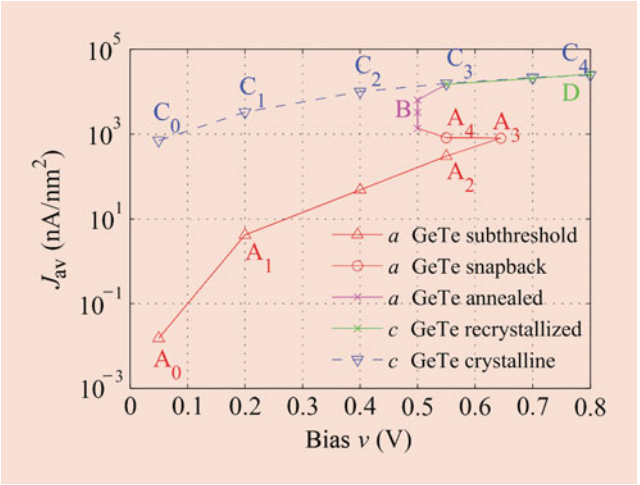

Fig. 40.29 $J_{av}(V)$ characteristic computed by means of an ab initio approach for a GeTe chalcogenide layer about 5.5-nm-long, with lateral dimensions about $1.2 \times 1.2\,\mathrm{nm}^2$, supplemented with TiN metallic contacts. (After [104])

40.5 Macroscopic Models

The preceding sections of this chapter dealt with simulation approaches based on microscopic models, which are usually applied to understand specific transport features of the large amorphous chalcogenide family. The effectiveness of the physical models is usually tested on simple structures. In order to move to the simulation of the more complex devices engineered for specific electronic applications, the theoretical framework must be simplified in order to reduce the computational burden to a reasonable extent and ease the interfacing with commercial device simulation platforms. An attempt to bridge microscopic and macroscopic approaches into a device simulation tool is described in [110], where a finite-element modeling of nucleation, growth, and amorphization processes in phase-change memory devices is carried out using a simplified 3D cylindrical geometry. A rate equation describing the evolution of the crystal density at each mesh point is coupled with the current-continuity and Fourier-heat equations; using the parameters of GST–225, the model performs electrothermal simulations describing consecutive set and reset cycles of a "mushroom" cell of the type presented in [54]. The model also allows for the simulation of cycle-to-cycle variations due to the stochastic nature of the nucleation process and of the interplay of crystallization, formation of percolation paths, and thermal runaway [111].

In a recent paper, where the same cylindrical geometry as in [110] is used (Fig. 40.32), the electric conductivity of GST-225 is written as the sum of two independent contributions $\sigma_{\mathbf{E}}$ and σ_T; it is assumed that the band mobile carriers are generated by two independent processes (a thermal and

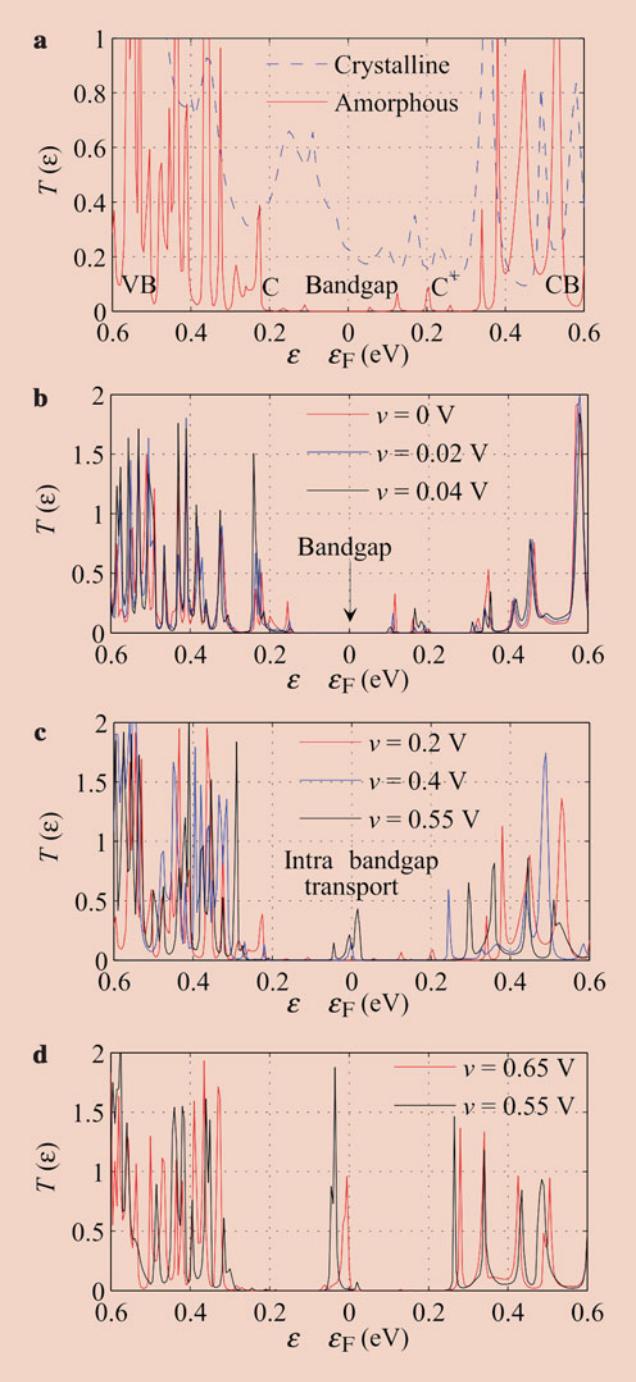

Fig. 40.30 Transmission coefficients as functions of the electron energy for the GeTe structure of Fig. 40.29. (After [104]). (**a**) a-GeTe and c-GeTe cases for $v = 0.2$ V (points A_1 and C_1 in Fig. 40.29); (**b**) and (**c**) a-GeTe case for small and moderate bias region (points A_0, A_1, A_2, A_3 in Fig. 40.29); (**d**) a-GeTe in the S-shaped part of the $J_{av}(V)$ curve (points A_3 and A_4 in Fig. 40.29)

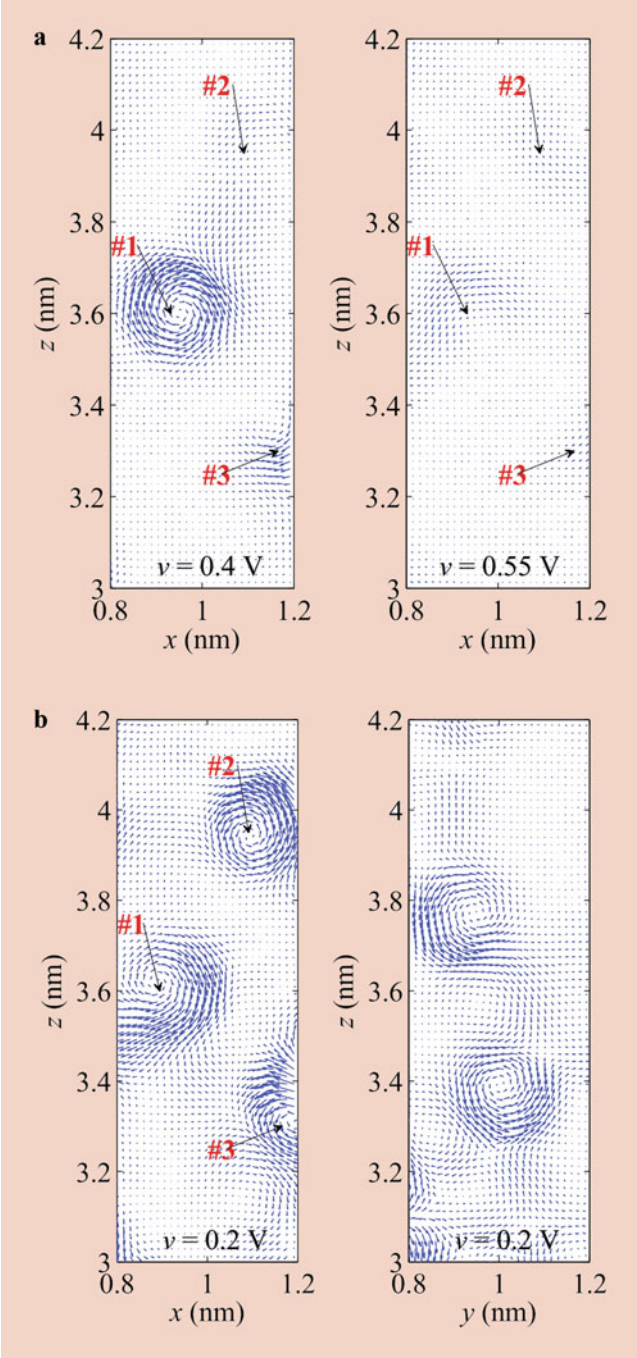

Fig. 40.31 2D plots of the normalised space-resolved scaled current density $\mathbf{D}(\mathbf{r})$ in the subthreshold linear (**a**) and exponential (**b**) regions of the $I(V)$ characteristic of the a-GeTe layer (see text). (After [104]). *Numbers* and *black arrows* in the figure identify the different detected swirls in the 2D mapping, in order to easily visualize their evolution at increasingly higher biases

an electric one), thus empirically decoupling the effect of the electric field $\mathbf{E}$ on the transport properties from that of temperature T. This ansatz avoids the more accurate, but computationally expensive, evaluation of the band-carrier concentration n in terms of integrals involving a nonequilibrium distribution at each iteration step and allows for an easier implementation of the numerical scheme simulating the transients. The relations yielding $\sigma_{\mathbf{E}} = q\,\mu\,n_{\mathbf{E}}$ and $\sigma_{\mathrm{T}} = q\,\mu\,n_{\mathrm{T}}$, with μ the carrier mobility and $n = n_{\mathbf{E}} + n_{\mathrm{T}}$ the

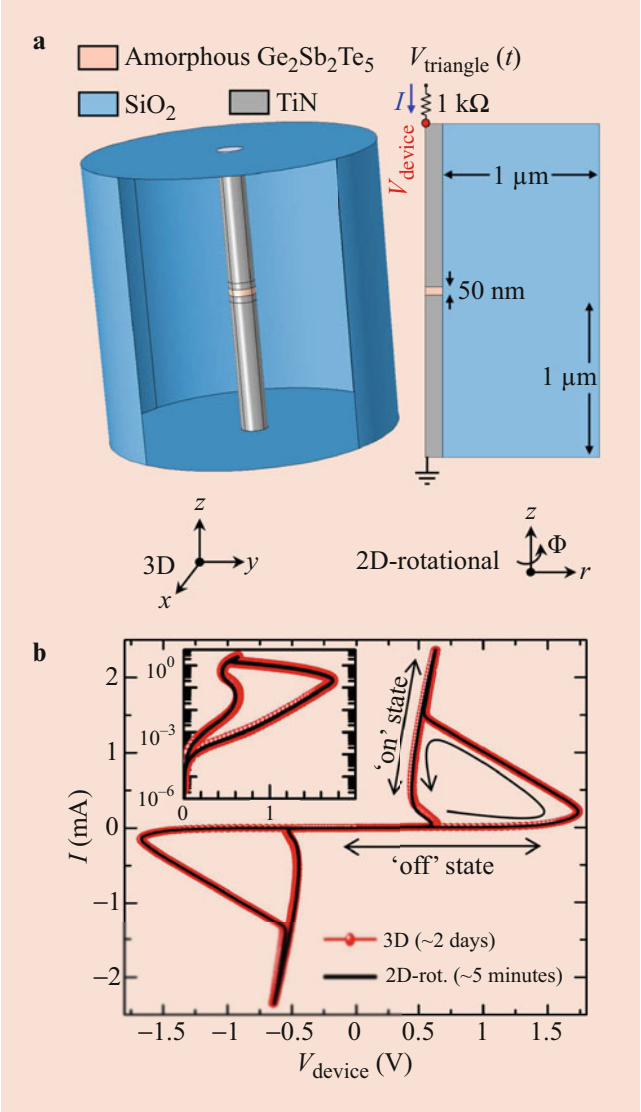

Fig. 40.32 (**a**) The cylindrical geometry simulated in [112] and (**b**) the corresponding $I(V)$ characteristic. The *inset* shows a portion of the same curve in a logarithmic scale; the *black and red curves* refer, respectively, to a 2D simulation exploiting the cylindrical symmetry and to a full-3D simulation. (Courtesy of J. Scoggin)

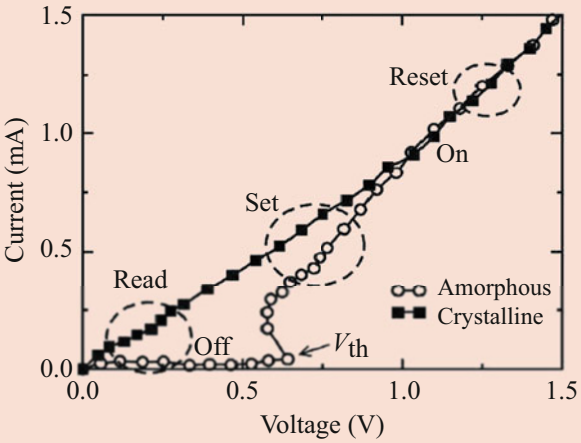

Fig. 40.33 Characteristic of a PCM in an $I(V)$ reference. (After [113]). The *linear curve* belongs to the crystalline phase, whereas the *S-shaped* one belongs to the amorphous phase. The device is current-driven; therefore, the actual characteristic is N-shaped and, consequently, single-valued (the N-shaped curve is sketched in Fig. 40.36). The threshold voltage is indicated with V_{th}

band-carrier concentrations produced by the two processes, are fitted on experiments [112].

Coming now closer to the industrial applications of amorphous semiconductors, in particular in the field of solid-state memories, this section provides a brief outline of how macroscopic simulation models are actually useful to design the device characteristics of the industrial prototypes. As mentioned in Sect. 40.1, the electric property of chalcogenides exploited to write, read, or erase a PCM device is that the $V(I)$ characteristic of the amorphous phase is N-shaped; an example is given in Fig. 40.33. In the following, the issue of modeling PCM oscillations under heating or quenching conditions, also in presence of crystallization, will be addressed after a preliminary discussion of the experimental problems one encounters when measuring the PCM characteristics in the amorphous phase; GST–225 will be considered as case study. Then, a stability analysis of the PCM oscillations will be carried out, and, finally, a study of the crystallization process will be discussed by means of a time-dependent analysis of the PCM temperature.

40.5.1 Macroscopic Modeling of PCM Oscillations

In the following analysis, we refer to the memory device illustrated in Fig. 40.34 (for further details about the design of PCM devices, see, e.g., [13,54] and, in this book, Chap. ▶ 30 by E. Piccinini and C. Jacoboni. Furthermore, we consider the "intrinsic" device, namely, the device obtained by ideally removing the series resistance due to the heater and contacts, along with the parasitic devices inevitably associated with the wiring and the measuring apparatus. A schematic cross section of the whole device is shown in the left part of Fig. 40.34; the rectangular region, limited above by the top electrode and below by the insulator or heater, visualizes the intrinsic device, which is initially amorphous; the white half sphere right above the heater is the volume that crystallizes first; finally, the red spherical shell is the maximum volume that crystallizes in the normal functioning regime of the PCM. The voltage-current characteristic of the intrinsic device will be indicated here and in the following with $V_S(I)$.

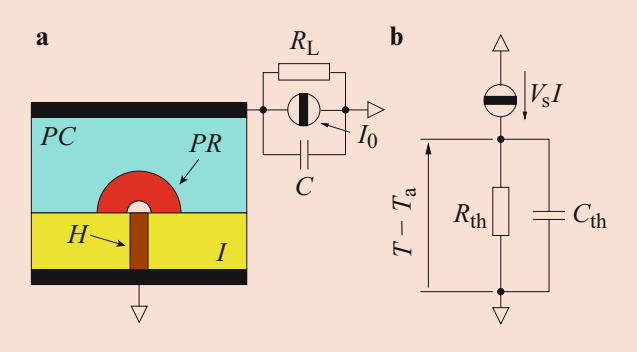

Fig. 40.34 (**a**) Schematic cross section of the device. (Adapted from [97]), connected to a lumped circuit representing the current drive and the parasitic devices; PC phase-change material, PR programmable region, I insulator, H heater. In the analysis carried out in Sect. 40.5, the material of the PC region is amorphous; initially, also the material of the red and white regions (PR) is such. The white region indicates the volume that crystallizes during the first, larger oscillation peak shown in Fig. 40.35. (**b**) thermal circuit for the PCM. (After [113]). A slightly different version of the figure is also in [114]

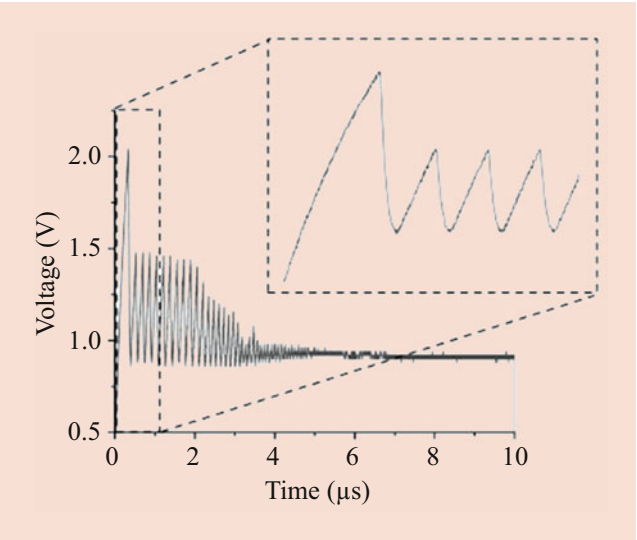

Fig. 40.35 Time evolution of the voltage V_S across a PCM in the amorphous phase during a dynamic measurement. (From Fig. 3 of [117], also in [114]). The oscillations are due to the instability produced by the NDR branch of the $V_S(I)$ characteristic. The *zoom* shows the amplitude of the first peaks, whose behavior is explained in the text

40.5.2 Measuring PCM Characteristics in the Amorphous Phase

Setting up a static measurement setup for $V_S(I)$ or other electric parameters of the amorphous PCM is notoriously complicated, because of the intrinsic instability due to the negative differential-resistance (NDR) branch. In fact, the amount of data available in the literature about the NDR branch of the characteristic is rather limited. A different approach tackles the problem using a dynamic setup, namely, it exploits the instability associated with the NDR branch of the PCM characteristic; this is done, e.g., in [115–117]. The arrangement is such that the voltage-current curve of the external load intersects that of the PCM in the NDR branch, with a suitably chosen slope that forces the circuit to oscillate. The analysis of the oscillatory regime shown in the following is based on the theory of [114].

One of the problems brought about by a dynamic measurement is the partial crystallization of the material produced by the heat injected into the device. When part of the volume crystallizes, the increase in the device conductance modifies, and possibly extinguishes, the oscillations. A typical pattern of the oscillatory condition is shown in Fig. 40.35 [117]: the first oscillation exhibits a large peak, followed by oscillations whose amplitude is smaller than that of the first peak and relatively stable; after a while the oscillation amplitude starts decaying. The decrease in amplitude from the first peak to the next ones is explained by observing that the concentration of the current lines flowing from the heater produces a sudden crystallization of a finite portion of material (the white half sphere right above the heater in Fig. 40.34a). The heater is in fact narrower than the amorphous region, and the temperature is the highest because the whole device is still amorphous. The sudden crystallization of the region in contact with the heater, which takes place during the first oscillation, leaves a smaller resistance for the next cycles. This event is followed by oscillations with a stable amplitude; in fact, although the temperature of the amorphous phase increases due to the injected heat, it is still $T < T_g$, with T_g the *glass temperature* (i.e., the temperature above which the amorphous-to-crystalline phase change occurs; it is $T_g < T_m$, with T_m the melting temperature). When the material temperature exceeds T_g, so that $T_g < T < T_m$, the oscillation amplitude starts to decay due to the decrease in the amorphous phase volume [82, 117] (for GST–225 it is $T_g = 550$ K and $T_m = 810$ K [113]). We conclude that the description of the oscillations must combine time-dependent circuit and thermal analyses with the modeling of crystallization; both of them can be carried out by means of the macroscopic model described in the next section.

Macroscopic Time-Dependent Modeling of PCM Dynamic Response

The description of the events that take place in the dynamic measurement described above must address a number of aspects, namely, *(a)* the analysis of a nonlinear circuit having an NDR branch whose properties depend on time, *(b)* a thermal analysis describing the dependence of the PCM temperature on time, *(c)* the time evolution of the crystallization of a part of the volume, and *(d)* the change in resistivity of the PCM due to crystallization and its effect on the shape of the voltage-current characteristic.

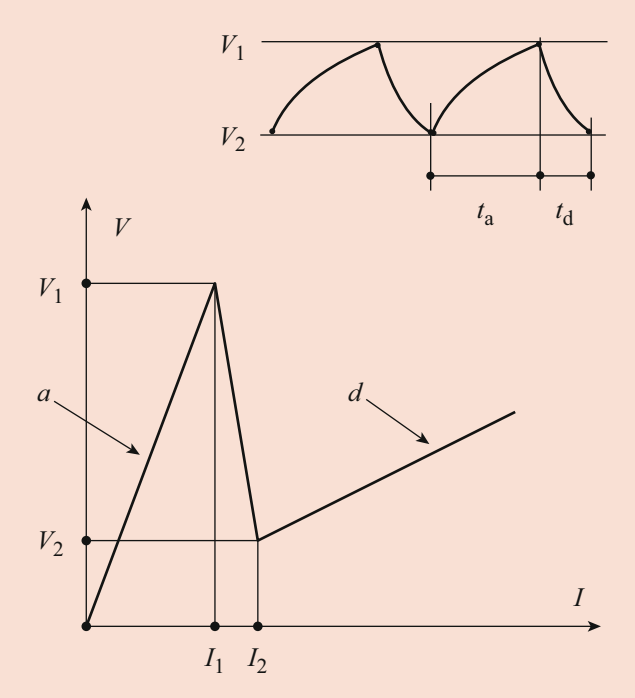

Fig. 40.36 The $V(I)$ characteristic approximated by a piecewise-linear curve (compare with Fig. 40.33). The *inset* shows the corresponding saw-like form of $V(t)$ that occurs when crystallization is absent. In the ascending part of the oscillation, corresponding to period t_a of the inset, I and V vary along the branch marked with a; in the descending part of the oscillation, they vary along the branch marked with d

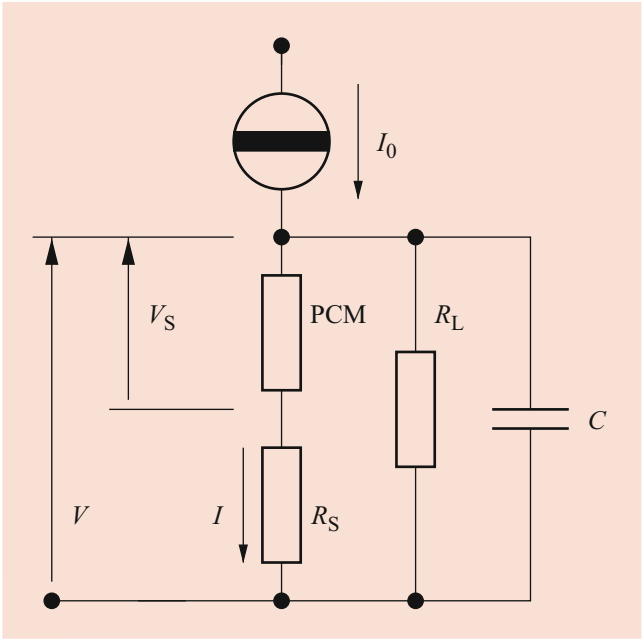

Fig. 40.37 Scheme of the circuit used for measuring the PCM parameters. Compare with Fig. 40.34a

As mentioned in Sect. 40.4.3, the origin of the N-type characteristic is traced back to a sharp increase in the trap-to-band transition rate, driven by the injected current I and starting at I_1 (Fig. 40.36). When the current reaches I_2, many of the initially trapped electrons have undergone the transition. The phenomenon, whose detailed analysis is given in [63], is equivalent to a filamentation that occurs in the energy domain instead of the space domain. Due to the larger mobility of the band electrons, it follows that, of the two positive-slope branches, the one crossing the origin has a larger slope than the other one. Also, for a given current density (equivalent to a given cross-sectional area in the case considered here), the collective electron-electron interaction that promotes the electrons from the traps to the band is such that the currents I_1 and I_2 enclosing the NDR branch do not depend on the volume of the amorphous phase [63].

The device of Fig. 40.34 is schematically described in Fig. 40.37 as the series of an intrinsic part, labeled PCM, embedding the N-shaped characteristic, and a constant series resistance R_S due to the heater and contacts. Prescribed parameters are the constant current I_0 and the load resistance R_L. They are chosen in such a way as to force an oscillatory regime in the circuit, which is sustained by the parasitic capacitance C due to the measurement setup. The quantity that is measured is the voltage $V(t)$ across the series made of the PCM and R_S. The circuit is described by the two coupled equations:

$$V = R_S\, I + V_S(I)\,, \qquad I = I_0 - \frac{V}{R_L} - C\,\frac{\mathrm{d}V}{\mathrm{d}t}\,. \tag{40.46}$$

The limit cycle in the I,V plane is determined essentially by the two points (I_1,V_1), (I_2,V_2), visible in Fig. 40.36, that enclose the NDR branch. Following [115,116], one estimates I_1 and I_2 by approximating the $V_S(I)$ curve with a piecewise-linear function; $V(I)$ becomes piecewise-linear as well, as better shown in Fig. 40.36.

As long as crystallization is absent, which happens when the amplitude of the oscillations is still stable as described earlier, the piecewise-linear approximation of $V_S(I)$ makes (40.46) easily integrable, to yield a saw-like oscillation as the one shown in the inset of Fig. 40.36; in fact, all parameters describing the coefficients of (40.46) are constant with respect to time, so that their extraction from the experiments is a relatively simple matter: in fact, defining $R_a = R_L \parallel (R_S + R_1)$ and $R_d = R_L \parallel (R_S + R_2)$ and using the symbols of Fig. 40.36, a straightforward calculation yields

$$t_a = R_a\, C\, \log\frac{V_2 - R_a\, I_0}{V_1 - R_a\, I_0}\,, \qquad t_d = R_d\, C\, \log\frac{V_1 - R_d\, I_0}{V_2 - R_d\, I_0} \tag{40.47}$$

(in general, the values of the circuit elements thus extracted are faulty due to noise or measurement errors; the calculation

must be improved by using the extracted elements as the initial guess of a fitting procedure).

In a realistic situation, instead, only some parameters are constant, specifically, R_S, C, I_1, and I_2, while V_1 and V_2 change with time because of the progressive crystallization of the material. Hence, they must be evaluated by consistently coupling their equations with other equations, produced by the thermal analysis, that are described in Sect. 40.5.3.

40.5.3 Thermal Analysis of the PCM

To find the time dependence of the PCM temperature, one solves the equivalent thermal circuit, shown in Fig. 40.34 (right) [113]. The latter is driven by the power $V_S\, I$ dissipated within the PCM, and is described by

$$\frac{\mathrm{d}T}{\mathrm{d}t} + \frac{T - T_a}{\tau_{th}} = \frac{V_S\, I}{C_{th}}\,, \tag{40.48}$$

where T_a is the ambient temperature and $\tau_{th} = R_{th}\, C_{th}$, with R_{th} and C_{th} the thermal resistance and capacitance, respectively. Typical values of the parameters of (40.48) are given below. It is worth remarking that, when a cell supplemented with an external heater is considered, the boundary conditions of (40.48) must account for the temperature of the boundary region where the heater contacts the cell; such a proviso is not necessary in a self-heating cell.

Crystallization often starts with the formation of small unstable clusters of the new phase (*nucleation process*, where "nucleus" indicates the minimum-size volume that crystallizes). Eventually some clusters reach a critical radius beyond which they are stable, so that they can grow rather than dissolve (*growth process*). As mentioned above, the dynamic model describing crystallization is that of [118]; letting g indicate the number of nuclei of the cluster, one must consider a balance equation for each index $g = 1, 2, \ldots, M$; such equations embed the corresponding condensation rates C_g and evaporation rates E_g, along with the generation rate r of the nuclei and a small number of fitting parameters. They form a set of nonlinear, coupled differential equations of the first order with respect to time, whose unknowns are the concentrations N_g of the g-clusters (i.e., clusters made of g nuclei). Once the maximum index $M = g_{max}$ has been fixed, the balance equations are supplemented with the closure condition $\sum_{g=1}^{M} P_g = 1$, with $P_g = N_g / \sum_{g=1}^{M} N_g$ the probability that a g-cluster exists; the initial condition is $T = T_a, P_g(0) = \delta_{1g}$, with T_a the room temperature. Note that M is unknown at the beginning: the unknown functions N_g or P_g enter the problem one by one; their number is fixed when the contribution to the crystal volume of the last function entering the problem is found to be negligibly small.

The cluster formation becomes effective when T is in the interval $[T_g, T_m]$. When, during the oscillations, the temperature increases beyond T_g, a portion of the volume crystallizes and the dissipated power lowers due to the decrease in resistance; for the same reason, the amplitude of the oscillations decays. On the other hand, the input power is still sufficient to continue the crystallization process; when the whole material is amorphous, the positive slopes are either R_1 or R_2. If, due to the heating and quenching process, the whole material crystallized, the two slopes would merge, namely, $R_1, R_2 \to R_c$, with R_c the resistance of a crystalline volume equal to that of the original material; when, instead, only a portion of the volume crystallizes, the $V(I)$ relations of the two positive-slope branches read

$$V = (R_S + r_{1(2)})\, I\,, \qquad r_{1(2)}(t) = (1 - \lambda)\; R_{1(2)} + R_c\, \lambda\,, \tag{40.49}$$

where $\lambda(t) = w \sum_{g=1}^{M} g\, N_g$ is the fraction of the crystallized volume (w is the volume of a nucleus). One may relate it to the geometrical parameters of the device by writing $0 \le \lambda = (H - H_{am})/H \le 1$, with $H_{am}(t)$ the length of the material that has not crystallized yet and H the initial length introduced above. Clearly (40.49) holds exactly for a one-dimensional device only; here it is used as an approximation. In turn, the thermal resistance at t is obtained from

$$R_{th} = (1 - \lambda)\, R_{th}^{am} + R_{th}^{cr}\, \lambda\,, \quad A\, R_{th}^{am(cr)} = H\, \rho_{th}^{am(cr)}\,, \tag{40.50}$$

where A is the area of the PCM cross section and ρ_{th} the thermal resistivity; suffix "am" ("cr") refers to the amorphous (crystalline) phase. The values used in the analysis carried out here are taken from [119] and read $H = 100\,\mathrm{nm}$, $A = 180 \times 180\,\mathrm{nm}^2$, $\rho_{th}^{am} = 500\,\mathrm{K\,cm\,W^{-1}}$, and $\rho_{th}^{cr} = 200\,\mathrm{K\,cm\,W^{-1}}$; the value of the thermal capacitance is $C_{th} = c_p\, H\, A$, $c_p = 1.25\,\mathrm{J\,cm^{-3}\,K^{-1}}$ (this parameter does not depend on the phase). The form of the N-shaped curve changes with time due to the time dependence of V_1 and V_2; the oscillation regime continues as long as the current-voltage of the external load intersects the NDR branch of the PCM characteristic.

In conclusion, the model is made of the M equations for $P_1, \ldots, P_M$ combined with (40.46)–(40.50). They constitute a set of nonlinear, coupled equations (differential or algebraic) in the unknowns $P_1, \ldots, P_M$, λ, V, I, T, r_1, r_2, R_{th}. The differential equations of the set are of the first order, which entails an open integration that may become rather cumbersome, also considering that in general M is large; the equations are dealt with, e.g., the integral equation method of [120].

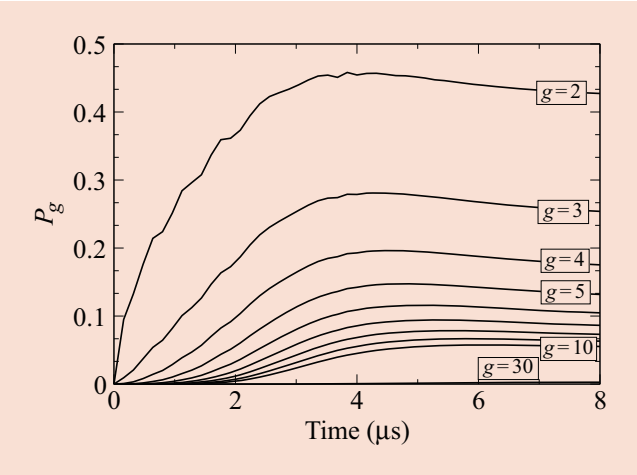

Fig. 40.38 Time dependence of $P_1, \ldots, P_{30}$. (After [114]). The figure shows that in the case in hand the probability of clusters with $g = 30$, or larger, is negligible. Each probability tends to saturate with time

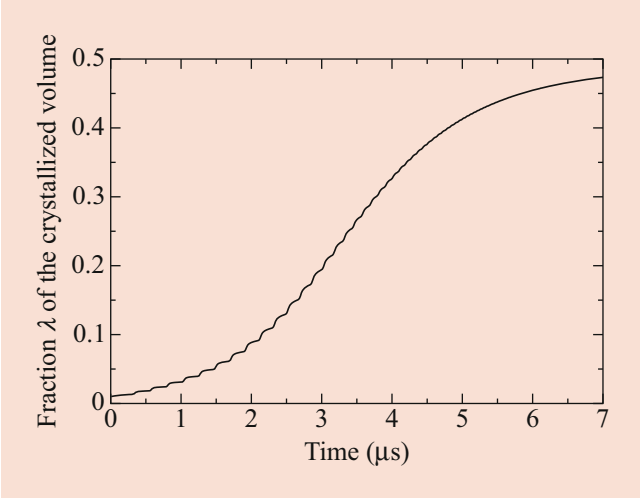

Fig. 40.39 Time dependence of the fraction λ of the crystallized volume. (After [114])

40.5.4 Comparison with Experiments

The model outlined above is compared here with the experiments of [117]. For the case in hand, it was found that the probability of clusters with a size larger than 30 is negligible; this made it possible to fix the value of M. The time dependence of $P_1, \ldots, P_{30}$ is shown in Fig. 40.38: indeed, the probability P_{30} is negligible. As anticipated above, the first peak visible in Fig. 40.35 is due to three-dimensional effects not included in the model; therefore, the comparison with the experiments starts from the second peak.

The integration of the differential equations of the model was carried out using a 5th-order method of the type [120] with a 1-ps discretization time. The circuit parameters were found to be $C = 2$ pF, $I_1 = 1.12$ μA, $I_2 = 33$ μA; in turn, the constant resistances in (40.49), through which the time dependences of voltages $V_1(t)$ and $V_2(t)$ are determined, were found to be $R_S + R_1 \simeq R_1 = 1.6$ MΩ, $R_S + R_2 \simeq R_2 = 24$ kΩ (the approximations are due to the fact that a separate estimate indicates that here R_S is of the order of 100 Ω).

The fraction λ of the crystallized volume, whose change in time is relatively slower than the period of the oscillations, is shown in Fig. 40.39; the decay of the peaks amplitude, visible in Figs. 40.35 and 40.40, is due to the increase in λ as illustrated above.

Finally, Fig. 40.40 compares the model with the experiments: both the decay of peaks due to the progressive crystallization and the oscillation period, are well captured by the model. Due to the peak decay, the crystallization conditions weaken and the fraction of crystallized material saturates (Fig. 40.39). In the case considered here, when saturation occurred the characteristic of the external load and that of the PCM still intersected in the NDR branch: in fact, after some decay, the oscillation amplitude stabilized (Fig. 40.40). In other experiments (not shown), the deformation of the PCM characteristic was such that the bias point shifted out of the NDR branch of the PCM, this eventually bringing the oscillations to an end.

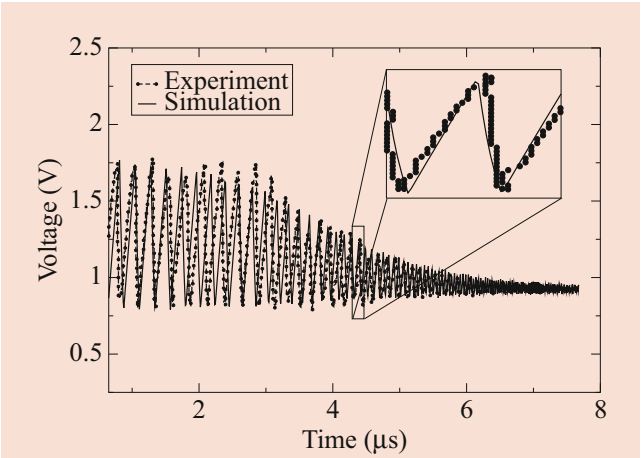

Fig. 40.40 Comparison between model (*continuous line*) and experiment of Fig. 40.35 (*dotted line*). (After [114]). To make the parameter fitting possible, the experimental curve was converted into a discrete set

40.5.5 Stability Analysis of PCM Oscillations

It is of interest to carry out a stability analysis of the electric response of the PCM, in order to ascertain the conditions under which the device electric performances are stable; this task is carried out in this section basing on the model proposed in [14] for the steady-state case and later extended in [73] to the dynamic case. The model can be viewed

as a simplified version of the hydrodynamic approach of Sect. 40.4.2: the electron energy is expressed in terms of the electron temperature T_e, spatial uniformity is assumed, a single energy is considered for the traps, and another single energy is considered for the conduction band. The model reproduces the electrical bistability and is able to identify the conditions that stabilize the measurement [121]; it reads

$$J = q\,\mu\,n_B\,F\,, \qquad \frac{n}{n_B} = 1 + c\,\exp\left(\frac{\Delta E}{k\,T_e}\right), \tag{40.51}$$

$$J\,F = n\,k\,\frac{T_e - T_0}{\tau_R} + \Delta E\,\frac{d}{dt}[n_B(T_e) - n_B(T_0)]\,, \tag{40.52}$$

where μ is the mobility of the band electrons, while J and F are the current density and electric field. As a one-dimensional and uniform device is considered, the equations do not depend on position; for this reason, carrier transport is described by the drift-only equation appearing in (40.51). Symbols T_0 and T_e denote, respectively, the room temperature and the band electron temperature, while τ_R and ΔE are the electron-temperature relaxation time and the difference between the band energy and the trap energy. Finally, c is the ratio between the density of states of the traps and that of the band [14].

The $J\,F$ product in (40.52) is the power per unit volume provided by the field: part of this power is absorbed by the phonons, while the remaining part produces the time change of the electron population of the band; the two parts are described by the first and second term at the right hand side of (40.52), respectively. Globally, (40.52) expresses the power balance of the band electrons. In turn, the second equation in (40.51) links the electron temperature with the fraction n_B/n of the electrons belonging to the band.

The model equations (40.51) and (40.52) in the four unknowns J, F, n_B, and T_e reduce, in the steady-state condition, to an algebraic relation involving only F and J. As the relation between F and J is clumsy, using auxiliary variables is preferable because the resulting expressions are managed analytically with more ease; this advantage manifests itself also in the time-dependent analysis. To proceed one defines the auxiliary variables $r = T_e/T_0$ and $f = F^2/F_0^2$, along with the normalization constants $a = \Delta E/(k\,T_0) = 14$ and $F_0^2 = k\,T_0/(q\,\mu\,\tau_R) = 10^{10}\ \mathrm{V^2\,cm^{-2}}$. Using the auxiliary variables reduces the steady-state form of (40.52) to

$$f = (r-1)\,[1 + c\,\exp(a/r)]\,, \tag{40.53}$$

whose graph is shown in the left part of Fig. 40.41 along with the line $f = f_u = 2.6$, corresponding to $F \simeq 1.6 \times 10^5$ V/cm. The latter value has been chosen purposedly, because the $f = 2.6$ line intersects the $f(r)$ curve in three points of which, in particular, the $r_u = 1.4$ one belongs to the branch of $f(r)$ having a negative slope. As in this representation the independent variable is r, the devices must be considered as "temperature driven" and constant field loaded.

Stability Analysis

To analyze stability one must use the dynamic model (40.51) and (40.52) and focus on the $r = r_u$ equilibrium point (in fact, the two intersections with the positive-slope branches are stable). Letting

$$N(r,f) = (r-1)\,\frac{n}{n_B} - f\,, \quad D(r) = \frac{a^2}{r^2}\left(\frac{n_B}{n} - 1\right). \tag{40.54}$$

turn (40.52) into

$$\frac{dr}{d\theta} = A(r,f) = \frac{N(r,f)}{D(r)}\,, \qquad \theta = \frac{t}{\tau_R}\,, \tag{40.55}$$

to be coupled with $df/d\theta = 0$ which is the differential equation for f. As in dynamic conditions (40.53) is not fulfilled, the right hand side of (40.55) does not vanish, apart from the equilibrium point where $N_u = N(r_u, f_u) = 0$. The analysis is carried out in the standard way [122], namely, by examining the system behavior near equilibrium; linearizing (40.55) about (r_u, f_u) after letting $r = r_u + \delta r$, $f = f_u$ yields $d(\delta r)/d\theta = s_{ru}\,\delta r$ and $s_{ru} = (\partial A/\partial r)_u$, whence $\delta r = \delta r_{t=0}\,\exp(s_{ru}\,\theta)$. Thus, the equilibrium point is stable (unstable) if $s_{ru} < 0$ ($s_{ru} > 0$). From (40.55) one finds $s_{ru} = (D_u\,N_u' - N_u\,D_u')/D_u^2$ with $N_u = 0$ and $D_u = (a/r)^2\,(n_B/n - 1) < 0$ for all r. It follows $s_{ru} = -N_u'/|D_u|$, so that stability is prescribed by the sign of N_u'. On the other hand,

$$N_u' = \left(\frac{\partial N}{\partial r}\right)_u = \frac{n}{n_B} - a\,\frac{r-1}{r^2}\left(\frac{n}{n_B} - 1\right), \tag{40.56}$$

which may have either sign; thus, the limit between stability and instability corresponds to $N_u' = 0$, namely, from (40.51),

$$r_u^2 - a\,(r_u - 1) = -\frac{r_u^2}{c}\,\exp(-a/r_u). \tag{40.57}$$

whose graphic solution is visible in the right part of Fig. 40.41. Two solutions r_{u1}, r_{u2} exist, indicated with the vertical lines: in the interval $r_{u1} < r_u < r_{u2}$, it is $N_u' < 0$ and $s_{ru} = N_u'/D_u > 0$; therefore, the solution at $r_u = 1.4$ is unstable. As from (40.53), (40.54) it also follows that $\partial N/\partial r = 0$ is equivalent to $df/dr = 0$, points r_{u1} and r_{u2} are the boundaries of the negative-slope branch; in other terms, for a load like $f = \text{const}$, all points of this branch are unstable, as expected.

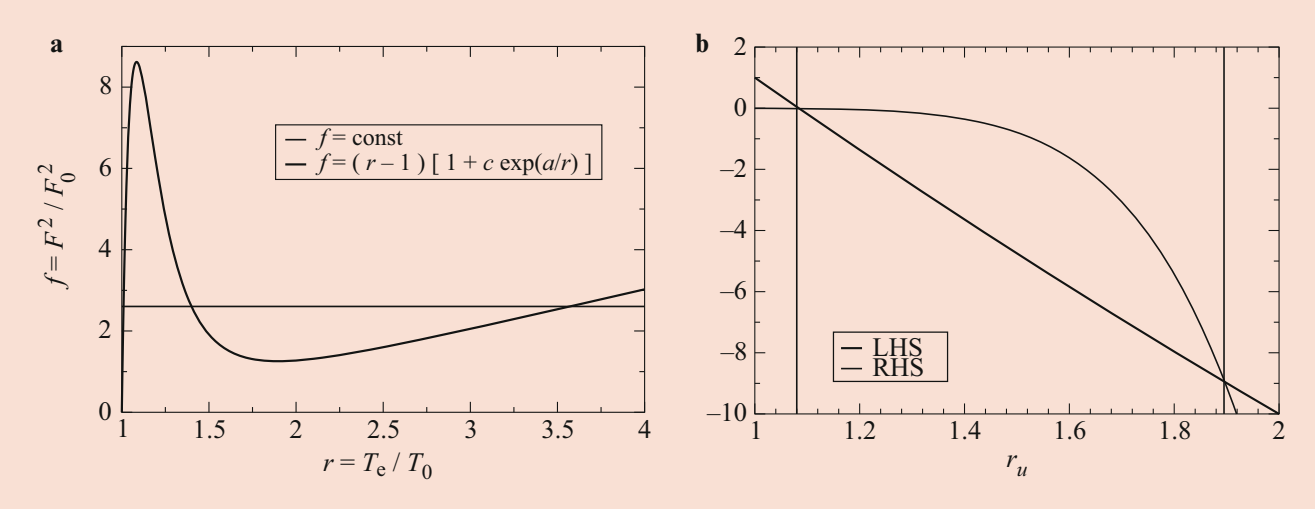

Fig. 40.41 (**a**) Graph of (40.53) (*thick line*) intersecting $f = f_u = 2.6$ in three equilibrium points; the one corresponding to $r_u = 1.4$ intersects (40.53) in the negative-slope branch. (**b**) Graphic solution of (40.57); the left (right) hand side is represented by the *thick (thin) line*, while the *vertical lines* indicate the two solutions r_{u1}, r_{u2}. (Both figures after [121])

Variable-Field Case

To carry out the stability analysis when the electric field to which the Ovonic device is subjected is allowed to change, one connects a series resistance R to the device and applies a voltage V_C as shown in Fig. 40.42, so that $V_C = V + RI$ with $V = LF$ the voltage across the device. The length and cross-sectional area of the latter are L, A, with $I = AJ$ the current through it. As in the previous analysis, the sample is considered one-dimensional and uniform; hence the equations do not depend on position. Letting L_R and A_R be the length and cross-sectional area of the resistor and $\rho = RA_R/L_R$ the resistivity of its material, one finds $V_C/L_R = \lambda F + \alpha\rho J$ with $\lambda = L/L_R$ and $\alpha = A/A_R$. Replacing J from (40.51) provides

$$\frac{F}{F_C} = \frac{1 + c\,\exp(a/r)}{\omega + 1 + c\,\exp(a/r)}\,, \qquad F_C = \frac{V_C}{L}\,, \tag{40.58}$$

with $m = \rho q \mu n$, $\omega = m\alpha/\lambda$ dimensionless parameters. Taking the $\omega \to 0$ limit in the above yields the original setup $R = 0$; the $R \neq 0$ setup is actually able to increase the number of degrees of freedom of the system and to provide the necessary information about the measurement stability. The load curve is obtained by taking the square of the first of (40.58) and letting $f_C = F_C^2/F_0^2$,

$$\frac{f}{f_C} = \left[\frac{1 + c\,\exp(a/r)}{\omega + 1 + c\,\exp(a/r)}\right]^2 . \tag{40.59}$$

shown in Fig. 40.43. Due to the choice of the variables, the load curve is not a straight line although a linear resistor R is used in the bias circuit. This does not affect the stability analysis, which is carried out by linearizing (40.55) along with

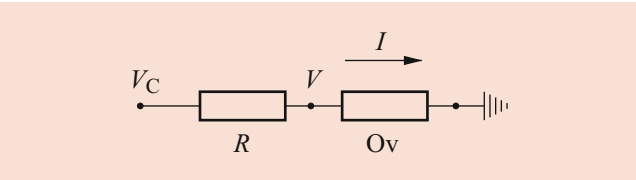

Fig. 40.42 When a resistance R is connected to the Ovonic device (Ov), the load characteristic is controlled by the value of R and of the applied voltage V_C, or other two parameters related to them (e.g., f_C and ω introduced in the text). (After [121])

$$B(r,f) = \frac{f}{f_C} - \left[\frac{1 + c\,\exp(a/r)}{\omega + 1 + c\,\exp(a/r)}\right]^2 = 0 \tag{40.60}$$

around r_u, f_u; letting

$$s_{ru} = \frac{N'_u}{D_u}\,, \quad w_{ru} = -\frac{\mathrm{d}}{\mathrm{d}r}\left[\frac{1 + c\,\exp(a/r)}{\omega + 1 + c\,\exp(a/r)}\right]_u^2, \tag{40.61}$$

one finds $\mathrm{d}(\delta r)/\mathrm{d}\theta = s_{ru}\,\delta r - \delta f/D_u$ and $w_{ru}\,\delta r = -\delta f/f_C$ whence, eliminating δf from the latter yields $\mathrm{d}(\delta r)/\mathrm{d}\theta = (N'_u + f_C\,w_{ru})\,\delta r/D_u$. Remembering that $D_u < 0$, one finds that the equilibrium point is stable when $N'_u + f_C\,w_{ru} > 0$, unstable when $N'_u + f_C\,w_{ru} < 0$. It is $N'_u < 0$ along the negative-slope branch, whereas

$$w_{ru} = \frac{2\,\omega\,a/r_u^2}{(\omega + n/n_B)^3}\left(\frac{n}{n_B} - 1\right)\frac{n}{n_B} > 0\,. \tag{40.62}$$

It follows that the sign of $N'_u + f_C\,w_{ru}$ depends on the value of f_C and ω. Replacing N'_u with $\mathrm{d}f/\mathrm{d}r$ and observing that

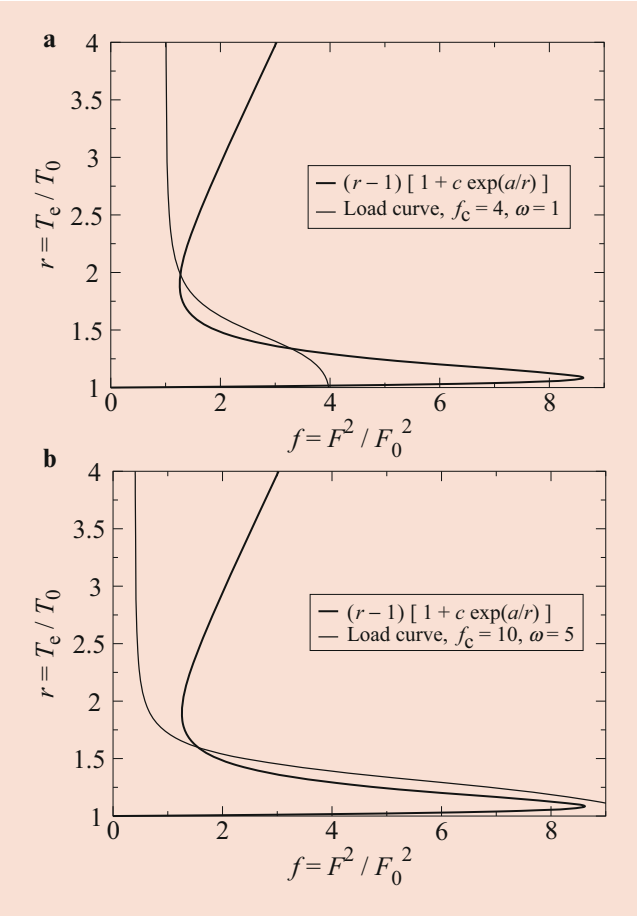

Fig. 40.43 (**a**) Inverse function of (40.53) (*thick line*) and of (40.59) with $f_C = 4$, $\omega = 1$ (*thin line*). The three intersections correspond to equilibrium points, of which the unstable one belongs to the negative-slope branch ($f_u \simeq 3.3$). (**b**) The thick line is the same as in the upper part of the figure; the thin line shows the inverse function of (40.59), with $f_C = 10$, $\omega = 5$. The two lines cross each other in only one point belonging to the negative-slope branch; this equilibrium point is stable. (Both figures after [121])

$-f_C\, w_{ru}$ is the derivative of (40.59) with respect to r, one renders the stability condition in compact form as $|\mathrm{d}f/\mathrm{d}r|_{\text{load}} > |\mathrm{d}f/\mathrm{d}r|_{\text{Ov}}$. Note that, in order to check the above inequality in Fig. 40.43, one must view the slopes from the r axis. For instance, point $f_u \simeq 3.3$ in the upper part of Fig. 40.43 is unstable, whereas the intersection between the Ovonic and load curves in the lower part of Fig. 40.43 is stable.

The analysis outlined above shows that a suitable tuning of the load curve provides a stable intersection point with the negative-slope branch. Thus, by choosing successive values of V_C and/or R, one sweeps the negative-slope branch completely, this making the measurement of the whole $I(V)$ curve possible.

This theory assumes that the time variation of the unknowns derives from the last term of (40.52) only, namely, is due to the internal behavior of the device; parasitic effects induced by the measuring equipment are not included. In fact these effects exist, and their description is achieved by adding a capacitance C in parallel to the Ovonic device. The new time constant $\tau = R\,C$ thus introduced is to be compared with the intrinsic one produced by the interplay of τ_R and ΔE of (40.52). Although the quantitative results are influenced by the new time constant, the analysis of stability is unaffected.

40.6 Open Challenges in Modeling: A Brief Outline

In the last 60 years, amorphous chalcogenide materials have provided many challenges to the scientific community working in the field of modeling and simulation. Despite an intense effort, both in academia and industry, which has already led to the release of products into the market, open questions still remain as for the physical models and numerical approaches. On the one side, it is clear that both charge and heat transport must be taken into account to model chalcogenide devices and that, close to threshold, an interplay between carrier and crystal heating determines whether the OTS or PCM effect, or both take place; on the other side, uncertainty still exists about the parameters to be included for simulating the material at hand. MD simulations, which proved very effective to characterize atomic structures and atomic states, are still not accurate enough as for the information about the trap and band density of states to be included into a transport simulation. The role of the interface between the electrodes and the amorphous chalcogenide and the effect of the electrode material on the switching voltage, typically accounted for as boundary conditions of the transport model, need to be modeled more accurately [123].

As PCM devices were integrated with advanced CMOS technology nodes, the necessity became apparent of scaling their dimensions to the nanometer range; the reduced dimensions require, in turn, a simulation approach to transport that goes beyond the hydrodynamic scheme. In fact, it is still questionable whether the ability to switch between two states, whose electrical conductivities differ by at least two orders of magnitude, is preserved in layers where the size of the amorphous region becomes comparable to the distance between two trap centers [81]. Also, the granularity of the atomic composition of the layer suggests that noise plays a key role in determining the electric response of these nanometer scale devices; at present, noise is one of the least studied topics of chalcogenide device physics. Furthermore, under extreme miniaturization the device dimensions become comparable to the wavelength of the carriers; numerical approaches based on quantum transport schemes are then necessary [101, 102, 124]. The energy exchange between carriers and lattice, commonly dealt with by assuming a

relaxation time approximation, is also likely to require a more accurate modeling in chalcogenides.

New materials are being envisaged to open new perspectives. Modeling tools are required to engineer the best alloy composition in order to fulfill assigned technology requirements [86]. The use of monatomic phase-change materials may remove compositional optimization issues and make nanosize elements for information storage more easily achievable [125]. Single-atom-scale Te nanowires encapsulated in carbon nanotubes constitute the smallest periodic materials with atom-wide motifs repeated in one dimension; single-walled carbon nanotubes provide ideal environments for the creation of such materials [126]. The ability to control functional properties of these systems opens the way to the implementation of future device applications. Furthermore, chalcogenide superlattice structures demonstrated superior switching performance in terms of time and energy [127]; the well-established expertise in the field of simulation of low-dimensional semiconductors can fruitfully be exploited to support the experimental activity in this area.

In another direction, the need of modeling PCM and OTS, starting from the device level and up to the description of circuits made of these devices, is strongly felt. The implementation of large arrays where the memory elements are PCM with OTS-based selectors is, in fact, one of the most studied candidates for next-generation, nonvolatile memories (NVM). On the one side, it is compatible with the standard process of integrated circuits; on the other side, using two- instead of three-terminal devices is quite attractive for manufacturers, as this approach simplifies the memory layout and allows achieving a very dense storage capability in the back end of line (BEOL).

Last, but not least, multilevel storage and non-von Neumann neuromorphic computer architectures using PCM foresee the possibility of incrementally crystallize the amorphous chalcogenide layer of the device by applying low-power pulses. A physics-based simulation of the process must couple the heat and transport equations with the numerical simulation of the nucleation process. A deeper insight into the aging effects is mandatory [38] to envisage applications of chalcogenides to neuromorphic computing [42].

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Application of the $k \cdot p$ Method to Device Simulation

41

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Contents

41.1 Introduction 1492

41.2 The Eight-Band k·p Model 1493
41.2.1 Bulk Unstrained Semiconductors 1493
41.2.2 Strained Semiconductors 1495
41.2.3 Confined Structures 1496

41.3 The k · p Method Applied to Tunnel Field-Effect Transistors 1498
41.3.1 Device Structures 1498
41.3.2 Impact of Strain on the Tunneling Current of Homojunction TFETs 1499
41.3.3 Impact of Strain on the Tunneling Current of Heterojunction TFETs 1500
41.3.4 GaSb-/InAs-Based TFET Optimization Exploiting Strain and Device Geometry 1502

41.4 TFET Inverters for a Complementary Technology Platform 1503

41.5 Modelling of Interface Traps in the k · p Scenario 1507

41.6 Conclusions 1509

References 1512

Abstract

As electronic devices approach the sub 10-nm size and new device topologies emerge specifically exploiting quantum mechanical effects, new device simulation tools are needed addressing such issues. Among full quantum approaches, the $\boldsymbol{k} \cdot \boldsymbol{p}$ model is known to provide a reasonably simple way to describe with good accuracy the complex system of valence and conduction bands of many semiconductors, including also their deformations induced by strain, which play a fundamental role in determining the electronic properties of the material. When used within the Non-Equilibrium Green's Functions framework for the charge transport problem and coupled with Poisson's equation, the $\boldsymbol{k} \cdot \boldsymbol{p}$ model becomes a powerful tool for the simulation of full nanoelectronic devices featuring lateral confinement and quantum transport.

In this chapter, a review of the $\boldsymbol{k} \cdot \boldsymbol{p}$ model is presented, with special emphasis on its applications to the simulation of nanoelectronic devices. The mathematical model of the so called eight-band version is duly recalled first, including the correction terms accounting for strain. Examples of energy band calculations are provided for III–V semiconductors, which are of great potential for the future development of the nanoelectronic industry, relative to both bulk and confined structures.

Significant examples of application of the $\boldsymbol{k} \cdot \boldsymbol{p}$ model to full device simulation are then given, all of them relative to tunnel FETs. Specific topics include the investigation of strain in homojunction and heterojunction nanowire tunnel FETs, the optimization of complementary tunnel FETs and the evaluation of the performance of inverters built with the latter FETs, the investigation of the effect of interface traps on the same nanowire tunnel FETs.

The main idea that this chapter would like to convey is that in the next future there will most likely be an increasing type and number of nanoelectronic devices for which the $\boldsymbol{k} \cdot \boldsymbol{p}$ model represents a well targeted simulation basis.

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k.p Hamiltonian · Band structure · Effective mass · Heterojunction · III–V semiconductor · Nanowire · Strain · Tunnel FET · Band-to-band tunneling

41.1 Introduction

Technology computer-aided design (TCAD) tools have actually replaced the former trial-and-error methodology for device design in the nanoscale, and its impact in terms of shortening the technology cycle is now widely recognized. The progressive device miniaturization down to minimum feature sizes of a few tens of nanometers anyway requires a continuous development of the modeling approaches. More specifically, the next-generation devices based on nanowire technologies will experience shrinkage in the transversal direction by structural confinement, leading to an increasing importance of quantization effects and the formation of energy subbands. In addition, as the gate length becomes comparable with the carrier mean-free path, carrier transport becomes quasi-ballistic. Thus, most carriers travel with a kinetic energy well above the band edge, where the subband energy dispersion relationships $E_n(k)$ are no longer parabolic and the effective-mass approximation (EMA) breaks down. Moreover, band-to-band and direct source-to-drain tunneling become increasingly important in scaled devices, while strain engineering continues to keep an important role as technology booster. On the other hand, novel device concepts are being developed, featuring band-to-band tunneling as the key working principle, leading to abrupt transition between the off- and on-states and allowing for a substantial reduction of the supply voltage. The performance of such new tunnel FET (TFET) devices will be largely improved by the use of III–V compound semiconductors, which are direct gap materials with small effective masses. A detailed description of the latter technologies is reported in Chaps. ▶ 6 and ▶ 9. The device architecture and operation principles are addressed in Chap. ▶ 24.

For the modeling tools to keep the pace with the technological developments and preserve their predictive capabilities, new specific modeling tools and schemes are therefore necessary accounting for the above quantum effects as well as for the relevant electronic properties of the new III–V channel materials, also in the presence of strain.

Concerning quantum approaches, a first classification can be made according to the adopted Hamiltonian model, which is built upon well-established theories for the calculation of the electronic and optical properties of solids. Tight-binding (TB) is an atomistic model, which has been proven very powerful also for device simulation, as described in Chap. ▶ 45. Provided a sufficient number of orbital functions per atom are included in the calculation, the full band structure of most semiconductors, including also the effect of mechanical strain, can be accurately captured by the TB model. Besides, defects at atomic level can be naturally accounted for. Of course, there is a limitation on the maximum number of atoms, and therefore the maximum device size, that can be handled in practical computations.

The $\boldsymbol{k} \cdot \boldsymbol{p}$ theory is another important semiempirical approach that has been very successful for understanding all the main properties of most semiconductors. Fundamental for its development have been the works of Luttinger and Kohn [1] and Kane [2]. Its basic principles are now illustrated in many solid-state physics textbooks [3–5], and detailed derivations of its many forms can be found in specialized literature [6]. In essence, the theory is based on a perturbation method around a high symmetry point of the crystal momentum space and leads to a $\boldsymbol{k}$-dependent Hamiltonian matrix, which in a space-dependent problem (i.e., in device simulation) becomes a differential operator acting on the multiple components of the wave-function envelope. Eventually, the resulting system of partial differential equations is discretized, typically by means of a finite-difference scheme. Therefore, as opposed to TB, the $\boldsymbol{k} \cdot \boldsymbol{p}$ method gives the user the flexibility of selecting a suitable discretization grid, resulting in a considerable saving of computational resources.

Even if it is possible to extend the $\boldsymbol{k} \cdot \boldsymbol{p}$ theory to the full Brillouin zone using an adequate number of basis functions [7], one of the major attractiveness of the theory, as far as device simulation is concerned, is its capability of providing a complete description of the complex system of valence bands around the Γ-point using only a limited number of basis functions, namely, six. Moreover, in the so-called eight-band version (i.e., with eight basis functions) [6], the description is extended to the first conduction band of direct bandgap semiconductors. For this reason, the method has been applied to full device simulation involving hole transport in silicon nanowires [8] and band-to-band tunneling in InAs nanowires [9] and has found since then a rather wide application in the simulation of novel devices employing several types of direct bandgap materials, such as III–V alloys, namely, when tunneling effects are to be investigated in detail [10–12]. To this purpose, the $\boldsymbol{k} \cdot \boldsymbol{p}$ algorithm is coupled with the nonequilibrium Green's function (NEGF) formalism as described in Chap. ▶ 44.

This chapter deals in particular with the eight-band $\boldsymbol{k} \cdot \boldsymbol{p}$ model and its applications to the simulation of III–V TFETs. The mathematical model is described in Sect. 41.2, where the Hamiltonian matrix, including also strain, is reported in full. The section includes a survey of the main band structure features and results for some bulk III–V materials and, for similar confined structures, underlying the effect of strain in particular. Section 41.3 is devoted to the applications of the model to the investigation of III–V TFETs under different stress conditions. An optimization study of TFET-based inverters for a complementary technology platform carried out in the framework of the $\boldsymbol{k} \cdot \boldsymbol{p}$ approach is addressed in Sect. 41.4. Finally, a simulation study where transport is treated with the $\boldsymbol{k} \cdot \boldsymbol{p}$ model and interface traps are also

consistently accounted for in the device electrostatics is described with details and examples in Sect. 41.5.

41.2 The Eight-Band k·p Model

In this section, the mathematical model of the Hamiltonian matrix for 3D bulk semiconductors is introduced first with an exhaustive description of the equations for the eight-band $\boldsymbol{k} \cdot \boldsymbol{p}$ model. The additional assumptions and equations required to accurately account for mechanical deformation are discussed along with some examples of calculated bulk band structures in unstrained and strained conditions. The generalization to confined structures is finally treated with special focus on 1D nanowire devices as the most promising potential candidates for future applications.

41.2.1 Bulk Unstrained Semiconductors

With the set of basis functions

$$[S\uparrow,\ X\uparrow,\ Y\uparrow,\ Z\uparrow,\ S\downarrow,\ X\downarrow,\ Y\downarrow,\ Z\downarrow]^{\mathrm{T}}\,, \tag{41.1}$$

where the arrows indicate the spin orientation, S the s-like spatial function for the conduction band and X, Y, and Z the p-like spatial functions for the valence band, the eight-band $\boldsymbol{k} \cdot \boldsymbol{p}$ Hamiltonian for values of $\boldsymbol{k}$ near the Γ point of zinc-blende crystals can be written as

$$H_8 = \begin{bmatrix} H_4 & 0 \\ 0 & H_4 \end{bmatrix} + H_{\mathrm{SO}}\,, \tag{41.2}$$

where H_4 is a 4×4 matrix given by

$$H_4 = \begin{bmatrix} H_{\mathrm{CC}} & H_{\mathrm{CV}} \\ H_{\mathrm{VC}} & H_{\mathrm{VV}} \end{bmatrix}\,, \tag{41.3}$$

with H_{CC}, H_{VV}, and H_{CV} reported below, and H_{SO} is the spin-orbit coupling matrix

$$H_{\mathrm{SO}} = \frac{\Delta}{3}\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & -i & 0 & 0 & 0 & 0 & 1 \\ 0 & i & -1 & 0 & 0 & 0 & 0 & -i \\ 0 & 0 & 0 & -1 & 0 & -1 & i & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & -1 & i & 0 \\ 0 & 0 & 0 & -i & 0 & -i & -1 & 0 \\ 0 & 1 & i & 0 & 0 & 0 & 0 & -1 \end{bmatrix}\,, \tag{41.4}$$

i being the imaginary unit and Δ the spin-orbit splitting parameter. In (41.3), H_{CC} is a scalar

$$H_{\mathrm{CC}} = E_{\mathrm{C}} + A_{\mathrm{C}}k^2\,, \tag{41.5}$$

where E_{C} is the conduction band edge, $k = \|\boldsymbol{k}\|$ and

$$A_{\mathrm{C}} = \frac{\hbar^2}{2m_{\mathrm{o}}}(1+2F)\,, \tag{41.6}$$

with m_{o} the free-electron mass and F the Kane parameter, which is formally related with the momentum matrix elements between the s-like conduction band and the remote bands. $H_{\mathrm{CV}} = H_{\mathrm{VC}}^{\dagger}$ is written as

$$H_{\mathrm{CV}} = [iPk_x \quad iPk_y \quad iPk_z]\,, \tag{41.7}$$

where the parameter P introduced by Kane

$$P = -\frac{i\hbar}{m_{\mathrm{o}}}\langle S|p_x|X\rangle \tag{41.8}$$

is proportional to the momentum matrix element between the s-like conduction band and the p-like valence band. H_{VV} is a 3×3 matrix given by

$$H_{\mathrm{VV}} = \begin{bmatrix} E_{\mathrm{V}} + Lk_x^2 + M(k_y^2+k_z^2) & Nk_xk_y & Nk_xk_z \\ Nk_yk_x & E_{\mathrm{V}} + Lk_y^2 + M(k_z^2+k_x^2) & Nk_yk_z \\ Nk_zk_x & Nk_zk_y & E_{\mathrm{V}} + Lk_z^2 + M(k_x^2+k_y^2) \end{bmatrix}\,, \tag{41.9}$$

where E_{V} is the valence band edge. The parameters L, M, and N are expressed in terms of the modified Luttinger parameters by

$$\begin{aligned} L &= -\frac{\hbar^2}{2m_{\mathrm{o}}}(\gamma_1 + 4\gamma_2)\,, \\ M &= -\frac{\hbar^2}{2m_{\mathrm{o}}}(\gamma_1 - 2\gamma_2)\,, \\ N &= -\frac{\hbar^2}{2m_{\mathrm{o}}}(6\gamma_3)\,, \end{aligned} \tag{41.10}$$

the modified parameters being in turn related with the original Luttinger parameters, which formally depend on the momentum matrix elements between the p-like valence bands and the remote bands, by

$$\begin{aligned} \gamma_1 &= \gamma_{1\mathrm{L}} - \frac{E_{\mathrm{P}}}{3E_{\mathrm{G}}}\,, \\ \gamma_2 &= \gamma_{2\mathrm{L}} - \frac{E_{\mathrm{P}}}{6E_{\mathrm{G}}}\,, \\ \gamma_3 &= \gamma_{3\mathrm{L}} - \frac{E_{\mathrm{P}}}{6E_{\mathrm{G}}}\,, \end{aligned} \tag{41.11}$$

where $E_P = (2m_o/\hbar^2)P^2$ and $E_G = E_C - E_V$ is the energy gap.

From the above equations, it is seen that the 8×8 $\boldsymbol{k} \cdot \boldsymbol{p}$ Hamiltonian is completely defined by the following set of seven parameters: the three Luttinger parameters γ_{1L}, γ_{2L} and γ_{3L}, the energy gap E_G, the band-coupling parameter P, the conduction band parameter F, and the spin-orbit splitting Δ. Though in principle such parameters can be calculated from their formal definitions in terms of matrix elements with first-principle methods, in practice they are extracted through a calibration on experimentally observable quantities. To this end, the following useful expressions of the electron effective mass m_e and of the light-hole (m_{lh}), heavy-hole (m_{hh}), and split-off (m_{so}) effective masses along high symmetry directions are obtained from the calculation of the eight-band energy dispersion relation

$$\frac{m_o}{m_e} = 1 + 2F + \frac{E_P(E_G + 2\Delta/3)}{E_G(E_G + \Delta)}, \tag{41.12}$$

$$\left(\frac{m_o}{m_{hh}}\right)_{[100]} = \gamma_{1L} - 2\gamma_{2L},$$
$$\left(\frac{m_o}{m_{hh}}\right)_{[111]} = \gamma_{1L} - 2\gamma_{3L}, \tag{41.13}$$

$$\left(\frac{m_o}{m_{lh}}\right)_{[100]} = \gamma_{1L} + 2\gamma_{2L},$$
$$\left(\frac{m_o}{m_{lh}}\right)_{[111]} = \gamma_{1L} + 2\gamma_{3L}, \tag{41.14}$$

$$\frac{m_o}{m_{so}} = \gamma_{1L} - \frac{E_P\Delta}{3E_G(E_G + \Delta)}. \tag{41.15}$$

An exhaustive compilation of the required parameters for the main III–V binary materials as well as ternary and quaternary alloys is found in [13], together with the valence band offsets for III–V heterostructures. In the case of alloys, linear or quadratic interpolating expressions are used as a function of the alloy composition.

Examples of bulk band structures are shown in Figs. 41.1 and 41.2. They refer to bulk GaAs and InAs crystals and are calculated along the [100] and [110] directions. Every band is spin degenerate. It is seen that the spin-orbit parameter Δ is mainly responsible for the breaking of the sixfold degeneracy of the valence band at the Γ-point into two groups, the first one fourfold degenerate, including light and heavy holes, and the second one double degenerate (split-off band). One can also notice the significant band non-parabolicity, especially for the conduction and *lh* bands in low bandgap materials. This makes the simple effective mass model inaccurate and is one of the reasons for going to the $\boldsymbol{k} \cdot \boldsymbol{p}$ approach.

The complex branches of the energy dispersion relation play an important role in devices where band-to-band tunneling is involved, such as tunnel FETs. Figures 41.3 and 41.4 show the bulk GaAs and InAs complex band structures along the [100] direction. They have been calculated by solving the inverse eigenvalue problem, i.e., by finding for any energy E the corresponding values of $\boldsymbol{k}_{100} \in \mathbb{C}$. In the figures, $|k|$ is reported on the x-axis if k is real and $-|k|$ if k is imaginary. Band-to-band tunneling is controlled by the shape of the imaginary branch connecting the valence and the conduction band edges. Since the *so*-band is not directly involved in the tunneling process, one is tempted to ignore spin-orbit coupling by setting $\Delta = 0$ and adjusting F in (41.12) in order

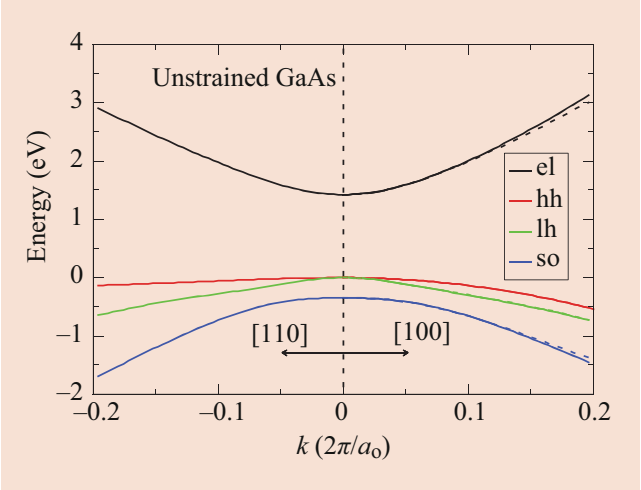

Fig. 41.1 Energy dispersion for the unstrained bulk GaAs along the [100] and [110] crystal directions. Continuous lines: bands calculated using the $\boldsymbol{k} \cdot \boldsymbol{p}$ approach with spurious solutions. Dashed lines in the [100] direction: bands calculated using the $\boldsymbol{k} \cdot \boldsymbol{p}$ approach with the changes proposed in [15]

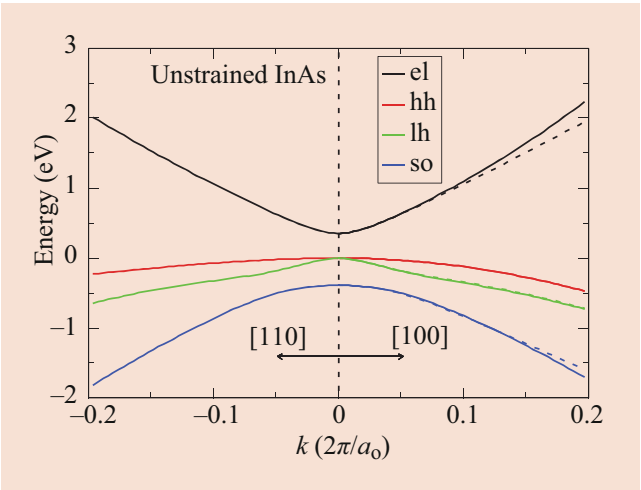

Fig. 41.2 Energy dispersion for the unstrained bulk InAs along the [100] and [110] crystal directions. Continuous lines: bands calculated using the $\boldsymbol{k} \cdot \boldsymbol{p}$ approach with spurious solutions. Dashed lines in the [100] direction: bands calculated using the $\boldsymbol{k} \cdot \boldsymbol{p}$ approach with the changes proposed in [15]

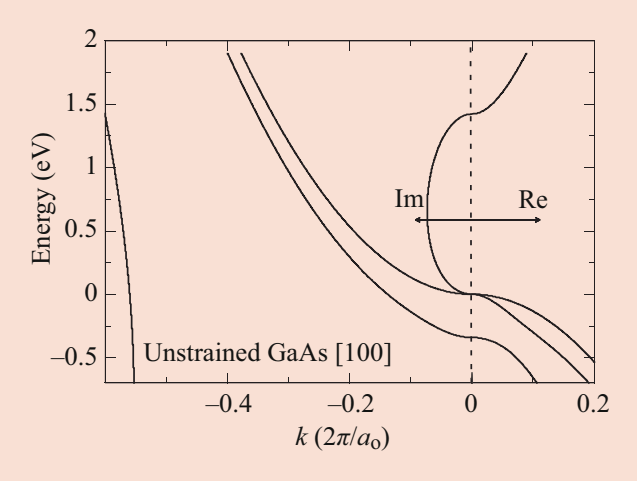

Fig. 41.3 Complex band structure for the unstrained bulk GaAs along the [100] crystal direction

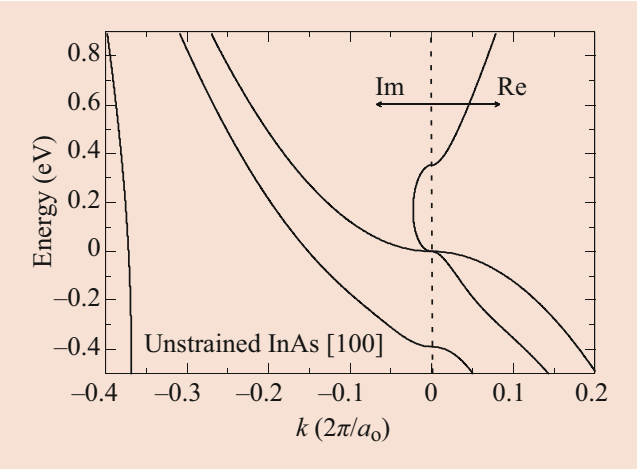

Fig. 41.4 Complex band structure for the unstrained bulk InAs along the [100] crystal direction

to obtain the correct electron effective mass. This procedure effectively reduces the Hamiltonian to a 4×4 matrix, with a significant numerical speedup in device simulations and is referred to as 4×4 $\boldsymbol{k} \cdot \boldsymbol{p}$ method. However, it must be noticed that so doing the total valence-band density-of-states is slightly modified, since without spin-orbit coupling the *so*-band collapses on top of the *hh*-band. The impact of this change on the simulated device behavior ultimately depends on the position of the Fermi level, and the opportunity of such simplification must be considered on a case by case basis.

In Figs. 41.3 and 41.4, the leftmost imaginary branch, which is not connected to any real branch, can be considered a spurious unphysical solution and is related with the high-order terms in k in the characteristic equation. Such spurious solutions can endanger the validity of the results of $\boldsymbol{k} \cdot \boldsymbol{p}$ calculations, in particular for confined heterostructures (quantum wells and wires), depending also on the model parameters as well as on the discretization grid [14, 15], where they can give rise to unphysical non-evanescent states within the gap. One possible recipe to solve this problem consists in a careful modification of the parameter E_P. For example, in [15] A_C in (41.5) is set equal to zero, thus reducing the order of the characteristic equation, at the same time modifying E_P through (41.12) and (41.6) so as to obtain the correct value of the electron effective mass. The required change in E_P is rather small for most important III–V Semiconductors, and, since the values of the effective masses are preserved, only the non-parabolic parts of the band structures are slightly modified. Figures 41.1 and 41.2 show (dotted lines, [100] direction) that this is indeed the case for bulk GaAs and InAs.

41.2.2 Strained Semiconductors

The mechanical deformation of the crystal leads to a displacement of the atomic sites and to a change in the energy-band structure. The $\boldsymbol{k} \cdot \boldsymbol{p}$ theory in the presence of strain has been developed in [16] and [17, 18]. The main result is that in order to account for strain, it is necessary to add to the matrix H_4 in (41.3) a strain-dependent matrix D function of the components ε_{ij} of the strain tensor [17, 18] given by

$$D = \begin{bmatrix} D_{CC} & D_{CV} \\ D_{VC} & D_{VV} \end{bmatrix}, \tag{41.16}$$

where

$$D_{CC} = a_c(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}), \tag{41.17}$$

$$D_{CV} = \begin{bmatrix} b'\epsilon_{yz} - iP\sum_j \varepsilon_{xj}k_j & b'\epsilon_{zx} - iP\sum_j \varepsilon_{yj}k_j \\ & b'\epsilon_{xy} - iP\sum_j \varepsilon_{zj}k_j \end{bmatrix}, \tag{41.18}$$

$$D_{VV} = \begin{bmatrix} l\varepsilon_{xx} + m(\varepsilon_{yy} + \varepsilon_{zz}) & n\varepsilon_{xy} & n\varepsilon_{xz} \\ n\varepsilon_{yx} & l\varepsilon_{yy} + m(\varepsilon_{xx} + \varepsilon_{zz}) & n\varepsilon_{yz} \\ n\varepsilon_{zx} & n\varepsilon_{zy} & l\varepsilon_{zz} + m(\varepsilon_{xx} + \varepsilon_{yy}) \end{bmatrix}, \tag{41.19}$$

and $D_{VC} = D_{CV}^{\dagger}$.

In (41.17) and (41.18), the deformation-potential constants a_c and b' describe the conduction-band strain interactions due to hydrostatic and shear deformations, respectively. The effect of b' is small and is often neglected. It is exactly zero in a diamond structure. The coefficients l, m, and n in (41.19) are related to the Pikus–Bir deformation-potential constants a_v, b, and d through

$$
\begin{aligned}
l &= 2b + a_\mathrm{v} \\
m &= a_\mathrm{v} - b \\
n &= \sqrt{3}d\,,
\end{aligned}
\tag{41.20}
$$

which are tabulated in [19] and [13] for the main III–V semiconductors. The parameter a_c can be easily related to the change in the conduction-band edge energy due to a hydrostatic deformation. It is negative in general, meaning that a compressive hydrostatic strain ($\varepsilon_{xx} = \varepsilon_{yy} = \varepsilon_{zz} < 0$) shifts the conduction band upward. Similarly, a positive a_v shifts the valence-band edge downward for a compressive hydrostatic deformation. The effect of both for compressive hydrostatic strain is therefore an increase in energy gap, which is the quantity that is directly measured. Finally, parameters b and d are responsible for *lh*- and *hh*-band splitting under non-hydrostatic strain configurations.

Additional strain interaction terms related to the spin-orbit coupling are reported in [17, 18]. They should be added to the H_SO matrix (41.4). They are typically small and are not considered here. The interested reader is referred to the original paper [17, 18] for details.

An example of band structure of a III–V semiconductor crystal subject to strain is shown in Fig. 41.5. The material is GaAs, and both the real and imaginary branches are reported as a function of the normalized k in the [001] direction. A biaxial stress condition in the [110] plane is applied, i.e., the only non-null stress tensor components T_{ij} are $T_{xx} = T_{yy} \equiv T \neq 0$, being the coordinate reference system aligned with the main crystal axes. The strain tensor components are calculated using the elastic constant matrix. In crystals with cubic symmetry, there are only three independent elastic constants c_{11}, c_{12}, and c_{44}, which give

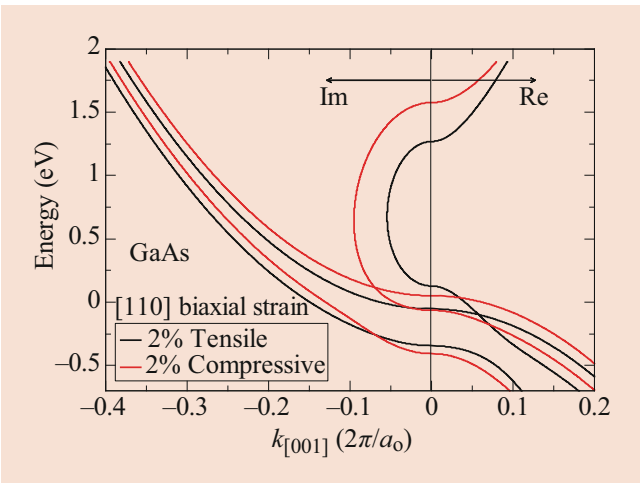

Fig. 41.5 Complex band structures for bulk GaAs along the [001] crystal direction under different [110] biaxial strain conditions. Black curves: tensile strain $\varepsilon = +2\%$. Red curves: compressive strain $\varepsilon = -2\%$

$$
\begin{bmatrix} T_{xx} \\ T_{yy} \\ T_{zz} \\ T_{xy} \\ T_{xz} \\ T_{yz} \end{bmatrix}
=
\begin{bmatrix}
c_{11} & c_{12} & c_{12} & 0 & 0 & 0 \\
c_{12} & c_{11} & c_{12} & 0 & 0 & 0 \\
c_{12} & c_{12} & c_{11} & 0 & 0 & 0 \\
0 & 0 & 0 & c_{44} & 0 & 0 \\
0 & 0 & 0 & 0 & c_{44} & 0 \\
0 & 0 & 0 & 0 & 0 & c_{44}
\end{bmatrix}
\begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{xy} \\ \varepsilon_{xz} \\ \varepsilon_{yz} \end{bmatrix}
\,. \tag{41.21}
$$

Such elastic constants are tabulated in material databases. The result is that the only nonzero components of the strain tensor are $\varepsilon_{xx} = \varepsilon_{yy} \equiv \varepsilon = T\,c_{11}/(c_{11}^2 + c_{12}c_{11} - 2c_{12}^2)$ and $\varepsilon_{zz} = -2\,c_{12}/c_{11}\,\varepsilon$. Figure 41.5 reports the results for $\varepsilon = +2\%$ (tensile strain) and $\varepsilon = -2\%$ (compressive strain).

It is seen that strain has important implications on the gap energy and on the effective masses. Besides, the imaginary branches are particularly important for the modeling of band-to-band tunneling. To this end, it should be noticed that, due to *lh*- and *hh*-band splitting, the imaginary branch connecting the valence and the conduction bands is not always the one (compressive case) that is responsible for gap energy.

41.2.3 Confined Structures

The energy dispersion relationships in confined structures can be easily obtained with the $\boldsymbol{k} \cdot \boldsymbol{p}$ approach by solving Schrödinger equation with $\boldsymbol{k}$ in the Hamiltonian described in the previous sections being replaced with the differential operator $-i\,\nabla$ and then using a finite difference discretization scheme.

The effect of quantization is manifold. First of all it increases the effective energy gap and changes the density-of-states according to the dimensionality of the carrier gas. In addition, quantization changes the imaginary branches of the dispersion relationship inside the gap. The effect of quantization on the energy dispersion in the gap of III–V materials was analyzed using the $\boldsymbol{k} \cdot \boldsymbol{p}$ method by [20]. Investigations on the band structures of quantum wells (2D gas) and nanowires (1D gas) with and without the effect of strain were reported in [21, 22] and [23].

In the following, the results of $\boldsymbol{k} \cdot \boldsymbol{p}$ calculations of an InAs nanowire with and without strain are reported with the aim of giving a description of the main features of the band structure. To this purpose, a square InAs nanowire with [100] transport orientation and 5 nm sides along the [010] and [001] directions is considered. The most interesting strain conditions are biaxial stress within the nanowire cross section, which can be obtained during the growing process, and uniaxial stress along the transport direction, which can be controlled via SiN offset spacers. Figure 41.6 reports the calculated energy dispersion relationships for the aforementioned strain conditions for both the tensile and compressive cases [23].

For each case, the nonzero components of the stress tensor are explicitly indicated in the figure caption, (y, z) being the

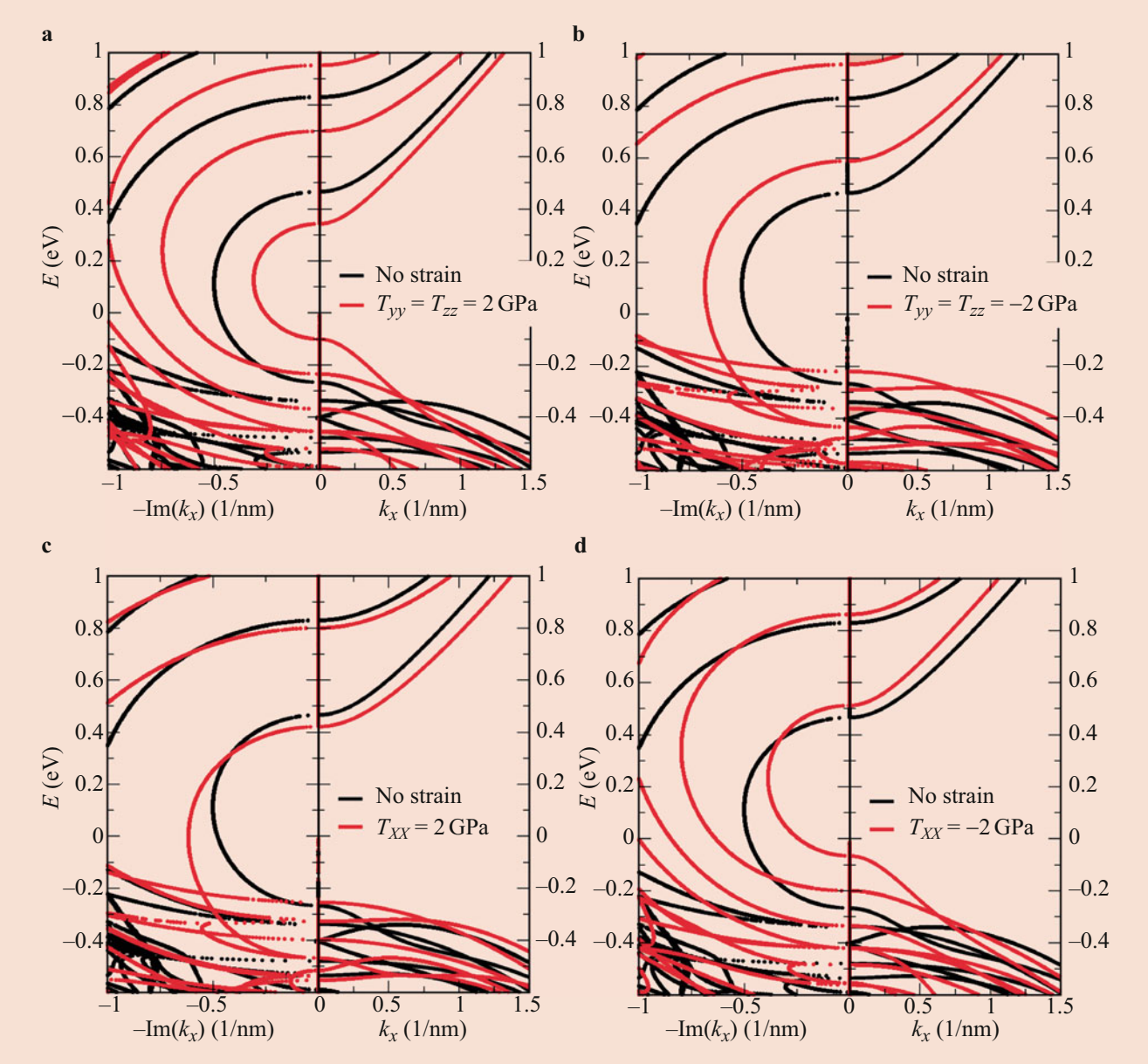

Fig. 41.6 Energy dispersion for a $5 \times 5\,\text{nm}^2$ InAs nanowire: (**a**) biaxial tensile $T_{yy} = T_{zz} = 2\,\text{GPa}$; (**b**) biaxial compressive $T_{yy} = T_{zz} = -2\,\text{GPa}$; (**c**) uniaxial tensile $T_{xx} = 2\,\text{GPa}$; (**d**) uniaxial compressive $T_{xx} = -2\,\text{GPa}$

cross-section plane and x the longitudinal direction of the nanowire. The strain tensor is then calculated with (41.21). By comparing the band structures in Fig. 41.6, we can observe the effects of the different strain conditions on bandgap and density-of-states. Starting from the tensile biaxial stress, significant changes are observed for the valence and conduction subbands, giving rise to a large reduction of the bandgap and of the imaginary wave vector in the gap. On the contrary, by applying a compressive biaxial stress, the opposite shifts of the valence and conduction bands are found, leading also to the fact that the lowest conduction subband is not connected to the highest valence subband by an imaginary branch. This leads to an effective bandgap, which is relevant for the band-to-band tunneling process, that is, ≈0.2 eV larger than the density-of-states (DOS) bandgap. The effect is very similar to the one shown in Fig. 41.5 for bulk GaAs and biaxial compressive stress. The values of both the effective and DOS bandgaps are reported in Table 41.1.

Such kind of condition plays a key role in nanoscale devices based on band-to-band tunneling, as it causes a reduction of the tunneling probability, which is determined by the imaginary branch of the $E(k)$ and not by the DOS bandgap.

Table 41.1 InAs NW bandgap, "effective" bandgap, and electron/hole effective mass of the first conduction/valence subband for the unstrained, biaxial, and uniaxial stress conditions as in Fig. 41.6. The effective masses are evaluated from the real branches of the $E(k)$ shown in Fig. 41.6

	E_G (eV)	"effective" E_G (eV)	m_e (m_0)	m_h (m_0)
Unstrained	0.735	–	0.057	0.057
Biax. tens.	0.45 (−39%)	–	0.036 (−37%)	0.033 (−42%)
Biax. comp.	0.81 (+10%)	1.0 (+25.5%)	0.077 (+35%)	0.33 (+226%)
Uniax. tens.	0.67 (−8%)	0.88 (+31%)	0.072 (+26%)	0.33 (+226%)
Uniax. comp.	0.58 (−21%)	–	0.043 (−24.5%)	0.039 (−31%)

Table 41.2 GaSb NW bandgap and electron/hole effective mass of the first conduction/valence subband for the unstrained, biaxial, and uniaxial stress conditions. The effective masses are evaluated from the real branches of the dispersion relations $E(k)$

	E_G (eV)	m_e [m_0]	m_h [m_0]
$5\times5\,nm^2$ GaSb NW − stress = 2 GPa			
Unstrained	1.18	0.068	0.13
Biax. tens.	0.86 (−28%)	0.05 (−26%)	0.07 (−46%)
Biax. comp.	1.29 (+9%)	0.084 (+23.5%)	0.25 (+97%)
Uniax. tens.	1.08 (−8%)	0.079 (+16%)	0.25 (+97%)
Uniax. comp.	1.06 (−11%)	0.058 (−15%)	0.08 (−38%)

Similar considerations apply for the uniaxial tensile and compressive strain conditions. In the tensile case, the same branch crossing already seen for biaxial compressive strain occurs. This is clearly confirmed by the bandgap values reported in Table 41.1.

The electron and hole effective masses of the InAs nanowire evaluated from the curvatures of the real branches defining the DOS bandgaps are also reported in Table 41.1. As expected, the density-of-states is significantly affected by the applied strain, leading to relative changes larger than 24% in all configurations. Moreover, due to the crossing of the valence subbands induced by biaxial compressive and uniaxial tensile strain, an increase as high as +226% of the hole effective masses is experienced.

It is worth noting that a similar effect takes place also for other materials (e.g., GaSb) and also for thin body structures (quantum wells) and is independent of the device cross section [24]. The results of similar calculations carried out for GaSb nanowires for the same stress conditions are reported in Table 41.2 and show very similar trends to those reported in Table 41.1 for InAs.

41.3 The k · p Method Applied to Tunnel Field-Effect Transistors

Tunnel FETs (TFETs) are among the potential disruptive solutions to overcome the conventional CMOS limitations in power consumption control, as they provide a very steep subthreshold slope (SS) and a reduced random dopant-induced variability, thanks to the use of intrinsic channels. Moreover, they provide an ample design flexibility, allowing for both horizontal and vertical implementations with double-gate (DG) and gate-all-around (GAA) configurations to suppress short channel effects (SCEs) and enhance device scalability [25,26]. Unlike conventional MOSFETs, which work by raising or lowering an energy barrier to control the current flow, TFETs keep this energy barrier high. The device switches on and off by altering the likelihood for electrons on one side of that barrier to tunnel to the other side, the barrier being the energy bandgap. The basic operation of such devices is reported in Chap. ▶ 24, while different device architectures based on new technologies, more specifically on III–V GAA nanowire structures, are detailed in Chaps. ▶ 6 and ▶ 9.

Current challenges to mainstream introduction of the TFET technology include the difficulty to achieve sufficiently high ON-currents (I_{ON}), to suppress the ambipolar effects affecting the off-state performance, and to deal with the superlinear onset and the unconventional saturation voltage of the output characteristics [27,28].

In this section, two different types of TFET devices are considered: (i) homojunction nanowires and (ii) heterojunction nanowires. Homojunction n-channel TFETs are investigated first, based on InAs, by assuming p-type/n-type doping in the source/drain regions, respectively, and an intrinsic channel. Next, heterostructure n-channel TFETs are considered as they have the potential to achieve larger I_{ON} levels, as reported in promising experimental studies on III–V compounds [29].

As far as charge transport is concerned, a quantum ballistic model is adopted in all cases, using the four-band or the eight-band $\boldsymbol{k}\cdot\boldsymbol{p}$ Hamiltonian, as indicated in Sect. 41.2, combined with the NEGF formalism [30] to cope with full 3D quantum transport. Details on the NEGF model can be found in Chap. ▶ 44. The NEGF module is self-consistently coupled with a 3D Poisson solver. The adopted software was validated against atomistic TB calculations [31], and a nice agreement between the two simulation approaches was reported in [32], boosting confidence in the predictive capabilities of the $\boldsymbol{k}\cdot\boldsymbol{p}$ framework.

41.3.1 Device Structures

Homojunction and heterojunction devices have a similar structure. The schematic view of the heterojunction device is

reported in Fig. 41.7 [33]. The homojunction device geometry is identical, with InAs being the only semiconducting material. A careful optimization of the device geometry, doping levels, and gate stack is required to optimize the overall TFET performance in both the homojunction and heterojunction cases.

A squared cross section of thickness $T_{side} = 5\,nm$ is assumed for both devices. The length of the source region is $L_S = 20\,nm$, the gate length is $L_G = 17\,nm$, and the drain-region length is $L_D = 40\,nm$ [33]. The source doping is assumed uniform and fixed to $N_A = 5 \times 10^{19}\ cm^{-3}$, the channel is intrinsic, and the drain doping is uniform and fixed to $N_D = 10^{19}\ cm^{-3}$. An abrupt doping variation is considered at the source/channel junction, consistently with a vertical fabrication process [34, 35]. It is worth pointing out that a gradual doping profile would have a strong impact on the tunneling probability and thus on the TFET performance. The drain doping is lower than the source doping to limit ambipolar effects. Therefore, a longer drain region is required to ensure charge neutrality at the drain contact. As far as the gate stack is concerned, the thickness of the gate oxide is fixed to $T_{ox} = 1\,nm$ of SiO_2 [33]. It is worth noting here that TFETs are less sensitive to fringing-field effects of the gate capacitance as compared with conventional field-effect transistors.

In the following analysis, the nanowire transport direction is [100], consistent with the assumptions made in the previous section for the band structure calculations under different stress conditions. However, recent studies of the energy dispersion curves carried out with the $\boldsymbol{k} \cdot \boldsymbol{p}$ method have shown that the real and imaginary branches have a similar behavior also when [110] and [111] transport orientations are assumed [36].

41.3.2 Impact of Strain on the Tunneling Current of Homojunction TFETs

In Fig. 41.8, the I–V curves for the $5 \times 5\,nm^2$ homojunction InAs nanowire TFET are reported for different stress conditions [23]. As indicated in the figure caption, the current is normalized to the nanowire side and all simulations are carried out at $V_{DS} = 0.3\,V$. By comparing the turn-on characteristics, the significant impact of stress can be appreciated, leading to changes in the leakage current in a range of almost 12 orders of magnitude, a shift of the threshold voltage V_T of about 0.5 V along with a substantial change in the subthreshold slope SS, and a variation of the ON-current in the 1–1000 μA/μm range.

A clear correlation can be inferred between leakage current and bandgap narrowing induced by stress (Table 41.1): the lower the bandgap, the larger the leakage current. From a physical standpoint, the leakage current is due to the ambipolarity of the device, i.e., to band-to-band tunneling occurring at the drain junction at low V_{GS}. The V_T as well as the SS variations follow the bandgap changes. The significant reduction of SS observed for the biaxial tensile and uniaxial compressive cases is mostly ascribed to the higher degeneracy caused by the effective-mass decrease, as reported in Table 41.1.

The role of the "effective" bandgap needs to be accounted for in order to fully explain the current reduction experienced in the uniaxial tensile case. To this purpose, Fig. 41.9 reports the current spectra (i.e., the current densities vs. energy) and the subband profiles for the uniaxial compressive (a) and uniaxial tensile (b) cases [23]. Different V_{GS} have been applied in the two cases to have almost the same conduction

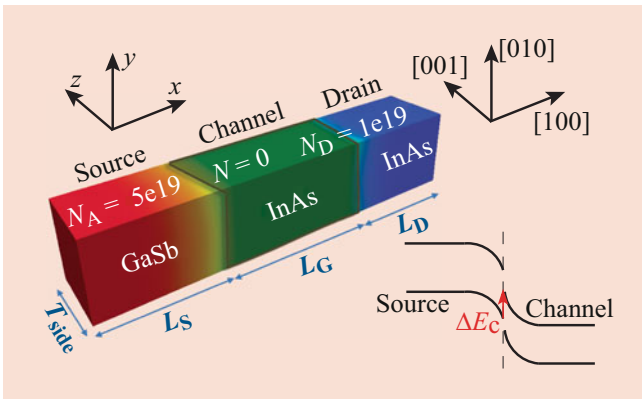

Fig. 41.7 Schematic view of the TFET device realized with a GaSb/InAs heterostructure. ΔE_C is defined as the energy difference between the channel conduction band edge and the source valence band edge at the heterojunction

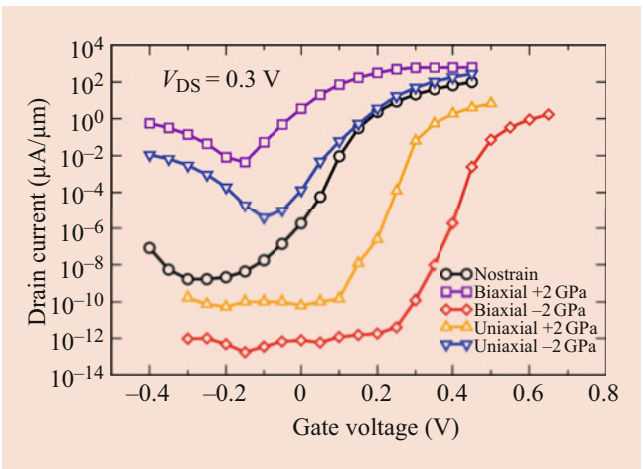

Fig. 41.8 I_{DS} versus V_{GS} curves at $V_{DS} = 0.3\,V$ for the InAs homojunction device with different strain types. The current is normalized with respect to the nanowire side. There are two unfavorable strain configurations which give a small I_{ON} and an unusual behavior: uniaxial tensile and biaxial compressive strain

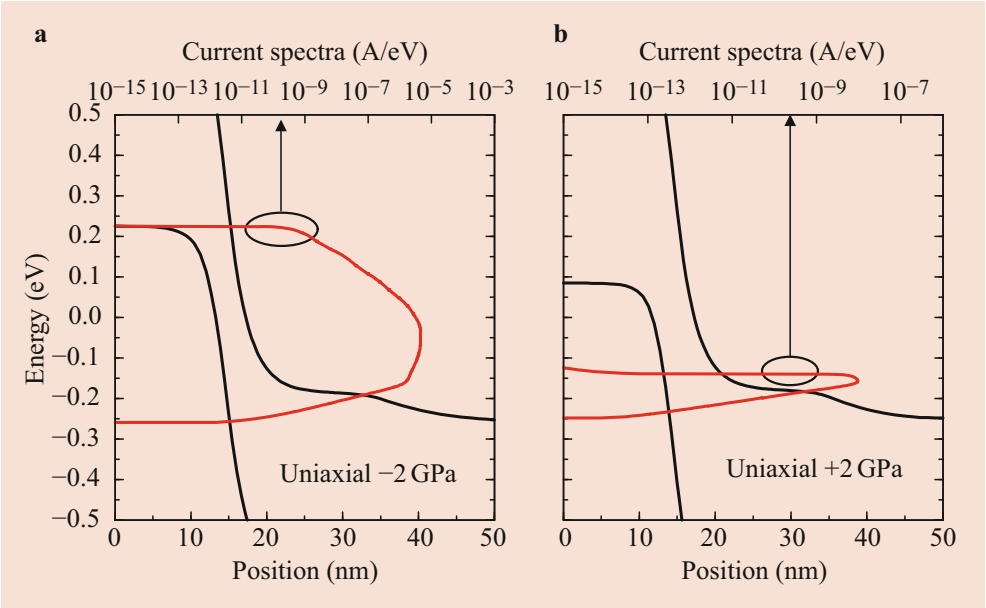

Fig. 41.9 Subband profile vs. position and current spectrum vs. energy for the InAs homojunction, for uniaxial compressive (**a**) and uniaxial tensile strain (**b**). Two different V_{GS} values have been chosen to have the conduction band edges almost aligned within the channel. For the uniaxial compressive case, the current flows at all energies for which there are available states both in the source and in the channel. In the uniaxial tensile case, the current is negligible up to 0.2 eV below the first valence subband in the source

band-edge level within the channel. The plot illustrates the change in the degeneracy level within the source. Moreover, in the compressive case, tunneling occurs in an energy window ranging from the top of the valence band in the source to the bottom of the conduction band in the channel, while in the tensile case, tunneling occurs in a limited energy window, ranging from about 0.2 eV below the valence band in the source to the bottom of the conduction band in the channel. This corresponds to the effective bandgap shown in Fig. 41.6c. The transport results confirm that the effective bandgap gives rise to an unexpected significant reduction of the ON-current.

In order to compare the subthreshold trend of the different curves, the metal gate work function has been adjusted for each stress case to fix the OFF-current $I_{OFF} = 1\,\text{nA}/\mu\text{m}$ at $V_{GS} = 0\,\text{V}$, following the specification of the ITRS Low Operation Power (LOP) application [37]. The resulting curves are compared in Fig. 41.10, showing a substantial SS degradation at low V_{GS} for the stress cases with higher ON-current, which provide the best overall trade-off.

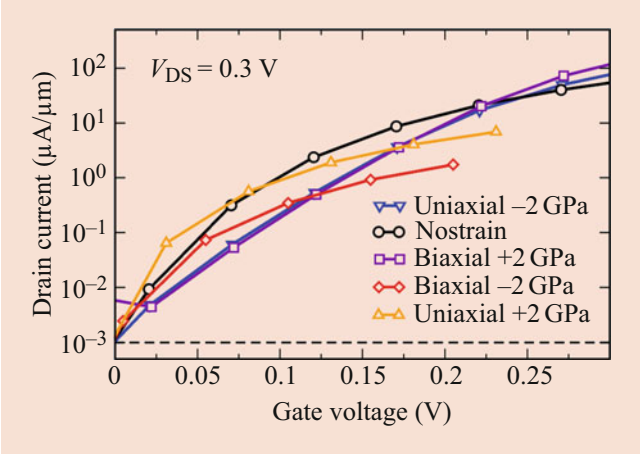

Fig. 41.10 I_{DS} vs. V_{GS} curves at $V_{DS} = 0.3$ V for the InAs homojunction device with different strain types. The current is normalized with respect to the nanowire side. The metal gate work function has been adjusted for each case to have $I_{OFF} = 1\,\text{nA}/\mu\text{m}$ at $V_{GS} = 0\,\text{V}$

41.3.3 Impact of Strain on the Tunneling Current of Heterojunction TFETs

In Fig. 41.7, a GaSb/InAs heterostructure at the source/channel interface is assumed. The corresponding band-edge profiles are plotted in the inset, showing how the heterojunction alignment between the channel conduction-band and the source valence-band edges ΔE_C can affect the tunneling probability. Compared to the homojunction devices reported in the previous subsection, this additional parameter can be used for band engineering as it is strictly related to the band-to-band tunneling at the source/channel junction. In analogy with the homojunction structures, the TFET performance is strongly influenced by structure confinement and applied

strain due to the band structure modifications explained in Sects. 41.2.2 and 41.2.3. More specifically, a GaSb/InAs nanowire with $T_{side} = 5$ nm shows a ΔE_C of 0.24 eV in the unstrained case, which decreases to −0.005 eV and 0.163 eV for the biaxial tensile and uniaxial compressive cases, respectively. A negative ΔE_C means a broken-gap heterojunction rather than a staggered one.

Even if heterojunctions feature an improved ON-current due to the band-structure engineering at the source/channel interface, further improvements are expected with strain similarly to the homojunction-based nanowires. Figure 41.11 compares the I–V curves of a 5×5 nm^2 GaSb/InAs heterojunction NW TFET for different stress conditions [33]. The reported current curves are normalized to the nanowire side and shifted with respect to V_{GS} in order to have $I_{OFF} = 5$ nA/μm at $V_{GS} = V_{GSoff} \equiv 0$ V and $V_{DS} = V_{DD} = 0.3$ V, as indicated by the specification of the ITRS Low Operation Power (LOP) application [37]. Accordingly, I_{ON} is defined as the current corresponding to $V_{GS} = V_{GSoff} + 0.3$ V and $V_{DS} = V_{DD} = 0.3$ V. The experienced V_T shift is in the range from −0.3 V to +0.4 V as shown in the inset. The main effects of strain on the heterojunction-NW TFETs are in line with those reported for the homojunction TFETs. We can observe a significant V_T reduction for the biaxial tensile case as well as an increase in I_{ON} but also a subthreshold slope degradation. The biaxial tensile and uniaxial compressive cases again provide the best trade-off between I_{ON} and SS, but with an advantageous increase of I_{ON} given by the heterostructure. The extracted values of I_{ON} for the latter stress cases are reported in Table 41.3 along with the average SS, calculated over three current decades, and the peak SS.

Table 41.3 I_{ON}, average subthreshold slope (SS_{avg}) computed over three current decades, and peak slope (SS_{peak}) extracted from the GaSb/InAs NW TFET currents reported in Fig. 41.11 for two stress conditions

5×5 nm^2 GaSb/InAs NW TFET			
	I_{ON}	SS_{avg}	SS_{peak}
	(μA/μm)	(mV/dec)	(mV/dec)
No strain	150.1	30	26
Biax. tens. +2 GPa	245.7	51	45
uniax. comp. −2 GPa	177.1	41	35

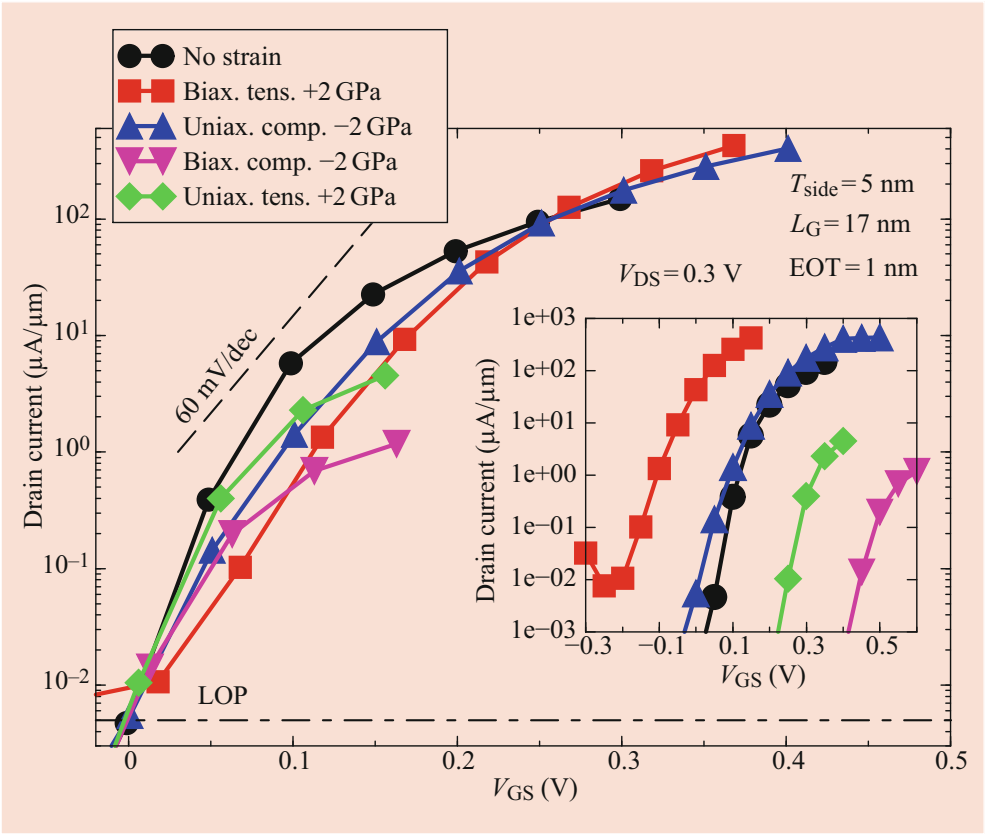

Fig. 41.11 Turn-on characteristics of a 5×5 nm^2 GaSb/InAs NW TFET for different stress conditions. The current is normalized by the device side and is shifted to match the I_{OFF} target of the LOP application (5 nA/μm). $V_{DS} = 0.3$ V. Inset: I–V curves with no gate voltage shift. The biaxial tensile stress increases the on-state current, while the uniaxial compressive stress has a smaller impact on the I–V curve. The uniaxial tensile and biaxial compressive strains produce unfavorable I_{ON} and a large threshold voltage shift

41.3.4 GaSb-/InAs-Based TFET Optimization Exploiting Strain and Device Geometry

A deep investigation on stress effects and on the choice of geometrical parameters in homojunction TFETs has been recently carried out in the literature by extensive use of the $\boldsymbol{k} \cdot \boldsymbol{p}$ method [36, 38, 39]. In [33], a similar systematic study was carried out on GaSb/InAs nanowire TFETs. To this purpose, the subthreshold swing, the ON-current, and the ON-/OFF-current ratio at low supply voltage have been calculated by means of a full 3D NEGF framework based on the eight-band $\boldsymbol{k} \cdot \boldsymbol{p}$ model.

The main outcomes of the latter investigations are briefly reported in the following with the aim of highlighting the potential and scope of the $\boldsymbol{k} \cdot \boldsymbol{p}$ method for the exploitation of novel nanoscale solutions. More specifically, the effects of changing the gate length and cross-section area are analyzed under different stress conditions, clearly showing the major role played by band structure engineering in such kind of devices.

I–V curves of GaSb/InAs TFETs with two different gate lengths are compared in Fig. 41.12 [33]. As in conventional MOSFETs, the increase of L_G in a TFET reduces source-to-drain tunneling, which is the main contribution to the leakage current in subthreshold regime. As a result, a significant improvement in the subthreshold slope is found along with a slight increase in the ON-current. The effect of strain in the TFET with a longer channel is comparable to the one in the short device so that, for the +2-GPa biaxial tensile stress, a 36% increase in I_{ON} and a 47% decrease in the average SS are achieved. The extracted data are reported in Table 41.4. However, it must be pointed out that even if a longer L_G is favorable to the device static performance, the corresponding augmented total gate capacitance and overall occupation area must also be considered in applications.

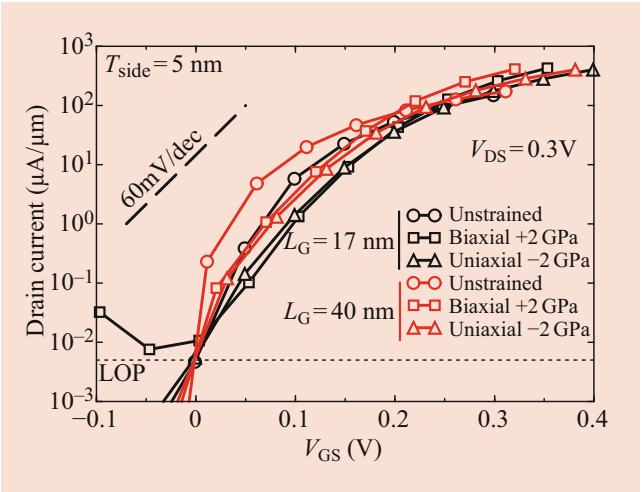

Fig. 41.12 Turn-on characteristics of a 5 × 5 nm^2 GaSb/InAs NW TFET for L_G = 17 and 40 nm for the unstrained, biaxial strain and uniaxial strain conditions. The current is normalized to the cross-section side, and the curves are shifted to match the target I_{OFF} of the LOP application (5 nA/μm). V_{DS} = 0.3 V. The L_G increase from 17 nm to 40 nm provides a decrease in leakage current and a slope improvement. For the biaxial tensile stress condition, a 36% increase in I_{ON} can be achieved

The *I–V* curves of GaSb/InAs TFETs with different cross-section sizes in unstrained conditions are reported in Fig. 41.13 [33]. The large differences between the curves can be explained by considering that the bandgap and the electron and hole effective masses are significantly influenced by the cross-section area, as illustrated for the 10 × 10 nm^2 InAs and GaSb nanowires by the data in Table 41.5, which must be compared with the corresponding data for 5 × 5 nm^2 nanowires in Tables 41.1 and 41.2. Besides, also ΔE_C at the source-channel interface depends on the cross-section size, due to the different quantization properties of the two materials (see, e.g., the different bandgaps reported for the two materials in Table 41.5). For a cross section of 10 × 10 nm^2, ΔE_C becomes 0.048 eV in the unstrained case, which is −80% of the 5 × 5 nm^2 nanowire.

Table 41.5 reports also the data for the same strain conditions discussed in the previous subsections, namely, biaxial tensile and uniaxial compressive, but with two different stress intensities, i.e., 1-GPa and 2-GPa. The 2-GPa results can be directly compared with the 5 × 5 nm^2 case and clearly show a huge reduction in the bandgap. As a significant ambipolarity is expected for such low bandgaps, the strain intensity of 1 GPa can be preferable to mitigate the effect. Besides, the drain region can be optimized [33] by using a nonuniform drain doping with a 20-nm-long region abutting the channel with $N_D = 10^{18}$ cm^{-3} and a 20 nm region with graded doping up to $N_D = 10^{19}$ cm^{-3} next to the drain contact.

The *I–V* curves of GaSb/InAs TFETs with different cross-section sizes under strain conditions are reported in Fig. 41.14 [33]. As expected, a significant increase in the current is observed when a 1-GPa biaxial tensile stress is applied in the larger nanowires. This is mostly due to a further decrease of ΔE_C at the source-channel interface,

Table 41.4 I_{ON}, average subthreshold slope (SS_{avg}) computed over three current decades, and peak slope (SS_{peak}) extracted from the GaSb/InAs NW TFET currents with L_G = 40 nm reported in Fig. 41.12 for various stress conditions

5×5 nm^2 GaSb/InAs NW TFET with L_G = 40 nm			
	I_{ON} (μA/μm)	SS_{avg} (mV/dec)	SS_{peak} (mV/dec)
No strain	161.3	15	8
Biax. tens. +2 GPa	334.9	27	18
Uniax. comp. −2 GPa	212.7	31	23

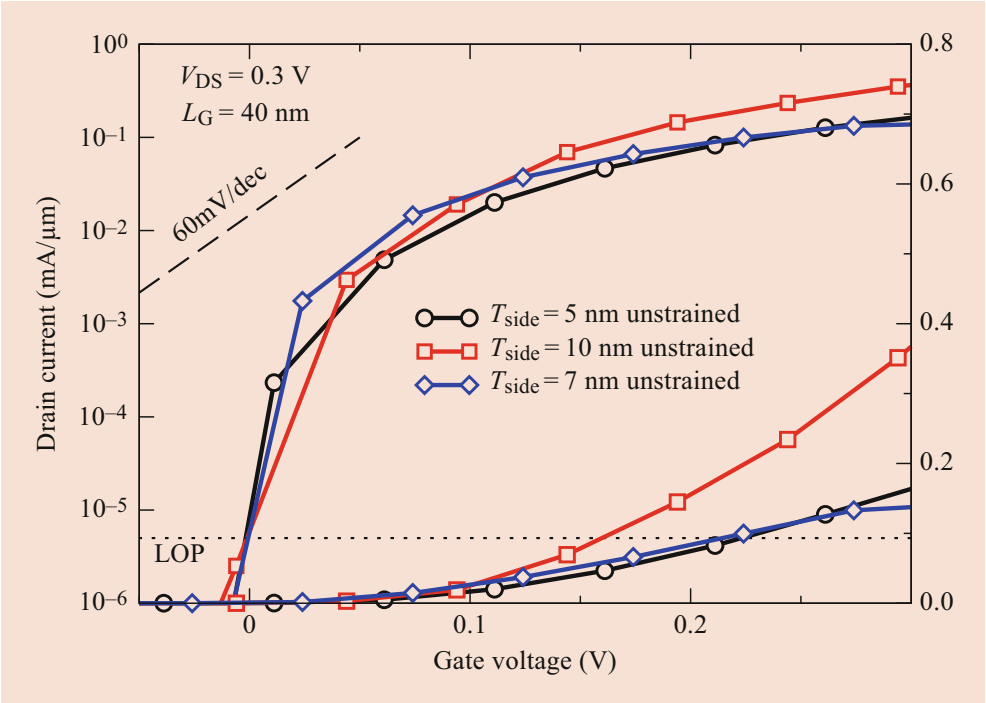

Fig. 41.13 Turn-on characteristics of a 5×5, 7×7 and $10 \times 10\,\text{nm}^2$ GaSb/InAs NW TFET without strain. $L_G = 40\,\text{nm}$, $V_{DD} = 0.3\,\text{V}$. $I_{OFF} = 5\,\text{nA}/\mu\text{m}$ (LOP)

Table 41.5 Energy bandgaps and electron (hole) effective masses in the first conduction (valence) subband for $10 \times 10\,\text{nm}^2$ InAs and GaSb NWs for the unstrained, biaxial tensile, and uniaxial compressive cases. Two stress values are considered, namely, 1 GPa and 2 GPa. The effective masses are evaluated from the real branch of $E(k)$

	E_G (eV)	m_e (m_0)	m_h (m_0)
$10 \times 10\,\text{nm}^2$ InAs NW			
Unstrained	0.49	0.037	0.04
Bi. tens. 1 GPa	0.35 (−28%)	0.03 (−28%)	0.03 (−30%)
Uni. comp. 1 GPa	0.4 (−15%)	0.03 (−20%)	0.03 (−30%)
Bi. tens. 2 GPa	0.2 (−58%)	0.016 (−57%)	0.015 (−63.5%)
Uni. comp. 2 GPa	0.3 (−38%)	0.024 (−35%)	0.02 (−50%)
$10 \times 10\,\text{nm}^2$ GaSb NW			
Unstrained	0.879	0.046	0.085
Bi. tens. 1 GPa	0.7 (−18%)	0.04 (−17%)	0.052 (−39%)
Uni. comp. 1 GPa	0.83 (−6%)	0.04 (−9%)	0.058 (−31%)
Bi. tens. 2 GPa	0.54 (−38%)	0.03 (−35%)	0.033 (−61%)
Uni. comp. 2 GPa	0.78 (−10%)	0.038 (−17%)	0.043 (−49%)

which for the $10 \times 10\,\text{nm}^2$ NW becomes $-0.093\,\text{eV}$ for 1-GPa biaxial tensile stress. The intermediate $7 \times 7\,\text{nm}^2$ TFET with 1-GPa biaxial tensile stress is able to fulfill the I_{OFF} requirement with $I_{ON} = 0.4\,\text{mA}/\mu\text{m}$. Table 41.6 collects the most significant extracted parameters.

41.4 TFET Inverters for a Complementary Technology Platform

The need of a complementary logic requires to investigate the complementary p-channel TFET in addition to the n-channel TFET already discussed. The investigations on n-channel TFETs clearly showed that heterostructures featuring broken or staggered band lineups are the most promising candidates [31]. Experimental and numerical investigations, like, e.g., those discussed in [29, 33, 40] and in the previous section, suggest that the GaSb/InAs heterojunction is most attractive for n-type devices. On the contrary, a different couple of III–V materials gained some interest for the realization of p-TFETs, namely, the InAs/AlGaSb one, which was proposed in [41] by exploring the possibility to achieve either staggered or broken gap alignments by varying the Al mole fraction in the channel.

In this section, simulation results of complementary heterojunction nanowire TFETs are reported based on the same InAs/AlGaSb heterostructure platform. The simulation framework is based on the four-band $\boldsymbol{k} \cdot \boldsymbol{p}$ model [42]. The schematic representation of the two devices is shown in Fig. 41.15 for the specifically chosen InAs/$Al_{0.05}Ga_{0.95}Sb$ couple [42]. A gate-all-around architecture is assumed. The gate, not shown in the figure, is self-aligned to the intrin-

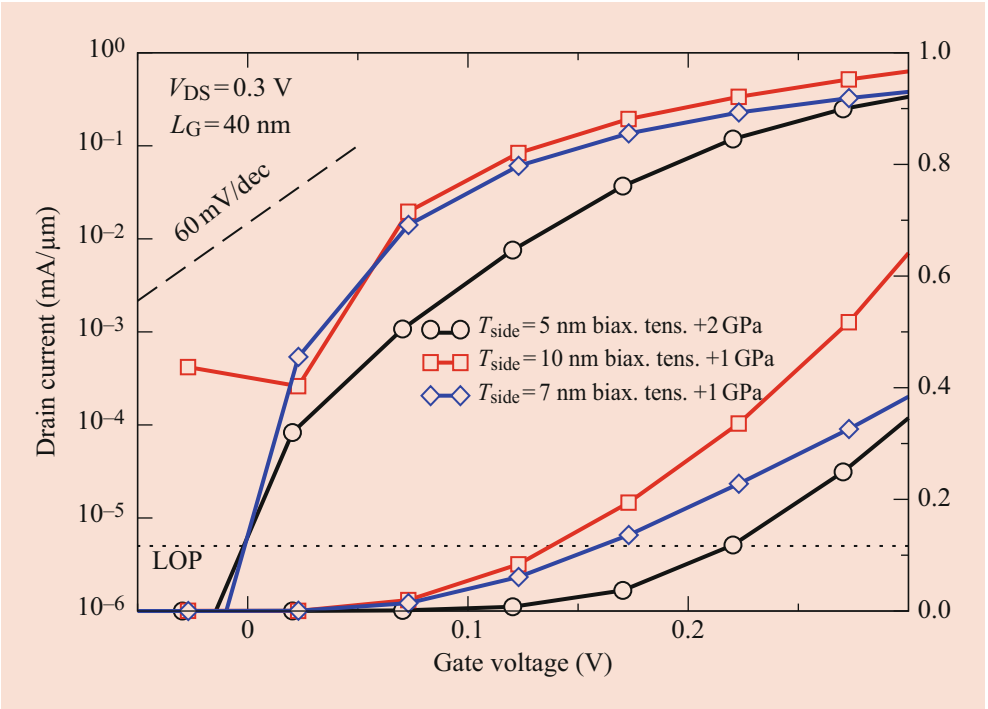

Fig. 41.14 Turn-on characteristics of a 5 × 5, 7 × 7 and 10 × 10 nm^2 GaSb/InAs NW TFET for different stress conditions. L_G = 40 nm, V_{DD} = 0.3 V. I_{OFF} = 5 nA/μm (LOP)

Table 41.6 I_{ON}, average subthreshold slope (SS_{avg}) computed over three current decades, and peak slope (SS_{peak}) extracted from the GaSb/InAs TFET currents reported in Figs. 41.13 and 41.14

5×5 nm^2 NW			
	I_{ON}	SS_{avg}	SS_{peak}
	(μA/μm)	(mV/dec)	(mV/dec)
No strain	161.3	15	8
Biax. tens. +2 GPa	342	27	18
7×7 nm^2 NW			
	I_{ON}	SS_{avg}	SS_{peak}
	(μA/μm)	(mV/dec)	(mV/dec)
No strain	143.7	19	9.5
Biax. tens. +1 GPa	391	20	12

sic channel. The square cross section of the nanowires is 7 × 7 nm^2 and the source, channel, and drain lengths are fixed to 20 nm. The source of the n-type TFET is made of AlGaSb doped with 5 × 10^{19} cm^{-3} acceptors, the InAs channel is assumed intrinsic, and the InAs drain is doped with a graded doping from 10^{18} to 10^{19} cm^{-3} donors to reduce the ambipolarity effect [42]. The p-channel device is realized with abrupt doping profiles in the source, channel, and drain regions as illustrated in Fig. 41.15.

In contrast with the majority of literature, where typically TCAD tools are used for the simulation of full inverters, the results reported hereafter are based on full quantum NEGF simulations with the four-band $\boldsymbol{k} \cdot \boldsymbol{p}$ model for both n- and p-channel devices.

The turn-on characteristics of the optimum n- and p-type TFETs are reported in Fig. 41.16a [32], showing full compliance with the ITRS requirements of the low operating power (LOP) nodes, with I_{OFF} = 5 nA/μm [37] when V_{DS} = V_{DD} = 0.4 V. The ITRS requirement on the off-state current for the low-standby-power (LSTP) nodes is also indicated in the figure (I_{OFF} = 10 pA/μm). The main features obtained for the n-type (Tn) and p-type (Tp) devices can be extracted from the *I*–*V* curves and are compared in diagrams (b), (c), (d), and (e) of Fig. 41.16. The turn-on characteristics are compared by assuming the same off-state at $V_{GS} - V_{OFF} = 0$. Starting from the subthreshold behavior, both devices exhibit a minimum SS lower than 40 mV/dec, with an average SS lower than 60 mV/dec, having defined the average over a number of current decades of about 3 for both Tn and Tp. The SS values experienced by the InAs/$Al_{0.05}Ga_{0.95}Sb$ nanowires do not compete with the results obtained by the GaSb/InAs TFETs reported in the previous section. Due to this lower performance, a larger V_{DD} has been applied here in order to reach larger on-state currents. The I_{ON} levels are relatively high, especially for the Tn device, which nicely compares with similar n-ch GaSb/InAs TFETs featuring strain effect. The Tp I_{ON} is four times smaller than the Tn one. Such a difference might require a compensation approach when dealing with practical circuits.

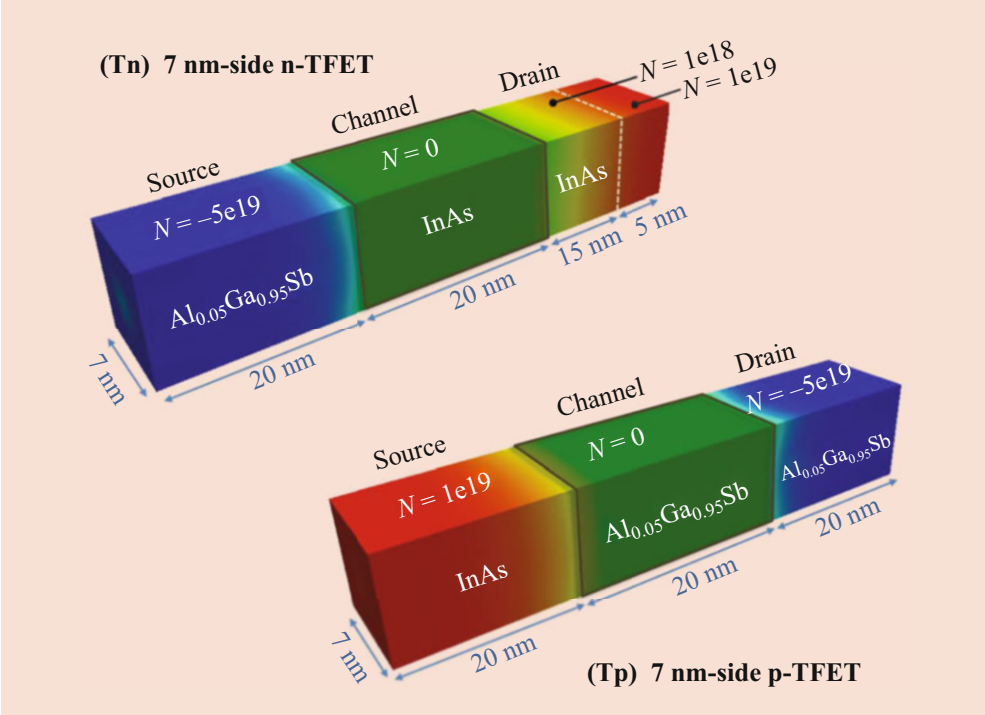

Fig. 41.15 Considered n-type (Tn) and p-type (Tp) heterojunction TFETs based on the same InAs/$Al_{0.05}Ga_{0.95}Sb$ material pair. Doping concentrations are indicated in cm^{-3} and abrupt profiles are assumed. A nonuniform drain doping is used to reduce ambipolarity in Tn. The gate dielectric is Al_2O_3 with an equivalent oxide thickness EOT = 1 nm

The design of a complementary TFET inverter, which can be assumed as the simplest circuit for a fair comparison with the conventional CMOS logic as far as power consumption and time response are concerned, was addressed in [32] by proposing two different solutions. The first one is indicated as *I*1 in Fig. 41.17: it is based on one p-channel and one n-channel transistor without any compensation of the asymmetry discussed above. The second one, called *I*2 in Fig. 41.17, compensates the lower I_{ON} of the p-channel device by using four devices in parallel. In order to normalize the off-state dissipation of both circuits to the same value, the turn-on characteristics of the four p-channel devices in *I*2 have been shifted in order to obtain the same OFF-current as in *I*1. Finally, a two-stage inverter chain is used to estimate the transient performance under self-loading. The main differences observed when comparing the *I*1 and *I*2 configurations are illustrated in the following figures taken from [32]. First of all, the n-TFET and p-TFET output characteristics calculated with the $\boldsymbol{k \cdot p}$ framework for I1 and I2 are shown in Figs. 41.18a and b, respectively, as a function of the inverter output voltage V_o, which corresponds to V_{DS} for the n-channel devices and to $V_{DD} + V_{DS}$ for the p-channel ones, for a number of inverter input voltages V_i, corresponding to V_{GS} for the n-channel devices and to $V_{DD} + V_{GS}$ for the p-channel ones. The voltage transfer characteristics (VTCs) of the two different circuits require to determine the V_o-V_i relationship from the analyzed *I*–*V* curves. To this purpose, the intersections between the *I*–*V* curves illustrated by the black dots in Fig. 41.18 for each input voltage V_i have been extracted and reported in Fig. 41.19a (a nonlinear interpolation is assumed between the *I*–*V* curves when needed). The improvement related to the symmetry of the *I*2 configuration is clearly visible in the corresponding VTC. Similar voltage gain is obtained for both configurations, while a larger current consumption is found for *I*2 due to the larger number of transistors used in the pull-up network (Fig. 41.19b and c, respectively).

The transient responses of the two inverters to an input voltage step have been calculated by considering a load capacitance C_L either equal to a fixed value or assuming a self-loading condition, i.e., a chain of two identical inverters [32]. To this end, the total gate capacitances of Tn and Tp have been calculated as

$$C_g = \frac{Q_{ON} - Q_{OFF}}{V_{DD}} \tag{41.22}$$

where $Q_{ON} - Q_{OFF}$ is the net charge variation inside the device between the on- and the off-states. Such quantities have been obtained by integrating the net charge density derived from the 3D simulations on the full nanowire domain. As shown in Fig. 41.20a, the n- and p-channel devices exhibit similar C_g values. The total input capacitances of the inverters (Fig. 41.20b) clearly show that a significantly larger C_{in} is

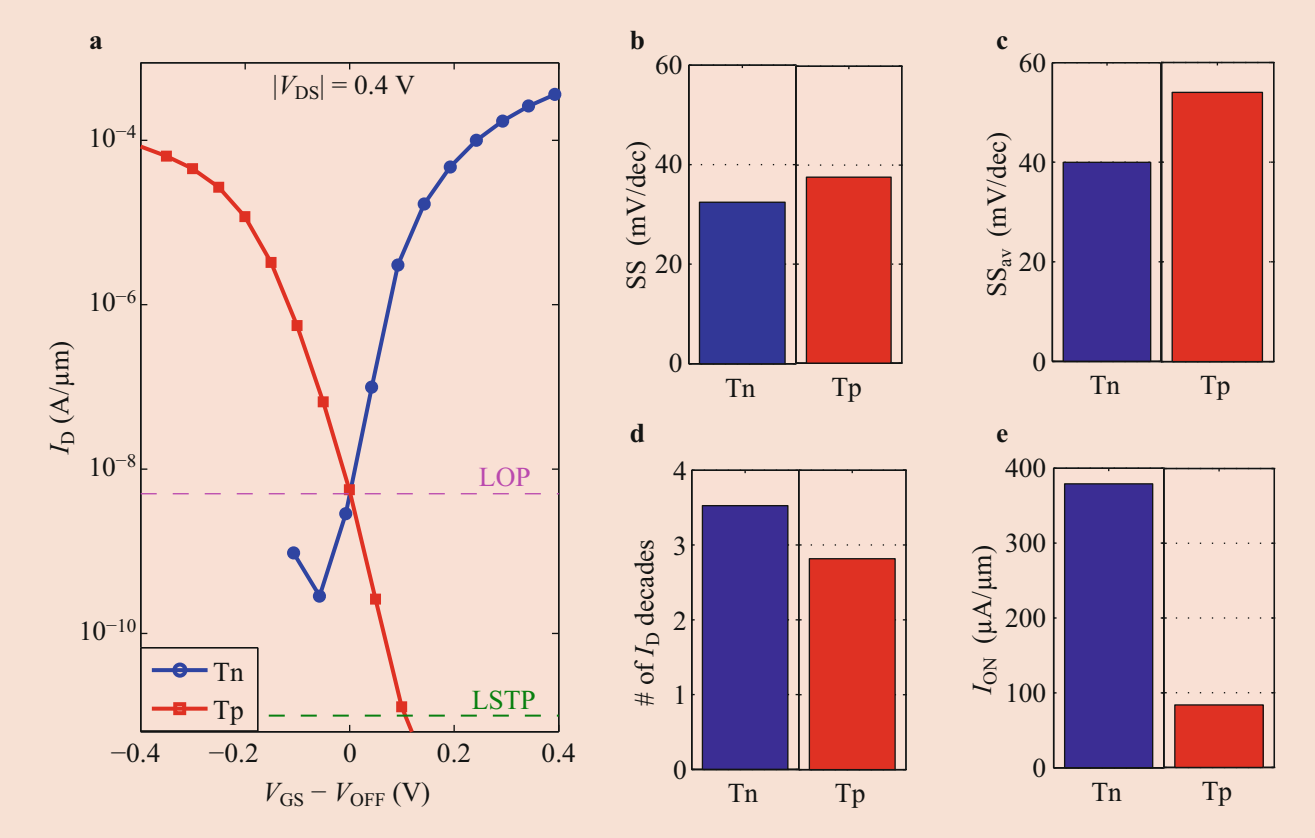

Fig. 41.16 (**a**) Simulated I_D-V_{GS} curves at $|V_{DS}| = 0.4$ V for the TFETs in Fig. 41.15 (normalized by device side for consistency with quantization-induced charge distribution). LSTP (10 pA/μm) and LOP (5 nA/μm) specs on I_{OFF} are indicated. Curves are shifted by the respective V_{OFF}, i.e., the V_{GS} at which $I_D = 5$ nA/μm ($=I_{OFF,LOP}$). Corresponding device performance is evaluated in terms of (**b**) minimum SS, (**c**) average subthreshold slope, SS_{av}, (**d**) number of current decades over which SS_{av} is computed, and (**e**) I_{ON} at $V_{DD} = 0.4$ V

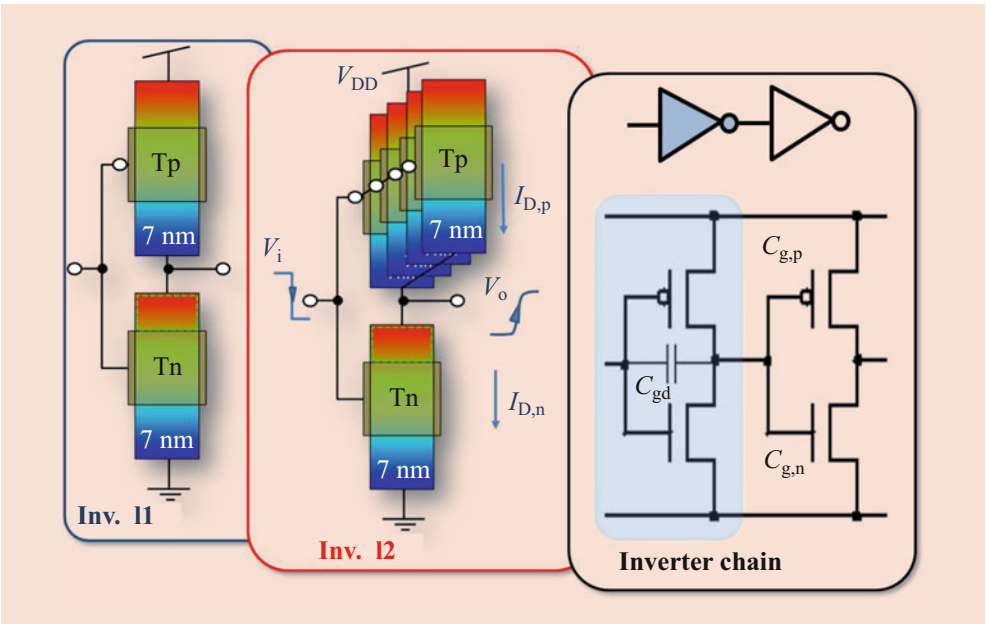

Fig. 41.17 Inverter designs I1 (Tn + Tp) and I2 (Tn + four Tp instances with modified WF), with indication of the switching behavior. A two-stage inverter chain is shown on the right, which is used for transient performance estimation under self-loading. The schematic illustrates device input capacitances $C_{g,n}$ and $C_{g,p}$ as well as the gate-drain capacitance C_{gd}, which is responsible for Miller effects

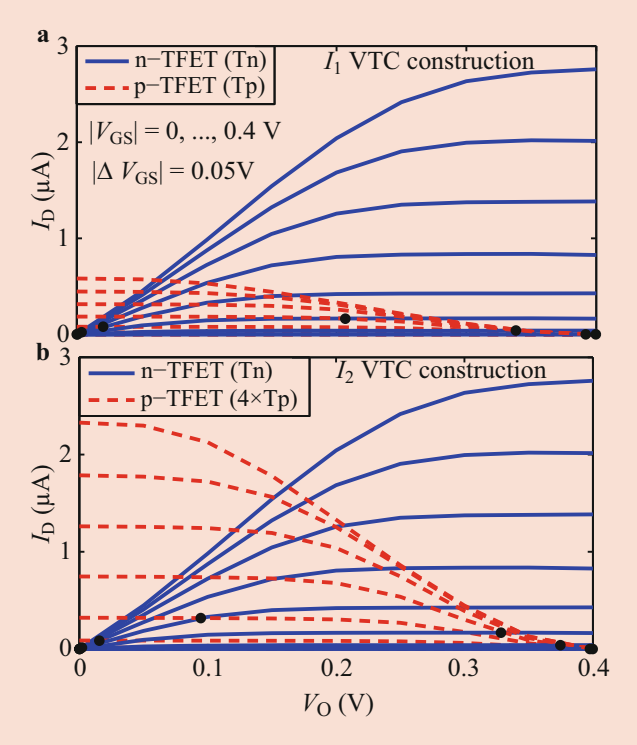

Fig. 41.18 Simulated I_D-V_{DS} families in 0.05 V V_{GS} steps for Tn and Tp. Additional curves at intermediate V_{GS} values are obtained through nonlinear interpolation between these characteristics. Curves are combined exploiting $V_o = V_{DS,n} = V_{DD} + V_{DS,p}$ (see Fig. 41.17) to compute VTCs in Fig. 41.19a for inverters I1 (**a**) and I2 (**b**)

given by the *I*2 inverter, which is clearly due to the presence of four Tp transistors in the pull-up block. In the self-loading case, the Miller effect has been approximately accounted for by adding to C_L a capacitance equal to $2 \times C_{gd}$, the gate-to-drain capacitance C_{gd} being calculated by using the estimation given by [43], with $C_{gd} \approx 0.8 \times C_g$. The rise and fall times $t_{r,f}$ of each inverter in response to an input voltage step are then computed by integrating the output currents obtained from Fig. 41.18 in the interval between 10% and 90% of V_{DD}:

$$t_{r,f} = C_L \int_{0.1V_{DD}}^{0.9V_{DD}} \frac{dV_o}{|I_{D,p}(V_o) - I_{D,n}(V_o)|} \tag{41.23}$$

The rise and fall times relative to the self-loading condition are reported in Fig. 41.21a for inverters *I*1 and *I*2, showing a fairly balanced response for *I*2, which is faster than *I*1. On the contrary, if a fixed C_L is assumed, the same fall time is determined for both inverters, while a factor of about 4 in the rise time is evinced between the two inverters, due to the different pull-up networks (Fig. 41.21b).

As a final outcome of the proposed investigation, in [42] the performance of the considered inverters has been compared with best-case predictions for aggressively scaled CMOS logic based on multi-gate architectures. The comparison was conducted for equal static power consumption, exploiting predictive technology models (PTM-MG) for CMOS simulation [44], and allows identifying favorable V_{DD} windows where TFET has the potential to outperform the traditional technology.

41.5 Modelling of Interface Traps in the k · p Scenario

Trap states located at the semiconductor/insulator interfaces may have a significant impact on the current of III–V TFETs, degrading I_{ON} and SS [45, 46]. In this respect, the achievement of low interface and border trap densities is one of the major technological challenges to be addressed [45, 47].

The combined effects of traps and strain on nanowire TFET characteristics have been investigated in the framework of the $\boldsymbol{k} \cdot \boldsymbol{p}$ approach in [40, 48]. Both acceptor and donor traps can be considered at the semiconductor/oxide interfaces. The trap occupation probability is calculated through a generalization of the Shockley-Read-Hall (SRH) theory consistent with the quantum ballistic NEGF approach and fully accounting for carrier degeneracy. The mathematical framework was first presented in [48] and then extended in [40]. In essence, the occupation probability of traps at energy E_t in steady state is determined from the balance of electrons and holes emission and capture processes. Only the electrostatic effect of traps is considered via Poisson's equation, while transport is still considered ballistic. The end result is that the densities per unit energy and area of electrons and holes trapped inside interface centers at energy E_t and position x are given by

$$n_t(E_t, x) = P_t(E_t, x) D_{it}^{(A)}(E_t, x) \tag{41.24a}$$

$$p_t(E_t, x) = [1 - P_t(E_t, x)] D_{it}^{(D)}(E_t, x) \tag{41.24b}$$

where $D_{it}^{(A)}$ and $D_{it}^{(D)}$ are the acceptor and donor trap densities per unit energy and area at energy E_t and position x and the trap occupation probability $P_t(E_t, x)$ can be approximated in the case of one type of dominant carriers as

$$P_t(E_t, x) \simeq \frac{n(x)}{n(x) + n_1(x)} \quad \text{(electronsmajoritycarriers)}$$

$$P_t(E_t, x) \simeq \frac{p_1(x)}{p(x) + p_1(x)} \quad \text{(holesmajoritycarriers)} \tag{41.25}$$

In (41.25) $n(x)$ and $p(x)$ are the total free electron, and hole densities at x and $n_1(x)$, $p_1(x)$ are given by

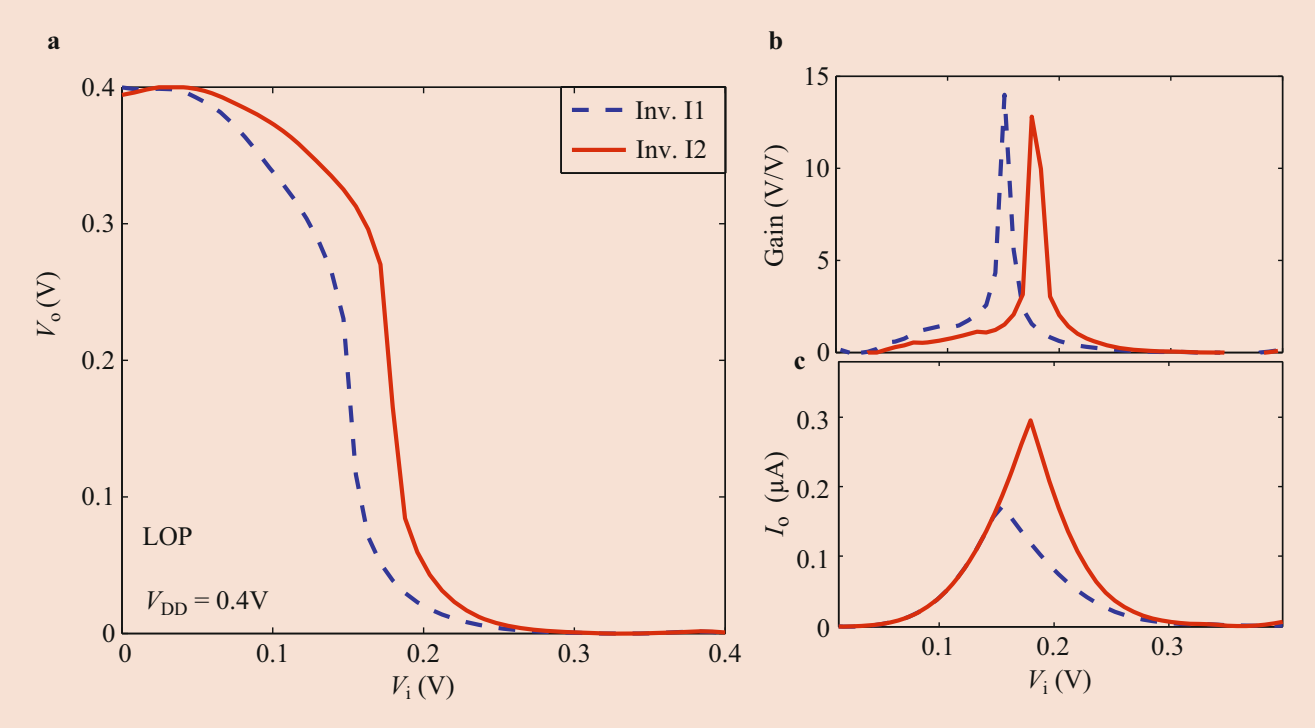

Fig. 41.19 (**a**) VTCs of inverters *I*1 and *I*2 in Fig. 41.17, computed exploiting nonlinear interpolation between simulated I_D-V_{DS} families, as described in Fig. 41.18. (**b**) Voltage gain and (**c**) current consumption during switching of the two inverters

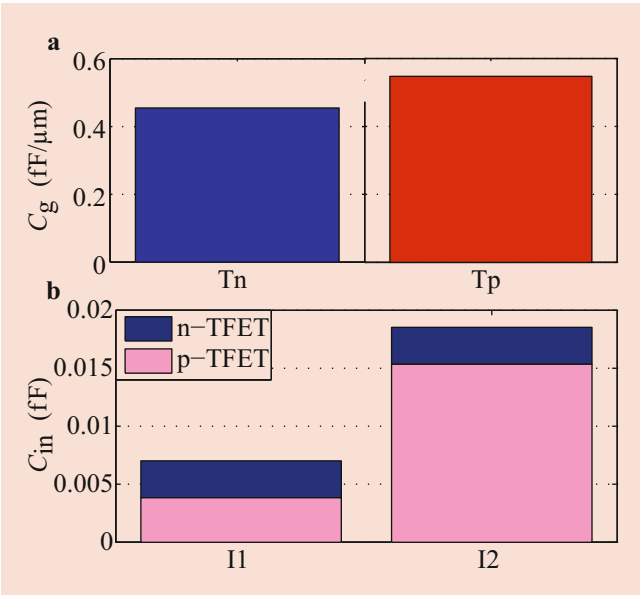

Fig. 41.20 (**a**) Gate capacitance computed through Eq. (41.22) for TFETs Tn and Tp and normalized by device side. (**b**) Total input capacitance of the two inverters, used to compute t_r and t_f in a self-loading configuration

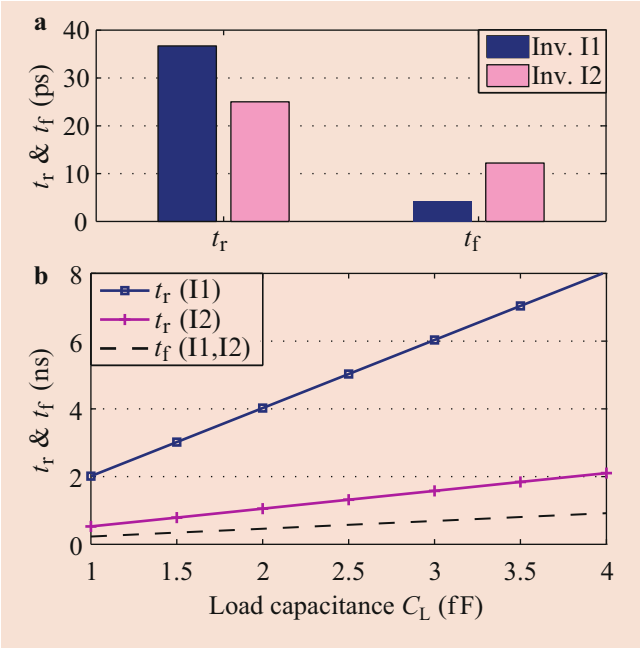

Fig. 41.21 Rise and fall times computed for inverters *I*1 and *I*2 in (**a**) self-loading (with Miller effects included) and (**b**) constant-loading. *I*2 provides more balanced and overall faster performance than *I*1

$$n_1(x) = n_S(x)\ \exp\left(\frac{E_t - E_{FS}}{k_B T}\right) + n_D(x)\ \exp\left(\frac{E_t - E_{FD}}{k_B T}\right) \quad (41.26a)$$

$$p_1(x) = p_S(x)\ \exp\left(\frac{E_{FS} - E_t}{k_B T}\right) + p_D(x)\ \exp\left(\frac{E_{FD} - E_t}{k_B T}\right) \quad (41.26b)$$

$n_{S/D}(x)$ and $p_{S/D}(x)$ being the electron and hole densities, respectively, at location x injected from the source/drain contact reservoir with Fermi level $E_{FS/D}$.

The following results refer to the same optimized Tn and Tp devices investigated in Sect. 41.4, in which traps at the semiconductor/oxide interfaces have been added. In order to use in the simulations a realistic trap density, the trap distribution measured in [49] on bulk MOS InAs structures was assumed for the InAs/oxide interfaces of the Tn and Tp heterostructures. Such D_{it}, assumed to be of acceptor type, is shown in Fig. 41.22, where E_C refers to the conduction band edge of the bulk material. For simplicity, the same D_{it} is also assumed for the AlGaSb/oxide interfaces, relative to the bulk conduction band edge of AlGaSb [40]. It should be noticed that in the investigated TFETs the oxide completely surrounds the nanowire for its full length, thus covering also the source and drain regions. Besides, D_{it} is assumed spatially uniform over the interface areas.

The turn-on characteristics of the optimum Tn and Tp TFETs with and without interface traps and in a stressed/unstressed condition are reported in Fig. 41.23 where no V_{GS}-shift has been applied [40]. $V_{DD} = 0.4\,V$ as in Sect. 41.4 and the currents are normalized to the nanowire side. A 0.5 GPa biaxial tensile stress is applied to improve I_{ON}: as shown in Sect. 41.3.3, this leads to a significant reduction in the bandgaps and effective masses, which causes an increase in the off-state current and a degradation of the subthreshold slope but also a relevant increase in I_{ON}. Indeed, the figure shows that when applying stress to both n- and p-channel devices with traps, the I_{ON} level of the ideal case is totally recovered (Fig. 41.24).

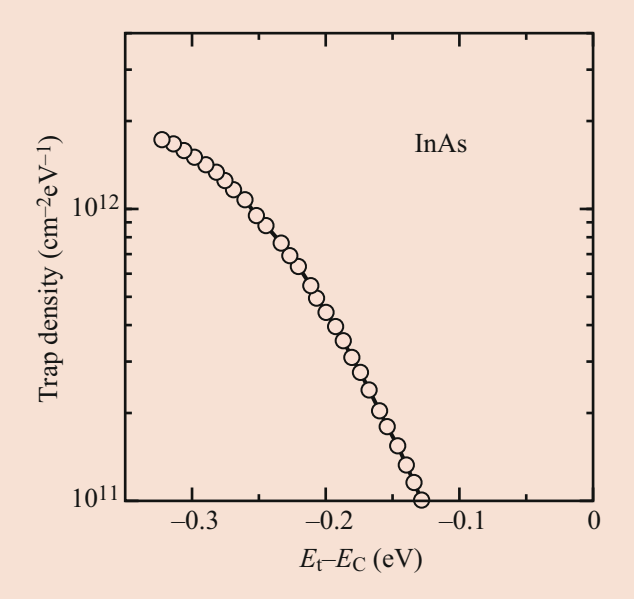

Fig. 41.22 Trap distribution taken from [49]

It is worth noting that traps play a different role in p- and n-channel devices, as traps are located at different energy windows within the two semiconductor bandgaps. A clear picture of the trap distribution in the AlGaSb and InAs nanowires is given in Fig. 41.25, where the trap energy windows are shown along with the band-edge profiles calculated with and without traps. The top panel of Fig. 41.25 refers to the n-channel TFET biased in subthreshold. Traps in the AlGaSb source region are almost empty, while the trapped electrons in the channel lift up the band edges and increase the source-to-drain tunneling distance. Thus, a threshold voltage shift comes out to be the most relevant effect induced by traps in Tn devices. In the bottom panel of Fig. 41.25, the subband profiles of the p-channel TFET are similarly reported in subthreshold regime. In this case, traps are empty in the channel region, while trapped electrons lift up the band edges in the InAs source region, thus reducing the amount of free electrons. The latter effect occurs at any gate bias. Thus, in the Tp devices, traps mainly induce a lower carrier injection.

As a final consideration, it is interesting to compare the different I–V curves after applying a V_{GS}-shift to match the same I_{OFF}, as shown in Fig. 41.24. The performance in terms of I_{ON}, average SS (SS_{avg}), and minimum SS (SS_{peak}) extracted from the curves in Fig. 41.24 is reported in Table 41.7 for both n- and p-channel devices. The detrimental effect of interface traps is quite evident, but strain shows a performance boost even with respect to the ideal cases.

41.6 Conclusions

In this chapter, a review of the $\boldsymbol{k} \cdot \boldsymbol{p}$ model has been presented, focusing in particular on its applications to the field of the simulation of nanoelectronic devices. The mathematical model of the eight-band version has been reported in full, including the additional terms required to cope with strain. The main goal was to convey the idea that the $\boldsymbol{k} \cdot \boldsymbol{p}$ model provides a reasonably simple way to describe with good accuracy the complex system of valence and conduction bands around the Γ point of many semiconductors and their deformations induced by strain, which play a fundamental

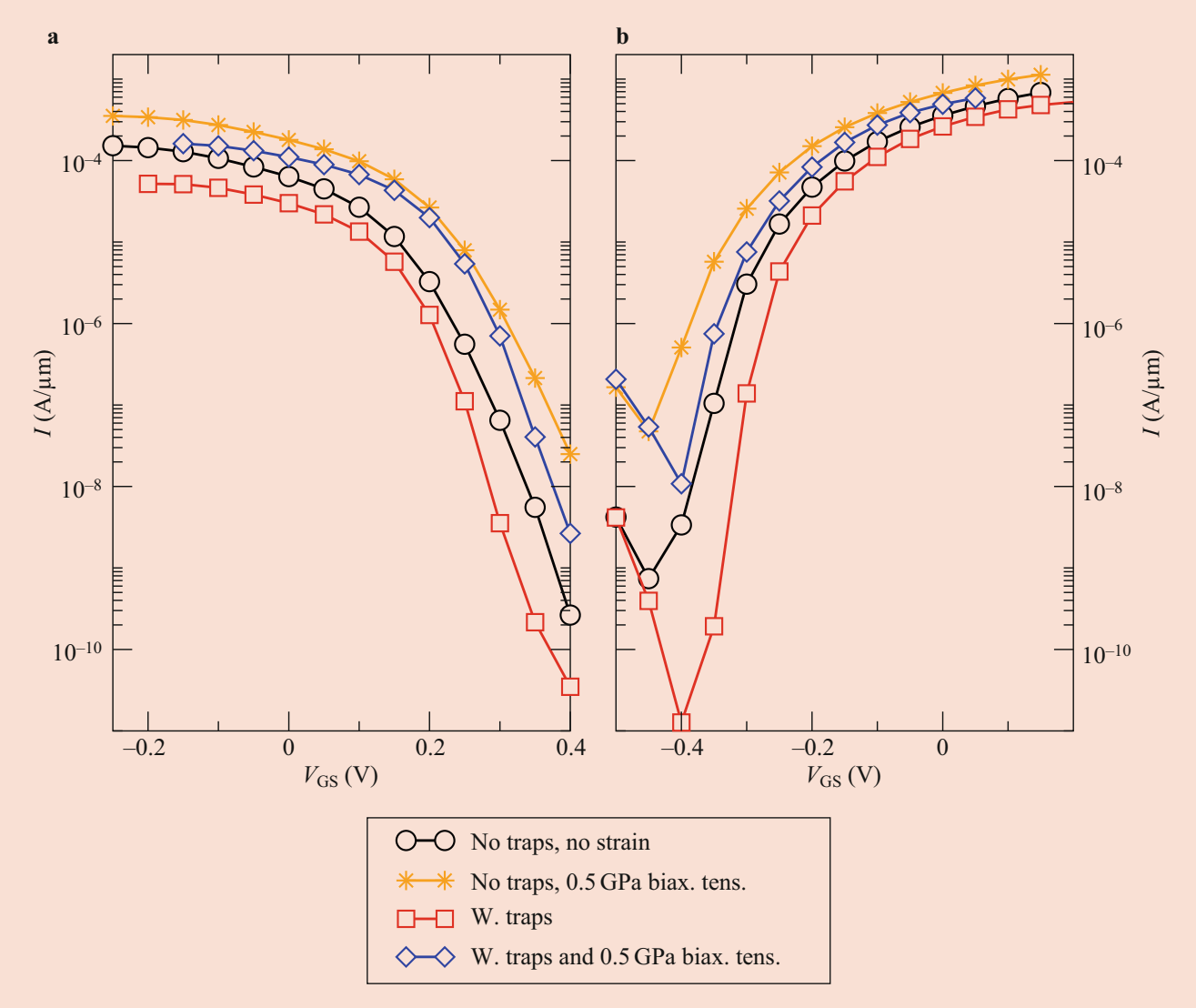

Fig. 41.23 I_{DS} versus V_{GS} at $|V_{DS}| = 0.4$ V with and without interface traps and with and without uniform biaxial tensile strain of 0.5 GPa on the cross section of the nanowire. (**a**): Tp. (**b**): Tn. Currents are normalized to the nanowire side

role in determining the electrical properties of the material. Several examples of energy-band calculations have been provided for III–V semiconductors of great potential for the nanoelectronic industry, relative to both bulk and confined structures.

When coupled with Poisson's equation and used within the nonequilibrium Green's functions framework, the $\boldsymbol{k} \cdot \boldsymbol{p}$ model becomes a powerful tool for the simulation of full devices. This is the case in particular for those devices where purely quantum mechanical effects, such as direct source-to-drain tunneling and band-to-band tunneling, play an essential role requiring also an accurate modeling of the details of the valence band, namely, Si and Ge p-channel FETs and direct-gap III–V tunnel FETs. This is because simpler approaches based on the effective mass are not adequate and, on the other hand, the physical picture does not justify to move to full-band atomistic methods, such as tight-binding, which become appropriate when high energy carriers far from the Γ point play an important role in the device.

Significant examples of application of the $\boldsymbol{k} \cdot \boldsymbol{p}$ model to device simulation have been given in this chapter, all of them relative to the field of tunnel FETs. Specific topics where the $\boldsymbol{k} \cdot \boldsymbol{p}$ model has been extensively applied are the investigation of the effects of strain in homojunction and heterojunction nanowire TFETs, the optimization of complementary TFETs and related inverters, and the investigation of the effect of interface traps on the same nanowire TFETs.

It is believed that the type and number of applications of the $\boldsymbol{k} \cdot \boldsymbol{p}$ model will increase as the device sizes will be pushed to the ultimate scaling limits and new emerging nanoelectronic devices will become available.

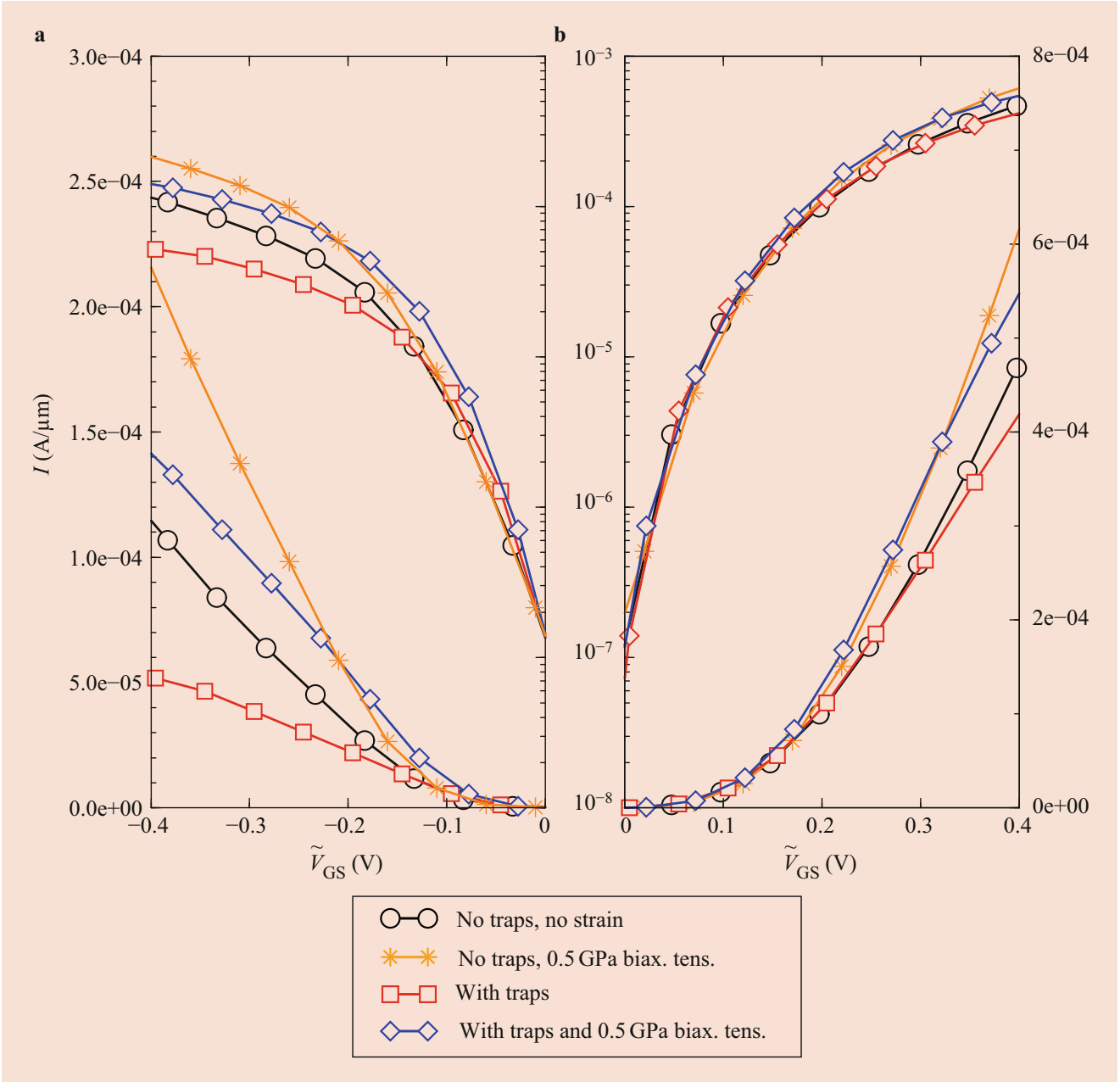

Fig. 41.24 I_{DS} versus $\widetilde{V}_{GS}$ at $|V_{DS}| = 0.4$ V with and without interface traps and with and without uniform biaxial tensile strain of 0.5 GPa on the cross section of the nanowire. (**a**): Tp. (**b**): Tn. Currents are normalized to the nanowire side and V_{GS}-shifted in order to have $I_{OFF} = 100\,\text{nA}/\mu\text{m}$ at $\widetilde{V}_{GS} = 0$ V

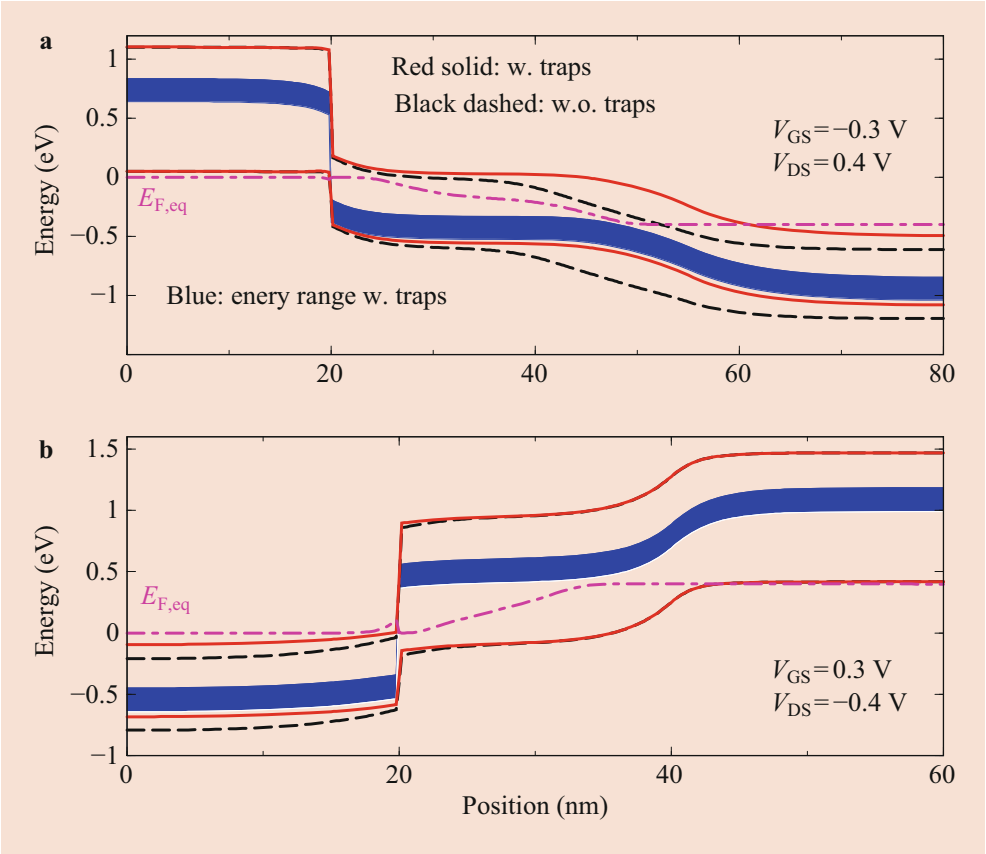

Fig. 41.25 Conduction and valence subband profiles for Tn (top) and Tp (bottom) TFETs. The two V_{GS} have been chosen to bias the devices in subthreshold: negative for Tn and positive for Tp. $V_{DS} = 0.4$ V. Dashed black: without traps. Solid red: with traps. The energy interval where trap levels are located is highlighted (in blue). Magenta dashed curve: equivalent Fermi level E_F^{eq}

Table 41.7 I_{ON}, average subthreshold slope (SS_{avg}) computed over three current decades, and peak slope (SS_{peak}) extracted from the curves for the NW TFETs reported in Fig. 41.24

n-TFET			
	I_{ON}	SS_{avg}	SS_{peak}
	(μA/μm)	(mV/dec)	(mV/dec)
No strain, no traps	466	40	31
Biax. tens., no traps	611	54	49
No strain, traps	413	40	34
Traps and biax. tens.	543	38	31
p-TFET			
	I_{ON}	SS_{avg}	SS_{peak}
	(μA/μm)	(mV/dec)	(mV/dec)
No strain, no traps	112	59	49
Biax. tens., no traps	214	62	54
No strain, traps	52	49	43
Traps and biax. tens.	140	43	41

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Ab initio Methods for Electronic Transport in Semiconductors and Nanostructures

42

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Contents

42.1 Introduction . . . 1516

42.2 Historical Overview . . . 1517
42.2.1 The Deformation Potential Theorem . . . 1517
42.2.2 The Rigid (Pseudo)ion . . . 1518

42.3 Theoretical Framework . . . 1519
42.3.1 Density Functional Perturbation Theory . . . 1522
42.3.2 Finite-Displacement Method . . . 1522
42.3.3 Electron-Phonon Interaction . . . 1523
42.3.4 *Ab initio* Simulation of Electronic Transport: The Monte Carlo Method . . . 1524

42.4 Silicon, Group-III Nitrides, and 2D Materials . . . 1525
42.4.1 Silicon . . . 1525
42.4.2 Group-III Nitrides . . . 1526
42.4.3 2D Materials . . . 1531

42.5 Dielectric Response of Low-dimensional Materials . . . 1538
42.5.1 Density-Density Response Function . . . 1539
42.5.2 Microscopic Poisson Equation . . . 1541
42.5.3 Microscopic Dielectric Tensor of 1D Materials . . . 1542
42.5.4 Microscopic Dielectric Permittivity of 2D Materials . . . 1544
42.5.5 Discussion . . . 1545

42.6 Quantum Transport . . . 1545
42.6.1 Ballistic Transport . . . 1547
42.6.2 Numerical Approach . . . 1547
42.6.3 Scattering—The Pauli Master Equation . . . 1549
42.6.4 Example 1: Graphene Nanoribbon Transistors . . . 1549
42.6.5 Example 2: Silicon Nanowire FETs . . . 1551

42.7 Conclusions and Outlook . . . 1552

References . . . 1555

Abstract

The past decade has seen the growing use of *ab initio* methods to study theoretically not only the atomic and electronic structure of semiconductors but also their charge-transport properties. This chapter focuses on "intrinsic" charge transport (limited by scattering with phonons) and starts with a brief historical overview of early work, mostly based at first on the deformation potential theorem and, later, on empirical pseudopotentials and on the rigid-ion approximation, to calculate electron-phonon matrix elements in semiconductors. This historical overview is followed by an outline of the theoretical framework employed when using density functional theory. Having described the full-band Monte Carlo method to solve the Boltzmann transport equation, the chapter presents examples of the use of *ab initio* methods to study the low-field mobility, high-field transport, and device performance in silicon, group-III nitrides, and two-dimensional materials. Throughout the discussion attention is paid to the limitations of *ab initio* methods. Finally, the chapter discusses how *ab initio* methods are used to study the dielectric response of solids and charge transport in the quantum limit.

Keywords

Density functional theory · Dielectric screening · Electronic transport · Electron-phonon interaction · Quantum transport · Two-dimensional semiconductors

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42.1 Introduction

Until recently, the theoretical study of charge transport in semiconductors and semiconductor devices has been based on some level of "empiricism." The library of software tools that constitute the technology computer-aided design (TCAD) in this area may indeed range from simple – but computationally efficient – models based on a drift-and-diffusion approximation of the semiclassical Boltzmann equation (BTE) [1], to models based on a hydrodynamic approximation [2, 3] or even to full-band Monte Carlo methods [4]. Yet, all of these models require some degree of empirical information, such as models for the carrier mobility as a function of doping and temperature, for the energy and momentum relaxation times, or deformation potentials to describe the strength of the interaction between charge carriers and phonons.

This degree of empiricism has been possible – and highly successful – thanks to the wealth of experimental information that has become available, since the late 1940s, about charge transport in silicon, germanium, and III–V compound semiconductors, materials used in the bulk of the micro- and nanotechnology products in logic, memory, and optoelectronics offered by the very-large-scale integration industry (VLSI). However, in the past decade or so, research has shifted to novel materials that may possibly replace or augment these "conventional" semiconductors, such as wide band gap semiconductors for power electronics (diamond, silicon carbide, group-III nitrides, or gallia – Ga_2O_3), or the growing number of two-dimensional (2D) materials that have attracted attention since the advent of graphene [5–8]. In many cases, little information is available about these materials, often not even their stability, and even less information is available about their charge-transport properties (*e.g.*, band gap, effective mass, and carrier mobility).

The rise of these new materials has moved the old dream of predicting the performance of an electronic device exclusively from "first-principles" (or *ab initio*) from the realm of a cultural and academic exercise to a necessity. Therefore, it is perhaps a fortunate coincidence that at the same time theoretical progress and improvement of the computational hardware have rendered *ab initio* methods reliable and predictable *almost* to the point at which experimental information is required not to build new empirical models but to simply confirm the theoretical predictions. (The reasons why we wrote *almost* will be evident below in Sect. 42.7.)

In the past, the use of first-principles methods has been restricted to small systems, mainly focused on their structures, total and formation energies, and bonding configurations but had little or no connection to electronic transport. However, the recent progress we have mentioned above has broadened their range of applications, improved their accuracy, and extended their scope to electronic transport [9, 10]. Density functional theory (DFT) is now routinely used to predict the atomic and electronic structure of new materials, thanks to the wide availability of computer packages, such as the Vienna *Ab initio* Software Package (VASP) [11–14] or Quantum ESPRESSO (QE) [15, 16]. Even the strength of the electron-phonon interaction can now be calculated using DFT using either the finite ion displacements [17] or density function perturbation theory (DFPT) [18, 19]. This constitutes a dramatic improvement since the early "pioneering" days in which the rigid-ion approximation [20] and empirical pseudopotentials were painstakingly used to estimate deformation potentials in Si, intervalley deformation potentials in III-V compound semiconductors [21–24], and used in Monte Carlo transport studies [25–28]. Even transport in open systems has been studied using DFT [29], and such an *ab initio* formalism has also been used to study dissipative transport in the two-dimensional materials of current interest [30].

In this chapter we present a birds-eye view of the historical evolution of "first-principles" methods toward the present state of art. Keeping in mind the scope of this chapter, we shall limit our attention to the use of first-principles methods in the study of electronic transport. Therefore, in this historical overview, we shall pay attention to the deformation potential theorem and the rigid-(pseudo)ion approximation, approximations that are now replaced by genuine *ab initio* methods, but that still play a huge role in research, thanks to their computational efficiency and their sound physical basis. Restricting our attention to density functional theory, in Sect. 42.3 we shall briefly present a general formulation of DFT and its application to the study of the electron-phonon interaction. As important examples of application of the theory, in Sect. 42.4 we shall consider silicon (obviously), considering the electron-phonon scattering rates, both intra-band and inter-band; the transport properties of group-III nitrides and selected 2D materials (to follow the present trend), employing DFT to compute the electron-phonon scattering rates and their transport properties (low-field mobility, velocity-field characteristics); and also device characteristics (in some cases) obtained from full-band Monte Carlo simulations based on the band structure and scattering rates obtained from these *ab initio* calculations. We shall then present, in Sect. 42.5, a different application of *ab initio* methods, namely, the calculation of the dielectric response of nanostructures, an important factor that controls the electrostatics of devices as well as dielectric screening of several perturbations. We shall present in Sect. 42.6 a brief overview of the use of pseudopotentials to deal with quantum transport in ultra-scaled devices, considering graphene nanoribbons as examples. In our final section, Sect. 42.7, having assessed the predictive power of *ab initio* methods, we shall consider also their limitations and speculate on what the future may promise.

Throughout this discussion, we consider only the electron-phonon interaction, since it is the subject that has received more attention as it is an intrinsic element in determining the charge-transport properties of electron devices. However, additional scattering processes, such as Coulomb scattering with ionized impurities and roughness at the semiconductor-insulator interface, have also been addressed using *ab initio* methods, as illustrated in Refs. [31, 32], for example. We also refrain from discussing molecular devices, although also in this case first-principles methods have been employed successfully (see Refs. [33, 34], for example).

42.2 Historical Overview

It is hard to define precisely the term "first principles" or *ab initio*. If we take a broad view and define a first-principles' approach as a way of expressing a transport-related quantity (such as the electron mobility, for example) in terms of "higher-level" physical quantities that are not directly related to transport (*e.g.*, a change of the band structure in the presence of vibrations of the crystal, phonons), probably the first example of such an *ab initio* approach is given by Bardeen's and Shockley's "deformation potential" theorem [35].

As we shall see below, the interaction between electrons and phonons can be expressed as the perturbation of the electronic motion caused by the displacements of the ions away from their equilibrium positions, displacements that are associated with the thermal vibrations of the lattice. Therefore, the Hamiltonian that describes this perturbation can be written as:

$$\widehat{H}_{\rm ep} = \int_{\Omega} {\rm d}\mathbf{r}\, \delta\widehat{U}_{\rm tot}(\mathbf{r})\widehat{\rho}(\mathbf{r})\,, \tag{42.1}$$

having indicated operators with a "hat." The quantity $\delta\widehat{U}_{\rm tot}(\mathbf{r})$ is the change of the total crystal potential at position $\mathbf{r}$ due to the presence of phonons and $\widehat{\rho}(\mathbf{r})$ is the electron density (that is, $\widehat{\psi}^{\dagger}(\mathbf{r})\widehat{\psi}(\mathbf{r})$ in terms of the (second-quantized) electron field $\widehat{\psi}$). The term $\delta\widehat{U}_{\rm tot}(\mathbf{r})$ can be written explicitly in terms of the displacement, $\delta\widehat{\mathbf{R}}^{(\eta)}_{l,\alpha,\mathbf{q}}$ of each ion α in the unit cell l caused by a phonon of wave vector $\mathbf{q}$ of branch η (longitudinal or transverse, acoustic or optical):

$$\delta\widehat{U}_{\rm tot}(\mathbf{r}) = \sum_{l,\alpha,\eta,\mathbf{q}} \frac{\delta E_{\rm tot}(\mathbf{r})}{\delta\mathbf{R}_{l,\alpha}} \cdot \delta\widehat{\mathbf{R}}^{(\eta)}_{l,\alpha,\mathbf{q}}\, {\rm e}^{{\rm i}\mathbf{q}\cdot\mathbf{r}}\,. \tag{42.2}$$

The quantity $\delta E_{\rm tot}(\mathbf{r})/\delta\mathbf{R}_{l,\alpha}$ represents the change of the total energy of the crystal at position $\mathbf{r}$ when the ion α in cell l is displaced from its equilibrium position by a shift $\delta\mathbf{R}_{l,\alpha}$. (In the following we shall express $\mathbf{R}_{l,\alpha}$ as $\mathbf{R}_l + \boldsymbol{\tau}_\alpha$, where $\boldsymbol{\tau}_\alpha$ is the position of ion α in the unit cell.) In second quantization, the ionic displacement can be expressed in terms of the phonon creation and annihilation operators $\widehat{b}^{(\eta)\dagger}_{\mathbf{q}}$ and $\widehat{b}^{(\eta)}_{\mathbf{q}}$, respectively:

$$\delta\widehat{\mathbf{R}}^{(\eta)}_{l,\alpha,\mathbf{q}} = \left(\frac{\hbar}{2\rho_{\rm x}\omega_{\mathbf{q}}}\right)^{1/2} \mathbf{e}^{(\eta)}_{\mathbf{q}}\, (\widehat{b}^{(\eta)\dagger}_{\mathbf{q}} + \widehat{b}^{(\eta)}_{-\mathbf{q}})\,, \tag{42.3}$$

where $\hbar$ is the reduced Planck's constant and $\mathbf{e}^{(\eta)}_{\mathbf{q}}$ is the phonon polarization vector. The use of first-order perturbation theory is standard practice in our context. Therefore, the matrix element for this process is given by (see Eq. (42.29) below):

$$\left\langle n', \mathbf{k}+\mathbf{q} \left| \delta\widehat{U}_{\rm tot}(\mathbf{r}) \right| n, \mathbf{k} \right\rangle\,, \tag{42.4}$$

where for simplicity we have denoted by $|n, \mathbf{k}\rangle$ a state in Fock space that contains a (Bloch) electron in band n and with wave vector $\mathbf{k}$. We have also omitted to write explicitly the phonons states, as we shall do in the following, since we shall assume them to be at thermal equilibrium.

42.2.1 The Deformation Potential Theorem

In the early days of research of semiconductor physics (around the late 1940s or 1950s), it was impossible to calculate the matrix element given by Eq. (42.4). However, Bardeen and Shockley viewed the *nonpolar* scattering of electrons with acoustic phonons (the process that limits the carrier mobility in Si and Ge), for example as caused by the local change of the energy of the conduction band minimum (or valence band maximum for the hole-phonon process) due to the local strain wave associated with the propagation of a phonon [35]. For example, under an isotropic (hydrostatic) dilatation/compression of the lattice, the lattice constant changes locally from a to $a+u$. This shifts the energy of the conduction band minimum. Therefore, as a dilatation/compression wave propagates in the crystal (*i.e.*, an acoustic phonon), an electron sees a "scattering potential":

$$\Delta E_{\rm c} = \frac{{\rm d}E_{\rm c}}{{\rm d}a} u\,. \tag{42.5}$$

More generally, since a displacement $\mathbf{u}$ of the medium corresponds to a local change $\Delta\Omega \approx \Omega\nabla\cdot\mathbf{u}$, of the volume Ω, we have (omitting the operator "hats" for simplicity):

$$\begin{aligned}\delta U_{\rm tot}(\mathbf{r}) &\sim \Delta E_{\rm c}(\mathbf{r}) \\ &= \Omega\frac{{\rm d}E_{\rm c}}{{\rm d}\Omega}\nabla\cdot\mathbf{u}(\mathbf{r}) \sim \Delta_{\rm ac}\, \mathbf{q}\cdot\mathbf{u}_{\mathbf{q}}\, {\rm e}^{{\rm i}\mathbf{q}\cdot\mathbf{r}}\,,\end{aligned} \tag{42.6}$$

where the last expression considers a single Fourier component $\mathbf{u}_{\mathbf{q}}{\rm e}^{{\rm i}\mathbf{q}\cdot\mathbf{r}}$ of the displacement $\mathbf{u}(\mathbf{r})$. The quantity $\Delta_{\rm ac} = \Omega{\rm d}E_{\rm c}/{\rm d}\Omega$ is called the "deformation potential". From Eq. (42.3) we see that the presence of an acoustic phonon

of wavelength $\lambda = 2\pi/q$ and frequency $\omega_{\mathbf{q}}$ (where $\mathbf{q}$ is the phonon wave vector) implies a shift of the atomic positions of magnitude:

$$u_{\mathbf{q}} \approx \left(\frac{\hbar}{2\rho_{\mathrm{x}}\omega_{\mathbf{q}}}\right)^{1/2}, \tag{42.7}$$

(where ρ_{x} is the crystal mass density). Thus, the scattering potential becomes:

$$\Delta E_{\mathrm{c}}\, q u_{\mathbf{q}}\, \mathrm{e}^{\mathrm{i}\mathbf{q}\cdot\mathbf{r}} \approx \Delta E_{\mathrm{c}} q \left(\frac{\hbar}{2\rho_{\mathrm{x}}\omega_{\mathbf{q}}}\right)^{1/2} \mathrm{e}^{\mathrm{i}\mathbf{q}\cdot\mathbf{r}}, \tag{42.8}$$

so that, for longitudinal phonons, the squared electron-phonon matrix element can be approximated as:

$$|\langle \mathbf{k}+\mathbf{q}|\widehat{H}_{\mathrm{ac}}|\mathbf{k}\rangle|^2 \approx \frac{\hbar\Delta_{\mathrm{ac}}^2 q^2}{2\rho_{\mathrm{x}}\omega_{\mathbf{q}}}\left(N_{\mathbf{q}} + \frac{1}{2} \pm \frac{1}{2}\right), \tag{42.9}$$

where the plus (minus) sign applies to emission (absorption) processes and $N_{\mathbf{q}}$ is the Bose-Einstein population of phonons of momentum $\hbar\mathbf{q}$ at thermal equilibrium. Therefore, considering that for small energies electrons emit or absorb only small-q acoustic phonons, we can assume a linear phonon dispersion with a slope given by the sound velocity υ_{s}, that is, $\omega_{\mathbf{q}} = \upsilon_{\mathrm{s}} q$. We can also assume that the phonon energy is much smaller than the thermal energy $k_{\mathrm{B}}T$ (where k_{B} is the Boltzmann constant), so that $N_{\mathbf{q}} \approx k_{\mathrm{B}}T/(\hbar\upsilon_{\mathrm{s}}q) \gg 1$ and scattering can be treated as an elastic process. Thus, finally, the momentum relaxation rate becomes simply:

$$\frac{1}{\tau_{\mathrm{ac}}(E)} = \frac{2^{1/2}\Delta_{\mathrm{ac}}^2 m^{*3/2} k_{\mathrm{B}}T}{\pi\hbar^4\rho_{\mathrm{x}}\upsilon_{\mathrm{s}}^2} E^{1/2}, \tag{42.10}$$

and the electron mobility can now be calculated with the only unknown parameter Δ_{ac} that can be obtained experimentally from measurements of the band gap of the crystal as a function of hydrostatic compression. Therefore, a transport quantity, the electron mobility, is now linked to a more fundamental quantity, the deformation potential, which is not directly related to charge transport.

In this oversimplified picture, electrons can couple only to longitudinal acoustic (LA) phonons, since the anisotropy of the band structure of silicon and germanium near the band extrema has been ignored. A few years later, Herring and Vogt [36] accounted for this effect and provided an approximated form for the deformation potentials for the interaction of electrons with LA and transverse acoustic (TA) phonons in terms of the dilatation deformation potential, Ξ_{d}, of the uniaxial shear deformation potential, Ξ_{u}, and of the angle $\theta_{\mathbf{q}}$ between the wave vector $\mathbf{q}$ of the phonon and the longitudinal axis of the ellipsoidal equi-energy surfaces:

$$\begin{aligned} \Delta_{\mathrm{LA}} &\approx \Xi_{\mathrm{d}} + \Xi_{\mathrm{u}}\cos^2\theta_q \\ \Delta_{\mathrm{TA}} &\approx \Xi_{\mathrm{u}}\sin\theta_q\,\cos\theta_q\,. \end{aligned} \tag{42.11}$$

42.2.2 The Rigid (Pseudo)ion

When Bardeen and Shockley presented their deformation potential theorem, there was only scant and often incorrect experimental information about both the band structure and the transport properties of silicon and germanium. However, in the mid-to-late 1960s, as more reliable experimental information became available and computer technology continued to progress, it became possible to perform full-band structure calculations, empirical pseudopotentials being at the time the preferred choice.

Developed for bulk semiconductors of the diamond and zinc blende structure at first [37,38], the pseudopotential only needs "form factors" for a small set of wave vectors coinciding with reciprocal lattice $\mathbf{G}$ vectors. For nanostructures, full functional forms $V_{\alpha q}$ were developed to study strained materials and nanostructures that require larger "supercells," since in both cases knowledge of $V_{\alpha q}$ is required for arbitrary values of q. Details about these functional forms for various semiconductors, as well as details about their applications to study electronic transport in nanostructures, can be found in Refs. [39,40].

These empirical pseudopotentials were used to calculate the phonon-induced narrowing of the band gap at high temperatures [41–44], finally giving a solid (if not *ab initio*) justification of the empirical models that were in use (see, *e.g.*, Ref. [45]). This problem has been revisited recently using methods that can be labeled genuine *ab initio* calculations [46]. However, this interesting problem falls outside the scope of this chapter.

Moreover, and more to the point of our discussion, these empirical pseudopotentials were used to improve upon the deformation potential approximation: once the empirical pseudopotential $V_\alpha(\mathbf{r})$ of an ion α is known, Eq. (42.2) can be re-expressed in terms of the Fourier components of the ionic pseudopotential, $V_{\alpha,\mathbf{p}}$, assuming that the ionic potential shifts rigidly:

$$\begin{aligned} &\delta\widehat{U}_{\mathrm{tot}}(\mathbf{r}) \\ &\quad\approx \sum_{l,\alpha,\eta,\mathbf{q},\mathbf{p}} \mathrm{i}\, V_{\alpha,\mathbf{p}}\, \mathrm{e}^{\mathrm{i}\mathbf{p}\cdot(\mathbf{r}+\mathbf{R}_{l,\alpha})}\mathbf{p}\cdot\delta\widehat{\mathbf{R}}_{l,\alpha,\mathbf{q}}^{(\eta)}\, \mathrm{e}^{\mathrm{i}\mathbf{q}\cdot\mathbf{r}}. \end{aligned} \tag{42.12}$$

Using some semiempirical models to obtain the phonon dispersion and polarization vectors, such as the valence shell model [47,48]), Zollner and Cardona were able to calculate the scattering rates for intervalley scattering in several III–V compound semiconductors [21–24], thus confirming the ex-

perimental results obtained by sub-picosecond pump-probe measurements [49].

At the same time, empirical pseudopotentials were beginning to be used not only to calculate the electron-phonon interaction (so, the electron dynamics) but also to extend the validity of transport models to a range of high energy in which the universally used effective mass approximation clearly failed. This was of tremendous practical interest because of the reliability issues caused by hot electrons in the ever-shrinking devices of the VLSI technology. The major breakthrough occurred in 1981, when Shichijo and Hess [50] developed a Monte Carlo approach to account for the electron kinematics (energy and group velocity) using the band structure of GaAs calculated using local empirical pseudopotentials. The electron-phonon scattering rates were treated empirically starting from the *Ansatz* that their energy dependence must reflect the density of (final) states, an *Ansatz* whose validity has been confirmed recently (see Ref. [51] and references therein). This "full-band" approach was later extended by Tang and Hess to silicon [52, 53], by Brennan and Hess to several other III–V compound semiconductors [54] and by Fischetti and Laux to simulate not only homogeneous transport but also inhomogeneous and realistic semiconductor devices [4].

Obviously, silicon has been the subject of studies performed by several groups also employing empirical pseudopotentials and empirical "deformation potentials" fitted to available experimental data on high-energy transport, such as velocity-field characteristics at high fields [55, 56], impact ionization [52, 55, 57–59], and injection into the SiO_2 gate insulator. Theoretical support for these semiempirical full-band models has been obtained by using empirical pseudopotentials (and Harris potentials) to calculate the electron-phonon scattering rates in Si and other semiconductors within the rigid-ion approximation [25–28], as discussed recently in Ref. [51]. In Fig. 42.1 we show the total electron-phonon scattering rates averaged over equi-energy surfaces and bands plotted as a function of electron kinetic energy as calculated using empirical deformation potentials [4, 55, 56] compared to quasi-*ab initio* calculations using Harris potentials [26–28, 56] and empirical pseudopotential [25].

More recently, the rigid-(pseudo)ion method has been extended to 2D materials, specifically to calculate the electron-phonon scattering rates in free-standing graphene [60]. Figure 42.2 shows the electron-phonon scattering rates calculated at 300 K for a free-standing sheet. The mobility and velocity-field characteristics obtained using these results (as reported in Ref. [60]) are in good agreement with available experimental data and show that even relatively poorly known materials (at least, less known than Si) can be studied successfully using these models.

The discussion presented so far can be viewed as a snapshot of the state of the art before DFT began to replace these

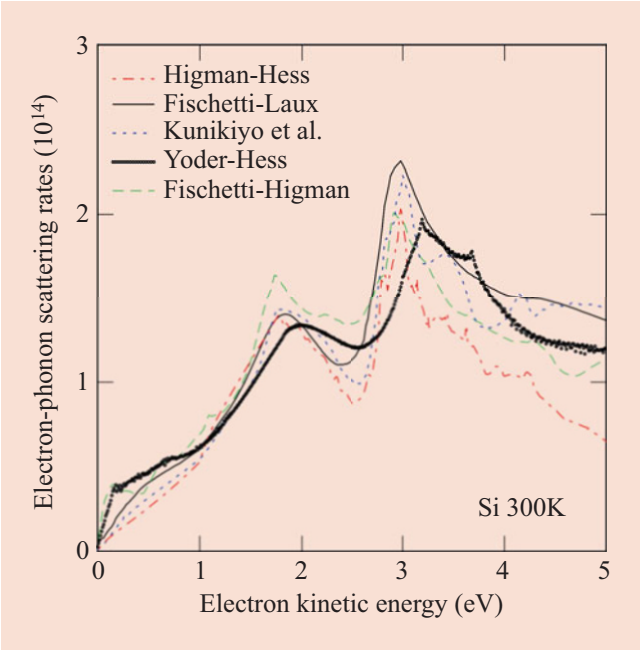

Fig. 42.1 Electron-phonon scattering rates calculated using the rigid-(pseudo)ion model and empirical pseudopotentials [25, 55] (labeled "Fischetti-Higman" and "Kunikiyo et al."), Harris potentials [27, 56] (labeled "Higman-Hess" and "Yoder-Hess") compared to rates calculated using empirically determined deformation potential calibrated to reproduce known experimental data [4] (labeled "Fischetti-Laux")

quasi-empirical methods. Most of the research has focused on electron transport in silicon, and undeniably the empirical nature of these models (via the calibrated pseudopotentials and simple models for the phonon spectra and polarization) limits their predictive power. Therefore, exploring novel materials requires the more fundamental approach inherent to genuine *ab initio* methods that we discuss next. Nevertheless, the very empirical nature of these pseudopotentials guarantees "by definition" an accurate description of the excited spectrum of semiconductors (viz., band gap and effective masses), as required when attempting to assess the performance of devices based on "known" materials. Considering also their relative numerical simplicity, these quasi-first-principles method are still used in useful applications.

42.3 Theoretical Framework

In this chapter we restrict our discussion to plane-wave DFT together with (self-consistent) pseudopotentials. However, we should at least mention the fact that ballistic electronic transport has been studied also using all-electron methods [62, 63] by Polizzi's group [64, 65], among others, thus avoiding the need to "pseudize" the system. Moreover, at least when studying relatively small molecules, all-electron methods have also been used without resorting to approxi-

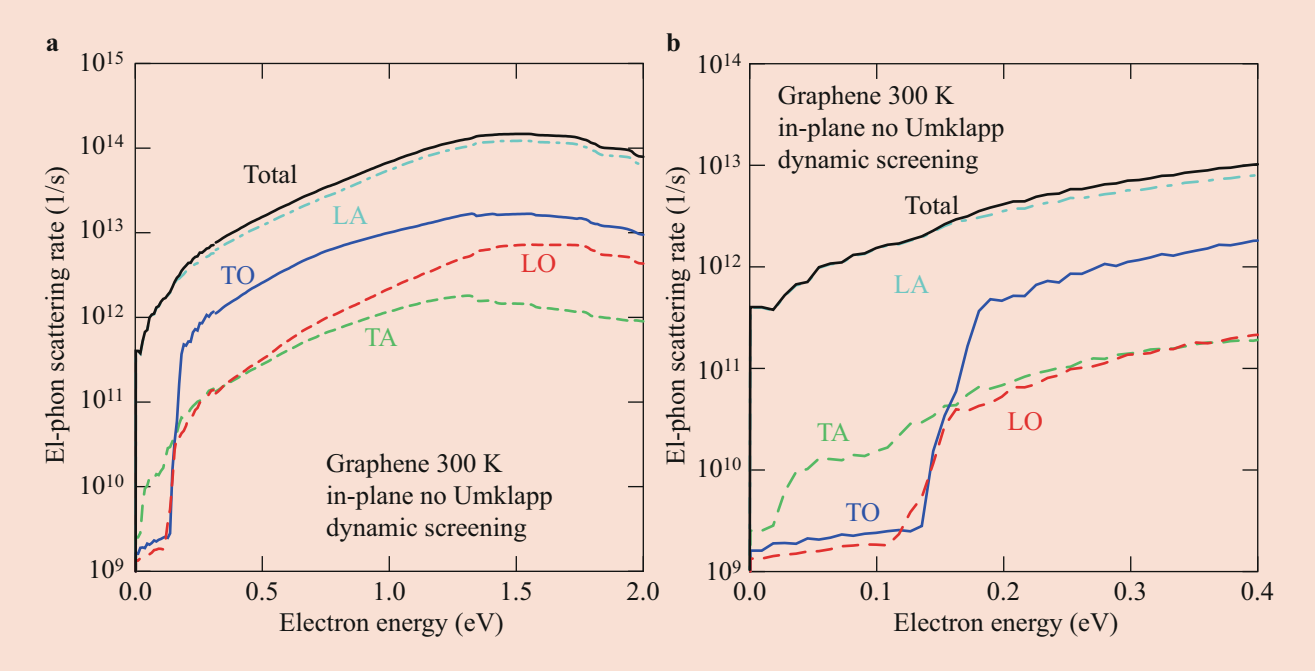

Fig. 42.2 (**a**) calculated total electron-phonon scattering rates in graphene at 300 K using the dynamic screening model by Wunsch et al. [61]. (**b**) as in the left frame but expanding the low-energy region. (After M. V. Fischetti et al. [60], with permission from the Institute of Physics ©2013 Institute of Physics)

mated exchange and correlation functionals but employing, instead, the GW method (see Ref. [66], for example).

The maturity of DFT can be judged by the number of software packages that are presently available. Most of them are based on plane waves or projector-augmented plane waves (VASP [11–14], Quantum ESPRESSO [15, 16], GPAW [67, 68], CASTEP [69], ABINIT [70]), others on localized orbitals (such as SIESTA [71, 72], or ATK [73, 74]). As we had noted in the Introduction, DFT has been born with the goal of studying the atomic and electronic structure of solids. Only recently some of these computer packages have been extended to handle electronic transport (such as TranSIESTA [75] or Quantum Wise-ATK [73, 74] or EPW [76, 77]). Here we shall focus only in DFT based on a plane-wave basis and look exclusively at electronic transport.

Modern DFT implementations start from the self-consistent solution of the Kohn-Sham equation [14, 15, 78, 79]:

$$H_e\psi_i = \left[-\frac{\hbar^2}{2m}\nabla^2 + V_{\text{eff}}(\mathbf{r})\right]\psi_i = E_i\psi_i(\mathbf{r})\,, \qquad (42.13)$$

where H_e is the electron Hamiltonian whose first term represents the kinetic energy and V_{eff} represents the effective Kohn-Sham potential:

$$V_{\text{eff}} = [V_{\text{ion}}(\mathbf{r}) + V_h(\mathbf{r}) + V_{xc}(\mathbf{r})]\ . \qquad (42.14)$$

Here $V_{\text{ion}}(\mathbf{r})$ is the sum of the ionic potentials $(-Z_j e^2/(4\pi\epsilon_0|\mathbf{r} - \mathbf{R}_j|))$ originating from all atoms, with valence Z_j and located at $\mathbf{R}_j$, in the system. The second term is the Hartree potential, capturing the effect of the interaction of all electrons with each other:

$$V_h = \int \frac{e^2}{4\pi\epsilon_0|\mathbf{r} - \mathbf{r}'|}\rho(\mathbf{r}')\mathrm{d}\mathbf{r}'\,, \qquad (42.15)$$

using SI units (e is the magnitude of the electron charge and ϵ_0 is the vacuum permittivity). The Hartree potential does not fully capture the interaction of electrons with each other. This is where DFT comes with the final term on the left-hand side, the exchange-correlation potential:

$$V_{xc}(\mathbf{r}) = \frac{\partial E_{xc}[\rho]}{\partial\rho(\mathbf{r})}\,, \qquad (42.16)$$

where $E_{xc}[\rho(\mathbf{r})]$ is the exchange-correlation functional. The final element required to generate a closed set of equations, is the charge density $e\rho(\mathbf{r})$ which is simply calculated by summing over all occupied Kohn-Sham wavefunctions:

$$\rho(\mathbf{r}) = 2\sum_i^{N/2}|\psi_i(\mathbf{r})|^2\,. \qquad (42.17)$$

The prefactor 2 accounts for spin degeneracy, and the sum runs over $N/2$ wavefunctions where N is the total number of electrons in the system.

Equations (42.13–42.17) provide a set of equations which can be solved for any atomic configuration, provided an exchange-correlation functional is selected. Some minor and major numerical issues appear in a practical implementation. Several approximations are generally in order. We discuss two important approximations that we use to study the electron-phonon interaction in crystals.

First, we consider ideal crystals; this means that an infinite number of atoms, arranged in a periodic configuration, is present in the system under consideration. The periodic system is described by a set of three basis vectors, spanning the unit cell, and an additional set of vectors specifying the location of all composing atomic species inside the unit cell, $\boldsymbol{\tau}_\alpha$. In Eq. (42.17), we introduced i as a generic quantum number. In a crystal, the ionic potential is periodic, and the quantum number i actually consists of a wave vector $\mathbf{k}$ and a band index n. The charge density is then determined by summing over an appropriate k-space discretization, possibly exploiting crystal symmetry, and a number of bands defined by the number of electrons in the system. We also introduced a second generic index j for the position of each atom; however, from now on we will use $\mathbf{R}_{l,\alpha}$ to denote the position of ion α in unit cell l.

Second, a numerical all-electron solution, solving Eq. (42.14) directly, is possible but requires a very fine discretization of the wavefunctions. To deal with systems of sufficiently large size, an approximation needs to be introduced that significantly reduces the computational burden. The need for a very fine discretization stems from the $-Z_j e^2/|\mathbf{r} - \mathbf{R}_{l,\alpha}|$ contributions to the ionic potential, which are singular at $\mathbf{R}_{l,\alpha}$. There are also a large number of core electronic states, which remain identical regardless of the crystal under consideration. A first simplification to reduce the computational burden is to compute only the charge density of the valence electrons, *i.e.*, the electrons which are not core electrons, and to incorporate the impact of core electrons through a modification of the (bare) ionic potential $V_{\text{ion}}(\mathbf{r})$. However, even when calculating only the valence states, rapid wavefunction oscillations remain near the center location of the ion $\mathbf{R}_{l,\alpha}$. To avoid these rapid oscillations, a pseudopotential approximation is introduced.

We omit the details of the implementation of modern pseudopotential-like approximations, such as the projector-augmented wavefunction approach [80, 81], but the general picture of these approaches is captured by a wavefunction composed of plane waves:

$$\psi_{\text{pw}}(\mathbf{r}) = \sum_{\mathbf{G}} c_{\mathbf{G}} e^{i\mathbf{G}\cdot\mathbf{r}} , \tag{42.18}$$

where $\mathbf{G}$ are reciprocal lattice vectors. The number of reciprocal lattice vectors $\mathbf{G}$ determines the size of the Hamiltonian in its numerical implementation. To realize maximal computational efficiency, approaches try to minimize the number of reciprocal lattice vectors while still faithfully capturing the electronic behavior of the system. The plane-wave wavefunctions are not actual wavefunctions and need to be augmented to accurately capture the rapidly oscillating nature of the actual wavefunction near the core. Overall, the pseudopotential approach gives excellent results and limits the number of plane waves required for an accurate solution quite efficiently.

Once the Kohn-Sham wavefunctions are found, the ground-state energy of the crystal is determined as:

$$\begin{aligned} E = &\sum_i \langle\psi_i| - \frac{\hbar^2\nabla^2}{2m} |\psi_i\rangle \\ &+ \frac{e^2}{2} \int\int \mathrm{d}\mathbf{r}\mathrm{d}\mathbf{r}' \frac{\rho(\mathbf{r})\rho(\mathbf{r}')}{4\pi\epsilon_0|\mathbf{r}-\mathbf{r}'|} \\ &+ \int \mathrm{d}\mathbf{r}\, V_{\text{ion}}(\mathbf{r})\rho(\mathbf{r}) + E_{\text{xc}}[\rho] + E_{\text{ions}} \end{aligned} \tag{42.19}$$

where the sum over i runs over all valence band states. This ground-state energy is a function of the atomic positions and is a measure of the stability of the structure under study, *i.e.*, a lower energy means a more favorable atomic configuration. The favorable/unfavorable nature of the configuration can be quantified through the calculation of the force acting on each atom:

$$\mathbf{F}_{l,\alpha} = -\frac{\partial E}{\partial \mathbf{R}_{l,\alpha}} . \tag{42.20}$$

This force can be evaluated from the Kohn-Sham wavefunctions using the Hellmann-Feynman theorem [82] and comes at minimal computational cost once the Kohn-Sham equation is solved.

This means that once an initial atomic configuration is provided, the energy of the atomic configuration can be computed as well as the force acting on each atom. Based on these forces, a new atomic configuration can be constructed and again the energy and the forces can be computed. Repeating this process and using an optimization algorithm like the Broyden-Fletcher-Goldfarb-Shanno (BFGS) algorithm [83], the atomic configuration with minimal energy can be determined. This process is referred to as "structural relaxation," and at the end of relaxation, the crystal is in its minimal energy configuration and the force acting on each atom vanishes.

Next, we are interested in the possible lattice vibrations in the system: the phonons. To determine the phonon spectrum, the second-order force-constant tensor is required:

$$\Phi_{l\alpha l'\alpha'} = \frac{\partial \mathbf{F}_{l,\alpha}}{\partial \mathbf{R}_{l'\alpha'}} \tag{42.21}$$

to construct the dynamical matrix. Unfortunately, the calculation of the second-order force constants is much more expensive compared to the calculation of the forces, *i.e.*, the first-

order force constants acting on each atom. The reason why the evaluation of the first-order constants is computationally cheap is because the ground-state energy minimizes the energy with respect to the charge density: $\partial E[\rho(\mathbf{r})]/\partial\rho(\mathbf{r}) = 0$. This enables the evaluation of the first-order force constants without computing $\Delta\rho(\mathbf{r}) = \partial\rho(\mathbf{r})/\partial\mathbf{R}_{l,\alpha}$. For the second-order force constants on the other hand, $\Delta\rho(\mathbf{r})$ has to be computed.

Similarly, the final quantity of interest for the electron-phonon interaction is the change in potential due to the displacement of an atom:

$$\frac{\partial(V_{\text{ion}} + V_{\text{h}} + V_{\text{xc}})}{\partial\mathbf{R}_{l,\alpha}}. \tag{42.22}$$

Just like for the second-order force constants, more information than is available from the solutions of the Kohn-Sham equation is required and $\Delta\rho(\mathbf{r})$ must be calculated.

Two methods are available to compute the second-order force constants and the change in potential due to atomic displacements: the density functional perturbation theory (DFPT) method and the finite-displacement method. Both methods are equivalent if implemented with sufficient accuracy; we give a brief overview of both methods next sections.

42.3.1 Density Functional Perturbation Theory

The density functional perturbation theory [16,84] approach introduces a new set of equations that have to be solved simultaneously to determine the change in the Kohn-Sham wavefunctions $\Delta\psi_n$ and the change in the energies ΔE_n under the application of a perturbation of the ionic potential $\Delta V_{\text{ion}}(\mathbf{r})$:

$$(H_{\text{e}} - E_n)\,|\Delta\psi_n\rangle = -(\Delta V_{\text{eff}} - \Delta E_n)\,|\psi_n\rangle\,, \tag{42.23}$$

$$\Delta V_{\text{eff}}(\mathbf{r}) = \Delta V_{\text{ion}}(\mathbf{r}) + e^2\int\frac{\Delta\rho(\mathbf{r}')}{4\pi\epsilon_0|\mathbf{r}-\mathbf{r}'|}\mathrm{d}\mathbf{r}' + \left.\frac{\mathrm{d}v_{\text{xc}}(\rho)}{\mathrm{d}\rho}\right|_{\rho=\rho(\mathbf{r})}\Delta\rho(\mathbf{r})\,, \tag{42.24}$$

where:

$$\Delta\rho(\mathbf{r}) = \sum_i \psi_i^*(\mathbf{r})\Delta\psi_i(\mathbf{r}). \tag{42.25}$$

These three equations have to solved simultaneously for every displacement of every relevant perturbation of the ionic potential under consideration. Assuming the computational burden to solve the DFPT equations (42.23–42.25) is similar to that of solving the Kohn-Sham equation (42.13–42.17); computing the phonon spectrum and the electron-phonon interaction strength is nominally $3N_{\text{ion}}N_q$ more expensive where N_{ion} counts the number of ions in each unit cell and N_q counts the number of phonon wave vectors of interest. Computing the phonon dispersion (or spectrum) is relatively straightforward for crystals with smaller unit cells, especially when symmetry further reduces the computational expense [85,86]. On the other hand, determining the phonon spectrum of crystals with large unit cells quickly becomes very expensive.

Having determined $\Delta\rho(\mathbf{r})$ and $\Delta V_{\text{eff}}(\mathbf{r})$, the second-order force constants as well as the change of the potential can be determined, and we can proceed with the calculation of the phonon spectrum or the electron-phonon matrix elements. To save computational resources, interpolation methods [76] can be used to interpolate calculated phonon energies and electron-phonon matrix elements onto a finer grid of phonon wave vectors.

42.3.2 Finite-Displacement Method

In the finite-displacement method [17,87], atoms are slightly displaced away from their equilibrium position $\mathbf{R}^{(0)}_{l,\alpha}$ to a new position $\mathbf{R}^{(0)}_{l,\alpha}+\delta\mathbf{R}$. The whole procedure of solving the Kohn-Sham equation (42.13–42.17) is repeated for a whole set of displacements, and for every displacement the forces are computed. The second-order force constants and the potential change due to atom displacement can then be found using the finite difference method.

For example, to determine the derivative of the total energy required to evaluate the electron-phonon matrix elements, the Kohn-Sham equation is solved when the atom $l\alpha$ is slightly displaced from its equilibrium position $\mathbf{R}^{(0)}_{l'\alpha'}$ along the positive and negative j direction, $\mathbf{R}_{l'\alpha'} = \mathbf{R}^{(0)}_{l'\alpha'} \pm \epsilon\mathbf{e}_j$, where $\mathbf{e}_j$ is a unit vector along the direction j and ϵ is a small number. This gives us the total crystal energies, E^{j+}_{tot} and E^{j-}_{tot}, after the positive and negative displacement along the j Cartesian direction. Repeating the procedure for the other two Cartesian directions and using the central difference scheme, the j component of the quantity $\delta E_{\text{tot}}/\delta\mathbf{R}_{l,\alpha}$ appearing in Eq. (42.2) (or ΔV_{eff} in Eq. (42.27) below) can be approximated by the expression:

$$\left.\frac{\delta E_{\text{tot}}}{\delta\mathbf{R}_{l,\alpha}}\right|_j \approx \frac{E^{j+}_{\text{tot}} - E^{j-}_{\text{tot}}}{2\epsilon}\,. \tag{42.26}$$

Moreover, the (j,j') element of the second-order force constant (*i.e.*, the (j,j') element of the dynamical matrix) can be obtained in a similar way, although somewhat more laboriously, by solving the Kohn-Sham equation when both the atom $l\alpha$ and the atom $l'\alpha'$ are slightly displaced from their equilibrium position along the positive and negative Cartesian axes, thus obtaining the second-order change, $\Delta^{(2)}E_{\text{tot}ll'\alpha\alpha'}$, which is central difference approximation to the dynamical matrix $\Phi_{jl\alpha,j'l'\alpha'}$, Eq. (42.21). In practice, such

a cumbersome and time-consuming procedure is streamlined by using the Hellmann-Feynman theorem, as mentioned above.

One important consideration for the finite-displacement method is the interaction between periodic images. When displacing an atom in one unit cell in the simulation, the equivalent atom in every unit cell is displaced in exactly the same way in all other unit cells. This generates spurious interactions between neighboring cells. To minimize these spurious interactions, it is important to perform the calculations on a larger unit cell. For example, in the extreme case of a crystal which has only one atom in its primitive unit cell, no change in the energy will be observed when moving the atom in the primitive unit cell. Instead, the primitive unit cell has to be duplicated forming a supercell that is larger in size by an integer factor γ in each direction. The supercell now contains γ^3 atoms instead of 1. A larger γ will result in reduced spurious interaction but will unfortunately also rapidly increase computational memory requirements.

Both the finite-displacement method and the density functional perturbation approach will give the same quantities, provided calculations are performed with sufficient accuracy. The choice of one method over the other may be motivated by convenience or by a more efficient execution on the available computational resources. The finite-displacement method has the advantage that it only needs the solution of the Kohn-Sham equation and only relies on the most mature part of DFT codes. Parallelization is straightforward in the finite-displacement method, and the calculation over all displacements can be performed as parallel DFT calculations. Interpolation onto a finer grid may also be more straightforward using the finite difference method compared to the DFPT method. The DFPT approach may however be more resource efficient and require fewer iterations than a new solution of the Kohn-Sham equation for every displacement.

42.3.3 Electron-Phonon Interaction

The final object of interest is the electron-phonon interaction Hamiltonian which is computed from ΔV_{eff} (which we can identify with $\delta\widehat{U}_{\text{tot}}$; see Eqs. (42.1), (42.2), and (42.4)):

$$\widehat{H}_{\text{e-ph}} = \int \mathrm{d}\mathbf{r}\, \widehat{\rho}(\mathbf{r})\Delta V_{\text{eff}}(\mathbf{r}) \approx \times \int \mathrm{d}\mathbf{r}\, \widehat{\rho}(\mathbf{r}) \sum_{l,\alpha,\eta,\mathbf{q}} \frac{\delta E_{\text{tot}}(\mathbf{r})}{\delta \mathbf{R}_{l,\alpha}} \cdot \delta\widehat{\mathbf{R}}^{(\eta)}_{l,\alpha,\mathbf{q}}\, \mathrm{e}^{\mathrm{i}\mathbf{q}\cdot\mathbf{r}}\,, \tag{42.27}$$

where $\delta\widehat{\mathbf{R}}^{(\eta)}_{l,\alpha,\mathbf{q}}$ is the ion displacement operator expressed in Eq. (42.3) in terms of the annihilation and creation operators, $\widehat{b}^{(\eta)}_{\mathbf{q}}$ and $\widehat{b}^{(\eta)\dagger}_{\mathbf{q}}$, for a phonon in branch η with wave vector $\mathbf{q}$ and frequency $\omega^{(\eta)}_{\mathbf{q}}$. Using a finite-volume normalization, here we define the amplitude of the displacement $d^{(\eta)}_{\mathbf{q}\alpha}$ as:

$$d^{(\eta)}_{\mathbf{q}\alpha} = \sqrt{\frac{\hbar}{2NM_\alpha\omega^{(\eta)}_{\mathbf{q}}}} \tag{42.28}$$

where M_α is the mass of ion α and N is the number of unit cells in the lattice.

Consider an electron in band n with wave vector $\mathbf{k}$ that makes a transition to band m with wave vector $\mathbf{k+q}$ while emitting a phonon. For this electron, the matrix element between states allowed by Pauli's principle reads:

$$\langle m\mathbf{k}+\mathbf{q} \mid \widehat{H}_{\text{e-ph}}\, \widehat{b}^{(\eta)\dagger}_{\mathbf{q}} \mid n\mathbf{k}\rangle = \sum_{l,\alpha} d^{(\eta)}_{\mathbf{q}\alpha}\mathrm{e}^{\mathrm{i}\mathbf{q}\cdot\mathbf{R}_{l,\alpha}}\mathbf{e}^{(\eta)}_{\mathbf{q}\alpha} \cdot \left(\int_\Omega \mathrm{d}\mathbf{r}\, \psi^*_{m\mathbf{k}+\mathbf{q}}(\mathbf{r})\frac{\delta E_{\text{tot}}}{\delta \mathbf{R}_{l,\alpha}}\, \psi_{n\mathbf{k}}(\mathbf{r})\right)\,. \tag{42.29}$$

Invoking the Bloch theorem, $\psi_{n\mathbf{k}}(\mathbf{r}) = u_{n\mathbf{k}}(\mathbf{r})\mathrm{e}^{\mathrm{i}\mathbf{k}\cdot\mathbf{r}}$, and for Eq. (42.29) to hold, the periodic part $u_{n\mathbf{k}}(\mathbf{r})$ must be normalized on the unit cell.

Equation (42.29) is proportional to the square root of the inverse of the phonon frequency $(\omega^{\eta}_{\mathbf{q}})^{-1/2}$ through the magnitude of the displacement. A smoother quantity measuring electron-phonon interaction strength is the deformation potential which can be implicitly defined using:

$$\langle m\mathbf{k}+\mathbf{q} \mid \widehat{H}_{\text{e-ph}}\, \widehat{b}^{(\eta)\dagger}_{\mathbf{q}} \mid n\mathbf{k}\rangle = \frac{1}{\sqrt{\Omega}}\sum_{\eta} DK^{(\eta)}_{nm\mathbf{k}\mathbf{q}}\sqrt{\frac{\hbar}{2\rho\omega^{(\eta)}_{\mathbf{q}}}}\,, \tag{42.30}$$

where we introduced the mass density $\rho_{\text{x}} = M_{\text{cell}}/\Omega_{\text{cell}}$ and the volume of the unit cell Ω_{cell}. The volume of the crystal Ω is then $N\Omega_{\text{cell}}$. Combining Eqs. (42.29) and (42.30), the deformation potential is:

$$DK^{(\eta)}_{\mathbf{k}\mathbf{q}mn} = \sum_{\alpha} \mathbf{M}_{mn\mathbf{k}\mathbf{q}\alpha}\cdot\mathbf{e}^{(\eta)}_{\mathbf{q}\alpha}\sqrt{\frac{M_{\text{cell}}}{M_\alpha}}\,, \tag{42.31}$$

where

$$\mathbf{M}_{mn\mathbf{k}\mathbf{q}\alpha} = \int_\Omega \mathrm{d}\mathbf{r}\, u^*_{m\mathbf{k}+\mathbf{q}}(\mathbf{r})\Delta V_{\text{eff}} u^*_{n\mathbf{k}}(\mathbf{r})\mathrm{e}^{\mathrm{i}\mathbf{q}\cdot(\boldsymbol{\tau}_\alpha-\mathbf{r})}\,, \tag{42.32}$$

where we should recall that $\boldsymbol{\tau}_\alpha$ is the position of ion α in the unit cell.

One subtlety in the calculation and interpretation of deformation potentials arises when initial or final electronic states are degenerate or when the phonon branches are degenerate. In case of degeneracy, the band or branch index is

not sufficient to uniquely determine the state and denoting the deformation potential as "$D^{(\eta)}_{nm\mathbf{kq}}$" is ambiguous. For example, this is the case for the threefold degenerate valence band at Γ in many popular materials, *e.g.* silicon.

Similarly, many materials have twofold degenerate TA and TO phonons. In the case of degeneracy, depending on which linear combination of the valence band wavefunctions is taken and the direction of the phonon displacement vectors, different values for "$D^{(\eta)}_{nm\mathbf{kq}}$" are obtained. One simple way to remove the ambiguity is to take the square root of the sum of all squared deformation potentials for degenerate initial or final electronic states, or degenerate phonons. An alternative choice is the largest deformation potential upon rotation of any wavefunctions or phonon displacement vectors within the subspace of the degeneracy.

42.3.4 *Ab initio* Simulation of Electronic Transport: The Monte Carlo Method

The Monte Carlo method is the most accurate method to study electron transport at the semiclassical level. It is a well-established method, originally proposed by Kurosawa in the context of semiconductors [88] that has been described in detail in Refs. [89–91]. Its use in conjunction with a description of the band structure of semiconductors obtained from empirical pseudopotentials has been pioneered by Hess' group [50, 52, 53] and by the IBM group [4].

In the context of *ab initio* studies of charge transport, the same numerical methods used in these latter references can be used, the major difference consisting in the use of DFT to obtain the band structure, of the electron-phonon scattering rates obtained using the finite-displacement method or DFPT. Moreover, the "exact" matrix elements given by Eqs. (42.4) and (42.27) are used together with the full phonon dispersion to select the final state after each collision.

Whereas a fully detailed presentation of the full-band Monte Carlo method goes beyond the scope of this chapter, here we present a brief outline.

We have employed the synchronous ensemble Monte Carlo method since it is suitable to study time-dependent transport in inhomogeneous systems, such as electron devices. In this method, the motion of an ensemble of particles (≈300 up to 50,000 particles, depending on whether one considers homogeneous transport or transport in a realistically large device), is simulated subjecting them to the externally applied electric field (possibly obtained self-consistently with Poisson equation) and to the given scattering mechanisms. An initial state $\mathbf{k}$, band n, and position $\mathbf{r}$ are assigned to each particle stochastically. The motion of each particle is then evolved for a constant duration of time Δt (free flight) conforming to the equations of motion: $\hbar \mathrm{d}\mathbf{k}/\mathrm{d}t = \mp e\mathbf{F}(\mathbf{r})$ (the sign depending on the type of carriers under study, electrons of holes) and $\mathrm{d}\mathbf{r}/\mathrm{d}t = \upsilon_n(\mathbf{k})$, where $\mathbf{F}(\mathbf{r})$ is the electric field at position $\mathbf{r}$ and $\upsilon_n(\mathbf{k})$ is the carrier group velocity in band n, $\nabla E_n(\mathbf{k})/\hbar$, $E_n(\mathbf{k})$ being the kinetic energy of the carrier. In synchronous simulations, the duration of the free flight, Δt, is chosen based on the maximum scattering rate in the energy interval under consideration. At the end of their free flight, a random scattering mechanism is chosen stochastically. Based on the selected scattering mechanism, a new $\mathbf{k}$ state is also chosen stochastically for the particles according to the probability distribution given by the density of final states (calculated using the Gilat-Raubenheimer algorithm [92, 93], obviously modified to deal with transport in 2D materials [39]) multiplied by the squared matrix element of the scattering process. This is then treated as the initial state for the next free flight.

Quantities of interest, such as average velocity, energy, carrier density, and currents at the contacts, are recorded at the end of each Monte Carlo iteration. This process is repeated until steady state is reached or until the end of a transient (such as the turn-on of a transistor). In full-band simulations, the energy and group velocity are calculated (in our case, using DFT) on a discretized Brillouin zone, and stored in look up tables, to solve the equations of motion in free flight. The scattering rates are calculated and tabulated on the same mesh.

Calculations performed assuming a homogeneous electric field are usually performed to obtain information about the "intrinsic" transport properties of a material, namely, the low-field mobility and velocity-field characteristics. In order to minimize the stochastic noise at low field (the drift velocity being of the same order of magnitude of – or even much smaller than – the thermal velocity), the low-field mobility, μ_θ, is calculated from the diffusion constant, D_θ, along the chosen direction θ, using the Einstein relation. We should note that in the case of 2D materials with a Dirac-like electron dispersion, μ_θ, has to be extracted from D_θ using a generalization of the Einstein relation [60]:

$$\mu_\theta = \frac{eD_\theta}{k_\mathrm{B}T}\int_0^\infty \mathrm{d}\eta\, \frac{\eta\, \mathrm{e}^{\eta-\eta_\mathrm{F}}}{[1+\mathrm{e}^{\eta-\eta_\mathrm{F}}]^2} \times \left(\int_0^\infty \mathrm{d}\eta \frac{\eta}{[1+\mathrm{e}^{\eta-\eta_\mathrm{F}}]}\right)^{-1}, \tag{42.33}$$

where now $\eta_\mathrm{F} = E_\mathrm{F}/(k_\mathrm{B}T)$ denotes the Fermi energy in thermal units. The diffusion constant is evaluated from the Monte Carlo simulator:

$$D_\theta = \frac{1}{2}\frac{\mathrm{d}}{\mathrm{d}t}\left\langle (x_\theta - \langle x_\theta\rangle)^2\right\rangle, \tag{42.34}$$

where $\langle x_\theta \rangle$ is the time-dependent ensemble-average position along the direction θ of electrons initially at the origin, $\mathbf{r} = 0$, diffusing in the absence of an electric field.

The simulation of electronic transport in inhomogeneous conditions, such as in a transistor, is performed in a similar way. In this case the electric field $\mathbf{F}(\mathbf{r})$ is obtained from a numerical solution of the Poisson equation. In "atomistic" simulations, like those considered below in Sect. 42.6, the problem arises of how to define dielectric interfaces (such as the channel/gate insulator interface). In Sect. 42.5 we shall provide an *ab initio* solution of this problem.

42.4 Silicon, Group-III Nitrides, and 2D Materials

42.4.1 Silicon

It is of the utmost interest to show how electron-phonon scattering rates calculated with the DFT method just discussed compare with the semiempirical rates shown in Fig. 42.1 and discussed in Sect. 42.2. Since these results have been verified against a wealth of experimental data (see Ref. [51]), this constitutes a stringent test for *ab initio* methods.

In Fig. 42.3 we show the results obtained using the Quantum ESPRESSO DFT computer program [15, 16] with a kinetic energy cutoff of 35 Ry using the Perdew-Burke-Ernzerhof (PBE) [94] generalized gradient approximation (GGA) exchange-correlation functionals, norm-conserving pseudopotentials [95], a uniform grid of $12 \times 12 \times 12$ **k**-points for the self-consistent charge density calculation, and of $6 \times 6 \times 6$ **q**-points for the calculation of the phonon spectra. The 300 K electron-phonon scattering rates have been calculated using the Wannier interpolation method implemented by the EPW package [76] on a finer grid of $18 \times 18 \times 18$ **k**-points with a Gaussian smearing of 10 meV.

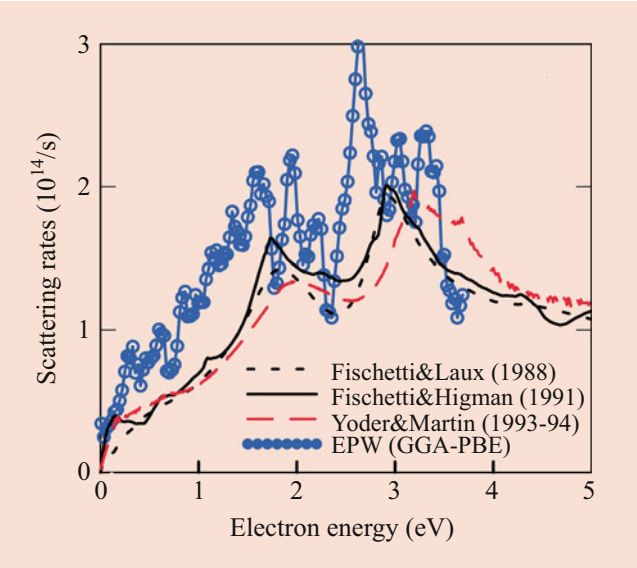

Fig. 42.3 Electron-phonon scattering rates at 300 K calculated following Refs. [76, 77] (EPW) compared to those obtained within the rigid-ion approximation [25–28] and those employed in the Monte Carlo simulations reported in Ref. [4]. The data represent an average over all "initial" wave vectors (distributed on a uniform mesh in the Brillouin zone) and bands at a given energy. The "noise" affecting the EPW data is the result of the coarser mesh used. The lines connecting the symbols are only a guide to the eye. (After M. V. Fischetti et al. [51], with permission from the American Institute of Physics ©2019 American Institute of Physics)

When looking at Fig. 42.3, we should stress that the results of Refs. [4, 25–28] have been averaged over constant-energy shells with weight given by the density of initial states using the algorithm proposed by Gilat and Raubenheimer [92, 93]. On the contrary, the EPW scattering rates shown here have been "smoothed" by averaging the raw data over the **k**-mesh described above over energy bins ∼27 meV wide. This permits a straightforward reproduction of these results.

The overall agreement is quite remarkable. However, as we shall discuss in Sect. 42.7, electron transport is very sensitive to variations of the band structure (such as effective masses and energy of satellite valleys, when present) that are usually considered "small errors" in DFT. For example, an error of the order of $k_B T$ (≈25 meV at room temperature) for the energy of satellite valleys in some 2D TMDs may be considered negligible when looking at optical absorption spectra but may cause very large errors in determining the electron mobility if intervalley scattering dominates transport.

To assess the sensitivity of the computed mobility and velocity-field characteristics to different choices of pseudopotentials and exchange-correlation functionals, we have calculated the mobility *(i)* using the GGA-PBE approximation and the less accurate local density approximation [95], both using the same norm-conserving pseudopotentials [95], and *(ii)* using the norm-conserving and ultrasoft pseudopotentials [96], both within the PBE-GGA approximation.

The results of this exercise are shown in Fig. 42.4. A significant spread of the data is quite evident. We shall discuss below, also in Sect. 42.7, how numerical issues may affect the results. This spread has been also discussed in Ref. [97] in the case of black phosphorus monolayers (phosphorene) and by Poncé et al. [77] in a general case. Accurate scattering rates can be obtained only when employing an extremely fine discretization of the Brillouin zone. This is certainly possible when considering only the "low-energy pockets" that are need to calculate the low-field carrier mobility, as indeed done in Ref. [77]. However, a fine discretization remains numerically challenging when considering the entire Brillouin zone as required when studying high-energy (high-field) transport. The practical need for a coarser discretization results in an additional and significant numerical uncertainty that affects the results. Therefore, at present we cannot yet expect a perfect quantitative or conclusive agreement with experimental data.

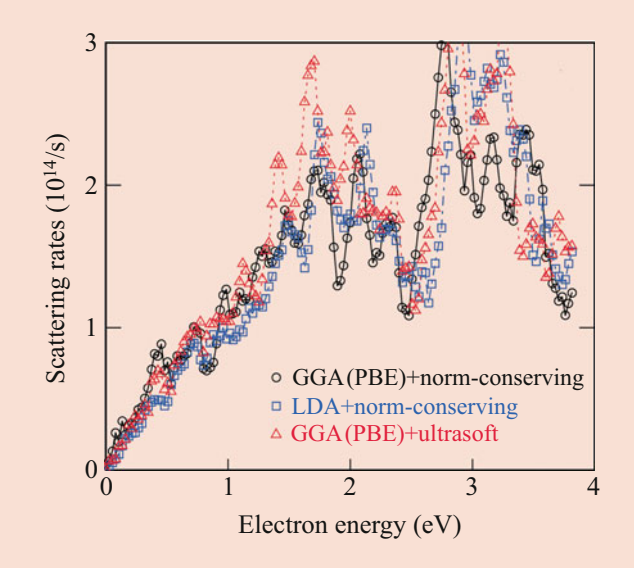

Fig. 42.4 As in the previous figure, but now the scattering rates shown have been calculated using different pseudopotentials and exchange-correlation functionals, as indicated. As in Fig. 42.3, the data represent an average over all "initial" wave vectors (distributed on a uniform mesh in the Brillouin zone) and bands at a given energy. The lines connecting the symbols are only a guide to the eye. (After M. V. Fischetti et al. [51], with permission from the American Institute of Physics ©2019 American Institute of Physics)

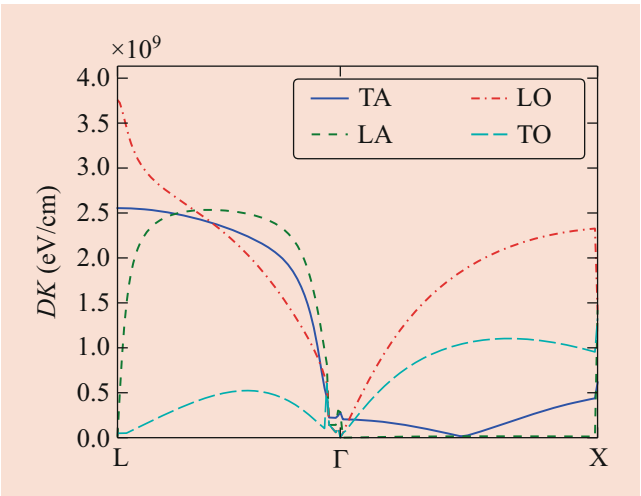

Fig. 42.5 Deformation potentials in bulk silicon for an electron starting at the valence band at Γ, transition to the conduction band along one of the Γ-L or Γ-X symmetry lines. For BTBT, the values at 0.85 in the Γ-X direction are the relevant quantity, and we find $D_{TA} = 3.5\times10^8$eV/cm, $D_{TO} = 1.0\times10^9$eV/cm, and $D_{LO} = 2.3\times10^9$eV/cm. (After W. G. Vandenberghe et al. [17], with permission from the American Institute of Physics ©2015 American Institute of Physics)

As an another important example of deformation potentials obtained from first principles, we consider the deformation potentials that determine the phonon-assisted inter-band tunneling exploited in tunnel field-effect transistors (tFETs). In this case, we have used the Vienna *ab initio* simulation package (VASP) [13] to solve the Kohn-Sham equation. We have used the finite-displacement method to find the phonon frequencies, polarization vectors, and electron-phonon *inter-band* matrix elements. The full details of the calculation can be found in Ref. [17].

In Fig. 42.5 we exhibit the calculated deformation potential for an electron transitioning from the top of the valence band to the first conduction band. We compute the interaction with all phonon branches along the Γ-L and the Γ-X high symmetry lines. Silicon has six phonon branches, but the two transverse branches (TA and TO) are twofold degenerate. Inspecting Fig. 42.5, we see that only the interaction with the TA vanishes. Values of the deformation potentials are quite large and measure up to 4×10^9eV/cm.

The deformation potentials relevant for BTBT are found at 0.85 in the Γ−X direction, and their calculated values are $D_{TA} = 3.5 \times 10^8$ eV/cm, $D_{TO} = 1.0 \times 10^9$ eV/cm, and $D_{LO} = 2.3 \times 10^9$ eV/cm. These values are much larger than previous theoretical estimates [98], but this is in line with the recent experimental estimate $D_{TO} \approx 10$–13×10^8 eV/cm from Ref. [99].

These results are very relevant to many practical applications since inter-band tunneling determines the probability of band-to-band transitions in silicon. In indirect-gap semiconductors, such as Si, band-to-band transitions (BTBT) are assisted by phonons and proceed from the valence band maximum (Γ) to the conduction band minimum, located near the X symmetry point.

42.4.2 Group-III Nitrides

Since wide band gap semiconductors are very important for power electronics, it is important to study their transport properties not just near thermal equilibrium, as it is assumed when calculating the low-field carrier mobility. Studies need to account for the high kinetic energy that electrons can reach at the high electric fields that are present in high-voltage devices. Group-III nitrides in the wurtzite phase constitute a key family of semiconductors that are employed in power devices. They have been investigated extensively theoretically using full-band Monte Carlo simulations based on empirical pseudopotentials and with electron-phonon scattering rates calculated using constant deformation potentials calibrated to experimental data, similarly to what had been done for Si before the "advent" of DFT, as discussed in Sect. 42.2. As in all empirical approaches, these studies – most notably those described in Refs. [100, 101] – must rely on experimental data that are often hard to obtain and interpret.

Most notably, the value of the all-important energy of the satellite valleys at the symmetry point L in GaN plays a crucial role in determining its high-field transport properties. Experimental data [102] and theoretical calculations using calibrated empirical pseudopotentials and DFT (VASP) [103]

have resulted in vastly different values for this quantity (0.8–1 eV experimentally, from Refs. [104, 105], 2.1–2.3 eV theoretically, from Refs. [106, 107]). This has resulted, in turn, in diverging opinions regarding the role of Auger recombination in these devices, a process that plays a major role at high injection levels in power devices. Therefore, it is of utmost interest to investigate this issue theoretically, coupling DFT and Monte Carlo studies to experimental data and establish the correctness of the theory compared to experiments. Here we shall not go into this controversial issue, but we shall see how *ab initio* methods can be used in two group-III nitrides of high interest in this context, GaN (with a band gap of ∼3.4 eV at 300 K [108]) and AlN (with a band gap of ∼6.026 eV at 300 K [109]).

The study has been performed obtaining the electronic band structure and the phonon dispersion using Quantum ESPRESSO [15, 16] with norm-conserving pseudopotentials [110] and the local density approximation (LDA) for the exchange-correlation functional. The dynamical matrix determined using DFPT was used to obtain phonon spectra, and the electron-phonon scattering rates have been calculated using the "electron-phonon coupling using Wannier functions" (EPW) program [76, 111, 112]. The maximally localized Wannier functions are obtained from the Wannier90 software package [113].

GaN

The band structure of wurtzite GaN along selected high symmetry lines is shown in Fig. 42.6a. We also list in Table 42.1 the energies of the satellite valleys compared with previous results [100, 101, 104–107, 114, 115], (one should recall the controversy we have mentioned above regarding the energy of the satellite L-valleys.) Rather than relaxing the structure, we have used the experimentally measured lattice constants $a = 3.215$ Å and $c = 5.241$ Å [116].

Table 42.2 shows the ability of DFT to give reliable values for the effective masses. These are extracted from the curvature of the electron dispersion at the bottom of the first-conduction band valleys. The effective mass at the Γ point of the first conduction band computed from DFT is 0.2 m_0 (where m_0 is the free electron mass). This value is in good agreement with the experimental values reported by Drechsler [117] (0.2 m_0) and Witowski [118] (0.222 m_0). The effective mass at the Γ point in the second conduction band is only slightly larger, 0.28 m_0.

Figure 42.6b shows the phonon dispersion of the wurtzite GaN. The longitudinal and transverse sound velocities are 7930 m/s and 3994 m/s, respectively [125]. Note the rather large energy of the highest-energy optical phonon, about 91.2 meV at Γ. The calculated polar and nonpolar scattering with optical and acoustic phonons are shown in Fig. 42.7a, b, respectively. Note that the polar scattering rate with acoustic phonons (*i.e.*, piezoelectric scattering) has a strength that is very similar to strength of the polar scattering with optical phonons at low energies. This shows that DFT correctly confirms the well-known fact that piezoelectric scattering plays an important role in determining the low-field electron mobility even at room temperature, unlike other III–V compound semiconductors like GaAs or InAs. In these figures we show also the scattering rates calculated with the analytical formulas presented in Ref. [90] to fit the first-principles scattering rates. These "analytic" scattering rates have been calculated using an effective mass of 0.2 m_0, a nonparabolicity factor of 0.58 eV^{-1}, and an intravalley deformation potential in the Γ-valley of ∼4.0 eV. For the nonpolar scattering rates with optical phonons, we have used an optical deformation

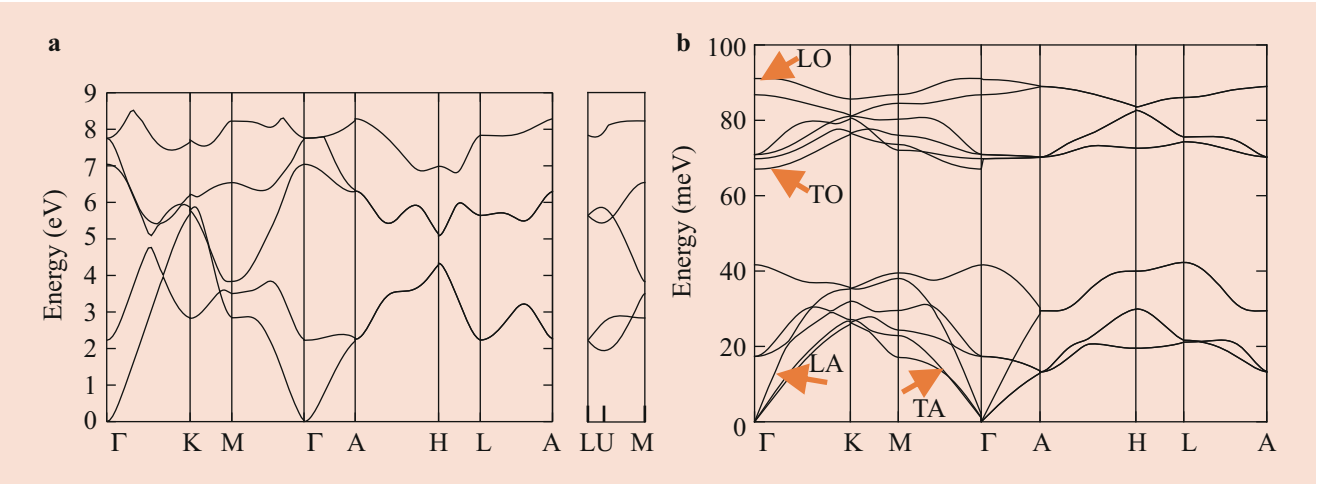

Fig. 42.6 (**a**) Calculated energy dispersion of the first five conduction bands of wurtzite GaN along several high symmetry lines; (**b**) Full phonon dispersion along several high symmetry lines of wurtzite GaN. The longitudinal and transverse acoustic phonon modes and the long-range transverse and longitudinal optical phonons are indicated by arrows. (After J. Fang et al. [133], with permission from the American Physical Society ©2019 American Physical Society)

Table 42.1 The conduction band energies at different satellite valleys (in units of eV) in wurtzite GaN and AlN

		K	U	L	A	Γ^3	M
GaN	This work	2.82	1.95	2.23	2.25	2.23	2.84
	LDA+G_0W_0 (Ref. [107])	3.06	2.32	2.60	2.43	2.50	3.27
	GW (Ref. [106])	3.1		2.5	2.6	2.4	3.0
	EPM(Ref. [114])	1.59	1.34			2.14	1.87
	EPM (Ref. [100])	3.08		2.43	2.37	2.35	3.05
	Expt. (Ref. [104])			0.90 ± 0.08			
	Expt. (Ref. [105])			0.97 ± 0.02			
	Expt. (Ref. [115])		1.34				
AlN	This work	0.64	0.61	0.92	2.11	2.27	1.33
	LDA+G_0W_0 (Ref. [107])	0.84	0.67	0.99	2.28	2.65	1.57
	GW (Ref. [106])	0.9		1.1	2.5	2.5	1.6
	EPM (Ref. [114])	0.9	1.05			2.49	1.68
	EPM (Ref. [100])	1.26		1.32	2.33	2.46	1.95

After J. Fang et al. [133], with permission from the American Physical Society ©2019 American Physical Society The conduction band energy at the Γ-valley of the first conduction band is set as the zero reference energy

Table 42.2 Electron effective mass (in units of the free electron mass m_0) along different crystalline directions at the first conduction band of different valleys and acoustic phonons' sound velocities (in units of m/s) of GaN

	This work	Other work
$m^\star_\Gamma(\Gamma \to K)$	0.20	0.18[a], 0.36[b]
$m^\star_K(K \to \Gamma)$	0.64	0.47[c]
$m^\star_K(K \to M)$	0.65	
$m^\star_M(M \to K)$	0.21	0.565[c]
$m^\star_M(M \to \Gamma)$	4.18	
$m^\star_\Gamma(\Gamma \to M)$	0.20	0.18[a], 0.33[b], 0.2[c],
		0.2[d], 0.21[e], 0.2283[f],
		0.2[g], 0.23[h]
$m^\star_\Gamma(\Gamma \to A)$	0.18	0.20[a], 0.27[b],
		0.1846[f], 0.19[h]
$m^\star_A(A \to \Gamma)$	–0.54	
$m^\star_A(A \to H)$	0.37	
$m^\star_U(U \to L/M)$	0.33	0.442[a], 0.285[b], 0.25[c]
$m^\star_L(L \to H)$	0.32	
$m^\star_L(L \to A)$	1.02	
$m^\star_A(A \to L)$	0.37	
c_s^{LA} ($\Gamma \to A$)	7930	7641[c], 6600[i]
c_s^{TA} ($\Gamma \to A$)	3994	4110[c], 2700[i]

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[a]Ref. [119], LDA
[b]Ref. [120], LCAO
[c]Ref. [114], EPM
[d]Ref. [121]
[e]Ref. [122]
[f]Ref. [100], EPM
[g]Ref. [117], Expt
[h]Ref. [123], LMTO
[i]Ref. [124]

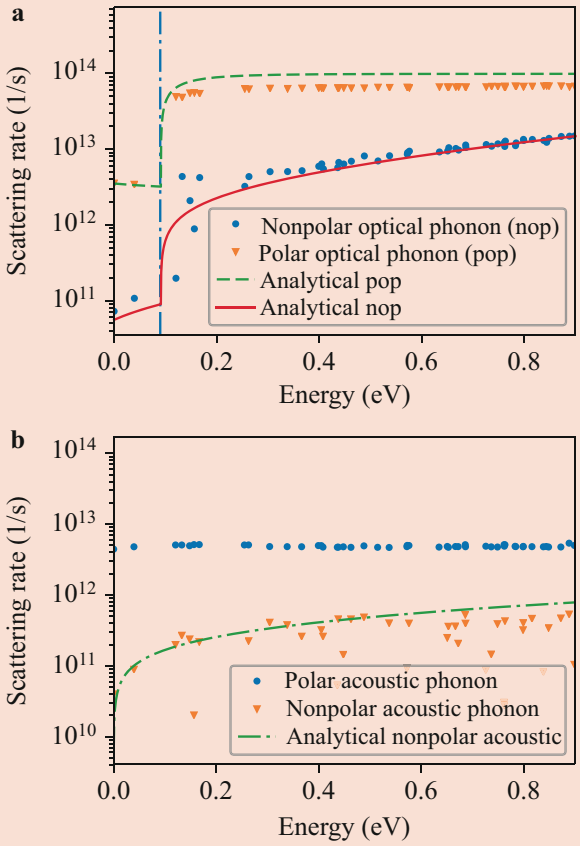

Fig. 42.7 Room-temperature (300 K) polar and nonpolar scattering rates with optical (**a**) and acoustic phonons (**b**) in wurtzite GaN calculated from first principles. A fine q-mesh of 80×80×80 and a Gaussian smearing of 0.1 eV are used in the calculations. The scattering rates calculated using analytical formula are also shown in (**a**) and (**b**). The fitting parameters are given in the text. (After J. Fang et al. [133], with permission from the American Physical Society ©2019 American Physical Society)

potential of 3.8×10^8 eV/cm. Such analytic expressions are a convenient way to simplify transport calculations when one wished to avoid the use of full-band Monte Carlo simulations. A similar analytic formula – that approximates quite well the DFT results – can be found to approximate the polar scattering rate with longitudinal optical (LO) phonons using the conventional Fröhlich expression [126] assuming a static relative dielectric constant of 8.9 and a high-frequency relative dielectric constant of 5.35 [127].

Figure 42.8 shows the low-field and high-field transport characteristics along the Γ-K symmetry line in the basal plane. These have been obtained by solving the Boltzmann transport equation with the full-band Monte Carlo method outlined in Sect. 42.3.4 with first-principles band structure and electron-phonon scattering rates. Our simulation results show a very high peak of the drift velocity of about 2.8×10^7 cm/s. Figure 42.8 also shows the average electron en-

ergies as a function of the homogeneous electric field. For electric fields smaller than 150 kV/cm, the average electron energies are close to the thermal energy. Above 150 kV/cm, the average electron energy increases sharply. It increases slowly again when the field strength exceeds 500 kV/cm. The evolution of the particle valley occupancy is the underlying reason for the trend. The trend shown here is similar to the results from the multi-valley Monte Carlo simulation results [124, 128].

The distribution of MC particles occupying the first and the second conduction bands in the first Brillouin zone is shown in Fig. 42.9 for a given electric field strength of 800 kV/cm. For particles (representing electrons) occupying the first conduction band, most of the particles are located around the Γ-valley with momenta exhibiting a noticeable drift along the reverse direction of the applied electric field, with a few particles located around the 12 satellite U-valleys. For particles occupying the second conduction band, most particles are distributed along the Γ-A symmetry line. Some particles occupy also the L-valleys. The particle occupation of the valleys is consistent with their energy splitting from the conduction band minimum. A two-dimensional plot in the $(k_x - k_y)$ basal plane is given for the convenience.

AlN

As we have done in the case of GaN, we show in Fig. 42.10a the band structure of the wurtzite AlN. Similarly, we list in Table 42.1 the conduction band energies of several satellite valleys. The experimental lattice constants of wurtzite AlN used in the calculations are $a = 3.110$ Å and $c = 4.980$ Å [127]. Table 42.3 lists the electron effective masses in different valleys of the lowest conduction band, compared with previous results [100, 119, 120, 123, 129]. Also in this case, the results obtained from DFT are in satisfactory agreement with the available experimental information. Note that for the first conduction band at the Γ-point, the effective mass is close to an isotropic value of 0.31 m_0, the same value used by Albrecht et al. [129]. From experimental measurements, it has been estimated that the electron effective mass ranges from 0.233 m_0 to 0.336 m_0 [130]. The effective mass for the second conduction band at Γ is 0.36 m_0.

Figure 42.10b illustrates the phonon dispersion. The LO energy at Γ-valley is ∼110 meV. The longitudinal and the transverse acoustic-phonon sound velocities are 10,877 m/s and 5880 m/s, respectively, listed in Table 42.3. Figure 42.11a

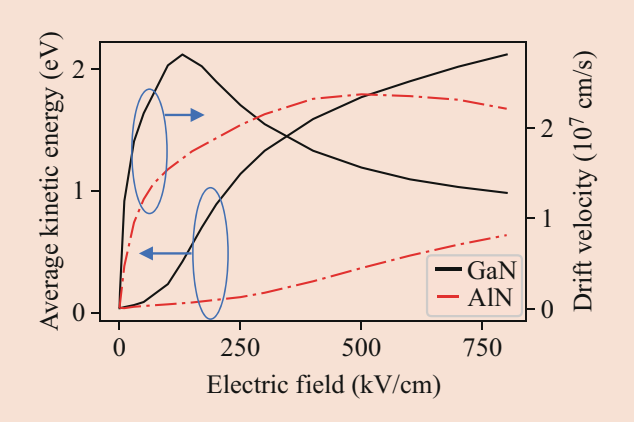

Fig. 42.8 Characteristics of the electric field versus average electron kinetic energy (left axis) and versus drift velocity (right axis) for wurtzite GaN and AlN along the Γ-K high symmetry line in the basal plane. The data for GaN are plotted with solid black lines and the data for AlN are plotted with dot-dashed red lines. (After J. Fang et al. [133], with permission from the American Physical Society ©2019 American Physical Society)

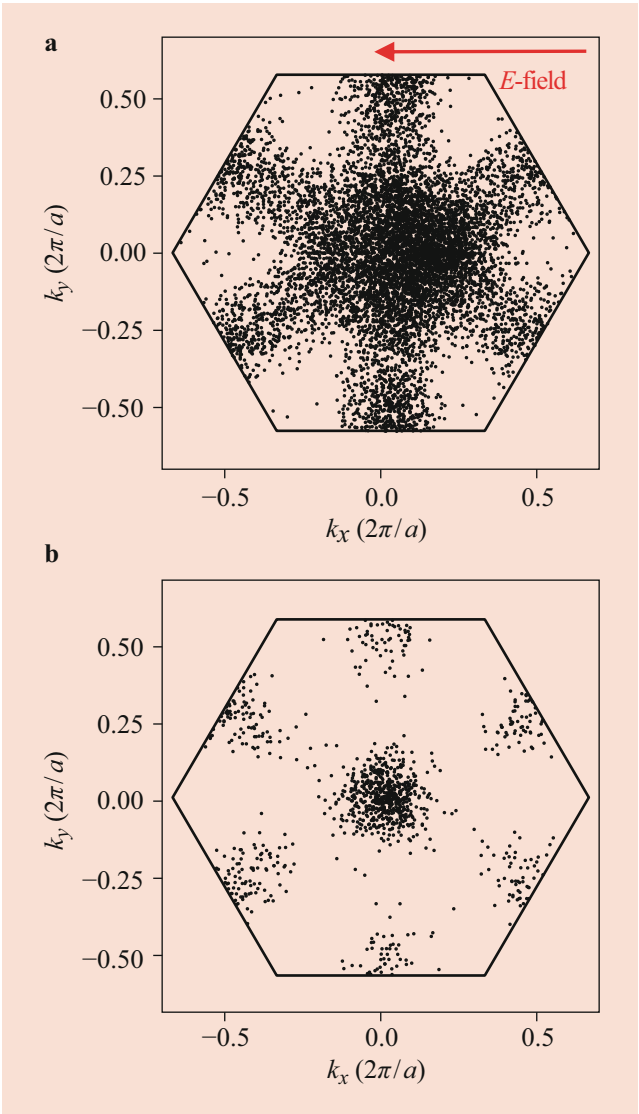

Fig. 42.9 Simulated distribution of MC particles occupying the first conduction band (**a**) and the second conduction band (**b**) of wurtzite GaN shown in reciprocal space for an electric field strength of 800 kV/cm. (After J. Fang et al. [133], with permission from the American Physical Society ©2019 American Physical Society)

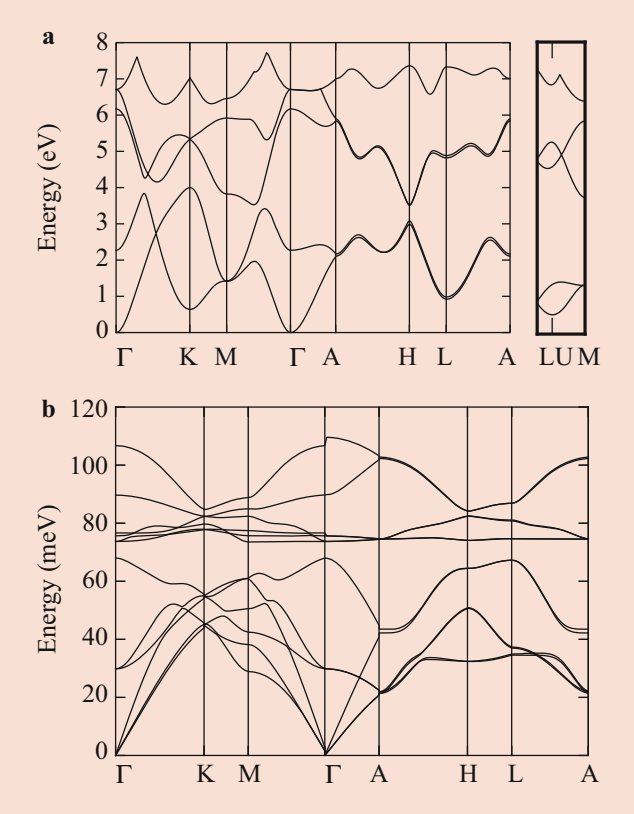

Fig. 42.10 (**a**) The energy dispersion of the first five conduction bands along several high symmetry lines of wurtzite AlN. (**b**) Full phonon dispersion along several high symmetry lines of wurtzite AlN. (After J. Fang et al. [133], with permission from the American Physical Society ©2019 American Physical Society)

Table 42.3 Electron effective mass (in units of the free electron mass m_0) along different crystalline directions at the first conduction band of different valleys and acoustic phonons′ sound velocities (in units of m/s) of AlN

	This work	Other work
$m^\star_\Gamma(\Gamma \to K)$	0.31	0.42[a]
$m^\star_K(K \to \Gamma)$	0.64	0.54[b], 0.488[c]
$m^\star_K(K \to M)$	0.65	0.54[b]
$m^\star_M(M \to K)$	0.25	0.629[c]
$m^\star_M(M \to \Gamma)$	1.20	
$m^\star_\Gamma(\Gamma \to M)$	0.31	0.40[a], 0.31[b], 0.26[c],
		0.35[d], 0.25[e], 0.3433[f]
$m^\star_\Gamma(\Gamma \to A)$	0.33	0.33[a], 0.35[b],
		0.33[e], 0.2938[f]
$m^\star_A(A \to \Gamma)$	−0.64	
$m^\star_A(A \to H)$	0.55	
$m^\star_U(U \to L/M)$	0.43	0.39[a], 0.495[c]
$m^\star_L(L \to H)$	0.40	
$m^\star_L(L \to A)$	0.89	
$m^\star_A(A \to L)$	0.55	
$c_s^{LA}(\Gamma \to A)$	10,877	
$c_s^{TA}(\Gamma \to A)$	5880	

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[a]Ref. [120], LCAO
[b]Ref. [129]
[c]Ref. [114], EPM
[d]Ref. [123], LMTO
[e]Ref. [119], LDA
[f]Ref. [100], EPM

presents the first-principles scattering rates for polar and nonpolar scattering with optical phonons. Figure 42.11a presents both polar and nonpolar scattering with acoustic phonons. We have used a Gaussian smearing of 0.1 eV to deal with the energy-conserving Dirac-delta functions. Interestingly, the rate for polar scattering with acoustic phonons is of the same order of magnitude as the rate for polar scattering with optical phonons for electrons with energies below 110 meV. Above 110 meV, the polar scattering rate with optical phonons is about ten times larger than the piezoelectric scattering rate. The scattering rates calculated from the analytical formula are also plotted in Fig. 42.11a, b. In order to fit these rates to the DFT results, we have used a relative static dielectric constant of 9.14 and a high-frequency relative dielectric constant of 4.84 for polar scattering with optical phonons [131]. Using a nonparabolicity factor of 0.35 eV^{-1}, we have obtained an "effective" nonpolar acoustic deformation potential of 7.0 eV and a nonpolar optical deformation potential of 1.32×10^9 eV/cm.

The velocity-field and average carrier energy-field characteristics are compared in Fig. 42.8 with those of GaN. An electron mobility of ∼450 $cm^2/(V \cdot s)$ at room temperature is extracted from the low electric field region. Taniyasu et al. have measured a room-temperature electron mobility of 426 $cm^2/(V \cdot s)$ for n-type AlN with Si doping concentration of 3×10^{17} cm^{-3} [132]. The peak drift velocity of AlN is smaller than that of GaN, and the corresponding critical field is larger. This is due to the heavier Γ-valley effective mass of AlN and also the smaller U-valley minima. We show in Fig. 42.12 the occupation of electrons at the first and the second conduction bands in reciprocal space at the field strength of 800 kV/cm. Particles populating the Γ-valley exhibit the expected momentum shift along the reverse direction of the electric field. The occupation of the satellite U- and K-valleys is larger in AlN than in GaN, a result of the smaller energy splitting from the conduction band minimum. The L-valleys and the M-valleys in the second conduction band are also occupied at large electric fields.

As "dry" as they may be, the approach and result that we have presented in this section – discussed in more detail in Ref. [133] – hopefully will shed some light on the still open issue of the energy of the satellite L-valleys in GaN, on the role of Auger recombination and its inverse process, impact ionization, in power devices based on group-III/nitrides semiconductors. The uncertainty (and controversy) we have

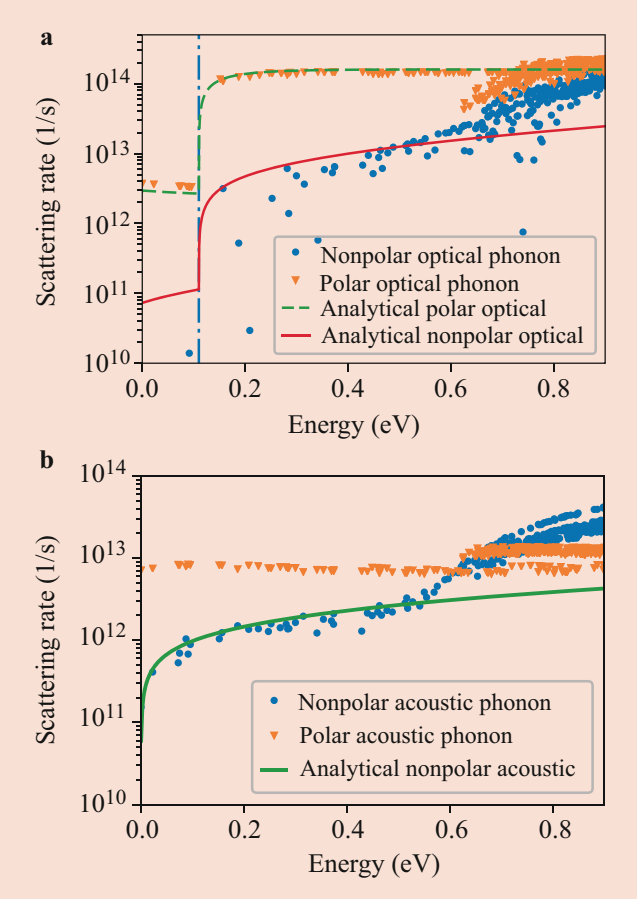

Fig. 42.11 Room-temperature (300 K) polar and nonpolar scattering rates with optical (**a**) and acoustic phonons (**b**) in wurtzite AlN calculated from first principles. A fine q-mesh of 40 × 40 × 40 and a Gaussian smearing of 0.1 eV are used in the calculations. (After J. Fang et al. [133], with permission from the American Physical Society ©2019 American Physical Society)

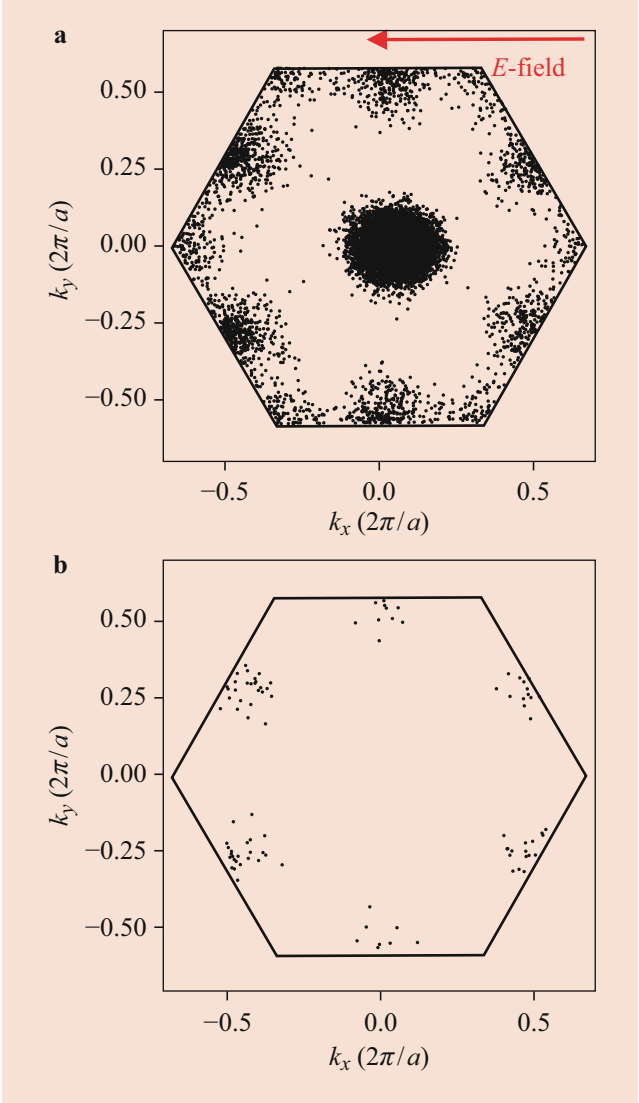

Fig. 42.12 For AlN, the distribution of MC particles on (**a**) the first conduction band and (**b**) the second conduction band of AlN in reciprocal space at an electric field strength of 800 kV/cm. (After J. Fang et al. [133], with permission from the American Physical Society ©2019 American Physical Society)

mentioned at the beginning of this section hints at a more general issue that we shall discuss in Sect. 42.7, namely, the accuracy and reliability of *ab initio* methods in guiding us when dealing with electronic transport.

42.4.3 2D Materials

Since the first isolation of graphene [5], two-dimensional materials have attracted considerable interests not only for the unusual physical properties that some of them exhibit (topological properties, such as quantum spin Hall effect, or superconductivity, for example) but also since extremely thin channels are required in order to continue the never-ending scaling of semiconductor devices. Therefore, in this section we consider some of these 2D materials and see what information *ab initio* methods can give us about their charge-transport properties and assess which of them – if any – could be used as the active channel material in ultra-scaled transistors or which of their unique properties could be exploited. We limit our attention mostly to homogeneous electronic transport (low-field mobility and high-field velocity and energy characteristics) in some of the popular 2D materials such as phosphorene, silicene, and germanene, calculated by full-band synchronous ensemble Monte Carlo method using the *ab initio* methods described above. We shall consider devices only cursorily, looking at a 10 nm gate-length phosphorene-based field-effect transistor (FET), to show the final connection that it is now possible to make between DFT and device characteristics.

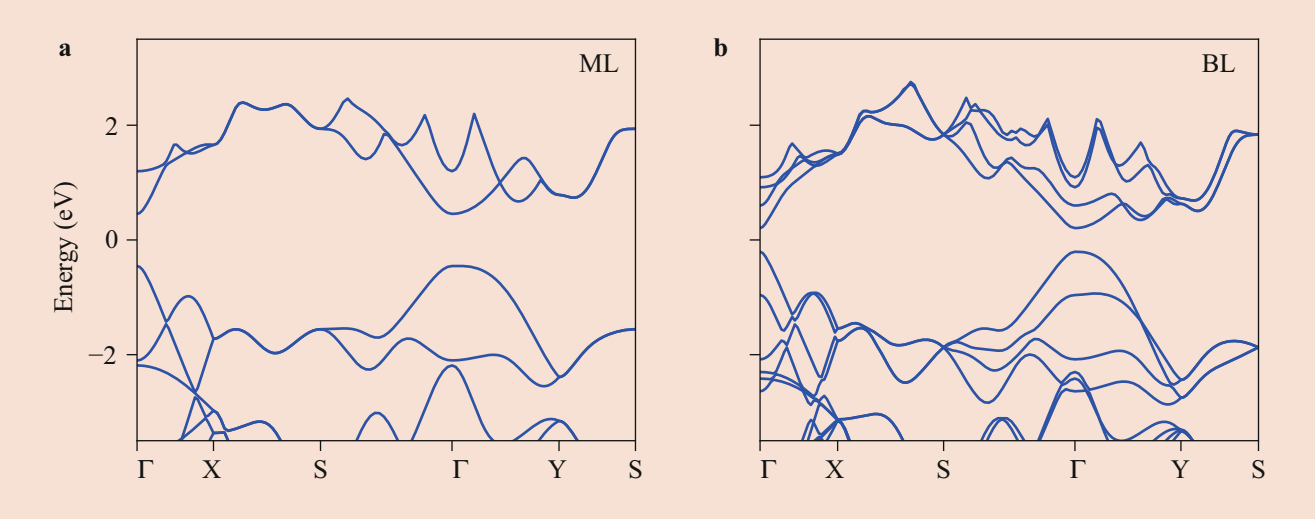

Fig. 42.13 The band structure of (**a**) monolayer phosphorene and (**b**) bilayer phosphorene calculated using VASP

Phosphorene

Phosphorene, mono- or few-layer black phosphorus, has gained wide interest due to high electron mobility observed in its bulk counterpart [134,135]. In this section, we present the results of low- and high-field electron/hole transport studies in monolayer and bilayer phosphorene. Reference [97] provides a more detailed description on transport calculations for phosphorene.

Single layers of black phosphorus, phosphorene, have a puckered honeycomb structure with a rectangular Brillouin zone. We show in Fig. 42.13 the electronic band structures for monolayer and bilayer phosphorene, calculated using the Vienna *ab initio* simulation package (VASP) [11–14], plotted along symmetry lines. VASP uses using projector-augmented wave (PAW) [136] pseudopotentials, and we have employed the Perdew-Burke-Ernzerhof generalized gradient approximations (PBE-GGA) [94] for the exchange-correlation functional. The relaxed lattice constants obtained are 4.62 Å and 3.30 Å for monolayers and 4.51 Å and 3.30 Å for bilayers. A direct band gap of 0.91 eV and 0.51 eV at the Γ symmetry point is obtained for mono- and bilayer. These values are lower than experimental values [137–139]. This is to be expected, since DFT is known to underestimate the band gap. However, this is not going to affect significantly our calculations since here we do consider inter-band transitions between the valence and conduction bands. The band structure of phosphorene exhibits also two additional valleys, the so-called Q and Y satellite valleys, along the Γ – Y symmetry direction. At high fields and large doping densities, electrons tend to populate these valleys. The calculated effective masses for both electrons and holes in monolayers and bilayers at Γ are shown in Table 42.4. Both the valence and the conduction bands are anisotropic with a smaller effective mass along the armchair direction. The electron energy and velocity are calculated on a fine mesh around the Γ symmetry point (145×205 **k** points in the first quadrant) in order to account for the anisotropy and nonparabolicity of the electron dispersion.

Table 42.4 Calculated effective masses, m_Γ^e and m_Γ^h, in monolayer and bilayer phosphorene

	m_Γ^e		m_Γ^h	
	Armchair	Zigzag	Armchair	Zigzag
ML	0.14	1.24	0.14	N/A
BL	0.10	1.33	0.09	3.08

After G. Gaddenane et al. [97], with permission from the American Physical Society ©2018 American Physical Society

We have calculated the phonon dispersion curves for monolayer and bilayer phosphorene calculated using the PHONOPY computer program [140]. In Fig. 42.14 we show the resulting dispersion along symmetry lines. One feature that is clearly evident in that figure – and that is common to all 2D materials – is the parabolic dispersion of the out-of-plane acoustic phonons, the flexural modes usually called ZA phonons. The effect of these phonons on carrier transport is detrimental in some of the 2D materials, such as silicene and germanene, that lack horizontal mirror (σ_h) symmetry [141]. However, in the case of phosphorene, the electron/hole-ZA phonon coupling is forbidden at the first order. Comparing the phonon dispersion of bilayers (Fig. 42.14b) with that of monolayers (Fig. 42.14a), we note the presence of low energy optical modes in bilayers. These are interlayer mode which are caused by weak interlayer coupling of entire unit cells in different layers that oscillate out-of-phase along either the in-plane (LO, TO) or out-of-plane (ZO) direction. Obviously, their low energy is due to the heavy mass of the entire unit cells that oscillate.

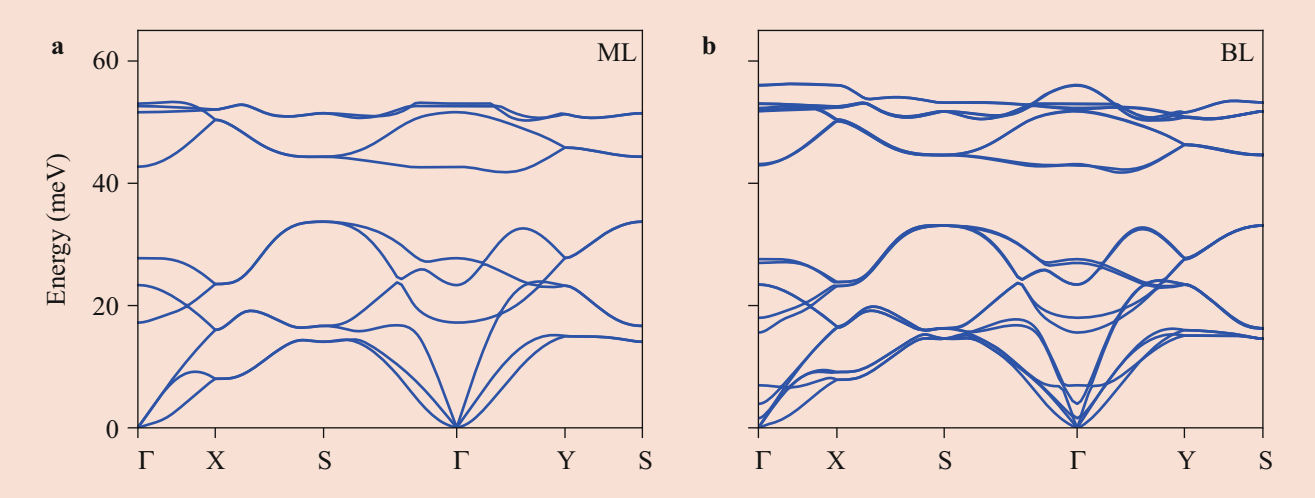

Fig. 42.14 The phonon dispersion for (**a**) monolayer phosphorene and (**b**) bilayer phosphorene calculated using PHONOPY

Figure 42.15 shows the angular average of the electron/hole-phonon scattering rate as a function of carrier kinetic energy for monolayer and bilayer phosphorene. The matrix elements are evaluated following the finite-displacement method described above. These are calculated on a very fine mesh to account for the angular dependence and wavefunction overlap effects. This is a crucial consideration, since failure to do so has shown to give inaccurate scattering rates and to overestimate the carrier mobility. Indeed, this is one of the main causes of the large discrepancy (μ_e = 20–26,000 $cm^2V^{-1}s^{-1}$) among the mobility values present in the literature [97, 137, 142–145]. Such a strong angular dependence is shown in Fig. 42.16. As we have just mentioned, in 2D materials with horizontal mirror symmetry (σ_h-symmetric crystal), scattering of electrons/holes with the ZA phonons is forbidden at first order [141]. Therefore, this process can be ignored in the case of phosphorene, a σ_h-symmetric crystal. In monolayers, in-plane acoustic modes dominate the intravalley scattering processes with a strong backward scattering for electrons (Fig. 42.15a), and optical modes for holes (Fig. 42.15b). For electrons, intervalley scattering between Γ and Q is dominated by the 32 meV optical phonon which has a rather large deformation potential of 1.7×10^9 eV/cm. On the contrary, in bilayers in-plane acoustic modes and low-energy interlayer optical phonons dominate the intravalley scattering processes for both electrons and holes (Fig. 42.15c, d), and the 32 meV optical phonon dominates intervalley scattering for electrons. We should remark that, due to the low energy of these interlayer modes and to the numerous "band crossings" among themselves and with acoustic modes, it is difficult to separate clearly their contribution from the contribution of the acoustic modes.

Table 42.5 lists the calculated low-field carrier mobility for mono- and bilayer phosphorene in the armchair and zigzag direction. When the electron/hole-phonon matrix elements calculations are treated correctly by accounting the angular dependence, including wavefunction overlap effects, including scattering by all phonon modes and intra- and intervalley processes, the mobility obtained is on the lower end of the range of values present in the literature. In both mono- and bilayers, the carrier mobility is larger along the armchair direction compared to zigzag direction due to lower effective mass along the armchair direction. The carrier mobility does not change significantly going from monolayers to bilayers. In fact, the hole mobility decreases slightly.

Figures 42.17 and 42.18 show the velocity-field and energy-field characteristics for electrons and holes in monolayer and bilayer phosphorene. The carrier mobility for electrons and holes obtained from the velocity-field characteristics along the armchair and zigzag directions is in good agreement with the value obtained from the diffusion constant. The saturated velocity for electrons in both mono- and bilayers is relatively low (4×10^6 cm/s in the armchair direction and 1×10^6 cm/s in the zigzag direction) because of strong intervalley transfer of electrons from the Γ to the Q and Y valleys (Fig. 42.19). For holes, the velocity does not saturate in the zigzag direction even at high fields due to extremely low hole mobility along that direction (Figs. 42.17b and 42.17d). The average carrier energy for electrons remains close to the thermal energy (≈25 meV) up to a field of 10^5 V/cm for both monolayers and bilayers (42.18). However, the Ohmic regime extends to higher fields, especially in the case of holes accelerated along the zigzag direction, because of extremely low mobility along that direction (Fig. 42.18b, d).

Finally, we show in Fig. 42.20 the structure and current-voltage characteristics of a double-gate FET with a phosphorene channel, a 10 nm gate length, assuming Al_2O_3 as top and bottom oxide with an equivalent oxide thickness

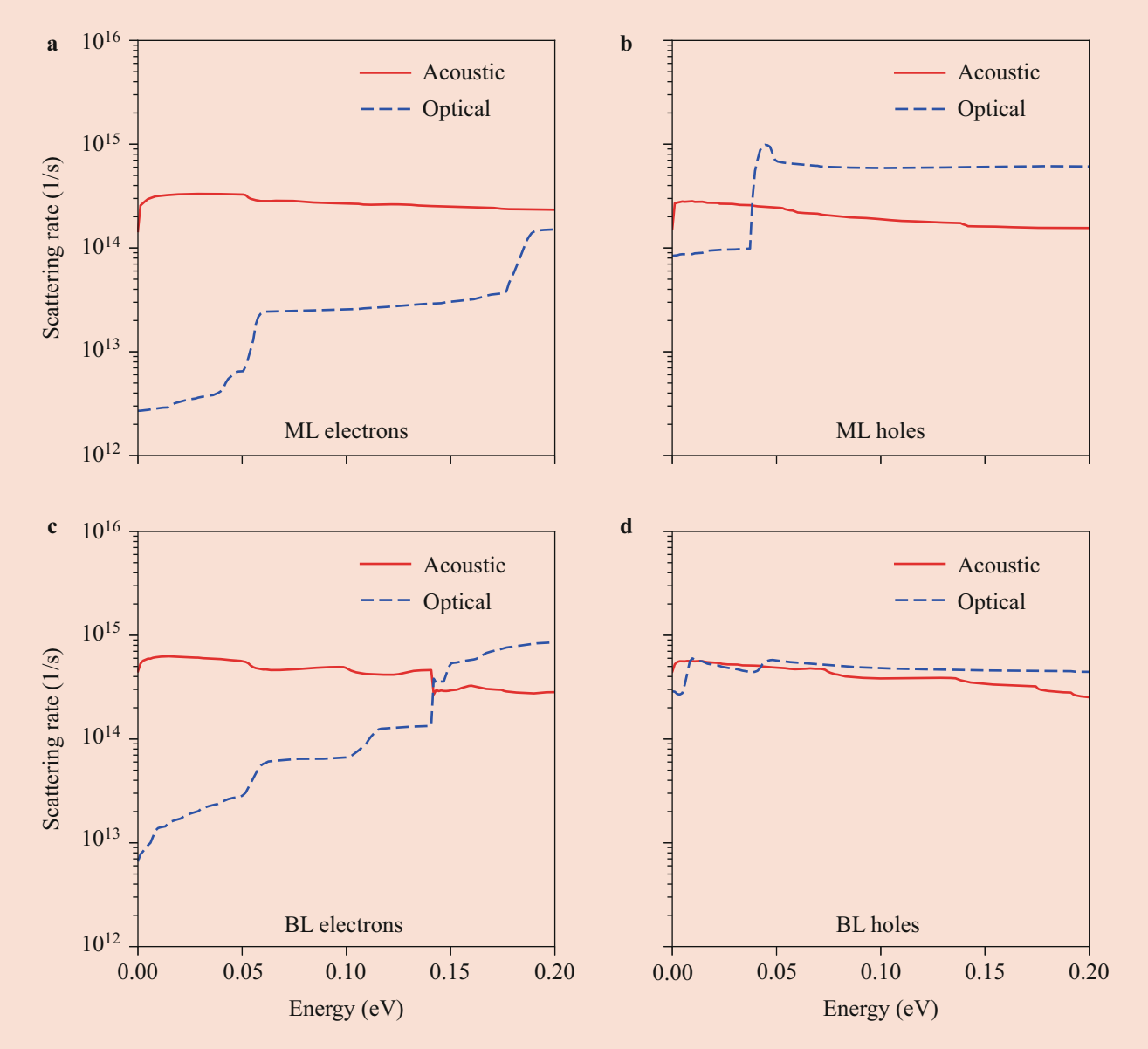

Fig. 42.15 Electron-phonon (left frames, (**a**) and (**c**)) and hole-phonon (right frames, (**b**) and (**d**)) scattering rates for monolayer phosphorene in (**a**) and (**b**), for bilayer phosphorene in (**c**) and (**d**), at 300 K, where the matrix element is obtained from VASP

(EOT) of 0.7 nm. Despite the poor mobility we have calculated for free-standing intrinsic monolayers, the performance of the device is satisfactory: an excellent I_{on}/I_{off} ratio of about 10^4, a transconductance g_m exceeding 1600 μS/μm at $V_{DD} \approx 0.5$ V, a subthreshold slope of 60–70 mV/decade, and a drain-induced barrier lowering (DIBL) of 10 mV/V. Only the on current fails to meet the latest target of the International Technology Roadmap for Semiconductor (ITRS) [146]. Indeed, the mobility is only one of the many factors that control the performance of a device, especially since at the nanoscale transport approaches the ballistic limit. Moreover, the mobility may increase at high carrier density, (thanks to dielectric screening by the free carriers and Pauli blocking), thus minimizing the negative effects of a high resistance in the source and drain regions.

Silicene and Germanene

Monolayer silicon (silicene) and germanium (germanene) have gained wide interest due to the tremendous role played by these semiconductors in their bulk form in the semiconductor industry in the last several decades. In this section we present the results of electron transport in these materials in monolayer form, following the procedure described above. Reference [147] provides for a more detailed description on how transport calculations have been performed to study these materials using first-principles methods.

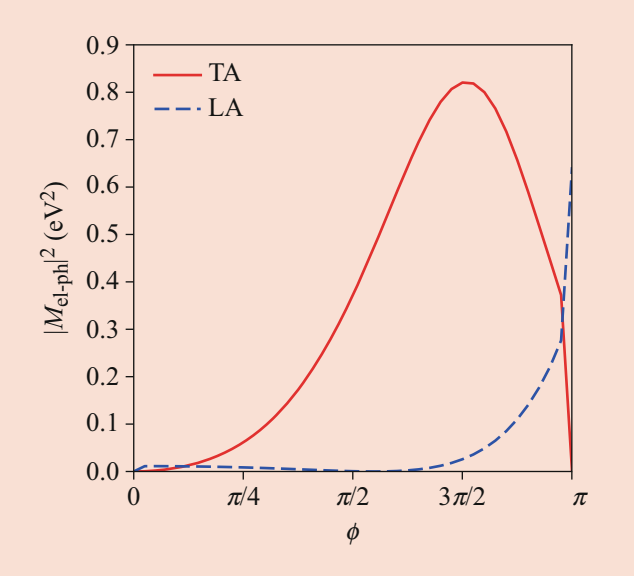

Fig. 42.16 Acoustic electron-phonon matrix element for electrons plotted for an initial and final electron kinetic energies ≈40 meV as functions of the angle ϕ of the final wave vector $\mathbf{k}'$ with respect to the armchair direction. The initial wave vector $\mathbf{k}$ is taken to be along the armchair direction

Figures 42.21 and 42.22 show the electronic band structure and phonon dispersion for ideal free-standing silicene and germanene, calculated by DFT using the VASP and PHONOPY packages. Similar to graphene, both these materials exhibit a Dirac-like electronic dispersion. However, the Fermi velocities we have obtained for silicene (≈5.3×10^7 cm/s) and germanene (≈5.3×10^7 cm/s) are lower than in graphene (≈9.5×10^7 cm/s), and, unlike graphene, their structures are buckled. The lattice and buckling constants we have obtained are 3.86 Å and 0.48 Å for silicene and 4.05 Å and 0.71 Å for germanene, respectively. Furthermore, our calculations were performed by neglecting the contributions of spin-orbit (SO) coupling for computational efficiency. This should not be a source of any major concern, since it has been shown that the SO interaction opens a rather small band gap in these materials (about 1.5 meV for silicene [148–150] and 25 meV for germanene [148, 149]). Given these small values, the effect of the SO interaction on the transport properties should be negligible for silicene and would result only in a slight overestimation of the mobility and drift velocity in germanene. We have chosen a supercell of size 5×5×1 unit-cells when calculating the phonon spectra, in order to avoid nonphysical "negative frequencies" (in reality, imaginary frequencies) of the low-energy acoustic phonons. Often these negative (square)frequencies are interpreted as a sign of the thermodynamic instability of the crystal, but in many cases they are simply the result of numerical artifacts when cells of excessively small dimensions are used to speed up

Table 42.5 Calculated electron and hole mobility, μ_e and μ_h, in monolayer and bilayer phosphorene

	μ_e cm^{2}V^{-1}s^{-1}		μ_h cm^{2}V^{-1}s^{-1}	
	Armchair	Zigzag	Armchair	Zigzag
ML	20	10	19	2.4
BL	14	7	12	2

Adapted from G. Gaddenane et al. [97], with permission from the American Physical Society ©2018 American Physical Society

the calculations. In Fig. 42.22 the various phonon branches are labeled only for convenience; such an identification of the various branches (acoustic or optical, longitudinal or transverse) should be interpreted with a grain of salt, since these branches are often somewhat mixed, and such a distinction is physically unjustified for wave vectors at the edge of the Brillouin zone.

Figure 42.23 shows the electron-phonon scattering rates for silicene and germanene calculated at 300 K. The lack of horizontal mirror (σ_h) symmetry in these materials results in a very strong coupling, in principle diverging, with the long wavelength flexural (ZA) phonons [141]. This effect is further enhanced by the Dirac-like dispersion which causes strong back scattering, effect that is due to the degeneracy of the valence and conduction band at the K symmetry point. In the absence of a process which suppresses the ZA phonons, the resulting mobility in these materials is extremely low (10^{-3} to 10^{-2} cm^2/V·s). In the calculations presented here, we have assumed a long wavelength cutoff of 1 nm for the ZA phonons to avoid the divergence. The cutoff is chosen such that intravalley scattering is suppressed and intervalley scattering is included. In both silicene and germanene, scattering with ZA and LA phonons dominates the scattering, in particular the K-K′ intervalley process.

Without delving too deeply into the extremely interesting problem of assessing which mechanism may suppress, or at least damp, the first-order interaction (one-phonon processes) with the ZA modes (issue discussed in detail in Ref. [141]), we should mention that, besides obvious effects like the finite grain-size and the rippling or crumpling of the layer, their anharmonic coupling to in-plane acoustic modes [151–154] has been shown to renormalize their dispersion from a square (quadratic) law to a power-law of the form q^r, with r being approximately 3/2. Moreover, in supported and/or gated layers, Amorim and Guinea [155] have shown that at long wavelengths the renormalized dispersion of the ZA phonons, $\tilde{\omega}^{(ZA)}(q)$, approaches a nonzero constant, taking the form $\tilde{\omega}^{(ZA)}(q) \sim \sqrt{\omega^{(ZA)}(q)^2 + \omega_0^2}$, where $\omega^{(ZA)}(q)$ is the dispersion in free-standing layers and $\omega_0 \approx \sqrt{g/\rho_{2D}}$, ρ_{2D} being the mass density of the 2D layer and g is a measure of the strength of the coupling between the layer and the substrate (or gate insulator). Typically, $\hbar\omega_0$ is of the order of a few meV, small but nonzero, which is what matters. These considerations, all derived in the continuum limit, solve the

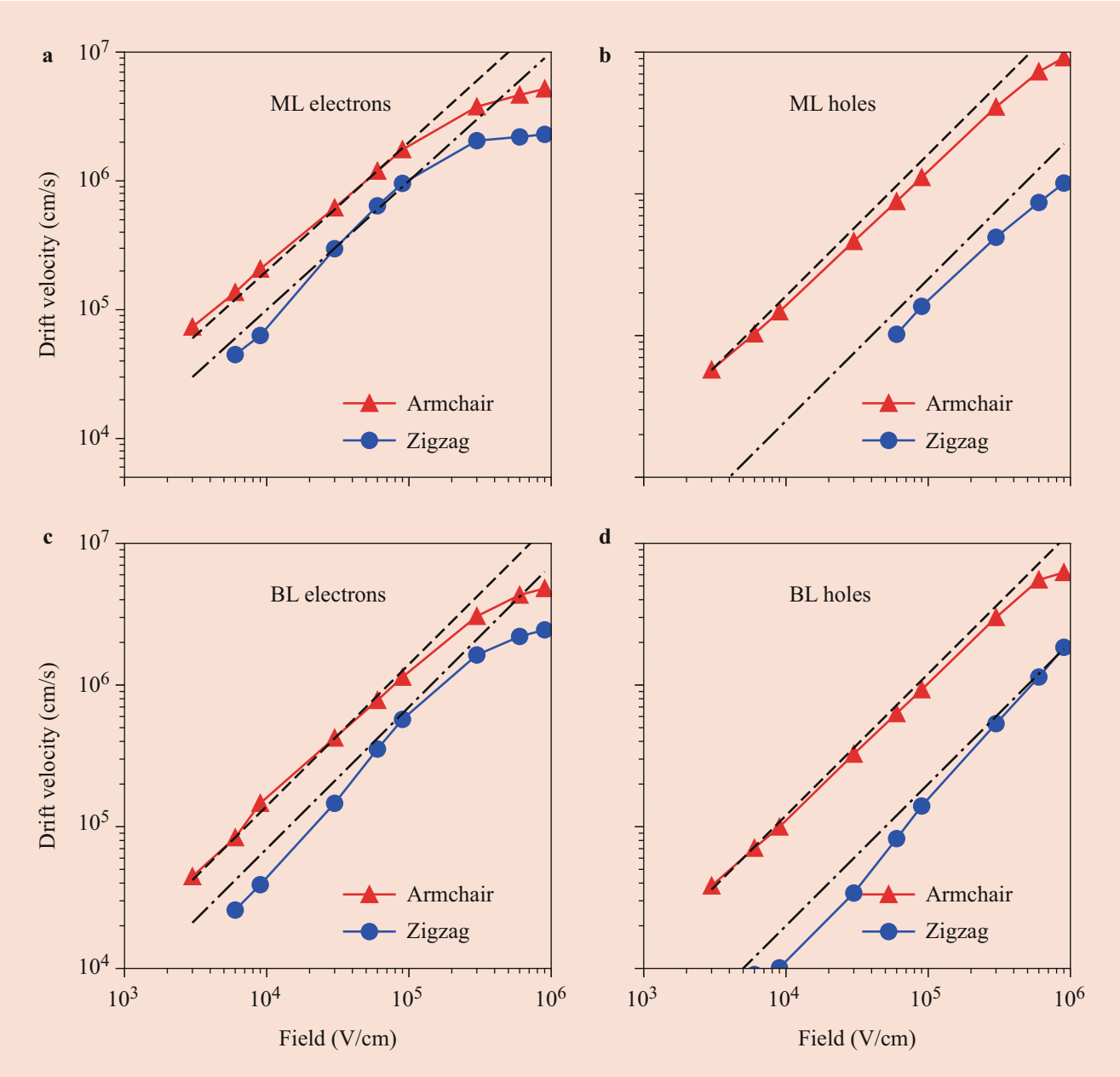

Fig. 42.17 Drift velocity *vs* field at 300 K for electrons (left frames, (**a**) and (**c**)) and holes (right frames, (**b**) and (**d**)), in monolayer phosphorene (**a**) and (**b**), and bilayer phosphorene (**c**) and (**d**)

Mermin-Wagner puzzle [156] but do not necessarily result in a negligible role of the ZA phonons in depressing the carrier mobility. In particular, even accounting for the emergence of a gap in supported and/or gated layers, the coupling with the Rayleigh waves of the substrate and/or gate [155, 157] may still play a huge role. Recently, Rudenko et al. [158] have concluded that even in nonsymmetric materials with a parabolic dispersion, the effect is small, amounting to no more than a 35% reduction of the mobility due to second-order interactions (two-phonon processes), arguing that even in this case the first-order coupling of the carriers to the acoustic flexural modes is forbidden by the rotational symmetry of the crystal. However, these conclusions are reached by approximating the 2D layer as a membrane of zero thickness, thus ignoring the "internal structure" of the membrane, an effect that may result in the breaking of the rotational and inversion symmetry of a non-σ_h-symmetric membrane. The situation is even less clear in the case of non-σ_h-symmetric materials with a Dirac-like electronic dispersion, like silicene and germanene.

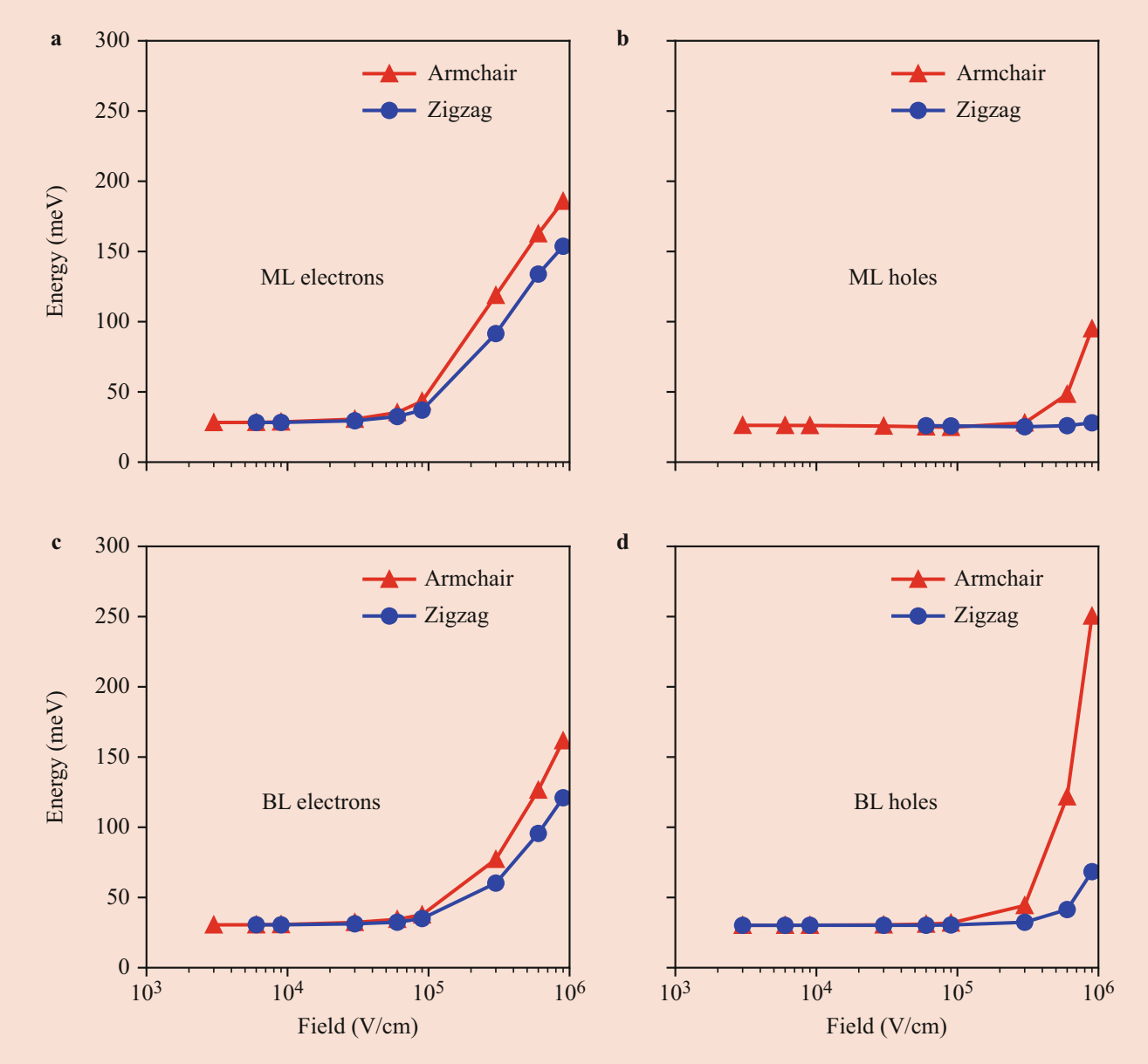

Fig. 42.18 Energy *vs.* field at 300 K for electrons (left frames, (**a**) and (**c**)) and holes (right frames, (**c**) and (**d**)), in monolayer phosphorene (**a**) and (**b**), and bilayer phosphorene (**c**) and (**d**)

Table 42.6 lists the electron mobility calculated along the [01] direction (Γ-K) for various scattering processes from the diffusion constant. With a 1 nm ZA phonon cutoff, the calculated electron mobility is 701 $cm^2/V{\cdot}s$ in silicene and 2327 $cm^2/V{\cdot}s$ in germanene. When we neglect scattering by ZA phonons completely, the mobility rises to 1296 $cm^2/V{\cdot}s$ and 4549 $cm^2/V{\cdot}s$, respectively. When intervalley scattering processes assisted by both LA and ZA phonons are ignored, the mobility increases by an order of magnitude.

Figure 42.24 shows the velocity-field and energy-field characteristics for silicene and germanene for an electric field applied along the [01] direction. The electron mobility extracted from the velocity-field characteristics is in agreement with the value obtained from the evaluation of the diffusion constant. At low fields, electrons remain thermal and exhibit Ohmic behavior in both materials. However, at higher fields, germanene exhibits negative differential mobility due to Γ-K intervalley scattering. Lower scattering rates and a smaller energy difference between the Dirac point K and the bottom of the Γ valley in germanene result in a significant transfer of electrons to the Γ valley, a lower velocity region. However, in silicene, we observe no significant population of the Γ valley due to large energy difference between the two valley minima, and we obtain a saturation velocity of $\approx 8 \times 10^6$ cm/s.

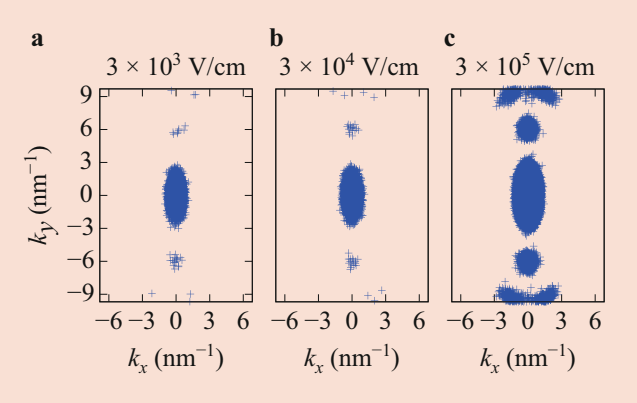

Fig. 42.19 Distribution in reciprocal space for electrons in monolayer phosphorene for a field of 3×10^3 (**a**), 3×10^4 (**b**), and 3×10^5 V/cm (**c**), along the armchair direction. Note the $\Gamma - Q$ intervalley transfer at center, the $\Gamma - Y$, and $Q - Y$ intervalley transfer at the highest field

This difference can be seen in Fig. 42.25, which compares the momentum distribution of electrons in silicene and germanene at high fields.

In summary, at least judging from the DFT results we have just reviewed, and at least in principle, silicene and germanene may exhibit satisfactory properties. However, understanding the role played by the acoustic flexural modes in determining their charge-transport behavior remains an open issue. Moreover, and probably more important, processing these materials (growth/deposition of the layers, their passivation, doping, and gating, formation of Ohmic contact, etc.) could constitute a formidable challenge.

42.5 Dielectric Response of Low-dimensional Materials

In Sect. 42.1, when outlining the content of this chapter, we mentioned the need to use a position-dependent dielectric constant (or function) when simulating nanoscale devices using atomistic models. Indeed, looking at the top frame of Fig. 42.20, a solution of Poisson equation requires the knowledge of the location of the interface between the 2D layers (for phosphorene a thin layer but still of a finite thickness) and the top and bottom insulators. When using conventional continuum models, approximating the location of this interface, the straight line drawn in the diagram will suffice. Not so when using atomistic models. In this case, the smooth transition between the dielectric and the 2D layer has to be resolved accurately. Moreover, a more intriguing question is how to define the dielectric constants (in plane and out of plane) of the 2D layer itself.

The case illustrated in Fig. 42.20 is only one example. Indeed, devices based on the many low-dimensionality nanomaterials of present interest, such as graphene nanoribbons

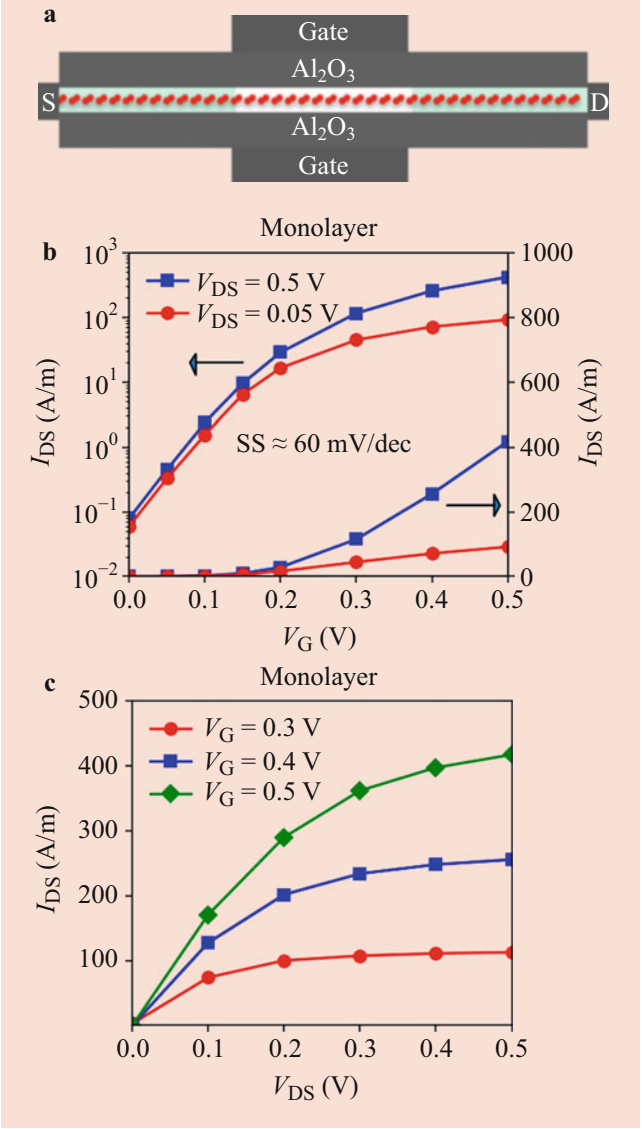

Fig. 42.20 (**a**) Schematic of the 10 nm gate-length phosphorene-based FET we have simulated. (**b**) Transfer characteristics of the device. (**c**) output characteristics of the device

[159], carbon nanotubes [160], silicon nanowires [161], graphene [5], silicene [162], phosphorene [163], and transition metal dichalcogenide (TMD) monolayers [164], all require this knowledge. Indeed, their dielectric properties determine macroscopic quantities, such as the gate capacitance and transconductance, and transport properties, as affected by dielectric screening and by the coupling of collective modes (plasmons) in the layers and insulators. However, the dielectric properties of these nanomaterials are not well studied, either experimentally or theoretically, compared with the bulk form of these materials. Different from the bulk materials which can usually be characterized by a single isotropic macroscopic dielectric constant if it has a

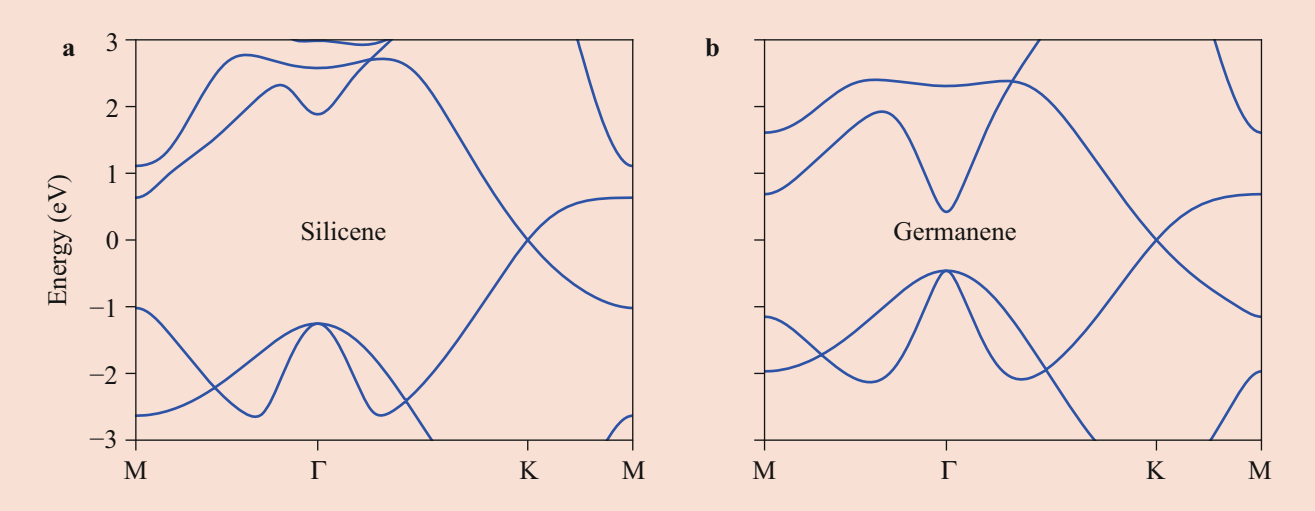

Fig. 42.21 The band structure of (**a**) silicene and (**b**) germanene calculated using VASP

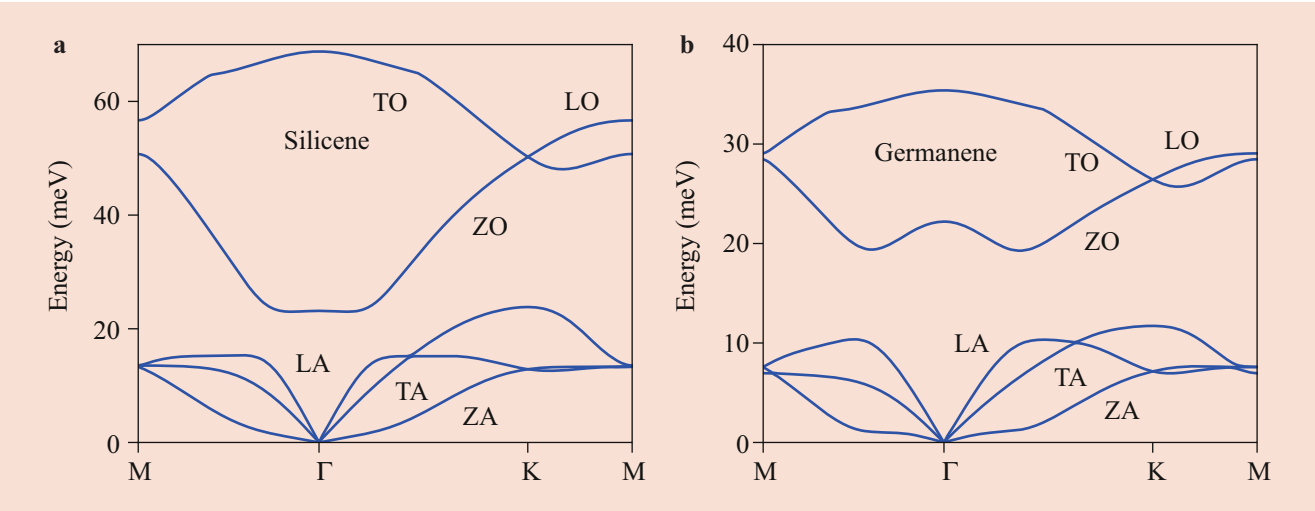

Fig. 42.22 The phonon dispersion of (**a**) silicene and (**b**) germanene calculated using PHONOPY

cubic crystal structure, low-dimensional nanomaterials are anisotropic by definition, and the study of their dielectric properties is more complex. Anisotropic tensorial dielectric properties are expected.

Here we shall outline how *ab initio* methods can provide the missing information. To keep the treatment simple and general, we shall consider only empirical pseudopotentials. Whereas this may be viewed as not a "first-principles" approach, the formalism can be extended to self-consistent pseudopotentials (DFT) in a straightforward way.

Several theoretical methods have been developed to study either the macroscopic or the microscopic dielectric response of nanosystems [165–176]. However, not much attention has been paid to the microscopic dielectric tensor of low-dimensionality nanomaterials. Therefore, here we present the derivation of a microscopic Poisson equation based on the density-density response function [177, 178] and its application to the study of these systems. We consider the particular case of the static dielectric properties of armchair-edge graphene nanoribbons (aGNRs) and graphene, but the method can be extended to other nanomaterials, such as Si nanowires (NWs, as illustrated in Fig. 42.30) and TMD monolayers (as recently reported by Laturia et al. using DFT [179]).

42.5.1 Density-Density Response Function

In the static linear response theory [177, 178, 180], the density-density response function, $\chi(\mathbf{r}, \mathbf{r}')$, describes the

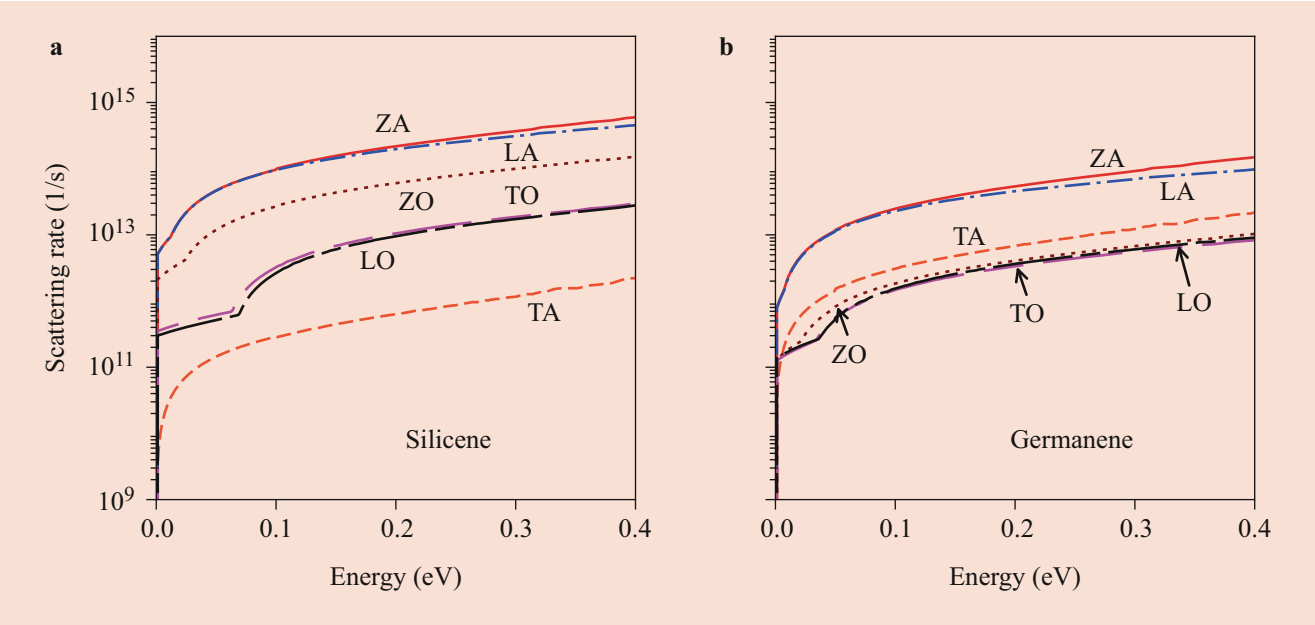

Fig. 42.23 Electron-phonon scattering rates for (**a**) silicene and (**b**) germanene per mode at 300 K, where the matrix elements are obtained from VASP

Table 42.6 Electron mobility in silicene and germanene in the [01] direction

	Silicene (germanene) ($cm^2V^{-1}s^{-1}$)
1 nm ZA phonon cutoff	$7.01 \times 10^2 (2.32 \times 10^3)$
Ignoring ZA phonons (intra- and intervalley)	$1.29 \times 10^3 (4.55 \times 10^3)$
Only intravalley with in-plane acoustic phonons	$4.3 \times 10^4 (2.6 \times 10^4)$
Only intervalley with acoustic phonons	$8.17 \times 10^2 (3.5 \times 10^3)$
Only optical phonons (intra- and intervalley)	$8.2 \times 10^3 (4.2 \times 10^4)$

After G. Gaddenane et al. [147], with permission from the American Institute of Physics ©2018 American Institute of Physics)

change of the charge density $e\delta\rho(\mathbf{r})$ when the external potential undergoes a small change, $\delta v_{\text{ext}}(\mathbf{r}')$, so that the electric polarizability (or "susceptibility") is $\chi(\mathbf{r},\mathbf{r}') = e\delta\rho(\mathbf{r})/\delta v_{\text{ext}}(\mathbf{r}')$. As an example, we first illustrate the independent-particle density-density response function $\chi^0(\mathbf{r},\mathbf{r}')$ of an armchair-edge graphene nanoribbon with a width given by seven atomic lines, here called a "7-aGNR." As mentioned above, in order to reduce the computational effort, we employ the local empirical pseudopotentials proposed by Kurokawa [181]. These pseudopotentials surprisingly yield the correct band structure of both sp^3-coordinated C in the face-center cubic phase(diamond) as well as sp^2-coordinated C, such as graphene [60]. The band structure of the ribbon has been calculated using a supercell size of 1.72 × 0.85 nm in the nonperiodic directions and an energy cutoff of 10 Rydberg, resulting in 2237 plane waves in the basis set. The static independent-particle polarizability matrix is then calculated as [180, 182, 183]:

$$\chi^0_{\mathbf{G}\mathbf{G}'}(\mathbf{q}) = \frac{4}{\Omega} \sum_{c,v,\mathbf{k}} \frac{\langle v,\mathbf{k}|e^{-i(\mathbf{q}+\mathbf{G})\cdot\mathbf{r}}|c,\mathbf{k}+\mathbf{q}\rangle\langle c,\mathbf{k}+\mathbf{q}|e^{i(\mathbf{q}+\mathbf{G}')\cdot\mathbf{r}'}|v,\mathbf{k}\rangle}{E^v_{\mathbf{k}} - E^c_{\mathbf{k}+\mathbf{q}}}, \tag{42.35}$$

using the eigenvalues $E^n_{\mathbf{k}}$ ($n = c, v$ for the conduction and valence bands, respectively) and eigenfunctions $|n,\mathbf{k}\rangle$ obtained from the calculation of the band structure. In Eq. (42.35), $\mathbf{G}$ and $\mathbf{G}'$ are reciprocal lattice vectors, $\mathbf{q}$ and $\mathbf{k}$ are the 2D vectors within the first Brillouin zone, and Ω denotes the crystal volume. In Eq. (42.35), the sum over the indices c and v denote the sum over all conduction and valence bands, respectively. The real-space susceptibility $\chi^0(\mathbf{r},\mathbf{r}')$ can be obtained by transforming $\chi^0_{\mathbf{G}\mathbf{G}'}(q_z \to 0)$:

$$\chi^0(\mathbf{r},\mathbf{r}') = \frac{1}{\Omega_{\text{cell}}} \sum_{\mathbf{G}\mathbf{G}'} e^{i\mathbf{G}\,\mathbf{r}} \chi^0_{\mathbf{G}\mathbf{G}'}(q_z \to 0) e^{-i\mathbf{G}'\mathbf{r}'}, \tag{42.36}$$

where Ω_{cell} is the volume of the supercell.

The screened response function, $P(\mathbf{r},\mathbf{r}')$, relates the induced charge, $e\rho_{\text{ind}}(\mathbf{r})$, to the total potential, $\varphi_{\text{tot}}(\mathbf{r})$, through:

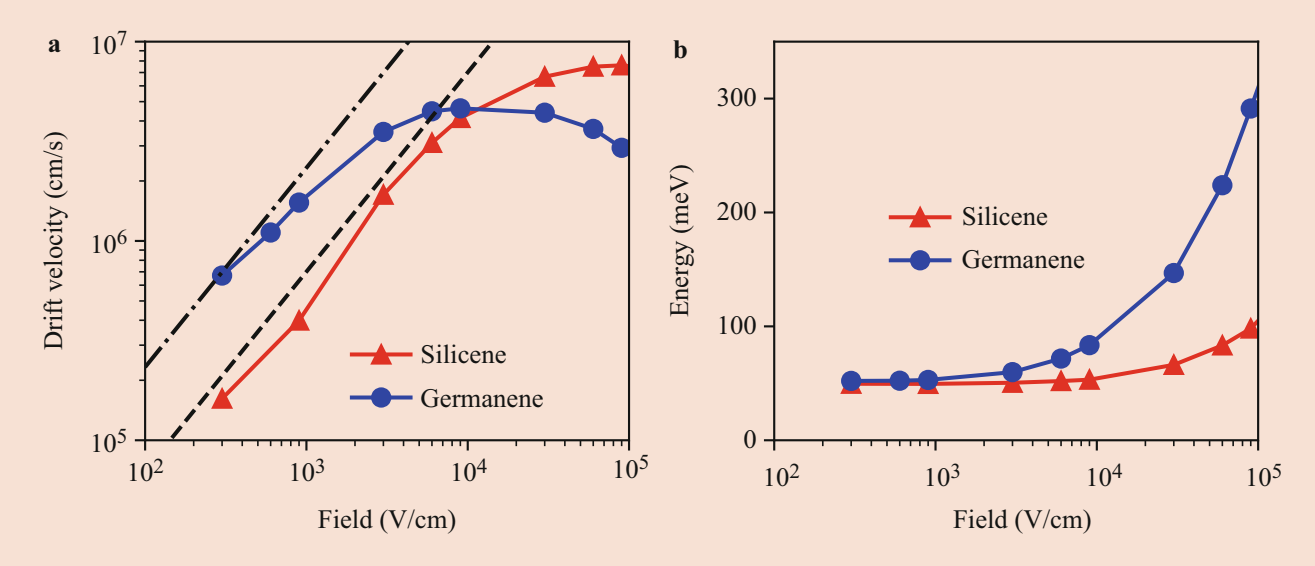

Fig. 42.24 (**a**) Drift velocity *vs* field and (**b**) average-energy *vs* field at 300 K for electrons in silicene and germanene

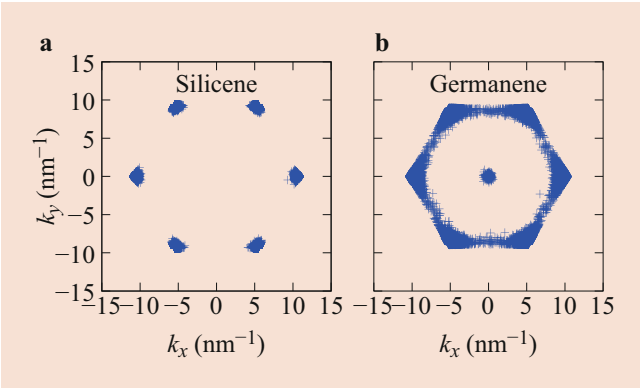

Fig. 42.25 Distribution of electrons in reciprocal space in (**a**) silicene and (**b**) germanene at a high field (≈10^5 V/cm) along the [01] direction

$$e\rho_{\text{ind}}(\mathbf{r}) = e^2 \int P(\mathbf{r},\mathbf{r}')\varphi_{\text{tot}}(\mathbf{r}')\mathrm{d}\mathbf{r}', \tag{42.37}$$

Within the random-phase approximation (RPA), $\chi^0(\mathbf{r},\mathbf{r}')$, obtainable as the Fourier-transform of the dielectric matrix, is $P(\mathbf{r}, \mathbf{r}')$. The function $\chi^0(\mathbf{r},\mathbf{r}')$, averaged along z, is shown in Fig. 42.26 for a perturbation at $\mathbf{r}'$, for $\mathbf{r}'$ is at the ribbon center (a) and at the bottom-left vacuum region (b), respectively.

Two important features of the density-density response function are its exponential spatial decay, like the electron density, and its scalar nature. The first feature enables us to employ a small supercell – as long as it is sufficiently large to guarantee the independence of the calculated band structure on its size – to study the dielectric response. The second feature allows us to avoid unwanted complexity in constructing the linear system of equations when solving the 'ordinary' Poisson equation with tensorial dielectric constants, as shown in the following.

42.5.2 Microscopic Poisson Equation

Of particular interest from the perspective of atomistic device simulations is the possibility of deriving a microscopic Poisson equation that accounts "exactly" for the position-dependent polarization of the system without having to employ any position-dependent "dielectric constant." This can be done by combining Gauss's law, $\nabla \cdot \mathcal{E}_{\text{tot}}(\mathbf{r}) = e\rho_{\text{tot}}(\mathbf{r})/\epsilon_0 = (e\rho_{\text{ext}}(\mathbf{r}) + e\rho_{\text{ind}}(\mathbf{r}))/\epsilon_0$, with the relation between the electric field and electrostatic potential, $\boldsymbol{E}_{\text{tot}}(\mathbf{r}) = -\nabla\varphi_{\text{tot}}$, in the Coulomb gauge and using Eq. (42.37), to express the induced charge as a function of the total potential:

$$\epsilon_0\nabla^2\varphi_{\text{tot}}(\mathbf{r}) + e^2 \int P(\mathbf{r},\mathbf{r}')\varphi_{\text{tot}}(\mathbf{r}')\mathrm{d}\mathbf{r}' = -e\rho_{\text{ext}}(\mathbf{r}), \tag{42.38}$$

where ϵ_0 is the vacuum permittivity, $\varphi_{\text{tot}}(\mathbf{r})$ is the total potential, and $e\rho_{\mathbf{ext}}(\mathbf{r})$ is the external charge. Equation (42.38) can be straightforwardly discretized and solved when Dirichlet/Neumann/periodic boundary conditions are applied. Assuming linear response and embracing the RPA, the solution of this microscopic Poisson equation with the polarizability $\chi^0(\mathbf{r},\mathbf{r}')$ – calculated using the procedure outlined above and either DFT of empirical pseudopotentials – provides the exact total microscopic potential for any arbitrary distribution of free charge.

In so doing, the total potential is obtained immediately, but separating the distinct contributions of the external potential

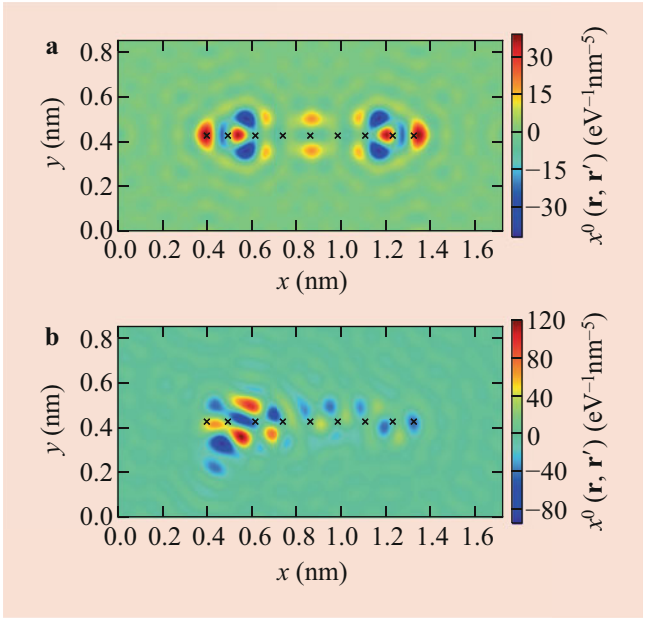

Fig. 42.26 The independent-particle density-density response function, $\chi^0(\mathbf{r},\mathbf{r}')$, of a 7-aGNR in response to a long-wavelength perturbing electric field $q_z \to 0$, (**a**) when the perturbation $\mathbf{r}'$ is at the ribbon center (*i.e.*, $\mathbf{r}' = (0.86\,\text{nm}, 0.43\,\text{nm})$), and (**b**) when the perturbation $\mathbf{r}'$ is at the bottom-left vacuum (*i.e.*, $\mathbf{r}' = (0.43\,\text{nm}, 0.21\,\text{nm})$). The microscopic distribution of the polarization charge can be observed. The seven carbon atoms in the center of the ribbon and the two terminating hydrogen atoms on the edges are indicated with the black cross symbols. (After J. Fang et al. [245], with permission from the American Physical Society ©2016 American Physical Society)

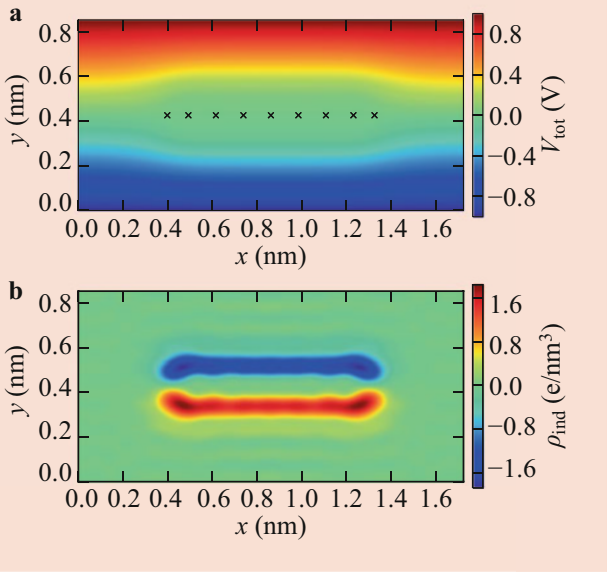

Fig. 42.27 The total potential (**a**) and the induced charge density (**b**) for a 'horizontal' parallel-plate capacitor when 1 V is applied to the top plate and −1 V to the bottom plate. In response to the external field, a dipole is formed. This counteracts the external electric field with a polarization field. (After J. Fang et al. [245], with permission from the American Physical Society ©2016 American Physical Society)

and of the induced (polarization) potential requires a brief discussion. Since we have assumed that the aGNR (or any other nanostructure) is embedded in vacuum, the polarization charge lies exclusively within the aGNR. This can be calculated using Eq. (42.37). Once this is known, the induced polarization potential can be obtained from:

$$\varphi_{\text{ind}}(\mathbf{r}) = e \int \frac{\rho_{\text{ind}}(\mathbf{r}')}{4\pi\epsilon_0|\mathbf{r}-\mathbf{r}'|}\mathrm{d}\mathbf{r}'. \tag{42.39}$$

In turn, having obtained the polarization potential, the applied external potential (*i.e.*, the bare unscreened perturbation) can be obtained from the difference between the total potential and the polarization potential. Finally, the external, polarization, and total electric fields can be calculated from the negative of the gradients of the corresponding potentials.

In two dimensions, averaging the charge distribution along the out-of-plane direction z, one should use the two-dimensional Green's function of the Poisson equation. Thus, the polarization potential is given by:

$$\varphi_{\text{ind}}(\mathbf{r}) = e \int \frac{\rho_{\text{ind}}(\mathbf{r}')\ln(|\mathbf{r}-\mathbf{r}'|/L)}{2\pi\epsilon_0}\mathrm{d}\mathbf{r}', \tag{42.40}$$

where L some arbitrary scaling length. In practice, to the integration over the singularity of the Green's function $\ln(|\mathbf{r}-\mathbf{r}'|/L)$, we can instead calculate the polarization potential by simulating the system using a larger region and Fourier-transforming the polarization charge to obtain $e\rho_{\text{ind}}(\mathbf{r}) \to e\rho_{\text{ind}}(\mathbf{q})$. Then, the polarization potential is finally obtained from $\varphi_{\text{ind}}(\mathbf{q}) = e\rho_{\text{ind}}(\mathbf{q})/(\epsilon_0|\mathbf{q}|^2) \to \varphi_{\text{ind}}(\mathbf{r})$.

42.5.3 Microscopic Dielectric Tensor of 1D Materials

To compute the microscopic dielectric tensor along the non-periodic directions of 1D materials, Eq. (42.38) can be used in the case of two nanocapacitors, a "horizontal" one with plates parallel to the aGNR surface and a "vertical" one with plates perpendicular to the aGNR surface. Since at $q_z \to 0$, the net polarization cannot be built to screen the external potential or electric field applied along the axial direction of the 1D materials, the axial dielectric constant is unity. For finite values of q_z, Eq. (42.38) can be applied to study the axial component of the dielectric tensor by assuming a periodic external (perturbing) potential or electric field and considering a nanocapacitor with length equal to the (spatial) period of the external perturbation. Here we restrict our attention to the simpler case of $q_z \to 0$.

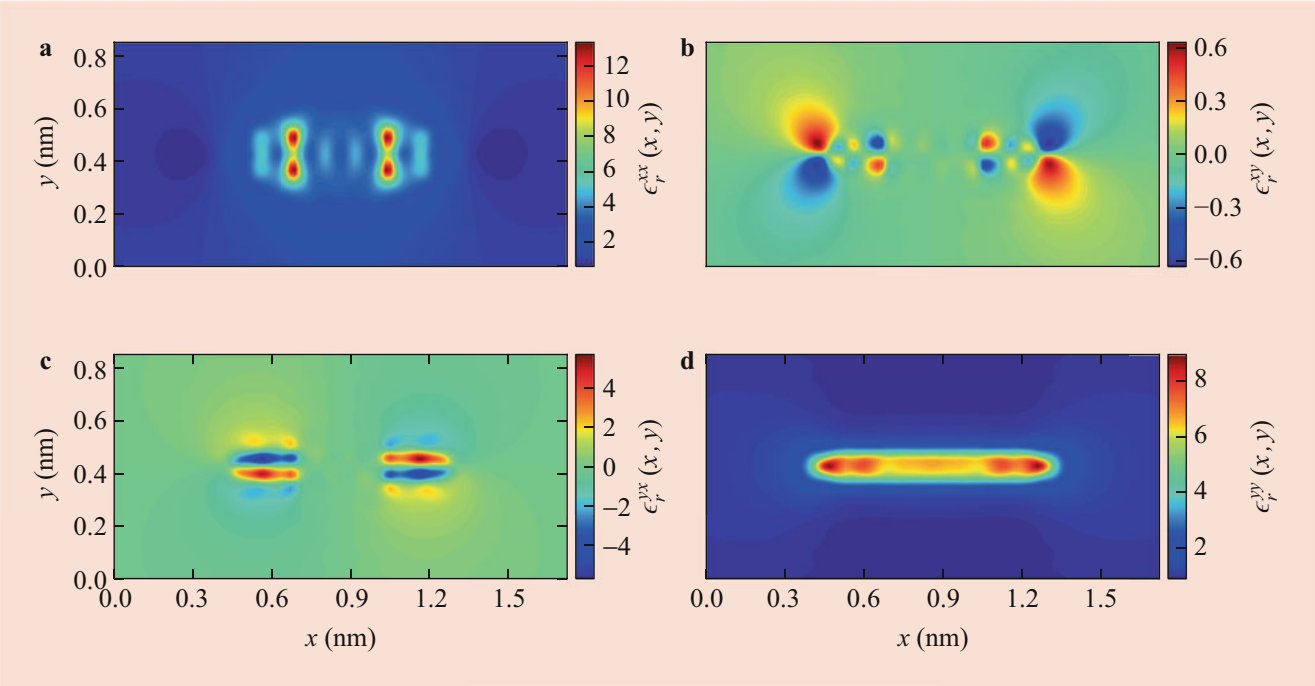

Fig. 42.28 The microscopic dielectric tensor of a 7-aGNR in vacuum. (**a**) and (**d**) show the diagonal components, and (**b**) and (**c**) show the off diagonal components. (After J. Fang et al. [245], with permission from the American Physical Society ©2016 American Physical Society)

The perturbation is defined by applying 1 V on the top plate and −1 V on the bottom plate of the horizontal nanocapacitor. Note that periodic boundary conditions are applied on the left and right boundaries and there are no free charges inside the capacitor. The spatial variation of the total potential and the induced charge, obtained by solving Eq. (42.38) in the two-dimensional case, are shown in Fig. 42.27. In the top frame, note the curvature of the potential distribution around the nanoribbon; in the bottom frame, one can clearly see the induced dipole. In the top frame, we can observe the curved potential distribution around the nanoribbon region; in the bottom frame, we can see the induced dipole. Although not shown, it is easy to obtain the potential and induced charge for the vertical nanocapacitor.

The microscopic external electric field and total electric field for the horizontal ($\boldsymbol{E}^{\text{hor}}_{\text{ext/tot}}$) and the vertical ($\boldsymbol{E}^{\text{ver}}_{\text{ext/tot}}$) capacitor can be easily derived having obtained $\varphi_{\text{tot}}(\mathbf{r})$ and $e\rho_{\text{ind}}(\mathbf{r})$. The microscopic dielectric tensor of a 1D nanostructure in the confined (x, y) plane (*i.e.*, the transverse dielectric tensor) is then evaluated as:

$$\begin{bmatrix} \epsilon_r^{xx}(\mathbf{r}) & \epsilon_r^{xy}(\mathbf{r}) \\ \epsilon_r^{yx}(\mathbf{r}) & \epsilon_r^{yy}(\mathbf{r}) \end{bmatrix} = \begin{bmatrix} \mathcal{E}^{\text{hor}}_{\text{ext},x}(\mathbf{r}) & \mathcal{E}^{\text{ver}}_{\text{ext},x}(\mathbf{r}) \\ \mathcal{E}^{\text{hor}}_{\text{ext},y}(\mathbf{r}) & \mathcal{E}^{\text{ver}}_{\text{ext},y}(\mathbf{r}) \end{bmatrix} \begin{bmatrix} \mathcal{E}^{\text{hor}}_{\text{tot},x}(\mathbf{r}) & \mathcal{E}^{\text{ver}}_{\text{tot},x}(\mathbf{r}) \\ \mathcal{E}^{\text{hor}}_{\text{tot},y}(\mathbf{r}) & \mathcal{E}^{\text{ver}}_{\text{tot},y}(\mathbf{r}) \end{bmatrix}^{-1}, \tag{42.41}$$

where $\mathcal{E}^{\text{hor/ver}}_{\text{ext/tot},x/y}(\mathbf{r})$ is the x or y component of the external/total electric field for the horizontal/vertical nanocapacitor and $\epsilon_r^{ij}(\mathbf{r})$ $(i,\ j = x,\ y)$ is a component of the dielectric tensor which indicates the dielectric response along the direction i when the perturbing electric field is applied along the direction j.

Microscopic Dielectric Tensor of a 7-aGNR

Using the empirical pseudopotentials of Ref. [181] for carbon and the terminating H atoms, we have used the method just outlined to calculate the microscopic dielectric tensor of a 7-aGNR. This is shown in Fig. 42.28. The anisotropy of the microscopic dielectric properties can be observed. Observing the distribution of both $\epsilon_r^{xx}(\mathbf{r})$ and $\epsilon_r^{yy}(\mathbf{r})$, the ribbon region exhibits a large microscopic dielectric constant whereas it approaches ϵ_0 in the vacuum region. Nevertheless, inside the ribbon, $\epsilon_r^{xx}(\mathbf{r})$ exhibits more pronounced microscopic oscillations compared to $\epsilon_r^{yy}(\mathbf{r})$. The off-diagonal elements of the microscopic dielectric tensor, $\epsilon_r^{xy}(\mathbf{r})$ and $\epsilon_r^{yx}(\mathbf{r})$, exhibit the inversion symmetry of the aGNR. Macroscopically, the off-diagonal elements of the microscopic dielectric tensor vanish. This is because x and y are two of the three principal axes of the nanosystem.

Ribbon-Width Dependence of the Dielectric Permittivity

We have simulated also a 3-aGNR, a 5-aGNR and a 6-aGNR. Using empirical pseudopotentials, we find for each of these ribbons a band gap of 1.19 eV, 0.43 eV, and 1.03 eV, respectively, in contrast to the band gap of 1.70 eV for the 7-aGNR. The variation of $\epsilon_r^{yy}(\mathbf{r})$ along the horizontal

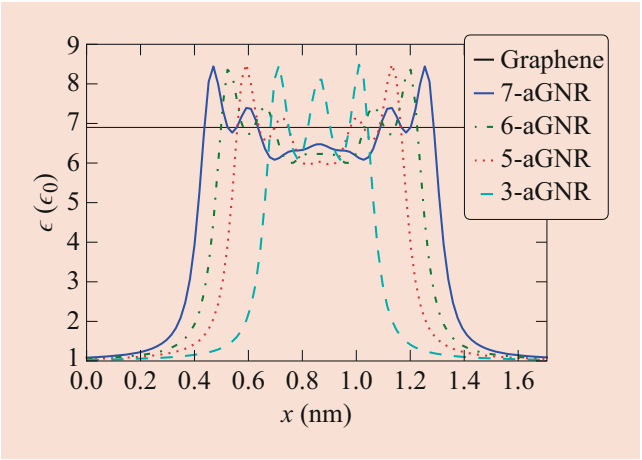

Fig. 42.29 Out-of-plane microscopic dielectric constant, $\epsilon_r^{yy}(\mathbf{r})$, in the horizontal plane for different ribbon widths. The local permittivity in the interior of all ribbons except for the 3-aGNR shows values close to 6 ϵ_0. The local permittivity at the edges of the ribbon shows similar oscillating peaks. The black horizontal straight line, $\epsilon = 6.9\epsilon_0$, indicates the macroscopic dielectric constant of graphene at the carbon-atom plane, as shown in Fig. 42.31. (After J. Fang et al. [245], with permission from the American Physical Society ©2016 American Physical Society)

plane of a 3-aGNR, a 5-aGNR, a 6-aGNR, and a 7-aGNR is plotted in Fig. 42.29. The permittivity in the center of all ribbons, except the 3-aGNR, is approximately 6 ϵ_0, and the permittivity at the edges of the ribbon shows similar peaks and valleys oscillating around $7\epsilon_0$. These features show that ribbon size barely affects the out-of-plane microscopic dielectric constant.

Microscopic Dielectric Tensor of a 3 × 3 Silicon Nanowire

To touch upon silicon, although only very briefly, in Fig. 42.30 we show results obtained for the *xx*-component of the dielectric tensor of a Si nanowire, $\epsilon_r^{xx}(\mathbf{r})$, following the same procedure and using the empirical local pseudopotentials of Ref. [184]. Given the small cross section of the nanowire (only 3 × 3 atoms) and the fact that it is free-standing (surrounded by vacuum, it is not surprising to see that the dielectric function inside the nanowire reaches only a small value, less than 4. This is the result of extremely small nanostructures inheriting the polarization (and, so, the dielectric constant) of the surrounding vacuum or bulk material.

42.5.4 Microscopic Dielectric Permittivity of 2D Materials

Similar to the study of aGNRs, we construct a nanocapacitor with graphene as dielectric and the capacitor plates are placed parallel to the graphene surface. The potential perturbation is applied by imposing a voltage on the plates and then

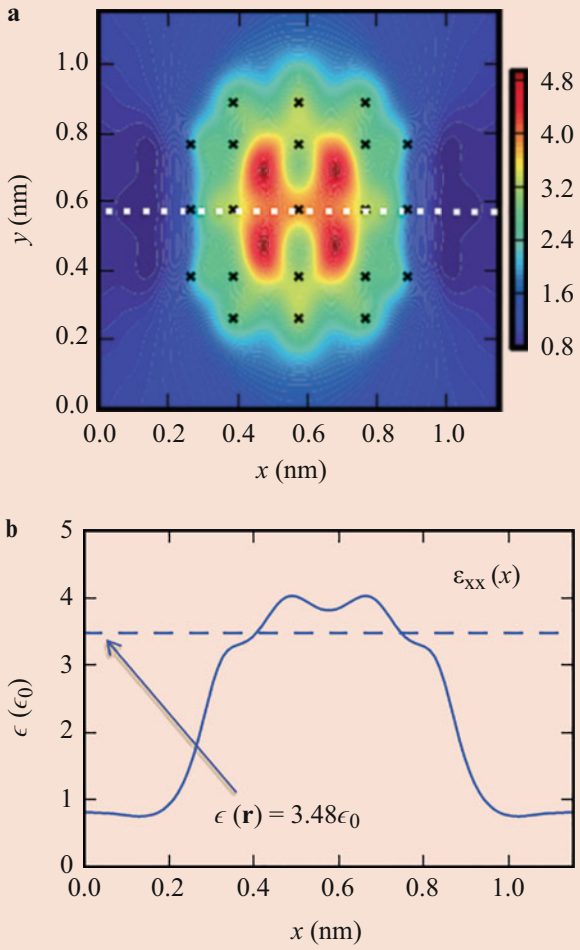

Fig. 42.30 (**a**) variation on the cross-sectional plane of the calculated diagonal *xx* component of the dielectric tensor of a small (3 × 3 atom in cross section) Si nanowire. (**b**) the same, but plotted along the dashed line in the left figure, showing how the maximum value of the dielectric constant in this very small nanostructure is affected by the surrounding medium, vacuum in this case. Note also the smooth transition between the semiconductor and the surrounding medium

we solve the microscopic Poisson equation. By solving the microscopic Poisson equation, Eq. (42.38), we obtain the induced charge density.

The induced charge density averaged on the (x, z) plane is shown in Fig. 42.31. The long-range oscillations of the induced charge are caused by local-field effects [171]. The polarization profile along y can be calculated by applying Gauss's law in 1D [185]. This is also shown in Fig. 42.31. The microscopic dielectric permittivity decays from 6.9 ϵ_0 in the carbon-atom plane to the vacuum permittivity within approximately 0.1 nm. This shows that the out-of-plane dielectric permittivity of the aGNRs resembles that of graphene. We also evaluate the capacitance per unit area of the graphene nanocapacitor as D/V, where D is the displacement field and V is the applied voltage. We find a capacitance of

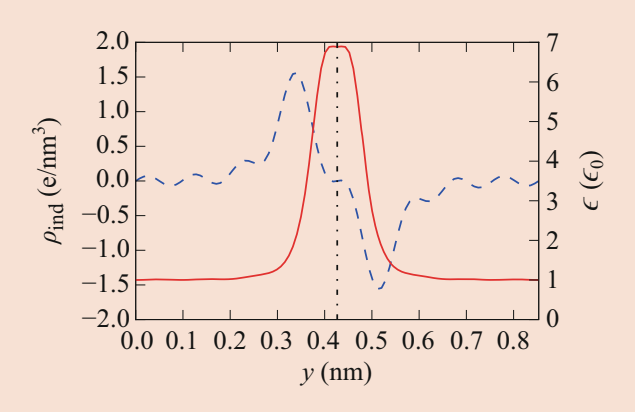

Fig. 42.31 Induced charge density (left y-axis, dashed blue line) when a voltage, $V = 2$ V, is applied to the graphene nanocapacitor and the microscopic dielectric constant of graphene along the direction perpendicular to the graphene plane (right y-axis, solid red line). In response to the potential perturbation, a dipole is formed across the graphene plane, as shown by the induced charge density. The microscopic dielectric permittivity exhibits a peak value of $6.9\epsilon_0$ on the carbon-atom plane and decays to the vacuum permittivity about 0.1 nm away from the carbon-atom plane, indicated by the dashed vertical line. (After J. Fang et al. [245], with permission from the American Physical Society ©2016 American Physical Society)

13.28 F/m^2. Equivalently, attributing an effective dielectric thickness, d, and a macroscopic dielectric constant, ϵ_{mac}, to graphene, the capacitance can also be calculated as $V/D = d/\epsilon_{mac} + (d_0 - d)/\epsilon_0$ (d_0 is the distance between the capacitor plates) since graphene and vacuum are connected in series. Assuming a macroscopic dielectric constant of $6.9\epsilon_0$, the effective dielectric thickness of graphene is about 0.22 nm. This corresponds roughly to the distance of the center of the respective induced charge layer comprising the dipole shown in Fig. 42.31.

42.5.5 Discussion

We have demonstrated that a direct solution of the microscopic Poisson equation incorporates all quantum effects on the electrostatics. This offers a physical-sound avenue for atomistic self-consistent quantum transport simulations in nanotransistors [186] without knowledge of the dielectric tensor of the nanosystems. This is different from the traditional treatment of the Poisson equation in atomistic device simulations reported by Guo et al. in Refs. [187, 188] and Fiori et al. in Ref. [189]. In these simulations the Poisson equation is solved with macroscopic empirical approaches, either using an arbitrarily assumed uniform dielectric permittivity throughout the entire devices or by defining interfaces as "straight ϵ-discontinuity lines," lines arbitrarily drawn among atoms. Thus, physical accuracy is not ensured.

42.6 Quantum Transport

In this final section, we deal with transport beyond the semiclassical limit. Other chapters in this volume discuss this issue in great detail from the perspective of the Wigner function formalism (Chap. 43 by P. Dollfus) and of the nonequilibrium Green's function formalism (Chap. 44 by S. Datta), as implemented using a tight-binding model for the electronic dispersion (Chap. 45 by G. Klimeck). Therefore, we give here only a brief introduction to the subject.

The discussion presented so far has been based implicitly on the idea that electronic transport can be described correctly using semiclassical models, the BTE in particular. However, as early as in 1950, doubts were raised regarding the suitability of such a model to deal with transport at electric fields and energies so large that the associated short electron scattering times render the electronic Bloch states an unacceptably poor approximation of the correct eigenstates of the total Hamiltonian (*i.e.*, that includes also the perturbation). Bardeen and Shockley considered this problem for the case of Si [190], concluding that a semiclassical approach is satisfactory in most cases of practical technological interest. However, the first full-band Monte Carlo study [50] was performed to study impact ionization in GaAs, a process that results in an electron lifetime, τ, as short as 1 fs. Capasso et al. [191] argued that in such cases collisional broadening renders the semiclassical BTE invalid, that is, the energy broadening of the electronic state, $\Delta E \sim \hbar/\tau$, becomes comparable to – or even exceeds – the energy itself of the state. This implies a failure of first-order perturbation theory and Fermi's golden rule. This problem had been already investigated in the context of high-field transport in polar insulators using Feynman path integrals [192]. However, the daunting nature of this formulation prompted, instead, the use of Monte Carlo simulations that account, somehow, for these "broadening" effects [193], vaguely in the spirit of the Barker and Ferry formulation [194]. However, Monte Carlo simulations that employ scattering rates computed beyond first-order perturbation theory soon proved to be affected by serious artifacts due to violations energy conservation. High-field transport was later studied by Jacoboni et al. [195, 196] using the concept of Wigner paths. However, the basic physical nature of this problem is so difficult that the use of *ab initio* methods in this context remains completely unexplored.

A second, and completely different, limitation of semiclassical transport stems, instead, from the ultra-fast dynamics of electrons coupled to elementary excitations of a crystal when stimulated, for example, by ultrashort laser pulses in pump/probe experiments. The eigenstates of the total Hamiltonian are now coupled modes, such as electron-phonon modes, and the semiconductor Bloch equations (SBE), essentially a density-matrix formulation handled by solving the

Heisenberg equations of motion, have been successfully used in the past (see, *e.g.*, Ref. [197] for a comprehensive review).

A third, and final, limitation of the BTE is the limitation that at present is raising the strongest concerns in devices scaled at the nanometer length. This limitation is caused by the small size of the structures that are used by the VLSI technology. Quantum-size (or confinement) effects, which historically originated from studies of the two-dimensional electron gas (2DEG) that is formed in Si inversion layers [198], does not present a particular problem: indeed, transport must be studied in a reduced dimensionality (much as we have seen here when dealing with 2D materials) but can still be treated semiclassically, as long as the length of the active layer (channel) of the device is much longer than the electron wavelength or phase-coherence length. However, in devices whose channels are as short as 10 nm or less, so dimensions comparable to the wavelength of the charge carriers and of their decoherence and scattering length, electrons (or holes) may traverse the active region almost coherently (ballistic transport), so that their full quantum mechanical behavior – neglected by the BTE and in what we wrote so far – must be included in any formulation of transport that we must use to study these devices. Tunneling is another genuine and important quantum mechanical effect that must be captured, since it affects small devices via leakage through thin gate oxides and source-to-drain tunneling and that may also be exploited not only in electrical-erasable programmable random-access memories (E^2PROM and flash-EPROM) but also in tFETs and interlayer tunneling between 2D materials [199]. While tunneling has been modeled using semiclassical expressions, this approach can fail for general nonuniform fields [200–202].

A varied set of methods have been developed to tackle the quantum mechanical description of electronic devices. This variety is caused by the many choices and approximation made:

1. The physics that is included in the (effective) Hamiltonian: Exchange and correlation, spin-orbit coupling, magnetism, etc. Similarly to the historical evolution of methods used to deal with semiclassical transport (as discussed in Sect. 42.2, empirical or semiempirical methods have been used at first, notably empirical tight-binding in the first computer program based on the nonequilibrium Green's function method, NEMO [203–205], empirical pseudopotentials [39, 186, 206, 207], or linear combination of atomic bands [208]. However, also in this case the progress made on numerical methods and hardware have begun to make it possible to consider first-principles approaches. Indeed empirical tight-binding has been replaced by its DFT counterpart [209, 210], and we have already mentioned approaches based on all-electron calculations [64, 65] and even earlier DFT itself [29].
2. The basis that is used to discretize the Hamiltonian: Linear combination of localized orbitals (LCAO) – as in many tight-binding studies [211], plane waves, Bloch waves, and Wannier functions. This choice affect also first-principles formulations, as we have seen before.
3. The representation of the nonequilibrium state, that is, the formulation of the quantum transport equations, such as single particle wavefunctions, Landauer-Büttiker formulation [212–214], density matrix [197, 215], Wigner functions [196,216,217], or nonequilibrium Green's functions (NEGF [218–220]). Even in the ballistic case, the quantum-transmitting boundary method (QTBM) [221] can be chosen in place of a (somewhat improperly termed but highly popular) "ballistic NEGF" approach.

One additional crucial issue is constituted by inelastic scattering, that is, collisions with scatterers with internal degrees of freedom, so that memory of the phase of the carriers is lost (phase decoherence). When using the Wigner formulation, inelastic processes are often included in an approximated way via a Boltzmann-like collisional integral, since the "correct" formulation [222] is numerically intractable. The NEGF formulation is equally daunting, unless the scattering processes are "diagonalized" in some *ad hoc* fashion (so, rendered local) or unless small systems are considered, such as molecules [33,34]. Nevertheless, this last method is arguably the method of choice, since, *in principle*, it is valid over the entire range of device dimensions, from long "semiclassical" channels to ultrashort "ballistic" devices. In particular, numerical difficulties notwithstanding, it can describe correctly the all-important intermediate regime, in which the device length is comparable to the other characteristic length-scales, namely, the electron wavelength, and the scattering/decoherence length associated with the various scattering processes, mainly, electron-phonon scattering, scattering with impurities or surface roughness.

In this section, we limit our discussion to length-scales short enough to render scattering processes a weak perturbation, starting from the ballistic limit, and extending in a natural way our methodology to include weak scattering processes. We employ plane waves since we consider them more suitable than localized orbitals to treat extended conduction states and we employ the simpler QTBM, rather than NEGF, because of its better numerical efficiency in the ballistic limit, a limit in which QTBM and NEGF are virtually identical from a physical perspective.

When considering *ab initio* transport within the density functional theory (DFT) framework, two options are available to approximate the Hamiltonian. The first option is to use the full self-consistent Kohn-Sham Hamiltonian, including exchange and correlation based on the nonequilibrium charge. However, since devices are large systems, self-consistently solving the Kohn-Sham Hamiltonian is com-

putationally expensive within the DFT framework. Since transport properties are only determined by electron states near the Fermi level, a second option is to use an effective low-energy Hamiltonian that is computationally less expensive. Such an effective Hamiltonian can be constructed from *ab initio* simulations of representative systems. A further benefit is that empirical data can supplement *ab initio* data in the construction of the effective Hamiltonian to correct for the deficiencies of DFT, such as underestimated band gaps and incorrect effective masses. Therefore, here we describe quantum electron transport within the pseudopotential approximation, using a plane-wave basis. However, the formulation can be easily generalized to first-principles methods. We first describe the ballistic transport formalism based on the extended states. We then detail the numerical approach based on envelope functions. Next, we introduce the addition of scattering using the Pauli Master Equation. Finally, we demonstrate our method by simulating highly scaled transistors based on graphene nanoribbons and silicon nanowires.

42.6.1 Ballistic Transport

In the ballistic limit, electron dynamics is described by the extended wavefunctions in the device and its infinitely long contacts. The extended wavefunctions are the solutions of the Schrödinger equation:

$$\left[-\frac{\hbar^2\nabla^2}{2m}+V_{\text{tot}}(\mathbf{r})\right]\psi_{\kappa\nu,E}(\mathbf{r})=E\psi_{\kappa\nu,E}(\mathbf{r})\,, \tag{42.42}$$

where E is the energy of the electron injected from contact κ and ν is a mode index. The potential energy $V_{\text{tot}}(\mathbf{r})$ captures all of the potential energy felt by an individual particle; this includes the ionic potential, the mean-field Hartree potential generated by the free charges, doping and electrostatic gates, as well as exchange and correlation contributions. In the contacts, the total potential is assumed to be lattice periodic, yielding Bloch wave solutions with a well-defined wave vector $\mathbf{k}_{\kappa\nu}$.

We assume that the device's contacts are connected to large equilibrium reservoirs, each at a fixed chemical potential μ_κ. When a bias is applied to the device (between contacts κ and κ'), it is driven out of equilibrium by a relative change in the Fermi level of the contacts, *i.e.*, $\mu_\kappa - \mu_{\kappa'} = V_{\text{bias}}$. To describe the statistics, we introduce the ballistic density matrix, which is diagonal in the basis of the extended states:

$$\rho^{(\text{bal})}_{\kappa\nu E,\kappa'\nu' E'}=\delta_{\kappa\kappa'}\delta_{\nu\nu'}\delta_{EE'}f_{\text{FD}}(E-\mu_\kappa)\,, \tag{42.43}$$

where the Fermi-Dirac distribution is given by

$$f_{\text{FD}}(E-\mu_\kappa)=\left[1-\exp\left(\frac{E-\mu_\kappa}{k_{\text{B}}T}\right)\right]^{-1}. \tag{42.44}$$

Using this density matrix, the expressions for electron density, as well as current density are readily obtained:

$$\rho^{(\text{bal})}(\mathbf{r})=\sum_{\kappa\nu}\int \text{d}E\left(\frac{\text{d}E_{\kappa\nu}}{\text{d}k}\right)^{-1} \times\left|\psi_{\kappa\nu,E}(\mathbf{r})\right|^2 f_{\text{FD}}(E-\mu_\kappa)\,, \tag{42.45}$$

$$\mathbf{J}^{(\text{bal})}(\mathbf{r})=\sum_{\kappa\nu}\frac{e\hbar}{m}\int \text{d}E\left(\frac{\text{d}E_{\kappa\nu}}{\text{d}k}\right)^{-1} \times \text{Im}[\psi_{\kappa\nu,E}(\mathbf{r})\nabla\psi_{\kappa\nu,E}(\mathbf{r})]f_{\text{FD}}(E-\mu_\kappa)\,, \tag{42.46}$$

where, since we have assumed that the injecting wavefunctions have been δ-normalized in their respective contacts, $(\text{d}E_{\kappa\nu}/\text{d}k)^{-1}$ is the density of states of mode ν contact κ.

42.6.2 Numerical Approach

In a numerical implementation, Eq. (42.42) needs to be discretized and the infinitely long contacts need to be truncated. In a periodic system, Eq. (42.42) is readily discretized on plane waves, $\psi_{\kappa\nu,E}=\sum_{\mathbf{G}}u_{\kappa\nu,E,G}e^{i\mathbf{G}\cdot\mathbf{r}}e^{i\mathbf{k}_{\kappa\nu,E}\cdot\mathbf{r}}$ using Bloch's theorem. Plane waves offer a mathematically complete basis that can be tuned to very high accuracy through the kinetic energy cutoff. By using the fast Fourier transform algorithm, plane waves have a relatively low computational cost and almost optimal scalability with system size. However, the application of bias and gate potentials breaks the periodic nature of the total potential in Eq. (42.42). This prevents the use of Bloch's theorem to express the electronic wavefunctions in the device. To circumvent this problem, the envelope function approach was developed [39, 186, 206]. More recently we developed a significantly more efficient method based on Bloch waves [223]. Once discretized, the truncation of the numerical domain is achieved by replacing the infinite contacts with a self-energy contribution, regardless of the chosen discretization.

While the Bloch wave method demonstrates significant progress in numerical efficiency, the envelope function has the benefit of conceptual clarity. For this reason, we highlight here the envelope function approach and its associated self-energies as an introduction to quantum transport simulations using pseudopotentials. We advise the interested reader to research advanced techniques, such as the Bloch wave-based method [223].

Envelope Functions

In the envelope-wavefunction approximation, we express the full electronic wavefunction at a given energy E as:

$$\psi_{\kappa\nu,E}(\mathbf{r}) = \sum_{\mathbf{G}} \phi_{\kappa\nu,E,\mathbf{G}}(\mathbf{r}) e^{i\mathbf{G}\cdot\mathbf{r}}, \tag{42.47}$$

where the envelope function in the periodic case $e^{i\mathbf{k}_{\kappa\nu,E}\cdot\mathbf{r}}$ is replaced by the more general envelope $\phi_{\kappa\nu,E,\mathbf{G}}$. The dependence of the envelope ϕ on $\mathbf{r}$ results indeed from the breaking of the periodicity caused by the applied bias and doping.

Using the envelope expansion in Eq. (42.47) in the Schrödinger equation (Eq. 42.42) yields an equation for the envelope functions

$$\sum_{\mathbf{G}'} \left\{ \left[\frac{\hbar^2}{2m}(-i\nabla + G)^2 + \bar{V}_{\text{tot}}(\mathbf{r}) \right] \delta_{\mathbf{G},\mathbf{G}'} + V_{\mathbf{G}-\mathbf{G}'} \right\} \times \phi_{\kappa\nu,E,\mathbf{G}}(\mathbf{r}) = E\phi_{\kappa\nu,E,\mathbf{G}}(\mathbf{r}) \tag{42.48}$$

where we have separated the total potential $V_{\text{tot}}(\mathbf{r}) = \bar{V}_{\text{tot}}(\mathbf{r}) + \sum_{\mathbf{G}} V_{\mathbf{G}} e^{i\mathbf{G}\cdot\mathbf{r}}$ into a slowly varying part $\bar{V}_{\text{tot}}(\mathbf{r})$ and the periodic lattice potential, captured by $V_{\mathbf{G}}$.

After discretization of the $\mathbf{r}$ coordinate, and using a finite difference scheme for the gradient, we obtain a sparse matrix equation:

$$\mathbf{H}\boldsymbol{\phi} = E\boldsymbol{\phi} \Leftrightarrow \begin{bmatrix} \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \mathbf{T}^\dagger & \mathbf{D}_{i-1} & \mathbf{T} & 0 & 0 \cdot \\ \cdot & 0 & \mathbf{T}^\dagger & \mathbf{D}_i & \mathbf{T} & 0 \cdot \\ \cdot & 0 & 0 & \mathbf{T}^\dagger & \mathbf{D}_{i+1} & \mathbf{T} \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \end{bmatrix} \begin{bmatrix} \cdot \\ \boldsymbol{\phi}(\mathbf{r}_{i-1}) \\ \boldsymbol{\phi}(\mathbf{r}_i) \\ \boldsymbol{\phi}(\mathbf{r}_{i+1}) \\ \cdot g \end{bmatrix} = E \begin{bmatrix} \cdot \\ \boldsymbol{\phi}(\mathbf{r}_{i-1}) \\ \boldsymbol{\phi}(\mathbf{r}_i) \\ \boldsymbol{\phi}(\mathbf{r}_{i+1}) \\ \cdot \end{bmatrix}. \tag{42.49}$$

where the explicit matrix structure is given for the one-dimensional case, for which $\mathbf{D}_i$ and $\mathbf{T}$ are block matrices of size $(N_{\mathbf{G}} \times N_{\mathbf{G}})$ [186]. The vector containing the discretized envelope function contains sub-vectors of size $N_{\mathbf{G}}$:

$$\boldsymbol{\phi}(\mathbf{r}_i) = [\phi_{\mathbf{G}_1}(\mathbf{r}_i), \phi_{\mathbf{G}_2}(\mathbf{r}_i), \ldots, \phi_{\mathbf{G}_{N_{\mathbf{G}}}}(\mathbf{r}_i)]^\intercal . \tag{42.50}$$

Self Energies

In order to solve Eq. 42.49 numerically, we truncate it to the device region, *i.e.*:

$$\boldsymbol{\phi} = [\boldsymbol{\phi}(\mathbf{r}_1), \boldsymbol{\phi}(\mathbf{r}_2), \ldots, \boldsymbol{\phi}(\mathbf{r}_N)]^\intercal . \tag{42.51}$$

This necessitates the introduction of boundary conditions (the so-called quantum-transmitting boundary conditions) at the contacts that can inject and absorb waves. Since we have forced the potential in each contact to be periodic, the solutions in the contacts are Bloch waves. Specifically, for a given energy E, the envelope functions of the eigenmodes $\psi_\kappa^{(c)}$ of a contact κ located at $\mathbf{r}_{i_\kappa}$ are found, using Bloch's theorem, as:

$$\left[\mathbf{T}^\dagger e^{-ik_\kappa \Delta} + \mathbf{D}_{i_\kappa} + \mathbf{T} e^{ik_\kappa \Delta}\right] \boldsymbol{\phi}_\kappa^{(c)}(\mathbf{r}_{i_\kappa}) = E\boldsymbol{\phi}_\kappa^{(c)}(\mathbf{r}_{i_\kappa}), \tag{42.52}$$

where the Δ is distance between r_{i_κ} and $r_{i_\kappa - 1}$.

For each energy E, Eq. (42.52) admits $2N_{\mathbf{G}}$ solutions $(k_\kappa, \boldsymbol{\phi}_\kappa^{(c)})$. Classifying the contact solutions into incoming and outgoing modes, we assemble the "Bloch matrices," $\left[\boldsymbol{\phi}_\kappa^{(c)}\right]_{\text{in}}$ and $\left[\boldsymbol{\phi}_\kappa^{(c)}\right]_{\text{out}}$, containing the respective solutions as their columns. Using these Bloch matrices, we calculate the contact self-energies directly as:

$$[\boldsymbol{\Sigma}]_\kappa = \mathbf{T}' \left[\boldsymbol{\phi}_\kappa^{(c)}\right]_{\text{out}} \text{diag}\left[e^{ik_\kappa \Delta}\right]_{\text{out}} \left[\boldsymbol{\phi}_\kappa^{(c)}\right]_{\text{out}}^{-1}, \tag{42.53}$$

where $\text{diag}\left[e^{ik_\kappa \Delta}\right]_{\text{out}}$ is a diagonal matrix containing the phase factors of their respective solutions in the Bloch matrices and $\mathbf{T}'$ is either $\mathbf{T}$ or $\mathbf{T}^\dagger$ depending on the position of the contact. From right to left, the effect of the matrices in Eq. (42.53) is to (1) project the envelope at the edge onto the basis of contact solution, (2) propagate each solution one step (Δ) inside the contact, (3) reassemble the envelope function, and (4) apply the truncated part of the Hamiltonian. For a detailed derivation of the various parts, we refer the reader to Ref. [186].

With the definition of the self-energies $[\boldsymbol{\Sigma}]_\kappa$, the envelope functions ψ obey the following linear system of differential equations [186]:

$$(\mathbf{H} - E\mathbf{I} + [\boldsymbol{\Sigma}]_\kappa)\,\boldsymbol{\phi} = [\mathbf{r.h.s.}]_\kappa^{\text{inj}}, \tag{42.54}$$

where $\mathbf{I}$ is the identity matrix and $[\mathbf{r.h.s.}]_\kappa^{\text{inj}}$ is the contact injection from contact κ that decides which mode gets injected.

Self-Consistency

At a given bias, we solve Eq. (42.54) for all electron injection energies with a rough initial guess on the external potential and obtain their respective envelope functions and the spatial electronic wavefunctions. We calculate the carrier density using Eq. (42.45), summing over all the energy states with their corresponding thermal occupation set by the Fermi level of each contact. We then solve the (macroscopic or microscopic, see Sect. 42.5.2) Poisson equation, to update the Hartree potential and, if accounted for, update the exchange and correlation contributions. This procedure is repeated using Newton-Rhapson iteration until the root-mean-square potential-difference between two successive it-

erations is smaller than a preset convergence criterion. To accelerate convergence, we succesfully employed the direct inversion of the iterative subspace (DIIS) method, also known as Pulay mixing in the chemistry community [223]. After convergence, we calculate the current density from the final envelope functions.

42.6.3 Scattering—The Pauli Master Equation

In realistic small devices, the ballistic limit is rarely, if ever, achieved. To account for scattering in short devices where scattering is still relatively weak, we can use the Pauli Master equation approach [39, 224–226]. In this approach, we replace the noninteracting ballistic density matrix $\rho^{(\mathrm{bal})}$ with the density matrix ρ for the interacting system.

By invoking the Van Hove limit, Fischetti [225] showed that the time-dependence of the elements of the density matrix is given by:

$$\begin{aligned}\frac{\partial}{\partial t}\rho_{\kappa\nu E,\kappa'\nu'E'}(t) &= -\frac{i}{\hbar}(E-E')\rho_{\kappa\nu E,\kappa'\nu'E'}(t)\\ &- \sum_{\kappa''\nu''E''}\left[W_{\kappa''\nu''E'',\kappa\nu E} + W_{\kappa''\nu''E'',\kappa'\nu'E'}\right]\rho_{\kappa\nu E,\kappa'\nu'E'}(t)\\ &+ \sum_{\kappa''\nu''E''}\delta_{\kappa\nu E,\kappa'\nu'E'}W_{\kappa\nu E,\kappa''\nu''E''}\rho_{\kappa''\nu''E'',\kappa''\nu''E''}(t)\,. \quad (42.55)\end{aligned}$$

Thanks to the Van Hove limit, where we assume the scattering process completes much faster than the dynamics of the electrons themselves, we can ignore memory effects and phase information. The scattering rates $W(\kappa\nu E,\kappa'\nu'E')$ for a perturbing potential V' are then obtained using Fermi's golden rule, in much the same way as for the semiclassical Monte-Carlo approach:

$$W(\kappa\nu E,\kappa'\nu'E') = \frac{\left|\langle\kappa\nu E|V'|\kappa'\nu'E'\rangle\right|^2}{|E-E'|}\,. \quad (42.56)$$

When considering small devices, where electrons scatter only rarely before being absorbed by a contact, the off-diagonal parts of the density matrix are negligible and the Pauli Master equation reduces to:

$$\begin{aligned}&\frac{\partial}{\partial t}\rho_{\kappa\nu E,\kappa\nu E}(t)\\ &\quad= \sum_{\kappa'\nu'E'}\left[W_{\kappa\nu E,\kappa'\nu'E'}\rho_{\kappa'\nu'E',\kappa'\nu'E'}(t)\right.\\ &\qquad\left.- W_{\kappa'\nu'E',\kappa\nu E}\rho_{\kappa\nu E,\kappa\nu E}(t)\right]\,. \quad (42.57)\end{aligned}$$

To account for the exchange of particles through the contact reservoirs, Fischetti [224] introduced an empirical term:

$$\begin{aligned}&\left(\frac{\partial}{\partial t}\rho_{\kappa\nu E,\kappa\nu E}(t)\right)_{\mathrm{res}}\\ &\quad= |A_{\kappa\nu E}|^2\, v_{\kappa\nu E,\perp}\left[f_{\mathrm{FD}}(E-\mu_\kappa) - \rho_{\kappa\nu E,\kappa\nu E}(t)\right], \quad (42.58)\end{aligned}$$

where particles (waves) are injected from a contact κ that is in equilibrium with chemical potential μ_κ with a group velocity $v_{\kappa\nu E,\perp}$ normal to the contact. $A_{\kappa\nu E}$ is the normalization factor applied to the injected wavefunction such that $\int_\Omega \mathrm{d}^3 r|\psi_{\kappa\nu E}(\mathbf{r})|^2 = 1$, where Ω is the volume of the device.

For device transport we are mostly interested in the steady state. In this case, the injection from the contacts needs to balance the scattering, *i.e.*, the right-hand sides of Eqs. (42.57) and (42.58) must be equal. The resulting linear matrix equation can be solved very efficiently using existing linear algebra packages.

42.6.4 Example 1: Graphene Nanoribbon Transistors

To study transport through graphene nanoribbons, we use the empirical pseudopotentials from Ref. [181] with an energy cutoff of 15 Ry. The atoms have been positioned in a perfect sp^2 lattice, without relaxation of the hydrogen atom positions. We calculate the band structure of several armchair graphene nanoribbons (aGNR), shown in Fig. 42.32a. In the given energy range, 7-, 10-, 13-aGNRs show two conducting bands, whereas the 6-aGNR shows only one conducting band. Fischetti et al. have shown that the electron effective mass of aGNRs at the conduction band minimum oscillates, so that, for example, $m_6^* < m_7^* < m_{13}^* < m_{10}^*$, where m_n^* represents the effective mass of the n-aGNR [60]. Figure 42.32b shows the dispersion of the lowest conduction band for 3-, 6-, 9-, and 12-aGNRs, and it indicates that $m_{12}^* < m_9^* < m_6^* < m_3^*$ [60]. The difference of the effective mass can result in different transport behavior of each ribbon, especially in the subthreshold region of device operation, as we will discuss later.

Ribbons with different body widths exhibit different band gaps, as shown in Fig. 42.32c [199]. The $3n$-aGNRFETs and $(3n{+}1)$-aGNRFETs with different channel lengths and different ribbon widths are simulated to investigate their device performance. The $(3n{+}2)$-aGNRs are not of interest here, since their small band gap results in a very poor subthreshold leakage as a consequence of a high tunneling current.

Transport Characteristics of aGNRFETs

The I_{DS}-V_{GS} characteristics are presented in Fig. 42.33a,b. Clearly, transistors with different widths show different transfer characteristics. We show the ribbon width dependence of the current at a gate overdrive, V_{GS}-$V_{\mathrm{th}} = 0.25\,\mathrm{V}$, and subthreshold swing in Fig. 42.35.

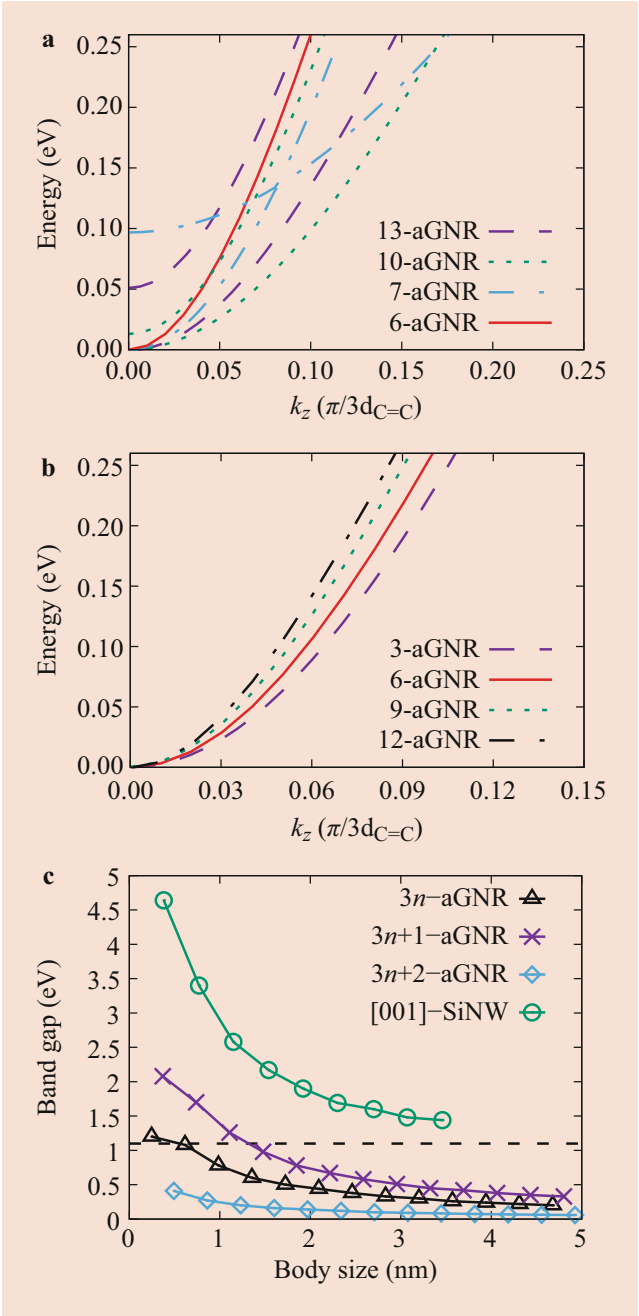

Fig. 42.32 (**a**, **b**) Conduction band dispersion of several aGNRs in a given energy range from E_{CBM}, the conduction band minimum, to $E_{CBM} + 10k_BT$ ($T = 300$ K). The energy of E_{CBM} is set as zero. (**c**) Body-size dependence of the band gap of aGNRs and [001]-oriented silicon nanowires. The horizontal dashed line indicates the band gap of bulk silicon, which is 1.1 eV. The index n is an integer which characterizes the ribbon width. The lines connecting the symbols are a guide to the eye. (After Ref. [206], with permission from IEEE)

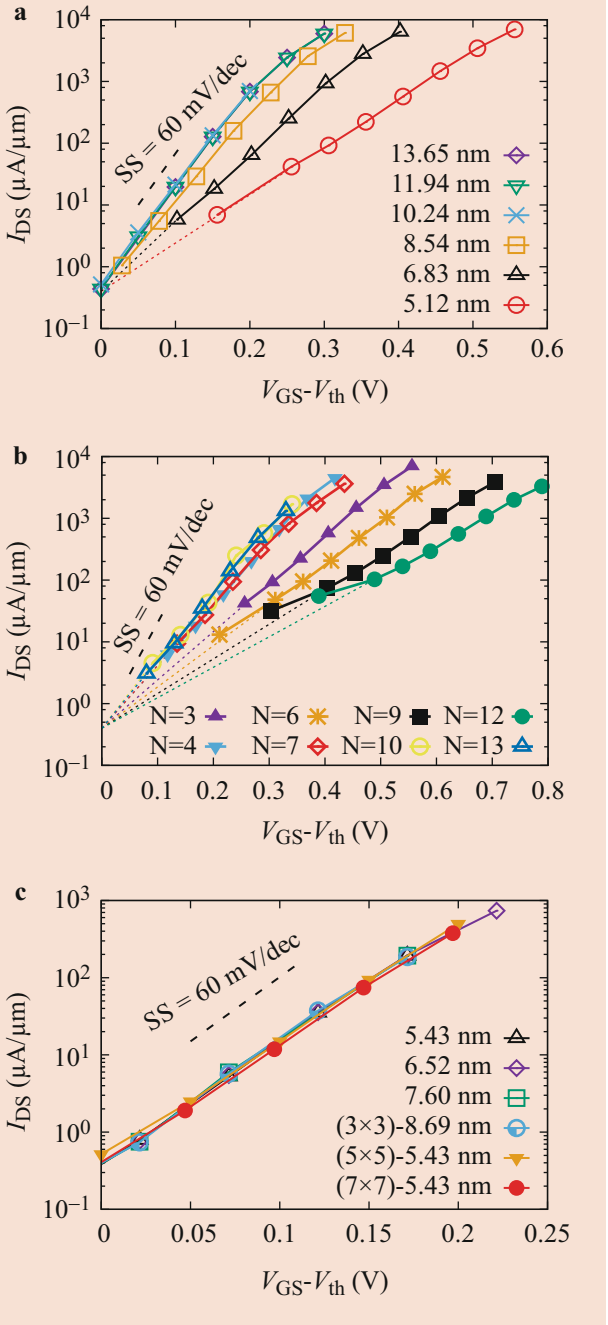

Fig. 42.33 (**a**) Gate-length dependence of transfer characteristics for 3-aGNRFETs at $V_{DS} = 0.1$ V (taken as representative of $V_{DD} = 0.4$ V, thanks to the saturation of the $I_{DS} - V_{DS}$ curves for $V_{DS} > 0.1$ V). The device gate length, L_G, ranges from 5.12 nm to 13.65 nm. (**b**) I_{DS}-V_{GS} transfer characteristics at $V_{DS} = 0.1$ V for aGNRFETs with the same gate length $L_G = 5.12$ nm and with different widths. (**c**) I_{DS}-V_{GS} transfer characteristics of four (3×3)-SiNWFETs with different gate lengths (from 5.43 nm to 8.69 nm) and of a (5×5)-SiNWFET and a (7×7)-SiNWFET both with a gate length of 5.43 nm, at $V_{DS} = 0.1$ V. The dotted lines extending to the threshold voltage have been obtained by extrapolating the current calculated at higher gate bias using the calculated subthreshold slope. The 60 mV/dec slope and the lines connecting the symbols are a guide to the eye. (After Ref. [206], with permission from IEEE)

Figure 42.32c illustrates the band gap of aGNRs with different body size (*i.e.*, ribbon width). For a ribbon wider than 5 nm, the band gap approaches the vanishing band gap of graphene. The band gap increases as the ribbon width de-

creases as a consequence of quantum confinement [227]. The band gap for a ribbon with a width about 4 nm is about 0.4 eV, which matches the experimental result reported in Ref. [228]. The gap of a 7-aGNR is also experimentally observed to be ∼1.8 eV [229]. These facts highlight the accuracy of band structure calculation based on empirical pseudopotentials, while maintaining computational efficiency. The 3-aGNRFETs with a body width $W_{body} = 0.25$ nm and a gate length L_G ranging from 5.12 nm (12 cells along z) to 13.65 nm (32 cells along z) are simulated. The source and the drain regions are both set as ∼6 nm, and we assume no gate-channel overlap. Both the source and the drain regions are doped as n-type with a density of 10^8 m^{-1}, and the channel region is doped as p-type with a density of 10^8 m^{-1}. Abrupt junctions are assumed. We use "vacuum" as a virtual gate insulator in the transport model. The size of "vacuum," t_{vac}, and its dielectric constant, ϵ, are related to the EOT as $t_{vac}/\epsilon = \text{EOT}/\epsilon_{SiO_2}$, where EOT is set as 0.43 nm and ϵ_{SiO_2} is the dielectric constant of silicon dioxide.

The current-voltage characteristics of these 3-aGNRFETs are shown in Fig. 42.33a. We define here the threshold voltage, V_{th}, as the gate bias at which the drain current reaches a preset value $I_{off} = 0.4\,\mu$A/μm. This definition allows us to compare various devices at the same I_{off} and the same gate overdrive $V_{GS} - V_{th} = 0.25$ V. Also we assume a power supply voltage $V_{DD} = 0.4$ V [1]. Since I_{DS} saturates for $V_{DS} > 0.1$ V, we shall consider the on-state at $V_{DS} = 0.1$ V as representative of the performance at $V_{DS} = V_{DD}$. When the gate length is larger than 10 nm, the current at a given bias is approximately independent of gate length. This is due to the assumption of ballistic transport. This is in contrast with "the linear model" or "the quadratic model" in traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) according to which carriers can scatter within the device when traveling along the channel. Thus, increasing the device length will increase the channel resistance proportionally and reduce the current (*i.e.*, $I_{DS} \propto 1/L$) [230]. For devices with a gate length below 10 nm, the current decreases with a decrease of the gate length at the same given gate overdrive due to the significant quantum-mechanical source-to-drain tunneling effect that causes a very poor turn-off behavior and thus threshold voltage shift for devices with a ultrashort gate length [231].

This is shown as well in Fig. 42.34a which compares the current for devices with different channel lengths at a given gate overdrive, $V_{GS} - V_{th} = 0.25$ V. The current does not show a strong dependence on the channel length when it is above 10 nm, whereas it decreases by two orders of magnitude when the channel length is below 10 nm.

The subthreshold behavior is shown in Fig. 42.34b. The subthreshold swing reaches the ideal performance of 60 mV/dec for traditional MOSFETs [232] when $L_G > 10$ nm. However, a shorter-channel device presents a degraded subthreshold swing due to the source-to-drain tunneling. Thus, for a given power supply V_{DD}, the I_{on}/I_{off} current ratio decreases for a shorter device.

42.6.5 Example 2: Silicon Nanowire FETs

Gate-all-around SiNWFETs with square and smaller cross sections are simulated as well. The SiNWs are with axis along the [100] crystallographic (transport) direction and with {100} surfaces since this yields a high ballistic conductance (at least in large cross-section NWs, Ref. [40], Fig. 7.34) while retaining a transport mass that for small cross-section NWs is large enough [233] to minimize source-to-drain tunneling. The band gap of [001]-oriented SiNWs with a square cross section and different body sizes (*i.e.*, NW side lengths) is also shown in Fig. 42.32c. When the NW side length is larger than 3.5 nm, the band gap approaches the band gap of bulk silicon. The electron effective mass at the conduction band minimum is $1.94m_0$, $0.88m_0$, and $0.73m_0$, respectively, for (3×3) SiNW, (5×5) SiNW, and (7×7) SiNW. The (3×3) SiNWFETs with gate lengths ranging from 5.43 nm (10 cells along z) to 8.69 nm (16 cells along z) are simulated. All of these nanowires have three atomic layers along each side of the cross section and thus have a side length of 0.39 nm (Ref. [186], Fig. 3). The surfaces of the NWs are hydrogen-terminated. The current-voltage transfer characteristics of these devices are shown in Fig. 42.33c. The current is the same at a given V_{DS} and V_{GS} for all gate lengths, and thus they have the same threshold voltage. Thus, there is no appreciable source-to-drain tunneling for a (3 × 3) SiNWFET with a ∼5 nm gate length. Normalizing the current at $V_{GS} - V_{th} \approx 0.25$ V and $V_{DS} = 0.1$ V to the NW side length (footprint), the current density reaches around 1000 μA/μm, which satisfies the performance requirement for continued device scaling suggested by ITRS [146]. The subthreshold swing is 66 mV/decade and I_{on}/I_{off} ratio is $\sim 2 \times 10^3$.

In Fig. 42.34a we compare their performance with aGNRFETs in a similar range of gate lengths. It is obvious that SiNWFETs have a much larger current than aGNRFETs when the gate length is below 10 nm. Especially, at the 5 nm gate length, (3×3) SiNWFET shows a current ∼25 times larger than 3-aGNRFET.

Both a (5×5) SiNWFET and a (7 × 7) SiNWFET are simulated to investigate the body-size effect of NWs on the device performance. They both have a gate length of 5.43 nm and a side length of 0.78 nm and 1.17 nm. These large cross-section SiNWFETs show very similar current density with the (3 × 3) SiNWFETs at the same gate overdrive.

The current at a gate overdrive of 0.25 V and the subthreshold swing are illustrated in Fig. 42.35. In Fig. 42.34 we compare the performance of SiNWFETs with that of aGNRFETs at different body sizes. The SiNWFETs show a

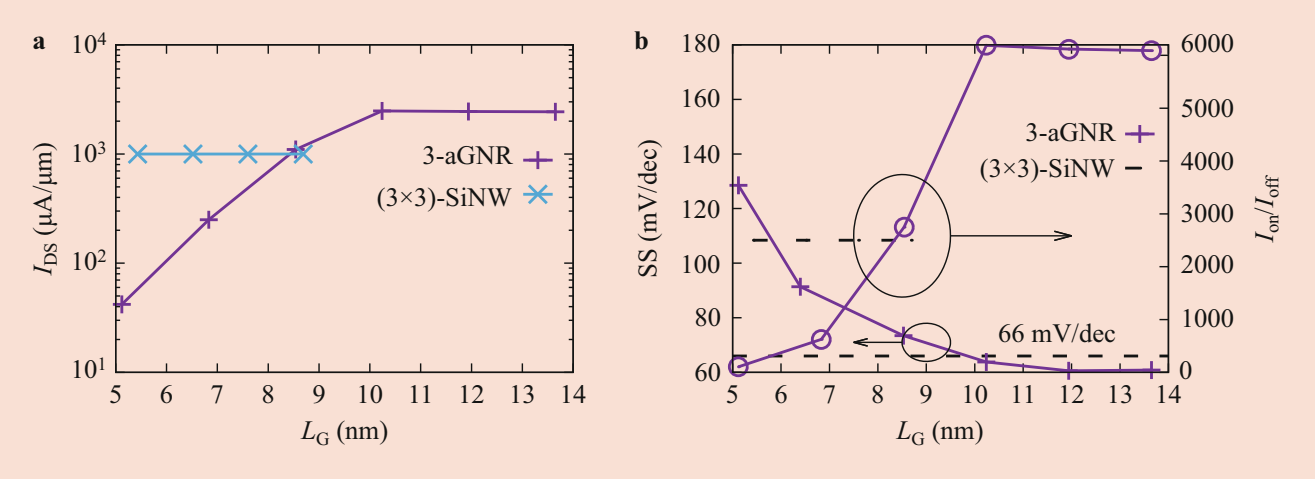

Fig. 42.34 (**a**) Drain-source current I_{DS} for 3-aGNRFETs and (3×3)-SiNWFETs with different L_G at $V_{DS} = 0.1$ V and $V_{GS} - V_{th} = 0.25$ V. (**b**) Subthreshold swing (SS) and I_{on}/I_{off} ratio as a function of L_G. The horizontal dashed line indicates the subthreshold swing, 66 mV/dec, for (3×3)-SiNWFETs in the given channel lengths. Lines connecting the symbols are a guide to the eye. (After Ref. [206], with permission from IEEE)

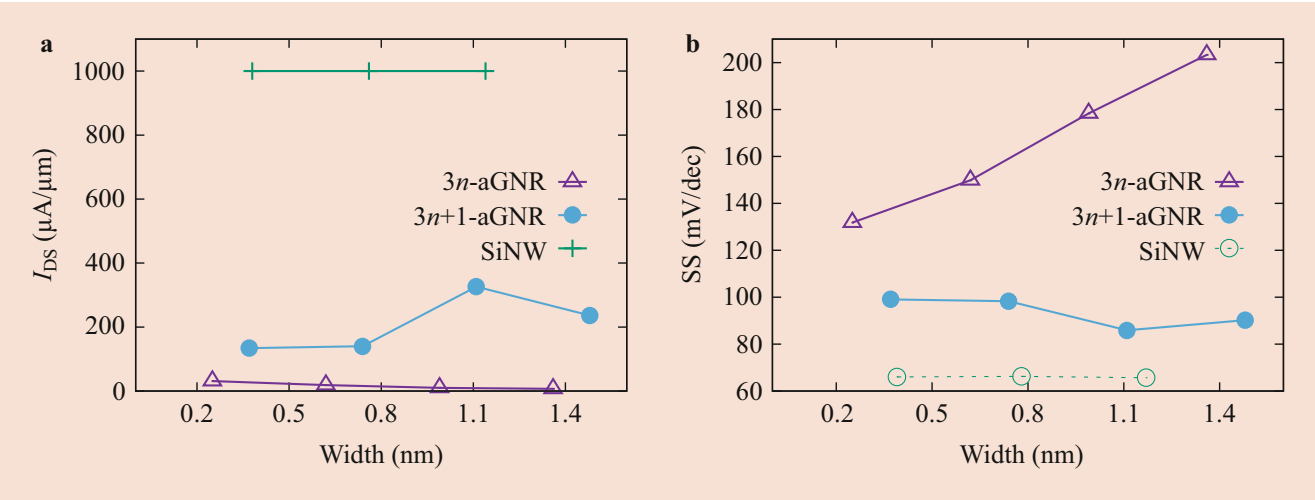

Fig. 42.35 (**a**) The current I_{DS} at $V_{DS} = 0.1$ V and $V_{GS} - V_{th} = 0.25$ V for aGNRFETs and SiNWFETs with different width and a similar gate length (~5 nm). (**b**) The SS as a function of width. The lines connecting the symbols are a guide to the eye. (After Ref. [206], with permission from IEEE)

current more than three times larger than aGNRFETs for the same gate length of 5 nm. To sum the studies shown above, SiNWFETs offer the avenue to scale transistors down to 5 nm channel lengths.

42.7 Conclusions and Outlook

So far, we have shown how DFT can be used to calculate electron-phonon scattering rates and transport properties of several bulk and two-dimensional materials. Comparing the power of these *ab initio* methods to what was possible as recently as 20 years ago (as discussed in Sect. 42.2), we can appreciate the enormous "cultural" value of the progress made. We must also express optimism about the possibility of investigating the transport properties of new materials without having to wait for expensive and time-consuming experiments that provide the information needed to assess the performance of devices based on these materials.

However, in a few occasions, we have also hinted at some uncertainty that still affects the accuracy and reliability of results obtained using *ab initio* methods. Broadly speaking, these difficulties originate from three causes: *(i)* the use of unsatisfactory approximations to calculate the carrier mobility and other transport characteristics, *(ii)* numerical "shortcuts" that reduce the computational efforts but introduce unwanted artifacts and errors, and *(iii)* intrinsic limitations of our knowledge of the basic physics.

(i) Regarding the accuracy and correctness of the formulations employed to compute transport characteristics, we have discussed in Ref. [97] how several results, labeled *ab initio*, rely on DFT calculations of the changes of the band structure under strain (the "proper" deformation potentials) to estimate the carrier mobility using oversimplified assumptions. To summarize what we wrote in Ref. [97] (and as also discussed in Refs. [234, 235]), these assumptions consists in the use of Takagi formula [236] to calculate the carrier mobility for a two-dimensional electron gas (2DEG):

$$\mu = \frac{e\hbar^3 C_{2D}}{k_B T m^* m_d E_1^2}, \tag{42.59}$$

where m^* and m_d are the conductivity and density-of-states effective masses, respectively, C_{2D} is the longitudinal or transverse elastic constant of the 2D material, and E_1 is the "proper" deformation potential mentioned above and calculated from the energy-shift, $\Delta E_{c,v}$, of the relevant band-edge (conduction for electron transport, valence for holes), under a relative change, $\Delta a/a_0$, of the lattice constant a_0:

$$E_1 = a_0 \frac{\Delta E_{c,v}}{\Delta a}. \tag{42.60}$$

This formula has been used to calculate extremely high values for the carrier mobility in silicene ($\approx 2 \times 10^5$ cm^2 V^{-1} s^{-1} for both electrons and holes [237]) and germanene ($\approx 6 \times 10^5$ cm^2 V^{-1} s^{-1} for both electrons and holes [238]), ignoring coupling to flexural acoustic modes [141]. Qiao et al. [137] have also used Eq. (42.59) to obtain an equally impressive electron and hole mobility in phosphorene. However, while approximately correct in the context of Si inversion layers, as originally intended by Takagi and coworkers, its validity should be considered carefully when extending it to other materials. Indeed, Eq. (42.59) accounts only for longitudinal phonons (unless the shear deformation potential is also accurately considered, as done in Ref. [144] for phosphorene), it ignores scattering with optical phonons, intervalley processes and ignores the anisotropy (*i.e.*, the dependence on the scattering angle) of the electron-phonon matrix element. This anisotropy is extremely important when estimating the carrier mobility, since it affects strongly the momentum relaxation rate. This has been shown even in bulk Si [36], strained bulk Si [239], and Si inversion layers [240]. Liao et al. [142] and Gaddemane et al. [97] have shown how this is also of paramount importance in monolayer phosphorene. Finally, Eq. (42.59) ignores effects that may result from the overlap integral of the initial and final wavefunctions, effects that are instead captured by the finite-displacement method or by DFPT. Therefore, the impressive values for the carrier mobility reported in Refs. [137, 237], among others, should be regarded as no more than extremely optimistic upper bounds.

Table 42.7 Theoretical calculations of the 300 K electron and hole mobility, μ_e and μ_h, in monolayer and bilayer phosphorene

Reference	μ_e (cm^{2}V^{-1}s^{-1})		μ_h (cm^{2}V^{-1}s^{-1})	
	Armchair	Zigzag	Armchair	Zigzag
Monolayers				
Qiao et al.[a]	1100	80	640–700	10,000–26,000
Jin et al.[b]	210	40	460	90
Rudenko et al.[c]	738	114	292	157
Rudenko et al.[d]	∼700		∼250	
Trushkov et al.[e]	625	82		
Liao et al.[f]	170	50	170	35
This work[g]	20	10	19	2.4
This work[h]	21	10	19	3
This work[i]	25	5		
Bilayers				
Qiao et al.[a]	600	140–160	2600–2800	1300–2200
Jin et al.[b]	1020	360	1610	760
This work[g]	14	7	12	2

After G. Gaddenane et al. [97], with permission from the American Physical Society ©2018 American Physical Society
[a]Ref. [137]
[b]Ref. [143], Monte Carlo and DFT (DFPT)
[c]Ref. [144], LA and TA, one-phonon processes
[d]Ref. [144], LA and TA, one- and two-phonon processes
[e]Ref. [145], LA and TA, at a density of 10^{13} electrons/cm^2
[f]Ref. [142], DFT (DFPT)
[g]Monte Carlo and DFT (finite differences), acoustic and optical phonons
[h]Monte Carlo and DFT (DFPT)
[i]Kubo-Greenwood, acoustic phonons only, elastic and equipartition approximation

We show in Table 42.7 (reproduced from Ref. [97]) the large discrepancies among the values of the electron mobility in phosphorene calculated using several different approximations or methods. As serious as the issue may be, paradoxically we should consider it a "minor problem," since reliable methods to calculate the electron mobility are available, such as the EPW computer package [77] and the by-now "conventional" full-band Monte Carlo simulations we have employed here.

(ii) Regarding numerical issues, we have also discussed in them in Ref. [97], and we have mentioned above in Sect. 42.4.1. These may be considered mundane issues, since the use of a sufficiently fine discretization of the Brillouin zone does not constitute an insurmountable conceptual obstacle. Even if today's hardware renders the task painful and (perhaps) impossible when dealing with high-energy transport, we are growing accustomed to ever-increasing computer resources, in terms of both speed and memory.

(iii) Much more fundamental are the reasons causing the dependence of the results on the choice of exchange-and-correlation functionals and even (very surprising to us) of the pseudopotentials used when performing *ab initio* calcula-

Table 42.8 Calculated electron mobility in monolayer WS_2

	SSSP-PBE without SO	ONCV-PBE without SO	ONCV-PBE with SO	ONCV-LDA without SO	ONCV-LDA with SO
Bandgap (eV)	1.81	1.835	1.56	1.99	1.66 (indirect)
ΔE_{KQ} (meV)	210	182	97	22	73
μ (cm^2/(Vs))	767	380	215	17	127

Table 42.9 Calculated electron mobility in monolayer TMDs

μ (cm^2/Vs)	SSSP-PBE without SO	ONCV-PBE without SO	ONCV-PBE with SO	ONCV-LDA without SO	ONCV-LDA with SO
MoS_2	127	147	145	127	116
$MoSe_2$	78	92	101	18	19
$MoTe_2$	49	43	50	17	11
WS_2	767	380	215	37	127
WSe_2	275	180	46	23	88
WTe_2	64	166	181	60	55

tions. In Sect. 42.4.3 we have already observed the surprising wide range of values for the calculated electron mobility in monolayer phosphorene that have been reported in the literature. Unfortunately, a similar puzzling observation can be made for monolayer TMDs. A typical example is provided by WS_2. As shown in Tables 42.8, the electron mobility calculated using DFT varies from a promising 767 cm^2/(Vs) to a disappointing 17 cm^2/(Vs). Indeed, different values are obtained when using different exchange and correlation functionals (PBE [94] or LDA [95]), different pseudopotentials ("standard solid-state pseudopotentials," SSSP [241] or "optimized norm-conserving," ONCV [242]) and depending on whether or not one accounts for the spin-orbit (SO) interaction.

The cause of this problem is twofold: first, the band structure of monolayer WS_2 shows conduction band minima at the six K symmetry points (the doubly degenerate K valleys) and local minima at a point along the Γ-K line (the sixfold degenerate Q valleys). The energy separation, ΔE_{KQ}, between these two sets of valleys obtained choosing different "flavors" of DFT using Quantum ESPRESSO [15, 16] varies between 22 and 210 meV. Since the K-Q intervalley scattering rates calculated using EPW [76] are quite strong, clearly different values of ΔE_{KQ} result in vastly different values of the mobility. In this case, we may blame the well-known inability of DFT – a ground-state theory thanks to the Hohenberg-Kohn theorems [243] – to reproduce the correct excitation spectrum with the accuracy required when performing transport calculations. However, in some sense, experimental information can guide us in choosing the proper combination of exchange-correlation functionals and pseudopotentials. In so doing, the problem is addressed very pragmatically, so that we have to accept some compromises in how we define the term "*ab initio*."

A similar problem affects our understanding of high-field electron transport in Si and GaN: regarding Si, Fig. 42.3 shows that DFT/EPW calculations yield peaks of the density of states at energies that are slightly smaller than those measured experimentally (and reproduced, by definition, by empirical pseudopotentials). This "compression" of the conduction bands results in a larger density of states that, in turn, results in scattering rates that are slightly larger than those predicted by rigid-(pseudo)ion calculations based on empirical pseudopotentials. Similarly, in GaN the energy of the satellite L-valleys computed from DFT seems to be inconsistent with some experimental data, as we have mentioned in Sect. 42.4.2. Ultimately and not surprisingly, the problem originates from the approximations that we must necessarily make in dealing with the exchange and correlation functionals that enter the Kohn-Sham equation. We should add, parenthetically, that accounting for the spin-orbit interaction still presents some fundamental issues.

Much more serious is the second cause of the broad range of calculated results. As shown in Table 42.9, even in materials in which intervalley scattering does not control transport, some differences are seen. If one may expect some dependence of the results on the choice made for the exchange-correlation functionals, more worrisome is the observation that even the choice made for the pseudopotentials matters. The situation is acceptable only in some particular cases, such as for MoS_2, but it remains generally unsatisfactory.

As a final important remark, we should note that results like those reported in Tables 42.8 and 42.9 have been obtained assuming free-standing 2D layers. Experiments are often performed on layers supported by insulating substrates, often also gated (occasionally supported *and* gated), and at a nonzero carrier density. Under these circumstances, dielectric screening by the dielectric environment (as reported for impurity scattering in Ref. [244]) and free-carrier screening may improve the mobility, whereas scattering with the hybrid plasmon/optical-phonon interface modes (often called "remote-phonon" scattering, somewhat improperly) may depress it. Therefore, comparison with experimental data should be made keeping these effects in mind.

If the choice of functionals and pseudopotential is an issue, using an all-electron method may solve the latter problem and employing the GW approximation may address the former issue. At present, such calculations are possible only in some particular cases (also employing the simpler G_0W_0 approximation). However, having already remarked how accustomed we have grown in witnessing the progress of numerical algorithms and computer hardware, we may speculate that in a not-too-distant future the term *ab initio*

will be considered synonymous of all-electron/GW, rather than DFT.

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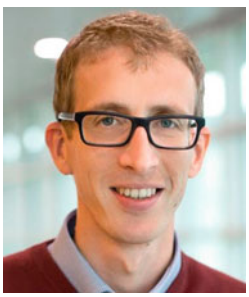

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Quantum Transport in the Phase Space, the Wigner Equation

43

Jean Michel Sellier and Philippe Dollfus

Contents

43.1 Why a Quantum Theory in the Phase Space? 1559

43.2 An Introduction to Standard Quantum Mechanics 1560

43.3 Quantum Mechanics in the Phase Space 1561
43.3.1 The Single-Body Problem 1561
43.3.2 The Many-Body Problem 1564
43.3.3 The Many-Body Liouville von Neumann Equation 1564
43.3.4 The Moyal Mathematical Formalization 1565
43.3.5 The Weyl Map and the Equations of Motion 1566
43.3.6 Admissible States in Phase Space 1566

43.4 Monte Carlo Methods to Simulate the Single-Body Wigner Equation 1566
43.4.1 The Affinity Method 1567
43.4.2 Affinity Evolution and Monte Carlo Algorithm 1568
43.4.3 Conservation of Affinity and Pseudo-Particle Injection 1568
43.4.4 Basic Validation for Typical Cases 1569
43.4.5 Application of the Affinity Method to Electronic Devices: The Resonant Tunneling Diode 1569
43.4.6 Electrical Characteristics 1570
43.4.7 Decoherence and Quantum/Semiclassical Transition 1571
43.4.8 The Signed Particle Method 1572

43.5 Monte Carlo Methods to Simulate the Many-Body Wigner Equation 1575
43.5.1 The Density Functional Theory 1576
43.5.2 The *Wigner* Density Functional Theory 1576
43.5.3 The Wigner Monte Carlo Method for Many-Body Systems 1577
43.5.4 Signed Particle Method 1577

43.6 Neural Networks to Compute the Kernel 1578

References 1580

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Abstract

In this chapter, we present and discuss the primary features of the Wigner equation and the related Monte Carlo techniques which allow quantum simulations in the phase space. We start by introducing some of the main aspects of the quantum theory. Afterwards, we proceed with the tenets of the Schrödinger formalism. It allows us to revise the details of such approach and to fix the notation we will use throughout this chapter. Then, we introduce and discuss the important role Monte Carlo methods have played in the field of applied physics and present the latest developments in the field of time-dependent, multidimensional, many-body, and full quantum simulations in the Wigner formalism. Two main techniques will be discussed and illustrated by some typical examples: one technique based on the concept of quantum affinity and the other one based on the concept of signed particles.

Keywords

Quantum mechanics · Wigner formulation · Quantum affinity · Signed particles · Monte Carlo methods

43.1 Why a Quantum Theory in the Phase Space?

Quantum mechanics was born from the necessity of explaining a series of experiments involving extremely small objects such as electrons, atoms, and molecules and which could not be approached in terms of classical mechanics. Puzzling concepts such as particle-wave duality and energy quantization were developed and utilized to describe physical observations for the first time. Since then, theoretical physicists have assembled a very successful set of rules which can explain and predict (impressively) the many ob-

served features of quantum systems. The modern approach to quantum mechanics was eventually made possible by the work of E. Schrödinger, completely describing quantum systems in terms of probability amplitudes or wave-functions (a revolutionary concept). A physical interpretation to this equation was provided, known as the standard or Copenhagen interpretation. This theory remains, to this day, the most rigorously tested theory in physics.

Right after the work of Schrödinger, other formulations and interpretations appeared, shedding a different light on different aspects of the theory. In this context, the work of E. Wigner stands out among the available (equivalent) alternatives as it is an intuitive approach which provides a direct connection between classical and quantum physics. In fact, it naturally creates a bridge with classical statistical mechanics which renders quantum mechanics a more natural theory: in this formulation, the description of quantum objects can completely be made in terms of quasi-distribution functions.

In spite of this intuitiveness, only recently we have observed a growing interest in the Wigner formulation of quantum mechanics. One plausible explanation is provided by the fact that the Wigner equation represents a challenging mathematical task, being a partial integro-differential equation where the unknown is a function defined over a $2 \times d \times n$ dimensional phase space, where d is the dimensionality of space ($d = 1, 2, 3$) and n is the number of involved particles or bodies (in this chapter, we use the terms body and particle interchangeably). Only very recently, Monte Carlo techniques have been designed which are capable of overcoming the many problems encountered with such model.

In this chapter, we focus on the Wigner equation and the related Monte Carlo techniques which allow quantum simulations in the phase space. Therefore, we start by introducing some of the main aspects of the quantum theory. Afterwards, we proceed with the tenets of the Schrödinger formalism. This is twofold. First, it allows us to revise the details of such approach, secondly it allows us to fix the notation we will use through this work. We, then, introduce and discuss the important role Monte Carlo methods have played in the field of applied physics and present the latest developments in the field of time-dependent, multidimensional, and full quantum simulations in the Wigner formalism. Two main techniques will be discussed: one based on the concept of *quantum affinity* and the other one based on the concept of *signed particles*. In the following, we suppose that the reader is familiar with the Schrödinger formulation of quantum mechanics.

43.2 An Introduction to Standard Quantum Mechanics

The time-dependent and time-independent Schrödinger equations are two linear partial differential equations which describe the state of a quantum system [1]. Both equations have played a crucial role in quantum mechanics and nowadays represent the standard approach. Several years after the appearance of Schödinger work, E. Wigner utilized one of these equations, the time-dependent one, as a starting point to create his own formalism [2]. Due to the importance it has gained during the years, in this section we briefly recall the tenets of the Schrödinger formulation. In the following, we adhere to the non-relativistic exposition of L.D. Landau [3].

The Born Rule A wave-function $\psi = \psi(\mathbf{x})$ completely describes a system. The probability of finding a particle around the position $\mathbf{x}$ in the interval $\mathrm{d}\mathbf{x}$ is given by its squared modulus $\psi^2(\mathbf{x})\mathrm{d}\mathbf{x}$. This heuristic rule is known as the Born rule [4]. In the general case, any other measurement can be predicted by a bilinear form:

$$\int \mathrm{d}\mathbf{x} \int \mathrm{d}\mathbf{x}' \psi(\mathbf{x}) \psi^*(\mathbf{x}') \phi\left(\mathbf{x}, \mathbf{x}'\right), \tag{43.1}$$

where the function $\phi = \phi(\mathbf{x}, \mathbf{x}')$ depends on the particular measurement performed. In particular, the probability of finding a particle at a certain given position is of the same form as (43.1) where $\phi(\mathbf{x}, \mathbf{x}') = 1$ for every $\mathbf{x}$ and $\mathbf{x}'$.

Principle of Superposition of States Given two valid wave-functions $\psi_1(\mathbf{x})$ and $\psi_2(\mathbf{x})$ for a system, and supposing that the state ψ_1 leads with certainty to a measurement $\mathbf{x}_1$ and the state ψ_2 leads with certainty to a measurement $\mathbf{x}_2$, then every linear combination of these two states $c_1\psi_1 + c_2\psi_2$ is an equivalently valid state for the given system (where c_1 and c_2 are two constants).

Operators For any physical quantity A, it is possible to construct an Hermitian (linear) mathematical operator $\hat{A}$ which eigenvalues a_n are the possible outcomes of the act of measurement of A [3]. The shape of the operator is determined by the particular measurement being performed. In the Schrödinger formalism, the only admissible operators are Hermitian ones.

The Momentum Operator In the Schrödinger formalism, the operator $\hat{p}$ corresponding to the momentum reads

$$\hat{p} = -i\hbar\nabla_{\mathbf{x}},$$

where i is the imaginary unit, $\hbar$ is the reduced Planck constant, and $\nabla_{\mathbf{x}} = \left(\frac{\partial}{\partial x}, \frac{\partial}{\partial y}, \frac{\partial}{\partial z}\right)$.

The Hamiltonian Operator The Hamiltonian operator has the following mathematical expression:

$$\hat{H} = \frac{\hat{p}^2}{2m} + U(\mathbf{x}, t) = -\frac{\hbar^2}{2m}\nabla^2_{\mathbf{x}} + U(\mathbf{x}, t), \tag{43.2}$$

with m the mass of the particle and $U = U(\mathbf{x})$ the potential energy of the particle in an external field and the operator $\nabla^2_{\mathbf{x}} = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}$.

The Time-Independent Schrödinger Equation The time-independent Schrödinger equation is an important milestone of quantum mechanics. It is an eigenproblem which eigenvalues represent the energy levels of a system. It describes quantum systems in the presence of a time-independent external field and reads:

$$\hat{H}\psi(\mathbf{x}) = E\psi(\mathbf{x}), \tag{43.3}$$

where $\hat{H}$ is the Hamiltonian operator of the system. Its solution formally reads as (E_n, ψ_n) for $n = 0, 1, 2, \ldots$, where the wave-functions ψ_n are also called stationary states. In particular, the function ψ_0 and the energy E_0 are known as the *ground state* function and energy, respectively. The reader should note that this equation implies the possibility for quantized energies.

The Time-Dependent Schrödinger Equation The evolution in time of the quantum state of a system is governed by the time-dependent Schrödinger equation which represents its most general description possible and reads

$$i\hbar\frac{\partial\psi(\mathbf{x}; t)}{\partial t} = \hat{H}\psi(\mathbf{x}; t). \tag{43.4}$$

The reader should note that, being a *linear* partial differential equation, the principle of superposition holds. This is a very peculiar characteristics which has no counterpart in classical mechanics.

43.3 Quantum Mechanics in the Phase Space

In his search for quantum corrections to classical thermodynamics, E. Wigner came up, in 1932, with a very peculiar, elegant, and intuitive formulation of quantum mechanics which involves familiar (classical) concepts such as the phase space and distribution functions [2]. We start this section with a focus on this formalism starting from the original work of Wigner and extending it to the case of mixed states. Afterwards, we proceed with the works of Moyal and Groenewold which provided firm mathematical foundations to this approach. These results eventually put the Wigner formalism on totally independent grounds. Finally, we conclude this section with a generalization of the single-body Wigner equation to the quantum many-body case and to systems of identical particles (with a particular attention to Fermions).

43.3.1 The Single-Body Problem

In this section, we describe the (single-body) formulation suggested by E. Wigner [2], which represents a peculiar and intuitive approach to quantum mechanics in the phase space. This is an important part of this chapter since it introduces many of the details related to the Wigner approach. The cases for the mixed states and for the many-body problem are directly connected to the pure state, single-body Wigner transport equation (WTE) presented in this section for coherent transport. Then, we introduce a simple approach frequently used to include scattering (dissipative) processes in the Wigner equation. It consists of using the Boltzmann collision operator for electron-phonon and electron-impurity interactions, which can be derived from the Wigner operator after a hierarchy of approximations.

The Single-Body Wigner Transport Equation

If one represents the state of a single-body quantum system by a wave-function $\psi(\mathbf{x}; t)$, it is possible to define the following transform:

$$f_{\mathrm{W}}(\mathbf{x}; \mathbf{p}; t) = \frac{1}{(\hbar\pi)^d}\int_{-\infty}^{+\infty} \mathrm{d}\mathbf{x}'\psi^*(\mathbf{x}+\mathbf{x}'; t)\psi(\mathbf{x}-\mathbf{x}'; t)\mathrm{e}^{-\frac{2i}{\hbar}\mathbf{x}'\cdot\mathbf{p}}, \tag{43.5}$$

(where $d = 1, 2, 3$ is the dimension of the spatial domain). It can be shown that the function $f_{\mathrm{W}} = f_{\mathrm{W}}(\mathbf{x}; \mathbf{p}; t)$ is real but not positive definite [2]; therefore, it is not a distribution function

(since it should be positive definite to qualify as such). However, this function has a very interesting and convenient mathematical property: when integrated with respect to **p**, it returns the following quantity:

$$\int_{-\infty}^{+\infty} \mathrm{d}\mathbf{p} f_{\mathrm{W}}(\mathbf{x};\mathbf{p};t) = |\psi(\mathbf{x};t)|^2,$$

which represents the probability of finding a particle in a certain position. Moreover, when integrated with respect to **x**, it returns the probability for the particle to have a certain momentum, i.e.,

$$\int_{-\infty}^{+\infty} \mathrm{d}\mathbf{x} f_{\mathrm{W}}(\mathbf{x};\mathbf{p};t) = \left| \int \mathrm{d}\mathbf{x} \psi(\mathbf{x};t) \mathrm{e}^{-\frac{i}{\hbar}\mathbf{x}\cdot\mathbf{p}} \right|^2.$$

Therefore, it is possible to calculate the space-dependent and space-independent expectation values, respectively $\bar{A}(\mathbf{x})$ and $< A >$, of any macroscopic variable defined as a function of coordinates and momenta $A = A(\mathbf{x};\mathbf{p})$, i.e.,

$$\bar{A}(\mathbf{x}) = \int_{-\infty}^{+\infty} \mathrm{d}\mathbf{p} A(\mathbf{x};\mathbf{p}) f_{\mathrm{W}}(\mathbf{x};\mathbf{p};t), \tag{43.6}$$

and

$$< A >= \int_{-\infty}^{+\infty} \mathrm{d}\mathbf{x} \bar{A}(\mathbf{x}) = \int_{-\infty}^{+\infty} \int_{-\infty}^{+\infty} \mathrm{d}\mathbf{x}\mathrm{d}\mathbf{p} A(\mathbf{x};\mathbf{p}) f_{\mathrm{W}}(\mathbf{x};\mathbf{p}).$$

It immediately follows that, in practice, one can still use the function f_{W} for the calculation of the variables $< A >$ and $\bar{A}(\mathbf{x})$ of a given macroscopic function $A(\mathbf{x};\mathbf{p})$ in spite of the fact that the function f_{W} is a quasi-distribution function. The reader should note, though, that the quantity $f_{\mathrm{W}}(\mathbf{x};\mathbf{p};t)$ cannot be interpreted as a probability for position and momentum of a particle simultaneously.

Now, knowing that the dynamics of a wave-function $\psi(\mathbf{x};t)$ is given by Eq. (43.4), and by making use of definition (43.5), it becomes possible to derive the time-dependent evolution equation for the quasi-distribution function $f_{\mathrm{W}}(\mathbf{x};\mathbf{p};t)$. In fact, the time derivative of the function $f_{\mathrm{W}}(\mathbf{x};\mathbf{p};t)$ [2] reads

$$\begin{aligned}
&\frac{\partial f_{\mathrm{W}}}{\partial t}(\mathbf{x};\mathbf{p};t) \\
&= \frac{1}{(\hbar\pi)^d} \frac{\partial}{\partial t} \int_{-\infty}^{+\infty} \mathrm{d}\mathbf{x}' \psi^*(\mathbf{x}+\mathbf{x}';t)\psi(\mathbf{x}-\mathbf{x}';t)\mathrm{e}^{\frac{2i}{\hbar}\mathbf{x}'\cdot\mathbf{p}} \\
&= \frac{1}{(\hbar\pi)^d} \int_{-\infty}^{+\infty} \mathrm{d}\mathbf{x}' \mathrm{e}^{\frac{2i}{\hbar}\mathbf{x}'\cdot\mathbf{p}} \left[\frac{\partial \psi^*}{\partial t}(\mathbf{x}+\mathbf{x}';t)\psi(\mathbf{x}-\mathbf{x}';t) \right. \\
&\quad \left. + \psi^*(\mathbf{x}+\mathbf{x}';t) \frac{\partial \psi}{\partial t}(\mathbf{x}-\mathbf{x}';t) \right],
\end{aligned} \tag{43.7}$$

where

$$\begin{aligned}
&\frac{\partial \psi}{\partial t}(\mathbf{x}-\mathbf{x}';t) \\
&= \frac{1}{i\hbar} \left[-\frac{\hbar^2 \nabla^2_{\mathbf{x}} \psi(\mathbf{x}-\mathbf{x}';t)}{2m} + U(\mathbf{x}-\mathbf{x}';t)\psi(\mathbf{x}-\mathbf{x}';t) \right].
\end{aligned} \tag{43.8}$$

Moreover, by using the complex conjugate of (43.4) one readily obtains

$$\begin{aligned}
&\frac{\partial \psi^*}{\partial t}(\mathbf{x}+\mathbf{x}';t) \\
&= \frac{1}{i\hbar} \left[\frac{\hbar^2 \nabla^2_{\mathbf{x}} \psi^*(\mathbf{x}+\mathbf{x}';t)}{2m} - U(\mathbf{x}+\mathbf{x}';t)\psi^*(\mathbf{x}+\mathbf{x}';t) \right].
\end{aligned} \tag{43.9}$$

By substituting (43.8) and (43.9) into (43.7), replacing the differentiations with respect to **x** by differentiations with respect to $\mathbf{x}'$, and performing partial integrations for the terms containing the operator $\nabla^2_{\mathbf{x}}$, one obtains

$$\begin{aligned}
\frac{\partial f_{\mathrm{W}}}{\partial t}(\mathbf{x};\mathbf{p};t) &= \frac{1}{(\hbar\pi)^d} \int_{-\infty}^{+\infty} \mathrm{d}\mathbf{x}' \mathrm{e}^{\frac{2i}{\hbar}\mathbf{x}'\cdot\mathbf{p}} \\
&\cdot \left\{ \frac{\mathbf{p}}{m} \left[-\nabla_{\mathbf{x}'} \psi^*(\mathbf{x}+\mathbf{x}';t)\psi(\mathbf{x}-\mathbf{x}';t) \right. \right. \\
&\quad \left. + \nabla_{\mathbf{x}'} \psi(\mathbf{x}-\mathbf{x}';t)\psi^*(\mathbf{x}+\mathbf{x}';t) \right] + \psi^*(\mathbf{x}+\mathbf{x}';t) \\
&\quad \left. \times \psi(\mathbf{x}-\mathbf{x}';t) \left[U(\mathbf{x}+\mathbf{x}';t) - U(\mathbf{x}-\mathbf{x}';t) \right] \right\}.
\end{aligned} \tag{43.10}$$

Finally, by replacing the differentiations with respect to $\mathbf{x}'$ back to **x**, one obtains the Wigner equation in the ballistic (collisionless) approximation:

$$\frac{\partial f_{\mathrm{W}}}{\partial t} + \frac{\mathbf{p}}{m} \cdot \nabla_{\mathbf{x}} f_{\mathrm{W}} = \int_{-\infty}^{+\infty} \mathrm{d}\mathbf{p}' V_{\mathrm{W}}(\mathbf{x};\mathbf{p}';t) f_{\mathrm{W}}(\mathbf{x};\mathbf{p}+\mathbf{p}';t), \tag{43.11}$$

with

$$\begin{aligned}
V_{\mathrm{W}}(\mathbf{x};\mathbf{p};t) &= \frac{i}{\pi^d \hbar^{d+1}} \int \mathrm{d}\mathbf{x}' \mathrm{e}^{-\left(\frac{i}{\hbar}\right)\mathbf{x}'\cdot\mathbf{p}} \\
&\quad \times \left[U\left(\mathbf{x}+\frac{\mathbf{x}'}{2};t\right) - U\left(\mathbf{x}-\frac{\mathbf{x}'}{2};t\right) \right],
\end{aligned} \tag{43.12}$$

known as the Wigner kernel, or potential, and where the function $U = U(\mathbf{x};t)$ can vary with time.

Equation (43.11) is known as the *Wigner equation*, or Wigner transport equation (WTE), and describes the dynamics of a single particle in the presence of an external potential expressed by the function $U(\mathbf{x};t)$. This equation will be the main focus of this chapter and has, in the phase-space formalism, the same place as the Schrödinger equation

(43.4) has in the standard formalism (in fact, they are mathematically equivalent). It represents a statistical approach to quantum mechanics, although not in a classical sense (f_W is not necessarily crypto-deterministic [5]). Moreover, in this rather different context, the emergence of classical mechanics can be easily explained [2].

Mixed States In practical experiments, one cannot always know which quantum state is being manipulated (e.g., in systems with a random preparation history). In this case, the pure state approach governed by Eq. (43.4) does not apply any longer, and the concept of density matrix becomes more suitable. It is possible to show, though, that the evolution equation for the Wigner function f_W remains unchanged. The interested reader is invited to read [6] for more details.

Scattering Effects: The Wigner-Boltzmann Transport Equation (WBTE)

The Wigner function approach allows to handle, in a natural way, open-boundary systems. Early works have investigated the theoretical and numerical properties of the coherent Wigner equation, appropriate for ballistic transport [7, 8]. However, in the real world of nanoelectronic devices, one cannot neglect the important role of decoherent and dissipative processes.

Dissipative interactions have been approached by means of phenomenological models based on the relaxation time approximation [9] and also by introducing an actual Boltzmann-like collision operator [10, 11]. It raised a fundamental question: Can the classical Boltzmann scattering operator and the quantum Wigner-potential operator reside in a common equation? The answer is not trivial: derivations from first principles and analysis of the assumptions and approximations have been provided only quite recently for interactions with ionized impurities [12] and with phonons [13], with two different approaches. The full derivation is beyond the scope of this chapter. We just summarized below the main steps.

Consider for instance the short-range Coulomb potential created by an ionized impurity $e^2 \exp(-\beta |\mathbf{r} - \mathbf{r}_i|)/4\pi E |\mathbf{r} - \mathbf{r}_i|$, where E is the semiconductor permittivity and β is the screening factor in the static screening approximation. The demonstration starts with the derivation of the Wigner potential associated with this Coulomb potential, from which a quantum evolution term is derived. After some tedious but straightforward calculations, considering a large number of dopants and within the fast collision approximation, the electron-impurity collision term finally takes exactly the same form as commonly derived for the Boltzmann collision operator with continuous doping density [14].

The semi-classical phonon collision is derived from the equation for the generalized Wigner function [15]. Along with the electron coordinates, the function depends on the occupation number of the phonon states in the system. We are actually interested in the electron, or reduced, Wigner function. It is obtained from the generalized Wigner function by a trace over the phonon coordinates. A closed equation for the reduced Wigner function can be derived after a hierarchy of approximations, which includes the weak scattering limit and assumes that the phonon system is in equilibrium [14]. The approximations only concern the interaction with phonons, while the potential operator remains exact. The Wigner-Boltzmann electron-phonon scattering operator is obtained after a classical limit in the phonon term, leading to the instantaneous and local Boltzmann operator.

It follows that, under some conditions, the collision term widely used in the Boltzmann transport equation (BTE) can also be used in the Wigner transport equation. It is a strong result and one of the main advantages of the Wigner function with regard to device modeling. All the knowledge acquired in the treatment of scattering in semi-classical transport can still be reused for quantum transport in the Wigner formalism. It makes it possible to study new problems such as scattering-induced decoherence and the transition from quantum to semi-classical transport regimes. The Wigner transport equation including the Boltzmann collision term is usually called the Wigner-Boltzmann transport equation (WBTE) [16]. As an extension of (43.11), it writes, finally

$$\frac{\partial f_W}{\partial t}(\mathbf{r}, \mathbf{p}, t) + \frac{\mathbf{p}}{m} \cdot \nabla_{\mathbf{x}} f_W(\mathbf{r}, \mathbf{p}, t) = Qf_W(\mathbf{r}, \mathbf{p}, t) + Cf_W(\mathbf{r}, \mathbf{p}, t) \tag{43.13}$$

where the Boltzmann collision term derives from the transition probabilities per unit of time $s_i(\mathbf{p}, \mathbf{p}')$ of each scattering process calculated in the first order perturbation theory of the Fermi golden rule [17], i.e.,

$$Cf_W(\mathbf{r}, \mathbf{p}, t) = \sum_i \int \mathrm{d}\mathbf{p}' \left[s_i(\mathbf{p}, \mathbf{p}') f_W(\mathbf{r}, \mathbf{p}', t) - s_i(\mathbf{p}', \mathbf{p}) f_W(\mathbf{r}, \mathbf{p}, t) \right]. \tag{43.14}$$

In the right hand side of (43.13), the quantum evolution term due to the potential U is given by

$$Qf_W(\mathbf{r}, \mathbf{p}, t) = \int \mathrm{d}\mathbf{p}' V_W(\mathbf{x}, \mathbf{p}', t) f_W(\mathbf{x}, \mathbf{p} + \mathbf{p}', t) \tag{43.15}$$

where the non-local effects of the potential appear in the Wigner potential V_W defined in (43.12).

This Wigner-Boltzmann approach of scattering cannot take into account quantum collision effects like collisional broadening and intra-collisional field effect related to the finite duration of the scattering processes. At this point, we should mention the Wigner paths method developed by Jacoboni's group at the University of Modena. This particle simulation technique makes it possible to go beyond the Wigner-Boltzmann equation since it can solve exactly

the Wigner equation without approximation on the electron/phonon coupling [15, 18–23]. It is based on the integral form of the Wigner equation and on a Neumann expansion of the Wigner function. Then, a subtle evolution of particle affinities and wave vectors is performed by following paths induced by the Wigner potential and phonon scattering. It is a rich tool for fundamental physics investigation but difficult to implement for device simulation.

Surprisingly, one of the most important results obtained using the Wigner paths technique is the fact that quantum collision effects play a reduced role inside devices, which tends to reinforce the validity of the Wigner-Boltzmann approach [24]. Indeed, the multiple collision processes tend to average the advanced effect of collisions, i.e., citing Bertoni: "multiple collisions reduce collisional broadening and contribute to understanding the success of the semiclassical approximation," which may explain the successful use of the Fermi golden rule beyond its expected theoretical limit.

43.3.2 The Many-Body Problem

We now introduce and discuss the time-dependent quantum many-body problem. At a first glance, the Wigner formulation does not seem to introduce any particular advantage over other approaches. In fact, the mathematics involved becomes incredibly complicated. Thanks to the Monte Carlo techniques nowadays available, though, this formalism brings a broad range of possibilities which would be hardly imaginable in other contexts.

We show now that one can define a many-body quasi-distribution function and that an evolution equation exists just as for the well-known single-body problem. For clarity, we first describe the problem in the Schrödinger formalism. Afterwards, we introduce the many-body Wigner equation. We conclude with a discussion on systems of indistinguishable particles in the phase space.

The dynamics of a system consisting of n interacting particles is described by a time-dependent Schrödinger equation similar to (43.4). The space of configurations now consists of the coordinates of n particles and reads

$$\mathbf{x} = (\mathbf{x}_1, \mathbf{x}_2, \ldots, \mathbf{x}_n), \tag{43.16}$$

where $\mathbf{x}_i = (x_i, y_i, z_i)$ are the spatial coordinates of the i-th particle, for $i = 1, 2, \ldots, n$, and the wave-function becomes a function of the n-body configuration space. Moreover, the many-body time-dependent Schrödinger equation reads

$$i\hbar \frac{\partial \psi}{\partial t}(\mathbf{x}_1, \mathbf{x}_2, \ldots, \mathbf{x}_n; t) = \hat{H}\psi(\mathbf{x}_1, \mathbf{x}_2, \ldots, \mathbf{x}_n; t), \tag{43.17}$$

where the Hamiltonian operator $\hat{H}$ reads

$$\begin{aligned}\hat{H} &= \hat{H}(\hat{\mathbf{x}}_1, \hat{\mathbf{x}}_2, \ldots, \hat{\mathbf{x}}_n; \hat{\mathbf{p}}_1, \hat{\mathbf{p}}_2, \ldots, \hat{\mathbf{p}}_n) \\ &= -\sum_{i=1}^{n} \frac{\hat{\mathbf{p}}_i^2}{2m} + U(\mathbf{x}_1, \mathbf{x}_2, \ldots, \mathbf{x}_n; t),\end{aligned} \tag{43.18}$$

with $\hat{\mathbf{x}}_i = (\hat{x}_i, \hat{y}_i, \hat{z}_i)$ and $\hat{\mathbf{p}}_i = -i\hbar\nabla_i = -i\hbar\left(\frac{\partial}{\partial x_i}, \frac{\partial}{\partial y_i}, \frac{\partial}{\partial z_i}\right)$, the position and momentum operators for the i-th particle respectively.

43.3.3 The Many-Body Liouville von Neumann Equation

In order to describe the dynamics of a many-body system, the Liouville von Neumann equation is modified accordingly to take into account the new shape of the configuration space and thus reads

$$\begin{aligned}&\frac{\partial \rho}{\partial t}(\mathbf{x}_1, \mathbf{x}_2, \ldots, \mathbf{x}_n) \\ &= \frac{1}{i\hbar}\left[H(\hat{\mathbf{x}}_1, \hat{\mathbf{x}}_2, \ldots, \hat{\mathbf{x}}_n; \hat{\mathbf{p}}_1, \hat{\mathbf{p}}_2, \ldots, \hat{\mathbf{p}}_n), \rho(\mathbf{x}_1, \mathbf{x}_2, \ldots, \mathbf{x}_n)\right],\end{aligned} \tag{43.19}$$

This can be considered as a generalization of the single-body Liouville von Neumann equation with the operator $\hat{H}$. It is important to note that, despite the mathematical structure of Eq. (43.19) is practically the same as the corresponding single-body equation, it is mathematically much more challenging, even when approached numerically. The same difficulty applies to the many-body Schrödinger equation. In fact, both models are defined over a $(n \cdot d)-$dimensional configuration space.

The Many-Body Wigner Equation

In the Wigner formulation as well, it is possible to follow the dynamics of a quantum system consisting of n interacting particles (or bodies) by means of a quasi-distribution function $f_W = f_W(\mathbf{x}; \mathbf{p}; t)$, where the phase space is now a $2 \cdot n \cdot d-$dimensional space $(\mathbf{x}; \mathbf{p}) = (\mathbf{x}_1, \mathbf{x}_2, \ldots, \mathbf{x}_n; \mathbf{p}_1, \mathbf{p}_2, \ldots, \mathbf{p}_n)$, and where $\mathbf{x}_i$ and $\mathbf{p}_i$ have the usual meaning. In the same way, it is possible to define the Wigner quasi-distribution function for the pure and mixed quantum states of a system of n particles. Indeed, the pure state Wigner function now reads:

$$\begin{aligned}f_W(\mathbf{x}; \mathbf{p}; t) = \frac{1}{(\hbar\pi)^{d \cdot n}} \int d\mathbf{x}' e^{-\frac{i}{\hbar}\sum_{k=1}^{n} \mathbf{x}'_k \cdot \mathbf{p}_k} \\ \times \Psi\left(\mathbf{x} + \frac{\mathbf{x}'}{2}; t\right) \Psi^*\left(\mathbf{x} - \frac{\mathbf{x}'}{2}; t\right),\end{aligned} \tag{43.20}$$

where $\Psi = \Psi(\mathbf{x}; t)$ is a Schrödinger many-body pure state, $\int d\mathbf{x}' = \int d\mathbf{x}'_1 \int d\mathbf{x}'_2 \ldots \int d\mathbf{x}'_n$, and $(\mathbf{x} \pm \frac{\mathbf{x}'}{2}) = (\mathbf{x}_1 \pm \frac{\mathbf{x}'_1}{2}, \mathbf{x}_2 \pm$

$\frac{\mathbf{x}'_2}{2}, \ldots, \mathbf{x}_n \pm \frac{\mathbf{x}'_n}{2}; t)$. Analogously, a definition can be given in the case of mixed states described by a many-body density matrix $\rho = \rho(\mathbf{x}; \mathbf{y}; t)$

$$f_{\mathrm{W}}(\mathbf{x}; \mathbf{p}; t) = \frac{1}{(\hbar\pi)^{d\cdot n}} \int \mathrm{d}\mathbf{x}' \mathrm{e}^{-\frac{i}{\hbar}\sum_{k=1}^{n} \mathbf{x}'_k \cdot \mathbf{p}_k} \rho\left(\mathbf{x} + \frac{\mathbf{x}'}{2}; \mathbf{x} - \frac{\mathbf{x}'}{2}; t\right). \tag{43.21}$$

If one applies the mathematical transform (43.20) to the many-body Schrödinger equation (43.17), one easily obtains the corresponding time-dependent many-body Wigner equation:

$$\frac{\partial f_{\mathrm{W}}}{\partial t}(\mathbf{x}; \mathbf{p}; t) + \sum_{k=1}^{n} \frac{\mathbf{p}_k}{m_k} \cdot \nabla_{\mathbf{x}_k} f_{\mathrm{W}} = \int \mathrm{d}\mathbf{p} f_{\mathrm{W}}(\mathbf{x}; \mathbf{p}; t) V_{\mathrm{W}}(\mathbf{x}; \mathbf{p}; t), \tag{43.22}$$

where $\int \mathrm{d}\mathbf{p} = \int \mathrm{d}\mathbf{p}_1 \int \mathrm{d}\mathbf{p}_2 \ldots \int \mathrm{d}\mathbf{p}_n$, m_k is the mass of the k-th particle, or body, and the many-body Wigner kernel $V_{\mathrm{W}} = V_{\mathrm{W}}(\mathbf{x}; \mathbf{p}; t)$ now reads

$$V_{\mathrm{W}}(\mathbf{x}; \mathbf{p}; t) = \frac{i}{\pi^{dn}\hbar^{dn+1}} \int \mathrm{d}\mathbf{x}' \mathrm{e}^{-\left(\frac{2i}{\hbar}\right)\sum_{k=1}^{n} \mathbf{x}'_k \cdot \mathbf{p}_k} \times \left[U(\mathbf{x} + \frac{\mathbf{x}'}{2}; t) - U(\mathbf{x} + \frac{\mathbf{x}'}{2}; t)\right]. \tag{43.23}$$

The function $U = U(\mathbf{x}; t) = U(\mathbf{x}_1, \mathbf{x}_2, \ldots, \mathbf{x}_n)$ represents the potential acting over the n bodies and, in general, it can vary in time.

Indistinguishable Fermions

A very interesting case consists of systems made of *indistinguishable Fermions*. In this section, we follow the work of Schram et al. [6]. Previously, we have shown that by applying the transform (43.21) to the many-body Liouville von Neumann equation (43.19), it is possible to obtain the many-body Wigner equation (43.22). The reader should note that no assumption has been made on the symmetry properties of the system [6].

Now, in the standard formalism, indistinguishable Fermions are described by antisymmetric wave-functions, which reads

$$\Psi(\mathbf{x}_1, \mathbf{x}_2, \ldots, \mathbf{x}_i, \ldots, \mathbf{x}_j, \ldots, \mathbf{x}_n; t) = -\Psi(\mathbf{x}_1, \mathbf{x}_2, \ldots, \mathbf{x}_j, \ldots, \mathbf{x}_i, \ldots, \mathbf{x}_n; t), \tag{43.24}$$

and, by taking into account the antisymmetric nature of the system, it is possible to define a (many-body) Weyl map for Fermions

$$f^{-}_{\mathrm{W}}(\mathbf{x}; \mathbf{p}; t) = \frac{1}{(\hbar\pi)^{d\cdot n}} \int \mathrm{d}\mathbf{x}' \mathrm{e}^{-\frac{i}{\hbar}\sum_{k=1}^{n} \mathbf{x}'_k \cdot \mathbf{p}_k} \times \Psi^{-}\left(\mathbf{x}_1 + \frac{\mathbf{x}'_1}{2}, \ldots, \mathbf{x}_n + \frac{\mathbf{x}'_n}{2}; t\right) \times \Psi^{-*}\left(\mathbf{x}_1 - \frac{\mathbf{x}'_1}{2}, \ldots, \mathbf{x}_n - \frac{\mathbf{x}'_n}{2}; t\right), \tag{43.25}$$

(the case for mixed states is similarly obtained in [6]). One can, thus, show that the many-body Wigner equation for indistinguishable Fermions is, again, Eq. (43.22) [6, 25]. This readily comes from the application of the transform (43.21)–(43.19) which does not depend on the symmetry of the system. Therefore, this proves that the Wigner formalism is already adapted to treat the case of antisymmetric systems [6]. This means, in particular, that the Pauli exclusion principle is directly embedded into the Wigner formalism without any *ad hoc* trick.

Consequently, the antisymmetric properties of a quantum system are defined through its initial conditions. In practice, when in presence of Fermions, one starts from a Slater determinant at time $t = 0$:

$$\Psi^{-}(\mathbf{x}_1, \ldots, \mathbf{x}_n) = \frac{1}{\sqrt{n!}} \begin{vmatrix} \phi_1(\mathbf{x}_1) & \phi_2(\mathbf{x}_1) & \ldots & \phi_n(\mathbf{x}_1) \\ \phi_1(\mathbf{x}_2) & \phi_2(\mathbf{x}_2) & \ldots & \phi_n(\mathbf{x}_2) \\ \ldots & \ldots & \ldots & \ldots \\ \phi_1(\mathbf{x}_n) & \phi_2(\mathbf{x}_n) & \ldots & \phi_n(\mathbf{x}_n) \end{vmatrix}. \tag{43.26}$$

It can be shown that this is equivalent to express the initial Wigner function as a sum of reduced single-particle Wigner functions and a number of integral terms [26, 27]. This process couples the involved Fermions together, in agreement with the fact that the corresponding initial Wigner function cannot be expressed as multiplications of independent wave packets.

43.3.4 The Moyal Mathematical Formalization

An important contribution to put the Wigner approach on solid mathematical foundations came from J. Moyal in 1949 who published a brilliant work on whether the phase-space approach was a proper statistical theory. In this attempt, he managed to merge the works of E. Wigner [2], J. von Neumann [28], H. Weyl [29], and H. Groenewold [30] in an elegant and firm mathematical framework [5]. In turn, this provides a way to connect classical mechanics to quantum mechanics, allowing a natural comparison between these very different theories. Furthermore, this work allows to avoid the use of operators for observables, a concept which, somehow, has always puzzled physicists. Below, we introduce the theory for the one-dimensional space, being the generalization to higher-dimensional spaces trivial.

43.3.5 The Weyl Map and the Equations of Motion

The Weyl map M_{W}, also known as the Wigner-Weyl transform, represents a fundamental mathematical tool in this context. It essentially is an isomorphism from the space of linear operators $\hat{A}$ to the space of functions $A(x; p)$ provided with a product $\cdot$ and a commutator $[.,.]$ defined over the phase space with a non-commutative product $*$, known as the Groenewold product [30], and bracket $[.,.]_{\mathrm{M}}$, known as the Moyal bracket [5]:

$$\left(\hat{A}\left(\hat{x};\hat{p}\right), \cdot, [.,.]\right) \rightarrow \left(A(x;p), *, [.,.]_{\mathrm{M}}\right).$$

Given a quantum operator $\hat{A} = \hat{A}\left(\hat{x};\hat{p}\right)$, expressed in terms of the position and momentum operators $\hat{x}$ and $\hat{p}$, the Weyl map is mathematically defined as

$$M_{\mathrm{W}}\left(\hat{A}\right)(x;p) = A(x;p) = \frac{\hbar}{2\pi}\int \mathrm{d}\xi \int \mathrm{d}\eta \mathrm{Tr}\left[\hat{A}\left(\hat{x};\hat{p}\right)\mathrm{e}^{i(\xi\hat{x}+\eta\hat{p})}\right]\mathrm{e}^{-i(\xi x+\eta p)}, \tag{43.27}$$

where Tr[.] is the trace of an operator and the exponential of an operator is defined as $e^{\hat{X}} = \sum_{l=0}^{+\infty}\frac{1}{l!}\hat{X}^l$. The Wigner mapping is invertible [31]. The Groenewold $*$-product and Moyal bracket $[.,.]$ can be defined in terms of the Weyl map: given two operators $\hat{A}$ and $\hat{B}$ which corresponding Weyl transforms are the functions $A = A(x; p)$ and $B = B(x; p)$ one has:

$$A * B = M_{\mathrm{W}}\left(\hat{A},\hat{B}\right) \tag{43.28}$$

$$[A,B]_{\mathrm{M}} = \frac{1}{i\hbar}(A*B - B*A) = \frac{1}{i\hbar}M_{\mathrm{W}}\left(\left[\hat{A},\hat{B}\right]\right). \tag{43.29}$$

According to the above mathematical definitions, the Wigner quasi-distribution function can now be defined as the Weyl transform of the density matrix operator multiplied by a normalization factor; in other words,

$$f_{\mathrm{W}}(x;p;t) = \frac{1}{2\pi\hbar}M_{\mathrm{W}}\left(\hat{\rho}(t)\right). \tag{43.30}$$

In the case of pure states, one can show that [31]

$$f_{\mathrm{W}}(x;p;t) = \frac{1}{2\pi}\int \mathrm{d}y\psi^*\left(x+\frac{\hbar y}{2};t\right)\psi\left(x-\frac{\hbar y}{2};t\right)\mathrm{e}^{-iyp} = \frac{1}{\hbar\pi}\int \mathrm{d}x'\psi^*(x+x';t)\psi(x-x';t)\mathrm{e}^{-\frac{2i}{\hbar}x'\cdot p},$$

which is equivalent to formula (43.5). As expected, one can show that the function $f_{\mathrm{W}}(x; p; t)$ is square integrable, normalized, and real, but not positive defined.

The Evolution Equations One can now obtain the time-dependent evolution equation for the Wigner function $f_{\mathrm{W}}(x; p; t)$. By supposing that the wave-function $\psi(x; t)$ is a solution of the Schrödinger equation (43.4), one can show that the function f_{W} obeys the following evolution equation:

$$\frac{\partial f_{\mathrm{W}}(x;p;t)}{\partial t} = [H, f_{\mathrm{W}}(x;p;t)]_{\mathrm{M}}, \tag{43.31}$$

which corresponds to the single-body Wigner equation in the Moyal formalism, and it is equivalent to Eq. (43.11). In this formulation of quantum mechanics, this is the equivalent to the time-dependent Schrödinger equation (43.4).

43.3.6 Admissible States in Phase Space

More recently, Tatarskii [7] and Dias and Prata [31] have provided a mathematically and physically sound definition of admissible states in the phase-space formulation of quantum mechanics, along with their conditions and properties for both pure and mixed states. This helps to define what properties a phase-space function must have in order to be a valid description of a quantum state. It also shows that the Wigner formalism can be defined completely independently from the Schrödinger formulation.

43.4 Monte Carlo Methods to Simulate the Single-Body Wigner Equation

Monte Carlo methods provide approximations of the solution of a given computational problem by exploiting random processes. In other words, such methods are capable of computing statistical estimates for any linear functional of the solution by performing random sampling of a certain random variable whose mathematical expectation is the desired functional [32]. In practice, this class of numerical methods reduces a given problem to the approximation of some mathematical expectation. They are well known to represent powerful tools when it comes to solve problems in mathematics, physics, and engineering where the deterministic methods hopelessly break down since their strength consists in not requiring any additional regularity of the solution. Moreover, it is always possible to control the accuracy of the solution in terms of the probability error, a very important feature to control the correctness of a solution. Another important advantage of these methods consists in their high efficiency in dealing with very large computational problems such as multidimensional integration, very large linear systems, partial integro-differential equations in highly dimensional spaces, etc. Finally, they are extremely efficient on parallel processors and parallel machines, a very interesting feature

due to the availability of modern hardware such as multi-core CPUs and GPUs.

The year 1949 is generally considered to be the official birthday of the Monte Carlo method in the Physics community [33], but it is fair to note that much earlier applications can be found in the scientific literature; see, for example, the work of the French mathematician Georges-Louis Leclerc in 1777 (L'aiguille de Buffon, the Buffon's needle) [34]. As pointed out by Marquis Pierre-Simon de Laplace in 1886, his approach can be utilized to compute the value of the number π, in other words the first Monte Carlo method to evaluate the number π. With the advent of modern computational resources based on electronics, intensive applications eventually started to be developed in the context of the Manhattan project (Los Alamos, USA), by J. von Neumann, E. Fermi, G. Kahn, and S.M. Ulam. The legend says that the name *Monte Carlo* was eventually suggested by N. Metropolis in honor of Ulam's uncle who was a well-known gambler. Nowadays, Monte Carlo algorithms exist to solve a plethora of different computational problems, and it would be practically impossible to specify an even barely complete list.

Nowadays, Monte Carlo methods can be divided into two main classes: (1) Monte Carlo simulations and (2) Monte Carlo numerical methods. The first one represents a class of algorithms which directly simulate physical processes by miming the corresponding physical laws, e.g., the very well-known Boltzmann Monte Carlo method for the simulation of electron transport in semiconductor devices [35]. The second class, instead, exploits stochastic numerical algorithms for the resolution of computational problems such as linear systems, eigenproblems, evaluation of multidimensional integrals, etc. and does not represent the focus of this chapter. The interested reader is invited to refer to works such as [36].

It should be mentioned that some works dedicated to the direct solution of the Wigner or Wigner-Boltzmann equation for device simulation have been successfully achieved, but either using the ballistic approximation [37], using a simplified relaxation time approximation to incorporate scattering [38], or using a more rigorous Boltzmann collision operator but limited to elastic acoustic phonon scattering and surface roughness scattering [39].

In this section, we focus on two different Monte Carlo methods for the time-dependent solution of the Wigner equation. Recently, several techniques to solve this very complex problem have been suggested, developed, and validated very successfully, one being based on the concept of *particle quantum affinity* [40–43] (inspired by the pioneering works [44, 45]) and the other being based on the concept of *signed particles* [46, 47]. Their equivalence has been investigated in [48] and is out of the scope of this chapter.

As for the subject of Sects. 43.4.1, 43.4.2, 43.4.3, and 43.4.4, the interested reader may find a more extended treatment in [43], pp. 71–86.

43.4.1 The Affinity Method

Principles This method is actually strongly inspired by, and extrapolated from, the traditional Monte Carlo method for solving the Boltzmann transport equation (BTE) that proved to be very efficient in simulating semiconductor devices. In the case of the single-body BTE, classical particles are simply described as Dirac excitations of the form

$$f_j(\mathbf{r}, \mathbf{p}, t) = \delta(\mathbf{r} - \mathbf{r}_j)\delta(\mathbf{p} - \mathbf{p}_j), \tag{43.32}$$

and the Boltzmann distribution function is just a sum of such particles.

Since it can take negative values, it may look nonsensical to represent the Wigner function with particles which cannot have a "negative presence." Classically, electrons either do or do not exist. To solve this apparent inconsistency with a view to developing a statistical particle approach to the solution of the WTE or the WBTE, it is necessary to give simulated particles the strange property to carry negative contributions. With this in mind, it has been suggested that the Wigner function be described as a sum of Dirac excitations of the form [41]

$$f_j(\mathbf{r}, \mathbf{p}, t) = \delta(\mathbf{r} - \mathbf{r}_j)\delta(\mathbf{p} - \mathbf{p}_j)A_j(t) \tag{43.33}$$

which are still localized in the phase space but weighted by an amplitude, usually called "affinity." This amplitude was not necessary to consider for the solution of the BTE since the Boltzmann function is always positive, but it is required to reconstruct the Wigner function which can take negative values. Accordingly, this amplitude may be negative too. The particle amplitudes will contain all the information on the quantum state of the electron system. Consistently with the Heisenberg inequalities, such excitations, which we will call pseudo-particles, cannot represent physical particles. They are just to be considered as mathematical tools for the solution of the WBTE. The advantage of this formulation is that the evolution of these excitations follows simple equations. In the signed particle technique, the affinity can just take integer values, either $+1$ or -1, but in the present "affinity" approach, it can take real values and evolves continuously. In this approach, initially suggested by Shifren, Ringhofer, and Ferry [49], the interpretation of the quantum evolution term is different from that of the signed particle technique. This term does not generate here some events determined by an MC technique, but it is considered to act continuously on the particle affinity at each time step. Only the collision term is assumed to generate random events, as in Boltzmann simulation.

43.4.2 Affinity Evolution and Monte Carlo Algorithm

The method is thus very similar to the Boltzmann Monte Carlo technique [17]. The main change consists in adding at each time step the update of the Wigner function and of the particle affinities. In a mesh of the phase-space $M(x, k)$, the quantum evolution term Qf_{W}, i.e., the right-hand side of the Wigner equation (43.11), induces the change of the affinity of particles in the mesh according to

$$\sum_{i\in M(x,p)} \frac{\mathrm{d}A_i}{\mathrm{d}t} = Qf_{\mathrm{W}}(x,p) = \int \mathrm{d}p' V_{\mathrm{W}}(x,p',t) f_{\mathrm{W}}(x,p-p',t), \tag{43.34}$$

which means that at each time step the affinity of all pseudo-particles in a mesh of the phase space is updated as a function of Qf_{W}. The simple idea on which is based this quantum Monte Carlo simulation now appears clearly. During a time step, the real and momentum space coordinates of pseudo-particles evolve as in conventional MC simulation. In other words, if the potential has been separated in slowly and rapidly varying parts, i.e., $U(\mathbf{r}) = U_{\mathrm{slow}}(\mathbf{r}) + U_{\mathrm{rapid}}(\mathbf{r})$ the coordinates of the j-th obey, in the effective mass approximation,

$$\begin{aligned} \frac{\mathrm{d}\mathbf{r}_j}{\mathrm{d}t} &= \frac{\mathbf{p}_j}{m} \\ \frac{\mathrm{d}\mathbf{p}_j}{\mathrm{d}t} &= -\nabla_{\mathbf{r}} U_{\mathrm{slow}}(\mathbf{r}) \end{aligned} \tag{43.35}$$

If the whole potential is included in the quantum evolution term, i.e., $U_{\mathrm{slow}}(\mathbf{r}) = 0$, the momentum of each particle is constant during a free flight and can take a new value only after scattering.

In the semi-classical limit, i.e., if the full potential is treated as a slowly varying quantity $U(\mathbf{r}) = U_{\mathrm{slow}}(\mathbf{r})$, the quantum evolution term Qf_{W} is zero, and the particle affinity is constant. The method turns out to be equivalent to the semi-classical Monte Carlo simulation. It should be noted that the strong similarity and even compatibility of this technique with the conventional MC solution of the BTE is one of its highest advantage. In summary, the Monte Carlo technique for solving the WBTE consists here of describing statistically the motion of each pseudo-particle as a succession of free flights interrupted by instantaneous scattering events. Prior to the simulation, the scattering rates are evaluated as function of energy and stored in a lookup table. The duration of free flights is randomly selected from the total scattering rate. The computation of free-flight duration is simplified by introducing a fictitious "self-scattering," the rate of which is adjusted to make the total scattering rate energy-independent. During a free flight the particle coordinates evolve according to classical laws (43.35), while its affinity is adjusted according to (43.34). At the end of a free flight, the scattering process responsible for the free flight interruption is randomly selected on the basis of the scattering rate of each possible mechanism according to the carrier state. Once the scattering mechanism is known, the final state can be selected according to the angular dependence of the scattering rate. The details of the derivation of various types of scattering rates in the first-order perturbation theory and of the random selection procedure may be found in many textbooks, e.g., in [17, 50].

In the case of device simulation self-consistently coupled to Poisson's equation, the ensemble Monte Carlo simulation consists of simultaneously simulating the time behavior of a large number of particles during very small time steps (typically 0.1–10.0 femtoseconds (fs) depending on the timescales of relevant phenomena, such as the dielectric relaxation time and plasma frequency). The Poisson equation is solved at the end of each time step with updated carrier density distribution and, possibly, new electrostatic potential at contacts. The Wigner kernel and the quantum evolution term Qf_{W} are updated as well.

43.4.3 Conservation of Affinity and Pseudo-Particle Injection

One of the most important difficulties in this MC method lies in the fact that even a particle with zero affinity may gain finite affinity through the quantum evolution term Qf_{W} according to (43.34). It means that if there is no particle in a particular region of the phase space where the affinity should evolve, a significant error may occur with possible non-conservation of charge since the contribution of each particle to the total charge in the device is weighted by its affinity. This problem is very important for device simulation and should be fixed by implementing an appropriate algorithm to inject particles of convenient affinity.

The technique proposed in [51] has proved to give good results. It can be described as follows. After each time step, the quantum evolution term $Qf_{\mathrm{W}}(\mathbf{x}, \mathbf{p})$ is calculated in the full phase space. If in a mesh $M(\mathbf{x}, \mathbf{k})$ of the phase space, even inside the device, the quantity $|Qf_{\mathrm{W}}(\mathbf{x}, \mathbf{p})|$ is finite, or greater than a threshold value, a pseudo-particle of zero affinity is injected in the mesh.

This injection procedure must come in addition to the injection of particles at Ohmic contacts, as commonly done in semi-classical device simulation, for which the only condition of particle injection is the neutrality of real-space cells adjacent to the Ohmic contacts. After each time step, if particles are missing in some "Ohmic" cells with respect to the charge neutrality, the appropriate number of carriers (of affinity equal to 1) is injected in these cells to recover the neutrality. Assuming these "Ohmic" regions to be in

thermal equilibrium, an equilibrium distribution is used to randomly select their momentum components. In this way, the consistence between the distribution of potential and the average number and distribution of particles in the device is reached. Obviously, this condition of particle injection should still be used in quantum simulation of Ohmic contacts within the Wigner equation if the transport in the contact region is assumed to be essentially semi-classical.

In summary, in the case of WBTE simulation, it is necessary to combine the "semi-classical injection" of particles of 1 affinity at Ohmic contacts to guarantee the electrical neutrality near the contacts and the "quantum injection" of pseudo-particles of 0 affinity in all regions of the phase space where particles are missing and Qf_W takes significant values. Though it works well, the disadvantage of this "quantum injection" is that it is demanding in terms of CPU time, because of the large number of pseudo-particles required to fill the phase space for a good evaluation of the Wigner function.

Other numerical issues regarding the discretization schemes and the calculation of the Wigner kernel must be carefully considered. They are beyond the scope of this book chapter but are discussed in details in [43]. Additionally, important considerations regarding the boundary conditions [52,53] and the way to carefully incorporate scattering in the Wigner formalism [54,55] have been recently discussed.

43.4.4 Basic Validation for Typical Cases

It has been verified that this affinity technique of Wigner MC simulation is able to reproduce quantum mechanical effects accurately. It consisted in simulating the interaction of a ballistic Gaussian wave packet with a tunnel barrier, without any scattering term [43]. Such a simple situation without collision term can be solved easily from the time-dependent Schrödinger equation. In the probability density plotted in Fig. 43.1, a good agreement is shown between the particle approach of the WTE and the solution of the Schrödinger equation at time $t = 80$ ps after the starting of the interaction, when we see clearly the separation between transmitted and reflected wave packets. In particular, the oscillations of the wave-function are very well reproduced. This shows that the method can accurately model the existence of space correlations and interferences. However, it should be noted that some particle noise inherent in the method remains visible.

It has been shown also that semi-classical transport can be very well reproduced by using the quantum evolution term Qf_W to describe the effect of a slowly variable potential. A simple GaAs $N^+/N/N^+$ structure was considered, with N^+ regions doped to $10^{18}\,cm^{-3}$ and the 50 nm-long central region doped to $10^{16}\,cm^{-3}$. No quantum effects are expected to occur in such a structure. The conduction band structure

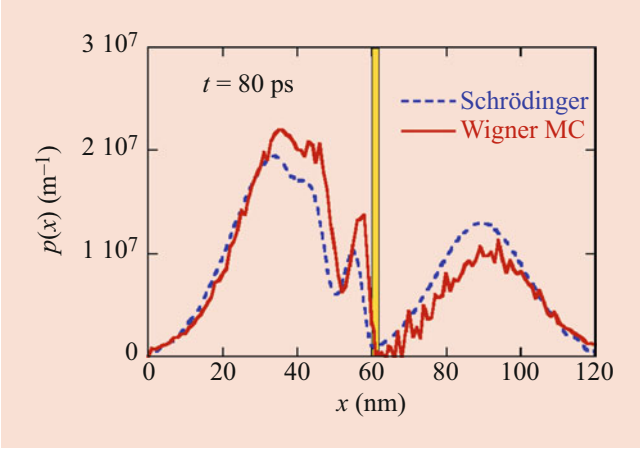

Fig. 43.1 Probability density resulting from the coherent interaction of a wave packet coming from the left with a square tunneling barrier at $t = 80$ ps after the starting of interaction, obtained from both Schrödinger equation and Wigner Monte Carlo simulation

was limited to the Γ valley with an effective mass of 0.6 m_0. The scattering mechanisms included in the collision term of the transport equation were interactions with acoustic phonons, polar optical phonons, and ionized impurities, at room temperature. The transport simulation was self-consistently coupled with the 1D Poisson equation. It was performed using both the semi-classical and the quantum MC models. In the latter case, the Poisson potential was fully included in the quantum evolution term, which means that the electron momentum is constant during free flights and may change only when the electron is scattered by a phonon or an impurity. After each time step, the Wigner potential associated with the Poisson potential is recalculated, and the affinity of particles is updated according to (43.34).

As expected, the I-V characteristics plotted in Fig. 43.2 are identical for semi-classical and quantum treatment of the potential. The results are superimposed on three orders of magnitude of current and voltage. It clearly shows that in semi-classical situation, i.e., for slowly varying potential, the semi-classical evolution of momentums and the quantum evolution of affinities are fully equivalent, though these two treatments are mathematically strongly different.

43.4.5 Application of the Affinity Method to Electronic Devices: The Resonant Tunneling Diode

Conveniently, coupled to the 1D or 2D Poisson equation within a self-consistent procedure, the affinity method described in Sect. 43.4.1 for solving the Wigner-Boltzmann transport equation has been successfully applied to a wide range of nanoelectronic devices or quantum problems, like the resonant tunneling diode (RTD) [51,56], silicon double-

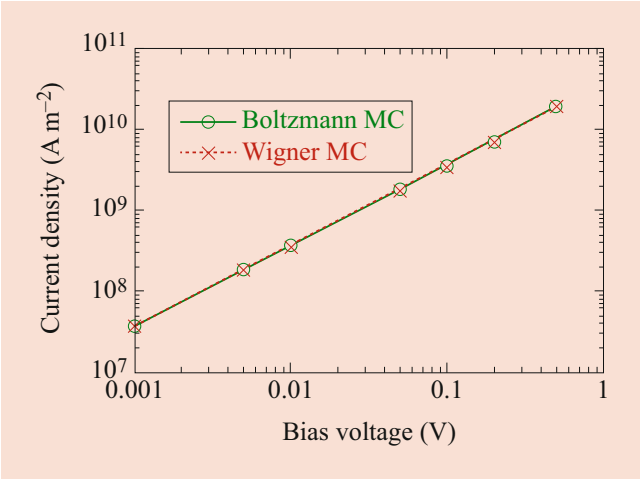

Fig. 43.2 Current-voltage characteristics for a 50 nm/50 nm/50 nm $N^+/N/N^+$ GaAs structure using semi-classical and quantum Wigner Monte Carlo simulation, including phonon and ionized impurity scattering. (After [43], with permission from Querlioz and Dollfus)

gate MOSFET [57, 58], the CNT-FET [59], GaAs/GaAlAs superlattices [60], or the phonon-induced decoherence effects [61].

Here, we restrict the discussion to the RTD that is certainly the simplest device operating at room temperature in which the wave-like behavior of electrons plays a prominent role. The operation of this device is based on the control of tunneling through the resonant state of a quantum well, e.g., GaAs, coupled to two leads via tunnel barriers, e.g., AlGaAs [62]. It results in a negative differential resistance (NDR) in the I-V characteristics. After the first experimental demonstration of this behavior at low temperature [63] and at room temperature [64], the RTD has been the subject of intense research both for its high potential of applications and for fundamental quantum device physics.

The NDR of the I-V characteristics may be used indeed for many electronic applications indeed [65], and for most of them, the peak-to-valley ratio (PVR) IP/IV of this characteristics is an important figure of merit. The RTD is often made of a GaAs quantum well with AlGaAs tunnel barriers, but other materials offering higher tunnel barriers, e.g., InGaAs or InAs quantum well between AlAs barriers, may be used to enhance the PVR up to 14 or even 30 at room temperature [66, 67]. Another important feature of the RTD comes from the very short lifetime of the quasi-bound states, which is the typical time constant associated with the operation of this tunneling device. If other transit times and parasitics are well controlled, the RTD may potentially operate in the THz regime.

Some typical results obtained on this device are presented here and we briefly discuss the physics of decoherence induced by electron-phonon scattering.

43.4.6 Electrical Characteristics

The simulated GaAs/GaAlAs RTD consists of a 5 nm-thick quantum well sandwiched between two AlGaAs barriers 0.3 eV high and 3 nm wide (Fig. 43.3). The quantum well, the barriers, and 9.5 nm-thick buffer regions surrounding the barriers are slightly doped to $10^{16}\,\mathrm{cm}^{-3}$. The 50 nm-long access regions are doped to $10^{18}\,\mathrm{cm}^{-3}$. Simulation was made at room temperature, including scattering with polar optical phonons, acoustic phonons and ionized impurities, for a single Γ valley with effective mass of 0.06 m_0. The Wigner-Boltzmann Monte Carlo (WBMC) algorithm was self-consistently coupled with the 1D Poisson equation.

In the current-voltage characteristics plotted in Fig. 43.4, the result obtained by including scattering (circles, solid line) is compared with that obtained from ballistic simulation, i.e., with scattering mechanisms artificially deactivated (squares, solid line). The curve obtained with scattering rates artificially multiplied by 5 (diamonds, dashed line) will be considered later, in the study of decoherence. It is clearly shown here that scattering effects significantly reduce the peak-to-valley ratio. We observe both a reduction of the peak current and an enhancement of the valley current. The latter effect is expected. In the valley regime where the coherent current is small, scattering induces an additional uncoherent path that generates an additional contribution to the current. In resonance (peak current) regime, when scattering is included a potential drop appears in the emitter region while the conduction band is flat in the ballistic case (see Fig. 43.5). This potential drop and the effect of inelastic scattering tend to induce an energy spreading of electrons, which reduces the fraction of electrons satisfying the resonant condition through the double barrier. It thus contributes to the suppression of current peak at the resonance, as observed in Fig. 43.4. It is thus essential to properly consider scattering mechanisms and self-consistence for room-temperature simulation of RTDs.

It should be noted that the peak-to-valley ratio obtained from such simulation for typical GaAlAs/GaAs RTDs at room temperature and 77 K has been found in good agreement with experimental data [51], which suggests this MC technique is actually able to provide realistic results for nanodevices exhibiting quantum transport effects with significant rates of scattering.

It is very instructive to examine the phase-space cartography of the Wigner function displayed in Fig. 43.6. Near the contacts, i.e., for $x < 40$ nm and $x > 120$ nm, the Wigner function appears to be very close to a displaced Maxwellian function, which is the signature of semi-classical transport regime in these regions. In contrast, the situation is very different in the quantum well. For the resonant state, i.e., $V = 0.3$ V (Fig. 43.6a), we can see between the barriers (schematized by vertical dashed lines) a peak (a spot) centered on $k =$

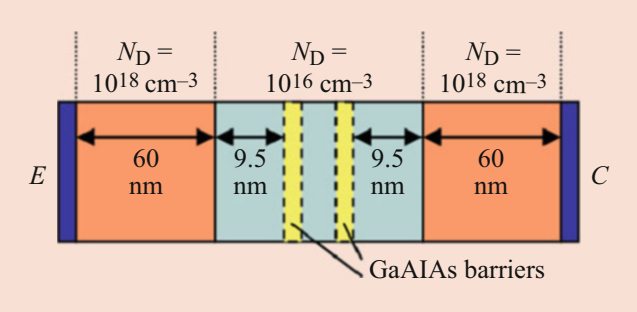

Fig. 43.3 Schematic cross-section of the simulated resonant tunneling diode. The GaAlAs barriers and the GaAs quantum well are 3 nm- and 5 nm-thick, respectively. (After [43], with permission from Querlioz and Dollfus)

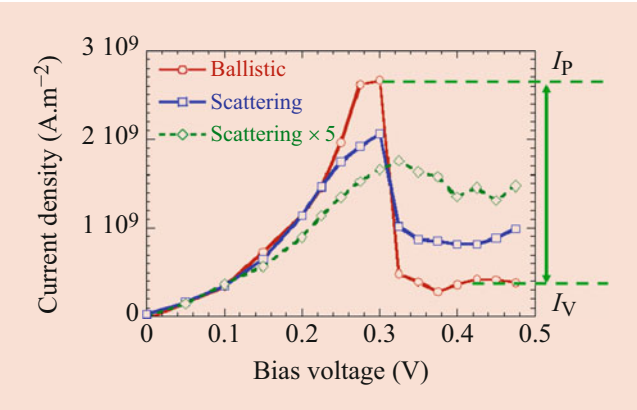

Fig. 43.4 I-V characteristics for the RTD obtained from WBMC simulation, with scattering artificially deactivated (circles), with standard scattering (squares), and with scattering rates artificially multiplied by 5 (diamonds). (After [43], with permission from Querlioz and Dollfus)

0 similar to that obtained for the Wigner function associated with the first energy level of a square quantum well. This peak is due to the contribution of electrons crossing the double-barrier through the resonant state in the well. For a non-resonant state (Fig. 43.6b), this peak vanishes and becomes almost invisible. It should also be noted that, in both cases, the oscillations of the Wigner function give rise to negative values in small regions of the phase space (dark blue areas), which is the signature of quantum coherence.

43.4.7 Decoherence and Quantum/ Semiclassical Transition

Let us come back to Fig. 43.6a that shows the Wigner function of the RTD operating at peak voltage ($V = 0.3$ V). In a large part of access regions ($x < 30$ nm and $x > 120$ nm), the transport is essentially semi-classical, and the Wigner function matches very well a semi-classical distribution function represented by a displaced Maxwellian function. In the

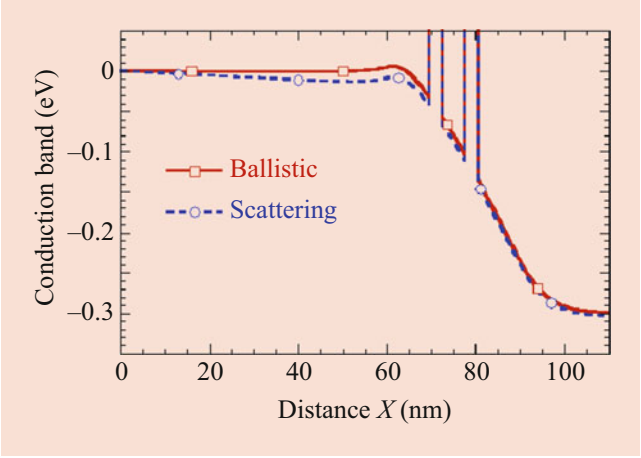

Fig. 43.5 Conduction band profile obtained by Wigner simulation, at resonance ($V = 0.3$ V), from either ballistic simulation (solid line) or including scattering (dashed line). (After [43], with permission from Querlioz and Dollfus)

overall active region of the device, oscillations of the Wigner function reveal the presence of spatial coherence. Hence, there is apparently a transition between coherent quantum and semi-classical regions within the device. To understand better this behavior and the de-coherence effect, it is insightful to analyze the density matrix (obtained by inverse Fourier transform of the Wigner function) for different strengths of electron-phonon scattering.

Accordingly, the density matrix is displayed in Fig. 43.7a–c for the same scattering situations, as in the I-V characteristics of Fig. 43.4. In Fig. 43.7a, the transport is fully ballistic in the active region, i.e., phonon scattering has been artificially switched off. In Fig. 43.7b, standard scattering rates were used as for the Wigner function plotted in Fig. 43.6. In Fig. 43.7c, phonon scattering rates have been artificially multiplied by five.

In Fig. 43.7a (ballistic case), a strong coherence is observed between electrons in the quantum well and in the emitter region. The amplitude of all off-diagonal elements is significant, even between collector and emitter regions, which is a clear indication of a fully coherent system. When considering standard scattering rates, the off-diagonal elements strongly reduce. When phonon scattering rates are artificially multiplied by five, the off-diagonal elements of the density matrix vanish, i.e., the coherence between electrons on the left and right side almost disappears. The tunneling process through the double barrier is thus no longer fully resonant. Electrons can be seen as entering and leaving the quasi-bound state via two distinct processes, with the possibility of energy exchange with the lattice through electron-phonon scattering. This illustrates the well-known coherent versus sequential tunneling regimes.

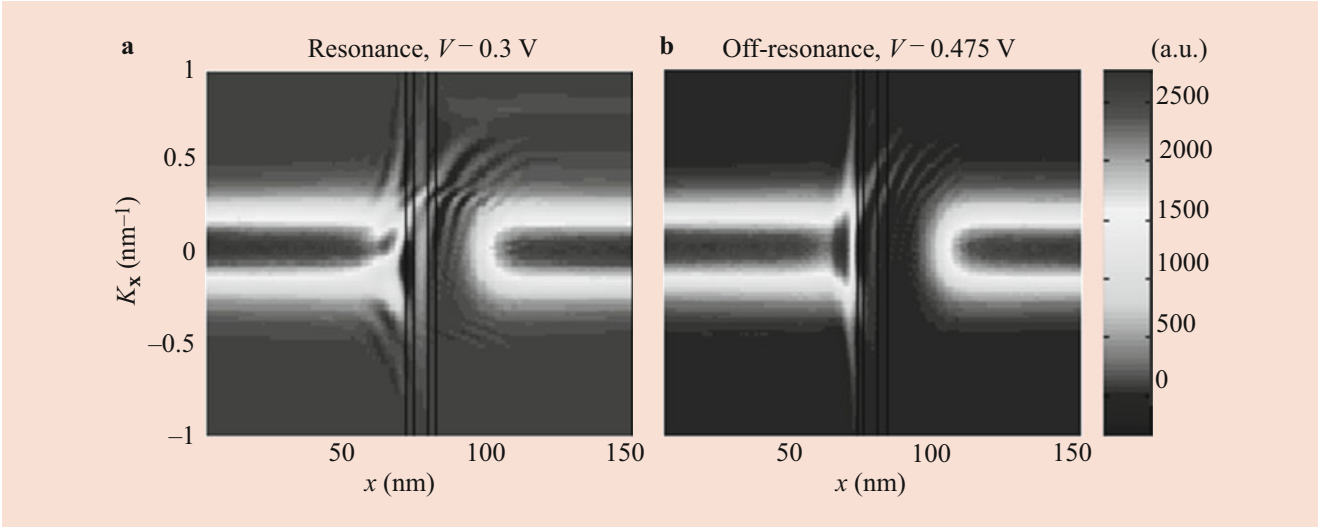

Fig. 43.6 Cartography in phase space of the Wigner function computed (**a**) for a resonant state ($V = 0.3$ V) and (**b**) a non-resonant state ($V = 0.475$ V). (After [43], with permission from Querlioz and Dollfus)

This transition between coherent and sequential tunneling regimes manifests itself in the current-voltage characteristics of the RTD plotted in Fig. 43.4 for the three scattering situations. Phonon scattering tends to suppress the resonant tunneling peak, while the valley current increases to such a point that the negative differential conductance effect almost disappears. The device tends to behave as two incoherent tunneling resistances connected in series for which a semi-classical-type description could be accurate enough.

More advanced considerations about the quantum to semi-classical transition may be found in [61].

43.4.8 The Signed Particle Method

In this section, we describe and discuss the signed particle Monte Carlo (MC) method which is based on the iterative Monte Carlo methods for the resolution of linear and non-linear systems of equations described in [36, 68] and which allows quantitative, time-dependent, multidimensional, single, and many-body simulations of quantum systems [16, 46, 47].

This method has shown to be a surprisingly powerful tool and has been applied to the simulation of quantum single-body problems in technologically relevant situations [69, 70] and even extended to time-dependent quantum many-body problems in the framework of density functional theory [71]. It has also been generalized to the ab initio simulations of strongly correlated many-body problems [72]. Finally, it has inspired a new formulation of quantum mechanics [73]. This is the first time that the Wigner formalism can be applied to such class of very computationally demanding problems and has the potential to profoundly impact the fields of electronics, physics, and chemistry.

The applications shown at the end of this chapter could not be fully understood without a comprehension of this section. Therefore, below, we start by going through the mathematical details of the theory. Furthermore, the interested reader can find an implementation of the Wigner MC method based on signed particles at [74]. The reader is advised to download the source code and study it for a faster, and more intuitive, comprehension of this approach.

Semi-Discrete Phase Space We have already seen that, in the Wigner formulation, any quantum system consisting of one particle, or body, is (completely) described by a quasi-distribution function defined over the phase-space $f_{\mathrm{W}}(\mathbf{x}; \mathbf{p}; t)$ which evolves in time according to Eq. (43.11). Therefore, our main goal consists in reconstructing this function for any given time of interest. To achieve this goal, the starting point is represented by the reformulation of the Wigner equation in a semi-discrete phase space with a continuous spatial variable $\mathbf{x}$ and a discretized momentum $\mathbf{p}$, with step $\Delta\mathbf{p} = \frac{\hbar\pi}{L_{\mathrm{C}}}$, where L_{C} is a free parameter, sometimes refered to as the coherence or cut-off length (a study on the dependence of the accuracy of a solution in function of L_{C} has been presented in [75]). In the semi-discrete momentum space, the Wigner equation now reads

$$\frac{\partial f_{\mathrm{W}}}{\partial t} + \frac{\hbar}{m}\frac{\mathbf{M}\Delta\mathbf{p}}{\hbar} \cdot \nabla_{\mathbf{x}} f_{\mathrm{W}} = \sum_{M'=-\infty}^{+\infty} V_{\mathrm{W}}(\mathbf{x}; \mathbf{M}'; t) f_{\mathrm{W}}(\mathbf{x}; \mathbf{M} - \mathbf{M}'; t), \qquad (43.36)$$

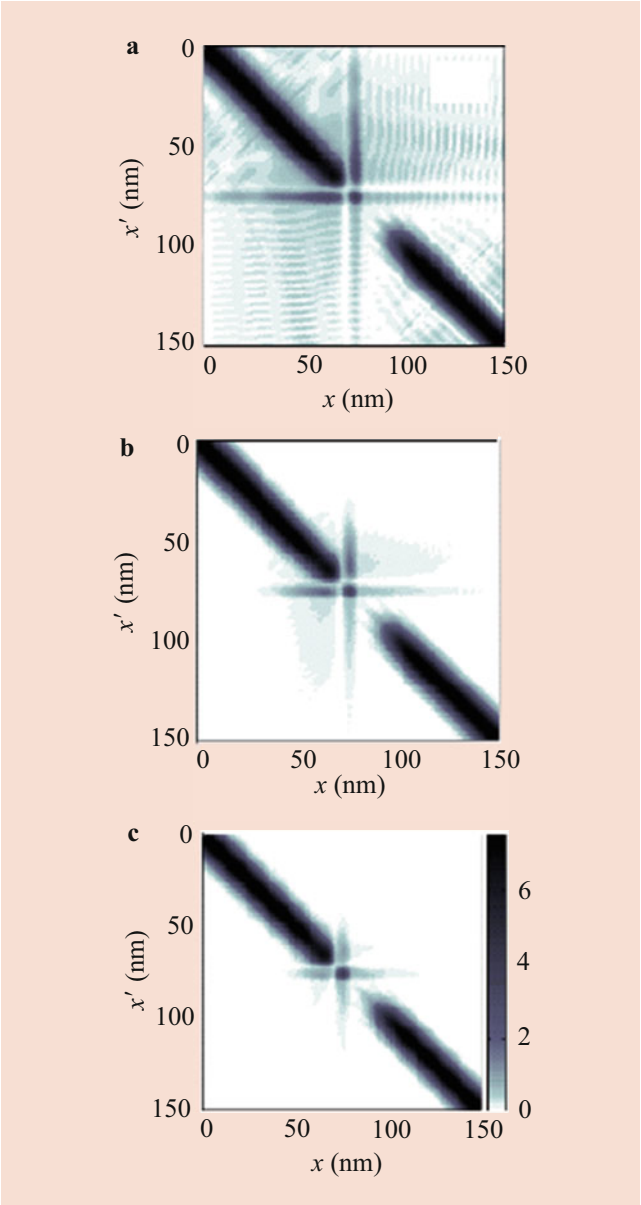

Fig. 43.7 Density matrix of a RTD operating at peak voltage for three cases: (**a**) no scattering, (**b**) standard phonon scattering rates, (**c**) standard rates multiplied by 5

where, for convenience, we use the notation $f_{\mathrm{W}}(\mathbf{x};\mathbf{M};t) = f_{\mathrm{W}}(\mathbf{x};\mathbf{M}\Delta\mathbf{p};t)$, with $\mathbf{M} = (M_1,\ldots,M_d)$ a set of integers with d elements, and $\mathbf{M}\Delta\mathbf{p} = (M_1\Delta p_1,\ldots,M_d\Delta p_d)$. Knowing the Wigner distribution function, it is possible to evaluate the expectation value $\langle A\rangle(t)$ of some generic physical quantity, described by a phase-space function, or $c-$number, $A = A(x;k)$ at a given time t. Therefore, the main computational problem becomes the calculation of the inner product (A, f_{W}) with the solution of (43.11). It can be shown that this task can be reformulated by exploiting the solution of the adjoint equation. In particular, we first obtain an integral form of (43.11) and then its corresponding adjoint equation.

Integral Formulation The semi-discrete Wigner equation (43.36) can be reformulated in an integral form. First, one defines a function γ as

$$\gamma(\mathbf{x}) = \sum_{\mathbf{M}=-\infty}^{\infty} V_{\mathrm{w}}^{+}(\mathbf{x};\mathbf{M}) = \sum_{\mathbf{M}=-\infty}^{\infty} V_{\mathrm{w}}^{-}(\mathbf{x};\mathbf{M}), \qquad (43.37)$$

where V_{w}^{+} is the positive part of V_{w}, i.e., it gives V_{W} if $V_{\mathrm{w}} > 0$ and 0 otherwise, and V_{w}^{-} is the negative part defined similarly (the equality was initially proven in [16] and afterwards in [46] and in [47]). In the stationary case, the Wigner potential is antisymmetric. It is clear that if $V_{\mathrm{w}}^{+}(x,-m) = 0$, then $V_{\mathrm{w}}^{-}(x,-m) \neq 0$ and, moreover, $V_{\mathrm{w}}^{-}(x,-m) = V_{\mathrm{w}}^{+}(x,m)$. Thus, the Eq. (43.22) can be rewritten by adding and substracting the term $\gamma(x(t'))$.

Let us, now, denote by Γ the following expression:

$$\Gamma(\mathbf{x}(t'),\mathbf{M},\mathbf{M}') = V_{\mathrm{w}}^{+}(\mathbf{x}(t');\mathbf{M}-\mathbf{M}') - V_{\mathrm{w}}^{+}(\mathbf{x}(t');\\ -(\mathbf{M}-\mathbf{M}')) + \gamma(\mathbf{x}(t'))\delta_{\mathbf{M},\mathbf{M}'}. \qquad (43.38)$$

For the sake of simplicity, we assume the evolution of an initial condition $f_i(x,m)$ starts at time 0. A common inclusion of both boundary and initial conditions, which formally resembles the free term of the Boltzmann integral equation, is performed, and by integration over the interval $(0,t)$, one recovers the following equation:

$$\begin{aligned} &f_{\mathrm{W}}(\mathbf{x};\mathbf{M};t) - \mathrm{e}^{-\int_0^t \gamma(\mathbf{x}(y))\mathrm{d}y} f_i(\mathbf{x}(0);\mathbf{M}) \\ &= \int_0^t \mathrm{d}t' \sum_{\mathbf{M}'=-\infty}^{\infty} f_{\mathrm{W}}(\mathbf{x}(t');\mathbf{M}';t')\Gamma(\mathbf{x}(t'),\mathbf{M},\mathbf{M}')\mathrm{e}^{-\int_{t'}^t \gamma(\mathbf{x}(y))\mathrm{d}y} \\ &= \int_0^{\infty} \mathrm{d}t' \sum_{\mathbf{M}'}^{\infty} \int \mathrm{d}x' f_{\mathrm{W}}(\mathbf{x}';\mathbf{M}';t')\Gamma(\mathbf{x}',\mathbf{M},\mathbf{M}') \\ &\quad \times \mathrm{e}^{-\int_{t'}^t \gamma(\mathbf{x}(y))\mathrm{d}y}\theta(t-t')\delta(\mathbf{x}'-\mathbf{x}(t'))\theta_{\mathrm{D}}(\mathbf{x}'), \end{aligned} \qquad (43.39)$$

where, to ensure the appearance of the variables $Q = (\mathbf{x},\mathbf{M},t)$ and $Q' = (\mathbf{x}',\mathbf{M}',t')$, the kernel has been augmented by the functions θ and δ which leave the value of the integral unchanged. In particular, the function θ_D keeps the integration within the simulation domain. In the same way, the expectation value of the physical quantity A at time τ is augmented and now reads

$$\langle A\rangle(\tau) = \int \mathrm{d}t \int \mathrm{d}\mathbf{x} \sum_{\mathbf{M}=-\infty}^{\infty} f_{\mathrm{W}}(\mathbf{x};\mathbf{M};t)A(\mathbf{x};\mathbf{M})\delta(t-\tau)$$
$$= \int \mathrm{d}Q f_{\mathrm{W}}(Q)A_{\tau}(Q), \tag{43.40}$$

(note the implicit definition of the symbol $A_{\tau}(Q)$).

Adjoint Equation The expectation value (43.40) can be rewritten by introducing the adjoint equation of (43.39) which has a solution g and a free term g_0 determined below:

$$f(Q) = \int \mathrm{d}Q' K(Q,Q')f(Q') + f_i(Q),$$
$$g(Q') = \int \mathrm{d}Q K(Q,Q')g(Q) + g_0(Q').$$

The first equation is multiplied by $g(Q)$ and integrated over Q, while the second equation is multiplied by $f(Q')$ and integrated over Q'. By subtracting the two equations, then one obtains

$$\int \mathrm{d}Q f_i(Q)g(Q) = \int \mathrm{d}Q' g_0(Q')f(Q')$$
$$\int \mathrm{d}Q' f_i(Q')g(Q') = \int \mathrm{d}Q g_0(Q)f(Q),$$

where the dummy variables have been exchanged for a more convenient comparison with (43.40). From this, one can show that

$$g_0(Q) = A_{\tau}(Q);$$
$$\langle A\rangle = \int_0^{\infty} \mathrm{d}t' \int \mathrm{d}\mathbf{x}' \sum_{\mathbf{M}'=-\infty}^{\infty} f_i(\mathbf{x}';\mathbf{M}')\mathrm{e}^{-\int_0^{t'}\gamma(\mathbf{X}'(y))\mathrm{d}y}$$
$$\times\, g(\mathbf{x}';\mathbf{M}';t'), \tag{43.41}$$

where $\mathbf{x}'(y)$ is the trajectory initialized by $(\mathbf{x}',\mathbf{M}',t')$, and $\mathbf{x}(0) = \mathbf{x}'$. Therefore, the adjoint equation (obtained by integration on the unprimed variables) reads

$$g(\mathbf{x}';\mathbf{M}';t')$$
$$= A_{\tau}(\mathbf{x}',\mathbf{M}',t') + \int_0^{\infty} \mathrm{d}t \sum_{\mathbf{M}=-\infty}^{\infty} \int \mathrm{d}\mathbf{x} g(\mathbf{x};\mathbf{M};t)\Gamma$$
$$\times\, (\mathbf{x}',\mathbf{M},\mathbf{M}')\mathrm{e}^{-\int_{t'}^{t}\gamma(\mathbf{x}(y))\mathrm{d}y}\theta(t-t')\delta(\mathbf{x}'-\mathbf{x}(t'))\theta_{\mathrm{D}}(\mathbf{x}'). \tag{43.42}$$

Now, we revert the parametrization of the fieldless trajectory and, therefore, $(\mathbf{x}(t') = \mathbf{x}'', \mathbf{M}, t')$ initialize the trajectory, and the variable $\mathbf{x} = \mathbf{x}(t)$ becomes the time-dependent variable. Consequently, the spatial coordinates for the function g become $\mathbf{x}'(t)$, and one has

$$g(\mathbf{x}';\mathbf{M}';t') = A_{\tau}(\mathbf{x}',\mathbf{M}',t')$$
$$+ \int_{t'}^{\infty} \mathrm{d}t \sum_{\mathbf{M}=-\infty}^{\infty} g(\mathbf{x}'(t);\mathbf{M};t)\Gamma(\mathbf{x}',\mathbf{M},\mathbf{M}')$$
$$\times\, \mathrm{e}^{-\int_{t'}^{t}\gamma(\mathbf{X}'(y))\mathrm{d}y}\theta_D(\mathbf{x}'). \tag{43.43}$$

In the same manner, one can reformulate Eq. (43.41) with the initialization changing from $(\mathbf{x}',\mathbf{M}',t')$ to $(\mathbf{x}_i = \mathbf{x}'(0),\mathbf{M}',0)$:

$$\mathbf{x}'(y) = \mathbf{x}_i(y) = \mathbf{x}_i + \frac{\mathbf{M}'\Delta\mathbf{p}}{m}y;\ \ \mathbf{x}' = \mathbf{x}'(t') = \mathbf{x}_i(t');$$
$$\mathrm{d}\mathbf{x}' = \mathrm{d}\mathbf{x}_i \tag{43.44}$$

$$\langle A\rangle = \int_0^{\infty} \mathrm{d}t' \int \mathrm{d}\mathbf{x}_i$$
$$\times \sum_{\mathbf{M}'=-\infty}^{\infty} f_i(\mathbf{x}_i;\mathbf{M}')\mathrm{e}^{-\int_0^{t'}\gamma(\mathbf{x}_i(y))\mathrm{d}y} g(\mathbf{x}_i(t');\mathbf{M}';t'). \tag{43.45}$$

Signed Particles in Practice Finally, by iterating consecutively (43.43) into (43.45), one can depict the numerical method based on signed particles. In fact, if one starts from the zero-th order term

$$< A >_0 (\tau) = \int_0^{\infty} \mathrm{d}t' \int \mathrm{d}\mathbf{x}_i$$
$$\sum_{\mathbf{M}'=-\infty}^{\infty} f_i(\mathbf{x}_i;\mathbf{M}')\mathrm{e}^{-\int_0^{t'}\gamma(\mathbf{x}_i(y))\mathrm{d}y} A(\mathbf{x}_i(t');\mathbf{M}')\delta(t'-\tau), \tag{43.46}$$

and applies the Monte Carlo theory for the computation of integrals, it is possible to interpret part of the integrand as the product of conditional probabilities. In practice, by assuming that f_i is normalized to unity, one generates a set of random points $(\mathbf{x}_i,\mathbf{M}')$ at time 0 which initialize the particle trajectories $\mathbf{x}_i(y)$. In this context, the above exponent provides the probability for a particle to remain over the trajectory given that the change of trajectory rate is expressed by the function γ. Thus, this probability filters out these particles, such that the randomly generated change of trajectory time is less than τ. If the particle stays in the trajectory until time τ, then it contributes to $< A >_0 (\tau)$ with a value equal to the rest of the integrand; in other words, $f_i(\mathbf{x}_i;\mathbf{M}')A(\mathbf{x}_i(\tau),\mathbf{M}')$. Otherwise, particles which have experienced a change of trajectory do not provide any kind of contribution. Therefore,

$< A >_0 (\tau)$ is estimated by averaging over the set of N initialized particles.

Similarly, the first-order term of the iteration term is obtained by replacing the term $g(\mathbf{x}_i(t'); \mathbf{M}'; t')$ in (43.45) by the kernel of (43.44) specifically rewritten; in other words, in (43.44), we substitute $\mathbf{x}'$ with $\mathbf{x}_1 = \mathbf{x}_i(t')$. In this case, the trajectory in the exponent is now initialized by the values $(\mathbf{x}_1, \mathbf{M}, t')$:

$$
\begin{aligned}
&< A >_1 (\tau) \\
&= \int_0^\infty \mathrm{d}t' \int \mathrm{d}\mathbf{x}_i \sum_{\mathbf{M}'=-\infty}^{\infty} f_i(\mathbf{x}_i; \mathbf{M}') \mathrm{e}^{-\int_0^{t'} \gamma(\mathbf{x}_i(y))\mathrm{d}y} \times \int_{t'}^\infty \mathrm{d}t \\
&\quad \times \sum_{\mathbf{M}=-\infty}^{\infty} g((\mathbf{x}_1(t); \mathbf{M}; t) \Gamma(\mathbf{x}_1, \mathbf{M}, \mathbf{M}') \mathrm{e}^{-\int_{t'}^{t} \gamma(\mathbf{x}_1(y))\mathrm{d}y} \theta_\mathrm{D}(\mathbf{x}_1).
\end{aligned}
$$

We then substitute the function $g(\mathbf{x}_1(t); \mathbf{M}; t)$ with the free term of (43.44) at point $A(\mathbf{x}_1(t), \mathbf{M}, t)\delta(t - \tau)$, and finally, we augment the equation by completing some of the probabilities enclosed in curly brackets. By partially reordering some of the terms, one obtains

$$
\begin{aligned}
&< A >_1 (\tau) = \int_0^\infty \mathrm{d}t' \int \mathrm{d}\mathbf{x}_i \\
&\times \sum_{\mathbf{M}'=-\infty}^{\infty} f_i(\mathbf{x}_i; \mathbf{M}') \left\{ \gamma(\mathbf{x}_i(t')) \mathrm{e}^{-\int_0^{t'} \gamma(\mathbf{x}_i(y))\mathrm{d}y} \right\} \theta_\mathrm{D}(\mathbf{x}_1) \int_{t'}^\infty \mathrm{d}t \\
&\times \sum_{\mathbf{M}=-\infty}^{\infty} \left\{ \frac{\Gamma(\mathbf{x}_1, \mathbf{M}, \mathbf{M}')}{\gamma(\mathbf{x}_i(t'))} \right\} \left\{ \mathrm{e}^{-\int_{t'}^{t} \gamma(\mathbf{x}_1(y))\mathrm{d}y} \right\} \\
&A(\mathbf{x}_1(t), \mathbf{M}, t)\delta(t - \tau).
\end{aligned}
$$

In a similar fashion, it is possible to give a purely Monte Carlo interpretation to this process: a particle is considered to be initialized at $(\mathbf{x}_i, \mathbf{M}', 0)$, which follows the trajectory until time t', i.e., the time when the particle changes its coordinates in the phase space. The time t' is then provided by the probability density in the first curly brackets since the enclosed term, if integrated over the time interval $(0, \infty)$, returns the unity. Moreover, the exponent can be interpreted as the probability of a particle staying in the same trajectory until time t', while $\gamma(\mathbf{x}_i(t'))\mathrm{d}t'$ can be interpreted as the probability to leave that trajectory during the interval $(t', t' + \mathrm{d}t')$. Its new phase-space coordinates now become $(\mathbf{x}_1 = \mathbf{x}_i(t'), \mathbf{M}')$ at t' and the evolution continues (as long as the particle remains in the simulation domain, otherwise its contribution is identically zero). The term in the next curly bracket becomes a source of change for the momentum, from $\mathbf{M}'$ to $\mathbf{M}$, at the spatial point $\mathbf{x}_1$ and at the time of scattering t'. Thus, at time t' the particle initializes the trajectory $(\mathbf{x}_1, \mathbf{M})$ and, with a probability provided by the exponent in the last curly brackets, remains on the same trajectory until time τ. In particular, t is set to τ by the δ function provided that $t' < \tau$; otherwise its contribution is zero. We note, however, that in this particular case the particle still has a contribution to the zero-th iteration term.

In other words, one can utilize the kernel of (43.44) to construct a transition probability for the numerical Monte Carlo trajectories which consist of pieces of fieldless Newton trajectories linked by a change of the momentum from $\mathbf{M}$ to $\mathbf{M}'$ according to Γ. These can be seen as particles being affected by events which change their phase-space coordinates, and the exponent in the formulas gives the probability that a particle remains on its trajectory with a changing rate equal to γ.

If a particle does not go under a trajectory changing event until time τ, then it contributes to $< A >_0 (\tau)$, and its contribution is equal to $f_i(\mathbf{x}_i; \mathbf{M}')g(\mathbf{x}_i(\tau); \mathbf{M}')$. If a particle goes under a trajectory event, then it contributes to a next term of the expansion. In fact, one could show that a particle contributes to one and only one term of this expansion, and the macroscopic value $< A > (t)$ is estimated by averaging over a set of N particles. Thus, we have seen that it is possible to depict a Monte Carlo algorithm for the ballistic, single-body, semi-discrete Wigner equation (43.36) where, after any free flight, an initial particle creates a pair of new particles with opposite signs and momentum offset (around the initial momentum), which are equal to $+\mathbf{L}$ and $-\mathbf{L}$, and where $\mathbf{L} = \mathbf{M} - \mathbf{M}'$. The initial particle and the two newly created ones represent three contributive terms of the series.

43.5 Monte Carlo Methods to Simulate the Many-Body Wigner Equation

The simulation of quantum many-body systems is an important problem which touches many practical aspects of our everyday life such as the design of chemical reactions, new materials, and electronics. It also represents, unfortunately, a complex task which requires immense computational resources. Therefore, it is not surprising to see that the first attempt to simplify the quantum many-body problem appeared very early, precisely in 1926, as a method to find the electronic structure in terms of a one-electron ground-state density $\rho(\mathbf{x})$ [76, 77].

In this section, we focus on two possible generalizations of the Wigner MC methods based on signed particles discussed previously, i.e., (1) the generalization to the density functional theory and (2) the generalization of the method for first-principle simulations of quantum systems.

43.5.1 The Density Functional Theory

This first approach to the quantum many-body problem, today known as the Thomas-Fermi theory, unfortunately introduces too many oversimplifications to be of any realistic use but represents an important result anyway since it has provided the foundations for the development of very advanced methods such as the density functional theory (DFT). Later on, Slater was the first one to introduce the combination of the ideas of Thomas and Fermi with Hartree's orbital method [78, 79], introducing the new (revolutionary) concept of a local exchange potential. Afterwards, the Hohenberg-Kohn theorem proved that, at least in principle, an exact method using the one-electron ground-state density $\rho(\mathbf{x})$ [80] could be developed and the Kohn-Sham system was introduced right after for the case of homogeneous electron gases [81]. The time-dependent counterpart of the Hohenberg-Kohn theorem appeared much later, in 1984, when Runge and Gross presented their theorem [82] (the reader should note, though, that this theorem only guarantees the validity of the time-dependent Kohn-Sham system for the calculations of the ground-state, nothing is proved for the excited states [83]). Nowadays, the DFT method is the most popular tool in quantum chemistry [84] and is being utilized by a growing number of different communities such as, for instance, the field of nanoelectronics. Therefore, in this section, we focus on the first extension to the many-body problem based on the signed particle Wigner MC method. This section is based on the work described in [71].

The DFT approach relies on the fact that computing the wave-function of a single-electron Schrödinger equation is relatively simple (at least numerically). In practice, the many-body problem is reduced to a system of coupled single-electron equations, known as the Kohn-Sham system, and effects such as electron-electron interaction are described in terms of the so-called density functional. This is the essence of both time-independent and time-dependent approaches in DFT [81, 82]. Although the exact mathematical expression for the density functional is usually unknown for systems of practical interest, this simplification allows the simulation of many-body problems in acceptable computational times. In spite of these limitations, practitioners can now choose among a huge number of functionals which work at least at a qualitative level; see, for example [81, 85, 86].

In standard quantum mechanics, the time-dependent dynamics of a many-body system is described by the many-body Schrödinger equation which reads

$$i\hbar\frac{\partial}{\partial t}\Psi = \hat{H}\Psi. \tag{43.47}$$

The unknown is represented by the wave-function $\Psi = \Psi(\mathbf{x}_1, \ldots, \mathbf{x}_n)$, which is a complex valued function, and the Hamiltonian $\hat{H}$ accounts for the various forces involved in the problem (e.g., see formula (43.19)). Resolving equation (43.47) is a formidable, see daunting, mathematical problem even when it is approached by numerical techniques. A great help in this context comes from the time-dependent Kohn-Sham system which reduces the difficulties involved in (43.47) by orders of magnitude and, therefore, allows practical (although qualitative) simulations of many-body systems. As a matter of fact, this problem becomes a much simpler set of n single-body Schrödinger equations coupled to each other by means of an effective density functional $v_{\text{eff}} = v_{\text{eff}}(\mathbf{x})$ [84]. The reader should note, again, that there is no unique way to express the density functional (e.g., [81, 85, 86]).

Finally, the time-dependent Kohn-Sham system reads ($i = 1 \ldots n$)

$$i\hbar\frac{\partial \Phi_i}{\partial t}(\mathbf{x}, t) = \left(-\frac{\hbar^2\nabla^2}{2m_i} + U_{\text{eff}}(\mathbf{x})\right)\Phi_i(\mathbf{x}, t) \tag{43.48}$$

which can be utilized to compute the one-electron density:

$$\rho(\mathbf{x}) = \sum_i |\Phi_i(\mathbf{x})|^2, \tag{43.49}$$

where the sum is performed over the states below the Fermi energy.

43.5.2 The *Wigner* Density Functional Theory

It is relatively easy to see that if one applies the Wigner-Weyl transform (43.27) to every equation of the system (43.48), one readily obtains a new time-dependent Kohn-Sham system which is now defined in terms of n single-body Wigner equations. Such a system reads

$$\frac{\partial f_w^i}{\partial t} + \frac{\mathbf{p}}{m_i}\cdot\nabla_{\mathbf{x}} f_w^i = Q\left[f_w^i\right], \tag{43.50}$$

where the Wigner kernel is a functional of the effective potential, i.e.,

$$V_{\text{w}}(\mathbf{x}, \mathbf{p}, t) = \frac{i}{(2\pi)^d\hbar^{d+1}}\int \mathrm{d}\mathbf{x}' \mathrm{e}^{-i\frac{\mathbf{p}\mathbf{x}'}{\hbar}} \times \left(U_{\text{eff}}\left(\mathbf{x} + \frac{\mathbf{x}'}{2}, t\right) - U_{\text{eff}}\left(\mathbf{x} - \frac{\mathbf{x}'}{2}, t\right)\right). \tag{43.51}$$

Thus, in this new context, the quantum many-body problem consists in solving the set of coupled equations (43.50). Obviously, this system is affected by the very same problems of standard DFT, e.g., the choice of the exchange-correlation potential is not unique, there is no guarantee that the excited states are correct, etc., and, if applied to a computational

quantum problem, it will provide the same answers provided by the standard DFT. Nevertheless, two important advantages appear in this new model. First, the Wigner formalism is based on the concept of a quasi-distribution function and, as such, offers a much more intuitive representation of the simulated system. Second, the Wigner MC method, based on signed particles, is known to be embarrassingly parallelizable [36, 68].

43.5.3 The Wigner Monte Carlo Method for Many-Body Systems

Traditionally, ab initio simulations, based on first principles of quantum mechanics, are known to be incredibly difficult to perform as they require an immense amount of computational power.

Although they are complex, it is important to find ways to simulate such systems, since they allow the simulation of so-called *strongly correlated* systems, which are relevant in both applied physics and chemistry. In this section, we briefly describe the first-principle many-body Wigner MC method based on signed particles which was suggested in [72]. Many details are skipped since it would be out of the scope of this chapter, and the interested reader is kindly invited to read [72] and [25] for more information.

First of all, as done previously for the single-body Wigner equation, the many-body Wigner equation needs to be rewritten in a semi-discrete phase space where the spatial coordinates $\mathbf{x}$ keep on being continuous while the space of momenta is discretized. In such context, the momentum $\mathbf{p}$ is expressed as multiples of the quantity $\Delta\mathbf{p} = \frac{\hbar\pi}{L_C}$, where L_C is the usual cut-off or coherence parameter encountered previously. It is possible to show that the semi-discrete many-body Wigner equation reads

$$\frac{\partial f_W}{\partial t}(\mathbf{x};\mathbf{M};t) + \sum_{k=1}^{n} \frac{\mathbf{M}_k \Delta\mathbf{p}}{m_k} \cdot \nabla_{\mathbf{x}_k} f_W = \sum_{\mathbf{M}=-\infty}^{+\infty} f_W(\mathbf{x};\mathbf{M};t) V_W(\mathbf{x};\mathbf{M};t), \tag{43.52}$$

with $\mathbf{M} = (\mathbf{M}_1, \mathbf{M}_2, \ldots, \mathbf{M}_n)$, $\sum_{\mathbf{M}=-\infty}^{+\infty} = \sum_{\mathbf{M}_1=-\infty}^{+\infty} \sum_{\mathbf{M}_2=-\infty}^{+\infty} \cdots \sum_{\mathbf{M}_n=-\infty}^{+\infty}$, and

$$V_W(\mathbf{x};\mathbf{M};t) = \frac{i}{\pi^{dn}\hbar^{dn+1}} \int \mathrm{d}\mathbf{x}' \mathrm{e}^{-\left(\frac{2i}{\hbar}\right)\sum_{k=1}^{n} \mathbf{x}'_k \cdot \mathbf{M}_k \Delta\mathbf{p}} \times \left[V\left(\mathbf{x} + \frac{\mathbf{x}'}{2}; t\right) - V\left(\mathbf{x} + \frac{\mathbf{x}'}{2}; t\right) \right].$$

Note that, now, the momentum of the i-th particle is represented by a set of d integers $\mathbf{M}_i = (M_1^i, \ldots, M_d^i)$ and $\mathbf{M}_i \Delta\mathbf{p} = (M_1^i \Delta p_1, \ldots, M_d^i \Delta p_d)$ where $\Delta\mathbf{p} = (\Delta p_1, \ldots, \Delta p_d)$.

At this point, it is possible to rewrite Eq. (43.52) in an integral form by defining the (many-body) function γ which now reads:

$$\gamma(\mathbf{x}) = \sum_{\mathbf{M}=-\infty}^{\infty} V_W^+(\mathbf{x};\mathbf{M}), \tag{43.53}$$

where V_W^+ has the usual meaning generalized in the many-body context. Then, the Eq. (43.52) can be rewritten by adding and substracting the term $\gamma(\mathbf{x})$. Similarly, the function Γ can be generalized to this new context and now reads

$$\Gamma(\mathbf{x};\mathbf{M};\mathbf{M}') = V_W^+(\mathbf{x};\mathbf{M}-\mathbf{M}') - V_W^+(\mathbf{x};-(\mathbf{M}-\mathbf{M}')) + \gamma(\mathbf{x})\delta_{\mathbf{M},\mathbf{M}'}. \tag{43.54}$$

If one follows the same strategy employed for the single-body Wigner equation, it is possible to rewrite the semi-discrete many-body Wigner equation in the form of a Fredholm integral equation of second kind:

$$f_W(\mathbf{x};\mathbf{M};t) - \mathrm{e}^{-\int_0^t \gamma(\mathbf{x}(y))\mathrm{d}y} f_i(\mathbf{x}(0);\mathbf{M}) = \int_0^\infty \mathrm{d}t' \sum_{\mathbf{M}'=-\infty}^{+\infty} \int \mathrm{d}\mathbf{x}' f_W(\mathbf{x}';\mathbf{M}';t')\Gamma(\mathbf{x}';\mathbf{M};\mathbf{M}') \times \mathrm{e}^{-\int_{t'}^t \gamma(\mathbf{x}(y))\mathrm{d}y} \theta(t-t')\delta(\mathbf{x}'-\mathbf{x}(t'))\theta_D(\mathbf{x}'). \tag{43.55}$$

43.5.4 Signed Particle Method

At this point, it is easy to see that the equations so far recovered are in the same shape as the ones obtained for the single-particle Wigner MC method. This suggests that we can simply follow the same procedure and express the expectation value of a variable as a Liouville von Neumann series. This eventually allows to depict a signed particle MC method for the many-body Wigner equation.

In the very same way as for the single-body problem, it is possible to show that the expansion of $\langle A \rangle$ branches and the total value is given by the sum of all branches. We can, thus, equivalently talk in terms of three appearing particles even for the many-body Wigner Monte Carlo method. The reader should note, though, that in this new context, by *particle* one now means a mathematical point defined in a *nd*-dimensional phase space, i.e.,

$$\frac{\Gamma(\mathbf{x};\mathbf{M};\mathbf{M}')}{\gamma(\mathbf{x})} = \left\{ \frac{V_W^+(\mathbf{x},\mathbf{M}-\mathbf{M}')}{\gamma(\mathbf{x})} \right\} - \left\{ \frac{V_W^-(\mathbf{x},\mathbf{M}-\mathbf{M}')}{\gamma(\mathbf{x})} \right\} + \left\{ \delta_{\mathbf{M},\mathbf{M}'} \right\}. \tag{43.56}$$

It is, therefore, possible to depict a Monte Carlo method which is based, again, on signed particles but, this time,

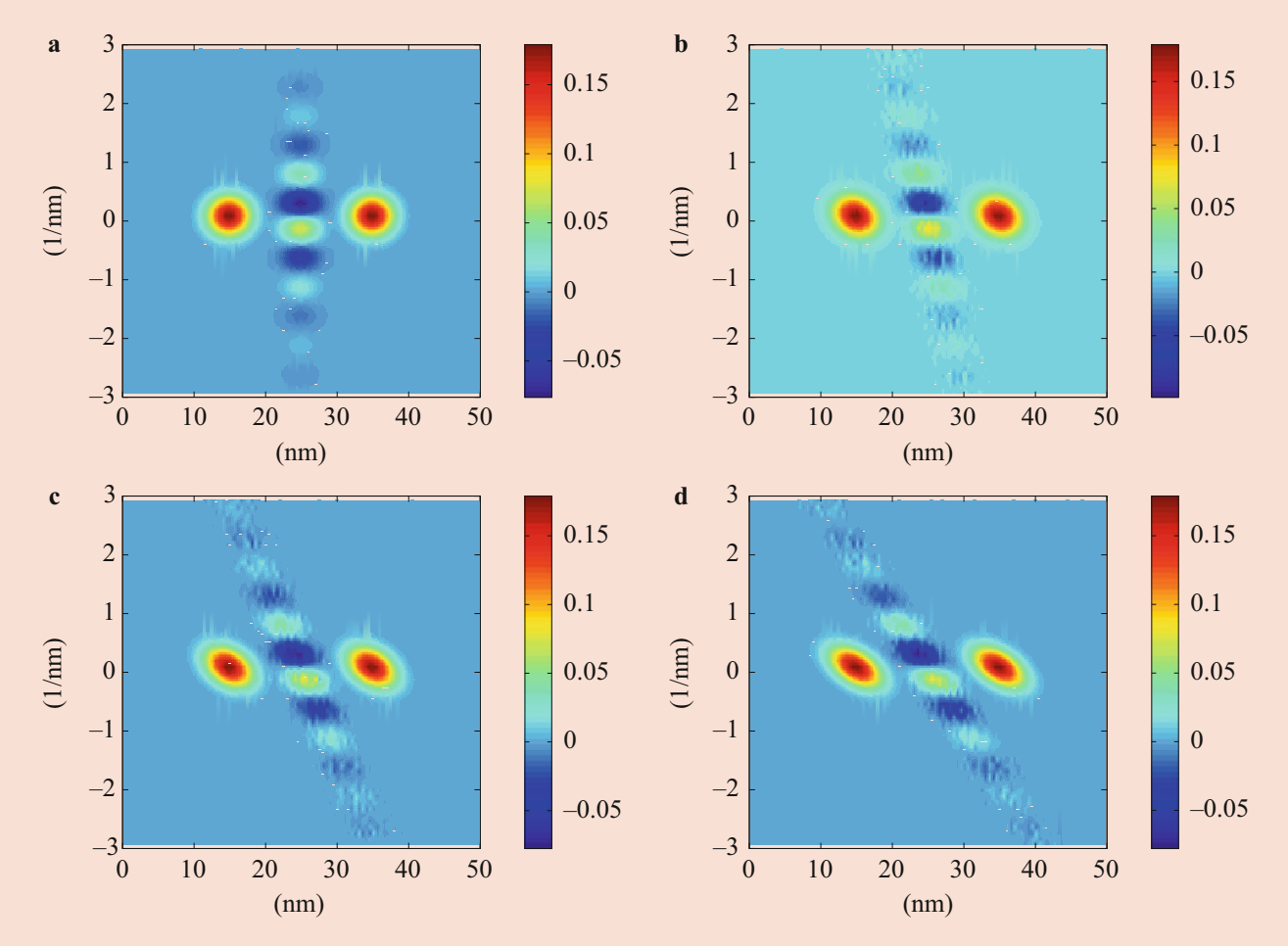

Fig. 43.8 Evolution of an entangled two-body system. The quasi-distribution function in the reduced phase space are shown at times 0 fs, 1 fs, 2 fs and 3 fs respectively (**a** to **c**, **a** to **b**). As expected, the entanglement oscillations rotates during the simulation

within the many-body context. According to the last term above, as for the one-body case, an initial parent particle generates a couple of new signed particles with the first two probabilities, i.e., the first many-body momentum state is generated $\mathbf{M} - \mathbf{M}' = \mathbf{L}$ with probability

$$\frac{V_{\mathrm{W}}^{+}(\mathbf{x}, \mathbf{L})}{\gamma(\mathbf{x})},$$

and with the same probability, another value is generated, say $\mathbf{L}'$, for the second state $\mathbf{M}' - \mathbf{M} = \mathbf{L}'$. In other words, the term $\Gamma(\mathbf{x}; \mathbf{M}; \mathbf{M}')$ allows to depict a Monte Carlo algorithm for the integration of the many-body semi-discrete Wigner equation (43.52). After any free flight, the initial particle creates two new particles with opposite signs and momentum offset, around the initial momentum, equal to $+\mathbf{L}$ and $-\mathbf{L}$ with $\mathbf{L} = \mathbf{M} - \mathbf{M}'$. The initial particle and the created couple represent three contributive terms to the many-body Liouville-Neumann series. Therefore, the solution of the many-body problem is constructed by an ensemble of fieldless Newtonian particles which are *independent* from each other. As an example, Fig. 43.8 shows the evolution of a two-body system consisting of two wave packets being entangled (represented by the oscillations between the two packets).

43.6 Neural Networks to Compute the Kernel

The computation of the (highly dimensional) Wigner kernel (43.12) can represent a serious bottleneck for the simulation of quantum systems, especially in the presence of time-dependent potentials which, in practice, amounts to the computation of such function at every time step. In this situation, its numerical computation becomes not only time consuming but also memory demanding. Mainly, two approaches are utilized in this case: a deterministic one, e.g., based on the finite element method, and a stochastic one, e.g., the sampling Monte Carlo method.

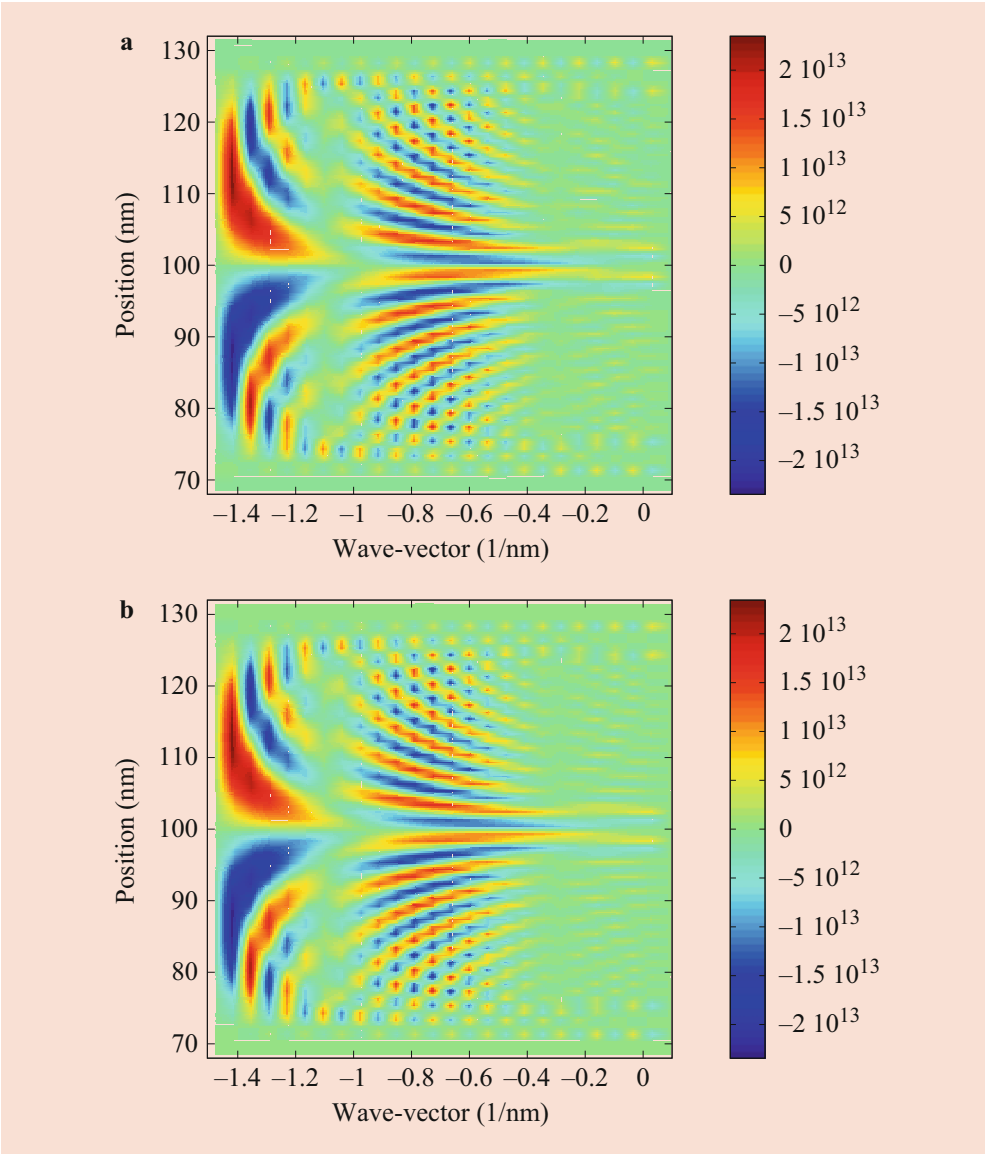

Fig. 43.9 Quantum one-body problem in the presence of a double barrier: (**a**) Wigner kernel computed by a finite difference method, (**b**) Wigner kernel computed by a trained neural network. A very good agreement is clearly achieved

Finite Difference Approaches Any finite difference integration, or quadrature, method is based on the evaluation of the integrand over a series of points defined within the integration interval which are, usually, equidistant (in other words, a discretized space). A well-known example is represented by the trapezoidal rule, which can be considered the archetypal of the numerical integration methods, and the Simpson rule [87]. Other methods exist, based on different weighted summations of the integrand evaluated over the cells of the discretized space. It is well known that the accuracy of these methods quickly degrades with the increase of the dimensionality of the integrand. Therefore, in this context, the only way to keep the accuracy is by increasing the number of evaluations of the integrand function [87]. Eventually, this amounts to a consistent number of evaluations which greatly slow down the computation of the integral along with an increase of the amount of memory involved in the process. One way to escape the increase of sampling points, while still being accurate, is by recurring to the use of Monte Carlo techniques.

Monte Carlo Approaches The main idea behind any Monte Carlo quadrature technique is simple and consists in supposing that the integrand $f(x)$ can be written as the product of two functions, say $f(x) = h(x)p(x)$, where $p = p(x)$ is a given function with certain convenient properties. It can be

mathematically proved that the computational complexity of such methods is linear [32]. The main drawbacks of such approach consists in the fact that the accuracy depends on what one knows about the integrand function $f = f(x)$. In fact, the integral can be evaluated only when a certain amount of information is available. Moreover, if the function $f(x)$ is rapidly oscillating, then the convergence usually tends to become very slow [87] and the amount of memory needed to perform such computation can increase very rapidly with the dimensionality of the problem at hand, which can represent a serious drawback in the case of the simulation of many-body quantum problems.

A Neural Network Approach In the last few years, artificial neural networks have been applied to broader sets of applications with immense success. For instance, they have been utilized, with impressive results, to the recognition of individual objects in photographs, to the problem of speech recognition, etc. In particular, they have shown to excel in tasks where information is complex and voluminous [88]. Inspired by these recent achievements, it seems more than reasonable to investigate whether they could provide advantages over the standard methods described above. It turns out that the answer is positive. As a matter of fact, artificial neural networks have been developed which are capable of accurately computing the Wigner kernel, when provided with a potential defined over the configuration space, with insignificant memory resources and at faster computational times [89].

In this particular and rather novel context, the main effort consists in the optimization of two antagonist objectives, i.e., the computational accuracy and speed. This can be achieved by selecting the appropriate network architecture. In [89], the search space of architectures has been restricted to feedforward neural networks, mainly motivated by their simplicity while still being able to capture global interactions between the inputs. Although one might end up with a relevant number of parameters, a speedup about 18 times faster has been achieved (compared to the simplest finite difference quadrature methods). Moreover, this approach easily allows efficient parallelization schemes on graphical processing units (GPUs), without any effort, with the use of modern deep learning libraries. In fact, within this approach, most of the computations consist of matrix multiplications. As an example, Fig. 43.9 shows the Wigner kernel corresponding to a double barrier potential computed by a finite difference method (left) and by a trained neural network (right). No difference is visible to the naked eye.

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The Nonequilibrium Green Function (NEGF) Method

44

Kerem Y. Camsari, Shuvro Chowdhury, and Supriyo Datta

Contents

44.1 Introduction 1584
44.1.1 Decoupling NEGF from MBPT 1585
44.1.2 Outline 1586

44.2 NEGF Equations 1586

44.3 NEGF Equations from One-Electron Schrödinger Equation 1586
44.3.1 NEGF Eqs. (44.1) and (44.2) 1587
44.3.2 NEGF Eq. (44.3) 1587

44.4 A Simple Example 1588
44.4.1 Hamiltonian **H** 1588
44.4.2 Self-Energy Due to Contacts 1588
44.4.3 Inscattering from Contacts 1589
44.4.4 Current 1589
44.4.5 Dephasing Interactions 1590
44.4.6 Diffusive Spin Transport Using NEGF 1591
44.4.7 Application to Superconducting Devices 1592

44.5 Frequently Asked Questions 1593
44.5.1 Shouldn't We Also Consider the Poisson Equation for Modeling Real Devices? 1593
44.5.2 Can You Arbitrarily Designate the Ends as Contacts? 1593
44.5.3 Does NEGF Give the Correct Coherent and Semiclassical Limits? 1594
44.5.4 How Is This Related to the Kubo Formalism? 1594
44.5.5 Isn't the Flow of Electricity Essentially a Many-Body Process? 1594
44.5.6 How Can We Teach NEGF Without Advanced Quantum Statistical Mechanics? 1595
44.5.7 But Is This the Real NEGF? 1595
44.5.8 Contacting Schrödinger 1595

References 1597

Abstract

The nonequilibrium Green function (NEGF) method was established in the 1960s through the classic work of Schwinger, Kadanoff, Baym, Keldysh, and others using many-body perturbation theory (MBPT) and the diagrammatic theory for nonequilibrium processes. Much of the literature is based on the original MBPT-based approach, and this makes it inaccessible to those unfamiliar with advanced quantum statistical mechanics. We obtain the NEGF equations directly from a one-electron Schrödinger equation using relatively elementary arguments. These equations have been used to discuss many problems of great interest such as quantized conductance, (integer) quantum Hall effect, Anderson localization, resonant tunneling, and spin transport without a systematic treatment of many-body effects. But it goes beyond purely coherent transport allowing us to include phase-breaking interactions (both momentum-relaxing and momentum-conserving as well as spin-conserving and spin-relaxing) within a self-consistent Born approximation. We believe that the scope and utility of the NEGF equations transcend the MBPT-based approach originally used to derive it. NEGF teaches us how to combine quantum dynamics with "contacts" much as Boltzmann taught us how to combine classical dynamics with "contacts," using the word "contacts" in a broad figurative sense to denote all kinds of entropy-driven processes. We believe that this approach to "contact-ing" the Schrödinger equation should be of broad interest to anyone working on device physics or nonequilibrium statistical mechanics in general.

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Keywords

NEGF · Contact · Rashba effect · Many-body perturbation · Hamiltonian matrix · Self-energy function · Occupation factor · Dephasing · Phase relaxation and momentum relaxation

44.1 Introduction

The nonequilibrium Green function (NEGF) method was pioneered in the 1960s by the classic work of Martin, Schwinger [1], Kadanoff, Baym [2], Keldysh [3], and others, which have been discussed in many review articles such as Danielewicz [4] and Mahan [5]. After the advent of mesoscopic physics in the 1980s, this method was combined with the Landauer approach (see [6–8]), and this "NEGF-Landauer method" has been widely used in the field of nanoelectronics for device modeling and technology development (see [9–23] as a small subset of a vast literature). The chapter by Klimeck and Boykin in this volume provides an introduction to state-of-the-art quantum transport simulation tools based on this method. The present chapter is intended to serve a complementary purpose, namely, to introduce the conceptual underpinnings of NEGF and to answer some frequently asked questions regarding them.

The iconic device in modern electronics is the field effect transistor (FET), billions of which are a part of every smartphone. An oversimplified sketch of an FET is shown in Fig. 44.1 consisting of an active region marked the *channel* sandwiched between two highly conductive regions labeled the *source* and the *drain*. An FET also has a third terminal (not shown) which can be used to control the resistance $R = V/I$ of the channel, but we will not get into such "details." We will focus just on the problem of calculating the steady-state charge current I for a given voltage V taking *quantum* effects into account.

Quantum mechanical descriptions usually start from a Hamiltonian matrix $\mathbf{H}$ whose eigenvalues give us the allowed energy levels. However, if we treat the structure like a closed system described just by an $\mathbf{H}$, an applied voltage will cause opposite charges to pile up in the source and drain, and we will have a capacitor and not a resistor. What makes it a resistor is the external battery that continually takes electrons out of the drain and inserts electrons back into the source to maintain an electrochemical potential difference: $\mu_1 - \mu_2 = qV$.

One way to describe such an open system is to describe the two contacts denoted 1 and 2 through self-energy functions $\mathbf{\Sigma}_{1,2}$, $\mathbf{\Sigma}^{\text{in}}_{1,2}$. The first of these $\mathbf{\Sigma}_{1,2}$ has a Hermitian part that modifies the Hamiltonian and an anti-Hermitian part that represents the rate at which electrons escape from the channel. The second of these $\mathbf{\Sigma}^{\text{in}}_{1,2}$ represents the inflow of the electrons into the channel from the contacts. In addition to these physical contacts, there are abstract "contacts" representing the interactions of the electrons with the lattice and with other electrons as they traverse the channel, and these are described the self-energy functions $\mathbf{\Sigma}_0$, $\mathbf{\Sigma}^{\text{in}}_0$. To apply the NEGF method to a given problem, there are two steps:

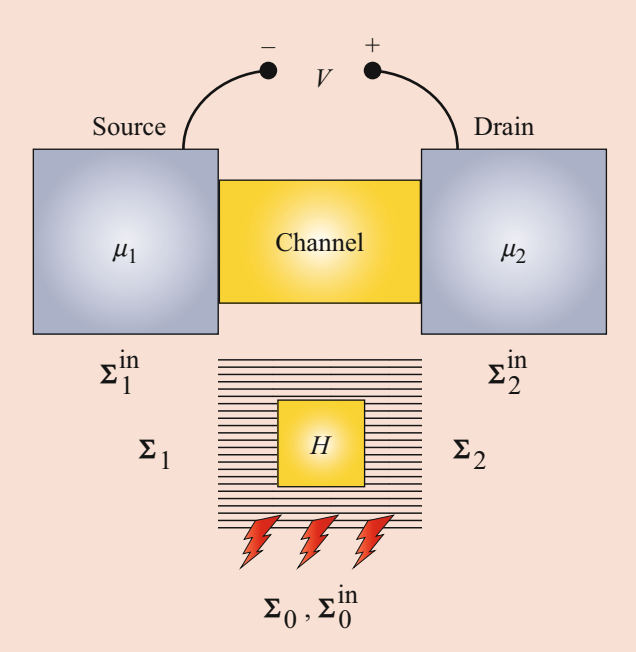

Fig. 44.1 A resistor: Physical structure comprising a channel with two contacts, labeled source and drain. In the nonequilibrium Green function (NEGF) method, the channel is described by a Hamiltonian $\mathbf{H}$, while its connection to the "contacts" is described by the self-energy functions $\mathbf{\Sigma}$, $\mathbf{\Sigma}^{\text{in}}$: subscripts 1 and 2 denote the physical contacts labeled source and drain, while the subscript 0 represents abstract contacts like the phonon bath

1. Identify the appropriate Hamiltonian $\mathbf{H}$ and self-energy functions $\mathbf{\Sigma}_m$, $\mathbf{\Sigma}^{\text{in}}_m$
2. Use these in the NEGF Eqs. (44.1–44.3) summarized in Sect. 44.2 to calculate quantities of interest like current, electron density, or density of states.

The NEGF method is commonly viewed as an esoteric tool accessible only to a small group of specialists. To quote from two popular books [24, 25]:

> …In this respect, the most difficult topic is probably the non-equilibrium Green's function formalism of Chapter 4 …

> …Because of my aim of avoiding too heavy formalism I have chosen not to describe non-equilibrium Green's function approaches to transport phenomena. Courses detailing these approaches usually spend half the time on the formalism, finding the poles of the various Green's functions, and figuring out analytic continuations and so on …

Both books are pedagogically outstanding, and we cite them only to stress that NEGF is considered difficult even by the foremost practitioners in the field. And the reason is that the traditional discussion of NEGF is based on many-body perturbation theory (MBPT) which takes many semesters of advanced quantum mechanics to master.

However, as we have often noted [26], the only aspect of NEGF that really requires MBPT is in writing down the self-energy functions $\mathbf{\Sigma}_0$, $\mathbf{\Sigma}_0^{\text{in}}$ describing interactions within the channel. Everything else can be accomplished without the use of MBPT, including deriving the NEGF Eqs. (44.1–44.3) and writing down the noninteracting channel Hamiltonian $\mathbf{H}$ along with the self-energy functions for the physical contacts $\mathbf{\Sigma}_{1,2}$ and $\mathbf{\Sigma}_{1,2}^{\text{in}}$. This is the approach one of us has used in all his books starting from Chapter 8 of [27] and later in [28] and Part B of [29]. The recent book by Ghosh [30] is unique in describing both our approach and the MBPT-based one along with special non-perturbative approaches.

44.1.1 Decoupling NEGF from MBPT

Why is the standard treatment so heavily dependent on MBPT? We believe the reason is historical. Until 1990 it was common to regard the physical contacts as an unimportant detail and view the channel interactions as the essential physics. And so the original papers in the field dating back to the 1960s described the resistance in terms of $\mathbf{\Sigma}_0$, $\mathbf{\Sigma}_0^{\text{in}}$ and never even considered the $\mathbf{\Sigma}_{1,2}$, $\mathbf{\Sigma}_{1,2}^{\text{in}}$ describing the physical contacts.

What changed around 1990 was the widespread experimental measurement of the resistance of *ballistic conductors* where electrons zip through the channel like bullets with little or no interactions making $\mathbf{\Sigma}_0$ and $\mathbf{\Sigma}_0^{\text{in}}$ negligible. Do such conductors have a resistance? The experimental answer was a resounding *yes* (For example, [31] is one of the first experiments that established the fundamental limits of conductance in such ballistic conductors. Later, scientists have even measured the resistance of a single molecule [32]!). A current I flowing through a nonzero resistance R must generate a heat I^2R. Heat is generated when energetic electrons give up some of their energy to the lattice making the atoms jiggle, which manifests itself as an increase in temperature.

But if there are no interactions in the channel, then how can heat be generated? The answer is that the heat is generated within the contacts (Fig. 44.2a) which is not surprising since a bullet heats up the material it hits and not the medium it flies through. A corollary of this observation is that although any resistance R is accompanied by the generation of I^2R heat, the heating need not occur exactly where the resistance is caused.

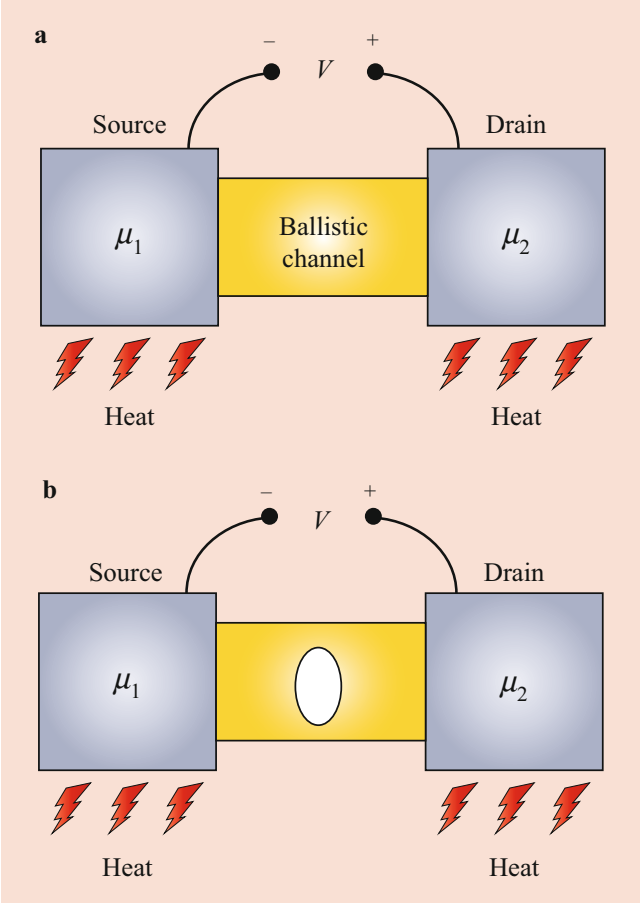

Fig. 44.2 (**a**) In a ballistic conductor, the resistance arises from the channel-contact interfaces, but the heating occurs deeper in the contacts. (**b**) A ballistic conductor with a hole further accentuates the spatial separation between the microscopic cause of resistance and the resulting generation of heat

For example, in the ballistic conductor, the resistance is caused by the channel-contact interfaces, while the heating could occur away from the interface. This separation of the resistance R and its heat I^2R is even more stark if we consider a ballistic conductor with a hole in the middle (Fig. 44.2b). We would expect the hole to cause a large increase in resistance by obstructing the flow of electrons. But it does not have the *internal degrees of freedom* needed to get heated which must still occur far away somewhere in the contacts (An experimental observation that supports this viewpoint is current transport through carbon nanotubes. Despite being extremely small in diameter and volume, carbon nanotubes can carry enormous amounts of current, and if there were any significant energy dissipation within the channel, they could not get rid of such excessive heat and would burn up.).

However, pre-1990, it was not common to talk of resistance in a model without explicitly including interactions and dissipation in the channel (Though device engineers had started to recognize that momentum and energy relaxation

lengths could be very different in late 1980s. See, for example, [33].). Indeed much of the work on quantum transport was based on the Kubo formula which equates resistance to dissipation and then relates it to noise through the fluctuation-dissipation theorem. This is a powerful approach to linear response problems, but it tends to create the impression that the origin of resistance is energy relaxation rather than momentum relaxation. But it now seems clear that resistance is caused by momentum exchange, and the resulting energy exchange need not occur at the same location. It is possible to create a zero-order model for resistance without including any $\mathbf{\Sigma}_0$ or $\mathbf{\Sigma}_0^{\text{in}}$, and this approach at least has enormous pedagogical value.

The NEGF Eqs. (44.1–44.3) obtained in the next section from elementary quantum mechanics are the *same* as those obtained in the classic paper by Keldysh using MBPT [3]. The difference is that we obtain them considering only the physical contacts described by $\mathbf{\Sigma}_{1,2}$ and $\mathbf{\Sigma}_{1,2}^{\text{in}}$, while the classic treatment considers only the many-body interactions described by $\mathbf{\Sigma}_0$ and $\mathbf{\Sigma}_0^{\text{in}}$. Our approach makes it accessible to a much wider audience, and for over a decade, we have been teaching the NEGF equations to advanced undergraduate and beginning graduate students, both on campus and online.

We believe the utility of this approach goes beyond the purely pedagogical. It decouples the NEGF Eqs. (44.1–44.3) from MBPT, thus clearing the path for alternative approaches to $\mathbf{\Sigma}_0$ and $\mathbf{\Sigma}_0^{\text{in}}$ including non-perturbative methods as well as phenomenological approaches. In this chapter we will present a simple example of the latter.

44.1.2 Outline

In Sect. 44.2 we will briefly summarize the NEGF equations followed by a brief outline of their derivation from the one-electron Schrödinger equation in Sect. 44.3. In Sect. 44.4 we present toy examples to give the reader a feeling for how the method is applied. Corresponding Python codes are also included for interested readers. We end in Sect. 44.5 with answers to a few commonly asked questions. For more detailed examples and discussions, we refer the reader to Chapter 8 of [27,28], and Part B of [29].

44.2 NEGF Equations

There are three NEGF equations as described below:

1. First is the equation for the quantum *density of states* (times 2π) (Note that the quantum density of states is generally a dense matrix of size $N \times N$ for a lattice size of N ($2N \times 2N$ if electron spin is included). Its diagonal entries correspond to the classical local density of states, but off-diagonal elements also contain useful information. For example, when the quantum density of states is multiplied by Pauli spin matrices, the diagonal elements provide local density of states *for a particular spin* as we show later by an example in Sect. 44.4.6. The matrix nature of $\mathbf{A}$ and $\mathbf{G}^{\text{n}}$ compared to their classical counterparts that are of size $N \times 1$ is due to the quantum generalization of these quantities.):

$$\mathbf{A} = i\left[\mathbf{G}^{\text{R}} - \mathbf{G}^{\text{A}}\right]$$

where the advanced Green function $\mathbf{G}^{\text{A}}$ is the Hermitian conjugate of the retarded Green function $\mathbf{G}^{\text{R}}$ given by ($\mathbf{\Sigma} = \mathbf{\Sigma}_0 + \mathbf{\Sigma}_1 + \mathbf{\Sigma}_2$):

$$\mathbf{G}^{\text{R}} = [E\mathbf{I} - \mathbf{H} - \mathbf{\Sigma}]^{-1} \tag{44.1}$$

2. Next is the equation for the quantum *electron density* (times 2π) per unit energy:

$$\mathbf{G}^{\text{n}} = \mathbf{G}^{\text{R}}\,\mathbf{\Sigma}^{\text{in}}\,\mathbf{G}^{\text{A}} \tag{44.2}$$

3. And finally the current per unit energy $\tilde{I}_m$ at contact m is given by:

$$\tilde{I}_m = \frac{q}{h}\,\text{Trace}\left[\mathbf{\Sigma}_m^{\text{in}}\mathbf{A} - \mathbf{\Gamma}_m\,\mathbf{G}^{\text{n}}\right] \tag{44.3}$$

where $\mathbf{\Gamma}_m = i\left[\mathbf{\Sigma}_m - \mathbf{\Sigma}_m^{\dagger}\right]$.

We use a notation that is slightly different from that used in the conventional literature because it helps provide a physical picture for different quantities. For example, we use $\mathbf{G}^{\text{n}}$ instead of the traditional $-i\mathbf{G}^{<}$ because $\mathbf{G}^{\text{n}}$ represents a matrix version of the *electron density*. The correspondences are summarized in a table to help the reader translate our equations as needed (Table 44.1).

Table 44.1 NEGF symbols used in this chapter and their counterpart in the literature

Conventional symbol	Physical interpretation	Symbol used in this book
$-i\mathbf{G}^{<}$	Matrix electron density	$\mathbf{G}^{\text{n}}$
$+i\mathbf{G}^{>}$	Matrix hole density	$\mathbf{G}^{\text{p}}$
$-i\mathbf{\Sigma}^{<}$	In-scattering function	$\mathbf{\Sigma}^{\text{in}}$
$+i\mathbf{\Sigma}^{>}$	Out-scattering function	$\mathbf{\Sigma}^{\text{out}}$

44.3 NEGF Equations from One-Electron Schrödinger Equation

Let us briefly indicate how the NEGF Eqs. (44.1–44.3) are obtained directly from the one-electron Schrödinger equation $E\,\boldsymbol{\psi} = \mathbf{H}\,\boldsymbol{\psi}$. The first step is to incorporate the effect of the *open boundary conditions* imposed by the contacts through

two additional terms:

$$E\,\boldsymbol{\psi} \;=\; \mathbf{H}\,\boldsymbol{\psi} \;+\; \underbrace{\boldsymbol{\Sigma}\,\boldsymbol{\psi}}_{\text{Outflow}} \;+\; \underbrace{\mathbf{s}}_{\text{Inflow}} \tag{44.4}$$

Note that the modification of the Schrödinger equation by the $\boldsymbol{\Sigma}$ and the $\mathbf{s}$ terms leads to a conceptually different viewpoint of energy. Instead of being the resonant energies of a given system described by $\mathbf{H}$, energy now becomes an independent variable related to the incoming electrons from the contacts that excite the channel (see Chapter 8 of [28] for a detailed discussion).

44.3.1 NEGF Eqs. (44.1) and (44.2)

From Eq. (44.4) we write the wave function as

$$\boldsymbol{\psi} \;=\; [E\mathbf{I} - \mathbf{H} - \boldsymbol{\Sigma}]^{-1}\,\mathbf{s} \;=\; \mathbf{G}^{\mathrm{R}}\,\mathbf{s}$$

making use of the definition of $\mathbf{G}^{\mathrm{R}}$ from NEGF Eq. (44.1). Note that $\boldsymbol{\Sigma}$ is non-Hermitian so that $E\mathbf{I} - \mathbf{H} - \boldsymbol{\Sigma}$ is not singular for any real value of E and has a well-defined inverse $\mathbf{G}^{\mathrm{R}}$.

Since different sources "$\mathbf{s}$" are incoherent, we cannot superpose the resulting $\boldsymbol{\psi}$s from multiple sources. So we define bilinear quantities that *can* be superposed:

$$\underbrace{\boldsymbol{\psi}\boldsymbol{\psi}^{\dagger}}_{\mathbf{G}^{\mathrm{n}}/(2\pi)} \;=\; \mathbf{G}^{\mathrm{R}}\;\underbrace{\mathbf{s}\mathbf{s}^{\dagger}}_{\boldsymbol{\Sigma}^{\mathrm{in}}/(2\pi)}\;\mathbf{G}^{\mathrm{A}}$$

giving us NEGF Eq. (44.2).

In our description $\boldsymbol{\psi}$ is the one-electron wave function whose square gives the probability of finding an electron. When averaged over all electrons in an ensemble, it gives the electron density. More generally $\boldsymbol{\psi}\boldsymbol{\psi}^{\dagger}$ is a matrix whose diagonal elements give the probabilities, and the off-diagonal elements give the correlations. For a more formal justification using field operators, the reader can check the Appendix in [28].

Note that $\mathbf{s}\mathbf{s}^{\dagger}$ reflects the availability of electrons at a given energy in the contacts which fill the available states in the channel giving rise to $\boldsymbol{\psi}\boldsymbol{\psi}^{\dagger}$. Fermi functions are invoked only in the contacts and not in the channel.

44.3.2 NEGF Eq. (44.3)

Starting from the time-dependent version of the modified Schrödinger equation, Eq. (44.4):

$$i\hbar\,\frac{\mathrm{d}}{\mathrm{d}t}\,\boldsymbol{\psi} \;=\; [\mathbf{H}+\boldsymbol{\Sigma}]\,\boldsymbol{\psi} \;+\; \mathbf{s}$$

and its conjugate transpose (noting that $\mathbf{H}$ is a Hermitian matrix):

$$-\,i\hbar\,\frac{\mathrm{d}}{\mathrm{d}t}\,\boldsymbol{\psi}^{\dagger} \;=\; \boldsymbol{\psi}^{\dagger}\,[\mathbf{H}+\boldsymbol{\Sigma}^{\dagger}] \;+\; \mathbf{s}^{\dagger}$$

and making use of the relations:

$$\boldsymbol{\psi} \;=\; \mathbf{G}^{\mathrm{R}}\,\mathbf{s} \quad\text{and}\quad \boldsymbol{\psi}^{\dagger} \;=\; \mathbf{s}^{\dagger}\,\mathbf{G}^{\mathrm{A}},$$

we can write:

$$\begin{aligned} i\hbar\,\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{\psi}\boldsymbol{\psi}^{\dagger} &= \left(i\hbar\,\frac{\mathrm{d}}{\mathrm{d}t}\,\boldsymbol{\psi}\right)\boldsymbol{\psi}^{\dagger} \;+\; \boldsymbol{\psi}\left(i\hbar\,\frac{\mathrm{d}}{\mathrm{d}t}\,\boldsymbol{\psi}^{\dagger}\right) \\ &= ([\mathbf{H}+\boldsymbol{\Sigma}]\,\boldsymbol{\psi}+\mathbf{s})\,\boldsymbol{\psi}^{\dagger} - \boldsymbol{\psi}\left(\boldsymbol{\psi}^{\dagger}\,[\mathbf{H}+\boldsymbol{\Sigma}^{\dagger}] + \mathbf{s}^{\dagger}\right) \\ &= \left[(\mathbf{H}+\boldsymbol{\Sigma})\,\boldsymbol{\psi}\boldsymbol{\psi}^{\dagger} - \boldsymbol{\psi}\boldsymbol{\psi}^{\dagger}(\mathbf{H}+\boldsymbol{\Sigma}^{\dagger})\right] \\ &\quad + \left[\mathbf{s}\mathbf{s}^{\dagger}\mathbf{G}^{\mathrm{A}} - \mathbf{G}^{\mathrm{R}}\mathbf{s}\mathbf{s}^{\dagger}\right] \end{aligned}$$

Making use of:

$$2\pi\,\boldsymbol{\psi}\boldsymbol{\psi}^{\dagger} \;=\; \mathbf{G}^{\mathrm{n}} \quad\text{and}\quad 2\pi\,\mathbf{s}\mathbf{s}^{\dagger} \;=\; \boldsymbol{\Sigma}_{\mathrm{in}}$$

we can write:

$$\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{\psi}\boldsymbol{\psi}^{\dagger} \;=\; \frac{[\mathbf{H}\mathbf{G}^{\mathrm{n}} - \mathbf{G}^{\mathrm{n}}\mathbf{H}]+[\boldsymbol{\Sigma}\mathbf{G}^{\mathrm{n}} - \mathbf{G}^{\mathrm{n}}\boldsymbol{\Sigma}^{\dagger}]+[\boldsymbol{\Sigma}^{\mathrm{in}}\mathbf{G}^{\mathrm{A}} - \mathbf{G}^{\mathrm{R}}\boldsymbol{\Sigma}^{\mathrm{in}}]}{i\,2\pi\hbar}. \tag{44.5}$$

We can interpret $\boldsymbol{\psi}\boldsymbol{\psi}^{\dagger}$ as the number operator so that its derivative represents the current operator. To find the change of any quantity A, we can multiply by the corresponding operator $\mathbf{A}_{\mathrm{op}}$ and take the trace to obtain:

$$\begin{aligned} \frac{\mathrm{d}A}{\mathrm{d}t} = -\frac{i}{\hbar}\mathrm{Trace}([\mathbf{H}\mathbf{G}^{\mathrm{n}} - \mathbf{G}^{\mathrm{n}}\mathbf{H}]\mathbf{A}_{\mathrm{op}} + [\boldsymbol{\Sigma}\mathbf{G}^{\mathrm{n}} - \mathbf{G}^{\mathrm{n}}\boldsymbol{\Sigma}^{\dagger}]\mathbf{A}_{\mathrm{op}} \\ + [\boldsymbol{\Sigma}^{\mathrm{in}}\mathbf{G}^{\mathrm{A}} - \mathbf{G}^{\mathrm{R}}\boldsymbol{\Sigma}^{\mathrm{in}}]\mathbf{A}_{\mathrm{op}}) \end{aligned}$$

The first term represents the change in the quantity A inside the channel due to the action of the Hamiltonian $\mathbf{H}$, while the last two terms represent the "*A current*" injected from the terminals. We can define the terminal current operator $\mathbf{I}_{\mathrm{op}}$ as:

$$\mathbf{I}_{\mathrm{op}} = -\frac{i}{h}\;\left([\boldsymbol{\Sigma}\boldsymbol{G}^{\mathrm{n}} - \mathbf{G}^{\mathrm{n}}\boldsymbol{\Sigma}^{\dagger}] \;+\; [\boldsymbol{\Sigma}^{\mathrm{in}}\mathbf{G}^{\mathrm{A}} - \mathbf{G}^{\mathrm{R}}\boldsymbol{\Sigma}^{\mathrm{in}}]\right) \tag{44.6}$$

such that the "*A current*" can be obtained from the trace of $\mathbf{A}_{\mathrm{op}}\mathbf{I}_{\mathrm{op}}$.

If we are interested only in the charge current, then we need the trace of $\mathbf{I}_{\text{op}}$ since the charge operator is an identity matrix (times the electronic charge). Noting that Trace [**AB**] = Trace [**BA**], we can write:

$$\text{Trace}\,[\mathbf{I}_{\text{op}}] \;=\; \frac{1}{h}\,\text{Trace}\left[\mathbf{\Sigma}^{\text{in}}\mathbf{A} - \mathbf{\Gamma}\mathbf{G}^{\text{n}}\right].$$

Both the left- and the right-hand sides of this equation are zero, since we are discussing steady-state charge transport with no time variation. But the terms on the left can be separated into two parts, one associated with contact 1 and one with contact 2. They tell us the currents at contacts 1 and 2, respectively, and the fact that they add up to zero is simply a statement of *Kirchhoff's law* for steady-state currents in circuits (Note that Eq. (44.6) can also be used to obtain terminal *spin* currents if both sides of the equation are multiplied by Pauli spin matrices corresponding to a desired spin direction. In this case however, the standard Kirchhoff's laws for charge transport may not hold, but it is still possible to design "spin circuits" that obey Kirchhoff's laws [34].). With this in mind, we can write for the current at contact m ($m = 1, 2$):

$$\tilde{I}_m \;=\; \frac{q}{h}\,\text{Trace}\left(\mathbf{\Sigma}_m^{\text{in}}\mathbf{A} \;-\; \mathbf{\Gamma}_m\,\mathbf{G}^{\text{n}}\right)$$

as stated in NEGF Eq. (44.3).

44.4 A Simple Example

In this section we will outline the application of the NEGF Eqs. (44.1) and (44.2) to a simple example centered around a one-dimensional conductor with a barrier U and connected to two contacts with Fermi functions $f_1(E) = 1$ and $f_2(E) = 0$ (Fig. 44.3). The reader can consult Part B of [29] for more details.

44.4.1 Hamiltonian H

We describe the 1D channel using a simple tight-binding Hamiltonian **H** with ε on the diagonal and t on the upper and lower diagonals, as shown pictorially in Fig. 44.4. This leads to a dispersion relation of the form:

$$E(k) \;=\; \varepsilon + 2t\cos(ka) \qquad (44.7a)$$

This cosine dispersion can approximate a parabolic one:

$$E \;=\; E_{\text{c}} + \frac{\hbar^2 k^2}{2m} \qquad (44.7b)$$

if we choose:

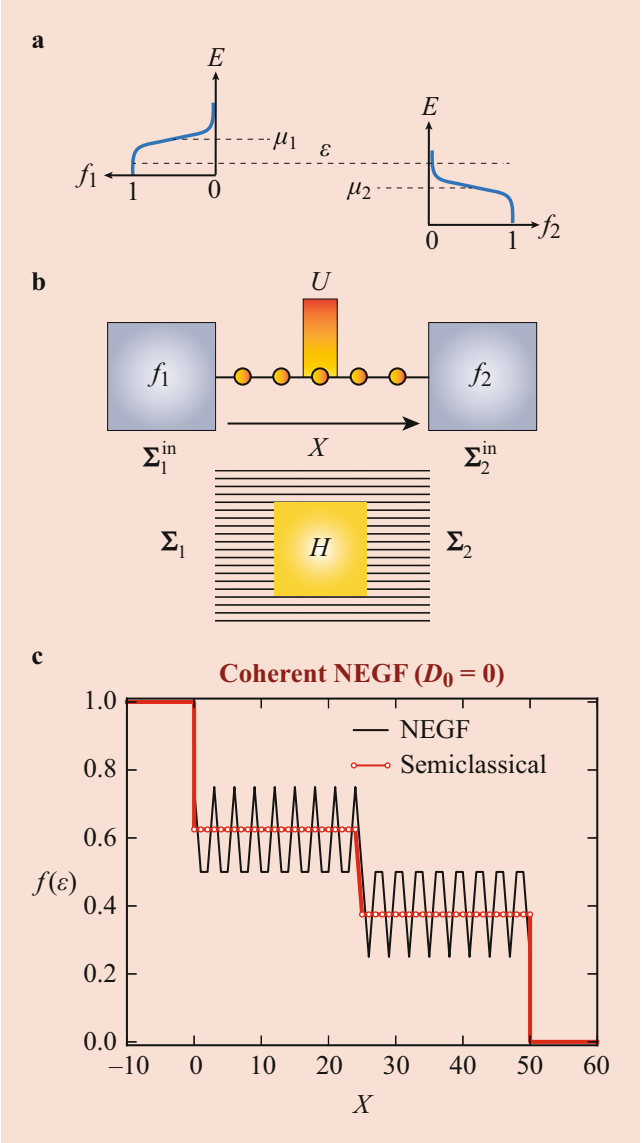

Fig. 44.3 (**a**) A simple one-dimensional conductor with a barrier U and connected to two contacts with Fermi functions $f_1(E) = 1$ and $f_2(E) = 0$. (**b**) To analyze it using the NEGF Eqs. (44.1) and (44.2), we need the **H** to describe the channel and the **Σ**s to describe the physical contacts. Interactions in the channel are ignored in this example ($D_0 = 0$). (**c**) Plot of the occupation factor across the channel

$$E_{\text{c}} \;=\; \varepsilon + 2t \qquad (44.8a)$$

$$\text{and} \qquad -t \equiv t_0 \equiv \frac{\hbar^2}{2ma^2}. \qquad (44.8b)$$

44.4.2 Self-Energy Due to Contacts

The self-energy function for each contact has only one nonzero element corresponding to the point that is connected to that contact:

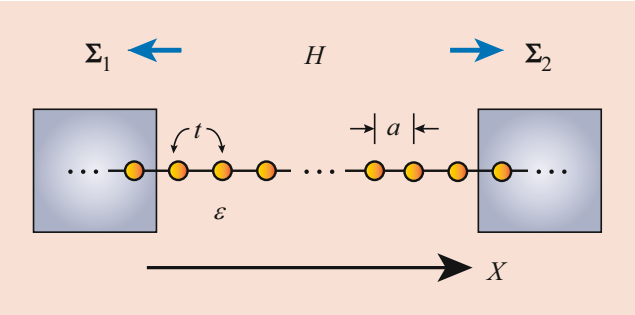

Fig. 44.4 For the one-dimensional examples discussed in this chapter, we use the 1D Hamiltonian shown with on-site elements ε and nearest neighbor coupling t

$$\boldsymbol{\Sigma}_1 = \begin{bmatrix} te^{ika} & 0 & 0 & \cdots & 0 \\ 0 & 0 & 0 & \cdots & 0 \\ 0 & 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 0 \end{bmatrix}, \quad \boldsymbol{\Sigma}_2 = \begin{bmatrix} 0 & \cdots & 0 & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & 0 & 0 \\ 0 & \cdots & 0 & 0 & 0 \\ 0 & \cdots & 0 & 0 & te^{ika} \end{bmatrix}$$

44.4.3 Inscattering from Contacts

The inscattering functions are given simply by the broadening functions times the corresponding occupation factor:

$$\boldsymbol{\Sigma}_1^{\text{in}} = \boldsymbol{\Gamma}_1 f_1 \quad \text{and} \quad \boldsymbol{\Sigma}_2^{\text{in}} = \boldsymbol{\Gamma}_2 f_2 \tag{44.9}$$

where the broadening functions are obtained from $\boldsymbol{\Gamma}_{1,2} = i[\boldsymbol{\Sigma}_{1,2} - \boldsymbol{\Sigma}_{1,2}^\dagger]$:

$$\boldsymbol{\Gamma_1} = \frac{\hbar v}{a} \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 \\ 0 & 0 & 0 & \cdots & 0 \\ 0 & 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 0 \end{bmatrix}, \quad \boldsymbol{\Gamma_2} = \frac{\hbar v}{a} \begin{bmatrix} 0 & \cdots & 0 & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & 0 & 0 \\ 0 & \cdots & 0 & 0 & 0 \\ 0 & \cdots & 0 & 0 & 1 \end{bmatrix}$$

noting that the velocity $v = \mathrm{d}E/(\hbar \mathrm{d}k)$ which from the dispersion relation Eq. (44.7a) equals $-2at/\hbar \sin(ka)$.

Given these matrices it is straightforward to use the NEGF Eqs. (44.1) and (44.2) to evaluate the "electron density" $\mathbf{G}^{\text{n}}/2\pi$ and the "density of states" $\mathbf{A}/2\pi$ from which we can obtain the ℓ-th element of the occupation factor

$$f_\ell = \frac{G^{\text{n}}_{\ell,\ell}}{A_{\ell,\ell}}$$

which is plotted in Fig. 44.3. Note that the NEGF occupation factor shows oscillations due to quantum interference around the average values expected from a semiclassical picture. The semiclassical curve is based on three localized resistors in series, one each at the two interfaces and one at the barrier:

$$\frac{R}{h/q^2} = \underbrace{\frac{1}{2}}_{\text{Channel-source interface}} + \underbrace{\frac{1-T}{T}}_{\text{Barrier}} + \underbrace{\frac{1}{2}}_{\text{Channel-drain interface}} \tag{44.10}$$

where T is the transmission probability through the barrier given by:

$$T(E) = \frac{(\hbar v/a)^2}{U^2 + (\hbar v/a)^2} \tag{44.11}$$

This is a standard result that can be obtained from scattering theory on a discrete lattice [28]; next we will show how the NEGF equations lead to the same result.

44.4.4 Current

If we are not interested in the spatial variation of quantities like the occupation factor but are only interested in the current that flows for a given voltage, we can simply let the channel represent one point and treat the rest as contacts. This makes all matrices collapse to (1×1) reducing them to just numbers:

$$H = \varepsilon + U$$

$$\boldsymbol{\Sigma}_1(E) = te^{+ika} = \boldsymbol{\Sigma}_2(E) \quad \text{where } ka = \cos^{-1}\left(\frac{E-\varepsilon}{2t}\right)$$

$$\boldsymbol{\Sigma}(E) = \boldsymbol{\Sigma}_1(E) + \boldsymbol{\Sigma}_2(E) = 2te^{+ika}$$

$$\boldsymbol{\Gamma}_1 = \frac{\hbar v}{a} = \boldsymbol{\Gamma}_2$$

$$\boldsymbol{\Sigma}_1^{\text{in}} = \boldsymbol{\Gamma}_1 f_1, \quad \boldsymbol{\Sigma}_2^{\text{in}} = \boldsymbol{\Gamma}_2 f_2 \quad \text{and} \quad \boldsymbol{\Sigma}^{\text{in}} = \boldsymbol{\Gamma}_1 f_1 + \boldsymbol{\Gamma}_2 f_2$$

Now we do not need a computer to evaluate the NEGF Eqs. (44.1–44.3). We can just do it by hand. First we calculate G^{R} from Eq. (44.1):

$$\begin{aligned} G^{\text{R}}(E) &= \frac{1}{E - (\varepsilon + U) - 2te^{ika}} \\ &= \frac{1}{-U - i2t\,\sin(ka)} \\ &= \frac{1}{-U + i\hbar v/a} \end{aligned}$$

so that:

$$\begin{aligned} G^{\text{A}}(E) &= \frac{1}{-U - i\hbar v/a} \\ A(E) &= \frac{2\hbar v/a}{U^2 + (\hbar v/a)^2} \end{aligned}$$

Next from Eq. (44.2):

$$G^{\text{n}} = \frac{\hbar v/a}{U^2 + (\hbar v/a)^2}(f_1 + f_2)$$

so that from Eq. (44.3):

$$\tilde{I}(E) = \frac{q}{h}\frac{(\hbar v/a)^2}{U^2+(\hbar v/a)^2}\left(2f_1 - \overline{f_1+f_2}\right)$$
$$= \frac{q}{h}\underbrace{\frac{(\hbar v/a)^2}{U^2+(\hbar v/a)^2}}_{T(E)}\left(f_1 - f_2\right)$$

The quantity $T(E)$ represents the transmission probability through the barrier U. Integrating $\tilde{I}$(E) we get the total current. The quantity $T(E)$ is the same as the semiclassical transmission that was shown in Eq. (44.11).

44.4.5 Dephasing Interactions

What we have done so far represents coherent transport with no interactions in the channel. In this limit, the results could also have been obtained from the scattering theory of transport, sometimes referred to as the Landauer-Büttiker formalism. The NEGF method provides a convenient way to get the same results. However, the NEGF method also allows us to include channel interactions through the self-energy functions $\mathbf{\Sigma}_0$, $\mathbf{\Sigma}_0^{\text{in}}$.

It is important to include these interactions because the purely coherent model predicts quantum interference effects like the oscillations in Fig. 44.3 which are usually not seen experimentally except at extremely low temperatures. The reason is that the phase of individual electrons is destroyed by the random scattering potential it sees due to the other electrons. Such electron-electron interactions normally do not lead to any overall loss of momentum from the system of electrons and so have little effect on the mobility or the current. But they do lead to dephasing which suppresses the coherent oscillations. Dephasing may also arise from other sources such as electron-phonon interactions [35]. However, they usually cause momentum relaxation as well, thereby affecting the resistance. We specifically mention electron-electron interaction because it can cause dephasing without having any first-order effect on the resistance. Resistance typically becomes temperature independent around 10 K, once phonons have frozen out. But electron-electron interactions continue to cause dephasing, and it usually takes much lower temperatures to see interference effects.

The classic NEGF provides definite prescriptions for including all such effects from first principles starting from a microscopic Hamiltonian using MBPT as described in many available references. Here we will use a phenomenological approach that incorporates dephasing in terms of a single parameter D_0 which can be adjusted to reflect experimental dephasing times:

$$\mathbf{\Sigma}_0 = D_0\,\mathbf{G}^{\text{R}} \tag{44.12a}$$
$$\mathbf{\Sigma}_0^{\text{in}} = D_0\,\mathbf{G}^{\text{n}} \tag{44.12b}$$

Note that we now need to solve Eqs. (44.1) and (44.2) self-consistently since the same quantity appears on both the left- and right-hand sides:

$$\mathbf{G}^{\text{R}} = \left[E\mathbf{I} - \mathbf{H}[\mathbf{\Sigma_1} - \mathbf{\Sigma_2} - D_0\mathbf{G}^{\text{R}}\right]^{-1} \tag{44.13a}$$
$$\mathbf{G}^{\text{n}} = \mathbf{G}^{\text{R}}\,[\mathbf{\Sigma}_1^{\text{in}} + \mathbf{\Sigma}_2^{\text{in}} + D_0\mathbf{G}^{\text{n}}\,]\mathbf{G}^{\text{A}} \tag{44.13b}$$

The self-consistent calculation is straightforward to implement numerically, and a Python code is provided for readers interested in reproducing the results shown in Figs. 44.3 and 44.5. Note that the results for pure dephasing agree well with the simple semiclassical model based on series resistors (Eq. 44.10) as described earlier. Figure 44.5 also shows results for a slightly different model of interactions which relaxes both phase and momentum leading to a linear drop in the occupation factor across the channel like an ohmic resistor. In this slightly different model, the diagonal elements of $\mathbf{\Sigma}_0$ and $\mathbf{\Sigma}_0^{\text{in}}$ are the same as before, but all off-diagonal elements are set to zero [36, 37].

Intuitively, we can justify the pure phase relaxation model by thinking of it as distributed "Büttiker probes" that take electrons out of the channel and reinject them back into it to break their phase coherence [38]. But because the electron density ($\mathbf{G}^{\text{n}}$) is preserved *exactly* by constant multiplication, no property other than phase is relaxed. In contrast, just keeping the diagonal elements of the $\mathbf{G}^{\text{n}}$ in the real space representation breaks momentum in addition to phase since the reinjected electrons have no definite momentum and can flow in any direction. This intuition allows an immediate extension to spin-preserving but momentum-relaxing $\mathbf{\Sigma}_0$ as follows: supposing we express $\mathbf{H}$, $\mathbf{G}^{\text{n}}$ and lead $\mathbf{\Sigma}$s in $2N \times 2N$ matrices for a lattice of N points, following the same principle, we could write down a spin-conserving but momentum- and phase-relaxing $\mathbf{\Sigma}_0$ as:

$$\mathbf{\Sigma}_0 = \begin{bmatrix} \begin{bmatrix}1&1\\1&1\end{bmatrix} & 0 & \cdots\cdots & 0 \\ 0 & \begin{bmatrix}1&1\\1&1\end{bmatrix} & 0 \cdots & 0 \\ \vdots & \vdots & \vdots\ddots & \vdots \\ 0 & 0 & \cdots\cdots & \begin{bmatrix}1&1\\1&1\end{bmatrix} \end{bmatrix},$$

where the 2×2 blocks in each lattice point preserve spin information but phase and momentum are relaxed. Indeed, using this principle, we can write down $\mathbf{\Sigma}_0$s that can preserve information within *any* unit cell with B basis functions by having $B \times B$ blocks of all 1s that preserve local correlations

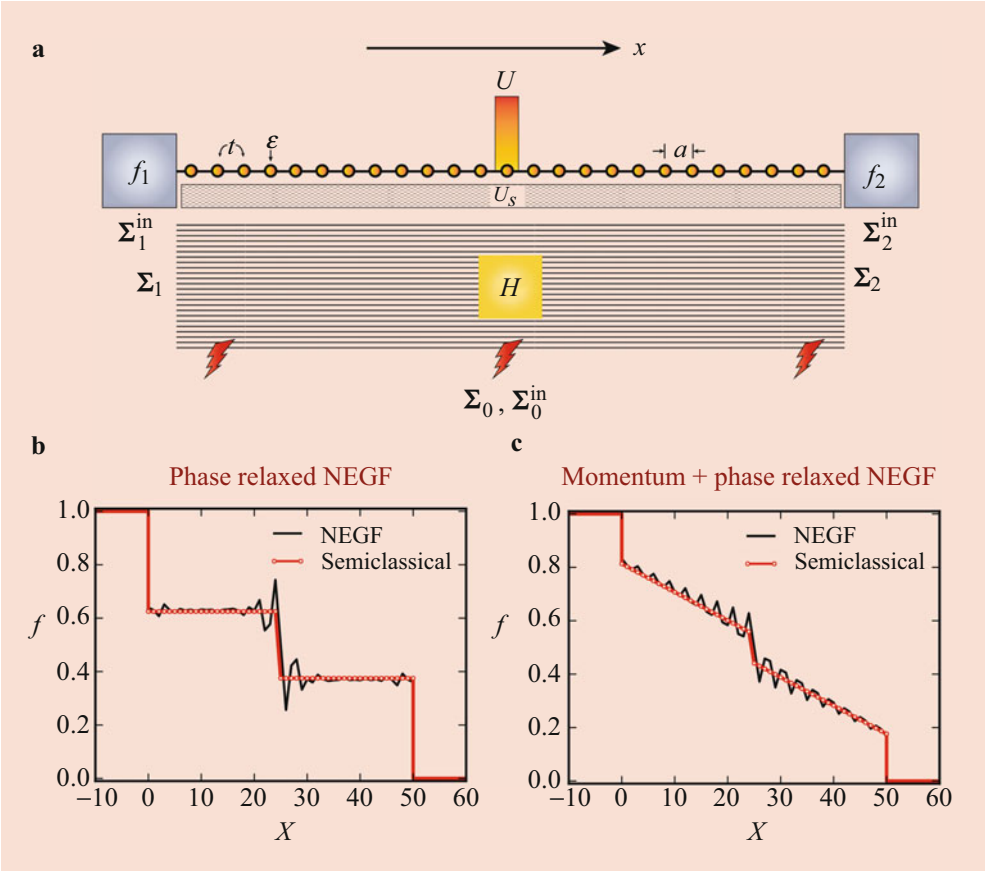

Fig. 44.5 (**a**) Same problem as in Fig. 44.3 but we now include the effect of a random potential U_S. (**b**) The effect of the random potential is incorporated through $\mathbf{\Sigma}_0$ and $\mathbf{\Sigma}_0^{in}$ where the magnitude of scattering, D_0, is $0.09\, t_0^2$. (**c**) Plot of occupation factor across channel for phase-relaxing scattering. (**d**) Plot of occupation factor across channel for phase- and momentum-relaxing scattering

in $\mathbf{G}^n$. In the next subsection, we show an example of spin-conserving dephasing in the context of spin transport.

44.4.6 Diffusive Spin Transport Using NEGF

Spin electronics or spintronics that combine spin transport with magnetics has attracted much attention in recent years [39]. Of particular interest are the so-called high spin-orbit materials such as Rashba channels or interfaces [40–43] as well as topological insulators [44] or heavy metals with high spin-orbit coupling [45,46]. NEGF allows a natural extension to incorporate spin transport in the tight-binding framework which makes the Hamiltonian for a lattice of N points a $2N \times 2N$ matrix. For example, consider a channel with a Rashba spin-orbit interaction that is described by the Hamiltonian:

$$\mathbf{H} = \mathbf{H}_0 + \eta\, (\boldsymbol{\sigma}_x k_y - \boldsymbol{\sigma}_y k_x) \tag{44.14}$$

where $\mathbf{H}_0$ represents the usual effective mass Hamiltonian, η is the Rashba coefficient, and $\boldsymbol{\sigma}$s are Pauli spin matrices. We can think of the Rashba interaction as an effective magnetic field that depends on the momentum of an electron if we associate $|\eta \mathbf{k}|$ as the magnitude of the effective magnetic field. Indeed, injecting x directed spins by using ferromagnetic contacts with momentum $(\pm k_x)$ can cause periodic oscillations of their spin, since these electrons would feel an effective magnetic field in the y direction. This effect was initially proposed in [47] and experimentally confirmed in [48], followed later by full demonstrations including the contacts [49–51].

Here, our purpose is to simply show how the NEGF formalism can be useful in modeling this effect in the presence of *momentum, phase, and spin* relaxations in a toy model. Figure 44.6a shows an NEGF simulation of 1D wire with Rashba spin-orbit coupling, attached to two ferromagnetic leads that point in the x direction. The left lead is an x-directed ferromagnet that injects x-spins in the channel. In the presence of momentum and phase relaxation, the chemical potential for charge goes steadily down as in Fig. 44.5. We can calculate the corresponding *spin* potentials by:

$$f_\ell^{x,y,z} = \frac{\text{Trace}\left[\mathbf{G}^n_{\ell,\ell}\, \boldsymbol{\sigma}_{x,y,z}\right]}{\text{Trace}\left[\mathbf{A}_{\ell,\ell}\right]}$$

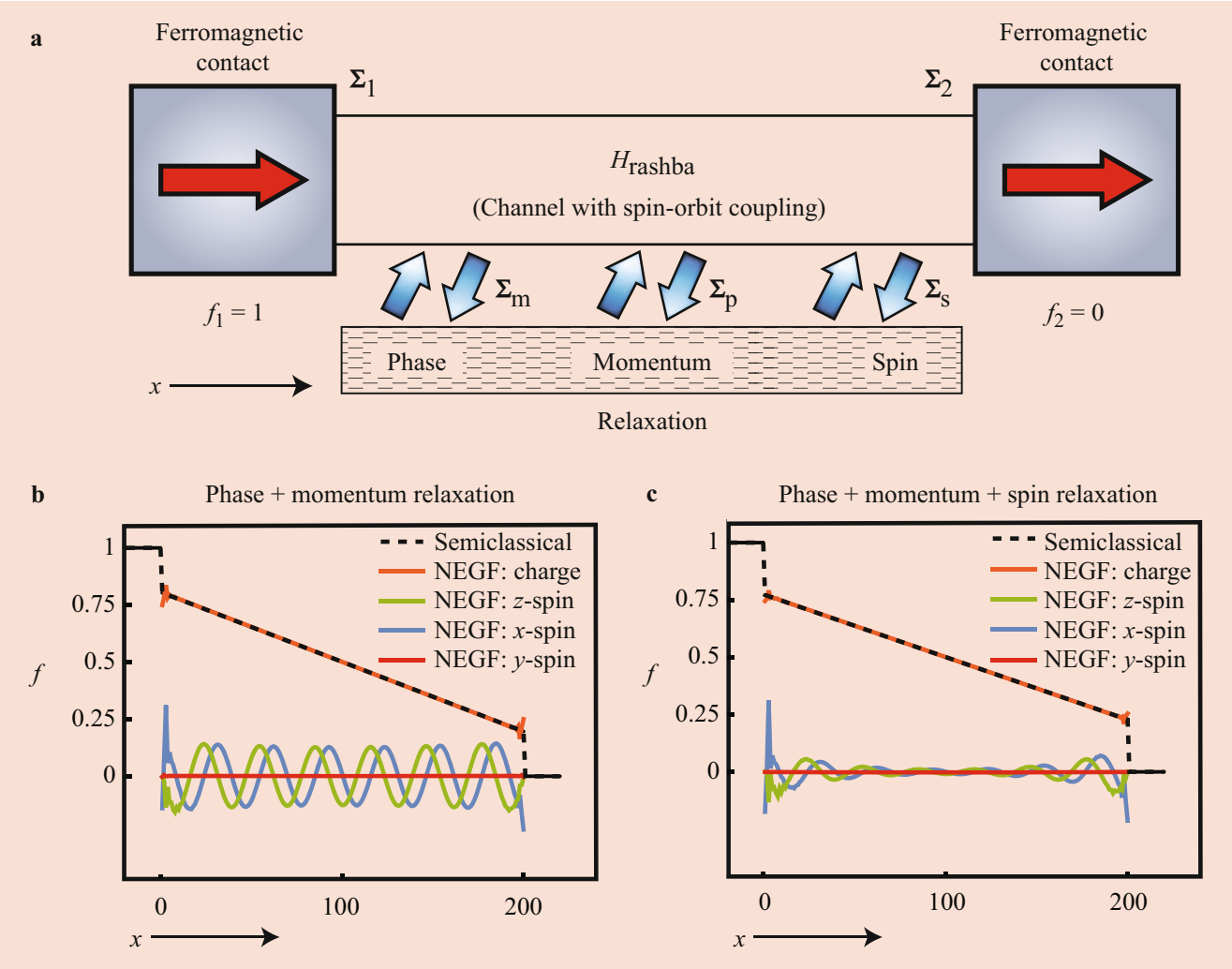

Fig. 44.6 (**a**) Rashba channel with ferromagnetic leads. Phase, momentum, and spin relaxation can be introduced to the system independently. (**b**) Spin precession is possible when $+x$-spins are injected to the channel even in the presence of phase and momentum relaxation. (**c**) Adding spin relaxation attenuates spin precession. (Python code available at the end of the article)

where "Trace" indicates tracing the 2×2 blocks of $\mathbf{G}^{\text{n}}$ and $\mathbf{A}$ at lattice point ℓ and $\boldsymbol{\sigma}$s are 2×2 Pauli spin matrices. Interestingly, if there is little to no spin relaxation, we see that the x-spins rotate in the channel even in the presence of high momentum and phase relaxation due to the effective magnetic field that is exerted on the x-spins by the Rashba channel. In practice, however, momentum relaxation in high spin-orbit materials is known to give rise to strong spin relaxation through the Elliott-Yafet [52] mechanism. Our purpose is simply to show that it is possible to include spin relaxation *independently* of momentum relaxation. This allows us to flexibly choose phase, momentum, and spin relaxation rates to match experimentally measured quantities when modeling real experiments. As discussed in [37], a possible spin flip relaxation model, $\boldsymbol{\Sigma}_0^{\text{sf}}$ can be written as:

$$\boldsymbol{\Sigma}^{\text{sf}}_{0,i,j} = D_0(\boldsymbol{\sigma}_x \mathbf{G}^{\text{n}}_{i,j} \boldsymbol{\sigma}_x + \boldsymbol{\sigma}_y \mathbf{G}^{\text{n}}_{i,j} \boldsymbol{\sigma}_y + \boldsymbol{\sigma}_z \mathbf{G}^{\text{n}}_{i,j} \boldsymbol{\sigma}_z) \qquad (44.15)$$

where the $\boldsymbol{\Sigma}_0^{\text{sf}}$ acts on all 2×2 subblocks of the $\mathbf{G}^{\text{n}}$ matrix that are labeled $\mathbf{G}^{\text{n}}_{i,j}$. By multiplying the terms out, we can easily see the effect of this dephasing is to reinject an electron *with an opposite spin* back to the channel that relaxes spin. In Fig. 44.6c we show how a pure spin relaxation model can be added in addition to momentum and phase breaking to reduce the spin signals in the channel.

44.4.7 Application to Superconducting Devices

An important application of the NEGF method is to devices where one of the contacts or the channel is superconducting. This is of great current interest due to the excitement surrounding the search for Majorana bound states (MBS) or equivalently Majorana zero modes (MZM) in Rashba

nanowire systems in proximity with superconductors [53–57]. It would take us too far afield to discuss the significant conceptual extensions needed for these problems, and so we will refer interested readers to a couple of old papers [58,59] and some recent ones [60–62].

44.5 Frequently Asked Questions

44.5.1 Shouldn't We Also Consider the Poisson Equation for Modeling Real Devices?

Yes. Earlier we mentioned the role of electron-electron interactions in causing dephasing which can be included through the anti-Hermitian part of the self-energy function $\mathbf{\Sigma}_0$. A far more important effect of electron-electron interactions is manifested through the Hermitian part of $\mathbf{\Sigma}_0$ which effectively modifies the Hamiltonian $\mathbf{H}$. The most important part of $\mathbf{\Sigma}_0$ is just the Coulomb potential U arising from the electron density $\mathbf{G}^n/2\pi$ and can be obtained by solving the Poisson equation and is often called the Hartree term. In addition there are more subtle contributions to $\mathbf{\Sigma}_0$ generally referred to as exchange and correlation effects which subtract from the Hartree term, see, for example, Chapter 2 of [28].

Since $\mathbf{\Sigma}_0$ depends on $\mathbf{G}^n$, this requires a self-consistent calculation: we start by assuming $\mathbf{\Sigma}_0 = 0$, use Eqs. (44.1) and (44.2) to calculate $\mathbf{G}^n$, use $\mathbf{G}^n$ to calculate $\mathbf{\Sigma}_0 = 0$, recalculate $\mathbf{G}^n$ from Eqs. (44.1) and (44.2), and so on till the results converge. This requirement for an iterative solution makes it much more difficult to calculate the energy levels even for helium which has two electrons compared to hydrogen which has only one electron and hence no electron-electron interactions.

Two more points to note. Firstly, in device simulations, it is common to use the Hamiltonian $\mathbf{H}$ from semiempirical methods that already include the $\mathbf{\Sigma}_0$ for a uniform channel material in equilibrium. As such it is necessary to include *only* the *change* in $\mathbf{\Sigma}_0$ when the channel is driven out of equilibrium by the applied bias. Secondly, this correction is not important for low applied voltages but plays a very significant role at high voltages. Indeed one can say that the saturation current for transistors is largely controlled by the Hartree term, making it primarily an electrostatically controlled device.

44.5.2 Can You Arbitrarily Designate the Ends as Contacts?

Designating a region as a contact implies that there is a significant increase in the number of conducting channels due to an increase in width and/or in the density of states. When analyzing a given structure, it is important to scrutinize the results carefully, to make sure that the assumed contacts are indeed functioning as nearly ideal reservoirs.

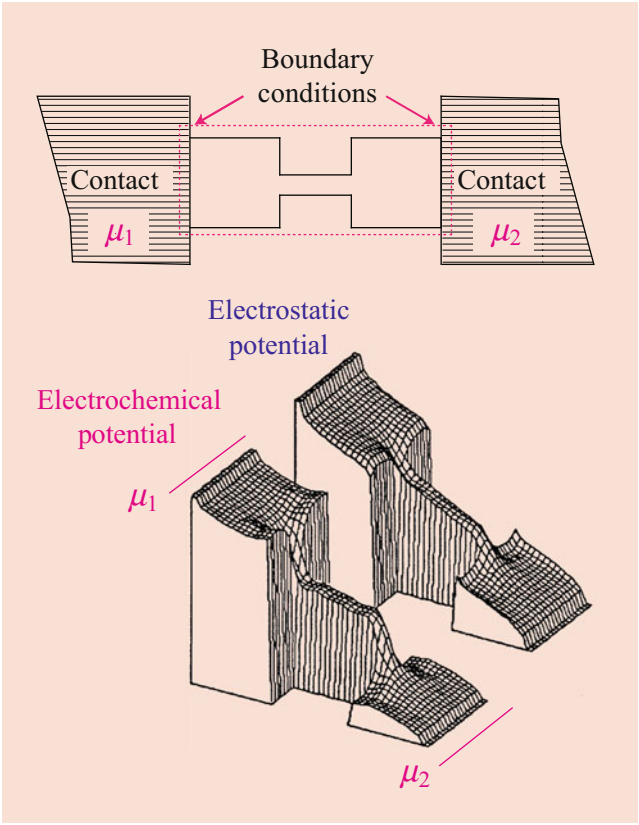

Fig. 44.7 A wide-narrow-wide ballistic constriction where the contacts are imposed inside the widest region. A numerical simulation with phase scattering shows the 2D profile of electrochemical and electrostatic potentials. (Reprinted Fig. 27b of [7] with permission from Michael et al. Copyright (1991) by the American Physical Society)

For example, Fig. 44.7 is an excerpt from an old paper showing a wide-narrow-wide structure (see Fig. 27a of [7]). We impose the contact boundary conditions inside the widest region as shown. Note the sharp drops in the occupation factor (or electrochemical potential) at the narrow-wide interfaces due to the interface resistance. The electrostatic potential is obtained by convolving the electrochemical potential with a screening function as explained in the paper (Fig. 27b of [7]). Note also the small drops where the wide regions meet the contacts indicating a small interface resistance.

One could save computation time by imposing the contact in the wide region rather than in the widest region. This may or may not be acceptable depending on how conductive the wide region is relative to the narrow region. A related phenomenon called the "source-starvation" effect where contact-like wide regions are driven out of equilibrium has been discussed in the context of ballistic nanotransistors [63].

44.5.3 Does NEGF Give the Correct Coherent and Semiclassical Limits?

Yes, with small dephasing, it matches the scattering theory for coherent transport, also called the Landauer-Büttiker formalism. With sufficient dephasing, it reproduces results from the semiclassical Boltzmann method, thus providing a bridge from quantum to semiclassical transport. The example presented earlier shows how the NEGF result for coherent transport includes oscillations around the Boltzmann result, which damp out when dephasing is included. Many such examples are included in [29] essentially as homework problems that are easily reproduced.

44.5.4 How Is This Related to the Kubo Formalism?

The Kubo formalism is a linear response theory based on small perturbations close to equilibrium. Many of the problems in modern nanoelectronics require a framework that can handle transport far from equilibrium. The results from NEGF agree with the Kubo formalism in the linear response regime close to equilibrium.

Isn't It a Problem to Have Separate Electrochemical Potentials in a Single System?

On the contrary, we would argue that current flow requires separate electrochemical potentials, just as the flow of heat requires separate temperatures. There is nothing fundamentally wrong with invoking two large reservoirs held at two different electrochemical potentials and/or temperatures connected by a nanoscale conductor.

Doesn't the Kubo Formula Use a Single Electrochemical Potential?

Yes, the Kubo formalism calculates an equilibrium quantity, namely, the noise, and relates it to the linear transport coefficients through the fluctuation-dissipation theorem. But this only works for transport close to equilibrium and is not possible in general. NEGF on the other hand addresses the nonequilibrium problem directly. Like the Boltzmann equation, NEGF too permits the use of separate electrochemical potentials as boundary conditions.

Can't You Have Equilibrium Currents with a Single Electrochemical Potential?

Yes, but these are distinct from the transport currents we are discussing. For example, in the quantum Hall regime, there are circulating edge currents which involve all electrons and not just the ones with energies close to μ. But these are normally not measured with external probes.

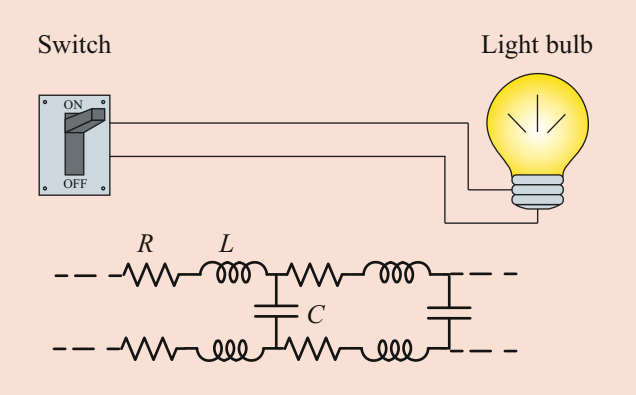

Fig. 44.8 When we turn the switch on, a signal propagates to the light bulb which can be described by a distributed *RLC* model. The capacitance *C* and the inductance *L* are determined primarily by electrostatics and magnetostatics, respectively

44.5.5 Isn't the Flow of Electricity Essentially a Many-Body Process?

As undergraduates we learn that current flow, at least in metals, is a many-body interacting process: when we turn the switch on, a signal propagates to the light bulb at the speed of light. One electron pushes the next electron, which pushes the next electron and so on. If we had to wait for an electron to transmit from the switch to the bulb, it would take far too long. And so it might seem futile to describe current flow without invoking many-body interactions. However, we believe that while signal propagation cannot be analyzed without interactions, the low-frequency resistance can be (Fig. 44.8).

This signal propagation can be described quantitatively by a distributed *RLC* model [64] (For a spin generalization of similar ideas, see [65].). The *L*s and *C*s in this model have a transport component but usually represent primarily the interactions, and the velocity is given by $1/\sqrt{LC}$. However, these parameters are not involved in determining the steady-state or *dc* current since at low frequencies the *L*s appear as short circuits and the *C*s are open circuits. The low-frequency resistance *R* can be understood at least approximately without invoking interactions.

This observation appears to apply to quantum transport as well. For example, in 1985 Richard Webb and collaborators from IBM reported [66] the Aharonov-Bohm (AB) effect in metallic rings with a period described quite well by the one-electron theory without interactions, as if we were talking about AB paths in vacuum! The one-electron picture works so well possibly because there is a Landau-style (We mean Landau, not Landauer!) dressed quasiparticle that "actually" moves from left to right. We have some mental pictures of what such a quasi-electron looks like, but we are not aware of any serious discussions along these lines.

Are Many-Body Effects Irrelevant in Transport Experiments?

That is not at all what we mean. Our point is that many-body effects are fairly obvious at high frequencies starting with the well-known fact that signals travel at the speed of light and not at the speed of electrons. By contrast their role at low frequencies are more subtle, like Coulomb blockade and the Kondo effect. More recently experiments on graphene have revealed intriguing evidence of collective motion [67].

In a volume published on the occasion of the 50th anniversary of *Anderson localization*, Phil Anderson commented "…What might be of modern interest is the channel concept which is so important in localization theory. The transport properties at low frequencies can be reduced to a sum over one dimensional channels."

Note the qualification *low frequencies*. Transmission of an electron from the left to the right contact is essential only for steady-state charge transport. High-frequency currents can flow capacitively without end-to-end transfer of electrons. Also, experiments have revealed that spins can be transported across insulators by magnons without the actual transmission of electrons (See, for example, [68,69] for possible practical applications of such pure spin conductors).

Would NEGF Be Suitable for Describing Such Effects?

NEGF provides a clear prescription for including arbitrary interactions to any desired order in perturbation theory. But some effects may require us to go beyond MBPT: perhaps a non-perturbative approach or a different perturbation parameter. Single-electron charging effects provide a good example [70].

44.5.6 How Can We Teach NEGF Without Advanced Quantum Statistical Mechanics?

The NEGF Eqs. (44.1) and (44.2) are essentially the same as Eqs. (75)–(77) of L. V. Keldysh [3], which is one of the seminal papers on the NEGF method that obtained these equations using MBPT and established the "diagram technique for nonequilibrium processes" for calculating the self-energy functions $\mathbf{\Sigma}_0$ and $\mathbf{\Sigma}_0^{\text{in}}$. Much of the literature is based on the original MBPT-based approach, and this makes it inaccessible to those unfamiliar with advanced quantum statistical mechanics.

We obtain the NEGF equations directly from a one-electron Schrödinger equation using relatively elementary arguments. These equations have been used to discuss many problems of great interest like quantized conductance, (integer) quantum Hall effect, Anderson localization, resonant tunneling, and spin transport without a systematic treatment of many-body effects. But it goes beyond purely coherent transport allowing us to include phase-breaking interactions (both momentum-relaxing and momentum-conserving) within a self-consistent Born approximation.

The NEGF equations provide a unified framework for such problems, spanning a wide range of materials and phenomena all the way from molecular to ballistic to diffusive transport, and have been widely adopted by the nanoelectronics community for device analysis and design.

44.5.7 But Is This the Real NEGF?

- The answer is NO, if we associate NEGF with the MBPT commonly used to obtain $\mathbf{\Sigma}_0$ and $\mathbf{\Sigma}_0^{\text{in}}$ appearing in Eqs. (44.1–44.3).
- The answer is YES, if we associate NEGF with Eqs. (44.1–44.3) irrespective of how the $\mathbf{\Sigma}$s are obtained.

Which answer we choose is clearly a matter of perspective, but the second viewpoint seems more in keeping with semiclassical transport theory, where the (steady-state) Boltzmann approach is identified with the equation:

$$\boldsymbol{v} \cdot \nabla f + \mathbf{F} \cdot \nabla_p f = S_{\text{op}} f$$

and NOT with the evaluation of the scattering operator S_{op} which is analogous to the $\mathbf{\Sigma}$s in NEGF. While the concept of the collision integral involved in S_{op} was well-known, the quantitative details of its evaluation has evolved significantly since the days of Boltzmann. Similarly, totally new approaches that go beyond many-body perturbation theory (MBPT) for evaluating the $\mathbf{\Sigma}$s have been and will be developed as we apply NEGF to newer problems.

44.5.8 Contacting Schrödinger

In summary, we feel that the scope and utility of the NEGF equations Eqs. (44.1–44.3) transcend the MBPT-based approach originally used to derive it. NEGF teaches us how to combine quantum dynamics with "contacts" much as Boltzmann taught us how to combine classical dynamics with "contacts," using the word "contacts" in a broad figurative sense to denote all kinds of entropy-driven processes. There are many problems of fundamental and applied significance that can be simulated straightforwardly within the NEGF method without a first principle treatment of many-body effects which in any case would be perturbative in nature. This includes novel phenomena like the (integer) quantum Hall effect as well as new devices like magnetic tunnel junctions. As such, we feel that this elegant framework for "contacting" the Schrödinger equation should be of broad interest to anyone working on device physics or nonequilibrium statistical mechanics in general.

Python codes for Figs. 44.3 and 44.5

```
# This code illustrates how to perform NEGF calculations on a simple
# 1D device with one scatterer in the middle of the channel region.
import numpy as np
import matplotlib.pyplot as plt
fontPlan = {'family': 'sans','weight': 'bold','size': 12,'color':'darkred',}

t0 = 1; Np = 51; X = np.arange(0,Np,1); Nh = int(Np/2);
zplus = 1e-12*1j
L = np.diag(np.append(1, np.zeros(Np-1)))
R = np.diag(np.append(np.zeros(Np-1), 1))
option = 'coherent' # This generates the bottom plot in Fig. 3
# use option = 'phase-relaxation' for Fig. 5c
#or option = 'both-relaxation' for Fig. 5d

DList = np.array([0, 9e-2*t0**2]); sigB = np.zeros(Np); siginB = np.zeros(Np)
H0 = 2*t0*np.diag(np.ones(Np))- t0*np.diag(np.ones(Np-1),1) \
- t0*np.diag(np.ones(Np-1),-1)                # 1D Hamiltonian
N1 = Nh; UB1 = 1*t0; H0[N1][N1] = H0[N1][N1] + UB1; H = H0
EE = t0; ck = (1-(EE+zplus)/(2*t0)); ka = np.arccos(ck); v = 2*t0*np.sin(ka)

# Semiclassical profile
T = np.real(v**2/(UB1**2+v**2)); R1 = (1-T)/T
D = DList[0] if option.lower() != 'both-relaxation' else DList[1]
TT = np.real(v**2/(D+v**2)); R2 = 1*(1-TT)/TT
RR = np.append(0.5,np.append(R2*np.ones(Nh),R1))
RR = np.append(RR,np.append(R2*np.ones(Nh),0.5))
RR = np.cumsum(RR); Vx = np.ones(Np+2)-(RR/RR[Np+1]); Fclass = Vx[1:Np+1]

# Based on resistance estimates
s1 = -t0*np.exp(1j*ka); sig1 = np.kron(L,s1); ck=(1-(EE+zplus)/(2*t0))
ka = np.arccos(ck); s2 = -t0*np.exp(1j*ka); sig2 = np.kron(R,s2)
gam1 = 1j*(sig1-np.conj(sig1.T)); gam2 = 1j*(sig2-np.conj(sig2.T))
G = np.linalg.inv((EE*np.eye(Np))-H-sig1- sig2)
Tcoh = np.real(np.trace(gam1*G*gam2*np.conj(G.T)))

if option.lower()!='phase-relaxation': ff = lambda x,y: np.diag(np.diag(x*y))
else: ff = lambda x,y: x*y;
D = DList[0] if option.lower()=='coherent' else DList[1]
change = 100
while change > 1e-6:
    G = np.linalg.inv((EE*np.eye(Np)) - H - sig1 - sig2 - sigB)
    sigBnew = ff(D,G); change = np.sum(np.sum(np.abs(sigBnew - sigB)))
    sigB = sigB + 0.25*(sigBnew - sigB)
A = np.real(np.diag(1j*(G-np.conj(G.T)))); change = 100
while change > 1e-6:
    Gn = np.matmul(G,np.matmul((gam1 + siginB),np.conj(G.T)))
    siginBnew = ff(D,Gn); change = np.sum(np.sum(np.abs(siginBnew - siginB)))
    siginB = siginB + 0.25*(siginBnew - siginB)
F = np.real(np.diag(Gn))/A

Xclass = np.append(np.arange(-10,0,1), np.append(-0.001,X))
Xclass = np.append(Xclass, np.append(50.001,np.arange(51,61,1)))
FclassFull = np.append(np.ones(11), np.append(Fclass,np.zeros(11)))

plt.plot(X,F,'k-', label='NEGF',linewidth=1.0)
plt.plot(Xclass, FclassFull ,'r-', linewidth=1.5)
plt.plot(X, Fclass ,'ro-', label='Semiclassical', linewidth=1.0,markersize=2)
plt.xticks(fontsize=10); plt.yticks(fontsize=10); plt.xlim(-10,60)
plt.ylim(-0.01,1.01); plt.xlabel('z', fontdict=fontPlan)
plt.ylabel('f', fontdict=fontPlan)
plt.legend(frameon=False,fontsize = 10, loc = 'best'); plt.show()
```

Python code for Fig. 44.6

```
# This code illustrates how to perform NEGF calculations on a simple
# 1D device with Rashba channel.
import numpy as np
import matplotlib.pyplot as plt
fontPlan = {'family': 'sans','weight': 'bold','size': 12,'color':'darkred',}

LL = 200e-10; h = 6.62e-34/2/np.pi; a = 1e-10; NM = int(np.ceil(LL/a));
m = 9e-31; q = 1.6e-19; t0 = h**2/(2*m*a**2)/q; I2 = np.eye(2);
Pauli_y = np.array([[0+0j, 0-1j], [0+1j, 0+0j]])
Pauli_z = np.array([[1+0j, 0+0j], [0+0j, -1+0j]])
Pauli_x = np.array([[0+0j, 1+0j], [1+0j, 0+0j]])

SZ = np.kron(np.eye(NM),Pauli_z); SX = np.kron(np.eye(NM), Pauli_x);
SY = np.kron(np.eye(NM), Pauli_y); SI = np.kron(np.eye(NM), I2);
S0 = np.mod(np.kron(np.eye(NM), np.array([[1, 1], [1, 1]])) + \
np.ones((2*NM, 2*NM)), 2);
S1 = np.kron(np.eye(NM), np.array([[1, 1], [1, 1]]));
S11 = np.ones((2*NM, 2*NM));

DP = 0.09*t0**2 ;DM = 0.15*t0**2; DS = 0.00125/4*t0**2; eta = 0.2*t0;
alpha = np.array([[2*t0, 0], [0, 2*t0]]) ;
gamma = np.array([[-t0, 0], [0, -t0]]) - eta*Pauli_y/2j

H = np.kron(np.eye(NM), alpha) + np.kron(np.diag(np.ones(NM-1),
-1),gamma) \
```

```
+ np.kron(np.diag(np.ones(NM - 1), +
      1),np.conj(gamma.T))

zplus = 1j*1e-12; EE = t0; ka = np.arccos(1 - (EE +
      zplus)/(2*t0));
px1 = 0.95; py1 = 0.0; pz1 = 0.0; px2 = 0.95; py2 = 0.0;
      pz2 = 0.0;
sigma1 = -t0*np.exp(1j*ka)*(I2 + pz1*Pauli_z +
      px1*Pauli_x + py1*Pauli_y);
sigma2 = -t0*np.exp(1j*ka)*(I2 + pz2*Pauli_z +
      px2*Pauli_x + py2*Pauli_y);

LL = np.zeros(NM); RR = np.zeros(NM); LL[0] = 1;
      RR[NM-1] = 1;
Sigma1 = np.kron(np.diag(LL), sigma1); Sigma2 =
      np.kron(np.diag(RR), sigma2);
SigmaB = 0*Sigma1; SigmaIn = 0*Sigma1;
Gamma1 = 1j*(Sigma1 - np.conj(Sigma1.T));
Gamma2 = 1j*(Sigma2 - np.conj(Sigma2.T));

f1 = 1; f2 = 0; error = 1;
while error > 1e-5:
  GR = np.linalg.inv(EE*np.eye(2*NM) - H - Sigma1 -
      Sigma2 - SigmaB);
  SigmaBnew = DS*(SZ@(GR)@SZ + SX@(GR)@SX +
      SY@(GR)@SY) + DM*(S1*GR) \
  + DP*(S11*GR);
  error = np.sum(np.abs(SigmaBnew - SigmaB)) \
  /np.sum(np.abs(SigmaBnew + SigmaB + 1e-15));
  SigmaB = SigmaB + 0.85*(SigmaBnew - SigmaB);
GA = np.conj(GR.T); AA = 1j*(GR - GA);

error = 1;
while error > 1e-6:
  Gn = GR@(Gamma1*f1 + Gamma2*f2 + SigmaIn)@GA;
  SigmaInNew = DS*(SZ@(Gn)@SZ + SX@(Gn)@SX +
      SY@(Gn)@SY) + DM*(S1*Gn) \
  + DP*(S11*Gn);
  error = np.sum(np.abs(SigmaInNew - SigmaIn)) \
  /np.sum(np.abs(SigmaInNew + SigmaIn + 1e-15));
  SigmaIn = SigmaIn + 0.85*(SigmaInNew - SigmaIn);


denom = np.sum(np.reshape(np.diag(AA@SI),(NM,2)),axis =
      1);
charge =
      np.real(np.sum(np.reshape(np.diag(SI@Gn),(NM,2)),axis
      = 1)/denom)
spin_x =
      np.real(np.sum(np.reshape(np.diag(SX@Gn),(NM,2)),axis
      = 1)/denom)
spin_y =
      np.real(np.sum(np.reshape(np.diag(SY@Gn),(NM,2)),axis
      = 1)/denom)
spin_z =
      np.real(np.sum(np.reshape(np.diag(SZ@Gn),(NM,2)),axis
      = 1)/denom)


coef = np.polyfit(np.arange(0,NM,1),charge,1);
      poly1d_fn = np.poly1d(coef);
X = np.arange(0,NM,1); Fclass = poly1d_fn(X);
XFull = np.append(np.arange(-10,0,1), np.append
(-0.001,X))
XFull = np.append(XFull,
      np.append(200.001,np.arange(201,211,1)))
FclassFull = np.append(np.ones(11), np.append(Fclass
      ,np.zeros(11)))

plt.plot(X,charge, label='NEGF: charge', linewidth=1.5,
      alpha=0.9, color=(0.92157,0.384366,0.207899))
plt.plot(XFull, FclassFull,
      '--k', label=' semiclassical ',linewidth=1.5)
plt.plot(X,spin_z, label='NEGF: z-spin', linewidth=1.5,
      color=(0.560784,0.690196,0.196218))
plt.plot(X,spin_x, label='NEGF: x-spin', linewidth=1.5,
      color=(0.368627,0.505882,0.709803))
plt.plot(X,spin_y, label='NEGF: y-spin', linewidth=1.5,
      color=(1,0,0))
plt.xticks(fontsize=10); plt.yticks(fontsize=10);
      plt.xlim(-20,240)
plt.ylim(-0.45,1.1); plt.xlabel('x',fontdict=fontPlan);
plt.ylabel('f',fontdict=fontPlan)
plt.legend(frameon=False,fontsize = 8, loc = 'best');
      plt.show()
```

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Tight-Binding Models, Their Applications to Device Modeling, and Deployment to a Global Community

45

Gerhard Klimeck and Timothy Boykin

Contents

45.1 Nanodevice Characteristics . . . 1602
45.2 Nanodevice Modeling Approaches . . . 1604
45.3 Empirical Tight-Binding Method . . . 1605
45.3.1 Bases for the Hamiltonian . . . 1605
45.3.2 Parameter Fitting . . . 1607
45.3.3 Strain . . . 1607
45.3.4 Consequences of Discreteness and Incompleteness . . . 1608
45.3.5 Effective-Mass Formula . . . 1609
45.3.6 Localized-Orbital Representations . . . 1609
45.3.7 Electromagnetic Coupling Hamiltonian . . . 1609
45.4 Interfaces and Transport . . . 1610
45.4.1 Complex Bands . . . 1610
45.4.2 Transmission Calculations with Transfer Matrices: Numerical Stability . . . 1612
45.4.3 Direct Transmission Methods . . . 1612
45.4.4 DFT-TB and Nanodevice Modeling . . . 1614
45.5 Transport with Green Functions . . . 1614
45.6 Large-Scale Numerical Aspects . . . 1615
45.6.1 Hamiltonian Matrix Structures and Scaling for Closed Systems . . . 1615
45.6.2 Scaling Issues with Open Boundary Conditions . . . 1616
45.6.3 Quantum Transport: Parallel Computing Scaling . . . 1618
45.6.4 Surface Passivation . . . 1618
45.7 Applications . . . 1620
45.7.1 Quantum Dots: Closed Systems . . . 1620
45.7.2 Nanowire Electronic Structure: Quasi-Periodic in 1D and Closed Systems in 2D . . . 1620
45.7.3 Ballistic Transport from Nanowire Dispersions with the Top-of-the-Barrier Model . . . 1622
45.7.4 Full Quantum Transport in "Long" 15 nm Nanowires: 3D Representation . . . 1623
45.7.5 Full Quantum Transport Versus an Analytical Model in "Long" 15-nm Nanowires . . . 1626
45.7.6 Full Quantum Transport in Short 5-nm Nanowires: 3D Representation . . . 1627
45.7.7 Convergence Issues in High-Bias Coherent Transport Simulations . . . 1629
45.7.8 Short Channel Devices: A New Design Paradigm with New Requirements . . . 1632
45.8 Beyond Device Physics Advancements: Reaching the World . . . 1633
45.9 Conclusions . . . 1634
References . . . 1636

Abstract

Tight-binding has become the state-of-the-art for realistically sized nanoscale device modeling. It has been implemented by multiple advanced device modeling research groups in conjunction with multiple quantum transport methodologies. Industry has begun to adopt some of the advanced codes and is beginning to implement company internal versions. Commercial software vendors are adopting the methodologies and are beginning to deploy the approaches into their commercial TCAD products. Intense software development combining tight-binding with the non-equilibrium Green's function (NEGF) approach and quantum transmitting boundary method (QTBM) for quantum transport began in 1994 at Texas Instruments. Acceptance of NEGF and tight-binding began with wider adoption in about 2004. The past 25 years have resulted in many model advancements, numerical technology development, and physics exploration that is by far too large to be covered here comprehensively. We start by setting forth the requirements for realistic modeling of extended

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nanoscale devices (Sects. 45.1 and 45.2), which include a full quantum mechanical treatment, atomistic interface treatments, atomistic representations of crystal symmetries, polarization, strain, and bond directions, and embedding into macroscopic fields such as electromagnetic potentials and long-range strain. We then proceed to describe the essential definitions and features for empirical tight-binding (Sect. 45.3). Sections 45.4, 45.5, and 45.6 address numerical issues of tight-binding in terms of transfer matrices, Green's functions, and parallel scaling. Section 45.7 is dedicated to several applications around quantum dots and nanowires. We highlight million-atom quantum dot simulations and focus on carrier transport though silicon nanowires. We demonstrate how effective masses and bandgaps become design parameters at the nanoscale, how heavy masses are desirable for end-of-roadmap transistors, and how coherent transport assumptions break down. The nanowire simulations can be duplicated by everyone on nanoHUB.org. Section 45.8 highlights the widespread use of tight-binding within nanoHUB applications. Section 45.9 concludes this chapter.

Keywords

Tight binding · Transport · NEGF · Quantum transport · Non equilibrium green functions · Quantum dot · Nanowire · Bandstructure · Effective mass · NanoHUB · Education

45.1 Nanodevice Characteristics

Nanodevices by definition have extremely small active regions, so small that the number of atoms is, as a practical matter, countable. The small size has consequences for nanodevice physics; thus, these devices operate far differently than traditional semiconductor devices. The most important aspects of nanodevice physics that follow from their small size are: (1) length scales smaller than the electron wavelength; (2) a much higher surface-area-to-volume ratio, necessitating detailed surface modeling; (3) the importance of crystal orientation, rendering continuum models as invalid; (4) the interaction of long-range Coulomb potentials and strain fields with short-range quantum confinement. These physical consequences of the exceptionally small nanodevice size determine the requirements for modeling nanodevices.

Prototypical nanodevices, listed roughly in order of historical technical developments, are the resonant tunneling diode (RTD), quantum dots (QDs), and modern nanoFETs. The RTD consists of 1D vertically stacked, nanoscaled layers and can be considered the first room temperature quantum device geared up for electronic circuits. The RTD has, however, never found widespread technical adoption owing to a variety of technical issues. Although no longer really technically relevant, RTDs offer a wonderful utility to study and understand the intricacies of quantum transport in simple 1D geometries that become even more complicated in 3D. QDs confine electrons in 3D to nanoscale dimensions, are sometimes called artificial atoms, and they have found utility in optical applications. Because of the 3D confinement, they offer an extraordinarily clear view of the interplay between geometry and band-structure effects on optical interactions in these artificial atoms. Nano-scaled field effect transistors (nanoFETs) are ubiquitous and literally in everyone's pocket inside modern smart phones, and certainly in our laptops and notebooks. Understanding and optimizing carrier transport in such highly sophisticated 3D geometries is complex and still undergoing extensive research and development. We next briefly summarize the dimensions of these three prototypical devices.

The central part of a typical RTD heterostructure consists of two barriers measuring 3–5 nm thick surrounding a quantum well measuring 3–5 nm thick. The material system is typically GaAs/AlGaAs or InGaAs/InAlAs for the well/barrier. The central region of the RTD is typically undoped and surrounded by 10–30 nm of undoped spacer layers to reduce ionized dopant scattering near the central quantum device. This undoped region is surrounded by heavily, degenerately doped regions, so that under forward (reverse) bias electron reservoirs form adjacent to the emitter (collector) barriers. These long, heavily doped regions eventually terminate in quasi-ohmic metal contacts. The overall semiconductor device that needs to be modeled for quantitative agreement with experiment is typically 100–200 nm long in the growth direction. This length represents a surprisingly small atomic count: 8 atoms in one dimension roughly occupy 1 nm in length. Thus, a device measuring 128 nm long corresponds to a one-dimensional string of around 1000 atoms. For an RTD, the most critical consequences of small size manifest as:

1. Electron confinement to a 5 nm quantum well is clearly significantly smaller than the phase coherence length of about 50 nm for typical GaAs or InGaAs at room temperature [1].
2. The cross section of the RTD is typically defined by mesas that are of the order of 1–100 μm and therefore effectively infinite. The mesa surface is designed to play no role. The heterostructure, however, needs to be treated in atomistic detail and the surfaces as such define the device.
3. Typical RTDs have been grown in III–V material systems in the [100] direction. Substrate orientation has not played a very critical role in these typical electron devices, but does play a role in understanding hole transport, owing to the anisotropy of the valence bands.

The long-range effects of the electrostatic potentials in the semiconductor do, however, play a critical role, and a multi-scale approach to the modeling of the central 15-nm-long RTD connected to 100-nm-long semiconductor regions is critical.

In self-assembled QDs, the dot materials provide the confinement. These QDs are typically of the size of 10–30 nm in the lateral dimension and around 5–10 nm in height. These dots are typically embedded in a buffer material that confines the electrons to the QDs and passivates any open surfaces. A typical QD/buffer/substrate material system is InGaAs/InAlAs/GaAs. The typically used Stranski–Krastanov growth mode [2] ensures that the overall structure is virtually defect free, even though complex 3D geometries in the form of (capped) pyramids or domes are formed. QDs can also be realized via electrostatic confinement. This class of QD typically consists of a 1D heterostructure that confines electrons in one dimension and electrostatic 2D gates that confine electrons in the lateral dimensions. This 2D lateral confinement is limited in its down-scaling by lithography and processing technology and is typically larger than the self-assembled QDs. Typical material systems are the III–V and column IV semiconductor families. Yet another structurally different QD is one formed by an individual impurity such as P embedded in Si.

Typical self-assembled QDs have 50,000–300,000 atoms. For example, typical dome-shaped QDs have dimensions of $5 \times 30 \times 30$ nm^3 corresponding to roughly 200,000 atoms. The electron and hole wavefunction and the eigenstates are not completely confined to just the central QD but leak out, or "feel" the buffer layers. The typical electronic structure domain size is around 1–4 million atoms and the strain domain must be even larger, as discussed further below. Electron states in a single P impurity have a very shallow binding energy below the conduction band and the wavefunction spreads out to a space of $30 \times 30 \times 30$ nm^3 corresponding to about 1.7 million atoms. These total atom numbers start to be large, but are still computationally feasible. Typically, these geometries have one dimension that is significantly smaller than the other two – generally the growth direction and electron are confined to less than 5 nm, making the geometry look similar to an RTD in that aspect. The physical consequences of the small QD size are:

1. Electron confinement of 5–30 nm is of the order of the electron wavelength in typical semiconductors and this length scale is smaller than typical decoherence lengths, even at room temperature. Modeling therefore requires a quantum mechanical treatment.
2. QDs are strongly influenced by the details of the heterostructures that confine them, and have high surface-area-to-volume ratios. The treatment of the interfaces is thus critical.
3. Crystal symmetry plays a critical role in any of the three described QDs in terms of the intricate details of optical polarization effects [3], as well as valley splitting in indirect-gap band-structure materials such as Si [4].
4. Self-assembled QDs form by differences in the lattice constants of the constituent materials and are subject to significant long-range strain. The strain can reach 20–30 nm down into the substrate and it must be managed in the design [5] of overlayer growth. Gated QDs and also gated impurity dots are embedded in long-range fields that extend tens to hundreds of nanometers. These long-range, classical fields must be coupled to the detailed central device models.

Field effect transistors (FETs) have evolved from planar to full 3D geometries. The core active material is some form of strained Si connected to SiGe contacts with sophisticated 3D gate stacks. A modern finFET looks a little bit like an old RTD (oriented vertically), except that the current flows in the plane/fin. The Si/Ge transistors are strained and subject to large electric fields. Many of the principles of operation of RTDs and QDs translate to modern finFETs. Today's commercially widespread "old" nano-FETs dating back to 2011 are 3D geometries that already have channel widths as small as 8 nm or 59 atoms and channel heights that are about 3 or 4 times larger [6–8]. The active device cross section has only around 1000 atoms. Channel lengths have been decreasing from nominally 22 nm in 2012 [6, 7] to around 7 nm in 2016 [8]. The centrally active device may be well-described by 100,000 to 1 million atoms. The physical consequences of ultra-scaling finFETs are:

1. Quantum mechanical treatment is required because the confinement within a finFET is of the order of the electron wavelength and smaller than the electron coherence length, as with an RTD.
2. Device performance is determined by interface details of the finFET or nanowire FET geometry in terms of shape and interface roughness; these effects must be included in the device model.
3. Crystal orientation has a profound effect on device performance. It has been a critical transistor device design parameter since the 90-nm transistor node [9], where Texas Instruments was able to avoid the very costly SiGe-based stressors employed by Intel [10]. A simple 45° rotation of the wafer/device provided the needed performance boost for PMOS transistors. This invention was motivated by observations derived from orientation effects in NEMO-modeled QDs. The rotated substrate approach is standard technology today, indicating the continued critical importance of crystal orientation.
4. Alternative materials beyond the traditional Si have been introduced into 3D device geometries. Intel introduced

SiGe in source/drain for strain-engineering the Si channel in 2002 [10] in their 90-nm node. The 7-nm channel transistor introduced by IBM, GLOBAL FOUNDRIES, and Samsung in 2016 features SiGe channels [8]. These new materials must be rapidly included in the modeling suite.

5. NanoFETs are strained by design [6–8, 10] to improve performance and are subject to electrostatic fields to control carrier flow. This classical long-range physics must be coupled to local, relatively small central devices.

45.2 Nanodevice Modeling Approaches

Thus, nanoscale feature size and its consequences are common across a broad range of devices: RTDs, QDs, and nanoFETs. Models for these devices must accurately take into account the quantum mechanical nature of the electrons, surface and substrate effects, and long-range Coulomb potentials and strains. *Taken together, these characteristics point to a basis that is fundamentally atomistic, localized (involving as few as possible neighbors), and transferrable.*

This conclusion to use an atomistic basis was, however, not obvious to most researchers involved with quantum device modeling over the past 30 years. The principal focus of the modeling community that studies quantum devices or nanodevices as we call them today had been on the quantum mechanical aspects of the modeling. This focus was natural, as nanostructure dimensions within the range 5–30 nm are of the length scale of the electron wavelength and significantly smaller than the coherence length. It was clear even then that only quantum mechanical models would work, but quantum mechanical models differ widely in the basis sets used for the electronic states.

At the most basic level, single-(quasi) electron models fall into one of two broad categories: (1) those that explicitly include the potential due to the atoms and (2) continuum models. Continuum models, called envelope-function or effective-mass approaches, deal with electrons (holes) in a single conduction (valence) band. Materials differences are incorporated only in terms of bandgaps and effective masses (inverse band curvatures). In these models, carriers in the conduction and valence bands are different quasiparticles. These models treat the crystalline environment as a continuum; the potential due to the atoms does not appear beyond the effective masses and energy gaps. The basis states are plane waves or decaying exponentials. In addition, these models are valid for energies only near the band edges. In a periodic crystal these models do not account for nonparabolic bands (unless they are empirically expanded ad hoc) and are useful only for wavevectors near the band extrema. The **k•p** method is a multi-band continuum approach, and has similar drawbacks (and is traditionally plagued by numerical stability issues). Chapter ▸ 45, by Baccarani and Reggiani is dedicated to the **k•p** method.

Beyond their deficiencies for periodic crystals, continuum approaches are completely unsuited to nanodevice modeling in other ways that relate to realistic device representations. They cannot model surface effects and cannot account for differences in substrate orientation, both of which are critically important. In addition, multi-band effects, such as valley splitting in Si and the Rashba and Dresselhaus effects, can only be included crudely via ad hoc specifically empirically fitted parameters. There is no predictive value in models that must use such ad hoc parameters. Effects critical to realistic device models such as atomistic interfaces and their roughness, 3D geometry effects that impose nontrivial strain fields, alloy disorder, alloy grading, and full-band representations cannot in general be included in continuum models, unless they are highly calibrated through ad hoc methods.

Although the traditional device modeling community pursues efforts that scale their large device models down toward small nano-devices, there is another community, originating in material science, that pushes their models up from a few atoms toward devices. This materials science (MS) approach has some commonality with electrical engineering (EE). At the nanometer scale, the distinction between material and device vanishes and the two approaches meet. MS brings the knowledge of the placement of atoms and the electronic ground state to the common problem. EE brings approaches to quantum transport under highly non-equilibrium conditions with the need for atomistic material resolution.

Myriad atomistic structure methods can be found in the area of material science [12]. The methods can be roughly

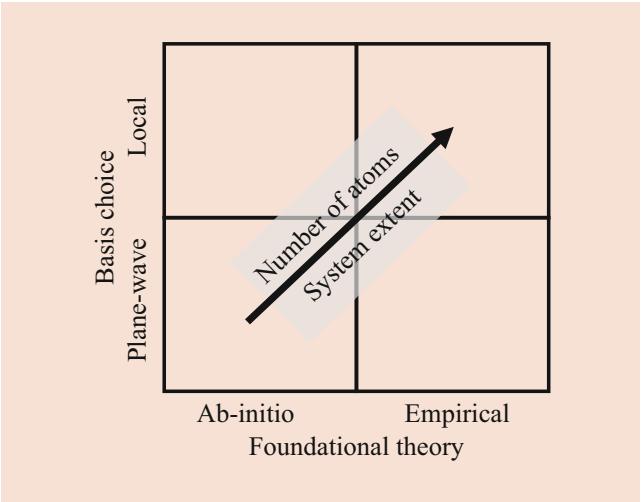

Fig. 45.1 Conceptual layout for the choice of foundational electronic structure theories and choice of basis sets. Empirical theories with localized basis sets generally scale to larger and realistically extended system sizes. Industry is now using non-equilibrium Green's function in NEMO5, utilizing empirical tight binding to design real devices [11]

distinguished into a 2 × 2 table, with one axis representing basis sets (plane waves versus local orbitals) [13, 14] and the other axis fundamental theory (ab initio versus empirical) [15, 16] (Fig. 45.1). Plane waves are appealing because they offer a quantifiable path to improve accuracy by adding more waves and are very efficient for modeling perfectly periodic crystals. However, plane waves are not well suited to modeling typical nanodevices, which are finite, with electrical contacts, and not periodic. Therefore, local orbitals are preferable, and computationally less expensive, for realistically extended device modeling. True industrial design and exploration require hundreds and thousands of simulation runs with reasonable accuracy, rather than representations of a few hero simulations.

Fundamental many-electron correlated methods based on perturbation theory [17], the quantum Monte Carlo method [18], or the GW approach [19] offer intellectual appeal, but can only predict electronic structure for very small systems (around 100 atoms). Empirical methods lose some fundamental claim to correctness but do much better in terms of incorporating correct bulk bandgaps and masses via their Hamiltonian parameters and can be scaled up to larger system sizes. Almost all ab initio and quantum chemistry codes treat closed systems close to or at equilibrium; that excludes the far-from-equilibrium irreversible electron transport needed to solve our problem. Beyond these considerations, the standards for sufficient accuracy in bulk band-structure calculations are very different in MS and EE.

Accuracy of bandgaps and masses must be significantly greater in EE than in MS. In MS ground state properties are usually the focus, and gaps off by 200 meV and masses within a factor of 2 are sufficient. In contrast, the interest in EE is on the upper valence bands and the conduction bands; gaps and band offsets need to be within about 10 meV and masses within 5%.

Forming and breaking bonds versus *stable systems:* MS is primarily concerned with the formation and establishment of the material systems and their equilibrium conditions. Realistic semiconductor devices must have stable bonds and transport characteristics are determined by the valence electrons only. Therefore, full ab initio methods are not necessary to simulate current/spin flow. Approximate methods that resolve the physics of the valence electrons with stable bonds are appropriate (and computationally feasible) for large systems.

Empirical orthogonal tight-binding (ETB) ($sp^3\ s^*$ and $sp^3\ d^5\ s^*$) is one of the oldest and conceptually simplest atomistic material descriptions available. The 'empirical' refers to fitting the Hamiltonian matrix elements to bulk band structures. ETB has proven to be scalable to very large system sizes and valid for standard semiconductor electronic structure and transport simulations under high bias current conditions [20–33]. ETB lacks an explicit basis and projection methods are needed to compute Coulomb matrix elements [34]. ETB treats the atomic positions as inputs. NEMO3D bases the positioning of the atoms on a valence force field [25, 26, 35].

The empirical tight-binding method is often questioned with regard to its accuracy of nearest-neighbor assumptions and the overall fitting process and the lack of explicit basis sets. As such many researchers prefer more fundamental approaches based on density functional theory (DFT). We reiterate here that to us the most accurate effective mass and bandgap representation that can be experimentally verified at room temperature, as well as the computational efficiency, outweigh the limitations. Typical DFT approaches that can scale up to device levels in general deliver 0K band structure with bandgaps and masses that are inaccurate.

In 2015, Intel began integrating empirical tight binding embodied in the NEMO5 implementation into their TCAD model stream. In 2019, Intel announced the integration of NEMO5 publicly at the International Electron Devices Meeting for accurate and calibrated device exploration and design [11].

45.3 Empirical Tight-Binding Method

45.3.1 Bases for the Hamiltonian

Tight-binding methods (or more specifically semi-empirical tight-binding methods) are ideally suited to nanodevice simulations. With a relatively small basis of usually no more than 20 orbitals per atom (when spin–orbit interaction is included) the bands of the device materials within the relevant energy range can be accurately reproduced throughout the Brillouin zone. Surface and interface parameters can be fit to special structures. The limited range of interactions, especially for nearest-neighbor models, allows for highly efficient device electronic structure and transport calculations. These characteristics are all highly desirable for nanodevice modeling.

The modern use of tight-binding for crystalline electronic structure calculations begins with the work of Slater and Koster [36]. The tight-binding method traditionally uses an orthonormal basis of atomic-like orbitals centered on the atoms of the crystal, with the orbitals having a limited range of interaction. Most applications are semi-empirical tight-binding, in which the orbitals do not have explicit spatial representations and are instead defined through their Hamiltonian parameters [36], although explicit, non-orthogonal, basis sets can be used, such as with the closely related extended Hückel theory [37]. In orthogonal tight-binding, there is no unique method for generating orthonormal atomic-like orbitals from true atomic orbitals, but the Löwdin orthogonalization [38] is one of the most useful. A very significant advantage of this method is that the resulting orthonormal orbitals, though no longer possessing full atomic symmetry,

nevertheless transform, as would their atomic antecedents under the symmetry operations of the crystal, and remain generally localized. For semi-empirical tight-binding models, the mere existence of such a basis is sufficient for most device modeling applications, as explicit wavefunctions are not needed most of the time.

Tight-binding bases are specified by their orbital compositions and the range of interaction. Nearest-neighbor models are best suited to nanostructures and nanodevices, which generally have a high proportion of surfaces or interfaces. In nanodevices it is often computationally preferable to use a nearest-neighbor model with a larger basis versus a smaller basis of more extended orbitals. A limited range of interactions also results in a more computationally efficient calculation. The basis set chosen must accurately reproduce the energy gaps and effective masses of all bands within the relevant energy range for the bulk materials. The earliest models for semiconductors employed an sp^3 basis (one s- and three p-orbitals per atom, doubled when the spin–orbit interaction is included), but proved unable to accurately reproduce the conduction bands. Vogl et al. [39] significantly improved conduction-band reproduction along the [100] directions by adding an excited s-like (s^*) orbital to the basis ($sp^3\ s^*$). Still, problems in the conduction band remained. Most problematic was the inability of the nearest-neighbor $sp^3\ s^*$ model to accurately reproduce the X-valley transverse effective mass. Two remedies for this deficiency were developed: (1) within the $sp^3\ s^*$ basis, extending the range of interaction to second-nearest neighbors [40]; or (2) retaining nearest-neighbor interactions with a basis including d-orbitals, the $sp^3\ d^5\ s^*$ basis proposed by Jancu et al. [41]. The nearest-neighbor $sp^3\ d^5\ s^*$ basis is usually preferred for nanodevices owing to its minimal range of interaction.

The parameters of tight-binding Hamiltonians are referred to as Slater–Koster [36] parameters and are characterized as two- and three-center integrals. The two-center integrals include only potentials centered on the two atoms of the orbitals involved in the matrix element; three-center integrals include the effects of potentials on other atoms as well. Most nanoelectronic-device, tight-binding models restrict interactions to nearest neighbors, so that the two-center approximation is justified. An example of one such matrix element in silicon or germanium is that between an s-orbital at the origin and a p_x-orbital at $\mathbf{d}$:

$$\langle s; \mathbf{0}| \hat{H} |x; \mathbf{d}\rangle = lV_{sp\sigma}. \tag{45.1}$$

In Eq. (45.1) l denotes the x-direction cosine for the vector $\mathbf{d}$. $V_{sp\sigma}$ is the Slater–Koster [35] parameter for this type of matrix element. Cyclic permutations of coordinates and direction cosines give the remaining two matrix elements for p_y- and p_z-orbitals. In compound semiconductors such as GaAs there are separate parameters for the s-orbital on the anion and the p_x-orbital on the cation ($V_{sapc\sigma}$) and vice-versa ($V_{scpa\sigma}$). The atomic locations are fixed by the crystal structure and lattice constant; the Slater–Koster parameters are determined via a fitting process.

Tight-binding basis states take different forms depending on the number of confined dimensions; in the nonconfined dimensions they obey the appropriate form of Bloch's theorem. In bulk 3D materials the basis states for the perfect crystal Hamiltonian are:

$$|\omega; l; \mathbf{k}\rangle = \frac{1}{\sqrt{N}} \sum_{j=1}^{N} \exp\left[i\mathbf{k}_j \cdot \left(\mathbf{R}_j + \mathbf{d}_l\right)\right] |\omega; \mathbf{R}_j + \mathbf{d}_l\rangle. \tag{45.2}$$

In Eq. (45.2) ω denotes the orbital type (s-, p_x-, etc., including spin where appropriate), $\mathbf{R}_j$ the location of the j-th primitive cell, $\mathbf{d}_l$ the location relative to the cell origin of the l-th atom in the primitive cell (for polyatomic primitive cells), $\mathbf{k}$ the wavevector (crystal momentum), and N the number of primitive cells. These states obey Bloch's theorem in three dimensions. Superlattice basis states are formally the same as expressed in Eq. (45.2), except that $\mathbf{R}_j$ denotes the supercell location, N the number of supercells, and $\mathbf{d}_l$ the location relative to the supercell origin of the l-th atom. (For a supercell of N_c primitive cells with N_a atoms per primitive cell, there are $N_c N_a$ different $\mathbf{d}_l$.) Basis states for a two-dimensional material such as graphene are constructed analogously, except that the wavevector and primitive cell vectors are two-dimensional. Basis states for nanowires are constructed, as are 3D superlattice states, except that there is translational symmetry in only one direction and thus only a one-dimensional wavevector.

Three-dimensional materials with confinement or broken translational symmetry in one or more dimensions require different basis states. In layered structures with only planar translational symmetry, the basis states are Bloch sums in the plane:

$$\left|\omega; l; L; \mathbf{k}_{\|}\right\rangle = \frac{1}{\sqrt{N_{\|}}} \sum_{j=1}^{N_{\|}} \exp\left[i\mathbf{k}_{\|} \cdot \left(\mathbf{R}_{j\|}(L) + \boldsymbol{d}_{l\|}\right)\right] \Big| \omega; L; \boldsymbol{R}_{j\|}(L) + \boldsymbol{d}_{l\|} \Big\rangle. \tag{45.3}$$

In Eq. (45.3) the subscript '||' denotes a vector in the plane, and L the layer index. A layer is usually defined as a grouping of one or more atomic planes so that there are only nearest-neighbor couplings between layers. Note that the bulk primitive cell origin may be offset depending on the layer index.

45.3.2 Parameter Fitting

The fitting process for three-dimensional materials begins with the perfect crystal Hamiltonian in the tight-binding basis of Eq. (45.2). Perfect 2D Hamiltonians are constructed analogously. The eigenvalues and eigenvectors of the Hamiltonian depend on the parameters and thus are used to fit them so that the relevant effective masses and energy gaps reproduce those of the bands within the relevant energy range. Until very recently, gaps and masses were the only targets used in the fitting process; the values for these targets are taken from ab initio calculations or experimental results. At high symmetry points there may be analytic formulas for some gaps and masses in terms of the parameters [40, 42–44]. These expressions are most useful for the band fitting process when the dependencies on the parameters are clear, meaning that in practice the Hamiltonian matrix $\underline{\mathbf{H}}(\mathbf{k})$ should be analytically block diagonalizable, with some of the blocks being of dimension 1 or 2. (Analytic solutions are always possible for up to quartic equations and thus the eigenvalues and eigenvectors of matrices up to 4×4, but the complicated solutions to quartic and cubic equations generally obscure parameter dependences.) Expressions for inverse effective masses (band curvatures) are possible once the Hamiltonian eigenvalues and eigenvectors are found at the $\mathbf{k}$-point of interest. The expression for the inverse effective mass is different from the standard formula found in solid-state textbooks owing to the incompleteness of the basis set [45, 46]. The issue of incompleteness and its consequences are discussed in Sects. 45.3.4, 45.3.5, 45.3.6, and 45.3.7 below.

Although analytic gap and mass formulas help in the fitting process, in practice, iterative computer algorithms are almost always used. Computational optimization is needed when fitting mass and gap targets that are not at high-symmetry points. Klimeck et al. [47] introduced genetic algorithms for global optimization in a very high dimensional space to the tight-binding parameter fitting problem. This genetic algorithm employs user-assigned weights for targets and from them computes a fitness function in each step. Then, random mutations of the current parameter set are generated and the one with the best overall fitness is preserved as the parent for the next mutation step. The algorithm terminates when a solution with acceptable fitness is found. Although fitting algorithms such as this are essential for parameter determination, there remains the possibility that the best solution might not be found. Sometimes very different parameter sets can reproduce the targeted gaps and masses to nearly the same accuracy. However, they may well differ in their wavefunction quality. The analytical expressions for bandgaps and effective masses discussed above are extremely helpful as they serve as additional constraints to the problem solution and guide the high-dimensional fitting problem to convergence.

To address the fundamental wavefunction variations for different parameter sets a new fitting method has been developed that includes matches to ab initio wavefunctions in addition to gaps and masses in the fitting process. Tan et al. [48–50] use DFT wavefunctions to construct real-space tight-binding wavefunctions. A low-rank approximate DFT Hamiltonian is then transformed into the tight-binding basis using the transformation between the DFT and tight-binding wavefunctions. The tight-binding Hamiltonian is iteratively improved by comparing gaps, masses, and wavefunctions at high-symmetry points with DFT results. Including wavefunction fitting removes much of the uncertainty about whether the true best fit has been found.

The work of Tan et al. [49, 50] on mapping tight-binding parameters from DFT calculations also helps to answer the question of the extent of interactions needed (nearest neighbor, second-nearest neighbor, etc.) to accurately reproduce semiconductor band structures. Heuristically, it has been observed that similar accuracy can be achieved with smaller basis sets and more distant neighbor interactions or larger basis sets and shorter range interactions. For example, comparable accuracy in common semiconductors (Si, Ge, and III–Vs) can be achieved with either the 2NN $sp^3\ s^*$ model or the NN $sp^3\ d^5\ s^*$ model. Tan et al. [49, 50] show that the DFT-mapped NN $sp^3\ d^5\ s^*$ model can achieve excellent accuracy for common semiconductor materials. The fact that the parameters in their model are derived from DFT calculations, including, critically, DFT wavefunctions, supports the utility and applicability of the NN $sp^3\ d^5\ s^*$ model.

45.3.3 Strain

Strains displace the atoms of a crystal from their ideal positions and can be either regular or irregular. Regular strains affect all primitive cells identically, and occur in strained layer superlattices (GaAs/InAs, Si/Ge, etc.) or when external strains are applied. Irregular strains affect differing primitive cells differently and occur in random alloys or in the presence of defects, for example, as well as in geometry variations in two- or three dimensions. Both types affect the electronic structure of the material by altering the Hamiltonian in terms of both its potentials and its basis states. Changes appear in both the neighboring-atom and onsite Hamiltonian matrix elements. The most obvious change is in the relative positions (distances and orientations) of the potentials centered on the two atoms involved in a two-center integral. The second, less obvious change, is to the orbitals themselves. Recall that orthonormal basis sets are generally constructed from non-orthogonal bases using Löwdin's procedure [38]. In the Löwdin method, an orthonormal set $\{|\varphi_j\rangle; j = 1, \ldots, N\}$ is constructed from a non-orthogonal set (e.g., atomic orbitals)

$\{|\eta_j\rangle; j = 1, \ldots, N\}$ using the square root of the overlap matrix:

$$|\varphi_j\rangle = \sum_{m=1}^{N} \left[\underline{\mathbf{S}}^{-1/2}\right]_{m,j} |\eta_m\rangle\,, \quad [\underline{\mathbf{S}}]_{m,n} = \langle\eta_m|\eta_n\rangle\,. \tag{45.4}$$

Displacing the atoms, and thus the non-orthogonal orbitals centered on them, changes the overlap matrix elements and thus the orthonormal basis of the Hamiltonian.

Both types of changes are incorporated into the neighboring-atom matrix elements (generally two-center integrals) via a power-law scaling relation. This scaling is referred to as the Generalized Harrison's Law. Harrison [43] fit the bands of a simple cubic crystal to the free-electron bands at $k = 0$ and $k = \pi/a$, which requires the s-s and s-p matrix elements to vary as d^{-2}, where d is the nearest-neighbor distance. The generalization allows for the power to vary with the bond type ($ss\sigma$, $sp\sigma$, $pd\pi$, etc.):

$$V_{\mathrm{ab}\gamma}(d) = V^{(0)}_{\mathrm{ab}\gamma}\left(\frac{d_0}{d}\right)^{\eta_{\mathrm{ab}\gamma}}. \tag{45.5}$$

In Eq. (45.5) $V^{(0)}_{\mathrm{ab}\gamma}$ is the ideal-crystal, two-center integral between orbitals a, and b (s, p, d, etc.) with bond type γ (σ, π, δ, etc.); d_0 is the ideal distance between the atoms and d the actual distance; and $\eta_{\mathrm{ab}\gamma}$ the scaling exponent (nominally 2). The exponents are fit in a process similar to the two-center integrals in order to reproduce the gaps and masses as functions of strain, using as targets either ab initio calculations or experimental results.

The issue of scaling the onsite matrix elements under strain is somewhat subtler. Although it is tempting to think of the onsite parameters as being atomic orbital energies, Eq. (45.4) and consideration of the crystalline environment make it clear that this cannot be the case. From Eq. (45.4) it is clear that the onsite terms are affected by the Löwdin orthogonalization [38]. These terms are likewise affected by the neighboring atom potentials. In a free atom there is no p_x-p_y Hamiltonian matrix element owing to the spherical symmetry of the atomic potential. In diamond or zincblende this term vanishes as well owing to symmetry: nearest neighbors are located at $(a/4)(1,1,1)$, $(a/4)(-1,-1,1)$, $(a/4)(1,-1,-1)$, $(a/4)(-1,1,-1)$. Under uniaxial [110] strain, however, the first two ($z > 0$) neighbors are at one common distance from the central atom whereas the second two ($z < 0$) are at a different common distance, leading to an incomplete cancellation of their effects. As a result, onsite matrix elements absent from the ideal crystal Hamiltonian can appear under some strain conditions.

Within the context of the $sp^3\,d^5\,s^*$ basis [41] four different approaches to the strain treatment of the onsite matrix elements have been proposed. Jancu et al. [41] scale only the onsite d parameters for regular strains, the only new parameter being the d-state shear parameter. In order to treat randomly varying strains, such as one finds in a random alloy, adjustments computed separately for each neighboring atom, and summed over neighbors to find the complete shift, have been proposed [50–53]. The implementation of each of these methods is sufficiently involved that the reader is referred to the original references for the details. Briefly, however, the differences between them are that Niquet et al. [51] include both neighboring atom potential and Löwdin renormalization effects into a pair of parameters for each type of onsite matrix element. These adjustments are relatively simple to calculate, but because both effects are bundled together into each matrix element, establishing physically meaningful limits on the strain parameters is difficult. Boykin et al. first included Löwdin renormalization [38] shifts only [52], and then added nearest-neighbor potential effects (for p- and d-orbitals only) later [53]. Although this approach is more complicated to implement, it does have the advantage of allowing physical limits on the parameters arising from the two separate effects to be determined [52, 53]. The most recent approach is the DFT-mapped method of Tan et al. [50], which reduces uncertainty in the parameter values. This method takes into account changes in neighboring atom potentials, but has the largest number of strain parameters of the methods discussed here.

45.3.4 Consequences of Discreteness and Incompleteness

Perhaps the least well understood and least appreciated properties of tight-binding models are their discreteness and incompleteness. Actually, any finite model is incomplete, and any model implemented on a computer is discrete. Even large-basis models, such as the linearized augmented plane wave method, are incomplete and the incompleteness must be properly taken into account [54]. The consequence of incompleteness is that many familiar relations from continuous quantum mechanics must be modified, because steps in their derivation assumed a complete basis. Not surprisingly, incompleteness is most readily seen in connection with the matrix elements of the momentum operator, which has a real-space representation: $\hat{p}^{(x)} = -i\hbar\partial/\partial x$, etc. Faithful representation of the derivative operator in a real-space basis implies an infinitesimal spatial resolution, which is clearly impossible in any finite basis. The momentum operator can only be exactly represented (for the included states) in a purely plane-wave basis, because plane waves are momentum eigenfunctions. Beyond this difficulty, commutators of the momentum operator are problematic in any finite basis. Graf and Vogl [45] point out that in any finite basis the position and momentum matrices no longer satisfy the commutator: $\left[\underline{\mathbf{r}}^{(\alpha)}, \underline{\mathbf{p}}^{(\beta)}\right] \neq i\hbar\underline{\boldsymbol{\delta}}_{\alpha,\beta}$. The reason is that for

any finite matrices $\underline{\mathbf{M}}$, $\underline{\mathbf{N}}$, trace $\left(\underline{\mathbf{MN}}\right)$ = trace $\left(\underline{\mathbf{NM}}\right)$, so that the trace of the commutator is zero. Because these operators and commutators appear in many different formulas, the consequences of incompleteness are far-reaching.

45.3.5 Effective-Mass Formula

The effective mass formula found in nearly all solid-state physics texts is incorrect and must be modified in an incomplete basis, because the leading term comes from the position–momentum commutator. Graf and Vogl [45] and Boykin [46] derive the correct formula (Boykin [46] also includes modifications for degenerate bands), which agrees exactly with the effective mass as calculated from the band curvature $\partial^2 E_n(\mathbf{k})/\partial k^{(\alpha)}\,\partial k^{(\beta)}$. The inverse effective mass tensor for a nondegenerate band state $|n,\mathbf{k}\rangle$ is [45, 46]:

$$\left[\frac{1}{m^*}(\mathbf{k})\right]_{\alpha,\beta} = \frac{-i}{m_0\hbar}\langle n,\mathbf{k}|\left[\hat{r}^{(\alpha)},\hat{p}^{(\beta)}\right]|n,\mathbf{k}\rangle + \frac{1}{m_0^2}\sum_{j\neq n}\frac{\langle n,\mathbf{k}|\hat{p}^{(\alpha)}|j,\mathbf{k}\rangle\langle j,\mathbf{k}|\hat{p}^{(\beta)}|n,\mathbf{k}\rangle + \langle n,\mathbf{k}|\hat{p}^{(\beta)}|j,\mathbf{k}\rangle\langle j,\mathbf{k}|\hat{p}^{(\alpha)}|n,\mathbf{k}\rangle}{E_n(\mathbf{k}) - E_j(\mathbf{k})} \tag{45.6}$$

In Eq. (45.6) the sum runs over all states j in the finite basis. In terms of the Hamiltonian matrix, these matrices and commutators are [46]:

$$\frac{\hbar}{m_0}\underline{\mathbf{p}}^{(\alpha)}(\mathbf{k}) = \frac{\partial\underline{\mathbf{H}}(\mathbf{k})}{\partial k^{(\alpha)}}, \quad \underline{\mathbf{p}}^{(\alpha)}(\mathbf{k}) = \frac{m_0}{i\hbar}\left[\underline{\mathbf{r}}^{(\alpha)},\underline{\mathbf{H}}\right](\mathbf{k}), \tag{45.7}$$

$$\frac{-i\hbar}{m_0}\left[\underline{\mathbf{r}}^{(\alpha)},\underline{\mathbf{p}}^{(\beta)}\right](\mathbf{k}) = \frac{\partial^2\underline{\mathbf{H}}(\mathbf{k})}{\partial k^{(\alpha)}\partial k^{(\beta)}}. \tag{45.8}$$

Note in particular Eq. (45.8), which is not (up to constants) $\underline{\boldsymbol{\delta}}_{\alpha,\beta}$. We remark that so long as the spin-orbit Hamiltonian $\underline{\mathbf{H}}_{so}$ has only same-atom couplings, as in Chadi's prescription [55], and the position operator is diagonal (see Sect. 45.3.7 below), $\left[\underline{\mathbf{r}}^{(\alpha)},\underline{\mathbf{H}}_{so}\right] = \underline{\mathbf{0}}$. As a result, the momentum and velocity matrices are proportional.

45.3.6 Localized-Orbital Representations

One cannot simply calculate localized-orbital position and momentum matrix elements as one does in atomic physics. The existence of discrete translational symmetry in an ideal crystal imposes a discrete real-space grid, which puts constraints on the position and momentum matrices. First, these matrices must be consistent with the band velocities and effective masses of the tight-binding model itself, see Eqs. (45.6–45.8) above. Calculating momentum matrix elements using the continuous-space momentum operator fails the consistency test [56]. Second, the formalism must be gauge invariant, which in an arbitrary localized-orbital basis requires commuting position matrices [56]. In an arbitrary basis the only guaranteed gauge-invariant definition of the position matrix is diagonal:

$$\langle\gamma;\mathbf{R}_m+\mathbf{d}_n|\,\hat{r}^{(\alpha)}\,|\omega;\mathbf{R}_j+\mathbf{d}_l\rangle = \delta_{\gamma,\omega}\delta_{m,j}\delta_{n,l}\left(\mathbf{R}_j^{(\alpha)}+\mathbf{d}_l^{(\alpha)}\right) \tag{45.9}$$

These position matrices commute [45, 56, 57] and, from the states Eq. (45.2), also satisfy the consistency tests, Eqs. (45.6–45.8).

The momentum matrices must therefore be calculated using the position operator:

$$\hat{p}^{(\alpha)} = \frac{m_0}{i\hbar}\left[\hat{r}^{(\alpha)},\hat{H}\right] \tag{45.10}$$

$$\begin{aligned}&\langle\gamma;\mathbf{R}_m+\mathbf{d}_n|\,\hat{p}^{(\alpha)}\,|\omega;\mathbf{R}_j+\mathbf{d}_l\rangle\\ &\quad= \frac{-im_0}{\hbar}\left(\mathbf{R}_m^{(\alpha)}+\mathbf{d}_n^{(\alpha)}-\mathbf{R}_j^{(\alpha)}-\mathbf{d}_l^{(\alpha)}\right)\\ &\quad\langle\gamma;\mathbf{R}_m+\mathbf{d}_n|\,\hat{H}\,|\omega;\mathbf{R}_j+\mathbf{d}_l\rangle.\end{aligned} \tag{45.11}$$

Using the diagonal form of the position operator therefore results in no same-atom position or momentum matrix elements (in an orthonormal basis). Same-atom, different-orbital position matrix elements generally result in noncommuting position matrices, thus violating gauge invariance: the only exception is for unusual, restricted bases. Foreman [58] has shown that gauge invariance with intra-atomic position matrix elements requires unconventional basis choices, for example, in cubic crystals: s^1, $s^1\,p^3\,d^2$, $s^1\,p^3\,d^3\,f^1$, or $s^1\,p^3\,d^5\,f^3$. Conventional bases, such as sp^3, $sp^3\,s^*$, and $s^1\,p^3\,d^5\,s^*$ are ruled out. Therefore, in an arbitrary basis, gauge invariance and consistency are only guaranteed with diagonal position matrices.

45.3.7 Electromagnetic Coupling Hamiltonian

In continuous quantum mechanics the vector potential couples into the Hamiltonian via the momentum operator. Because the discrete, finite-basis expression should become the continuous-space expression in the limit of a complete basis, the vector potential should enter with the momentum operator in tight-binding as well. A further requirement is that the expression be gauge invariant. The matrix elements of the tight-binding Hamiltonian with a vector potential are given by the Peierls substitution [59], which weights the

Hamiltonian matrix elements with a phase (called the Peierls phase) [45, 56, 57]:

$$\left\langle \gamma; \mathbf{R}_{m,n} \right| \hat{H}^{(\mathbf{A})} \left| \omega; \mathbf{R}_{j,l} \right\rangle = \exp\left[-\frac{ie}{\hbar} \int_{\mathbf{R}_{j,l}}^{\mathbf{R}_{m,n}} \mathbf{A}\left(\mathbf{s}, t\right) \cdot d\mathbf{s} \right] \left\langle \gamma; \mathbf{R}_{m,n} \right| \hat{H}^{(0)} \left| \omega; \mathbf{R}_{j,l} \right\rangle . \tag{45.12}$$

In Eq. (45.12) $\hat{H}^{(\mathbf{A})}$ $\left(\hat{H}^{(0)}\right)$ denotes the Hamiltonian with (without) vector potential $\mathbf{A}$, and $\mathbf{R}_{a,b} = \mathbf{R}_a + \mathbf{d}_b$ the position of atom b (for polyatomic unit cells) in unit cell a. Equation (45.12) is manifestly gauge invariant, but requires further justification on two points: (1) Its relationship to the minimal coupling Hamiltonian of continuous quantum mechanics, and (2) the path to be taken in the Peierls integral. Concerning the latter point, Graf and Vogl [45] propose the straight-line path connecting the two atoms. This choice is clearly the simplest and most natural, especially for nearest-neighbor models. It is also reasonable in view of the discrete nature of the model. If additionally, one uses the trapezoidal rule for the integral, which is in fact exact for linear $\mathbf{A}$ (e.g., a uniform $\mathbf{B}$-field as in $\mathbf{A} = (\mathbf{B}_0 \times \mathbf{r})/2$), the result bears a striking resemblance to the minimal-coupling Hamiltonian:

$$\begin{aligned} &\left\langle \gamma; \mathbf{R}_{m,n} \right| \hat{H}^{(\mathbf{A})} \left| \omega; \mathbf{R}_{j,l} \right\rangle \\ &\quad = \exp\left[-\frac{ie}{2\hbar} \left(\mathbf{R}_{m,n} - \mathbf{R}_{j,l}\right) \left[\mathbf{A}\left(\mathbf{R}_{m,n}, t\right) + \mathbf{A}\left(\mathbf{R}_{j,l}, t\right) \right] \right] \\ &\quad \left\langle \gamma; \mathbf{R}_{m,n} \right| \hat{H}^{(0)} \left| \omega; \mathbf{R}_{j,l} \right\rangle \end{aligned} \tag{45.13}$$

In particular, note that an expansion of the exponential to first order in $\mathbf{A}$ gives for the first-order term the average of the momentum matrix element, Eq. (45.11), times $\mathbf{A}$ evaluated on the two atomic sites. The full power series for the exponential gives matrix elements of multiple commutators of the position and Hamiltonian. Thus, there are solid physical reasons for favoring the straight-line path.

More formally, Boykin [60] has shown that in the continuous $\{|\mathbf{r}\rangle\}$ basis, the matrix elements

$$\left\langle \mathbf{r} \right| \hat{H}^{(\mathbf{A})} \left| \mathbf{r}' \right\rangle = \exp\left[-\frac{ie}{\hbar} \int_{\mathbf{r}'}^{\mathbf{r}} \mathbf{A}\left(\mathbf{s}, t\right) \cdot d\mathbf{s} \right] \left\langle \mathbf{r} \right| \hat{H}^{(0)} \left| \mathbf{r}' \right\rangle \tag{45.14}$$

result in the usual minimal-coupling Schrödinger equation:

$$\left\langle \mathbf{r} \right| \hat{H}^{(\mathbf{A})} \left| \psi(t) \right\rangle = \frac{1}{2m} \left[\hat{\mathbf{p}} + e\mathbf{A}\left(\mathbf{r}, t\right) \right]^2 \psi\left(\mathbf{r}, t\right) . \tag{45.15}$$

Note the analogy of Eqs. (45.14) to (45.12). In Eq. (45.14) it is critical to realize that the continuous-space basis matrix elements are generalized functions. In the continuous $\{|\mathbf{r}\rangle\}$ basis the path is immaterial, as one might expect. In addition, Boykin et al. [57] derive Eq. (45.12) in a different way. Using a multiple-commutator expansion and diagonal position operators (Eq. 45.9), they obtain an infinite series in terms of the momentum operator and the vector potential. In a complete basis the series terminates at second order in the vector potential, resulting in the usual minimal coupling Hamiltonian. Furthermore, they show that when the straight-line path between the two atoms is used in the Peierls integral in Eq. (45.12), the multiple commutator series and the Peierls substitution give the same matrix elements. Thus, when one uses diagonal (i.e., commuting) position matrices and takes into account the incomplete basis, the vector potential is accommodated by weighting the Hamiltonian matrix elements by the Peierls phase.

External, scalar potentials are handled consistently with the diagonal form of the position matrices, Eq. (45.9). The applied scalar potential, $U(\mathbf{r})$, can be expanded in a Taylor series in the position operators, so that its matrix elements are:

$$\left\langle \gamma; \mathbf{R}_{m,n} \right| \hat{U}\left(\mathbf{r}\right) \left| \omega; \mathbf{R}_{j,l} \right\rangle = \delta_{\gamma,\omega} \delta_{m,j} \delta_{n,l} U\left(\mathbf{R}_{j,l}\right) . \tag{45.16}$$

This prescription for the scalar potential also satisfies gauge invariance [45, 56, 57].

45.4 Interfaces and Transport

45.4.1 Complex Bands

The complex bands are the evanescent surface/interface modes of a crystal [61–67]; they come in growing/decaying pairs. These surface/interface states are used in constructing the open boundary conditions of planar devices, such as nanowire transistors, or resonant tunneling diodes (RTDs). They also determine the confinement, as with barriers in RTDs or the cladding of a QD. In RTDs, for example, the confinement determines the sharpness of the resonances and thus greatly affects the current-voltage characteristics. In a QD it determines the wavefunction leakage out of the dot. The complex bands are found by imposing periodic boundary conditions only in the plane of the surface/interface, using basis states of Eq. (45.3); one or more atomic planes are grouped together into layers, so that there are only nearest-layer couplings. The resulting Hamiltonian sub-matrices are defined as:

$$\left[\underline{\mathbf{H}}_{(L',L)} \right]_{(\omega' l', \omega l)} = \left\langle \omega'; l'; L'; \boldsymbol{k}_{\parallel} \left| \hat{H} \right| \omega; l; L; \boldsymbol{k}_{\parallel} \right\rangle . \tag{45.17}$$

The total state is:

$$\left|\psi\left(\boldsymbol{k}_{\parallel}\right)\right\rangle = \sum\nolimits_{\omega',l',L'} C_{L'}^{\omega',l'} \left|\omega';l';L';\boldsymbol{k}_{\parallel}\right\rangle. \tag{45.18}$$

The Schrödinger equation therefore has rows:

$$\underline{\mathbf{H}}_{(L-1,L)}^{\dagger}\mathbf{C}_{L-1} + \left[\underline{\mathbf{H}}_{(L,L)} - \underline{\mathbf{1}}E\right]\mathbf{C}_{L} + \underline{\mathbf{H}}_{(L,L+1)}\mathbf{C}_{L+1} = \underline{\mathbf{0}}. \tag{45.19}$$

In Eq. (45.19) $\mathbf{C}_L$ is the vector of all coefficients for layer L; in bulk, $\underline{\mathbf{H}}_{(L-1,L)} = \underline{\mathbf{H}}_{(L,L+1)}$.

The propagation equation is found by introducing $\mathbf{C}_L = \mathbf{C}_L$ along with Eq. (45.19):

$$\begin{bmatrix} \underline{\mathbf{H}}_{(L,L+1)} & \underline{\mathbf{0}} \\ \underline{\mathbf{0}} & \underline{\mathbf{1}} \end{bmatrix} \begin{bmatrix} \mathbf{C}_{L+1} \\ \mathbf{C}_{L} \end{bmatrix} = \begin{bmatrix} -\left(\underline{\mathbf{H}}_{(L,L)} - \underline{\mathbf{1}}E\right) & -\underline{\mathbf{H}}_{(L,L+1)}^{\dagger} \\ \underline{\mathbf{1}} & \underline{\mathbf{0}} \end{bmatrix} \begin{bmatrix} \mathbf{C}_{L} \\ \mathbf{C}_{L-1} \end{bmatrix}. \tag{45.20}$$

The traditional way of solving Eq. (45.20) is to multiply by the inverse of the left-hand matrix to generate a transfer matrix:

$$\underline{\mathbf{M}}_{(L+1,L)} = \begin{bmatrix} \underline{\mathbf{H}}_{(L,L+1)} & \underline{\mathbf{0}} \\ \underline{\mathbf{0}} & \underline{\mathbf{1}} \end{bmatrix}^{-1} \begin{bmatrix} -\left(\underline{\mathbf{H}}_{(L,L)} - \underline{\mathbf{1}}E\right) & -\underline{\mathbf{H}}_{(L,L+1)}^{\dagger} \\ \underline{\mathbf{1}} & \underline{\mathbf{0}} \end{bmatrix};$$
$$\begin{bmatrix} \mathbf{C}_{L+1} \\ \mathbf{C}_{L} \end{bmatrix} = \underline{\mathbf{M}}_{(L+1,L)} \begin{bmatrix} \mathbf{C}_{L} \\ \mathbf{C}_{L-1} \end{bmatrix}. \tag{45.21}$$

Setting $\mathbf{C}_{L+1} = \lambda_{+}\mathbf{C}_{L}$ gives an ordinary eigenvalue equation for the transfer matrix. Its eigenstates are the surface states for the crystal and they can be propagating or growing/decaying.

Although this equation is intuitively satisfying, it unfortunately has a severe problem: it might not exist. For certain parameter sets or simply values of $\boldsymbol{k}_{\parallel}$ the left- and/or right-hand matrices in Eq. (45.20) become singular and the transfer matrix does not exist [65, 66]. The alternative, and most numerically stable way of finding the surface states is to solve either the forward $\mathbf{C}_{L+1} = \lambda_{+}\mathbf{C}_{L}$ or reverse $\mathbf{C}_{L-1} = \lambda_{-}\mathbf{C}_{L}$ propagation problem as a generalized eigenproblem [65]; an ordinary eigenproblem with a shift strategy can also be used [67]. The forward generalized eigenproblem is:

$$\lambda_{+}\begin{bmatrix} \underline{\mathbf{H}}_{(L,L+1)} & \underline{\mathbf{0}} \\ \underline{\mathbf{0}} & \underline{\mathbf{1}} \end{bmatrix} \begin{bmatrix} \mathbf{C}_{L} \\ \mathbf{C}_{L-1} \end{bmatrix} = \begin{bmatrix} -\left(\underline{\mathbf{H}}_{(L,L)} - \underline{\mathbf{1}}E\right) & -\underline{\mathbf{H}}_{(L,L+1)}^{\dagger} \\ \underline{\mathbf{1}} & \underline{\mathbf{0}} \end{bmatrix} \begin{bmatrix} \mathbf{C}_{L} \\ \mathbf{C}_{L-1} \end{bmatrix} \tag{45.22}$$

The eigenvalues come in pairs $\left(\lambda_{\pm}, \lambda_{\pm}^{*}\right)$ and eigenvalues $\lambda_{\pm} \neq 0$ come in pairs $\left(\lambda_{\pm}, 1/\lambda_{\pm}^{*}\right)$; for every m-fold $\lambda_{+} = 0$, there is likewise an m-fold $\lambda_{-} = 0$ [65]. Thus, for every immediately decaying state there is an immediately growing one; for every forward-propagating state there is a reverse-propagating one. The nonzero eigenvalues $\lambda_{\pm} \neq 0$ are conveniently written as $\exp[ik_{\perp}a_{\perp}]$, where $k_{\perp}$ is the wavevector normal to the surface and is in general complex (real for Bloch states) and $a_{\perp}$ is the layer thickness. The forward or reverse generalized eigenproblem therefore yields wavevectors $k_{\perp}(E, \boldsymbol{k}_{\parallel})$.

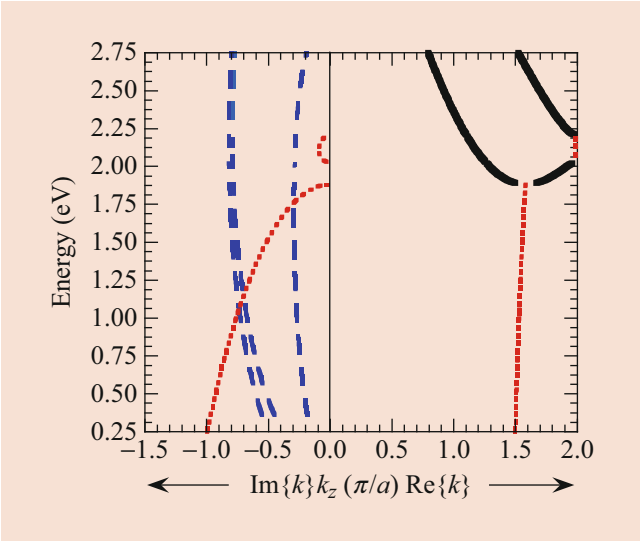

Fig. 45.2 The complex bands [65] of AlAs calculated using the parameter set of Schulman and Chang [63]. All three types of bands are present: real (solid black lines), imaginary (dashed blue lines), and complex (dotted red lines), which have wavevectors with both real and imaginary parts

An example of complex band structure is plotted in Fig. 45.2, part of the AlAs complex bands [65] for the [001] surface, calculated using the sp^3s^* parameter set given in Schulman and Chang [63]. In Fig. 45.2 *a* is the face-centered cubic conventional unit cube edge. The real bands are plotted with black solid lines; purely imaginary bands with blue dashed lines; and the real and imaginary parts of complex bands are plotted with red dotted lines. Real bands and real parts of complex bands are plotted for $k_z > 0$ only; imaginary bands and imaginary parts of complex bands are plotted for $k_z < 0$ only. The imaginary bands connect the valence band maxima (degenerate heavy/light hole and split-off hole) with conduction band minima. The lowest X-valley minimum occurs at $k_z \approx 1.5\pi/a$, so that at the Brillouin zone face the lowest conduction band has a shallow local maximum. This maximum is connected to the minimum of the next lowest band by a small complex band between around 2.0 and 2.2 eV with $\mathrm{Re}\{k_z\} \approx 2\pi/a$ (i.e., at the zone face). Another complex band begins off the X-valley minimum.

We conclude this subsection on complex bands with a brief discussion on a closely related issue: interface parameter determination. The inter-layer coupling matrices in Eq. (45.21) incorporate the interface treatment scheme. As a first step, the onsite terms of one material are uniformly

shifted relative to the other to incorporate the correct valence band offset. The interface handling for common anion or cation interfaces (e.g., GaAs/AlAs) traditionally averages the onsite parameters of the common atom and retains the nearest-neighbor couplings appropriate to the bulk materials. In the GaAs/AlAs interface example, the onsite As parameters are an average of the As onsite terms for GaAs and AlAs. The As/Ga couplings are those of GaAs and the As/Al couplings are those of AlAs. This method generally works well in practice but lacks a sound theoretical footing. To address this shortcoming, Tan et al. [50] recently introduced an environment-dependent, transferrable tight-binding model with parameters mapped from DFT (including input from DFT wavefunctions). The onsite parameters include terms dependent on the nearest neighbors to a given atom, as well as transferrable inter-atomic couplings, and therefore remove the uncertainty of interface treatment. Tan et al. [50] validate their approach by comparing tight-binding superlattice bands with those calculated with DFT and find good agreement.

45.4.2 Transmission Calculations with Transfer Matrices: Numerical Stability

Wavefunction-based transport calculations involve injecting propagating state(s) into a device and calculating the reflection and transmission coefficients (probabilities), and are thus open systems. The energy is continuous, not quantized, and the boundary conditions on the terminal wavefunction coefficients come from the complex band structure calculations discussed above. Mathematically, in a direct transmission calculation, this results in an $\underline{\mathbf{A}}\mathbf{x} = \mathbf{b}$ problem at each energy, with the inhomogeneous vector representing the open-system boundary conditions.

The transfer matrix Eq. (45.21) is a conceptually simple way of calculating the wavefunction in a layered device or structure such as an RTD, superlattice, or nanowire. Its structure is similar to that of the transfer matrix used to calculate the transmission through an RTD in the envelope function (i.e., effective mass) model [68], or to propagate electromagnetic waves through layered dielectrics. Because of its success in envelope function modeling of RTDs, the transfer matrix was the method first applied in early tight-binding models of these devices in the late 1970s/early 1980s. For a structure with boundaries at layers 0 and $(N+1)$, the wavefunction coefficients were calculated as:

$$\begin{bmatrix} \mathbf{C}_{N+1} \\ \mathbf{C}_N \end{bmatrix} = \prod_{L=0}^{N-1} \underline{\mathbf{M}}_{(L+1,L)} \begin{bmatrix} \mathbf{C}_1 \\ \mathbf{C}_0 \end{bmatrix}. \tag{45.23}$$

The boundary conditions applied on the layer 0 side include only a forward-propagating state and reflected reverse-propagating and reverse-decaying states; those on the layer $(N+1)$ side include only transmitted forward-propagating and forward-decaying states.

This procedure often worked for very thin structures, but once the number of transfer matrices exceeded around 20 or so, the calculation rapidly became severely inaccurate [69]. The sum of reflection and transmission probabilities, which *must* be unity, would instead turn out to be much higher, often in the range $10^2 - 10^6$. As a result, tight-binding models were not used to model realistic devices, which have long space-charge regions.

The cause of the instability is easily seen in the AlAs complex band plot of Fig. 45.2. Notice that the lowest conduction-band states (in the X-valleys) appear at around 1.90 eV (lowest black solid line). In addition to these purely propagating states, at the same energy, there are also three imaginary bands (blue dashed lines) connecting valence-band maxima to conduction-band minima at the zone center; these states grow and decay. Generally, then, there are evanescent (growing/decaying) states at the same energy as propagating states, and that is the source of the numerical problem. Products of transfer matrices can even be problematic in single-band models owing to accumulated round-off errors, but it generally takes many more than in the multi-band case, where there are evanescent and propagating states at the same energy.

The boundary conditions result from accurate, but still finite-precision, numerical calculations of the eigenvectors in Eq. (45.22), whether via an ordinary (transfer-matrix) or generalized eigenproblem. Thus, the boundary condition vectors will be corrupted with tiny amounts of other, disallowed eigenvectors; namely, those that grow in forward propagation; at a given energy, these evanescent states are generally present with propagating states. At each subsequent transfer-matrix multiplication, these initially small, erroneous eigenvectors grow in magnitude, and the growth is exponential. It does not take many transfer-matrix multiplications before the corrupt growing eigenvectors overwhelm the true eigenvectors, leading to a catastrophic failure of the calculation [69, 70]. In principle, this sort of failure can occur in an envelope-function calculation, but it requires extraordinarily thick barrier regions because each material supports only a single pair of states, propagating or evanescent, at a given energy.

45.4.3 Direct Transmission Methods

The numerical instabilities discussed above prevented multi-band tight-binding models from being used to model realistic aperiodic structures and devices for around a decade. Then, in the late 1980s–early 1990s, a series of solutions to the problem were developed [69, 71, 72]. Although the three methods differ in their details, they all recast the transmission problem as a large, sparse, matrix equation. This

reformulation into a large, sparse linear system is the key to preventing corruption of the true eigenvectors by erroneous growing eigenvectors. The renormalization method [72] was initially used for superlattice electronic structure calculations (thus with periodic, as opposed to open-system, boundary conditions). The first numerically stable resonant-tunneling diode calculations were those of Boykin et al. [69, 73], which included long, realistically sized space-charge layers. They divided the device into segments of a few layers over which wavefunction propagation using transfer-matrices was still accurate. The result is a large, sparse, linear system consisting of many small transfer-matrix problems, although the dimension is considerably smaller than the Hamiltonian with open-system boundary conditions. The next year, Ting et al. [71] published a similar method, in which they solve the $\underline{\underline{\mathbf{A}}}\mathbf{x} = \mathbf{b}$ problem resulting from the Hamiltonian with open-system boundary conditions directly. The large, sparse, linear system is larger than that of Boykin et al. [69] but avoids transfer matrices and their products.

The methods of Boykin et al. [69] and Ting et al. [71] work well for structures that have periodicity in the plane normal to the transport or quantization axis, such as RTDs and quantum wells. However, they can be costly for nanowires that have finite cross-sections, because the resulting layer-basis now consists of perhaps dozens of atoms (versus as few as two), each with many (often 20) orbitals. The layer matrices in Eq. (45.19) are therefore very large, which for a general basis and nanowire orientation can significantly slow the computation. However, for a nearest-neighbor basis and for [100]- and [111]-oriented nanowires in zincblende/diamond materials, these matrices are very sparse because each atomic plane contains atoms belonging to only one of the two face-centered-cubic sublattices, so there are no same-plane interatomic couplings. In 2008, Boykin et al. [74, 75] published an optimized renormalization method [72] to exploit this sparsity.

The optimized method [74, 75] is easily illustrated for the case of a [100]-oriented NW in diamond or zincblende. In these nanowires, four atomic planes make up a layer (i.e., a primitive cell for a perfect nanowire). In terms of layer matrices and vectors, the Schrödinger equation for a wire of L layers is written as [74]:

$$\begin{bmatrix} \underline{\underline{\mathbf{H}}}_{1,1} + \underline{\underline{\mathbf{\Sigma}}}_1 - \underline{\underline{1}}E & \underline{\underline{\mathbf{H}}}_{1,2} & \underline{\underline{\mathbf{0}}} & \cdots & \underline{\underline{\mathbf{0}}} \\ \underline{\underline{\mathbf{H}}}_{1,2}^{\dagger} & \underline{\underline{\mathbf{H}}}_{2,2} - \underline{\underline{1}}E & \underline{\underline{\mathbf{H}}}_{2,3} & \underline{\underline{\mathbf{0}}} & \underline{\underline{\mathbf{0}}} \\ \underline{\underline{\mathbf{0}}} & \ddots & \ddots & \ddots & \underline{\underline{\mathbf{0}}} \\ \vdots & \ddots & \ddots & \ddots & \underline{\underline{\mathbf{H}}}_{L-1,L} \\ \underline{\underline{\mathbf{0}}} & \cdots & \underline{\underline{\mathbf{0}}} & \underline{\underline{\mathbf{H}}}_{L-1,L}^{\dagger} & \underline{\underline{\mathbf{H}}}_{L,L} + \underline{\underline{\mathbf{\Sigma}}}_L - \underline{\underline{1}}E \end{bmatrix} \begin{bmatrix} \vec{\mathbf{C}}_1 \\ \vec{\mathbf{C}}_2 \\ \vdots \\ \vdots \\ \vec{\mathbf{C}}_L \end{bmatrix} = \begin{bmatrix} \vec{\mathbf{V}}_I \\ \vec{\mathbf{0}} \\ \vdots \\ \vdots \\ \vec{\mathbf{0}} \end{bmatrix}, \tag{45.24}$$

where the self-energies $\underline{\underline{\mathbf{\Sigma}}}_1$, $\underline{\underline{\mathbf{\Sigma}}}_L$ couple the emitter in Eq. (45.1) and collector (L) layers to the semi-infinite contact regions (unbiased nanowire), the vectors $\vec{\mathbf{C}}_j$ are the j-th layer orbital coefficients, and the injection into the emitter is the vector $\vec{\boldsymbol{V}}_I$.

As mentioned above, the layer matrices in Eq. (45.24) are themselves sparse: layers l and $(l+1)$ are only coupled by the last atomic plane of l and the first atomic plane of $(l+1)$. This means that the nanowire can be very efficiently treated one atomic plane at a time; the renormalization method [72] is ideally suited to the task. Renormalization decouples one plane from its neighbors and then re-couples the surrounding planes; no other planes are altered. Decoupling such a plane is accomplished as follows [74]:

$$H = M_{L,p}^{-1} \tilde{H} M_{R,p}^{-1}, \tag{45.25}$$

$$H = \begin{bmatrix} \ddots & \ddots & & & \\ \ddots & \underline{\underline{\mathbf{H}}}_{p-1,p-1} - \underline{\underline{1}}E & \underline{\underline{\mathbf{H}}}_{p-1,p} & \underline{\underline{\mathbf{0}}} & \\ \underline{\underline{\mathbf{0}}} & \underline{\underline{\mathbf{H}}}_{p-1,p}^{\dagger} & \underline{\underline{\mathbf{H}}}_{p,p} - \underline{\underline{1}}E & \underline{\underline{\mathbf{H}}}_{p,p+1} & \\ & & \underline{\underline{\mathbf{H}}}_{p,p+1}^{\dagger} & \underline{\underline{\mathbf{H}}}_{p+1,p+1} - \underline{\underline{1}}E & \underline{\underline{\mathbf{H}}}_{p+1,p+2} \\ & & & \ddots & \ddots & \ddots \end{bmatrix}, \tag{45.26}$$

$$\tilde{H} = \begin{bmatrix} \ddots & \ddots & & & \\ \ddots & \hat{\underline{\underline{\mathbf{H}}}}_{p-1,p-1} - \underline{\underline{1}}E & \underline{\underline{\mathbf{0}}} & \hat{\underline{\underline{\mathbf{H}}}}_{p-1,p+1} & \\ \underline{\underline{\mathbf{0}}} & \underline{\underline{\mathbf{0}}} & \underline{\underline{\mathbf{H}}}_{p,p} - \underline{\underline{1}}E & \underline{\underline{\mathbf{0}}} & \\ & \hat{\underline{\underline{\mathbf{H}}}}_{p-1,p+1}^{\dagger} & \underline{\underline{\mathbf{0}}} & \hat{\underline{\underline{\mathbf{H}}}}_{p+1,p+1} - \underline{\underline{1}}E & \underline{\underline{\mathbf{H}}}_{p+1,p+2} \\ & & & \ddots & \ddots \end{bmatrix}, \tag{45.27}$$

$$M_{L,p}^{-1} = \begin{bmatrix} \ddots & \underline{\mathbf{0}} & \ddots & \cdots & \\ \ddots & \underline{\mathbf{1}} & \underline{\mathbf{X}}_p^\dagger & \underline{\mathbf{0}} & \ddots \\ \ddots & \underline{\mathbf{0}} & \underline{\mathbf{1}} & \underline{\mathbf{0}} & \ddots \\ \vdots & \underline{\mathbf{0}} & \underline{\mathbf{Y}}_p^\dagger & \underline{\mathbf{1}} & \ddots \\ \vdots & \ddots & \ddots & \underline{\mathbf{0}} & \ddots \end{bmatrix}, \quad M_{R,p}^{-1} = \left(M_{L,p}^{-1}\right)^\dagger, \tag{45.28}$$

$$\underline{\mathbf{X}}_p = \left(\underline{\mathbf{H}}_{p,p} - \underline{\mathbf{1}}E\right)^{-1} \underline{\mathbf{H}}_{p-1,p}^\dagger, \quad \underline{\mathbf{Y}}_p = \left(\underline{\mathbf{H}}_{p,p} - \underline{\mathbf{1}}E\right)^{-1} \underline{\mathbf{H}}_{p,p+1}, \tag{45.29}$$

$$\begin{aligned} \hat{\underline{\mathbf{H}}}_{p-1,p+1} &= -\underline{\mathbf{H}}_{p-1,p}\underline{\mathbf{Y}}_p, \quad \hat{\underline{\mathbf{H}}}_{p-1,p-1} \\ &= \underline{\mathbf{H}}_{p-1,p-1} - \underline{\mathbf{H}}_{p-1,p}\underline{\mathbf{X}}_p, \quad \hat{\underline{\mathbf{H}}}_{p+1,p+1} \\ &= \underline{\mathbf{H}}_{p+1,p+1} - \underline{\mathbf{H}}_{p,p+1}^\dagger \underline{\mathbf{Y}}_p. \end{aligned} \tag{45.30}$$

Clearly, each plane is decoupled only once. Also, no complicated inversions are required for the decoupling matrices M:

$$M_{L,p} = \begin{bmatrix} \ddots & \underline{\mathbf{0}} & \ddots & \cdots & \\ \ddots & \underline{\mathbf{1}} & -\underline{\mathbf{X}}_p^\dagger & \underline{\mathbf{0}} & \ddots \\ \ddots & \underline{\mathbf{0}} & \underline{\mathbf{1}} & \underline{\mathbf{0}} & \ddots \\ \vdots & \underline{\mathbf{0}} & -\underline{\mathbf{Y}}_p^\dagger & \underline{\mathbf{1}} & \ddots \\ \vdots & \ddots & \ddots & \underline{\mathbf{0}} & \ddots \end{bmatrix}, \quad M_{R,p} = M_{L,p}^\dagger. \tag{45.31}$$

The matrices $\underline{\mathbf{X}}_p$, $\underline{\mathbf{Y}}_p$ and the inverses $\hat{\underline{\mathbf{H}}}_{p,p}^{-1}$ for later wavefunction reconstruction. The emitter and collector layers require a somewhat different, but not overly complicated, treatment because the open-system boundary conditions make them non-Hermitian [74].

The method becomes highly efficient when the decoupling proceeds by *alternating* interior atomic planes. In the initial step, inverting the diagonal blocks is trivial in the no-spin-orbit case and nearly trivial in the spin-orbit case. The interplane coupling matrices are themselves very sparse, so that in the initial step one-half of the nanowire is decoupled with trivial inversions and sparse-matrix multiplies. Subsequent steps use the alternating-plane method as well, and savings accrue in the second step (decoupling a further one-fourth of the NW), which requires a mixture of sparse- and full-matrix operations. Only the last fourth of the NW requires full-matrix operations. The computational efficiency improvement can be substantial [74, 75].

45.4.4 DFT-TB and Nanodevice Modeling

In the foregoing treatment we have concentrated on the empirical tight-binding approach for two important reasons: (1) It allows for efficient full-band structure transport calculations; (2) It has an orthonormal basis. The second point might seem an unusual one to make, but density functional theory tight-binding (DFT-TB) approaches [76–78] have non-orthogonal bases. From a purely electronic structure perspective the ab initio nature of DFT-TB is attractive [77]; however, device modeling involves more than electronic structure. As seen above, the calculation of currents and electromagnetic coupling involves the position and momentum operators and dealing with these in a non-orthogonal basis is problematic to say the least. In fact, all of the considerable formalism presented above appears very different in a non-orthogonal basis. Even including a scalar potential in a gauge-invariant manner is not easy. The overlap matrix, its inverse, and very often its square root and/or inverse square root are required for even simple calculations [79, 80]. These are the same size as the Hamiltonian: very large for any realistic nanodevice. Obtaining the exact non-orthogonal basis expressions from their orthonormal basis forms is very costly, although in some cases a first-order approximation will work [80]. Nevertheless, the cost involved (especially if a first-order approximation is insufficient) negates most of the advantages of tight-binding.

Sections 45.7.2, 45.7.3, 45.7.4, 45.7.5, 45.7.6, and 45.7.7 describe in detail the critical physics of nanowire transport based on our orthogonal empirical tight-binding with two very different transport models. The conclusion there is that the accurate modeling of the effective masses and the bandgaps is of utmost importance for silicon nanowires. The full charge self-consistency is important in the context of the overall nanowire charge and the details of the potential profile in 3D. These aspects can be handled using our method without the presence of an atomistic wavefunction basis. As discussed above, the passivation of dangling bonds can also be handled without an explicit basis. Although our method and its parameters are empirical and although more fundamental methods are appealing, we need to keep in mind the critical requirements of modeling realistic devices.

45.5 Transport with Green Functions

The numerical instability of transfer matrices can also be totally avoided by using a completely different Ansatz to compute transmission and transport: the non-equilibrium Green's Function (NEGF) approach. This approach is based on the formulation of an explicit, real-space representation of the whole device in a (sparse) Hamiltonian. The discussion

of the NEGF approach is beyond the scope of this book chapter. The foundational theory for NEGF was developed in the 1960s by Kadanoff and Baym [81] and Keldysh [82], but it remained confined to the physics literature. Bertoncini et al. [83] and Datta [84] took NEGF from an esoteric physics approach to a useful tool in electrical engineering by placing quantum transport simulations on a solid theoretical footing in the early 1990s. Datta refined the essential description of the methodology into very good introductions to NEGF for engineers in the early 2000s [85–87] and published a series of well received text books [88–90]. The latest two books [91, 92] accompany two self-paced study courses in nanoHUB-U [93, 94]. In Chapter ▶47, Datta provides an overview of NEGF.

The NEMO code developed at Texas Instruments to model resonant tunneling diodes provided the first tight-binding implementation within NEGF [20, 95]. The concept of an impulse response at every site inside the device eliminates the transfer matrix issue altogether. However, the computation of the open boundary conditions of the infinite contact layer is still battling similar issues depending on the detailed approach. Bowen provided a solution to the wavefunction-based quantum transmitting boundary method (QTBM)-based conditions [67, 96] in the case of singular coupling matrices [97]. Completely stable iterative surface green function treatments have been developed [98] and refined to a point of geometrically fast convergence [99].

The perception in the field of quantum transport is that the strength of the NEGF is derived from foundational physics principles and offers the fundamentally solid capability to include incoherent scattering. Yet most researchers in the field shy away from actually treating incoherent scattering owing to the high computational burden and use NEGF in a purely coherent, ballistic approach. Relatively few full implementations of incoherent scattering in NEGF for quantum transport with generally applicable device modeling considerations have been reported overall. NEMO1D, with its representation of local and nonlocal, inelastic optical phonon scattering in 1D RTDs [100], OMEN with inelastic phonon scattering [101, 102], and NEMO5 with nonlocal scattering [103], showed that this can be done, but also how computationally intensive the effort is.

Most researchers implement NEGF for its foundational physics principles and numerical stability in a purely coherent model without scattering self-energies. In that framework one can ask if there are other approaches that are equivalent. In this "coherent NEGF" context Bowen [94] demonstrated that the coherent wavefunction approach based on QTBM [67, 96] is in its physical content equivalent to the coherent NEGF approach. For 1D RTD devices Bowen showed that the NEGF is delivering results faster than the QTBM. Luisier showed that the QTBM is computationally less intensive than the NEGF approach in 2D and 3D systems [104].

It is the opinion of these authors that the real strength of the NEGF approach is the treatment of the open boundary conditions and their influence in broadening the interior quantum states, which provide finite lifetimes. This concept can now be conveyed to undergraduate students in EE by Datta's books [91, 92] and courses [93, 94]. Such general boundary conditions enable the treatment of complex, irregular contacts that inject carriers from scattering-broadened quasi-bound states [105] formed in quantum wells, geometrically L-shaped contacts, superlattice energy filters [106], and generally shaped [107] and disordered [107, 108] contacts. Such contact treatment includes an empirical broadening that compiles together scattering mechanisms of any sort. The empirical broadening parameter is typically chosen [20, 105] to be around 6.6 meV, equivalent to a scattering time of 0.1 ps. The parameter must be chosen to be energy dependent to avoid filling the gap with artificial states and so that it can be mapped to Urbach tails [103]. Recently, such broadening has been shown to be specifically critical in geometries such as heterostructure tunnel FETs (TFETs) that typically contain quasi-bound states confined close to the tunneling region owing to heterostructure design [109] or traps [110]. With the assumption of a local quasi-Fermi level in the contact regions one can easily link the NEGF approach with drift diffusion in sophisticated, quantum-state-dominated contact regions in 1D [111] and 2D/3D [112] to enable truly multi-scale transport modeling that ranges from ab initio-based atomistic representations to realistic device domains that extend hundreds of nanometers [105, 111, 112]. The use of tight-binding enables the multi-scale modeling of long-range, spatially dependent strain, or piezo-electric effects [3, 5, 25–28] and electron–nucleus interactions [29]. Chapter ▶11 by Meinerzhagen and Jungemann is dedicated to the multi-scale modeling approaches. Chapter ▶33 by Seabaugh and Paletti and Chapter ▶41 by Reggiani et al. discuss TFETs in detail in analytical and **k•p** approaches. Tight-binding approaches are used in He et al., Ameen et al., and Long et al. [109–111] and the extensive references therein.

45.6 Large-Scale Numerical Aspects

45.6.1 Hamiltonian Matrix Structures and Scaling for Closed Systems

One critical application-oriented advantage of the nearest-neighbor orthogonal tight-binding model is its very sparse matrix representation. The valence electrons of each atom are represented with a number of orbitals, where typical choices are s, sp^3, $sp^3\ s^*$, or $sp^3\ d^5\ s^*$ with 1, 4, 5, and 10 orbitals respectively, which ultimately determine the per-atom matrix size. If spin is explicitly included, which is typically necessary for most applications, then the number of orbitals simply

doubles. Each atom forms a well-structured block matrix that is coupled with the same block size to any neighboring atom (typically 4 in Si/Ge and III–V semiconductors). The on-site block matrix elements are diagonal only with a few off-diagonal terms coupling up and down spin through spin–orbit interaction. The block matrices coupling neighboring atoms are typically close to full, but couple only the same spin. Spin-up and spin-down coupling blocks are typically identical, unless modified by an external magnetic field. Rather, general Hamiltonian matrix construction algorithms were implemented early in the NEMO1D work [20]. The NEMO5 [113, 114] implementation was further generalized to include any number of orbitals such as *f*, which resulted in a rather rapid incorporation of piezoelectric materials such as SmSe and SmTe [115].

The specific block matrix Hamiltonian structure offers significant opportunities for computational optimization with regard to: (1) optimized Hamiltonian construction (pre-compiled Slater–Koster tables); (2) memory storage requirement reductions (number of stored elements and real/complex custom storage); (3) optimized matrix–vector multiplications; and (4) short integer-based pointers to address individual atoms. With these optimizations it was possible in NEMO3D to compute million-atom electronic structures in the year 1999 on the first Beowulf cluster computers built at Caltech/NASA/JPL [31, 32, 116]. Further optimized matrix–vector optimizations based on Intel-specific SSE instruction sets enabled scaling to 50 million atoms, which roughly corresponds to a chunk of semiconductor measuring $100 \times 100 \times 100\ \text{nm}^3$.

Figure 45.3 shows the excellent scaling on a moderate size cluster of 2008 [3]. The compute time represents the end-to-end computing time including set-up and output for four conduction band and four valence band states of an InAs QD embedded in GaAs. The fixed-size InAs QD is in the middle of the simulation domain and the GaAs buffer size is increased in this numerical experiment to demonstrate several key aspects of NEMO3D and its algorithms: (a) that the eigenenergies and eigenstates should be independent of the GaAs buffer size as long as the buffer is large enough; (b) that the calculation of interior eigenvalues remains stable regardless of the system size; (c) that memory requirements remain under control even in such large system sizes (special data structures and addressing schemes had to be developed to minimize storage and avoid duplicate storage on the distributed MPI-based algorithms); (d) that parallel scaling performance remains linear with system size. MPI communication requirements increase with the number of cores and with the number of atoms at each MPI parallel overlap region. The required times increase from 28.3 h per million atoms on eight cores to 83 h per million atoms on 128 cores. As the overall system size increases, more cores must be used to fit the overall computation into memory.

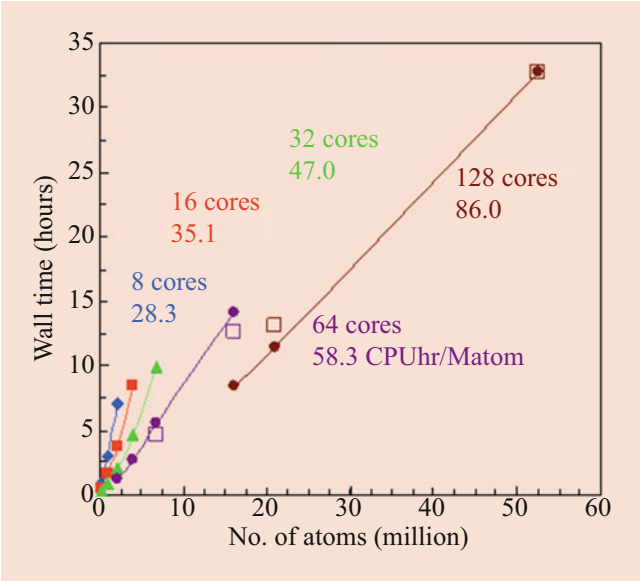

Fig. 45.3 Wall clock time versus number of atoms for end-to-end computations of the electronic structure of a quantum dot, for various numbers of cores on the PU/Woodcrest cluster. Listed next to the number of cores are the CPU h/million atoms needed in the simulation. (From Ahmed et al. [3] Fig. 45.10a)

45.6.2 Scaling Issues with Open Boundary Conditions

Scaling electronic structure calculations to multiple millions of atoms has been critical for the study of QDs and single shallow impurities such as or P in Si as discussed below. In these problems the system is considered to be closed and the eigenvalues are real (even though the Hamiltonian is in general complex). The introduction of open boundary conditions turns the Hamiltonian system into a non-Hermitian system. Any atom inside a unit cell that is connected to a semi-infinite lead is part of a full boundary condition sub-matrix that is completely full. Typical unit cells of a 2.1-nm Si nanowire cross section with transport in the [100], [110], and [111] crystal directions are depicted in Fig. 45.4 below. Numerical inversion stability in double precision limits such matrix sizes to typically dimension 2000 to 10,000. With a typical number of 20 orbitals only 100 to 500 atoms can be in open system boundary condition. Ignoring spin or ignoring *d* orbitals can result in a $\times 2$ or $\times 10$ increase in allowed atoms in the open surface. Either way the open cross sections in nanowires can barely reach 5–10 nm in diameter.

The NEGF method has now been established as the state-of-the-art in quantum transport modeling. The retarded Green's function is the inverse of the open system non-Hermitian Hamiltonian, is for realistic systems computationally prohibitively expensive, and is in almost all cases really not needed. The first and last columns of

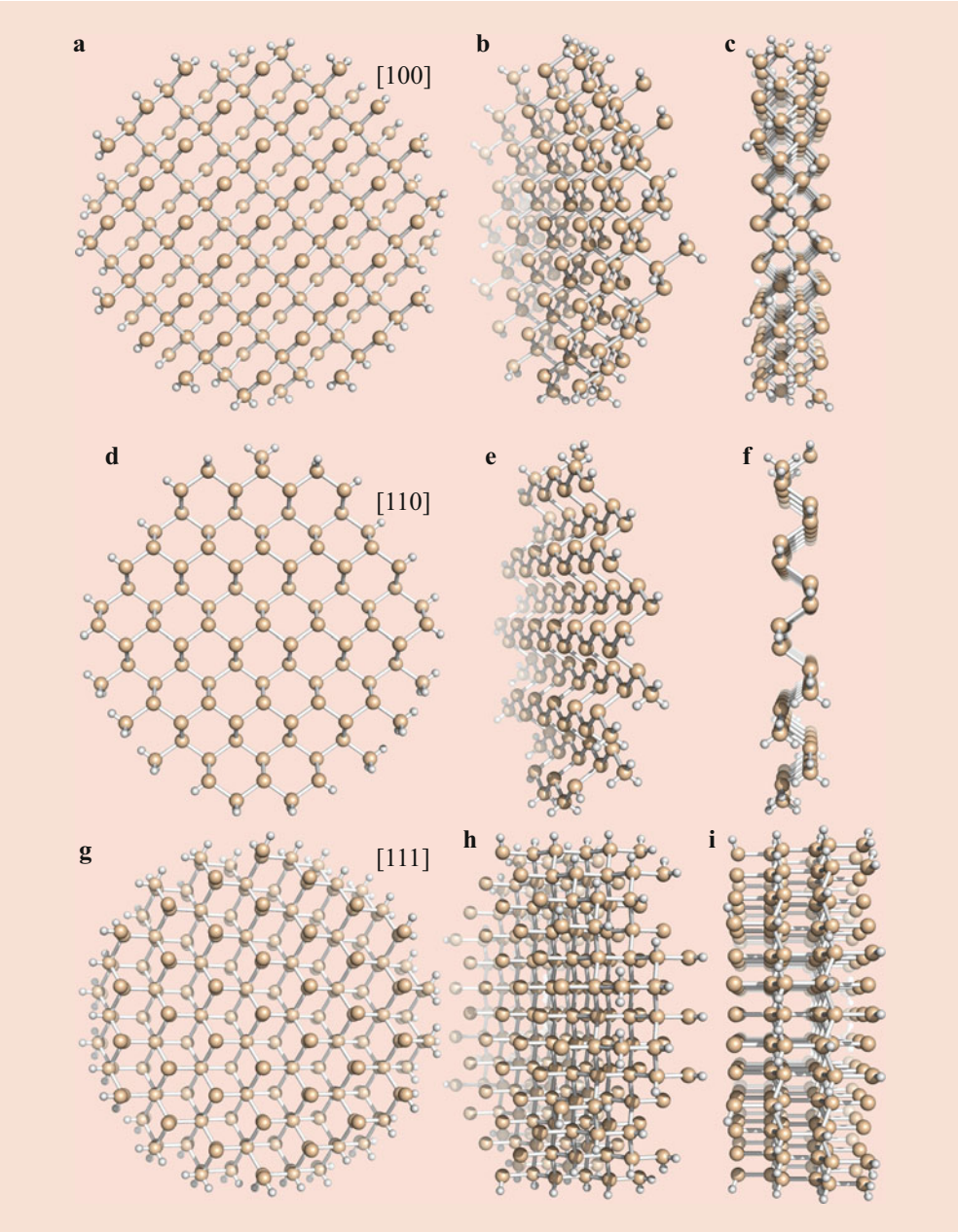

Fig. 45.4 Unit cells of three nanowires measuring 2.5 nm thick with transport in three different crystal directions [100], [110], and [111]. The full cross sections are shown in **a, d, g**, a tilted side view in **b, e, h** and a side view of the repeated cell in **c, f, i**. (The images were created with *Band Structure Lab* on nanoHUB [117])

the off-diagonal matrix elements are needed to compute the charge injection from the left and the right ends of the device. The diagonals represent the local density of states in the system and are needed if some sort of physics-based decoherence or scattering is included in the model [95, 105]. The Hamiltonian of the open system remains sparse, as described above, except for the block of atoms at the contacts that create a full-matrix sub-block. This sub-block is determined by the number of atoms in the contact regions, such as source and drain, that are modeled as infinite leads.

The size of the cross section scales the computational load in the number of atoms in the open surface in $O[(NB)^3]$, where N is the number of atoms in the repeated boundary cell and B is the number of orbitals in the basis (per atom). The length of the nanowire in terms of number of layers (L) enters the scaling of the computation basically linearly $O[L(NB)^3]$ in the typical recursive Green's function (RGF) algorithm [95]. The RGF remains the fastest general-purpose algorithm to compute the diagonals and selected off-diagonals of the system's Green's function, which is effectively the inverse

of the open-system Hamiltonian. Algorithm enhancements to reduce the cubic scaling dependence $O[L(NB)^3]$ to lower order, reduce the layer coupling, decompose the blocks, and to enable efficient parallelization have been developed over the years [72, 74, 75, 118–123].

The computational load can also be reduced by compressing the real-space basis in the cross section into modes [124]. This approach works very well for effective mass models and has been applied extensively [125, 126]. This basis transformation enables reduced computation times and increased cross-section sizes. The tool *nanowire* [127] on nanoHUB.org allows anyone to visualize the modes and explore larger cross-section devices interactively. The mode space method, however, has serious issues in multi-band (**k•p**) and atomistic basis sets, where the quantization in the cross section couples different orbitals. Careful construction of the mode space can be performed for **k•p** models [128–131]. The use of mode space representations in real space tight-binding models has been limited to carbon nanotubes and graphene, where simple p_z-orbitals were used for each atom [132–134]. (A 1D π-coupled chain is mathematically identical to a 1D s-orbital chain.) The mode approach has been shown to be extremely challenging if not impossible to implement systematically for atomistic highly coupled tight-binding approaches [135]. A related reduced-order method not requiring explicit eigenstates has been demonstrated for effective-mass models [136]. Relatively recently Mil'nikov et al. developed a methodology [137] that eliminates spurious eigenvalues in a specific energy window. This method has been used for nanowire metal–oxide–semiconductor field-effect transistors (MOSFETs) [137] and Tunnel FETs [138]. The method was further used in non-orthogonal DFT methods [139] and 2D ultra-thin body (UTB) devices [140]. The Mil'nikov method has been further automated and stabilized such that larger cross sections can be considered and implemented in NEMO5 [141].

If only coherent transport is considered and no quasi-bound, lead-decoupled states exist in the device, then fully atomistic implementations of wavefunction-based approaches such as the QTBM [67, 96] and optimized renormalization [74, 75] can scale significantly better than $O[L(NB)^3]$ owing to the usage of highly optimized linear solvers. For UTB transistors this method has been shown to be at least $\times 4$ faster than NEGF in the highly optimized and parallelized OMEN code [104].

45.6.3 Quantum Transport: Parallel Computing Scaling

With the QTBM or the NEGF the computational cost of quantum transport under high bias is so intense that large supercomputers can be utilized efficiently, if the transport algorithms are implemented efficiently. The art of parallel computing is to maximize the number of computing cores, to keep them busy computing, and to reduce the communication between nodes as much as possible. Communication can be minimized by the design and grouping of independent computing tasks. In an ideal world one would write a scientific program and a compiler would understand the levels of parallelism and distribute the computational load automatically. This has been a dream for a long time and still has not reached practical utility beyond shared memory use in a single CPU with OpenMP for real application programs. Many mathematical libraries use the shared memory OpenMP or threaded paradigm for parallelization within a single chip to about 24 or 64 cores. The message passing interface (MPI) paradigm requires the explicit design and programming of messages between cores or groups of cores. Such programming requires careful design, intense testing, and fine tuning. OMEN was designed to have four or even five levels of parallelism. At the highest level are independent groups of bias points that do not need to communicate at all until assembly of the final I–V curve. The next two levels parallelize the internal transport kernels of momentum (k) and energy (E) integrals. The (outer) k-integral requires the evaluation of (inner) E-integrals for fixed k. At the lowest level a transport kernel needs to be solved as a function of (E,k). That kernel consists of the computation of the open boundary conditions in source and drain and then the subsequent QTBM or NEGF transport equation solution. In the QTBM this requires an eigenvalue solution for the boundary conditions and a solution of a linear system of equations. Each of these can utilize standard libraries that have been parallelized in MPI or even OpenMP, or a combination of both. The dual-level MPI + OpenMP parallelization has not really delivered better computational performance within OMEN than the pure MPI parallelization. Within the four-level parallelization OMEN scaled almost perfectly to over 220,000 computational cores [75, 104]. In an ideal world of so-called strong scaling, one would divide the compute time by two if the number of computational cores is doubled. This strong scaling results in a straight line of reduced compute time on a logarithmic scale. OMEN delivers almost perfect strong scaling as depicted in Fig. 45.5. Running for 1 h on 221,400 cores corresponds to about 25.3 years compute time on a single CPU. The OMEN implementation was recognized with the Gordon Bell Prize Honorable Mention as the first Engineering Code running at the peta-scale in 2011.

45.6.4 Surface Passivation

The strength of empirical tight-binding methods is the valence electron bonding electronic structure representation within an atomistic representation of the physical geometry.

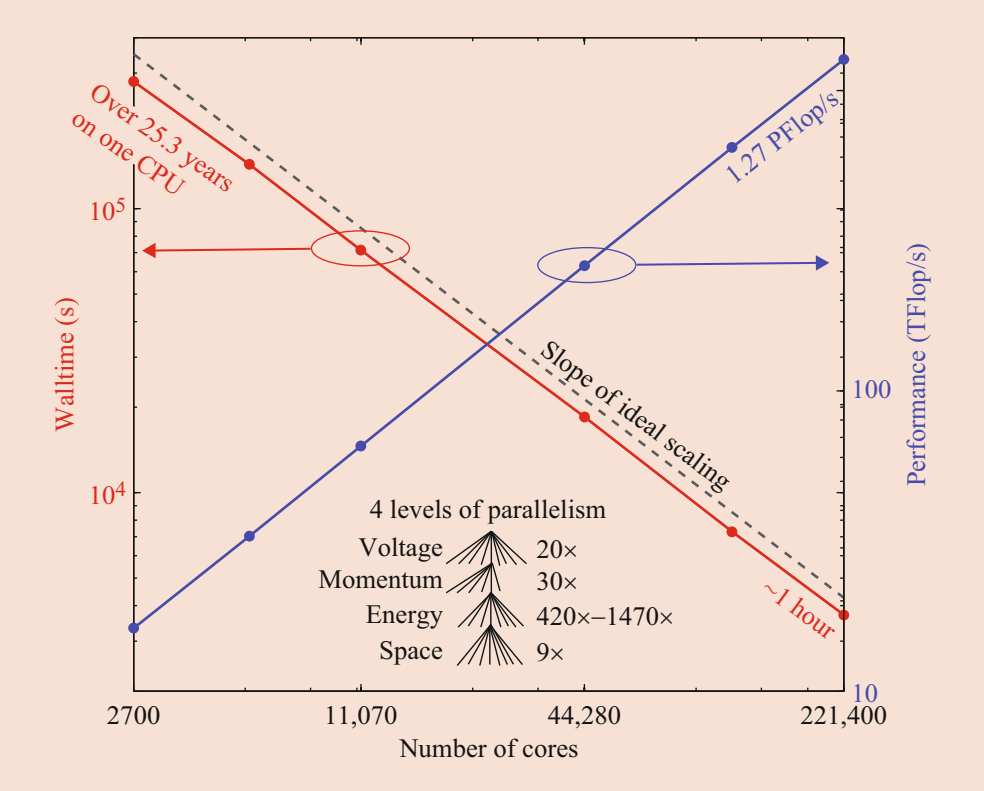

Fig. 45.5 OMEN parallel compute times for an ultra-thin body transistor as a function of the number of computational cores on a logarithmic scale. The dashed line indicates the slope of perfectly strong scaling. Also indicated on the right axis is the computational throughput in tera floating point operations per second. OMEN was the first engineering code to reach the peta-scale [104]

This representation lends itself very well to the numerical description of nanoscale structures. There is, however, one critical pitfall that needs special attention owing to finite size structures: dangling bonds. Here, we cover just some of the numerical aspects [142]. The physical interpretation and mapping to DFT are discussed in references Tan et al. and Lee et al. [49, 143].

For the NEMO team this issue of dangling bonds first emerged in the NEMO3D work, where InAs QDs embedded in a GaAs matrix were to be simulated. A finite amount of GaAs buffer layer needs to be included to properly model the wavefunction penetration into the buffer layer and to include the effects of spatial distortion to built-in strain. A periodic boundary condition would create a 3D array of QDs that would result in band structure and not in discrete states. Furthermore, such a periodic boundary condition requires the boundary surfaces to be perfectly flat and periodic, which is typically not the case in the strained and bulged systems. The simulation domain needs to be finite. If the simulation domain is simply terminated, then something really interesting can be numerically "observed" in the computed eigenspectrum of this finite system: eigenstates localized at the surfaces and edges emerge in the simulation domain with eigen-energies distributed across the whole energy spectrum, including the nominal band edge. These surface states are in this case of course an artifact due to the numerical requirement of a finite simulation domain. Naïve attempts to shift the onsite matrix element energies up or down to push the surface states out of the bandgap failed to achieve any generally reliable solution. Lee et al. [142] developed a numerical methodology for the typical $sp^3\ s^*$ and $sp^3\ d^5\ s^*$ models through a basis transformation into the direction of the dangling bonds and adding an adjustable energy shift to that bond energy. This method results in a very robust and stable method of eliminating the effects of the dangling bonds and has been highly adopted and cited in the literature.

Other, non-embedded, nanostructures actually do have exposed surfaces that require a physical and corresponding numerical passivation. The passivation method in Huang et al. [142] has found very wide use in the field to manage the surface states that naturally emerge in the tight-binding calculations. Twelve years later, the NEMO5 team generalized this passivation method [143] and linked it to chemical bonding. For the very thinnest active regions, however, explicit hydrogen passivation is often the most accurate method. Explicit passivation parameters have been determined by mapping ab initio wavefunctions and bands to tight-binding Hamiltonians [49]. We note here that in tight-binding meaningful surface

states emerge naturally. As such, this basis set naturally captures topological surface states [144] without any ad hoc parameters that are required in continuum basis sets.

45.7 Applications

45.7.1 Quantum Dots: Closed Systems

Quantum dots (QDs) enable designers to custom-create optical transitions at specific wavelengths or confine electrons at specific spatial locations with specific energies. Therefore, QDs are sometimes also called "artificial atoms." These systems are studied very widely in the literature. To highlight the enabling capabilities of tight-binding we just highlight a few QD applications here [145].

Figure 45.6 depicts in a graphically appealing way an InAs QD on an InAs wetting layer on a GasAs substrate, capped by an InGaAs capping layer. With such carefully engineered designs one can achieve optical emission at 1.5 μm for optical communication. A detailed description of the required modeling and the understanding of the design space is given in Usman et al. [5].

A typical dome-shaped QD of 20 nm in diameter and 5 nm in height might nominally only contain around 100,000 atoms. However, such QDs are formed by significant crystal lattice mismatches in the GaAs and InAs system via the Stranski–Krastanov growth method [2]. As such, these systems have a significant built-in strain that reaches far beneath the QD into the substrate. Cutting off the finite, closed system simulation domain too small results in significantly false eigenvalues with variations in conduction band states of over 150 meV and valence band states over 40 meV, underestimating the gap by over 20% [116]. Figure 45.7, taken from Ahmed et al. [3] shows that eigenvalue convergence and proper state polarization significantly depend on the size of the simulation domain. In Fig. 45.7b, the substrate is extended down to 50 nm underneath the QD. Eigenstate tuning can be controlled by the capping layer as indicated in Fig. 45.7b.

45.7.2 Nanowire Electronic Structure: Quasi-Periodic in 1D and Closed Systems in 2D

Nanowires as depicted in Fig. 45.8 are of significant technical relevance for transistor scaling at the end of Moore's law. The last generations of CMOS-based transistors in the so-called 5-nm node might be vertical stacks of such nanowires or nanosheets with wrap-around gate control. The following sections provide an overview of how empirical tight binding can deliver fundamental and quantitative insights into the performance of nanowires. We start from a very "simple" top-of-the-barrier model for a long nanowire, compare it with a sophisticated full transport model, and then explore the limitations of these transport models as the gate lengths are reduced. The two transport models vary significantly in a variety of aspects: (1) Use of a semiclassical dispersion versus full quantum transport, and (2) the treatment of charge in the nanowires: only the full quantum transport model considers full charge self-consistency. Somewhat surprisingly, these models deliver virtually identical results for long nanowires. These performance results show how critical the details of the band structure are versus the charge details in the wire and the surface. For short wires the accurate representation of the band structure is just as critical for effects of tunneling. Without the accurate representation of bandgaps and

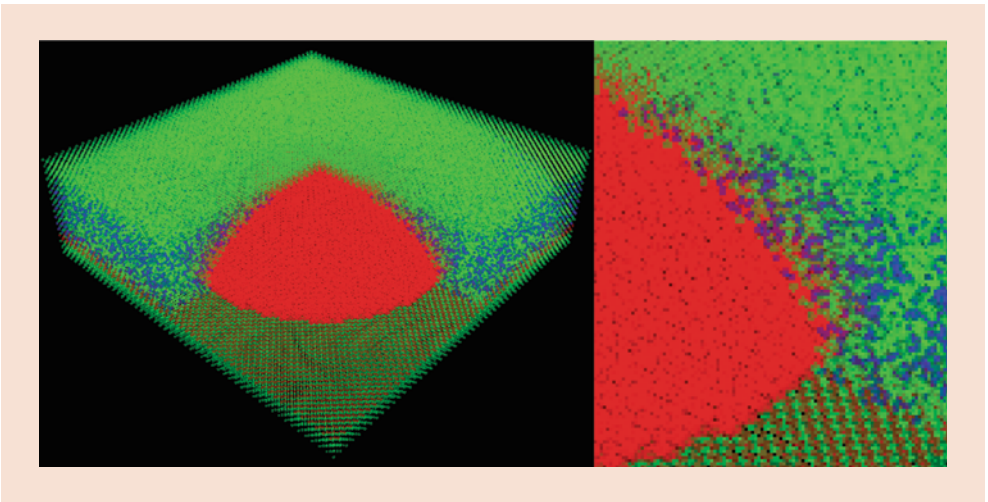

Fig. 45.6 Dome-shaped InAs QD measuring 20 nm in diameter and 5 nm tall embedded in an AlGaAs buffer layer grown on top of a GaAs substrate [5]. Image is also accessible on nanoHUB [146]

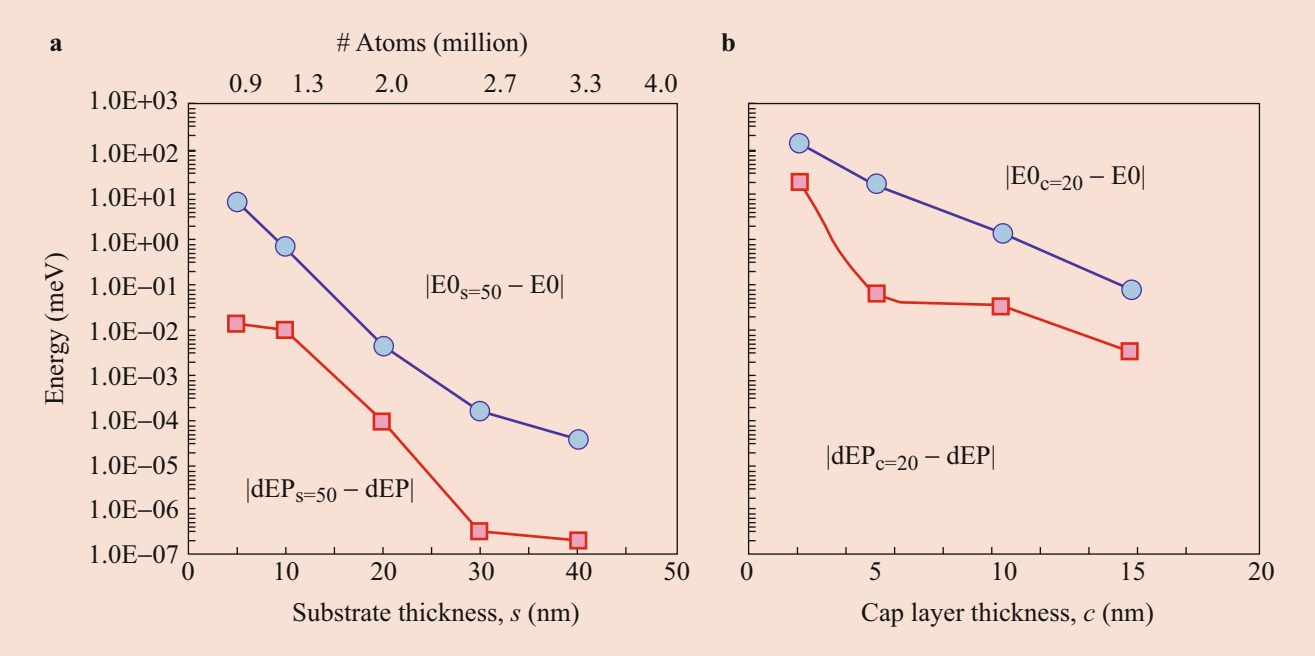

Fig. 45.7 (**a**) Substrate layer thickness dependence of the conduction band minimum and the P level splitting. Other structural parameters remain constant ($h = 5.65$ nm, $d = 11.3$ nm, $c = 10$ nm, and $D = 31.3$ nm). (**b**) The impact of cap layer thickness (with substrate, $s = 30$ nm and other structural parameters remaining the same). Lanczos convergence tolerance $= 1 \times 10^{-7}$. The changes in both these quantities are calculated with respect to the largest s (50 nm) and c (20 nm) respectively. (From Ahmed et al. [3])

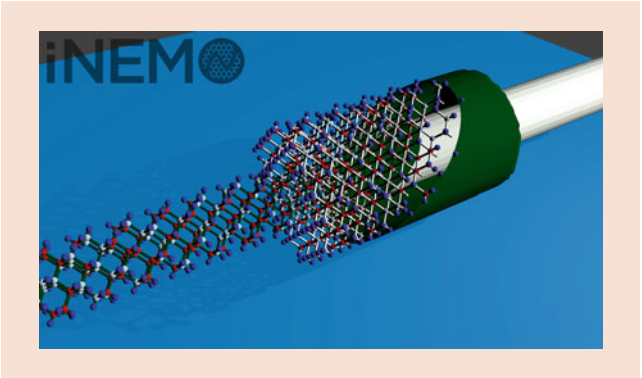

Fig. 45.8 Conceptualization of a finite sized nanowire. The difference between a typical continuum representation (**right end**) and an atomistic representation (**left end**) is eye opening. (Figure published online [147] created by Dr. Daniel Mejia in the NEMO5 development team)

effective masses one cannot provide real guidance to the design of nanometer-scaled transistors. These effective mass and bandgap accuracy requirements exemplify the concerns about DFT-TB discussed in Sect. 45.4.4 above.

Figure 45.4 above depicts unit cells of two different nanowires measuring 2.5 nm thick in the [100], [110], and [111] transport directions. If periodic boundary conditions are applied in the transport direction, then a dispersion in the transport direction can be computed with confinement in two dimensions. Band folding and band-to-band interactions result in complex new band structures owing to the confinement, as discussed extensively in the literature. For early tight-binding examples see Meija and Boykin et al. [148–151].

Visual inspection shows that the dispersions shown in Fig. 45.9 for [100], [110], and [111] Si nanowires vary dramatically. The [100] wire has four almost degenerate minimum band-edges at the Γ point with an effective mass of 0.31. The [110] wire has two almost degenerate bands of very light masses 0.14 and 0.18 at the Γ point. The [111] wire has three minimum band-edges off the Gamma point with an effective mass, two with masses $m^* = 0.48$, and one with $m^* = 0.68$. At the Γ point the [111] oriented wire has a negative effective mass of -0.26, effectively repelling carriers back into the source. Clearly, one can expect the [100] and [110] nanowires to conduct current much better than the [111] oriented wire.

The four lowest [100] wire bands are almost degenerate, with a mass of 0.31. In contrast, the two lowest bands of the [110] wire have effective masses of 0.14 and 0.18. Determining which one of the two nanowires has "better" electron transport requires more quantitative transport models.

At the macroscopic scale bandgap and effective mass are determined solely by bulk material properties. At the nanoscale, geometry, surfaces, and crystal orientation are equally important. Consequently, electron transport in nanowires varies significantly as a function of geometry.

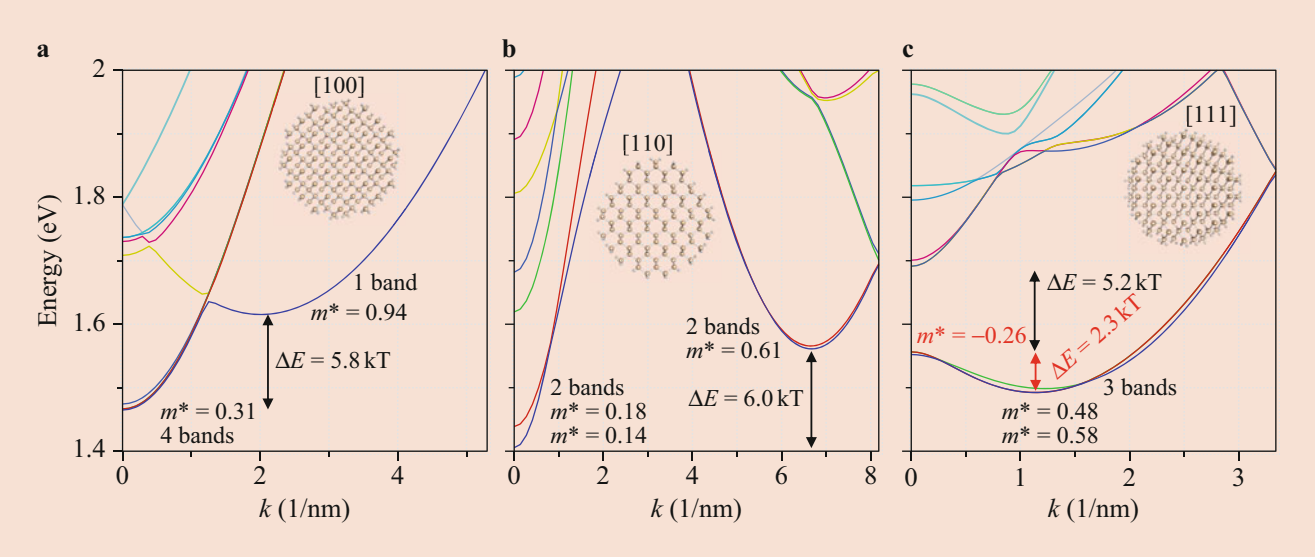

Fig. 45.9 Dispersion in the transport direction of infinitely long, ungated, and hydrogen passivated 2.1-nm Si nanowires in the (**a**) [100], (**b**) [110], and (**c**) [111] transport directions. (**a**) Four bands with $m^* = 0.31$ (units are the free-electron mass, m_0) at Γ are separated by an energy of about $5.8k_BT$ (at room temperature) from the next band with a heavier mass of $m^* = 0.94$. The heavy band with $m^* = 0.94$ is not occupied at the source injection of a transistor. (**b**) Two very light effective mass bands of $m^* = 0.14$ and $m^* = 0.18$ at Γ are separated by $6k_BT$ in energy from the next conduction band. (**c**) Three bands with the minimal conduction band of Γ, two with masses $m^* = 0.48$ and one with $m^* = 0.68$. These bands are close in energy of $2.3k_BT$ of hole-like masses of $m^* = -0.26$. Transport in the [111] direction experiences a significantly heavier mass and even carrier rejection due to the negative mass

This discussion demonstrates conclusively that *effective masses and bandgaps can be designed*!

45.7.3 Ballistic Transport from Nanowire Dispersions with the Top-of-the-Barrier Model

The beautifully simple top-of-the-barrier (TOB) model developed by Rahman et al. [152] can provide intuitive insight into the effects of material, geometry, and strain on the transport in nanoscaled transistors. Significant work has been published using the TOB model to examine and illustrate: atomistic versus effective mass models in Si nanowires [153]; injection velocity in ultra-thin-body Si [154] and III–V MOSFETs [155]; geometry effects on electrons [156] and holes [157, 158] in Si nanowires (as discussed above). The early application of the TOB model considered just the dispersion diagram without consideration of the effects of electrostatics. Later implementations, as are now available in NEMO5 or *Band Structure Lab* on nanoHUB [117] also consider the electrostatic effects in the device, which self-consistently relate band structure and local potential. Analytical extensions even help with estimating the effects of tunneling through the gated region with an "under-the-barrier model" [159].

The goal of this section is to demonstrate that very fast and "simple" tight-binding dispersion calculations for realistically sized nanowires can be mapped into simple methods that result in very fast estimates of nanowire I–V characteristics. The calculation of these I–V characteristics requires minutes versus hours in a full quantum transport model. We then compare these very fast calculations with full quantum transport calculations.

To estimate the transistor performance of the three nanowires considered here we utilize the TOB model implemented in the nanoHUB tool *FETtoy* [160]. *FETtoy* is configured with a small set of model parameters that are reminiscent of a compact model. The material parameters are entered as effective masses, band degeneracies, and dielectric constants. Multiple nondegenerate bands cannot be entered into the published version of *FETtoy*, but can, of course, be considered in the TOB model. For simplicity we choose the lowest lying bands to be degenerate and average out the masses. For the three wires considered we used [100]: $m^* = 0.31$ fourfold degenerate; [110]: $m^* = 0.16$ twofold degenerate; and [111]: $m^* = 0.51$ threefold degenerate. Shape and size of the nanowire are also entered. A gate dielectric measuring 1 nm thick is chosen, with dielectric constant 3.9. The TOB model can estimate effects of drain-induced barrier lowering (DIBL) and the degradation of the subthreshold swing with a gate control parameter α_G and a drain control parameter α_D. For clarity of the arguments we set $\alpha_G = 1$ and $\alpha_D = 0$, ignoring these gate issues and focus on the ideal, long wire performances.

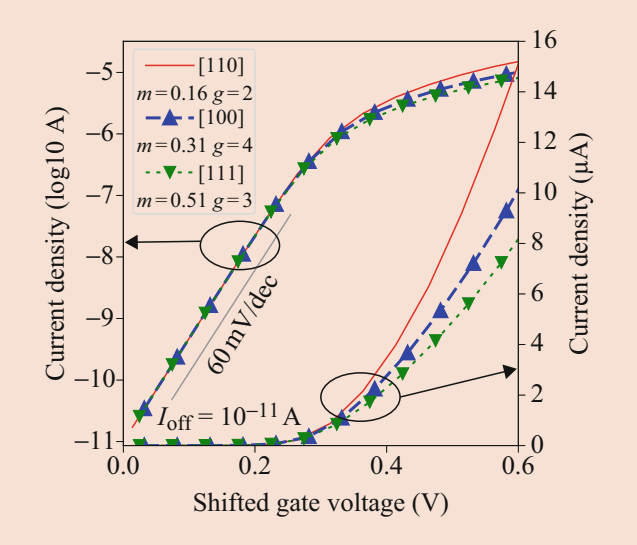

Fig. 45.10 Drain current versus gate voltage computed with the top-of-the barrier model implemented in the nanoHUB tool *FETtoy* [160]. Effective masses and band degeneracies taken from atomistic dispersions. The [110] wire delivers the highest ON current and the [111] wire delivers the lowest ON current

Figure 45.10 depicts the drain current versus gate voltage computed within the TOB as implemented in the nanoHUB tool *FETtoy* [160]. The left vertical axis is on a logarithmic scale and the right vertical axis on a linear scale for the drain current. The tool allows the user to set a threshold voltage that effectively adjusts the OFF current. We have taken the three current voltage characteristics for the three wires and shifted them to the same OFF current $I_{OFF} = 10^{-11}$A. As we consider ideal wires and neglect electrostatic effects along the channel all three transistors behave perfectly in the OFF region and deliver a subthreshold swing (SS) of 60 mV/dec. The three wires behave differently in their delivered ON current. As expected, the [111] wire delivers the lowest ON current. The low effective mass [110] with just two degenerate bands provides a higher ON current than the fourfold degenerate [100] nanowire with a mass that is roughly doubled compared with the [110] wire.

With these performance estimates for the three nanowires we emphasize here again that at the nanoscale geometry and crystal direction modify parameters such as bandgap and effective masses that in the past we considered material constants. *Bandgap and effective mass have become design choices.*

From the dispersion alone and the TOB significant insights can be gleaned about the transport properties of the nanowires. These calculations are computationally cheap as they principally involve the computation of a set of eigenvalues of a relatively small unit cell, as depicted in Fig. 45.4. Full quantum transport simulations are significantly more expensive and are discussed in the next section.

45.7.4 Full Quantum Transport in "Long" 15 nm Nanowires: 3D Representation

The TOB model is an excellent choice for screening for the fundamental effects of a variety of crystal directions and confinement effects. The TOB model has the ability to include some electrostatic effects to estimate DIBL and a subthreshold degradation. Analytical extensions might even help with estimating the effects of tunneling through the gated region with an "under-the-barrier model" [159]. A full TCAD-based 3D simulation of a wire, however, requires a full 3D representation of the carrier charges, gates, tunneling processes, and relaxation in the reservoirs. One of the first full 3D implementations of atomistic quantum transport was performed by Luisier et al. in the OMEN code [67, 75, 161]. Luisier continues to develop his OMEN code at ETH and Klimeck et al. continue to develop NEMO5 [113, 114] at Purdue. Within the scope of these modeling capabilities different cross-section shapes, materials, and stress conditions have been explored in a variety of materials systems such as Si, graphene, SiGe, III–V, and 2D materials.

OMENwire is a tool published in nanoHUB [161] powered by the OMEN simulation engine. *OMENwire* can easily be configured through a graphical user interface for different wire and UTB transistors. *OMENwire* runs on parallel machines typically for an hour or so to deliver the results in a fully graphical and interactive form. Different simulations for user choices such as geometries, crystal orientation, and material properties can be run and compared interactively. The results presented in this section have been generated with *OMENwire* code [161] and anyone can duplicate these results on nanoHUB.

We consider the same nanowire geometries as depicted in Fig. 45.4 above: 2.5 nm diameter Si in [100], [110], and [111] crystal direction. 10-nm source and drain at 2×10^{20} doping. 15 nm gate length with 1 nm EOT oxide. The drain voltage is set to 0.6 V and the gate voltage is ramped from 0 to 0.6 V. We use the default parameters of the dielectric constant of the Si channel (11.9), the channel material affinity (4.05 eV), dielectric function of the oxide (3.9), and the gate contact work function (4.1 eV). Figure 45.11 shows the drain current as a function of gate voltage on a logarithmic scale (left vertical axis) and a linear scale (right vertical axis).

Figure 45.11a depicts the direct numerical results as delivered by *OMENwire* given the specific geometries. Figure 45.11b shifts the three performance curves to the same OFF current $I_{OFF} = 10^{-11}$A. We note that the [111] wire simulations do not converge to meaningful results for gate voltages above 0.4 V, as further discussed below.

The threshold-shifted performance curves in Fig. 45.11b show that for the long gate length of 15 nm the three nanowires perform perfectly identically at 60 mV/dec in the subthreshold regime. With full 3D electrostatics the three

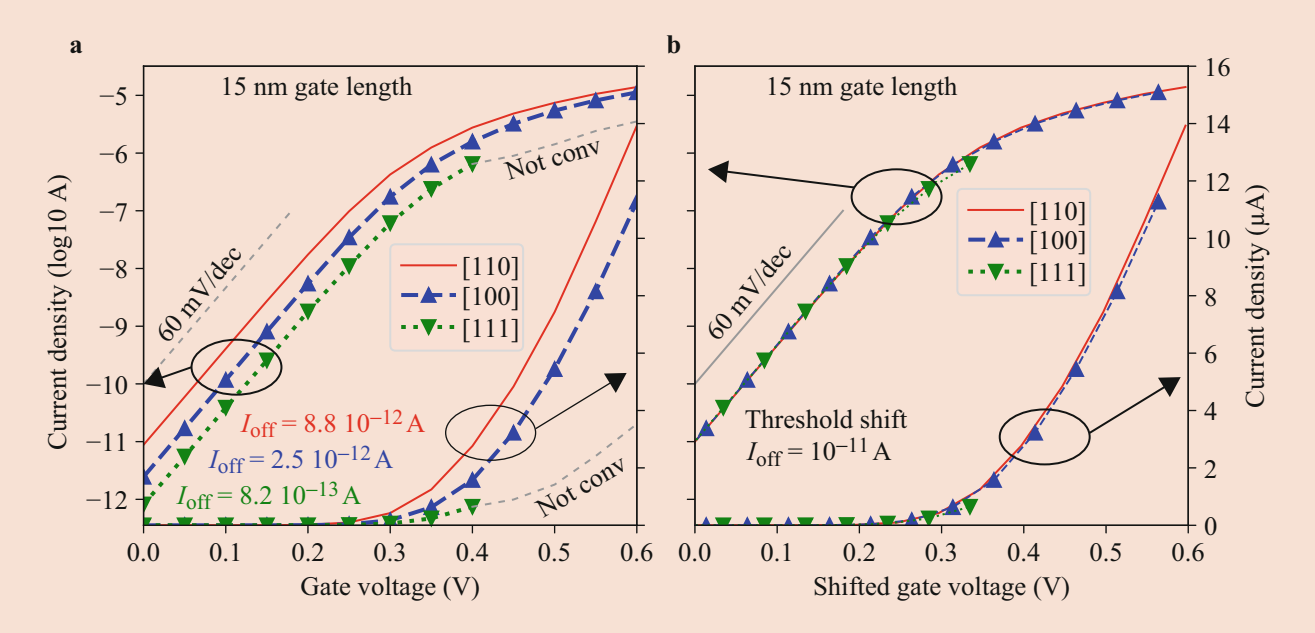

Fig. 45.11 (**a**) $I_d - V_g$ performance curves of the discussed [100], [110], and [111] nanowire transistors measuring 2.5 nm in diameter. Source-drain bias is 0.6 V. The gate length is long at 15 nm. (**a**) Simulation results with specific gate work function value of 4.05 eV. The [110] wire delivers the highest current and the [111] wire delivers the smallest current. (**b**) Performance curves of (**a**) shifted to a common OFF current 10^{-11} A. All transistor curves are virtually identical

wires also perform virtually the same in the ON region in this long channel device with ballistic transport. We note here that this result of virtually identical performance is different than the analytical TOB result depicted in Fig. 45.10.

Figure 45.11a shows the specific performance curves without adjustment of the threshold voltage. The [110] wire delivers the highest current and the [111] wire delivers the lowest current. Understanding the different performances requires a deeper understanding of the band structure, density of states and charge densities in the different wires.

Figure 45.12 shows a composite picture of localized band edge (black line), band structure in the source (green lines), band structure in the drain (orange lines), normalized current density (blue line), and transmission coefficient (brown line) for the three nanowires considered, with a source–drain voltage of 0.6 V and a gate voltage of 0.3 V. Each of these plots is available in *OMENwire* [161]. The rather different band structures discussed in Fig. 45.9 above are evident, resulting in rather dramatic transmission coefficients. The normalized current density under high bias is the product of the transmission and the Fermi function in the source. This composite picture Fig. 45.12 illustrates the relative energy scales and spatial positions in the nanowires. The different effective masses in the three wires combined with the same doping level results in three very different Fermi levels in the source and the drain, as indicated by the horizontal red lines. For the very heavy mass [111] wire the Fermi level is just under the conduction band by 5.4 meV, whereas the [100] and [110] Fermi levels are above the conduction band by 26.1 meV and 98.6 meV respectively. From a classical transport perspective, we can now look at the maximum barrier height in the channel measured against the Fermi level in the source. For the [111] wire that energy distance is 141 meV or about $5.5k_BT$. For the [100] and [110] wires this energy difference is much smaller, at 85 meV and 69 meV respectively, corresponding to about $3.3k_BT$ and $2.7k_BT$. With a barrier about $3k_BT$ higher in the [111] wire one can expect a factor of e^3, so about a $\times 20$ lower current in the [111] wire, regardless of transmission coefficient details. The simulated I_{OFF} difference in Fig. 45.11a is a factor of about $\times 10$, indicating that the Fermi level difference estimate is off by a factor of 2. The I_{OFF} difference in Fig. 45.11b between [110] and [100] is a factor of $8.8/2.5 \approx 3.5\times$. The Fermi level energy difference to the top of the barrier is just $0.6k_BT$, corresponding to a Fermi tail difference of $e^{0.6}$ or a factor of $\times 1.8$. Also, this Fermi level estimate difference is off by a factor of 2. The difference in current between the [100] and [110] requires some more detailed understanding.

The normalized current density and transmission coefficients shown in Fig. 45.12 are depicted for more clarity and ease of comparison in Fig. 45.13 again (taken directly from the *OMENwire* code) [161]. The figures are augmented by the band structure information in Fig. 45.9, which measures the number and effective mass of the lowest bands. For each available injection band one can see a close to step-like feature to a discrete value of transmission as expected. As

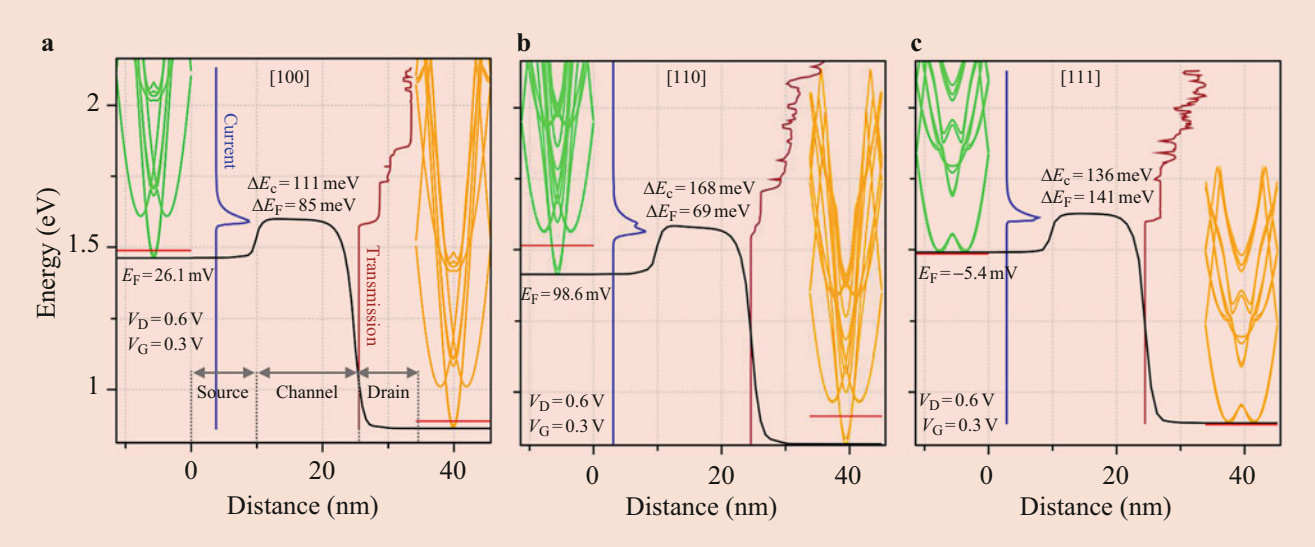

Fig. 45.12 Localized band edge (black line), band structure in the source (green lines), band structure in the drain (orange lines), normalized current density (blue line), and transmission coefficient (brown line) for the three nanowires considered, with a source–drain voltage of 0.6 V and a gate voltage of 0.3 V. (**a**) [100] wire, (**b**) [110] wire, and (**c**) [111] wire. The Fermi levels in the source are indicated as E_F, the maximum barrier height in the channel measured against the conduction band and Fermi level in the source as ΔE_C, ΔE_F respectively

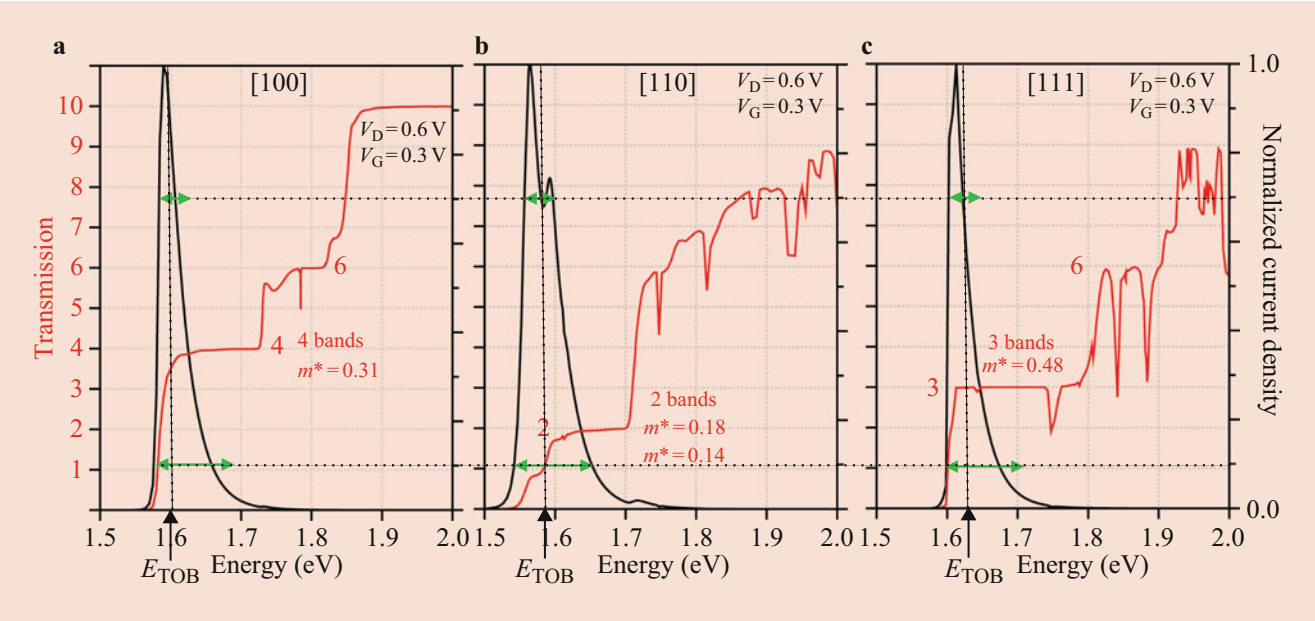

Fig. 45.13 Transmission (red lines) and normalized current density (black lines) for the three nanowires considered with a source–drain voltage of 0.6 V and a gate voltage of 0.3 V. The effective masses of the lowest bands correspond to the values in Fig. 45.9. The vertical dashed line labeled with E_{TOB} indicates the energy of the top of the barrier inside the channel. The green double arrows in (**b**) indicate the energetic width of the current flow at a normalized value of 10% and 70%. These two green vectors are also inserted in (**a**) and (**c**), indicating that the energetic width of current flow in the [100] and [111] wires is much narrower than in the [110] wire

discussed above in the context of effective masses of the three different wires, one can expect the [111] wire to conduct the current less well than the other two wires owing to its much larger effective masses. As also discussed above, the [100] wire has a nearly fourfold degenerate band set with effective mass of 0.31, whereas the [110] wire has two bands close to degenerate with masses 0.14 and 0.18.

The transmission coefficient of the [111] wire with its three lowest bands with effective mass 0.48 shows a rather steep rise at the band edge to a value of 3. The [100] wire,

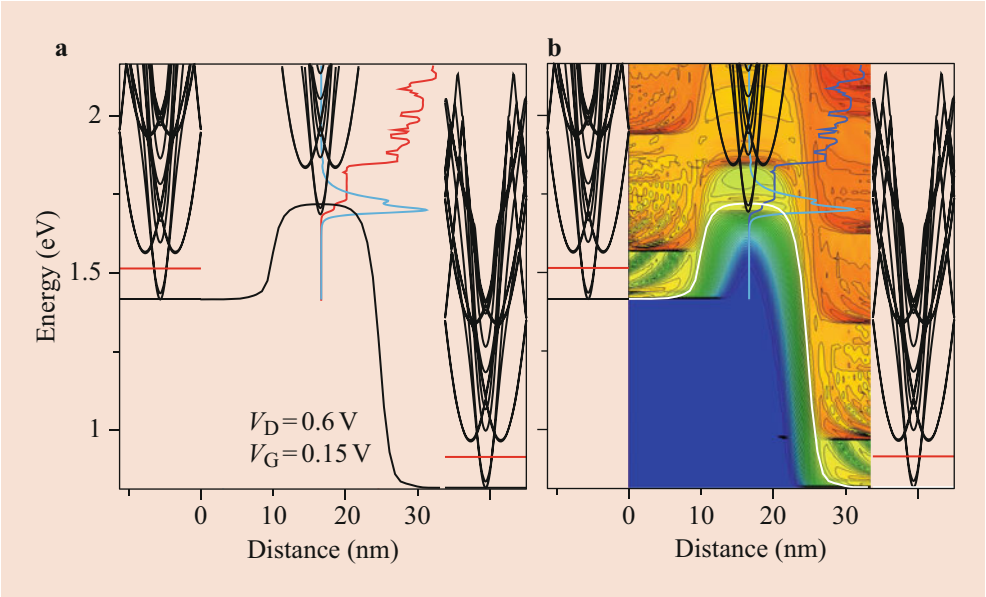

Fig. 45.14 (**a**) Localized band edge, band structure in the source and drain, normalized current density (blue line), and transmission coefficient (red line) for the [110] nanowire similar to Fig. 45.11b. The specific gate bias here is different – it is further in the OFF state at 0.15 V. The source/drain band structure is also superposed into the middle of the channel and aligned with the second set of bands. (**b**) Same as (**a**) but the local density of states is superposed in the quantum device simulation region

with its four lowest bands of effective mass 0.31, has a more gradual slope to a maximum transmission of 4 above the band-onset. The [110] wire has the broadest onset of the transmission and the two bands that are not quite degenerate result in a transmission step to values of 1 and 2. These different slopes of the transmission coefficients have a significant effect on the three different normalized current densities. Each of the three plots in Fig. 45.13 shows a dashed vertical line labeled E_{TOB}, corresponding to the TOB conduction band edge in the channel under 0.3 V gate bias. Even for this large gate length geometry of 15 nm *there is a significant tunneling current flow under the conduction band edge*. Just by visual inspection it appears that the [110] wire has the largest energy range in its tunneling current contribution. However, the tunneling current alone does not yet explain the differences in the current between the [100] and the [110] wire.

Two horizontal arrows in Fig. 45.13b "measure" the energetic width of the current density at a level of 10% and 70% of the peak value of the normalized current. These two arrows are transposed in the figures for the [100] and the [111] wire showing that the [110] wire transmits current over a significantly wider energy range.

Figure 45.14 examines in more detail why the [110] wire has a much wider energetic range in its current density. Figure 45.14a basically repeats Fig. 45.12b for a [110] wire, where, however, the gate bias is reduced to 0.15 V, further into the OFF region. Clearly, there is a lot of current flowing under the conduction band edge in the center of the device. Figure 45.14b superposes in addition the local density of states (DOS) in the simulation domain. It is rather evident that there is a significant DOS under the nominal conduction band edge. In the source and drain the DOS aligns with the band structure of an ideal wire. However, in the central device region the band structure really no longer aligns perfectly with the local DOS. There is a significant DOS in the bandgap and also the state spacing is (slightly) different to the additional OFF-state electrical confinement in the middle of the channel.

The conclusive reason why the [110] wire delivers a higher current than the [100] wire is the interplay of electrostatic potentials and tunneling through the gate-controlled potential.

45.7.5 Full Quantum Transport Versus an Analytical Model in "Long" 15-nm Nanowires

The full quantum transport simulations presented above provide significant insights into the device physics of the 2.5-nm-thin cross-section wires. Tunneling and modeling of the detailed potential are critical in the understanding of the device performance. It is, however, particularly interesting to see that the overall device characteristics for the long 15-nm gate length of the wires in the [100], [110], and [111] directions perform virtually the same when they are shifted

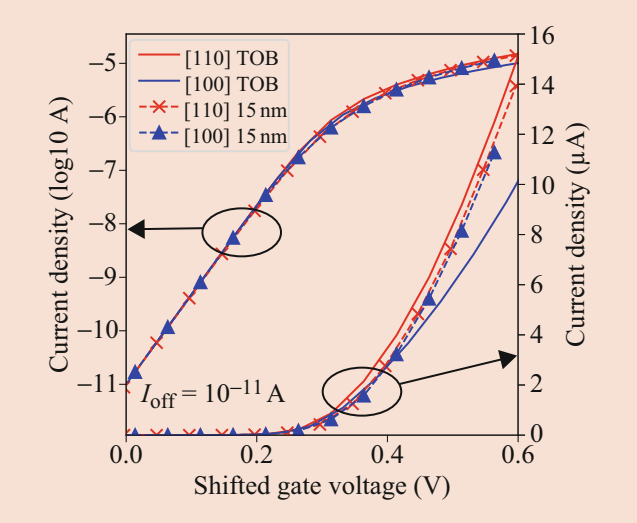

Fig. 45.15 Comparison of the TOB and full 3D quantum transport calculations. Solid lines are the results with the analytical top-of-the-barrier model shown in Fig. 45.10 for [110] and [100] wires. The dashed lines with labels correspond to the full 3D OMEN quantum transport results shown in Fig. 45.11b for a 15-nm gate length wire. All curves are threshold voltage shifted to the same off current at 10^{-11} A

to the same OFF current (see Fig. 45.11b). Not only are the subthreshold performance results the same at 60 mV/dec but the ON currents are also virtually the same. Figure 45.15 compares the full 3D quantum transport simulation results threshold-shifted from Fig. 45.11b and the analytical TOB results depicted in Fig. 45.10 for the [100] and [110] wires. The TOB model is configured in the *FETtoy* simulation on nanoHUB to ignore any assumptions of short channel effects. These simulations are agnostic of a channel length and the results are shown in solid lines. The full 3D *OMENwire* simulations are labeled in dashed lines with symbols. The subthreshold behavior of the cases considered is identical, performing at 60 mV/dec. Only the linear scale shows that the TOB model predicts slightly different ON currents for the two wires, whereas the full 3D model predicts virtually identical ON currents. If we were to consider the full 3D model as ground truth, then the TOB model underpredicts the [100] wire ON current by about 30%. There are plenty of uncertainties in the full 3D quantum transport model and one is compelled to ask: "are the hours of CPU time consumed in full quantum transport simulations worth it?" The next section will show the strength of a full 3D quantum transport model in a regime, where the analytical TOB model really breaks down – going from "long" 15-nm channel lengths to 5 nm.

45.7.6 Full Quantum Transport in Short 5-nm Nanowires: 3D Representation

The full quantum transport simulations presented above provide significant insights into the device physics of the 15-nm gate length nanowires with 2.5-nm cross sections. In this segment we consider a gate length of 5 nm and keep all other device parameters such as doping source/drain extension, gate oxide, etc., the same. Figure 45.16a depicts the drain current as a function of applied gate voltage for a source-drain voltage of 0.6 V. Just as before for the 15-nm gate length wire, here also for the 5-nm gate length the [100] wire delivers the highest current, followed by the [110] wire, and the [111] has the lowest current for the same work function specifications. However, Fig. 45.16a shows that the three different wire orientations show very different SS, far worse than the ideal 60 mV/dec. The high-current [110] wire shows the worst SS at 119 mV/dec. For zero gate voltage, its OFF current is 2 orders of magnitude higher than the [111] OFF current. The ON–OFF swing for the high-current [110] wire in the 0.6-V gate sweep is less than 3 orders of magnitude. For typical circuits the usual requirement is an ON–OFF swing of 4 or 5 orders of magnitude. *Although the [110] wire delivers the highest current, it fails to turn off effectively.*

Figure 45.16b depicts the same performance curves as (a) except for thresholds shifted to an OFF current of 5×10^{-10}A. The [110] wire is shifted out of range as it does not deliver such a low OFF current with the chosen work function in the simulation. Possibly, some work-function configuration could turn off the [110] wire enough to reach 5×10^{-10}A. The [100] and [111] wires roughly perform the same in the threshold region at an SS of 81 mV/dec and 79 mV/dec, respectively. The [100] wire delivers about twice as much ON current as the [111] wire.

Figure 45.17 explains the origin of the very different OFF current behaviors of the three different wires. Figure 45.17 depicts the local conduction band edge and density of states for the three different nanowires at zero gate voltage and source–drain voltage of 0.6 V. In each of the three wire source regions the Fermi level is indicated with a horizontal red line and an energy window of $5k_BT$ above the Fermi level is indicated with a gray box. The [110] has the highest Fermi level and the [111] wire has the lowest Fermi level owing to the very different effective masses, as discussed above. The normalized current density as a function of energy is indicated as a blue line and the red line indicates the transmission coefficient.

There is a significant density of states available under the nominal conduction band edge resulting in significant tunneling. The [110] wire (middle) with the very high Fermi level has virtually all of its normalized current flow within the $5k_BT$ energy range around the Fermi level. The central barrier height measured against the Fermi level in the source is $9.9k_BT$. The barrier is nominally high enough if this were a classical transport problem. Clearly, the OFF current in the [110] wire with its light effective mass is completely carried by tunneling.

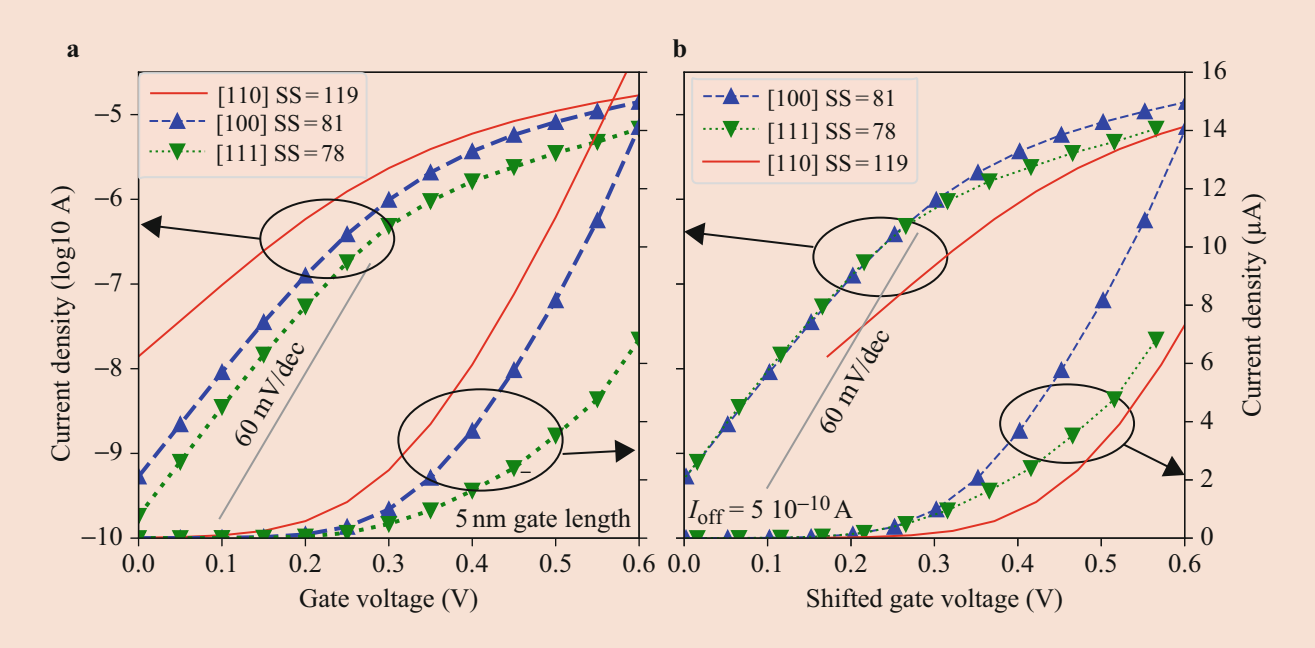

Fig. 45.16 $I_d - V_g$ performance curves of the [100], [110], and [111] nanowire transistors measuring 2.5 nm in diameter and with a gate length of 5 nm. Source–drain bias is 0.6 V. (**a**) Simulation results with specific gate work function value of 4.05 eV. The [110] wire delivers the highest current and the [111] wire delivers the lowest current. The [110] high-current wire fails to turn off effectively and has a subthreshold swing of 119 mV/dec. The ON/OFF current swing is less than 3 orders of magnitude. (**b**) Performance curves of (**a**) shifted to a common OFF current 5×10^{-10} A. The [100] wire delivers the best performance

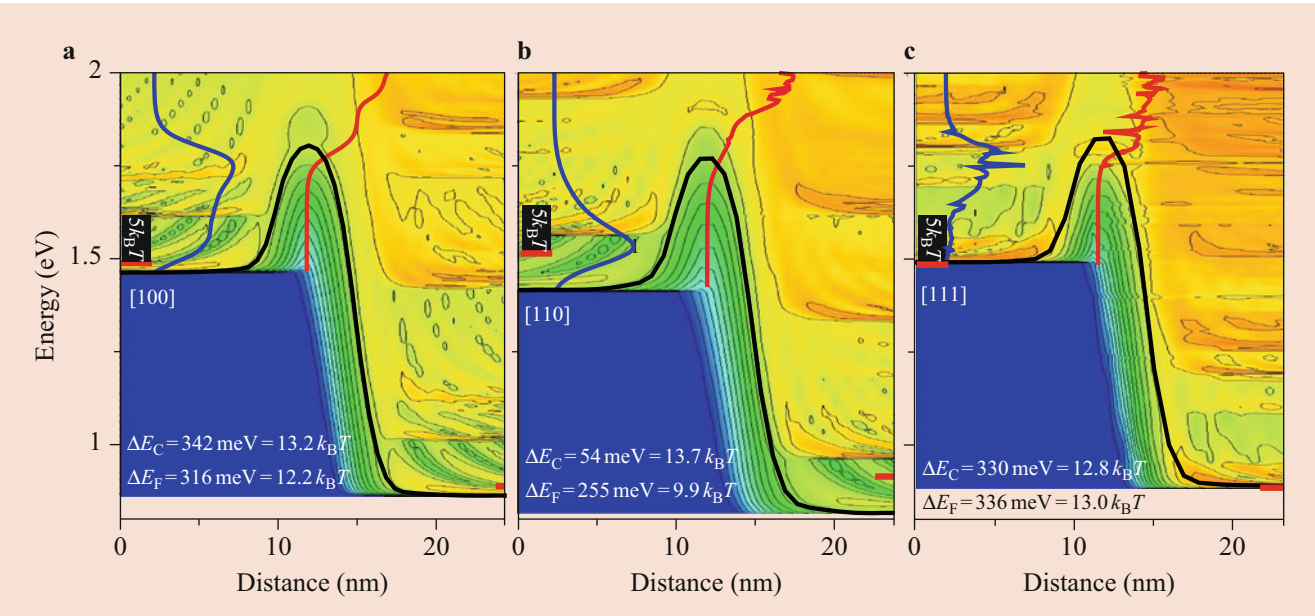

Fig. 45.17 Local conduction band edge and density of states for the three different nanowires a) [100], b) [110], and c) [111] at zero gate voltage and 0.6 V source–drain voltage. In each wire source region the Fermi level is indicated with a horizontal red line and an energy window of $5k_BT$ above the Fermi level is indicated with a black box. The blue line in the source region indicates the normalized current density as a function of energy and the red line in the central device indicates the transmission coefficient. ΔE_C and ΔE_F indicate in each figure the energy difference between the source conduction band and the Fermi level with respect to top of the barrier in the channel. There is a significant density of states available under the nominal conduction band edge resulting in significant tunneling. The [110] wire (**b**) has virtually all of its normalized current flow within the $5k_BT$ energy range around the Fermi level. The [100] wire (**a**) has some current flow within that $5k_BT$ energy range, but most of the current flows above. The [111] wire has virtually all its current flow above the $5k_BT$ window. Current flow above the 5kBT energy range implies that it is quite small in its absolute value. Therefore there is significant tunneling for the [110] (**b**) wire in terms of absolute current

The [100] wire shows some normalized current flow within that $5k_BT$ energy range, but most of the current flows above. As the availability of injected carriers above the $5k_BT$ window is exponentially lowered, one can clearly see why the [100] wire OFF current is much lower than the [110] wire OFF current. The [111] wire has virtually all its current flow above the $5k_BT$ window. In both [100] and [111] wires the exponential carrier fall-off above the Fermi function is compensated for by the exponential increase in the tunneling below the nominal barrier in the gate region, which results in some tunneling current flow. In these two wires, [100] and [111], the OFF current is dominated by tunneling, but because of the heavier transport effective masses the tunneling currents are significantly smaller.

45.7.7 Convergence Issues in High-Bias Coherent Transport Simulations

In Fig. 45.11 the dashed lines labeled "not conv" indicate that several high bias points calculations are not converged for the [111] wire. Such high bias convergence issues are not unusual for coherent quantum transport simulations and several authors have discussed the issues and suggested solution approaches [162–166]. At this time, we are not aware of a publicly available simulator that fundamentally addresses the non-equilibrium treatment of contacts. The *OMENwire* tool we use here does not have an implementation that can manage these fundamental contact issues. The tool can therefore be driven into nonconvergence and we would like to openly discuss the fundamental issues and limits of the simulation approach.

We focus on the drain current versus gate voltage characteristics of the [111] wire in a bias point range of 0.3 V to 0.6 V, as depicted in the insert of Fig. 45.18a. The main component of Fig. 45.18a depicts the electrostatic potential in the middle of the wire as referenced to the local band structure in the source similar to Fig. 45.12c, which depicted a single gate bias of 0.3 V. Here, we plot the band edge for gate biases ranging from 0.3 V to 0.6 V in steps of 0.05 V. The lowering of the barrier as a function of gate voltage is well visualized. At a gate bias of 0.5 V the local band edge develops an additional, step-like feature in the middle of the channel, which migrates closer to the source side for further increased gate voltages. The formation of the "unreasonable

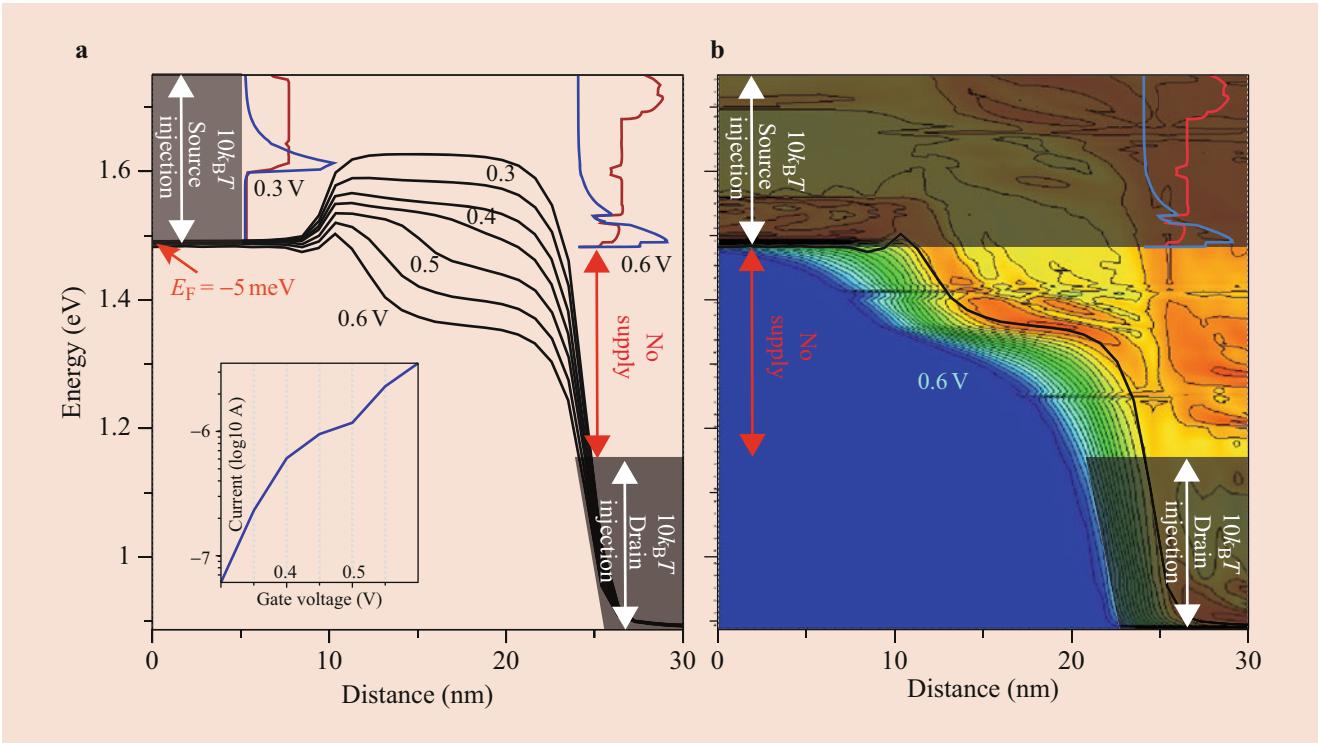

Fig. 45.18 (**a**) Insert: drain versus gate current voltage characteristic of the [111] 15-nm gate nanowire. A nonsmooth curve is visible, with a dip at 0.5 V. The main part shows the conduction band edge in the [111] nanowire for different gate biases ranging from 0.3 V to 0.6 V. Top left and bottom right shaded regions indicate the available Fermi sea of electrons to a height of $10k_BT$ above the Fermi level. Blue lines at the top right and left indicate the energy distribution of the current density for 0.3 V (**a**) and 0.6 V (**b**). (**b**) Similar to (**b**) for a gate voltage of 0.6 V with the local density of states superposed

looking" potential band edge in the middle of the channel is a symptom related to the sharp increase in dI/dV in the inset current-voltage characteristic.

The top left of Fig. 45.18 indicates the transmission coefficient (red) and current density injected from the source at a gate bias of 0.3 V. Next to it a gray box indicates a carrier distribution in the source that reaches as high as $10k_BT$. For the gate voltage of 0.3 V one can see that the barrier in the channel still limits the distribution of the current flow. That is, the current turns on about 0.1 eV or $4k_BT$ above the Fermi level in the source. At a gate bias of 0.6 V the barrier has virtually completely vanished and the current (as indicated in the top right of the figure) now flows above the source conduction band edge. As expected, there is no current flow under the conduction band edge. The bottom right of Fig. 45.18 indicates the supply function of carriers in the drain. Clearly, no electrons can reach from the drain into the channel at the applied source drain voltage of 0.6 V. All carriers in the channel must come from the source. The red vertical arrow between the label "No Supply" between the source and drain supply functions indicates that there are no carriers that can be injected within that energy range from either source or drain coherently.

The transport effective masses of the [111] wire are much larger than those of the [100] and [110] wires and therefore the injection of carriers from the source into the channel is not as intense in the [111] wire. The [111] wire cannot supply enough charge into the channel to "oppose" the electrostatic pull down from the gate and the drain.

Figure 45.18b considers the gate bias point 0.6 V in more detail with a superposition of the local density of states under the local band edge diagram of (a). The source and drain injection energy ranges are included, as well as the current density and transmission coefficient. The local density of states is numerically well resolved, and the channel broadened quasi bound states that were also visible in Fig. 45.14b. Again, there is no indication that the quantum mechanical components of this simulation have any issues of energy or spatial resolution.

One can now argue that the Poisson solution is not really stable and causes the step-like feature in the channel potential. Numerical experiments on this very device show that neither tightening the Poisson convergence criteria nor increasing the momentum or energy resolution in the quantum transport simulation neither changes the convergence of the potential nor adds more numerical detail. The Poisson solution "converges" to the same potential and overall current every time. Physical intuition tells us that the potential does not "look right." This electrostatic potential is not a result of bad numerical stability but is due to the incompleteness of the physical model. In a more realistic simulation one would need to include energy loss mechanisms in the channel and a more detailed model of the source contact.

The intuitive view to "fix" the issue of Fig. 45.18 is to include inelastic electron scattering mechanisms [101, 102, 167] such that the electrons can lose energy and populate the states in the channel, and then the potential will float up, restoring the expected smooth evolution of the electrostatic potential in the channel. In fact, OMEN has shown that scattering adds an additional potential drop into the channel and the source extension region. However, in light of the relatively short channel of 15 nm and an expected high degree of ballistic/coherent it is the authors' opinion that a more sophisticated treatment of the channel will not provide the real physical solutions.

The real issue is the treatment of the source contact [162–166]. The model assumption is that the Fermi level at the numerical start of the device is constant with regard to the equilibrium, zero bias condition. It is assumed that the contact can supply unlimited carriers, even at perfectly unit transmission in all available channels. A more realistic representation of that source injection would include the details of the electron reservoir and its ultimately connected metal contact. A comprehensive model would represent in more detail the ability of the "contact" to inject carriers into the device. A very nice depiction on how scattering self-consistently modifies the electrostatic potential in the gate region, as well as the highly doped spacer, has been given in Luisier and Klimeck [101, 102].

The failure of the coherent quantum transport model was relatively obvious for the 15-nm gate length [111] nanowire, as the current showed "unusual" behavior. The natural question now emerges, why was something similar not observed in the 5-nm gated [111] wire? The *OMENwire* simulator returns "converged" results and the current voltage characteristics do not reveal any trouble.

Intuitively, one can argue that the 5-nm gate region is already so short that the gate and drain voltage combined will pull very hard on the channel potential so that the drop should almost be linear. That intuition is actually about right, as depicted in Fig. 45.19a, where the expected electrostatic potential is shown throughout the nanowire for different gate potentials ranging from 0 to 0.6 V. Nicely visible is the increased asymmetry of the potential in the gate region, where the peak of the potential shifts from the middle of the channel more and more to the source. This effect is called drain-induced barrier lowering (DIBL).

The low gate voltage data sets from $V_G = 0$ V to $V_G = 0.4$ V are drawn in dotted lines. The last "reasonably looking" gate voltage data sets at $V_G = 0.5$ V are shown in a solid line and the data for $V_G = 0.6$ V are denoted with long dashed lines to draw the viewer's attention. All the potential profiles "look" reasonable except for the last bias point of 0.6 V, which we discuss below.

The charge filling of the channel as a function of gate voltage is depicted in Fig. 45.19b for different gate volt-

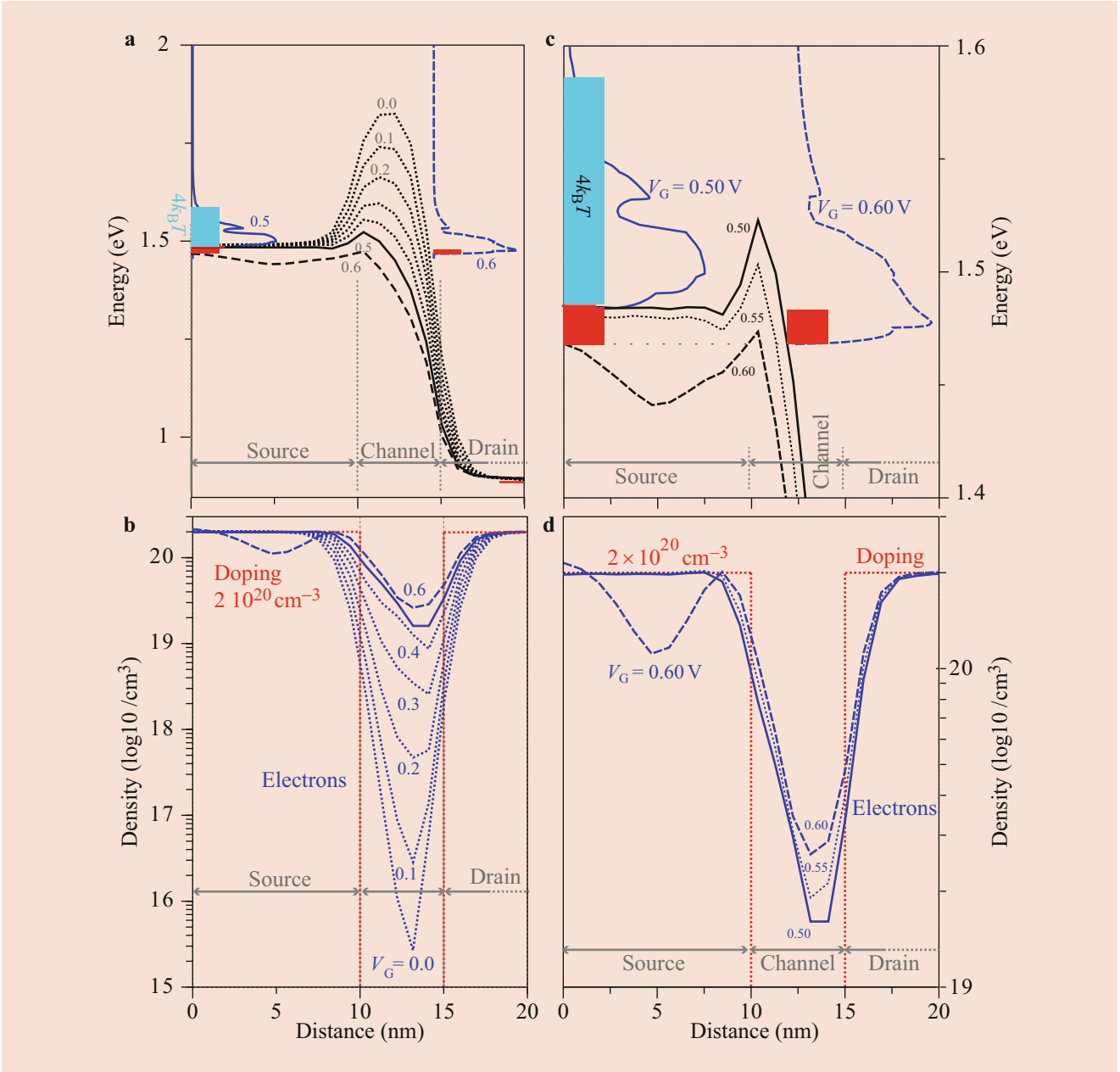

Fig. 45.19 (**a**) Conduction band edge (black lines) in the [111] nanowire for gate biases ranging from 0 to 0.6 V. Blue line indicates the energy distribution of the normalized current density (blue line). Fermi levels in source and drain are indicated by red lines. An energy range of $4k_BT$ above the Fermi level is indicated by a blue shaded region. Only a 5-nm section of the 10-nm drain region is shown. (**b**) Electron density (blue line) and doping density (red dashed line) in the wire for the same gate voltages as (**a**). (**c**) Zoomed in data of (**a**) for the gate bias $V_G = 0.5$ V and $V_G = 0.6$ V. A dotted line guiding the view of the potential evolution at $V_G = 0.55$ V is added as a dotted line. The conduction band edge shows a potential dip in the source at $V_G = 0.6$ V. There is a significantly increased energy range of injection from the source (red shaded area). (**d**) Zoomed in data of (**b**) for the gate bias $V_G = 0.5$ V and $V_G = 0.6$ V. A dotted line guiding the view of the potential evolution at $V_G = 0.55$ V is added as a dotted line

ages. At zero gate voltage the channel is virtually empty, with a smooth exponential decay at the abrupt doping profile change. Of course, this corresponds well to the high gate potential barrier in Fig. 45.19a for $V_G = 0$ V. As the gate voltage is increased, the charge in the channel increases linearly on a logarithmic scale, which corresponds to the linear subthreshold current increase on a logarithmic scale (Fig. 45.16). Everything looks reasonable about these charge profiles except the one for the gate voltage $V_G = 0.6$ V.

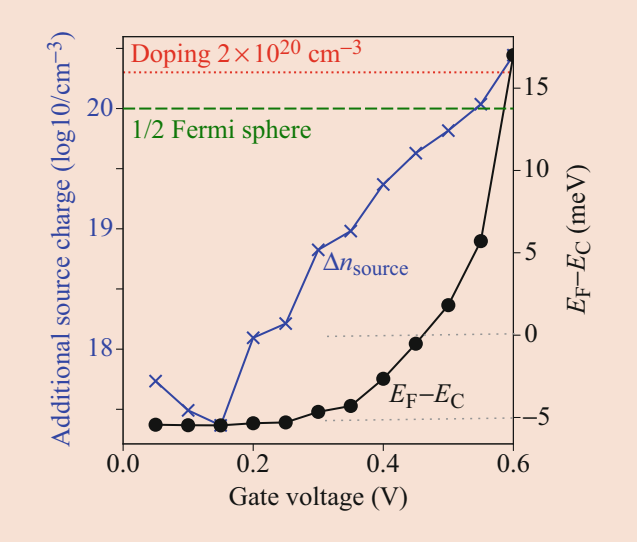

Fig. 45.20 Right scale: energy difference between the Fermi level and the conduction band edge at the coherent injection point at site 0 nm of the [111] 5-nm gate length nanowire. Left scale: additional charge needed at the coherent injection point to balance the charge throughout the device. At high gate biases that additional charge approaches and then exceeds that of half the forward-moving Fermi sphere. The source cannot possibly provide enough charge moving forward through the device

The right column of Fig. 45.19 shows the zoomed-in data sets of the left column for the gate voltages $V_G = 0.5$ V (solid line) and $V_G = 0.6$ V (long dashed line). A data set at $V_G = 0.55$ V is added as a dotted line to guide the eye in the evolution as a function of gate voltage. The data at $V_G = 0.5$ V all look very reasonable. At $V_G = 0.5$ V the source potential is still flat and pegged to the Fermi level (Fig. 45.19c). Current flow (blue line) sets in as expected above the conduction band edge, basically tunneling through the remaining tiny barrier. The electron density (Fig. 45.19d) for $V_G = 0.5$ V is converged to the doping profile level in the source region.

As the gate potential is increased above $V_G = 0.5$ V all the device internal quantities begin to show unusual behavior. At $V_G = 0.55$ V the electrostatic potential in the source region begins to drop slightly (on this scale) under the potential values that correspond to an equilibrium source. At $V_G = 0.6$ V the electrostatic potential at the injection point drops precipitously and the overall source potential develops a physically very unreasonable dip. The current continues to increase because now there is current flow within a potential range that previously had no injection (see the red energy range). The charge density in Fig. 45.19d shows a very unphysical dip in the source region. Clearly, something is starting to go "wrong" in the simulation that requires some careful attention.

Figure 45.20 depicts (black line with circles) the energy difference between the Fermi level and the conduction band edge at the coherent injection point of the source (at the 0-nm coordinate). As discussed above, the Fermi level is about 5 nm under the conduction band edge for $V_G = 0.0$ V. As the gate voltage is increased, the Fermi level remains roughly constant and then begins to increase. The Poisson solution in *OMENwire* requires more and more charge in the source to balance the doping level and the transport throughout the whole device. Let us look at a very trivial and incomplete model based on semiclassical charge, where

$$N_{\text{class}} = N_c \exp\left[-\left(E_C - E_F\right)/k_B T\right]. \tag{45.32}$$

At $(E_C - E_F) = -5.51$ meV for $V_G = 0.0$ V and a balanced doping of $N_D = 2 \times 10^{20}$ cm^{-3} we can take $N_C = 2.48 \times 10^{20}$ cm^{-3}. Now we define

$$\Delta n\left(V_G\right) = N_c \left\{\exp\left[-\left(E_C\left(V_G\right) - E_F\right)/k_B T\right] - 1\right\} \tag{45.33}$$

and plot $\Delta n(V_G)$ in Fig. 45.20 with a blue line. Although there is some numerical noise for gate voltages below $V_G = 0.2$ V we numerically observe that the extra charge in the source injection point grows exponentially over 3 orders of magnitude. At a bias of $V_G = 0.55$ V the additional charge reaches 1/2 of the Fermi sphere in the source and at $V_G = 0.6$ V the additional charge exceeds the doping in the source.

Figure 45.20 clearly demonstrates that the source injection is driven to a point where the assumption that it can provide "infinite" charge breaks down. As the charge needed to balance the Poisson equation approaches that of the doping level, the physical model breaks down completely and results in erroneous charge and potential profiles.

We argue the point here that the erroneous high gate bias results are not caused by a bad numerical implementation, but by the fundamental model assumption [162–166]. With prior research results, we conclude that a more comprehensive model of the contact regions of the highly doped semiconductor, as well as the connected metal, are needed in the limits of extreme bias operation, which would deplete the numerical contact regions.

We conclude this section by advising caution – look at the numerical data carefully even as you use sophisticated tools!

45.7.8 Short Channel Devices: A New Design Paradigm with New Requirements

Effective mass and bandgaps are design parameters: the discussions above have shown that at the nanometer scale effective masses and bandgaps *can be designed by geometry and crystal direction* [67, 168]. Strain alters the atomic arrangements and can be used to tune the band structure further [67, 156, 168–171]. The self-consistently calculated charge distribution in nanowires shows that the band structure is affected by charge filling [156]. Silicon nanowires can be designed to have effective masses that are competitive and

even lower than the traditional III–V materials. We note here that especially under scaling into the 5-nm regime, III–V materials show significantly increased masses owing to their nonparabolic band structure [20, 101, 102]. This typically reduces the perceived benefits of III–V materials even more [155, 171, 172].

III–V material versus *Silicon materials :* the discussions in the previous sections demonstrated that for a "long" 15-nm channel a light effective mass material can in principle deliver the highest current as derived from the TOB model. This seems to confirm the long-standing expectation that lighter effective masses as found typically in III–V materials will outperform typical silicon devices. However, with smart crystal orientation choice and strain engineering the effective masses in silicon can be tuned, as discussed above. The III–V material insertion into the silicon process flow is extremely expensive and silicon has been able to achieve competitive performance.

Fast materials with light effective masses are not desirable: for short channel devices such as the 5-nm gate length nanowire discussed here we can clearly demonstrate that low effective mass materials are not desirable at all. At such short gate lengths, the potential barrier becomes very small, electrons principally tunnel through it and a heavy mass is desired to suppress that tunneling [155, 169–174].

Tight-binding captures critical device physics: here, we have focused on the more intuitive electron transport physics. We note here that a nanowire electron dispersion begins to look just as complicated as a hole dispersion. All the methodologies presented here can be explored for hole transport and have been implemented in OMEN and NEMO5. Necessary physical details, such as spin-orbit coupling, strain dependence, geometry and crystal direction dependence can be captured efficiently with only a few model assumptions. Transport in hole nanowires and device design as a function of geometry and gating have been studied [158, 168, 173, 174].

Tight-binding combined with coherent and incoherent transport models: the combinations of tight-binding with QTBM and tight-binding with NEGF have now been established as the state-of-the-art device modeling basis sets and approaches. Software packages based on this baseline are built by industrial and by academic research groups and commercialization efforts are underway to release these methods in standard device TCAD packages. The methodology is stable and reliable enough that they can be released to the scientific community. The *OMENwire* and *Band Structure Lab* codes used here are available on nanoHUB as discussed below.

Roadmap modeling changed from analytical device models to full 3D quantum transport models: the 2013 International Technology Roadmap for Semiconductors (ITRS) roadmap [178] in its Process Integration, Device, and Structure chapter, relies for its device model performance projection on a compact model using the computer-aided design tool MASTAR [179]. The SS enters this model as a phenomenological parameter, rather than as a characteristic predicted by a physics-based model. Full 3D atomistic quantum transport modeling showed that such a compact model can lead to erroneous predictions [177] and physics-based model results were adopted to calibrate predictions in the subsequent ITRS release.

Physics-based contact models require further development: in the sections above we have also demonstrated and explained in detail how the state-of-the-art transport models break down, when driven to extreme conditions. We are not the first to explore these issues [162–166], but described this in detail so that users can be aware of the pitfalls of state-of-the-art simulation tools such as *OMENwire*. Under very high bias conditions the source may no longer supply enough charge to satisfy the channel transport ability. More sophisticated models are needed to model the heavy doping semiconductor source/reservoir, as well as the metal contact to that reservoir region. Several efforts to treat the occupation limitations of the injecting source regions in 1D geometries with an effective mass model have been reported [162, 166]. It is our opinion that the traditional NEGF perturbative scattering methods may provide some help when used in the semiconductor device region. However, we also believe that the source depletion and treatment of the contacts is a first-order effect that must be treated not as a perturbation but by a fundamental approach.

45.8 Beyond Device Physics Advancements: Reaching the World

Nanoelectronic devices such as QDs and nanowires that have been subject to intense research in the past 25 years are finding widespread adoption in today's technologies. As these devices are inserted into real products their design and optimization now require accurate physics-based models that can explore the design space through simulation. The approaches are literally used today, in the year 2022, to advance, develop, and integrate the 7-nm and 5-nm transistors that have been deployed for billions of users around the world in commercial products. This view and understanding of modeling transport at the nanometer scale truly enable products that impact the globe. However, transferring such modeling and simulation into the education and training of engineers who will shape the future requires more: (1) building upon, rather than rebuilding every time on the results of prior researchers, (2) duplicating the results of prior researchers, and (3) pushing the recent research knowledge into the education and training of future engineers.

nanoHUB.org offers the opportunity to researchers to share their simulation tools and results to the broader community. Anyone can contribute their own simulation tools and results into nanoHUB to enable duplication of research results and to infuse these results into further use. We utilize this capability extensively in this chapter with nanoHUB tools *Band Structure Lab* [117], *FETtoy* [160], and *OMENwire* [161] *where any reader can now duplicate the results shown here*.

nanoHUB analytics have shown that simulation tools will be adopted into the first classroom in a median time of 6 months [178]. This constitutes a rather rapid change in curricula compared with writing a new text book, which typically requires 4–6 years. As of January 2021 we have identified over 89,700 students at over 3840 classes at 185 institutions who have used nanoHUB for formal instruction in a classroom. *nanoHUB can support education!*

As of January 2021 [179], 2500+ citations of nanoHUB in the literature demonstrate that these tools are used in subsequent research. Over 30% of these papers include experimental data or an experimentalist as a co-author. nanoHUB does not just serve the computational folks, but also experimental work. The 2500 citations generated over 54,000 secondary citations, resulting in an h-index of 105. *nanoHUB can support research!*

The NEMO/OMEN team has deployed nine tools in nanoHUB over the years, which have been used by 30,700 users, as depicted in Fig. 45.21 (data as of summer 2019). These users have run over half a million simulations. The tools have been used in over 380 structured education settings or classrooms. The nine tools have been cited in the literature 112 times. All the data and figures involving the nanowire simulations in this chapter are directly generated using nanoHUB tools *Band Structure Lab* [117], *FETtoy* [160] and *OMENwire* [161].

The bottom-line message in this chapter on tight-binding is that through nanoHUB we can provide simple and rapid access to tight-binding-based physics descriptions for anyone in the world to use. We have reached a stage where users do not have to write their own tight-binding codes any more but can explore the physics and design devices. We provably reach users in education and in research with research-based, yet usable, software.

45.9 Conclusions

We have seen that the empirical tight-binding method is well-suited to modern nanodevice modeling. It is physics based, and naturally incorporates geometry at the atomic level (e.g., strain, disorder). It can successfully model both semiconductors and metals, and is efficient as it excludes core electrons; it handles varying geometries and materials easily. Its parameters represent interactions between orbitals centered on the same and neighboring atoms, and may be determined by either fitting to bulk band structures or by projection from ab initio Hamiltonians and wavefunctions. The method offers great flexibility in terms of basis orbitals and the extent of their interactions.

This flexibility in basis is responsible for one of the strengths of tight binding: its numerical efficiency. Choosing a somewhat larger atomic basis usually allows for a reduced range of interactions, often to first- or second-near neighbors. When the extent of interactions is limited in this way the Hamiltonian matrix becomes sparser, resulting in better time and memory efficiency. As a result, multi-million atom electronic structure calculations are possible on very small computer clusters, and realistic, extended nanowire and UTB transistor calculations are possible on moderately sized computer clusters.

Like all models, tight binding has challenges and limitations. Parameterization from experimental results or ab initio calculations can require significant effort. When projecting out of ab initio wavefunctions, the resulting tight-binding basis functions are not uniquely determined, so there remains some art in choosing their form. Likewise, for new materials (especially two-dimensional ones), determination of a basis that correctly reproduces the important band structure features is not easily automated; it still requires significant expertise. Finally, because the parameters depend on the interatomic potentials, parameters are generally not transferrable between dissimilar materials systems. Although these issues are different than those faced by other full-band methods, they are no worse.

Today, the method has been widely adopted in numerical simulation tools. QTBM and NEGF were established as state-of-the-art by 2004; somewhat later, the underlying materials models transitioned to tight-binding bases. The tight-binding approach coupled to QTBM or NEGF is now in wide use by academics, industrial researchers, and software vendors. Tight binding can be fed into compact-model-like approaches such as the TOB model and very rapidly deliver device trends. Many such tools are fully accessible to researchers, educators, and students on nanoHUB. The computational intensity for realistic nanodevice models is sufficiently low that NEMO/OMEN tools can be used on nanoHUB by anyone in the world.

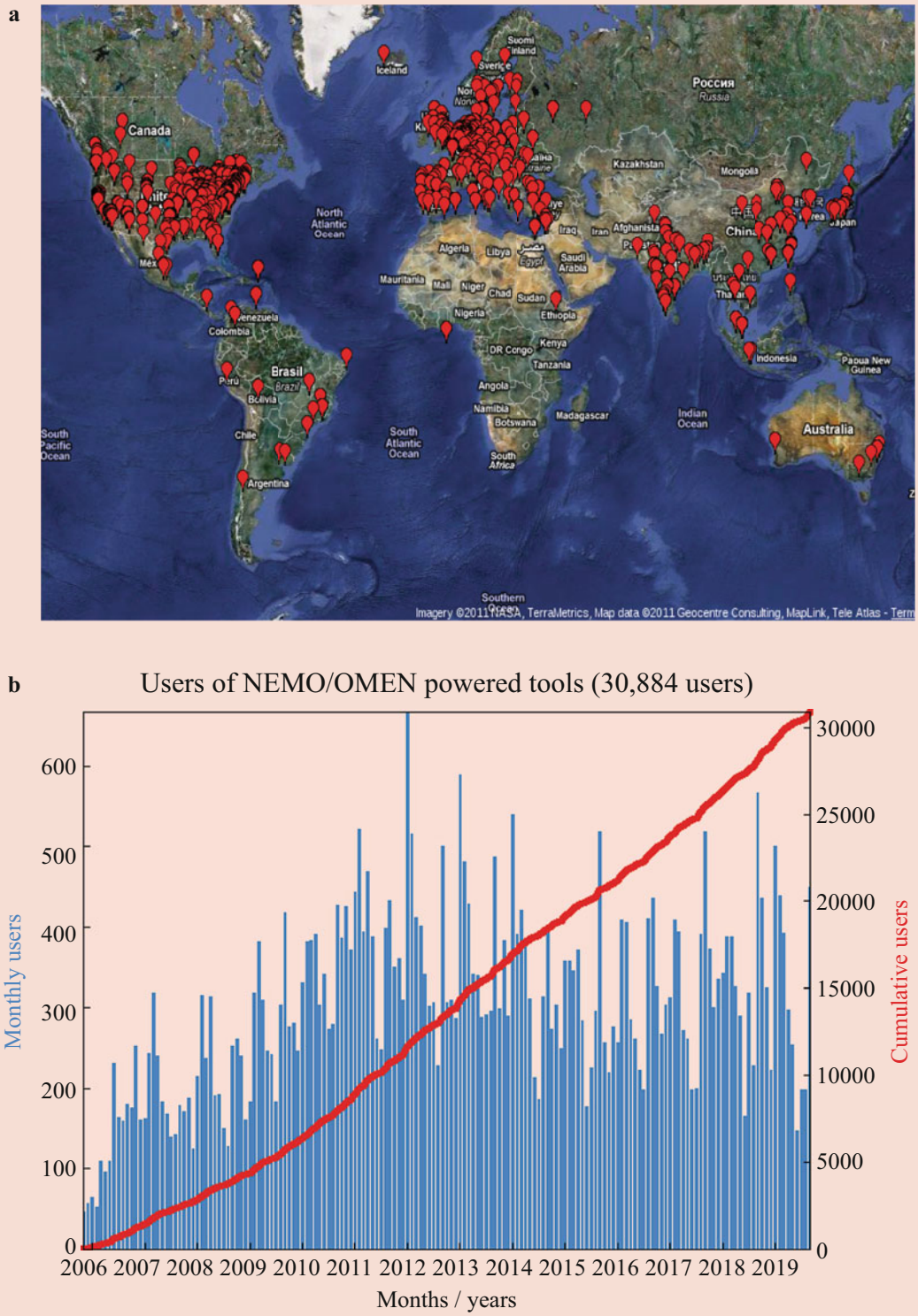

Fig. 45.21 (**a**) Global map of 30,884 NEMO/OMEN users running over half a million simulations. (**b**) Monthly and cumulative usage statistics

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Index

A
Abbe approach, 1287, 1290
ab initio calculations, 1515–1517, 1519, 1524, 1525, 1531, 1539, 1552
ab initio molecular dynamics (AIMD), for amorphous phase, 1474
Absorption-limited detector sensitivity, 769
Accelerometers, 654
Acceptor(s), 1272
  concentration, 375
Access device (selector), 1095, 1101, 1110, 1111
Access resistance, 398–401
Access transistor scaling, 49
Accumulation, condition, 334
Accuracy, 649
  estimation, 1433
AC/DC conversion, 101
ACM model, 1247
Acoustics, 1320
Acoustic-phonon, scattering, 353
Activation, 1260, 1261, 1271, 1282
  transient, 1280
  volume, 1273
Activation energy, 1273
  for conduction, 1098, 1102
  for crystal growth, 1104
  for crystallization, 1102, 1106, 1113
  for nucleation, 1104
Active electrode (AE), 1049
Active matrix array (AMA), 754
Active-pixel sensor (APS), 361
Active SPICE, models
  BJT, 1240–1243
  diode, 1239
  Fowler-Nordheim diode, 1240
  JFETs, 1250–1252
  MOSFETs, 1243
  photo diode, 1240
  SOI MOSFET models, 1247–1250
AC wafer bias, 197
Adaptive procedure, 1394–1395
Additives, 193
Adhesion, 183, 185, 192, 197, 199, 659
Adjoint analysis, 1321, 1322
Adjoint derivative, 1321, 1322
Adjoint equation, 1321, 1322, 1574
Adjoint method, 1321
Adjoint operator, 1321
Adjoint variable, 1321
Advanced concept photovoltaics, 733–740
Advanced macroscopic transport models
  ansatz-based approaches, 1362–1364
  higher order moment models, 1364–1366
  table-based parameter modeling, 1366–1368
Advancing front method, 1393
Aerial image, 1288
Affinity method, 332, 1567
Agglomerate, 204
Aharonov-Bohm effect, 1594
AIM-SPICE MOS15, 1253
Air gap, 189, 211
Air spacer, 189
Airy diffraction pattern, 282
AIST application, 1466
AlGaN/GaN heterostructures, 145
Algebraic methods, 1392
Algebraic solvers
  linear solvers, 1401–1402
  nonlinear solvers, 1398–1401
Aliasing, image sensors, 361
All-electron calculations, 1519, 1521, 1554, 1555
Alloy (doped) Cu seed layers, 208
Alloy(s)
  chalcogenide, 1452
  target, 199
  ternary, 1454
All-printed organic TFTs, 974–975
α-phase, 193
Alternating phase shift masks, 23
Aluminium, 192, 379, 385
Aluminum nitride (AlN), 536, 1526–1531
Aluminum oxide, 211
Ambipolar conduction, 885
Ambipolar effect, 374
Ambipolarity, 374
Ambipolar operation, 375
Ambipolar tunneling current, 885
Ammonia, 208
Amorphization process, 1099, 1476
Amorphous
  to crystalline transition, 1097, 1100
  OFF state, 1100, 1101, 1110
  ON state, 1100, 1101, 1110
  phase, 1098, 1099
  semiconductors, 1094, 1095, 1452–1454
Amorphous indium gallium zinc oxide (a-IGZO), 1024
Amorphous Monte-Carlo simulation, 1269
Amorphous oxides semiconductors, 961–962
Amorphous semiconductors, 159
Amorphous silicon (a-Si), 960–1452

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aMOS, 1247
Analog and RF applications, 405
Analog filtering, 358–359
  CCD, 358
Analog-to-digital converter (ADC), 685
Analytical chemistry, 1322
Analytical modeling, 1308–1318
Analytical one-dimensional multilayer models, 1263
AND
  array, 612
  logic operation, 1079
AND-OR-INVERT (AOI), 944
Anderson localization, 1595
Angular frequency, 1420
Anion generation
  acid generation efficiency, 304
  acid generator molecules, 304
  acid yield and distribution, 304
  DUV photoresists, 304
  electrons, 304
  resolution and efficiency, 304
  thermalized electrons, 305
Anisotropic etching, 1304
Anisotropic magnetoresistive (AMR) sensors, 675, 677
Annealing, 343
  furnace, 12
  process of, 12
  rapid thermal, 12
Ansatz-based approaches, 1362–1364
Anti reflective coatings, 24
Anti-ferroelectric layer (AFE), 936
Anti-fuse based memory, 83
Anti-lock braking system (ABS), 102
Anti-stokes processes, 137
Anti-stokes Raman scattering, 137
Applications, CCD, 356, 358–361, 532
Approximation
  ASCE, 337, 342
  Born, 1474
  gradual-channel, 345
  relaxation time, 1465
APS, *see* Active-pixel sensor (APS)
Aqueous-based inks, 968
Architectures, CCD, 355
ArF DUV lithography
  capabilities, 290
  capillary forces, 290
  density of transistors, 290
  hardmasks, 290
  inorganic Si-ARC layer, 290
  isotropic etching, 288
  LELE approach, 288
  organic layers, 290
  pattern deformation, 290
  patterning procedures, 288
  plain photoresist, 290
  plasma etching, 288
  residual mechanical stress, 290
  spacer deformation, 290
  spacer technology, 288
  Young's modulus, 290
Argon, 193, 197
  sputter gas, 196
  Armchair-edge graphene nanoribbons (aGNRs), 1539, 1540, 1542–1544, 1550
Armchair-edge graphene nanoribbons field-effect transistors (aGNRFETs), 1549, 1551
Arrhenius law, 1273, 1285
Artificial annealing, 1203
Artificial intelligence (AI), 1044
Artificial neural networks (ANNs), 1087, 1172
Artificial surface, 1323
Artificial synapses, 1169
ASCE approximation, 337, 342
a-Se, 757
  based x-ray detectors, 766
  detectors, 759, 767
Ashing, 186
a-Si:H, photoconductivity, 1452
ASIM, 1247
Aspect-ratio-trapping (ART), 268
Assembly, 650
Asymmetric double-gate device, 380
Asymptotic
  boundary conditions, 333
  concentrations, 333
Atom probe tomography (APT), 152
Atomic force microscopy techniques, 152
Atomic layer deposition (ALD), 19, 564, 888, 965, 1077, 1296
Atomic layer etching, 21
Atomic structure, of chalcogenides, 1454–1456
Atomically smooth, 890
Atomistic simulators, 1283
Attempt-to-escape frequency, 1473
Attenuated phase shift masks, 23
Attenuation(s)
  CCD, 359
  depth, 759
Audio amplifier, 83
Auger analysis, 206
Auger generation/recombination, 882
Auger recombination, 706
Automated process control (APC), 248
Automotive applications, 1096, 1105, 1116
Automotive micro-sensors, 638–640
Avalanche breakdown, 780
Average
  energy flux of carriers, 1462
  energy of carriers, 1462
  velocity of carriers, 1462, 1465
Axicon-like metalens, 1324

B

Back-barrier selection, 528–529
Back end of line (BEOL), 180, 192, 1069
  damascene, 170
  integration, 170
Back gate, 379, 380, 384
Backplate, 668
Back surface field (BSF), 709
Backpropagation (BP), 1083, 1169, 1175, 1178, 1183, 1187, 1190
Backscattering, 11
Backside illuminated structure (BSI), 688
Backward differentiation formulas (BDF), 1384, 1385
Balance equation, 1426–1429, 1460
  current, 1428, 1431
  energy, 1428
  energy current, 1428
  energy distribution function, 1418

Baliga's figure-of-merit (BFOM)
power devices, 432
for semiconductors, 493
Ballistic conductor, 1585
Ballistic rectifier (BR), 838–842
ballistic formalism, 839–840
electrical characteristics, 840
perspectives, 842
THz BR detection, 841
Ballistic transport, 838, 1519, 1534, 1546, 1547, 1549, 1551, 1622–1623
Band alignment, 372, 1028, 1029
Band bending, 373
Band diagram, 378
Band edge, 893
steepness, 893
Band gap, 371–373, 382, 718, 725, 811, 828–831, 859, 1605
Band-modulation FET, 381, 384
Band renormalization, 853
Band states
dispersion of, 1464
of parabolic type, 1464
Band structure, 852, 870, 1342, 1492–1497, 1499, 1501, 1502
Band tails, 893–896
Band-to-band tunneling (BTBT), 268, 373, 376, 380, 382, 869, 870, 1432, 1434, 1526
Barber poles, 678, 679
Barrier height, 374
Barrier layer, 192
Barrier lowering, drain induced (DIBL), 353
Barrier width, 374
Base-collector insulators (BCI), 916
Basic semiconductor equations, 1340
BBT, *see* Band-to-band tunneling (BBT)
Beam quality, 858
Bending contours, 132
Berkeley Short-channel IGFET Model, 1244–1245
Bias-induced doping, 372, 379–380, 385
lateral p-n junction, 380–381
vertical p-n junction, 381–382
Biasing scheme, 54
Bias power, 198, 204
Bias stability, 662
Bias temperature instability (BTI), 270
Bi-directional field effect transistor, 517–518
Bi-layer defect, 124
Bilayer deposition, 193
Bilayer TFET, 882
Binarized-neural-networks (BNNs), 1087
Binary collision approximation, 1268, 1269
Binding energies, 193
Biocompatibility, 1026
Biodegradable batteries, 1032
Biodegradable cellulose substrates, 1021
Biodegradable electronics, 1027, 1038
Biodegradable materials, 1020
Biodegradable natural plastics, 1020
Biodegradable polymers (BP), 1020
Biodegradable powering devices, 1033
Biodegradable sensors, 1029
Biological processes, 1020
Biological sensing
current mainstream biosensing technologies, 1004
fully integrated CMOS biosensor, 1007–1009
heterogeneously integrated biosensor, with disposable electrodes, 1009–1011
impedance-based immunosensor, 1011–1013
semiconductor technologies, 1004–1007
TFT-based biosensors, 1013–1015
Bioresorbable pressure, 1031
Biorthoganolize, 1329
Bipolar action, 374
Bipolar CMOS (BiCMOS), 829, 833–838
Bipolar, CMOS and DMOS (BCD) technology, 67
application evolution, 81–109
architecture, 72–83
development challenges, 107–112
platforms, 69–74
power ICs, 69
Bipolar electrochemical metallization, 1046
Bipolar junction transistor (BJT), 376, 379, 588, 826–830, 1240–1241
Ebers and Moll BJT model, 1241
Gummel-Poon BJT model, 1241–1242
HiCUM, 1242–1243
IGBT, 1243
MEXTRAM, 1242
model, 987, 990
VBIC vertical BJT model, 1242
Bipolar transistors, 376, 826
common-base configuration, 594–595
configurations, 590
cut-off region, 595–596
DC operations, 590
output characteristics, 595
principle of operation, 589–590
structure, 589
Bipolar-type behavior, 375, 376
Bipolar-type conduction behavior, 375
Bistability, 1453
Bit lines (BL), 1069
Black phosphorous (BP), 315, 790
Bloch sphere, 1206
Bloch's theorem, 1606
Blocking voltage, 536
Blooming, 363
image sensors, 363
Bløtekjær's approach, 1351, 1352
Body-centered cubic (bcc), 193
Body effect, 346
Body factor, 868, 899
Body region doping profile, 87
Body thickness, 890
Bolometers, 782–783
Bolometric effect, 781
Boltzmann approximation, 376
Boltzmann constant, 333
Boltzmann distribution function, 1567
Boltzmann equation, 1318
Boltzmann method, 1594
Boltzmann scattering, 1563
Boltzmann transport, 1267
Boltzmann transport equation (BTE), 1336, 1341–1342, 1360, 1414–1415, 1417, 1422, 1427, 1445, 1516, 1528, 1531, 1563, 1567
small-signal BTE, 1420
Boltzmann's constant, 808, 1339
Bond(s)
alignment, 1103
in chalcogenides, 1454

Bonding
metavalent, 1455
pads, 105
structure, 187
Boolean computing, 948
Boolean logic computing, 1082
Born approximation, 1474, 1595
Born rule, 1560
Boron-interstitial clusters (BICs), 1282
Boron nitride, 191
Bose-Einstein distribution, 137
Bottom anti-reflective coatings, 24
Bottom electrode (BE), 1044, 1181
Bottom port, 668
Bottom-up, 890
Bound, electronic states, 1468
Boundary conditions, 1384, 1388, 1593
asymptotic, 333
distribution function, 1415
Ideal Ohmic contact, 1431
Neumann-type, 1431
Bounded continuous mapping operator, 1320
Bounded inverse, 1320
Box integration method, 1442
β-phase, 193
Bragg diffraction, 118
Bragg mirrors, 795
Bragg's law, 130
Brain-computer-interfaces (BCI), 625
Brain-inspired neural networks, 1174
Branch point, 872
Bravais lattice, 123
Bread loafing, 195, 199, 202
Breakdown, 185
strength, 191
voltage, 205, 534
Brillouin zone, 1605
Broadband solar spectrum, 723
Broadening functions, 1589
Broken gap, 886, 891
BSIM-CMG model, 1249
BSIM-SOI, 1248–1249
BSIM2, 1243–1245
BSIM3, 1243, 1245
BSIM4, 1245
BSIM6, 1245
Buffer leakage, 534
Built-in potential, 581–582
Bulk
charge per unit area, 336
contact, 332, 343
resistivity, 713
Si CMOS, 310
simulation, 1366
unstrained semiconductors, 1493–1495
velocity, 1368
Bulk-recombination, 1274
Bulk transconductance, 347
in MOSFETs, 347, 351
Burgers vector, 119
Buried-channel, CCD, 355
Buried oxide (BOX), 260
Buried-recessed access device (BRAD), 48
Butler-Volmer equation, 1051, 1066

C
Calibration, 653
Cambridge's TFT model, 977
above-threshold model, 977–979
subthreshold model, 979, 980, 982
CAMCAS model, 985
Cameras, 643
Cap dielectric constant, 204
Cap film, 204
Cap-layer deposition process, 172
Capacitance, 171, 187, 189, 190, 204
distribution, 544
reduction, 184, 187
Capacitance matching condition (CMC), 934
Capacitance per unit area
at flat band, 337
of semiconductor, 336
of the oxide, 334
Capacitance-voltage (C-V) measurements, 149
Capacitive, 638
MEMS gyroscopes, 662
MEMS microphones, 668
model of FG MOSFET, 51
Capacitor, 1235
chip, 1236
CPW, 1236
metal-insulator-semiconductor, 332–336
MOS, 332, 334, 342
with frequency-dependent capacitance, 1236
Capillary action, 203
Capillary effect, 203
Capping, 172
Carbon, 161, 1304
Carbon doped oxide, 182
Carbon nanotubes (CNTs), 311, 315, 316, 372, 374, 380, 381, 384, 1470
band structure, 921
CMOS and integrated digital circuits, 922–925
dispersion relation, 923
electrodes, 1106, 1116
TFETs, 897
Carbon-based tunnel FETs, 320
Carbon-doped buffers, 529
Carbon-fluorine-hydrogen (CxFyHz), 225
Carbonyl-based precursor, 209
Carrier
average energy flux, 1462
average velocity, 1462, 1465
concentration, 1462
confinement, 855
contact solar cells, 717
flux equation, 1462
injection, 855
mobility, 1340
scattering, 853
selective contact, 717
temperature, 1103
thermalization, 879, 892
Cascaded linear system model, 768
Cascode circuit, 539
Cassie-Baxter wettability, 1322–1324
Cathode fall, 195
Cathode luminescence (CL), 127
Cathode-ray tubes, 354

Cauchy relation, 160
Cauchy-Schwarz inequalities, 1388
Cavity quantum electrodynamics (cQED), 1210
CCD, *see* Charge-coupled device (CCD)
CdTe, 751
CdZnTe, 751, 757
Cell, mushroom-like, 1470
Cell-removal, 1293
Cellulose-based films, 1020
Central implant MOSFET (CI-MOSFET), 510
Central processing unit (CPU), 1146, 1168
Chalcogenide, 85
  alloys, 1452
  atomic structure, 1454–1456
  bonds, 1454
  electronic states, 1454, 1456–1457
  photonics, 1452
  short-range order, 1454
  sp_3 hybridization, 1455
  ternary, 1454
  transport, quantum models, 1473–1477
Chalcogenide alloys
  band diagram, 1098
  density of states, 1098
  doping, 1116, 1117
  electrical properties of, 1097
  Fermi level, 1098
  Ge enrichment, 1116, 1117
  growth dominated, 1105
  nucleation dominated, 1105
  optical properties of, 1097
  switching of, 1096
  technological properties of, 1116
  ternary diagram, 1096
Channel, 1584
  length, 343
  in MOSFET, 343
  well formed, 343
  width, 343
Channel hot-electron injection (CHEI), 1170, 1172–1174, 1176
Channeling, 1262, 1264, 1269
Chaotic advection, 1322
Charge
  carrier concentration, 372
  carrier density, 371
  collection, 769
  neutrality point, 782, 797
  packets, CCD, 359
  partitioning, in MOS capacitors, 365
  per unit area, 334
Charge-coupled device (CCD), 354, 681
  analog filtering, 358
  applications, 356, 358–361
  architectures, 355
  attenuations, 359
  buried-channel, 355
  charge packets, 359
  clock, 355, 359
  convolution, 359
  duty cycle, 360
  dynamics, 362
  floating diffusion, 362
  Fourier transform, 359
  input circuit, 362
  integration period, 359
  linear sensors, 359
  linearity, 359, 363
  noise, 362
  optical sensing, 359
  output circuit, 362
  parallel-to-series-conversion, 360
  phases, 354, 359
  resolution, 361
  sampling, 359
  surface-channel, 355
  three-phase, 355
  transfer function, 359
  transfer inefficiency, 356, 363
  two-dimensional, frame-transfer, 360
  two-dimensional, line-transfer, 360
  two-phase, 355
  video interlacing, 361
Charge-coupled silicon powder MOSFET, 496
Charge-coupling concept, 440
Charge-injection device (CID), 354, 356–357
  floating gate, 357
  performance, 357
Charge plasma concept, 379
Charge plasma device (CP device), 372, 378–379
Charge plasma diode, 378
Charge plasma p-n junction diode, 378
Charge qubit, 1211
Charge storage solutions, 52
Charge transfer devices (CTD), 354
  CCD, 354–356
  CID, 356–357
  floating-gate operation, 357–358
  transfer efficiency, 356
Charge transport models, for amorphous chalcogenides
  amorphous semiconductors, 1452–1454
  atomic structure and electronic states, 1454–1458
  macroscopic models, 1476–1485
  microscopic models, 1461–1477
  physical models and numerical approaches, 1458–1461
Charge-trapping, 555, 556
Chemical amplification, 295
Chemical doping, 371, 372, 374, 383
Chemical mechanical planarization (CMP)
  barrier/setting, 247, 248
  chemicals, 241
  Co liner, 250, 251
  copper, 242, 243
  copper inhibitor, 244–246
  definition, 239
  delamination, 248
  dendrites, 249
  metal voids, 249
  overburden, CU, 243
  oxidizer, 243
  pad, 240
  polish, 239, 240
  RU liner, 249
  scratches, 248
  slurry, 239
  STI, 242
  tool, 239
Chemical-mechanical-planarization (CMP), 170

Chemical mechanical polishing (CMP), 74, 192, 260
planarization, 20
Chemical vapour deposition (CVD), 18, 199, 209, 229, 877, 965, 1023
co wetting layers, 201
wetting layers, 203
Chemically amplified resists (CARs), 291
Chemoepitaxy, 28
Chip, 366
capacitor, 1236
Chip-package-interaction (CPI), 186
Chiral angle, 921
CID, *see* Charge-injection device (CID)
Circular transmission line model (C-TLM)
carrier lifetimes, 151, 152
carrier profiling, 150
definition, 148
differential capacitance, 150
Hall scattering factor, 150
ionization energy of the dopant, 149
mobility, 151
net doping density, 150
semiconductor charge, 150
sheet resistance, 149
SIMS measurements, 149
structure, 148
temperature dependent measurements, 149
test structures, 148
total resistance, 148
Circulatory force, 1313
Citric acid, 1022
Classical macroscopic device simulation
advanced macroscopic transport models, 1362–1367
applications, 1367–1376
drift-diffusion and energy transport models, validity for, 1355–1362
energy transport models, 1349–1355
history, 1336
macroscopic transport models, 1345–1349
microscopic transport modeling, 1341–1345
phenomenological drift-diffusion model, 1338–1341
Clock, CCD, 355, 359
Closed loop, 655
Closure problem, 1346, 1356
Clusters, 1280, 1281, 1481
boron-interstitial, 1282
CMOS image sensors (CIS), 681
CMP pad
conditioner, 240
definition, 240
wafer carrier, 240
wafer cleaning, 240, 241
wafer drying, 241
CNOT gate, 1207
CNT-TFET, 380
Coalesce, 194, 199
Cobalt, 199, 232, 379
Co cap, 209
Coherence, 1208
Coherent transport, 1590, 1594
Cold Maxwellian, 1344
Co liner, 209
Collection efficiency, 761
Collection probability, 711
Collective oscillations, 1324
Collimated sputter deposition, 195
Collimator, 196
Collinear four-point probe configuration, 144
Collisional ionization, 195, 197
Colloidal quantum dots (CQDs), 730
Color filter, 685
Coloring problem, 21
Common-base configuration, 594–595
Common-collector configuration, 592–594
Common-emitter amplifier, 596–597
Common-emitter configuration, 590
Compact discs (CDs), 862
Compact model coalition (CMC), 394
Complementary FET (CFET), 33
CMOS, 272
definition, 271
pMOS, 272
Complementary metal oxide semiconductor (CMOS), 372, 383, 681, 687, 834–838, 860, 942, 962, 987, 990, 991, 994–997, 1001, 1006, 1007, 1009, 1011, 1035, 1045, 1167, 1169, 1170, 1173, 1178, 1182, 1184, 1189, 1191, 1304, 1305
detectors, 838
emitters, 836
perspectives, 838
semiconductor-on-insulator formation, 33
stress engineering, 34
technology, 371, 372
transistor process, 1070
Complex band(s), 870, 872, 1610–1611
Complex gate dielectrics, 897
Compliance mechanism, 1320
Complimentary III-V TFET logic, 888
Complimentary metal-oxide-semiconductor (CMOS), 1124
Compositional segregation, 1113
Compostable materials, 1020
Compostable sensors, 1037
Compressive air test, 671
Computational fluid dynamics, 1292
Computer aided design (CAD), 975, 977, 1305
Computer software, 17
Concentration
asymptotic, 333
of carriers, 1462
distribution, 1323
Concurrent multi-scale modeling, 1432–1437
Condensation rate, 1481
Condition of stability, 1313
Conductance
of drain, 346
output, 346
slope, 893, 894
Conductance, differential, in MOSFETs, 346, 350
Conduction
band, 373
band edge, 1493
electrons, 1324
trap-limited, 1460
Conductive atomic force microscopy (CAFM), 153, 1046
Conductive-bridge random access memory (CBRAM), 604, 1045, 1046, 1051, 1184
Ag nanoparticles, 1049
CF, 1049, 1061, 1067, 1068
chemical reactions, 1063
experimental data, 1066
growth dynamics, 1052, 1053
HRS/LRS, 1063, 1065
IE, 1051
material parameters, 1052
Monte Carlo simulation, 1061

performance evaluation, 1068
physical effects, 1051
resistance network, 1066
resistive switching, 1052
Conductive filament (CF), 1045, 1181
Conductivity
amorphous semiconductors, 1452
GST–225, 1476
Confined cells, 1107
Confined structures, 1496–1498
Conformality, 195
Conformal spacer dielectric, 177
Conservation laws, 1349, 1384
Constant-field scaling rules, 366
Constant-voltage stress, 565
Constitutive law, 1308
Consumer market, 640
Contact, 1584–1586, 1593
angle, 1323
approaches, 717
bulk, 332, 343
drain, 343
gate, 332, 343
noise, 763
resistance, 371, 909–910, 988–989
source, 343
Contact etch stop layers (CESL), 260
Contact-minimized cells, 1107–1110, 1115
μ-trench, 1108, 1115
matchstick, 1108
ring, 1108
wall, 1108, 1110
Contacted poly pitch (CPP), 260, 263
Contactless eddy current measurements, 145
Contamination, 671
Content addressable memories (CAMs), 947
Continuity equation, 1338
Continuum approaches, 1283
Continuum models, 1604
Control gate, 374, 384
Controlled sources (CC), 1237
Convective energy, 1347, 1356
Conventional computing system, 1077
Conventional solar cells, 705–719
Conventional TEM (CTEM)
Burgers vector, 119
dislocations, 119, 120
microscopes, 121
SFs, 119, 120
simulation of GaAs, 121
uses, 119
Conversion noise, 763
Convolution, CCD, 359
Convolutional neural networks (CNN), 622
CoolCube™, 34
Cooper pair tunneling, 1210, 1211
Copper-alloy seedlayers, 199
Copper electroplating
applications, 229
BEOL processing, 229
BEOL yield/reliability, 233, 234, 236–238
chemistries, 230–232
CVD, 237–239
extendibility, 236, 237
planarization, 232
SEM, 230
tooling, 232
topography, 230, 234
Copper hillocks, 206
Copper-low k Interconnect, 180
Copper damascene interconnects, 192
Copper diffusion, 206
Copper interconnect, 31, 192
Copper line wiring, 170
Copper Re-Distribution Layer (*RDL*), 79
Copper seed, 199
Copper seed layer, 171, 198
Copper sputtering, 193
Copper sulfate, 193
Core-shell nanowires, 890
Coriolis force, 660
Coriolis vibratory gyroscope (CCVG), 663
Correlated double sampling (CDS), 686
Corrosion, 192, 674
Cosine dispersion, 1588
Couette flow, 1318
Coulomb energy, 1212
Coulomb interaction, 853, 1467
Coulomb potential, 1563, 1593
Coulomb scattering, 853
Coupled-oscillator-based processing, 948
Coupling qubits, 1213
Co wetting layer, 209
CP-TFET, 384
CPW capacitor, 1236
Crank-Nicholson method, 1468
Critical dimension (CD), 171, 186, 295, 1290, 1296
Cross-linking bonding, 182
Cross-point array, 1095, 1110–1112, 1116
Crossbar RRAM array, 1071
Crosspoint RRAM array, 1070
Cryogenics, 9
Crystal orientation, 1603
Crystal symmetry, 1603
Crystalline
to amorphous transition, 1101
Monte-Carlo simulation, 1269–1270
Crystallization, 613, 1114, 1472
of PCM, 1479
probability, 1114
process, 1106
speed, 1105, 1106
stochastic, 1105
temperature, 1099, 1105, 1113
CSIM, 1247
CTD, *see* Charge-transfer device (CTD)
Current, 1584, 1586, 1590
amplification, 375
difference, 1069
leakage, 205
operator, 1587
source converter, 424
swirls, 1476
Current aperture vertical electron transistor (CAVET), 546, 566
operation principle, 548
review, 548
Current-continuity equation, 584–585
Current-strapping, 192
Current-to-voltage converters, 1069
Current-voltage characteristics, 343–350, 1099, 1103, 1111
Current-voltage (I-V) measurements, 146
Current-voltage relation, 978–979

Cut-off distance, 1469
Cut-off frequency, 1002
Cut-off region, 595–596
Cyclic deposition, 208
Cyclic process, 209
Cycling endurance, 1113–1114
Cycloidal orbits, 195
CYTOP, 974

D
Damaged layer, 186
Damascene, 170, 229, 231
  aluminium, 203
  interconnect structure, 197
  metal processes, 31
  thick copper, 79
Damping coefficient, 1311
Dangling bonds, 875, 890
Dark current, 706, 707
Data cube, 127
Data line noise, 765
Data retention, 1105, 1112–1113, 1115, 1116
Dataset, 127
DC magnetron, 194
DC operation, 590
De-ionized (DI) water, 1022
De-trapping kinetics, 558
Deal-Grove model, 1284
Debye-Waller factor, 160
Debye length, 877
Decamethylcyclopentasiloxane, 182
Decoupling, 1613, 1614
Deep level acceptors, 891
Deep level transient spectroscopy (DLTS), 152
Deep neural network (DNN), 1086, 1169, 1178, 1181
  with memristive devices, 1186
Deep trench isolation (DTI), 70
Deep-UV (DUV), 279, 284
Defect(s), 875, 886, 1375
  annihilation, 1115
Defocus, 1287
Deformation potential, 1516–1519, 1523, 1524, 1526, 1530, 1553
  theorem, 1517
Degas, 197
Degenerately doped source, 884
Degradable metals, 1024
Degradation mechanisms, 566
Degradation of contrast, image sensors, 362
Delamination, 1113, 1114
Delaunay criterion, 1393
Delaunay tessellation, 1442
Delay time, 1100, 1103
Dense SiCOH, 184
Density-functional perturbation theory (DFPT), 1516, 1522–1524, 1527, 1553
Density functional theory (DFT), 1457, 1516, 1519, 1520, 1523–1527, 1529–1532, 1535, 1538, 1539, 1541, 1552–1555, 1576
  in chalcogenide transport, 1474
Density matrix, 1206
Density method, 1320
Density of states (DOS), 893, 1098, 1103, 1456, 1497, 1584, 1589, 1593, 1626
  band tails DOS, 895, 896
  function, 1430
  modulation, 873
  switching, 873, 894
Dephasing, 854, 1590–1591, 1594
Depleted, region, 336
Depletion layer width, 432
Depletion mode MOSFET, 425
Depletion regime, 334, 335
Depletion type, MOSFETs, 347, 351
Depletion width, 334, 335, 582, 870
Depolymerization, 1020
Deposition, 17, 1291–1295, 1297
  atomic layer deposition, 19
  chemical vapor deposition, 18
  molecular beam epitaxy, 19
  physical vapor deposition, 17
  rate, 195
  sequences, 197
Depth of focus (DOF), 239, 284
Descent direction, 1321
Design domain, 1323, 1326
Design variable, 1320, 1322
Design-technology co-optimization (DTCO), 261, 1290, 1298
Detailed balance, 723
Detective quantum efficiency (DQE), 767
Detectivity, 779
Detector, 819, 820, 823–826, 836–842
Detrapping
  due to e-e interaction, 1467–1469, 1480
  probability, 1468
Device architectures, 1106
  figures of merit, 1110
Device/circuit hybrid modeling, 542
Device modeling calibration, 543
Device under test (DUT), 994
Dewetting, 204
DFT, *see* Density functional theory (DFT)
Diamagnetic levitation, 1310
Dicing, 444
Dielectric, 1026, 1324
  barrier cap, 211
  barrier film, 204
  breakdown, 192
  capping layer, 199
  constant, 182, 186, 190, 204, 207
  function, 1541–1545
  high-k, 332, 367
  isolation, 70
  layer, 172
  permittivity, 1338, 1541, 1543–1545
  stack, 171
Dielectric cap, 185
  first generation, 205
  low k ultra thin, 207
  low k value, 206
  oxidation barrier test, 205
  requirements, 205
  second generation, 205
  selective cobalt, 208
Dielectric-semiconductor interface, 1028
Diethoxymethylsilane (DEMS), 182
Differential conductances, in MOSFETs, 346, 350
Differential equations (DE), 1308
Differential Hall effect (DHE), 149, 151
Differential methods, 1392
Differential operator, 1384

Differential resistance, negative (NDR), 1469, 1479
Diffraction-limited, 1324
Diffraction pattern (DP), 118
Diffusion, 199, 203, 1261
  approximation, 1349–1350
  barrier, 190, 192
  cap, 184
  coefficient intrinsic, 1273, 1277
  current, 1339
  high concentrations, dopant diffusion at, 1278–1279
  implantation-enhanced, 1280, 1281
  macroscopic diffusion behavior of dopants, 1275
  oxidation-enhanced, 1280
  oxidation-retarded, 1280
  and reaction mechanisms, 1273
  scaling, 1350
  surface processes on dopant diffusion, 1279–1280
  tensor, 1423
  transient, 1280–1281
Diffusion-barrier, 192
Diffusion-limited reactions, 1275
Diffusion-reaction equations, 1275, 1283
Diffusive Maxwellian, 1344
Diffusive spin transport, 1591–1592
Digital circuits, 906, 923, 924
Digital computers, 62
Digital logic design, 941
Digital micro-fluidics, 1310
Digital power management, 83
Digital twin, 1304
Digital versatile discs (DVDs), 862
Digitline capacitance, 45
Dill model, 1290
Dilute hydrofluoric acid (dHF), 220, 221, 225
Dimethyl silacyclopentane, 207
Diode, 916, 918–921, 1239
  laser, 855
Dirac point, 907
Dirac spinor, 1206
Directed self-assembly, 28–29
Directional sputter deposition, 195
Directional sputtering, 193
Direct transmission methods, 1612–1614
Direct tunneling, 871, 872
Dirichlet boundary condition, 1443
Dirichlet conditions, 1384
Dirichlet data, 1389
Discontinuity models, 1238
Discrete empirical interpolation method (DEIM), 1328–1330
Discrete output sequence, image sensors, 361
Discrete power MOSFETs, 492
Discretization, 1384
  error, 1393–1394
Discretized design objective, 1329
Dislocations, 556
Dispersion
  of band states, 1464
  relation, 1589
Dissolution mechanisms, 1036
Dissolution rates, 1034
Dissolvable medical devices, 1026
Distance, cutoff, 1469
Distortion, of the Peierls type, 1455
Distributed Bragg reflector (DBR), 856, 861
Distributed feedback, 856
Distribution
  dopant, 1261
  distribution function, 1261, 1341, 1414, 1415, 1462
  lateral, 1266
  Maxwell–Boltzmann, 1429
  Pearson, 1262, 1263, 1266
  vertical, 1261
Disturb
  proximity, 1115
  read, 1112, 1114–1115
  thermal, 1112, 1115–1116
Domain decomposition, 1290
Donor(s), 1272
  concentration, 375
  energy, 531
Dopant(s), 1260, 1274
  activation, 16
  distribution, 367, 1260–1262, 1265, 1266, 1296, 1297
  fluctuations, 890
  high concentrations, dopant diffusion at, 1278
  inhomogeneity, 893
  macroscopic diffusion behavior of, 1275
  pockets, 877, 878
  surface processes on dopant diffusion, 1279
Dopant-based qubits, 1208
Doped silicon nanomembranes, 1030
Doping, 1338
  pocket, 879
Doping-less TFET, 379, 382
DOS, *see* Density of states (DOS)
Double gate, 877
Double gate MOSFET, 393, 395, 406, 1371
  drain current, 1371, 1372
  numerical properties, 1372
  predictiveness, 1371
  velocity, 1371
Double patterning (DP), 175, 288
Double pulsed measurements, 557
DOUST, 1247
Downscaling, 1106, 1115
Drain, 1584
  contact, 343
  extension region, 92
Drain conductance, in MOSFETs, 346, 354
Drain-controlled vertical leakage, 570
Drain current, 1370–1372
  in MOSFETs, 352
  transient (DCT), 556
Drain-induced barrier lowering (DIBL), 312, 353, 1622, 1623
Drift current, 979, 1339
Drift-diffusion, 373, 376
  equation, 1102
  model, 542, 1336, 1338–1341, 1349, 1360, 1385–1386, 1431–1432, 1437–1445
Drift energy, 1356
Drift velocity, 352, 810, 811, 813, 814, 1524, 1528–1530, 1533, 1535–1537
  saturation of, 352–354
Drive, 660
Drude model, 160
Dry etch, 20
Dual damascene, 170, 193
  trench first process flow, 173
  via first process flow, 173
Dual grid, 1443
Dual inlaid, 170

Dual material gate, 885
Dual pairing, 1321
Dual phase material, 185
Dumbbell Nebula, image sensors, 363
Duty cycle, CCD, 360
D-wave systems, 1203
Dye-sensitized solar cell (DSSC), 728
Dynamic(s), 362
  CCD, 362
  Monte-Carlo simulation, 1270
  nonlinear sources, 1238
  R_{ON} issues, 534
  temperature, 1428, 1430
  viscosity, 1318
Dynamic high-temperature operation life (D-HTOL), 571
Dynamic random access memory (DRAM), 41, 427, 1145, 1168
  access transistor scaling, 48–49
  capacitor scaling, 46–48
  cell, array and operating principles, 44–46
  product evolution, 49–50
  technology evolution, 46
Dynamic range (DR), 682
Dynamic response of PCM, macroscopic models, 1479–1481

E
Ebeam lithography, 1324
Ebers and Moll (EM) BJT model, 1241
E-compass, 675
Eddy current, 1312
Edge-averaged FE (EAFE), 1390
Edge currents, 1594
Edge placement error (EPE), 295
e-e interaction, detrapping, 1467–1469, 1480
Effective density of states, 373, 1430
Effective electron mobility, 344
Effective mass, 811, 1492, 1494, 1495, 1498, 1502, 1509, 1510
Effective-mass approximation (EMA), 1492
Effective-mass formula, 1609
Effective mobility, 344, 350, 353
Effective normal field, 353
Effective oxide thickness (EOT), 877
Effective scaling, 868
EHB-TFET, 382, 384
Eigensystem, 1307
Eigenvalues, 1584
Eight-band $\boldsymbol{k} \cdot \boldsymbol{p}$ model
  bulk unstrained semiconductors, 1493, 1495
  confined structures, 1496–1498
  strained semiconductors, 1495–1496
EIM, 1328–1330
Einstein oscillator model, 160
Einstein relation, 1339, 1388, 1423, 1428, 1431, 1465
EKV2.6, 1246
EKV3, 1247
Elastic modulus, 183, 185
Elative dielectric value, 189
Electrical activation, 1271
Electrical conversion efficiency, 702
Electrical dissipation function, 1309
Electrical dissolution rates (EDR), 1022, 1024
Electrical engineering (EE), 1604, 1605
Electrical profiling techniques, 151
Electric field, 371, 372, 379, 1325, 1385, 1415
Electric fuse based memory, 83
Electric length, of gate, 343
Electric levitation, 1310
Electric response, time resolved, 1464
Electrochemical dissolution, 1034
Electrochemical metallization cell (ECM), 1046
Electro-chemical method, 1065
Electrochemical potential, 1593, 1594
Electrochemical potential difference, 1584
Electrocorticography (ECoG) recording system, 1030
Electrodes, 656
Electroless deposition, 208
Electrolytic plating, 193
Electromagnetic coupling Hamiltonian, 1609–1610
Electromagnetic levitation, 1308
Electromagnetic levitation micro-systems
  dynamics of, 1313
  stability of, 1313–1314
Electromagnetics, 1324
Electromagnets, 197
Electromigration (EM), 31, 79, 193, 199, 201, 204, 207–209, 1113
Electromigration activation energy, 201
Electron affinity, 332, 372, 383
Electron and hole pair (EHP) creation energy, 750
Electron beam (EB) resists, 30, 183
Electron-beam induced current (EBIC), 127
Electron beam lithography (EBL), 29, 120, 279, 293, 294
Electron beam–specimen interaction, 122
Electron confinement, 1602
Electron-continuity equation, 340
Electron current density, 1427
Electron density, 1427, 1584, 1586, 1589
Electron-electron interactions, 1590
Electron energy current density, 1427
Electron energy density, 1427
Electron energy loss spectroscopy (EELS), 118, 123, 125, 127–129
Electron-hole bilayer (EHB), 372, 381–382
Electron-hole bilayer TFET (EHB TFET), 877
Electron-hole pair, 724, 853
Electron-hole-plasma, 853
Electronic design automation (EDA) tools, 394
Electronic models, 1102–1103
Electronic states
  bound, 1468
  extended, 1468
  of chalcogenides, 1454, 1456–1457
Electronic stopping, 5, 1263, 1268
Electron mobility, 543
Electron-phonon interaction, 1516, 1517, 1519, 1521–1523
Electron-phonon matrix element, 1517, 1518, 1522–1524, 1526, 1533–1535, 1540, 1553
Electron-phonon scattering rates, 1516, 1519, 1524–1527, 1552
  AlN, 1528, 1530, 1531
  GaN, 1527, 1528
  germanene, 1535, 1537, 1540
  graphene, 1519, 1520
  phosphorene, 1533, 1534
  Si, 1519, 1525, 1526
  silicene, 1535, 1537, 1540
Electrons, 195, 1338
Electrophysiology (EP) biosensor, 1030
Electroplating, 192, 193, 199, 203
Electrospun, 1022
Electrostatically doped device, 372
Electrostatic coupling, 381
Electrostatic doping, 371–372, 378, 382–383
  bias-induced doping, 379–382
  CMOS, 383–384

limitations and drawbacks, 384–385
Schottky barrier based devices, 372–375
workfunction-induced doping, 375–379
Electrostatic potential, 1593
Electrostatics analysis equilibrium, 579–583
Electro-thermal instability, 1102
Elliott-Yafet spin relaxation mechanism, 1140
Ellipsometer apparatus, 158
Ellipsometric angles, 158
Ellipsometric measurement, in a-GST, 1458
Elliptic band structures, 872
Embedded-PCM, 1096, 1105, 1116
Embedding, 1320
EM induced mass flow, 208
Emission microscopy, 569
Emitter, 814, 816, 818–823, 836–838
Emitter-base insulator (EBI), 916
Emitter-push effect, 1279
Emitter switched thyristor, 476–477
EM lifetime distribution, 209
Empirical orthogonal tight-binding (ETB), 1605
Empirical pseudopotential method, 1141
Encapsulation processes, 1035
Endurance, 1096, 1105, 1112–1114, 1116
degradation, 1060–1062
test, 1056
Energetic disorder, 1027
Energy analysis, 597
Energy balance equation, 1462
Energy band diagram, 553
Energy conservation, 1317
Energy consumption per bit, 1106
Energy dispersive X-ray analysis (EDX), 118, 123
Energy distribution, 598–599
Energy distribution function, 1418, 1420
Energy filtering, 873
Energy landscape, 936
Energy loss near edge structure (ELNES), 125, 127
Energy relaxation time, 1353
Energy transport models, 1349
Bløtekjær's approach, 1351, 1352
Bløtekjær *vs*. Stratton approach, 1355
diffusion approximation, 1349–1350
diffusion scaling, 1350
relaxation times and carrier mobilities, 1353–1355
Stratton's approach, 1350–1351
Energy-filtered transmission electron microscopy, 122
Enhancement factor, 1325
Enhancement-mode operation, 505
Enhancement mode power MOSFETs, 425
Enhancement type, MOSFETs, 347, 351
Ensemble Monte (EMC) simulation, 739
Entanglement, 1207–1208
Environment health & safety (EHS), 225
eNVM demonstrators, 617
eNVM for neuromorphic applications, 622–625
eNVMs comparison, 611–617
Enzymatic degradation, 1034
Enzyme-linked immunosorbent assay (ELISA), 1011
Epitaxial layer, 658
P-type and N-type, 73
Epitaxially templated regrowth, 32
Epitaxy, 526–530
EPROM, 78
EPW software package, 1520, 1525, 1527, 1553, 1554
Equation
for the carrier flux, 1462
for the energy balance, 1462, 1465
Fourier, 1469, 1476
Poisson, 1462, 1465
Schrödinger, 1467
Equation of Poisson
in a semiconductor, 333
in MOSFETs, 364
in scaling rules, 366
Equilibrium distribution, 1343
Equipment simulation, 1260, 1291–1294
Equivalent circuit, 358, 1058, 1059, 1067, 1234, 1253, 1254
Equivalent oxide thickness (EOT), 275
Equivalent scaling, 932
Erasable programmable read only memory (EPROM), 49
Erase operation, 55
Erbium, 378
Error
discretization, 1394
equidistribution, 1394
estimator, 1394
goal-oriented estimator, 1394
indicator, 1394
local estimator, 1394
a posteriori analysis, 1394
a priori analysis, 1394
recovery-based estimator, 1394
residual-based estimator, 1394
Error correction code (ECC) techniques, 52
Error estimator, 1326
Escape time, 1461
Etching, 19, 1291, 1293, 1294, 1296, 1297
atomic layer, 21
dry, 20
selectivities, 21
wet, 20
Etch selectivities, 21
Etch stops, 211
Euler's method, 1465
EUV, 23
single exposure, 174
single-patterning, 179
Evanescent modes, 870
Evaporation, 194
Evaporation rate, 1481
Evolutionary technique, 1320
Excess noise, 763
Exchange and correlation functional, 1520, 1521, 1525–1527, 1532, 1547, 1548, 1553, 1554
Excimer laser annealing (ELA), 961
Excitation induced dephasing (EID), 853, 854
Excitatory postsynaptic current (EPSC), 1083
Excitons, 853
Expectation value, 1426
Exponential-fitting method, 1465
Ex situ dielectric capping, 211
Extended, electronic states, 1468
Extended X-ray absorption fine structure (EXAFS)
in chalcogenides, 1454
External quantum efficiency (EQE), 779
Extreme ultra violet lithography (EUVL), 279, 294
acid generator, 301
DUV, 294
exposure-development procedure, 302
modern industrial plants, 295

Extreme ultra violet lithography (EUVL) (*cont.*)
patterning process, 301
photolithography, 301
photon energy, 300, 301
photon-induced chemical amplification, 301
polymer, 300, 301
proton generation, 305, 306
proton migration, 306
radiation energy, 302
requirements, 295–297
transmission mode, 301
See also Radiation energy
Extreme ultraviolet (EUV) lithography, 27, 284, 1287
E-waste, 1038

F
Fabrication, 1035, 1037, 1038
Fabrication methods
ink formulation and printability, 968–970
printing techniques, 965–968
vacuum depositions, 964–965
Fabry-Perot type resonator, 855
Face pattern, 1085
Face-centered-cubic (FCC) sublattices, 1613
Fano factor (F_N), 753
Fanout (FO), 180
Faraday, 1305
Far-BEOL (FBEOL), 170
Far IR absorption, in chalcogenides, 1454
Fast diffusion, 208
Fast Fourier transform-SSRM (FFT-SSRM), 156
Fast modulation, 863
FAST selectors, 1072, 1073
FD-UTB device, 376, 381
FE-Capacitor RAMs (FeRAMs), 946
Fermi-Dirac distribution, 868, 1343
Fermi-Dirac integrals, 873
Fermi-Dirac statistics, 376
Fermi distributions, 853, 1430
Fermi energy, 855, 1430, 1576
Fermi functions, 1588
Fermi level, 332, 373, 376, 716, 980, 1624
Fermi potential, 1431
Fermi's golden rule, 1344
Ferroelectric-dielectric stacks (FE-DE), 939
Ferroelectric field-effect transistor (FEFET), 610, 1182, 1183
Ferroelectric gate ($HfZrO_2$), 325
Ferroelectric layer (FE), 934
Ferroelectric memory, 58
Ferroelectric MOSFETs (FeFETs), 936
Ferroelectric random access memory (FERAM), 1182
Ferromagnetic nanoparticles, 1038
Few time programmable memory, 83
Fick's first law, 1273
Fick's laws of diffusion, 14
Fick's second law, 1273
Field assisted superlinear threshold (FAST), 1071
Field-effect transistor (FET), 823–826, 830, 835–838, 932, 1006, 1584, 1603
frequency limitations, 824–825
perspectives, 826
as THz detector, 825–826
as THz emitters, 826
Field enhancement, plasmons, 783
Field of view, 694
Field oxide, 73
Figures of merit (FOMs), 778, 1001–1002
Filament-based eNVM, 622
Filament-based memories, 605
Filamentary conduction, 1095, 1101, 1102
Filamentation, 1471, 1480
Film doping, 142
Filter radius, 1322
Fully Depleted Silicon-On-Insulator (FDSOI) device, 260
FinFET
advantages, 260
CMOS scaling, 262
CPP, 263
DTCO, 261, 262, 264
features, 262
FP, 261
GAA, 263
high mobility materials, 267
nanosheet case, 267
nanosheet devices, 262, 265
scaling, 262, 275
SRB, 266
TEM, 266
VFET, 267
Finite difference approaches, 1579
Finite difference (FD) discretization, 1384
Finite-difference time-domain (FDTD), 1288, 1290
Finite elements
Lax-Milgram lemma, 1388
weak form, Slotboom variable, 1388
well-posedness, 1388
Finite volume method, 1442
Fin pitch (FP), 261
F-ion implant, 537
First firing, 1103
First-order Hamilton's equation, 1310
First order parameter model, 395
First order partial differential equation system, 1307
First-principles calculations, 1516, 1517, 1527, 1528, 1530, 1534
Five-stream model, 1275
Flash annealing, 13
Flash memory, 78, 611, 617, 1174, 1189, 1433
array architectures, 51
charge injection/extraction mechanisms, 54
charge storage solutions, 52–53
MOSFET devices, 51–52
NAND flash, 56
NOR, 55
Flat-band
condition, 332, 334
voltage, 338
capacitance, per unit area, 337
Flat panel X-ray imagers (FPXI), 754
Flexible electronics, 911, 913–915, 919, 924
Flexible photodetectors, 797
Flexible transistors, 911
Flexographic printing, 968
Flicker noise, 763, 938
Floating-body RAM, 58
Floating diffusion, 362
Floating-gate
CID, 357
equivalent circuit, 358
operation, 357
Floating gate MOSFET devices, 50–51
Flowable gap fill CVD, 187
Flowable low-k SiCOH 2.7, 188

Fluctuation-dissipation theorem, 1594
Fluctuations, 1270
Fluidic problem, 1320
Fluid mechanics, 1308
Fluorinated silicon glass (FSG), 182
Flux, 195
Flux density, 1419
Fluxgate, 675
Flux qubit, 1212
Flying qubits, 1222–1223
Focused ion beam (FIB), 118, 170
Folded architectures, 110
Force, 1308
  circulatory, 1308
  dissipation, 1308
  gyroscopic, 1308
  potential, 1308
Forming-free device, 1044
Forming process, 1044, 1059, 1103
Forward bias, 583
Forward polarization, 587
Four-moments energy transport model, 1352
4-point bending, 183
Four-point-probe technique
  correction factor, 145
  geometries, 145
  layers, 144
  resistivity, 142, 144, 145
  semiconductor, 143
  sheet resistance, 145
Fourier equation, 1469, 1476
Fourier heat equation, 1102, 1105
Fourier heat-flow equation, 1049
Fourier law, 1316
Fourier transform
  CCD, 359
  image sensors, 361
Fourier transformed infrared (FTIR) spectra, 183
Fourier's law, 1351
Fowler-Nordheim (FN) diode, 1240
Fowler-Nordheim (FN) tunneling, 54, 1170
Fröhlich interaction, 1528
Fractional diffusivity, 1277
Frame-transfer
  CCD, 360
  sensor, 360
Fréchet derivative, 1320
Fréchet differentiable, 1320
Fréchet differentiable map, 1320
Free energy of formation, 1272
Free-wheeling diode, 480, 544
Frenkel pair, 1269
Frequency
  attempt-to-escape, 1473
  cutoff, 1425
  maximum oscillation, 1425
Fresnel coefficients, 158
Fringe field effect, 378
Fringing fields, 878
Front end of line (FEOL), 270, 1069
Frontside illuminated structure (FSI), 687
Fully Aligned Via (FAV), 188
Fully coupled Newton approach, 1390–1391
Fully-depleted silicon-on-insulator (FD-SOI), 372, 380, 384
Full molded pressure sensor, 673
Full-order model (FOM), 1326, 1327
Full quantum transport
  vs. analytical model in long 15nm nanowires, 1626–1627
  in long 15nm nanowires, 1623–1626
  in short 5nm nanowires, 1627–1628
Full width at half maximum (FWHM), 135, 752
Functioning regimes, MOS capacitor, 334, 342
Fundamental balanced mixers (FBM), 819
Furnace annealing, 12, 171

G
Gate-all-around (GAA), 263
GaAs bulk, 1419
Gain
  current, 1425
  medium, 851–854
  unilateral, 1425
Gallium-arsenide (GaAs), 376
  Gallium nitride, 143, 371, 385
  epitaxial layer, 136
  screw dislocation density, 135
  uses, 135
Galvanic isolation, 69, 107
Gallium nitride (GaN), 112, 1526–1529
  epilayers, 135
  lateral devices, 533, 540
  material, 526–530, 532
  power transistors, 526
  vertical transistors, 554
Gallium nitride-based power HEMTs, 555, 563
Gallium nitride-on-Si epitaxy, 528
  Game consoles, 641
Gap, 656
Gartner hype cycle, 1117
Gate
  contact, 332, 343
  control, 877
  efficiency, 895
  electric length, 343
  geometrical length, 343
  insulator, 1170
  leakage, 938
  potential, 374
Gate-all-around (GAA) transistor, 34, 877
Gate-drain capacitance, 884
Gate-drain underlap, 885
Gate set tomography (GST), 1208
Gate-stack reliability, 564
Gate voltage, 981
Gâteaaux derivative, 1321
Gâteaux derivative, 1321
Gated Schottky based FD-UTB device, 376, 377
Gated Schottky based ultrathin-body devices, 376–378
Gauss law, 1249, 1338
Gaussian
  distribution, 1262
  wavepacket, 1467
Gear method, 1465
Generalized coordinate, 1309, 1311, 1312
Generalized Einstein relation, 1428
Generalized gradient approximation (GGA), 1525, 1532
Generalized Harrison's Law, 1608
Generalized magnetic flux, 1310
Generalized momentum, 1310
Generalized scaling theory, 366
Generation and recombination, 1344

Generation rate, 1481
Generation-current contribution, 587
Generation-recombination (GR) noise, 763
Generation/recombination model, 1102
Generations, of integrated circuits, 366
Genetic algorithms, 1290, 1607
Geometrical length of gate, 343
Geometrical scaling, 867, 868
Geometric constraint, 1324
Geometry, 145, 1260, 1261, 1265, 1291, 1293, 1295
German traffic sign benchmark (GTSRB), 624
Germanene, 1531, 1532, 1534–1541, 1553
Germanide, 30
Germanium (Ge), 134, 375, 384, 1518
  displacement field, 134
  end-of-range (EOR) defects, 134
  HR-XRD pattern, 135
GeSbTe alloys, 131, 132
$Ge_2Sb_2Te_5$ (GST-225)
  bandgap, 1098
  conductivity, 1107
  crystal structure, 1097
  reflectivity, 1098
  resistivity, 1098
$Ge_2Sb_2Te_5$ matrix, 614
GeTe
  reflectivity, 1098
  resistivity, 1098
Getter layer, 665
Ghosting, 769
Giant magnetoresistance (GMR), 675, 1146
Gibbs free energy, 933, 1103
Glass, 1304
Glass temperature, 1479
Global shutter (GS), 684
Goal-oriented error estimators, 1394
Golden composition, 1116
Gradient-based topology optimization, 1320
Gradual-channel approximation (GCA), 345
Grain size, 612
Granularity, 612
Graphene, 372, 384, 838, 840, 842, 890, 906, 1516, 1520, 1531, 1535, 1539, 1544, 1545
Graphene-based bolometers, 782–783
Graphene-based heterostructures
  graphene/organic semiconductors, 787–790
  graphene/perovskites, 790–791
  graphene/III-V semiconductors, 786–787
  graphene/silicon, 785–786
  graphene/2D materials, 790–795
Graphene based transistors
  basic device geometry and characterization, 907
  contact resistance, 909
  flexible transistors for high frequency applications, 911–915
  radio frequency transistors, 909
  vertical transistors/hot electron transistors, 915–919
Graphene/BP heterostructures, 791
Graphene/C8-BTBT, 790
Graphene/$CH_3NH_3PbI_3$, 790
Graphene nanoribbon (GNR) TFETs, 880
Graphene/organic semiconductors, 787–790
Graphene/pentacene, 787
Graphene/perovskites, 790–791
Graphene photodetectors, 800
  graphene-based bolometers, 782–783
  graphene-based heterostructures, 785–795
  integrated, 795–797
  MGM photodetectors, 781–782
  photogating, 783–785
  plasmonics enhanced, 782–783
Graphene/porous Si Schottky diodes, 786
Graphene/III-V semiconductors, 786–787
Graphene sheet, 1116
Graphene/silicon heterostructures, 785–786
Graphene/silicon nanowire, 786
Graphene/silicon Schottky junctions, 785
Graphene/SiO_2/Si, 785
Graphene/WS_2/graphene heterostructure, 791
Graphene/WSe_2/graphene, 791
Graphics processing unit (GPU), 1168
Graphoepitaxy, 28
Gravitational force, 1310
Gravure printing, 967
Greedy algorithm, 1326
Grid generation, 1384, 1391
  hybrid meshes, 1393
  mesh adaptation, 1393–1396
  meshes for semiconductor devices, 1396–1398
  structured meshes, 1392
  unstructured meshes, 1392–1393
Groenewold product, 1566
Growth process, 1476, 1481
Growth velocity, 1104
GST–225 application, 1454, 1466, 1468, 1476
Gummel map, 1386–1388, 1401
  discretization of, 1389–1390
  flow chart, 1387
  numerical solution, 1388–1389
Gummel plot, 1424
Gummel-Poon (GP) BJT model, 1241–1242
Gummel's nonlinear relaxation method, 1440
Gummel symmetry test (GST), 980
Gunn diodes, 810–814
  materials for, 811
  perspectives, 814
  realizations of Gunn oscillators, 811–813
  transit-time mode Gunn oscillations, 810–811
GW approximation, 1520, 1554, 1555
Gyroscopes, 660, 662, 663

H

Hänsch's mobility model, 1362
Hafnium, 379
Half pitch, 366
Hall coefficient, 150
Hall effect technique, 150
Hall magnetic sensors, 107
Hall sensors, 675
Hamiltonian function, 1328
Hamiltonian matrix, 1308, 1475, 1584, 1607–1610
Hamiltonian operator, 1561, 1564
Hamiltonian system, 1328
Hard-disk air bearing, 1315–1318
Hard disk drives (HDD), 89, 1315
Hardmask (HM), 171, 172, 221
Hard recovery characteristics, 484
HD, *see* Hydrodynamic models
Healthcare, 643
Heat conduction, 1318
Heated chuck, 203

Heated displaced Maxwellian distribution, 1344
Heated implants, 9
Heated Maxwellian distribution, 1343, 1351, 1352, 1359, 1376
Heater, 1107, 1108
Heat transfer, 1308
Heaviside function, 1415
Heavy-doping, 893
Hecht collection efficiency, 753
Helmholtz resonator, 667
Hermeticity, 665
HEMT heterostructures, 529–530
Hermetic packages, 651
Hermitian matrix, 1587
Herring–Vogt transformation, 1417
Heteroepitaxial coupling, 129
Hetero-epitaxy of GaN, 527
Heterojunction, 384, 826, 828, 830–833, 890, 1492, 1494, 1498, 1500, 1501, 1503, 1510
Heterojunction bipolar transistor (HBT), 826–836, 915
  compact modeling for circuit design, 834
  complete small-signal equivalent circuit, 829, 830
  III-V HBTs, 830
  InP/GaAsSb HBT, 832–833
  InP/InGaAs HBT, 831–832
  performances and limitations, 830
  performances of HBTs-based circuits, 835
  perspectives, 835–836
  reduction of total emitter-collector transit time τ_{EC} and base resistance, 830
  SiGe HBT, 833–834
Heterojunction doping pocket, 879
Heterojunction FETs (HFETs), 824
Heterojunctions, 715
Heterojunction solar cells, 714
Heterojunction TFET (HTFET), 885
  band tails, 893
  III-nitride HTFETs, 891
  lateral heterojunction TFET, 888
  layered two-dimensional HTFET, 890–891
  vertical heterojunction TFET, 887–888
  vertical nanowire HTFETs, 889–890
Heterostructures, 715, 785–793, 795–797, 886
Hexagonal, 193
HfO_x, 607
HgI_2, 751, 757, 767
HiCUM, 1242–1243
Hierarchical drift-diffusion model, 1431–1432
Hierarchical hydrodynamic model, 1427–1431
Hierarchical simulation, 1297
High angle annular dark field (HAADF), 121, 123
High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM), 270
High-aspect ratio damascene, 195
High-bias coherent transport simulations, 1629–1632
High electron mobility, 532
High electron mobility transistors (HEMTs), 530, 567, 824, 826
Higher order models, 1364
Higher order moment models, 1364–1365
  kurtosis, properties of, 1365
  transport parameters, modeling of, 1366
Higher-quality thin films, 1038
Highest order moment closure, 1356
High-frequency small-signal model, 987
High-frequency TFT model, 990–991
High-g sensors, 654
High-k, dielectrics, 332, 367
Highly accelerated temperature and humidity stressing test (HAST), 673
High resistance state (HRS), 946, 1044, 1181
High resolution X-ray diffraction (HR-XRD), 130
High vacuum level, 665
High-voltage double-pulsed system, 558
High-volume manufacturing (HVM), 299
High voltage power devices, 101–103
HiSIM MOSFET model, 1247
HiSIM SOI, 1249–1250
HiSIM-HV, 1252
Hohenberg-Kohn theorem, 1576
Holding voltage (Vhold), 614, 1101, 1102
Holes, 1338
Homogeneous energy balance equation, 1340
Homojunction TFET, 886, 888
Hopkins's equation, 1287
Hopping
  conduction by, 1458, 1461
  current, 1058
  in amorphous semiconductors, 1452
Horizontal tube furnaces, 12
Hot atom damage (HAD), 938
Hot carrier degradation, 1375
Hot carrier effects, 1373
  hot carrier degradation, 1375
  hot carrier gate currents, 1375
  impact ionization, 1375, 1376
  kurtosis, 1374–1375
  velocity overshoot, 1374
Hot carrier gate currents, 1375
Hot-carrier model, 1103
Hot carrier solar cells, 737
Hot carrier tunneling, 54, 1375
Hot carriers, 98
Hot-electron transistors (HETs), 915
H-transform, 1418
Humectants, 969
Humidity, 186
HV/power compact models, 1252
Hybrid case (H-S3D), 272
Hybrid charge-flux qubit, 1212
Hybridization, sp_3, in chalcogenides, 1455
Hybrid organic-inorganic perovskite, 722
Hybrid RAM, 604
Hydrodynamic approach, 1461–1464
Hydrodynamic formalism, 1102
Hydrodynamic models (HD), 1347–1348, 1427–1431
  isotropic symmetry, 1348
  numerical properties, 1348
  phenomenological highest order moment closure, 1348
Hydrogenated amorphous silicon, 960
Hydrogen plasma, 197
Hydrophobicity, 186, 1323, 1324
Hydrophobic solid substrate, 1323
Hydrophobic surface, 1323
Hyperbolic system, 1349
Hyper-scaling, 868, 869
Hysteresis, 193
Hückel theory, 1605

I

IC, *see* Integrated circuit (IC)
Ideal contacts, 715
Ideality factor, 1424

Ideal Ohmic contact, 1431
IGZO TFTs, subthreshold model
DC model, 1001
small signal model, 1001
III-nitride HTFETs, 891–893
III-V materials, 828, 830, 831, 833, 834, 1633
III-V semiconductor, 1492, 1494–1496, 1498, 1503, 1507
Image lag, 769
Image resolution, 765–767
Image sensors
aliasing, 361
blooming, 363
degradation of contrast, 362
discrete output sequence, 361
Dumbbell Nebula, 363
Fourier transform, 361
moiré fringes, 362
Nyquist limit, 362
output spectrum, 362
pattern noise, 362
performances, 361–363
resolution, 361
sampling function, 361
sensitivity, 363
spatial sampling, 361
spectral responsivity, 363
Supernova Cosmology Project, 363
X-ray detection, 363
Imaginary path, 871
Imaging, 1287
Immersion lithography, 173, 284, 285, 1287
Immunoassay, 1011
Impact ionization (II), 1102, 1375, 1376, 1432, 1433
Impact parameter, 1269
Impedance-based immunosensor, 1011–1013
Implantation damage, 1280
Implantation-enhanced diffusion, 1280, 1281
Implant damage, 9
Implant dose, 9
Implant energy, 9
Implants, 9
Implicit function theorem, 1320
Implicit interface, 1320
Implicit methods, 1384
Imprint, 968
Impurities, 1272
Impurity doping, 371
InAlN/GaN heterostructure, 530
Incipient metals, 1103
Indistinguishable Fermions, 1565
Induced eddy current, 1312
Inductive levitation system, 1310, 1311
Inductively coupled plasma, 197
Inductor, 1236–1237
Inductor coupling coefficient, 1237
Inert electrode (IE), 1049
Inertial measurement units (IMU), 660
In-Ga-Zn-O (IGZO), 765
Injection enhancement (IE) effect, 465
Injector drivers, 102
Ink
compositions, 969–970
fluid physical properties, 970
types, 968–969
Inkjet printing, 966–968, 972
In-memory computing (IMC), 620, 1168
Innovative applications, 618–622
Innovia Films, 1020
Inorganic dielectrics, 1027
Inorganic Layer (IL), 287
Inorganic semiconductors, 1025
Input circuit, CCD, 362
Inscattering functions, 1589
In-situ dielectric capping, 211
Insulated gate bipolar transistor (IGBT), 448, 492
design concepts for, 470
development of, 448–449
evolution of structure and design concept, 463
future research, 473
intelligent gate drive control, 474
junction temperature and power density, 472–473
module technologies, 466–468
next-generation transistor cell and vertical structures, 473–474
p-ch, 468–469
reverse blocking and reverse conducting, 470–472
safe operating area, 458–463
structure and operation, 450–453
switching characteristics, 453–458
thermal management, 474
Insulated-gate field-effect transistor (IGFET), 343
Insulator-metal transition (IMT), 939, 1071
Integral constraint, 1321, 1322
Integral formulation, 1573
Integrated circuits (ICs), 180, 279, 366, 867
design, 1241
Integrated graphene photodetectors
optical cavity, 795
special geometry/architectures, 797
Integrated optics, 1213–1215
Jaynes-Cummings model, 1215
qubits, 1216
qubits and gates, 1217
Integrating X-ray detector, 760
Integration period, CCD, 359
Integration process flow, 1074
Integration time, in photocapacitors, 340
Intelligent gate drive control, 474
Intelligent motor drivers, 83
Intel processors technologies, 43
Interactions, 1585
Interband tunneling, 869
Interface, 1589
Interface hybrid phonon/plasmon modes (remote phonons), 1554
Interface resistance, 1593
Interface states, 378
Interface trap density, 378
Interface traps, 380, 1507–1509
Interfacial diffusion, 16
Interfacial layer, 199
Interfacial phase change memory (iPCM), 124, 1116
Interfacial strengths, 184, 185
Interlayer dielectric (ILD), 265
Inter-level (ILD) dielectric, 19, 182
Inter-trap transitions, 1472–1473
Intermediate band (IB), 733
Internal degrees of freedom, 1585
Internal quantum efficiency (IQE), 779
Internal voltage amplification, 935
International Technology Roadmap for Semiconductors (ITRS), 152
Internet of things, 620, 643, 1147

Interstitials, 1267, 1272, 1273, 1280, 1282
Intervalley deformation potentials, 1516
Intervalley scattering, 1518, 1525, 1533, 1535, 1537, 1554
Intrinsic density, 1431
Intrinsic device, of PCM, 1478
Intrinsic diffusion coefficients, 1278
Intrinsic Fermi level, 373
Intrinsic gain, 989, 1001
Intrinsic point defects
  analytical models for, 1267–1268
  and impurities, 1271
Inverse design, 1322
Inverse Fourier transformation, 1288
Inverse lithography, 24
Inversion, 855
  charge, 336–339
  coefficient, 406, 409, 412, 418
  factor, 853
  layer, 335
  point, in MOSFETs, 365
Inverter, 180
Ion beam mixing, 12
Ion implantation, 4, 1261
  analytical one-dimensional multilayer models, 1263
  intrinsic point defects, 1267–1268
  ion beam mixing, 12–14
  ion stopping, 5
  model parameters for analytical models, 1266–1267
  Monte-Carlo simulation, 1268
  multidimensional implantation models, 1265
  one-dimensional analytical models, 1262
  plasma implant, 10–11
Ion-sensitive field-effect transistor (ISFET), 1004, 1006, 1014
Ion stopping, 5–7
Ionization energy, 750
Ionization potential, 198
Ionized gas, 194
Ionized PVD, 196
Ionized sputtering, 198
IonQ, 1204
IRDS Roadmap, 310
Irreversible thermodynamics, 1336
Isolated gate bipolar transistor (IGBT), 1243
Isotropic symmetry, 1348
Iterative approach, 1321

J
Jacobian matrix, 1390
Jacobians monotonicity theorems, 1441
Jaynes-Cummings model, 1213, 1215
JBSFETs, 511–512
JFET resistance, 432
Josephson-based qubit, 1209–1211
  charge qubit, 1211
  coupling qubits, 1213
  flux qubit, 1212
  hybrid charge-flux qubit, 1212
Joule heating, 1059, 1102, 1106, 1107, 1115, 1116
JUNCAP model, 1239–1240
Junction-barrier controlled Schottky (JBS) structure, 495
Junction electric field, 877
Junction field-effect transistors (JFETs), 1250–1252
Junction isolation, 69
Junctionless FET (JLFET), 939
Junction termination extension (JTE) structures, 444

K
K-edge fluoroluminescence, 763
Kelvin configuration, 144
Kick-out mechanism, 1274
Kikuchi backscattering, 204
Kinchin-Pease formula, 1269
Kinematic viscosity, 1318
Kinetic Monte-Carlo (KMC) algorithm, 1283
Kink and tail, 1279
Kirchhoff approximation, 1288, 1290
Kirchhoff's law, 1440, 1588
Kirk effect, 829, 830, 832, 834
Klein relationship, 751
Klein rule, 760
Knudsen number, 1350
Kohn-Sham equation, 1520–1523, 1526, 1554
Kohn-Sham system, 1576
Kohn-Sham wavefunctions, 1520–1522
$\boldsymbol{k} \cdot \boldsymbol{p}$ Hamiltonian, 1492–1496, 1498
$\boldsymbol{k} \cdot \boldsymbol{p}$ model
  eight-band, 1493, 1498
  TFETs, 1498–1503
Kronecker symbol, 1416
K-space (KS), 1414–1416, 1426, 1427
Kubo formalism, 1594
Kurtosis, 1261, 1364, 1374–1375
  lateral, 1262, 1266
  properties of, 1365

L
Lab-on-a-chip, 1322
Lagrange-Maxwell equation, 1309–1311
Lagrangian formalism, 1308, 1310
Lag signal, 770
Lambert's law, 302
Landauer-Büttiker formalism, 1590, 1594
Landau FETs, 932
Landau-Khalatnikov Equation (LKE), 935
Landau Theory, 933
Larger-grain morphology, 1028
Large-scale system, 1326
Laser-assisted plasma sources
  beam transportation system, 298
  chamber, 298
  CO_2 laser, 297
  conversion efficiency, 299
  development, 297
  droplet emission, 298
  emission spectrum, 299
  irradiation dose, 299
  light sources, 297, 299
  lithographic systems, 297
  multilayer Mo/Si technology, 298
  open-loop power, 300
  optical energy, 300
  plasma generation, 299
  power requirement, 299
  principle of operation, 297
  requirement, 300
  secondary emission, 298
  Sn droplets, 300
  source power, 299
  UV radiation, 298
Laser annealing, 188
Laser heating, 13

Laser processing, 1013
Laser produced plasmas (LPP), 297
Latency, 39, 1096, 1113
Lateral devices architectures, 530–540
Lateral direction, 1261
Lateral DMOS, 87
Lateral heterojunction TFET, 888–889
Lateral p-n junction, 380–381
Lattice kinetic Monte Carlo (LKMC) schemes, 1283
Law of Moore, 366
Layered two-dimensional HTFET, 890–891
Layer stacks, 526
Layout optimization, 1319
LDMOS, 75, 1252
Leakage, 185, 192
Leakage current, 374, 495, 1110
LED lighting, 101
Legendre polynomials, 1416, 1418
Legendre transform, 1310
Leti L-UTSOI, 1250
Level set method, 1294, 1320
Levitation actuator, 1315
Levitation micro-actuator, 1314
Levitation micro-system, 1315
Life science, 1322
Light detection and ranging (LIDAR), 862
Light effective masses, 1633
Light emission, 374
Light-emitting devices, 381
Light-emitting diode (LED), 1032
Lightly porous SiCOH, 184
Light management, 705, 730
Light trapping, 711
Limit cycle, measurement of PCM characteristics, 1480
Limits to scaling theory, 367
Linear controlled sources, 1237
Linear dynamic range (LDR), 779
Linearity, 359, 363, 762
Linearized augmented plane wave (LAPW), 1608
Linear models, 1238
Linear-parabolic model, 347–348
Linear parametric system, 1329
Linear region, in MOSFETs, 346, 351
Linear response theory, 1539, 1541
Linear sensors, CCD, 359
Linear solvers, 1401–1402
  BiCGSTAB, 1401
  direct methods, 1401
  GMRES, 1401
  ILUT preconditioner, 1402
  Krylov subspace methods, 1401
  preconditioning, 1402
  re-ordering, 1401
  sparse factorization, 1401
  sparse matrix, 1401
  TFQMR, 1401
  transpose free solvers, 1401
Linear system, 1307
Linear time invariant system (LTI), in MOSFETs, 347, 351, 352, 1307
Liouville equation, 1342
Lipschitz boundary, 1320
Liquid phase epitaxy (LPE), 527
List, 1305
Lists of lists, 1305
Lithium doped Si detectors, 751
Litho etch litho etch (LELE), 175, 221
Litho-freeze-litho-etch (LFLE) process, 24, 293
Lithographic process, 296
Lithography, 21, 1304
  Airy circular pattern, 282
  Airy diffraction pattern, 282
  ArF laser sources, 286
  basic principle, 280, 1286
  carbon and oxygen atoms, 286, 287
  CMOS technology, 286
  constraints due to light source, 22
  contrast parameter, 280
  development procedure, 280
  directed self-assembly, 28–29
  distribution of light, 281
  EUV, 1287, 1289
  geometrical considerations, 283
  goals of, 22
  hard masking, 287
  immersion, 286, 288, 1287
  light diffraction, 281
  liquid immersion, 286
  Moore's law, 279
  multiple patterning, 1287
  Ohnishi parameter, 286
  optical resolution, 281
  optical system, 284
  performance of a resist material, 280
  photoresist, 280, 281, 286
  plasma etching process, 286
  polymers, 287
  projection, 281, 284, 1286
  Rayleigh principle, 282
  refraction index, 283
  role of resist in, 23
  scanner projection systems, 284
  silicon-rich material, 287
  step-and-repeat systems, 281
  step-and-scan systems, 281
  stepper, 23
  thin chrome layer, 281
  thin resist layers, 286
  transmission pattern, 281
  types, 280
  UV light, 287
Lithography-etch-lithography-etch (LELE) approach, 288
Lithography simulation, 1286, 1290
  principle of, 1287
  resist development, 1290
  simulation of imaging, 1287
Litho-litho-etch (LLE), 175, 293
Littrow configuration, 856
Load curve, measurement of PCM oscillations, 1484
Local density approximation (LDA), 1525, 1527, 1554
Local error estimators, 1394
Local heating, 1114
Local interconnect, 30
Localised states, network of, 1460
Localized-orbital representations, 1609
Localized resistors, 1589
Localized states (traps), 1098, 1102
Localized surface plasmon resonances (LSPRs), 1324, 1325
Local oxidation of silicon (LOCOS), 74
Local substrate removal (LSR), 536
Local vibrational modes (LVM), 161
Logic gate, 942
Long diodes, 585–586

Longitudinal Optical LO phonon with plasmons (LOPC), 137
Long-throw PVD, 195
Lookup table, 1430
Lorentz model, 160, 161
Low-g sensors, 654
Low-k silylation, 189
Low noise amplifier (LNA), circuit characteristics, 416
Low-power design, 409
Low resistance state (LRS), 615, 946, 1044, 1181
Low-temperature polycrystalline silicon (LTPS), 961
Low-voltage, 409, 410
Lucky electron model, non local, 1433
L-UTSOI, 1250
Luttinger parameters, 1493
Löwdin method, 1607

M
Materials, high mobility, SAG, 268
Machine learning (ML), 621
Macromolecular materials, 1032
Macroscopic diffusion behavior of dopants, 1275
Macroscopic models, 1476–1478, 1485
  of PCM dynamic response, 1479–1481
  of PCM oscillations, 1478
  stability analysis of PCM oscillations, 1482–1485
  thermal analysis of PCM, 1481
Macroscopic observables, 1342–1343, 1345
Macroscopic relaxation time approximation, 1345–1346, 1427, 1428
Macroscopic transport models, 1345
  closure problem, 1346
  hydrodynamic models, 1347–1349
  macroscopic relaxation time approximation, 1345–1346
  method of moments, 1345
  parabolic band, moment equations for, 1346–1347
Magnet, 194
Magnetic levitation, 1310
Magnetic permeability, 1310
Magnetic random access memories (MRAMs), 85, 947
Magnetic tunnel junction (MTJ), 947, 948, 1131, 1147, 1182, 1254–1255
Magnetoelectric spin–orbit (MESO) devices, 1161
Magnetometers, 675
Magnetoresistive sensors, 676
Magnetoresistivity, 675
Magnetoresistor, 678
Magnetron, 193, 194
Magnon, 1595
Majorana bound states (MBS), 1592
Majorana zero modes (MZM), 1592
Mandrel, 177
Manhattan rule, 1085
Manifold absolute pressure (MAP), 638
Manufacturability, 1322–1324
Many-body interactions, 1586
Many-body Liouville-von Neumann equation, 1564–1565
Many-body perturbation theory (MBPT), 1585, 1586, 1590, 1595
Many-body problem, 1564
Many-body Wigner equation, 1564
Many-body Wigner equation, Monte Carlo methods
  density functional theory, 1576
  signed particle method, 1577–1578
  Wigner density functional theory, 1576–1577
  Wigner Monte Carlo method, 1577
$MAPbI_3$ films, 790
Mask correction methods, 285
Mass tensor, 1428
Master oscillator power amplifier (MOPA), 297, 300
Material distribution, 1319
Material removal, 194
Materials, high mobility
  GE CMOS, 271
  InGaAs, 270
  pCMOS, 271
  SEM, 269
  semiconductor, 268
Materials science (MS), 1604, 1605
Mathematical model, 1308
Matrix, 1305
  Hamiltonian, 1475
  overlap, 1475
Matrix-vector multiplication (MVM), 62, 1168
Maximum oscillation frequency f_{max}, 828–836
Maxwell's equations, 1324, 1338
Maxwell-Boltzmann distribution, 1343
Maxwell-Boltzmann statistics, 1386
Maxwell's equations, 1287
MD, *see* Molecular dynamics (MD)
Mean free path, 196, 1423
Measurement
  ellipsometric, in a-GST, 1458
  of modulated photocurrent, 1456
  of Seebeck effect, 1456
  of steady-state photocurrent, 1456
Measurement of dose, 748
Measurement of PCM characteristics, 1478
  amorphous phase, 1479–1481
  dynamic setup, 1479
  limit cycle, 1480
Measurement of PCM oscillations
  load curve, 1484
  stability, 1482–1485
Mechanical properties, 182
Mechanical strength, 183
Medical implants, 1036
Melt-quenching speed, 1099, 1101, 1105, 1106
Melting temperature, 1099, 1101, 1104, 1105, 1479
Memory
  applications, 621
  cost per bit, 1096
  cross-point, 1095, 1110, 1116
  hierarchy, 1096
  key attributes of, 1096
  selectors, 625–630
  3D, 1095, 1116
  wall, 1045
  window, 1105
Memory switching (MS), 1100, 1102, 1103, 1105
Memory threshold switching (MTS), 1453
Memory transistor
  and mainstream Flash technologies, 1170–1174
  synaptic arrays, 1172–1178
Memristive devices
  2-terminal memristive devices, 1181
  3-terminal memristive devices, 1182–1184
  DNNs with, 1186
  SNNs with, 1184
Memristive technologies, 1191
Memristor, 1045, 1169, 1181, 1184, 1254
MEMS, 636
  pressure sensors, 673–674
Merged pin and Schottky (MPS) diode, 484

Mermin-Wagner theorem, 1536
MESFETs, 1250, 1251
Mesh, 1307
  adaptation, 1393, 1394
  coarsening, 1395
  conformal, 1391
  connectivity matrix, 1392
  Delaunay criterion, 1393
  hybrid, 1393
  isotropic, 1396
  metric, 1395
  node movement, 1395
  octree, 1392
  quadtree, 1392
  quality, 1395
  refinement, 1395
  regularization, 1395
  remeshing, 1395
  for semiconductor devices, 1396–1398
  structured, 1392
  unstructured, 1392–1393
Message passing interface (MPI), 1618
Metal cap layer, 209
Metal contact, 197
Metal element, 383
Metal flux density, 197
Metal grain granularity (MGG), 1296
Metal hardmask (MHM), 172
Metal insulator graphene (MIG) diodes, 918
Metal lines, 173
Metal nitride, 385
Metal organic chemical vapor deposition (MOCVD), 270, 724
Metal organic vapor phase epitaxy (MOVPE), 859
Metal oxide semiconductors, 961
Metal pitch (MP), 182, 261
Metal resistivity, 182
Metal work function, 385
Metal-ferroelectric-insulator-semiconductor (MFIS), 933
Metal-ferroelectric-metal-insulator-semiconductor (MFMIS), 933
Metal-graphene-metal (MGM) photodetectors, 781–782
Metal-induced doping, 375
Metal-insulator-metal (MIM) capacitor, 106
Metal-insulator-metal (MIM) structure, 1044
Metal-insulator-semiconductor (MIS) capacitor, 332–336
Metal-insulator-semiconductor (MIS) system, 182, 385, 564
Metal-insulator-transition (MIT), 123
Metal-organic chemical vapor deposition (MOCVD), 526, 527
Metal-organic vapor phase epitaxy (MOVPE), 527
Metal-oxide semiconductor (MOS)
  capacitor, 332, 342–343
  junction structures, 150
  model 11, 1246
  model 9, 1246
  photocapacitor, 339–341
  structure, 336
  transistor, 343, 350
Metal-oxide-semiconductor field effect transistors (MOSFETs), 128, 343, 350, 373, 375, 376, 379, 532, 830, 867, 868, 896, 897, 933, 960
  Berkeley Short-channel IGFET Model, 1244–1245
  Bloch sphere, 1125
  BSIM3, 1245
  BSIM4, 1245
  BSIM6, 1245–1246
  body diode, 443–444
  channel, 343
  n-channel MOSFET, 343–350
  channel strain, 1124
  CMOS, 1124, 1125
  compact models, 1247
  definition, 1124
  dichalcogenide monolayer devices, 1125
  electron spin, 1126
  EKV2.6, 1246
  EKV3, 1247
  5nm technology node, 1124
  HiSIM MOSFET model, 1247
  mobility, 1124
  Philips MOS model 11, 1246
  Philips MOS model 9, 1246
  PSP MOSFET model, 1246
  Poisson's equation, 364
  scaling rules, 366–368
  silicon, 1125
  transfer characteristics, 868
Metal-semiconductor interface, 372, 379
Metal-semiconductor junction, 375
Metal-semiconductor Schottky diode
  energy analysis, 597
  energy distribution, 598–599
  recombination time delay, 597
  Schottky diode under non-equilibrium, 599–601
Metal-semiconductor system, 372
Metal-to-insulator transition (MIT), 939
Metalens, 1324, 1325
Metallic electrodes, 1032
Metals, 1023
Metal–oxide–semiconductor field-effect transistor (MOSFET), 309
Metavalent bonding, 1103, 1455
Methacrylate polymers, 305
Methacrylic acid (MAA), 292
Method of moments, 1345
Method of moving asymptotes, 1322
Methyl methacrylate (MMA), 291
Methylammonium lead halides, 757
Methyltriethoxysilane, 182
MEXTRAM, 1242
Micro-accelerator, 1310
Micro-actuator, 1308
Micro-bearing, 1310
Micro-coil, 1308
Micro-inertial-sensor, 1310
Micro-motor, 1310
Micro-sensor
  assembly, 651–653
  classification, 645–648
  terminology, 648–649
Micro-transporter, 1310
Microcavity lasers, 861–862
Microelectromechanical systems (MEMS), 1303–1305, 1308, 1309, 1322, 1326
  analytical mechanics, 1308
Microfabrication, 649–650
Microfluidics, 1322
Microlens, 685
Micromachining, 649–650
Micro/nano-electronic technology, 310
Microneedles, 1026
Microphones, 666
Microscopic distribution function, 1341

Microscopic models, 1461–1477
3D simulation, on random network, 1469–1472
ab initio quantum transport models, for ultrascaled chalcogenide devices, 1473–1477
detrapping due to electron-electron interaction, 1467–1469
dispersive band states, inclusion of, 1464–1467
hydrodynamic approach to trap-limited transport, 1461–1463
inter-trap transitions, 1472–1473
Microscopic relaxation time, 1422, 1427
approximation, 1344
Microscopic transport models, 1341
analytical distributions, 1343–1344
band structure, 1342
BTE, 1341–1342
macroscopic observables, 1342–1343
microscopic generation and recombination, 1344–1345
microscopic relaxation time approximation, 1344
Microstrip inductance, 1238
Microstrip line, 1238
Microtexture, 1323, 1324
Mid-gap condition, 335
Mid-gap silicide, 374
Midband small signal model, 986–987
Midband TFT model, 988
V_T shift, effect of, 989–990
contact resistance, effect of, 988–989
Miller capacitance, 433
Miller theory, 939
Miniaturization of ICs, 366
Minimos-NT, 1377
Minority carrier concentrations, 583–584
Minority-alloy, 199
Minority-carrier current, 584–585
MIS, 1240
MIS-transistors, 562
MISHEMT, 537
MISNAN, 1247
Mixed National Institute of Standards and Technology (MNIST), 624
Mixed–ionic–electronic conduction (MIEC), 1071
M-matrix, 1444
MM20 LDMOS Model, 1252
MM9, 1243
MMA, 1322
Mobile wireless charging systems, 83
Mobility, 151, 1340, 1353–1354
in AlN, 1530
degradation, 392, 395–397, 399–401
degradation in MOSFETs, 364
edge, 1456
effective, 344, 350, 353
in GaN, 1527
gap, 1098, 1116
in germanene, 1535, 1537, 1540, 1553
low field, 1516–1519, 1524–1526, 1534, 1552, 1553
in monolayer TMDs, 1554
in monolayer WS_2, 1554
in phosphorene, 1533–1535, 1553, 1554
in silicene, 1535, 1537, 1540, 1553
in 2D materials, 1531, 1536, 1553, 1554
small field, 352
tensor, 1423
universal curve, 353
Model order reduction (MOR), 1330
Modelocking, 862
Models, 1233
analytical, 1261
macroscopic, 1476–1485
microscopic, 1461–1477
Modified Gram-Schmidt process, 1329
Modulation transfer function (MTF), 765
Modulus, 186
Moiré fringes, image sensors, 362
Moisture absorption, 185
Molecular beam epitaxy (MBE), 19, 724, 859, 877, 888
Molecular dynamics (MD), 1454, 1457
Molecular dynamics, ab initio (AIMD), 1474
Molten state, 1113
Molybdenite, 1094
Molybdenum trioxide (MoO_3), 1032
Moment of distribution function, 1342
Moments
mixed, 1261, 1262
of the distribution function, 1462
range, 1261, 1266, 1267
Momentum conservation, 871
Momentum exchange, 1586
Momentum operator, 1561, 1608
Momentum-relaxing scattering, 1591
Monolayer, WS_2, 1554
Monolithic integration, 889
Monolithic membranes, 672
Monte Carlo (MC) method, 1336, 1345, 1516, 1519, 1524–1529, 1531, 1553, 1572
many-body Wigner equation, 1575–1578,
reverse MC calculation, 1455
single-body Wigner equation, 1566–1575
Monte Carlo techniques, 1105
Monte-Carlo simulation, 157, 1268, 1270, 1318, 1340, 1357
amorphous, 1269
crystalline, 1269–1270
dynamic, 1052, 1270
non-self-consistent, 1433
physical models, 1268–1269
Moore's law, 180, 259, 279, 366, 1202
MOR method, 1326, 1328
More-than-Moore (MtM), 637
Morphable components, 1320
MOS C-V technique, 150
MOS capacitor
exact charge partitioning, 365
functioning regimes, 334, 342
N-type substrate, 342–343
quantitative relations, 339
MOS gate thyristors
and IGBT competition, 477
base resistance controlled thyristor, 476
circuit, 475
emitter switched thyristor, 476–477
MoS_2/graphene/WSe_2 heterostructure-based photodetector, 791
Mott FET, 932
Mott insulators, 604
Movable mass, 655
Movable membrane, 668
Moyal mathematical formalization, 1565
MRAM, 609–610
MS interface, 375, 376, 384, 385
MTS, *see* Memory threshold switching (MTS)
Multi domain FeFET (MD-FeFET), 946
Multi domains (MD), 949, 951
Multi-functional biodegradable sensors, 1030

Multi-gate and multi-channel (MG-MC), 317
Multi-scale analysis, 1426
Multi-scale modeling
  concurrent, 1432–1437
  sequential, 1426–1432
Multidimensional implantation models, 1265
Multigate, 877
Multigate nanodevices, 326
Multijunction solar cells, 724–727
Multilayer deposition, 206
Multilayer perceptron (MLP), 1168
Multilevel programming, 609
Multiphase DC/DC power converters, 108
Multiple constraints, 1320
Multiple exciton generation (MEG), 734
Multiple linear least squares, 128
Multiple patterning, 286
Multiple patterning lithography, 1287
Multiple stepped oxide field-plate trench MOSFET, 439
Multiple-level cells (MLC), 1101, 1106, 1115, 1116
Mushroom cells, 1107, 1108
Mushroom-like cell, 1470
Mutual coupling, 1237
Myriad atomistic structure, 1604

N
NAND
  array, 612
  flash, 56–58
  flash memories, 1434–1437
  flash technologies, 1171, 1172
  logic operation, 1079, 1081
  memory technology, 39
Nanoanalysis, 124
Nanocrystals (NCs), 728
Nanodevice
  characteristics, 1602–1604
  modeling approaches, 1604–1605
Nano-diffraction (ND), 127
Nanoelectromechanical systems (NEMS), 936, 1304, 1305, 1308, 1322
Nanoelectronic devices, 326
Nano-force sensor, 1310
nanoHUB.org, 1634
Nanoimprint lithography (NIL), 28, 279, 294
Nanoindentation, 183
Nanomaterials, 727
Nanomembranes (NMs), 1027, 1034
Nano-optics, 1322
Nano-oscillators, 949
Nanoparticles (NPs), 728
Nanoring, 1324
Nanoscale CMOS
  FDSOI, 311, 312
  quantum effects, 312, 313
  Si/SiO_2-high k interface, 314
  strained channels, 313
  ultimate device architecture, 314–316, 318, 319
  variability, 313
Nano-scaled field effect transistors (nanoFETs), 1602, 1604
  architectures and materials, 316
  CMOS, 317
  ferroelectric gate devices, 325, 326
  nanostructure, 323
  tunnel, 318, 320–324
Nanostructure, 371, 1324, 1325
Nanotechnology, 727–733
Nanotubes, 727
  carbon, 1470
Nanowire(s), 310, 371, 384, 727, 1496, 1498, 1501–1503, 1507, 1510
  electronic structure, 1620–1622
  HTFETs, 890
  solar cells, 731
Navier-Stokes equation, 1316
Navigation, 642
N-channel MOSFET, 343–345
  differential conductances and drain current, 346–347
  GCA, 345
  linear-parabolic model, 347
  subthreshold current, 347–350
  test, 1397, 1402–1407
Near-infrared spectral region (NIR), 1032
Near-UV (NUV) region, 284
Negative differential resistance (NDR), 1469, 1479
Negative bias temperature instability (NBTI) effect, 78, 440, 938
Negative capacitance (NC), 899, 933, 934
Negative capacitance FET (NCFET), 310, 933
Negative capacitance model, 1254
Negative capacitance tunnel FETs (NC-TFETs), 932
Negative differential resistance (NDR), 869, 1095, 1099
Negative U-centers, 1102
Negative-differential-conductance (NDC), 810, 821, 822
NEMO computer program, 1546
Nerst, 1305
Network of localised states, 1460
Neumann conditions, 1384
Neural networks, 952, 1082, 1168, 1169, 1178, 1181, 1183, 1185–1187, 1189–1191, 1578–1580
Neuromorphic applications, 622–625
Neuromorphic computing, 949, 1095, 1168–1170, 1181, 1184, 1190, 1191
Neuromorphic networks
  memory transistor synaptic arrays, 1172
  SRAM arrays, 1178
  with memristive devices, 1184–1192
Neurotherapy, 1033
Neutral regions, 580
Neutron scattering, in chalcogenides, 1454
Newton–Raphson method, 1424, 1470
Next generation MEMS gyroscopes, 665–666
Nickel oxide (NiO), 1026
Nickel-silicon compounds, 131
NiFe resistors, 677
NiO_x, 607
Nitridation-enhanced diffusion, 1280
Nitrogen, 193, 197
Nitrogen-vacancy (NV) centers, 1218–1220
NLPH, 1328, 1329
n+ nn+ test structures
  drain current, 1370
  model check, 1369
  velocity profile, 1369
Node in IC technology, 366
Noise, 1432, 1594
  CCD, 362
Noise equivalent power (NEP), 779, 825, 841
Non-affine, 1330
Non-aqueous-based inks, 968, 969
Non-Boolean computing, 948
Non-equilibrium Green's function (NEGF), 401, 1584, 1586, 1588–1590, 1594, 1595, 1601, 1604, 1614–1616, 1618, 1633, 1634

in chalcogenide transport, 1474
decoupling, 1585–1586
dephasing interactions, 1590–1591
diffusive spin transport, 1591–1592
equations, 1586–1588
Hamiltonian, 1588
inscattering functions, 1589
self-energy function, 1588
superconducting devices, 1592
Non-ideal recombination, 716
Noninjecting contacts, 752
Non-interacting channel Hamiltonian, 1585
Nonlinear function, 1329, 1330
Nonlinear port-Hamiltonian system, 1328
Nonlinear solvers, 1398–1401
backtracking, 1399
damped inexact Newton method, 1400
damped Newton method, 1399
forcing term, 1399
globalization strategies, 1399
inexact Newton method, 1399
matrix-free approach, 1400
Newton method, 1398
stopping criteria, 1398
Non-linearity (NL), 627
Non-Maxwellian energy distribution, 1357
distribution function, shape of, 1358
qualitative analysis, 1357–1358
Non-orthogonal orbitals, 1608
Nonparabolic approximation, 872
Non-parabolic band structure, 1356
Non-perturbative methods, 1586
Non-polar semiconductors, 161
Non-quasi-static (NQS) models, 414–415, 1243, 1248
Non-scalable quantities, 367
Non-selective CVD Co liner, 201
Non-thermionic FETs, 932
Nonvolatile magnetoresistive memories
CMOS DRAM, 1146
CMOS SRAM, 1146
in-memory computing, 1150
MRAM developments, 1155, 1156
MTJ, 1146
racetrack memory, 1156
SOT, 1150
STT, 1146–1150
Non-volatile memory (NVM), 49–50, 78, 947, 954, 1082, 1095, 1096
dense floating gate transistor, 84
storage mechanism, 84
Norbornenes, 182
NOR flash memory
applications and roadmap, 55–56
array, operations and reliability, 55
NOR flash technologies, 1172
Normal field, effective, 353
Normalized surface potential, 333, 334
Normally-off configuration, 537
NOT gate, 1207
N-shaped $V(I)$ characteristics of PCM, 1478
N-type buried layers, 72
Nuclear magnetic resonance (NMR), 183
Nuclear scattering, 1263, 1268
Nuclear stopping, 5
Nucleation, 526
energy, 1051
heterogeneous, 1103
homogenous, 1103
rate, 1103
process, 1476, 1481
theory of, 1103
Number operator, 1587
Numerical aperture, 284, 285, 1287
Numerical method
backward difference formulas, 1390
edge-averaged finite element method, 1390
fully coupled Newton method, 1390
Gauss-Seidel solver, 1388
Gummel map, 1386
hole continuity equation, 1387
Jacobi solver, 1388
Jacobian matrix, 1390
linearized electron equation, 1387
Newton method, 1387
Sharfetter-Gummel method, 1390
trapezoidal rule, 1390
upwind scheme, 1390
Numerical range scaling model, 1263, 1265
Numonyx, 604
NVM panorama, 615
Nyquist limit image sensors, 362

O

Objective functional, 1322, 1323
Occupation factor, 1589–1591, 1593
Occupation function, 870, 893
Octamethylcyclotetrasiloxane (OMCTS), 182
Octree approach, 1392
Off-axis illumination, 285
Off condition, in MOSFETs, 346, 351
OFF current, 879–883
Off-normal flux, 195
Off-state
characteristics, 554
reliability, 567
stress, 569
tunneling, 880
Ohm's law, 1339
Ohmic contacts, 145, 147, 716
Ohnesorge number, 970
Oligoethylene tetratetracontane, 1028
OMENwire, 1623, 1627, 1633, 1634
On condition, in MOSFETs, 346, 351
ON-current, 875
One-dimensional analytical models, 1262
1D Lebesgue measure, 1443
1D nanowires, 310
1-D Schottky based devices, 375–376
ON/OFF ratio, 1105, 1110
ON/OFF resistance ratio, 614
On-state resistance, 532
One time programmable memory, 83
One-electron Schrödinger equation, 1586, 1595
One-transistor–one-resistor (1T1R), 1045
Open boundary conditions, 1586
Open loop, 655
Open packages, 652
Operation, floating-gate, 357
Operators, 1560
Optic module, 685
Optical absorption, 703
Optical antenna, 1325

Optical cavity, 795
Optical communication, 863
Optical critical dimension (OCD), 248
Optical data storage, 1452
Optical elements, 158
Optical gap, 159, 160
Optical memory, 1095
Optical phonon scattering, 1367
Optical power, 858–859
Optical properties, 702–705
Optical proximity correction (OPC), 23, 285
Optical pumping, 854
Optical sensing, 359–361
  CCD, 359
Optical sensors, 1007
Optical trapping, 1325
Optical vortices, 1324
Optimization problem, 1320
Optimization process, 1326
Optimization variable, 1319
Optoelectronic devices, 1038
Opto-electronics, 526
Ordinary differential equations (ODE), 1308
Organic coating (OC), 287
Organic dielectrics, 974
Organic planarizing layer (OPL), 171, 221, 287
Organic semiconductor deposition, 973–974
Organic semiconductors, 962–964, 1026
Organic solar cells, 721–722
Organic TFT, 1252–1253
Organometallic precursors, 199
Organosilicate glass, 182
Organosilicon, 182
  precursors, 183, 207
Orthonormal set, 1607
Oscillation frequencies, 810, 837
Oscillations of PCM, 1479, 1482–1485
  macroscopic models, 1478
Oscillator, 810, 812, 817, 818, 820–823, 830, 835–837
  PTM, 949
Ostwald ripening, 1280
OTS, *see* Ovonic threshold switching (OTS)
Output characteristics, 347, 883, 891, 893, 895
  in MOSFETs, 347, 351
Output circuit, CCD, 362
Output conductance, in MOSFETs, 346, 350
Output spectrum, image sensors, 362
Over pad metallization, 80
Overdamped plasma waves, 781
Overlap matrix, 1475
Ovonic snap back, 1462
Ovonic materials, 1094, 1110
Ovonic threshold switching (OTS), 1071, 1100–1103, 1110, 1453, 1459, 1485, 1486
  electronic models, 1101–1103
  possible explanations, 1459
  structural models, 1101, 1103
  thermal models, 1101, 1102
Oxidation, 17, 1282–1283
  barrier, 211
  barrier properties, 191
  barrier test, 205
  dry, 1284
  local, 1283
  multidimensional simulation, 1285
  one-dimensional simulation, 1283
  stress-dependent, 1285
  wet, 1284
Oxidation-enhanced diffusion, 1280
Oxidation-reduction reaction, 1065
Oxidation-retarded diffusion, 1280
Oxide-based resistive RAM (OXRAM), 604, 607–608
Oxide capacitance, 334
Oxide flow, viscoeleastic, 1286
Oxide growth, parabolic and linear, 1284
Oxide injection, 1432, 1433
Oxide isolation, 98
Oxide semiconductors, 1024
Oxidized copper (CuOx), 206
Oxygen, 161, 193
Oxygen-barrier layer, 171
Oxygen doped silicon carbide (ODC), 211
Oxygen vacancies (Vo), 608
Oxygen-vacancy-based RRAM (Ox-RRAM), 1045
  CF, 1054, 1057
  endurance test, 1056
  equivalent circuit, 1059
  LRS, 1057
  LRS to HRS, 1048
  physical processes, 1047, 1055
  RESET processes, 1048, 1054
  resistive switching mechanisms, 1046
  SET process, 1055
  simulation flowchart, 1053
  temperature, 1049
  thermally controlled process, 1048
  uniformity/reliability, 1046
  unipolar *vs*. bipolar, 1049
  unipolar mode, 1048, 1049
  voltage, 1055

P
Packaging, 650–653
Pair-diffusion models, 1274
Palladium, 378
Parallel computing scaling, 1618–1619
Parallel-to-series-conversion, CCD, 360
Parameter fitting, 1607
Parameter modeling, 1340
  carrier generation and recombination, 1340–1341
  mobility, 1340
Parameterization, 1319
Parametric model order reduction (pMOR), 1326
Parametrised data, 1307
Parasitic bipolar action, 374
Parasitic capacitance, 433
Parasitic conduction, 534
Parasitic resistance, 180
Partial differential equations (PDEs), 1308, 1320–1322, 1383–1385
Partially depleted (PD) SOI MOSFETs, 1248
Particle current density, 1415
Particle trap, 1310
Pass transistor (PT), 949, 950
Passivated emitter and rear contact (PERC), 709
Passivation, 80, 711
Passive SPICE, models
  capacitor, 1235
  inductor, 1236–1237
  linear controlled sources, 1237
  MOSCAP, 1235–1236
  resistor, 1234–1235
  transmission lines, 1238

Passive micromixer, 1322
Pattern collapse, 190
Pattern-density variation, 171
Patterned copper approach, 79
Pattern noise, image sensors, 362
Pauli exclusion principle, 1427
Pauli spin matrices, 1586, 1588
PbO, 757
P-ch IGBT devices, 468
P-channel (P-ch) MOSFETs, 436–437
PCIM, 1247
Pearson distributions, 1262, 1263
Peierls
  distortion, 1455
  substitution, 1609, 1610
Percolation, 1279
  conduction, 978
  mobility, 978
  model, 1113
Perdew-Burke-Ernzerhof functional, 1525, 1532, 1554
Performance and characteristics of GaN devices, 559
Performances
  CID, 357
  image sensors, 361–363
  limits, 719
  specification, 1319
Periodic microtexture, 1322
Perovskites, 607, 790–791
Perpendicular magnetic anisotropy (PMA), 614
Perpendicular MTJs (p-MTJs), 1148
Petrov-Galerkin method, 1328, 1346
P-GaN, 539
P-GaN gate structure, 550
pH buffers, 969
Phase change materials, 326
Phase change memories (PCMs), 58–62, 85, 608–609, 1169, 1181, 1182, 1184, 1186, 1187, 1189, 1190, 1453, 1459, 1482, 1485, 1486
  crystallization, 1479
  device architectures, 1106–1112
  device operation, 1099–1101
  historical overview, 1094–1095
  intrinsic device, 1478
  materials and PCM performances, 1105–1106
  memory switching and physics of phase change, 1103–1105
  in non-volatile memory market, 1095–1096
  optical and electrical properties of chalcogenide materials, 1097
  oscillations, 1479, 1482–1485
  OTS, 1101–1103
  performance improvements and perspectives, 1116–1117
  reliability, 1112–1116
  set, reset, 1453
  thermal analysis, 1481
  thermal capacitance, 1481
  thermal circuit, 1479
  thermal resistance, 1481
Phase-change memories (PCM) characteristics, 1478
  amorphous phase, 1479–1481
  dynamic setup, 1479
  limit cycle, 1480
  $V(I)$, N-shaped, 1478
Phase-change memories (PCM) macroscopic models
  of dynamic response, 1479–1481
  of oscillations, 1478
Phase change tunnel FETs (PC-TFETs), 932
Phase distribution, 1325
Phase field method, 1320
Phase locking loop (PLL), 662
Phase shift masks (PSM), 23, 285
Phase space, 1414
Phase transition (PTM), 940
Phase-relaxing scattering, 1591
PhaseFET, 941
Phases, CCD, 354, 359
Phenolic compounds, 305
Phenomenological drift-diffusion model, 1338
  diffusion current, 1339
  drift current, 1339
  parameter modeling, 1340–1341
  Poisson's equation and continuity equation, 1338
  semiconductor equations, 1339–1340
Philips MOS model 11, 1246
Philips MOS model 9, 1246
Phonon spectrum, 1521, 1522, 1524–1527
  GaN, 1527
  germanene, 1535
  phosphorene, 1532
  silicene, 1535
Phonon-assisted inter-band tunneling, 1526
Phonon-assisted tunneling, 875
Phonons, 1517, 1518, 1521, 1523
  acoustic, 1517, 1518, 1527, 1528, 1530
  flexural out-of-plane acoustic, ZA, 1532, 1533, 1535–1537, 1553
  longitudinal, 1553
  longitudinal optical, 1528
  optical, 1527, 1530
  optical, interlayer, 1532, 1533
  polarization, 1517
  spectrum, 1519
  transverse, 1524
PHONOPY computer program, 1532, 1533, 1535, 1539
Phosphorene, 372, 1525, 1531–1536, 1538, 1553, 1554
Phosphorene field-effect transistor, 1533, 1537, 1538
Photo acid generators (PAGs), 294, 296
Photo diode, 1240
Photoabsorption-based biosensors, 1004
Photoactive compound, 1290
Photocapacitor, 354, 356, 359
  integration time, 340
  MOS, 339
  MOS, epitaxial, 340
  sampling time, 340
Photoconductance decay (PCD), 151
Photoconductive gain, 779
Photoconductivity, in a-Si:H, 1452
Photocurrent, 700, 710
  modulated, measurement of, 1456
  steady-state, measurement of, 1456
Photodetection mechanism, 780
  bolometric effect, 781
  photogating effect, 781
  photovoltaic effect, 780
  plasma-wave-assisted mechanism, 781
  PTE effect, 780–781
Photodetectors
  detectivity, 779
  LDR, 779
  NEP, 779
  performance metrics, 778–779

Photodetectors (*cont.*)
photoconductive gain, 779
quantum efficiency, 779
response speed, 779
responsivity, 778
Photodiode, 682
Photoemission, in chalcogenides, 1454
Photogating, 781, 783–785
Photon fluence, 759
Photonic crystal cavities (PCC), 795
Photonic nanostructure, 1324
Photonics, with chalcogenide, 1452
Photoresists, 22, 186
alicyclic groups, 292
amplification factor, 291
catalyzer, 291
chemical compositions, 292
chemical environment, 291
chemical reactions, 290
coating materials, 292
development, 291
dry etching resistance, 292
hydrophobic monomers, 292
immersion lithography, 291
implementations, 293
multiple patterning techniques, 293
pattern transfer procedures, 291
polymer chains, 291
polymethacrylate backbone, 293
radiation wavelengths, 290
SADP methods, 291
ultrapure water, 292
UV irradiation, 291
Photothermoelectric (PTE) effect, 780–781
Photovoltage, 780
Photovoltaic converter, 722–724
Photovoltaic effect, 700, 780, 1032
Photovoltaic materials, 703
Photovoltaics, 700, 730
P3HT, 790
Physical and empirical modelling, 976
Physical unclonable function (PUF), 621
Physical vapor deposition (PVD), 17, 186, 194, 229
Physics of phase change, 1103
Physics-based compact model, 1055
Physics-based contact models, 1633
Piezo-electric polarization, 529
Piezoelectric energy harvesters (PEHs), 1033
Piezoelectric scattering, 1527, 1530
Piezoelectricity, 669
Piezoresistivity, 672
Pinch off, 189, 202
Pinned photodiode (PPD), 682
Pitch
division, 24
halving, 26
size, 173
split double pattering, 174
Pixel, 682
manufacturing, 687
response to an incident exposure, 762
Pixelated detectors, 769
Planar technology, 367
Planarize, 171
Planck's constant, 870
Plane waves, 1605
Plasma
density, 195
deposited SiCOH, 182
deposition process, 182, 183
doping, 1270
etch selectivity, 207
immersion ion implantation, 10
implant, 10–11
nitridation, 208
oscillations, 1429
potential, 195, 197
preclean, 188
screening, 853
surface treatments, 186
treatment process, 208, 209
waves, 1421
Plasma-enhanced atomic layer deposition (PEALD), 564
Plasma enhanced chemical vapor deposition (PECVD), 182, 960, 965, 1035, 1292
Plasma induced damage (PID), 185, 186, 190
Plasma reactive ion etch (PRIE), 219
Plasma-wave-assisted mechanism, 781
Plasma-wave photodetection, 781
Plasmonics enhanced graphene photodetectors, 783
Plating bath, 171
Plating initiation layer, 199
Platinum, 379
Plethora, 609
PN junction, 373, 375–378, 824, 827
diode, 380
at equilibrium, 579–583
forward bias, 583
reverse bias, 583
POD method, 1328, 1329
Point-contact transistor, 375
Point defects, 1261, 1269, 1272, 1273, 1278
intrinsic, 1267, 1271, 1274–1276, 1280
schematic representation, 1272
Point response function, 1265, 1270
Gaussian, 1266
Point slope, 875
Poiseuille flow, 1318
Poisoning, 192
Poisson equation, 1102, 1415, 1462, 1465, 1593
in a semiconductor, 333
in MOSFETs, 364
in scaling rules, 366
Poisson problem, 1386
Poisson process, 768
Poisson statistics, 763
Poisson's equation, 978, 1249, 1338, 1341, 1507
Polar bonding, 182
Polarity controlled device, 374
Polarity gate, 374
Polarizability, 182
Polarization, 158, 543, 608, 858, 1288
Polarization field, 531
Polycaprolactone (PCL), 1032
Poly(caprolactone)-poly(glycerol sebacate) (PGS-PCL), 1022
Polycrystalline silicon (poly-Si), 960
Polyesters, 1022
Polyglycolic acid (PGA), 1022
Polyhydroxystyrene (PHS), 291
Polyimides, 80
Polylactic acid (PLA), 1022
Polymers, 1020, 1304

Poly(methyl methacrylate) (PMMA), 1013
Poly(vinyl alcohol) (PVA), 1022
Poly(4-vinylphenol) (PVP), 974
Ponderamotive force, 1310
Ponderomotive force, 1310
Poole/Poole-Frenkel effect, 882, 1460, 1461, 1464, 1466
Population inversion, 851
Pore collapse, 183, 185
Porogen, 182, 183, 187
Porosity, 182
Porous low-k SiCOH, 183
Porous SiCOH, 182, 184
Port-Hamiltonian system, 1326
Positive feedback, 1102, 1103
Positive programming pulse, 612
Post etch residues (PER), 225
Post exposure bake (PEB), 291, 306
Post-implantation annealing, 1280, 1282
Post-synaptic neuron, 1169
Potassium hydroxide (KOH), 1035
Potential at the semiconductor's surface, 333
Potentials and charges, 579–583
Power
  consumption, 636
  devices, 1032
  management, 80
Power MOSFET
  current and voltage characteristics, 426
  depletion mode, 425
  edge terminations for, 444–446
  enhancement mode, 425
  epitaxial layers and substrate wafers, 447–448
  MOSFET body diode, 443–444
  parasitic capacitance, 433
  superjunction MOSFET, 440
  types of, 427
  U-groove and V-groove structures, 427
Power P-i-N diodes, 494
Power rectifiers
  bipolar devices, 480–484
  unipolar devices, 477–480
Power semiconductor devices, 424
Power-performance-area-cost (PPAC), 259
Poynting vector, 1324, 1325
Prandtl number, 1318
Pre-amorphized region, 8
Pre-synaptic neuron, 1169
Precipitates, 1282
Precision, 649
Prediction, 1038
Predictiveness of macroscopic models, 1371
Preferential paths, 1470
  crystallization, 1471
Pressure sensors, 672–674
Principle of superposition of states, 1560
Printed organic TFTs, 973
  all-printed organic TFTs, 974–975
  organic dielectrics, 974
  organic semiconductor deposition, methods of, 973–974
  solution-processable organic semiconductors, 974
Printed with a soft stamp (PDMS), 1035
Printing techniques, 965
  features, 968
  flexographic printing, 968
  gravure printing, 967
  imprint and nano-imprint, 968
  inkjet printing, 966
  screen printing, 966
Probability of detrapping, 1468
Process simulation
  basic diffusion and reaction mechanisms, 1273
  deposition and etching, 1291–1296
  discretization and movement of surfaces, 1293–1294
  dopant diffusion at high concentrations, 1278–1279
  electrical activation, clusters and solid solubility, 1281
  equipment simulation, 1291–1293
  intrinsic point defects and impurities, 1271
  ion implantation, 1261–1271
  lithography simulation, 1286–1291
  macroscopic diffusion behavior of dopants, 1275
  oxidation, 1283
  process variations, 1296–1297
  scope and history, 1260–1261
  segregation, 1282
  simulation methodologies, 1283
  surface processes on dopant diffusion, 1279–1280
  transient diffusion effects, post-implantation annealing, 1280–1281
Process variations, 1290, 1297
  hierarchical simulation, 1297
  statistical, 1296
  systematic, 1296
Process window, 1296
Process-induced damage (PID), 186
Program disturb, 1434
Programming
  current, 1106, 1116
  curve, 1100, 1109–1111
  disturb, 1115
Progressive breakdown (PBD), 566
Progressive modeling directions, 1253–1255
Projected range, 1261
  lateral, 1266
Projection matrix, 1326
Propylene glycol methyl ether acetate (PGMEA), 970
Proton generation, 305, 306
Proximity disturb, 1115
Pseudo-particles, 1268, 1270
Pseudoatomic orbital (PAO), 1475
Pseudopotential, 1516, 1518, 1519, 1521, 1525, 1526, 1532, 1539, 1547, 1553, 1554
  empirical, 1516, 1518, 1519, 1524, 1526, 1539–1541, 1543, 1544
  norm-conserving, 1525, 1527
  ultrasoft, 1525
PSP MOSFET model, 1246
P-type buried layers, 72
P-type MOSFET (pMOS), 373
P-type substrate, 333–334, 336
Pull-down network (PDN), 944
Pull-up network (PUN), 944
Pulse height spectroscopy, 752
Pump process, 854–855

Q
Qiskit, 1204
Quadrature phase-shift keying (QPSK), 913
Quality factor, 1237
Quantization effects, 886
Quantronium, 1212
Quantum affinity, 1560, 1567
Quantum cascade lasers, 860–861
Quantum chemistry, 1605

Quantum computing, 1203–1204
bits and qubits, 1204
braiding, 1220–1222
entanglement, 1207
flying qubits, 1222–1223
integrated optics, 1213–1218
Josephson-based qubit, 1209
NV centers, 1218–1220
qubits as two-level atoms, 1205
silicon qubit, 1208–1209
surface bonds, 1222
Quantum confinement, 377, 384, 852
Quantum confinement structures, 860
Quantum density of states, 1586
Quantum dots (QDs), 728, 783, 860, 1206, 1209, 1253, 1254, 1602, 1603
closed systems, 1620–1621
crystal symmetry, 1603
self-assembled, 1603
Quantum efficiency (QE), 681, 711, 712, 758, 779
Quantum ESPRESSO software package, 1516, 1525, 1554
Quantum Fourier transform, 1203
Quantum Hall regime, 1594
Quantum hydrodynamics (QHD), 1474
Quantum interference, 1589, 1590
Quantum limit, 1212
Quantum mechanical interactions, 853
Quantum mechanics, 1203
Quantum mechanics, in phase space, 1559
admissible states, 1566
many-body Liouville-von Neumann equation, 1564–1565
many-body problem, 1564
Moyal mathematical formalization, 1565
single-body problem, 1561–1564
Weyl map and equations of motion, 1566
Quantum noise, 763
Quantum supremacy, 1204
Quantum transmitting boundary method (QTBM), 1546, 1618, 1633, 1634
Quantum transport, 1615, 1618–1619
Quantum wave function, 1205
Quantum well, 820, 852, 888, 892
Quasi leaky (QL) behavior, 952
Quasi steady-state photoconductance (QSSPC) method, 151
Quasi-equilibrium, 853, 855
Quasi-Fermi functions, 855
Quasi-Fermi potential, 344, 1431
Quasi-stationary potential, 1415
Quaternary amplitude-shift keying (QASK), 913
Qubit-oscillator system, 1217
Qubits, 1216
and bits, 1204–1205
and gates, 1217
braiding, 1220
flying, 1222–1223
Josephson-based, 1209
NV centers, 1218–1220
silicon, 1208
surface bonds, 1222
as two-level atoms, 1205–1206
Que and Rowlands rule, 760

R
Radiant-lamp, 203
Radiation energy
absorption coefficient, 302
electron, 303
electrostatic forces, 304
gain, 302
high-energy electrons, 302
ion-electron pair, 303
Lambert's law, 302
material molecules, 303
Monte Carlo simulations, 304
nanometers, 303
Onsager's theory, 303
photoelectrons, 302
photons, 302, 303
photoresist, 302
polymer, 303
proton, 302
secondary electrons, 302, 303
thermalization process, 302, 303
wavelength, 303
Radiative recombination, 706
Radio frequency (RF), 960, 1031, 1033
coils, 197
transistors, 906, 909
Radioimmunoassay (RIA), 1011
Raman scattering, 137
in chalcogenides, 1454
Raman spectroscopy
Brillouin zone, 137
carrier generation rate, 141
definition, 137
degree of disorder, 137
energy conservation, 137
experimental setup, 138
i-LOPC method, 142, 143
LO Raman shift, 142
micro Raman, 138
phonon peaks, 137
point defects, 141
silicon, 137
steady state, 141
Random dopant fluctuations (RDF), 1260, 1296
Random phase approximation (RPA), 1541
Random potential, 1591
Range
projected, 1263
straggling, 1261, 1263
Rapid single-flux quantum (RSFQ), 1254
Rapid thermal annealing, 12–15
Rapid thermal chemical vapor deposition (RTCVD), 564
Rashba channels, 1591, 1592
Rashba coefficient, 1591
Rashba spin-orbit interaction, 1591
Rate
condensation, 1481
evaporation, 1481
generation, 1481
Rayleigh criterion, 22, 1287
Rayleigh principle, 282
Rayleigh scattering, 138
RC delay, 897
RD, *see* Resistance drift (RD)
Reactive clean, 197
Reactive ion etching (RIE), 186, 225
Reactively sputtered, 193
READ operation, 1099, 1100, 1114
Read disturb, 1112, 1114–1115

Read window budget (RWB), 52
Read-out technology, 755
Recessed access device (RAD) technology, 48
Recessed gate, 98
Reciprocal space mapping (RSM), 135, 136
Recombination, 706
Recombination-current contribution, 587
Reconfigurable circuit, 381, 384
Reconfigurable device, 372, 374, 380, 384
Reconfigurable FET, 374, 381, 383
Reconfigurable nanowire FET (RFET), 383
Reconfigurable SB-MOSFETs, 374
Reconfigurable TFET, 384
Recovery-based error estimators, 1394
Recovery operation, 1114
Recrystallization, 17, 1096, 1112, 1114, 1115
Rectenna, 841
Reduced basis method, 1330
Reduced order model (ROM), 1330
Reduction ratio, 179
Reflection high-energy electron diffraction, 19
Reflow, 201, 203
Refraction index, 158
Regrowth based vertical MOSFET, 551
Regularization, 1321
Regularized design variable, 1322
Relative error, 1369
Relaxation oscillation frequency, 857
Relaxation time approximation, 1344, 1345, 1465
  macroscopic, 1345–1346
  microscopic, 1344
Relaxation times, 1353, 1357
Reliability, 192
  issues, 1112
Reliability, PCM
  cycling endurance, 1113–1114
  data retention, 1112–1113
  read disturb, 1114–1115
  thermal disturb, 1115–1116
Renormalization method, 1613
Replacement metal gate (RMG), 263, 265
Representation, pseudoatomic orbital, 1475
Research lab, 1038
RESET, 613, 614
  current, 1105, 1108, 1110, 1116
  current density, 1106
  operation, 1099, 1105, 1106
  in PCM, 1453
  power, 1105
  pulse, 1099, 1101, 1105, 1113, 1115
  state, 1099, 1105, 1106, 1111, 1112, 1116
Residual current, 770
Residual-based error estimators, 1394
Resist development, 1287, 1290
Resistance, 1584–1586
  change with time, 1457
Resistance drift (RD), 1106, 1109, 1116, 1453, 1457–1458
Resistance variation, 615
Resistive power loss, 713
Resistive RAM memory, 85
Resistive switching (RS), 1020, 1044
Resistive-switching random access memory (RRAM), 1044
  AND logic, 1078
  applications, 1045
  brain-inspired computing, 1082, 1083
  classification, 1045
  computing in memory, 1078
  crosspoint array, 1084
  embedded memory, 1075, 1077, 1078
  face pattern, 1085
  MIM structure, 1044, 1045
  NAND logic, 1080, 1081
  output/input signals, 1085
Resistivity, 193, 626
  assumptions, 144
  cases, 144
  contactless, 145
  expression, 142
  ion implantation, 143
  precautions, 145
  semiconductor, 143, 144
Resistor, 1234
  R3_CMC, 1235
  thin film, 1235
Resolution, 649, 765
  CCD, 361
  image sensors, 361
Resolution enhancement techniques (RET)
  immersion lithography, 284, 285
  mask correction methods, 285
  multiple patterning, 286
  off-axis illumination, 285
Resolution of spectrometric detector, 754
Resonance frequency, 656
Resonant periodic gain (RPG), 862
Resonant-tunneling diodes (RTDs), 820–823, 1254, 1615
  applications, 823
  frequency limitations, 822–823
  oscillators, 821–822
  perspectives, 823
Resonator, 851, 855–856
  feedback, 855
  modes, 855
Resorbable sensors, 1029
Response speed, 779
Responsivity, 758–762, 778, 840, 841
Reststrahlen band, 161
Resurf effect, single and double, 77
Reuseability, 1305
Reverse bias, 583
Reverse biased P-N junctions, 69
Reverse biased SOA, 458
Reverse blocking IGBT, 470–472
Reverse conducting IGBT, 471
Reverse polarization, 587
Reverse transfer capacitance, 433
Reversible switching, 1458
Reynolds number, 970, 1322, 1323
RF superconducting quantum interference device (RF-SQUID), 1212
Riedel peak, 1210
Rigorous coupled wave analysis (RCWA), 1288, 1290
Robin conditions, 1384
Rock-salt structure, 1456
Roll off frequency, 667
Rolling shutter (RS), 684
ROM, 1326–1330
Rotor, 655
RPI a-Si TFT Model, 1253
RRAM array, 1071
Runge-Kutta schemes, 1384
Ruthenium, 199

S
Safe operating area (SOA), 91
Sample-under-test (SUT), 1013
  Sampling
  CCD, 359
  function, image sensors, 361
  time, 339
  time, in photocapacitors, 340
Samsung, 605
Saturation
  current, 346, 351, 352
  drain voltage, 397
  surface potential, 346, 351
  velocity, 352, 1340, 1359
  voltage, 346, 351, 352, 396, 883
Saturation region, 346, 592, 595
  in MOSFETs, 346, 351
SB electro-optical devices, 374–375
Scalability, 626, 1105, 1204
Scalar variable, 1386
Scale, 1305
  effect, 1322
  factor, 661
Scaled dimensionless DD model, 1386
Scaling, 260
Scaling length, 870, 877, 886
Scaling of Boltzmann equation, 1350
Scaling rules
  in MOSFETs, 366–368
  with constant field, 366
Scaling theory, 1202
  generalized, 366
  limits to, 367
Scanners, 23
Scanning capacitance microscopy (SCM), 122
  active dopant concentration, 156
  AFM tip, 153
  Al concentration profile, 157
  AlGaN/GaN heterostructure, 155, 156
  capacitance variations, 153
  channel region, 155
  DC bias, 153
  4H-SiC power MOSFET, 155
  lateral resolution, 153
  oxidized/non-oxidized regions, 155, 156
  quantitative carrier profiles, 153
  schematic illustration, 154
  signal *vs*. p-type/n-type Si, 153, 154
  TEM analyses, 155, 156
  uses, 155
Scanning electron microscope (SEM), 224, 230, 234
Scanning spreading resistance microscopy (SSRM)
  active dopant concentration, 156
  calibration curves, 153, 154
  conductive tip, 153, 154
  contributions, 153
  lateral resolution, 154
  limitations, 156
  resistivity profile, 157
  schematic illustration, 154
  semiconductors, 156
  3D carrier distribution, 156
  total resistance, 153
  2D MOSFET structure, 155, 157
  2D resistivity distribution, 153
  uses, 155
Scanning transmission electron microscopy (STEM), 181
  AlGaAs multishell nanowire, 124, 126
  EELS, 125
  electron wave functions, 122
  $GeSb_2Te_4$, 126
  $GeSb_2Te_4$, 125
  HAADF micrographs, 123–125
  microanalysis, 124
  micrographs, 123
  nanoanalysis, 124
  principle, 122
  schematic illustration, 122
  SI, 128
  SiO_2/4H-SiC interface, 127, 129
  stoichiometries, 124
  twin defect, 124
  vacancies, 123
  Z-contrast, 123, 125
Scattering
  acoustic phonons, 353
  angle, 1268, 1418
  effects, 1563–1564
  integral, 1415, 1427
  operator, 1344, 1595
  potential, 1590
  surface roughness, 353
Scharfetter–Gummel discretization, 1340, 1445
Schawlow-Townes formula, 857
Schottky barrier (SB) based devices, 372–375
Schottky barrier diode (SBD), 477, 814, 817, 818, 820, 823, 825–827, 1239
Schottky barrier height (SBH), 373, 375, 376, 383
Schottky barrier junctions, 1247
Schottky barrier metal-oxide semiconductor field-effect transistor (SB-MOSFET), 372–374, 383
Schottky barrier TFTs, 1000
  accuracy requirement for biasing circuitry, 1003
  current sensitivity to variations, 1003
  figure of merit, 1001–1002
  IGZO TFTs, subthreshold model for, 1001
Schottky contact, 372, 375–377
Schottky controlled injection diode structure, 486
Schottky diodes, 376, 599–601, 840, 1250
  driving application of THz Schottky diodes, 819–820
  perspectives, 820
  terahertz Schottky junction, 815–816
  terahertz Schottky multipliers and mixers, 817–819
  terahertz Schottky planar diode, 816–817
Schottky point-contact transistor, 375
Schottky rectifiers, 495
Schottky-barrier junction, 1351
Schottky-contact diode, 1250
Schottky-Mott relation, 384
Schrödinger equation, 1467, 1564, 1595, 1610
Schubweg, 753
Screen printing, 966, 968
Second order partial differential equation system, 1307
Secondary ion mass spectroscopy (SIMS), 149, 1264
Secondary plasma region, 197
Security systems, 1038
Seebeck coefficient, 780
Seebeck effect, 1305, 1456
Seed layers, 192, 193
Segregation, 1282
  coefficient, 1282
  interface, 1282

Selberherr, Siegfried, 1336
Selected area electron diffraction pattern, 119
Selective-area-growth (SAG), 268
Selective Co cap, 211
Selective CVD Co deposition, 201
Selective metal cap, 172
Selective-area growth, 890
Selectively implanted collector (SIC), 834
Selectors (access device), 1072, 1095, 1101, 1110, 1111
Self adjoint, 1441
Self-aligned double pattering (SADP), 26, 58, 175, 177, 221, 288, 293
Self-aligned implant process, 509
Self-aligned quadruple patterning (SAQP), 26, 288
Self-aligned silicide (SALICIDE), 91
Self-aligned-via (SAV) integration scheme, 174
Self-amorphization, 8
Self-assembled monolayers (SAMs), 973
Self-assembly, 1305
Self-capping, 200
Self-consistent calculation, 1590
Self-energy function, 1584, 1585, 1590
Self-heating cells, 1107
Self-heating effects, 559
Self-interstitials, 1280
Self-ionized copper seed, 199
Self-ionized PVD copper, 203
Self-ionized sputtering, 198
Self-sputtering, 204
Self-sputtering plasma, 198
Semi-discrete phase-space, 1572
Semi-hermetic packages, 652
Semiconductor Bloch equations (SBE), 1545
Semiconductor capacitance, per unit area, 336
Semiconductor device, 1385–1386
  n-MOSFET, 1402
Semiconductor equations, 1338–1340
Semiconductor lasers
  applications, 862–863
  beam quality, 858
  dynamics, 857
  fundamental behavior, 857
  gain medium, 851–854
  microcavity lasers, 861–862
  optical power, 858–859
  polarization, 858
  pump process, 854–855
  quantum confinement structures, 860
  resonator, 855–856
  semiconductor materials, 859–860
  spectral properties and coherence, 857–858
  temperature dependence, 859
Semiconductor materials, 859–860
Semiconductor memory, 38
  types of, 38
  volatile memory, 40
Semiconductor modeling
  Auger mechanism, 1402
  Canali's model, 1402
  charge neutrality condition, 1386
  dimensionless form, 1386
  drift-diffusion model, 1385
  Einstein's relation, 1388
  finite element discretization, 1389
  Masetti's model, 1402
  Maxwell-Boltzmann statistics, 1386
  Poisson equation, 1386
  Shockley-Read-Hall mechanism, 1402
  thermodynamical equilibrium condition, 1386
Semiconductor saturable absorption mirror (SESAM), 862
Semiconductor technologies, bio-sensing, 1004–1007
Semiconductor-on-insulator (SOI) formation, 33
Semiconductors, 1024, 1234, 1253, 1254
  absorption coefficient, 158
  amorphous, 1452–1454
  defects, 161, 162
  dielectric function, 160
  dispersion relations, 160
  doped substrate *vs*. wavelength, 161
  Drude-like term, 161
  glasses, 159
  impurities, 161, 162
  index of refraction, 158
  joint density of states, 161
  lattice vibrations, 160
  optical gap, 159, 160
  reflectance, 158
  Si *vs*. wavelength, 160
  SiO_2 films, 159
  transparent layers, 160
Semiconductor–insulator–semiconductor (SIS) capacitor, 47
Sense, 662
Sense amplifiers (SAs), 1069
Sensitivity
  image sensors, 363
  of threshold, 1472
Sensitizing centers, 783
Sensor(s), 636
  cube, 1305
  integration, 687
  market, 638
  market revenue, 639, 640
  networks, 643–645
  solid-state, 354
Sequential 3D integration
  BEOL, 273
  CMOS, 272
  definition, 272
  FEOL, 273
  nMOS/pMOS, 275, 276
  Si layer, 273
  T-S3D/C-S3D cases, 273
  TEM, 275
Sequential multi-scale modeling
  balance equations, 1426–1427
  hierarchical drift-diffusion model, 1431–1432
  hierarchical hydrodynamic model, 1427–1431
Series eesistance, 712
SET
  energy, 606
  operation, 1099, 1100, 1115
  in PCM, 1453
  power, 1105
  pulse, 1099, 1105, 1113
  speed, 1105
  state, 1099, 1105, 1106, 1111, 1113, 1116
7-nanometer node, 180
Shadowing, 10, 195
Shallow trench isolation (STI), 74, 241, 263
Shannon's theorem, 361
Shape optimization, 1319, 1320
SHE, *see* Spherical harmonics expansion (SHE)
Sheet resistance, 144, 1234, 1235

Shichman-Hodges, 1244
Shielded SiC planar power MOSFET structure
  channel mobility, 507
  device structure, 505
  experimental results, 508
  gate oxide screening, 505
  on-resistance, 507
  threshold voltage, 505
Shielded trench-gate SiC power MOSFET
  device structure, 513
  experimental results, 514
  on-resistance, 513
Shielding, 194
Shifted Maxwellian, 1344
Shock test, 660
Shockley and Queisser's (SQ) limit, 723
Shockley equation, 1239
Shockley-Ramo theorem, 748, 769
Shockley-Read-Hall model, 1340, 1345, 1507
Shockley-Read-Hall (SRH) recombination, 151, 707, 880
Short channel effects (SCEs), 260, 352, 1338, 1367, 1498
Short-channel MOSFETs, 352
Short-circuit SOA, 459–463
Short diodes, 586
Short-range order, in chalcogenides, 1454
Shot noise of the dark current, 763
Shunt resistance, 712
Sidewall contact, 378
Sidewall image transfer (SIT), 26, 175, 221
Sidewalls, 193
Sidewall scattering, 201
Sidewall voids, 204
SiGe HBT, 1424
Signal, 762
Signal to noise ratio (SNR), 128, 667, 763, 767
Signed particle method, 1577–1578
Signed particles, 1560, 1567, 1572
Silica (SiO_2), 241
Silicene, 372, 1531, 1532, 1534–1541, 1553
Silicides, 29, 91, 373, 374, 376
  grain boundaries, 132
  heteroepitaxial coupling, 132
  laser annealing, 132
  NiSi layer, 132, 133
  transrotational, 132, 133
Silicon, 309, 1305, 1421, 1516, 1518, 1519, 1524–1526
  amorphous, 1452
  based tandem, 726
  dioxide, 192
  nanowires, 1539, 1544
  image sensors, 679–696
  materials, 1633
  nanomembranes, 1028
  nanoparticles, 133, 134
  nanowires, 1632
  qubit, 1208
  semiconductor sensor, 637
  substrates, 527–528
Silicon-anti reflective coating (Si-ARC), 287
Silicon-boron nitride, 191
Silicon carbide power devices
  bi-directional field effect transistor, 517
  body-diode, MOSFET, 510
  commercialization of, 518
  DI-MOSFET structure, 498
  ideal specific on-resistance for, 493
  JBSFETs, 511–512
  MOSFET, 496–498
  MOSFET with improved high frequency performance, 510
  MOSFET with two deep P_+ regions, 516
  power device applications, 519
  rectifiers, 494–495
  shielded planar power structure, 505
  shielded trench-gate power MOSFET, 512
  short-circuit capability, 512
  thick trench bottom oxide, trench-gate power MOSFET, 515–516
  unclamped inductive switching stress, 512
  V-groove trench-gate MOSFET, 516
Silicon carbide power DI-MOSFET structure
  blocking characteristics, 498
  on-resistance, 500
  reliability, 503–504
  threshold voltage, 503
Silicon carbides (SiC), 132, 134, 143, 371, 526
Silicon chromide, 106
Silicon heterojunctions (SHJ), 717
Silicon nanowires field-effect transistors (SiNWFETs), 1551
Silicon on insulator (SOI), 70, 272, 310, 879, 1028
Silicon-oxide-nitride-oxide-silicon (SONOS), 52
Silicon oxycarbide (SiCO), 263
Silicon photo multiplier (SiPM), 685
Silicon power devices
  IGBTs, 448
  MOS gate thyristors, 474–477
  power MOSFET, 426
  power rectifiers, 477
  UMOSFET, 437
  See also Insulated gate bipolar transistor (IGBT); Power MOSFET
Silicon SpinMOSFET and SpinFET
  Dresselhaus spin-orbit interaction, 1138, 1139
  electron current, 1136
  example, 1137
  semiconductor, 1138
  spin signal, 1136
  spin-orbit field, 1139, 1140
  spin-orbit interaction, 1137
  transmission probabilities, 1138
Silicon storage technology (SST), 1174, 1175
Silicon superjunction MOSFETs, 427
Silylation process, 188
SIMOX, 33
Simple harmonic oscillator model, 161
Simplified electrical Verilog-A photodiode model, 1240
Simulation, 1336
  equipment, 1260, 1291–1294
  feature-scale, 1291
  ion implantation, 1261
  lithography, 1286
  of deposition and etching, 1291
  of diffusion and activation, 1271–1283
  of oxidation, 1283–1286
  plasma, 1292
  process variations, 1296
  TCAD, 1473
Simulation program with integrated circuit emphasis (SPICE), 440
Single bandgap absorber, 724
Single-body Wigner equation, Monte Carlo methods, 1566, 1567
  affinity evolution and Monte Carlo algorithm, 1568
  affinity method, 1567
  basic validation, 1569

conservation of affinity and pseudo-particle injection, 1568
decoherence and quantum/semiclassical transition, 1571–1572
electrical characteristics, 1570–1571
resonant tunnelling diode, 1569, 1570
signed particle method, 1572
Single-body Wigner transport equation, 1561–1563
Single damascene, 170
Single electron charging effect, 1595
Single electron spin systems, 1125
Single-electron transistors (SET), 1253
Single-functional biodegradable sensors, 1030
Single gate, 877
Single heterojunction bipolar transistor (SHBT), 829
Single impurity qubits, 1208
Single junction technologies, 719–722
Single-layer graphene (SLG), 778
Single mode operation, 856
Single photon avalanche diode (SPAD), 684
Single-spin transistor, 1131–1134, 1136
Single-wafer process, 197
Singlet-triplet qubit, 1209
SiO_x dielectric, 182
SIS layer device, 1240
Six-moments model, 1336, 1364, 1373
Size optimization, 1319, 1320
Size-induced quantum confinement, 877
Skeleton precursors, 182
Skewness, 1261
Slater-Koster parameters, 1606
Sleep mode, 620
Slew rate, 897
Small drain voltage, 979
Small pixel effect, 769
Small-signal circuit, in MOSFETs, 347
Small-signal equivalent circuit, 910
Small-signal mobility, 1420, 1421
Smartphones, 638, 641–643
Snap back, 1467
ovonic, 1462
Soft X-rays lithography, 297
Software construction, 1305
SOI MOSFET models, 1247–1250
Solar cells, 700–702
Solar irradiance, 702
Solar spectrum, 702–705
Solid geometry, 1307
Solid phase epitaxial recrystallization, 17
Solid solubility, 1282
Solid-state sensors, 354
Solid-state memory system, 38
Solubility, 192
Solution-processable organic semiconductors, 974
Solvent-based inks, 969
Source, 1584
contact, 343
Source and mask optimization (SMO) methods, 285
Source conductance, in MOSFETs, 350
Source degeneracy, 873
Source line (SL), 1070
Source resistance, 879
Source/drain (S/D) boosters, 260
Source-drain current, 908
Source-mask co-optimization, 1290
Source-starvation, 1593
Source-to-drain tunneling, 1546, 1551
Space charge regions, 335, 580–581, 587–588
Spacer, 878, 897
layer, 288
patterning, 26
thickness, 177
Sparse matrix, 1305
Spatial frequency, 765
Spatial resolution, 361–362
Spatial sampling, image sensors, 361
Spectral responsivity, 681
image sensors, 363
Spectroscopic detectors, 752–754
Spectrum imaging (SI), 127
Spherical harmonics expansion (SHE), 1414, 1416–1419, 1445
BTE, 1417, 1419
distribution function, 1417
GaAs bulk, 1419
in-scattering, 1418
KS, 1416
N^+NN^+ structure, 1421
out-scattering, 1418
SiGe HBT, 1424
Spherical wavefront, 1324
SPICE model, 983, 984, 1234
active, 1239–1252
passive, 1234–1238
Spike-rate-dependent plasticity (SRDP), 1082
Spike-timing dependent plasticity (STDP), 63, 951, 1082, 1087, 1169, 1170, 1174, 1176, 1177, 1184, 1187, 1189
Spiking neural networks (SNNs), 1087, 1169
with memristive devices, 1184
Spin-based switches, digital applications
silicon SpinMOSFET/SpinFET, 1136
silicon switch, 1143, 1145
single-spin transistor, 1131
spin relaxation suppression, 1140
Spin-circuits, 1588
Spin electronics, 1591
Spin field-effect transistor (SpinFET)
definition, 1126
electric spin injection, semiconductors, 1127, 1128
spin-dependent hopping, 1131
spin-dependent trap-assisted hopping, silicon, 1128–1130
Spin-orbit coupling matrix, 1493
Spin-orbit splitting parameter, 1493
Spin-orbit torque (SOT), MRAM
CMOS, 1151
definition, 1150
magnetic field-free switching, 1151
MTJ, 1150
NM1, 1152
NM2, 1152, 1154, 1155
parameters, 1151
TIs, 1150
Spin precession angle, 1137
Spin qubits, 1209
Spin relaxation mechanism
CMOS, 1140
Elliott process, 1140
Hamiltonians, 1142
intersubband optical phonons, 1143
Pauli matrices, 1141
spin-orbit interaction, 1142
subbands, 1143

Spin-torque magnetic RAM (STTARM), 609–610
Spin-transfer-torque (STT), 1146, 1254
Spin-transfer-torque MRAM (STT-MRAM), 1255
Spintronic logic
  all-spin logic, 1159
  benchmarking/magnetoelectric spin-orbit logic, 1160, 1161
  buffered magnetic logic environments, 1159
  CMOS-based logic circuits, 1157
  logic-in-memory, 1157
  magnetic domain wall, 1157
  stateful, 1158, 1159
Split gate configuration, 380
Spontaneous emission, 855
Spreading resistance probe (SRP), 149, 151
Spurious velocity overshoot (SVO), 1361
Sputter deposition, 193
Sputter etching, 194
Sputter gases, 193
Sputter tool vendors, 196
Sputtered atom flux, 195
Sputtering, 964–965
S-shape negative differential resistance, 60
S-shaped characteristic, 1099, 1101
Stability, 659, 1308
  inequality, 1444
  in semi-on conditions, 571
  measurement, PCM oscillations, 1482–1485
Stabilizers, 969
Stable bonds, 1605
Stacking faults (SFs), 123, 135
Staggered, 886, 891
Staggered heterojunction, 888
Stand-alone memories, 618
Standard cell scaling (SDC), 261
Standard clean 1 (SC1), 220
Standard clean 2 (SC2), 220
Standard quantum mechanics, 1560–1561
State variables, 1320, 1342
Static induction transistor, 552
Static random access memory (SRAM), 41, 944, 1169, 1170, 1178
  cell and operating principles, 41–42
Static shielding diode, 484
Statistical variability, in dopant distribution, 367
Stator, 655
Steady-state currents, 1588
Steep slope devices, 870
Step stress, 566
Stepper, 23
Stereo light, 691
Sticking coefficient, 193, 195
STMicroelectronics device, 680
Stoichiometric vacancies, 1097, 1098
Stoichiometries, 124
Stokes processes, 137
Stopping criteria, 1322
Storage class memory (SCM), 62, 619, 1096, 1116
Straight-line patterns, 177
Strain, 853, 1286, 1492, 1495–1498, 1501, 1502, 1507, 1509, 1607–1608
  engineering, 897
  management, 526
Strain relaxed buffers (SRB), 265
Strained superlattice (SSL), 528
Stratton's approach, 1350–1351
Stratton, Robert, 1350
Stress, 886, 1260, 1273, 1285, 1286
  engineering, 34
  in PCM systems, 1458
  Stress-dependent oxidation, 1285
Stretchable electrodes, 1022
Stretchable electronics systems, 1027
String algorithm, 1293
Stripe cell surface topology, 438
Strong inversion, 335, 375
Structural design, 1319
Structural models, 1103
Structural relaxation, 1116
Structure preserving MOR, 1328
Structured light, 693
Stuck-reset, 1113, 1114
Stuck-set, 1113, 1114
Sub-resolution assist features (SRAF), 286
Sub-threshold swing (SS), 932
Subspace, 1328
Substrate current, 1433
Substrates, 526
Subthermal slopes, 895
Subthreshold approximation, 349–350
Subthreshold condition, 349
Subthreshold current, 347–350, 365, 871
Subthreshold slope, 979, 1512
Subthreshold swing (SS), 317, 349, 868, 872, 1633
Subtractive methods, 184
Supercapacitor electrodes, 1032
Supercapacitors, 1032
Superconducting levitation, 1310
Superconductor, 1593
Super FETs, 932
Super-hydrophobicity, 1323
Superjunction MOSFET, 440–443
Super-junction solutions, 109
Superlattice, 1116
Superlinear onset, 883–885, 891
Supernova Cosmology Project
  image sensors, 363
Surface states, 338
Surface barrier transistor, 375
Surface bonds, 1222
Surface-channel, CCD, 355
Surface channel tunnel junction, 869
Surface charge, 377
Surface cleaning, 194
Surface diffusion, 204
Surface mobility, 203
Surface passivation, 1618–1620
Surface plasmon resonance, 1324
Surface plasmons, 783
Surface potential, 333, 376
  and gate voltage, 334–336
  p-type substrate, 333–334
Surface recombination, 707
Surface-roughness
  scattering, 353
Surface states, 338
Surface tension, 204, 1322, 1323
Surface-to-volume ratio, 1322, 1323
Surfactants, 969
Surrogate, 1326
Swirls, in current, 1476
Switche, 1310

Switching, 1467
reversible, 1458
Synaptic devices, 951
Synchronous DRAM, 49
System
center-of-mass, 1268
laboratory, 1268
System in package (SiP), 650
System on chip (SoC), 273, 415, 650
System-technology co-optimization (STCO), 273
Systematic process variations, 1296

T
Table-based parameter modeling, 1366–1368
Tablets, 641–643
Ta/Cu interface, 171
TaN, 106
TaN barriers, 203
Tandem cell, 726
Tandem PiN Schottky (TPS) structures, 486
Tantalum (Ta), 192
Tantalum nitride (TaN), 192, 193, 247
Target surface, 195
Target voltage, 193
Target-to-substrate spacing, 195
Tauc equation, 1098
Tauc gap, 160
Taylor expansion, 990
Taylor series expansion, 1384
t-butyl methacrylate (TBMA), 291
TCAD simulation, 382
Technology
node, 366
planar, 367
Technology computer-aided design (TCAD), 1260, 1304, 1336, 1492
simulations, 376–379, 382, 384, 1473
Temperature
dependence, 859
glass, 1479
melting, 1479
profile, 1115
Temperature-dependent thermal conductivity, 1054
Template-assisted selective epitaxy (TASE), 888
Tendential value, 1465
Tensor processing unit (TPU), 1168
Tensor quantities and anisotropy, 1356
Terahertz (THz), 808–810, 814–832, 834–842
Terahertz electronic devices
ballistic rectifiers, 842
complementary metal oxide semiconductor transistors, 836–838
field-effect transistor, 823–826
Gunn diodes, 810–814
heterojunction bipolar transistors, 827–836
resonant tunneling diodes, 820–823
Schottky diodes, 814–820
Terahertz Schottky junction, 815–816
Terahertz Schottky multipliers and mixers, 817–819
Terahertz Schottky planar diode, 816–817
2-terminal memristive devices, 1181–1182
Ternary alloys, 1454
Terpinenes, 182
Testing, 653
Tetragonal, 193
Tetramethoxyl silane (TMOS), 188
Tetramethyl silane, 182
Tetramethylammonium hydroxide (TMAH), 1035
Tetramethylcyclotetrasiloxane (TMCTS), 182
TFT-based biosensors, 1013–1015
The Broglie wavelength, 377
The National Renewal Energy Laboratory (NREL), 719
Thermal, 1320
analysis of PCM, 1481
capacitance of PCM, 1481
circuit of PCM, 1479
conductivity, 1105, 1106, 1116
confining materials, 1116
cross-talk, 1115
cure, 183
disturb, 1112, 1115–1116
energy, 1356
equilibrium, 1341
equilibrium approximation, 1339
evaporation, 964
models, 1102
resistance of PCM, 1481
stability, 1116
TBR, 1108, 1115
therapy platforms, 1031
vibrations, 893
voltage, 1428
Thermal boundary resistance (TBR), 1108, 1115
Thermalization, 723
Thermionic current, 880
Thermionic emission, 376, 868
Thermo-mechanical stresses, 104
Thermodynamic equilibrium, 1428
Thermodynamics, 1308
Thick oxide, 73
Thin film
analysis, 131, 132
deposition techniques, 1035
resistors, 106, 1235
solar cells, 721
technology, 721
Thin-film transistors (TFTs), 754, 1027, 1253
amorphous oxides semiconductors, 961–962
amorphous silicon, 960
basic performance and fabrication specifications, 960
CAD, 975–977
Cambridge's TFT model, 977–982
CAMCAS model, in simulation environment, 985
compact modelling, 975–985
computer interpretation of device model, 982–985
device architectures, 971–972
low-temperature polycrystalline silicon, 960
off region model, 981
organic semiconductors, 962–964
organic TFT, 1252–1253
printed organic TFTs, 972–974
Schottky barrier TFTs, subthreshold operation for, 1000–1003
small signal modelling, 986–1000
unified model, 981–982
Three-axial device, 655
3D-coherent X-ray diffraction imaging (3D-CXDI), 133
3D deposition, 1304
3D horizontal stacking RRAM array (HRRAM), 1073, 1074
3-D integration, 690
3D micro-coil fabrication, 1308
3D (nano) lithography, 1304
3-D sensing, 645, 691
3-D stack, 687

3D substrates, 797, 800
3D vertical stacking RRAM array (VRRAM), 1074, 1075
3DXPointTM technology, 62
Three-moments energy transport model, 1351–1352
Three-phase CCD, 355
Three-terminal injection scheme, 1128
3-terminal memristive devices, 1182
Three terminals test-pattern, 147
Threshold
  current, 1100
  field, 1102, 1106, 1461
  incomplete LU, 1402
  method, 1322
  of strong inversion, 335
  sensitivity of, 1472
  switching effect, 60
  temperature, 1102
  voltage, 346, 351, 398, 503, 1027, 1100, 1102, 1105, 1106, 1110, 1111
Threshold selector (TS), 939
Through-silicon-vias (TSV), 271, 650
THz time-domain spectroscopy (TDS), 809
Tight-binding (TB), 1492
Tight-binding approximation (TBA), 906
Tight-binding Hamiltonian, 1588
Tight-binding models
  ballistic transport from nanowire dispersions, TOB model, 1622–1623
  complex bands, 1610–1611
  consequences of discreteness and incompleteness, 1608–1609
  DFT-TB and nanodevice modeling, 1614
  direct transmission methods, 1612–1614
  effective-mass formula, 1609
  electromagnetic coupling Hamiltonian, 1609–1610
  full quantum transport *vs*. analytical model in long 15nm nanowires, 1626–1627
  full quantum transport, in long 15nm nanowires, 1623–1626
  full quantum transport, in short 5nm nanowires, 1627–1628
  Green functions, transport with, 1614–1615
  Hamiltonian, 1605–1606
  Hamiltonian matrix structures and scaling for closed systems, 1615–1616
  high-bias coherent transport simulations, convergence issues in, 1629–1632
  interfaces and transport, 1610–1614
  large-scale numerical aspects, 1615–1620
  localized-orbital representations, 1609
  nanodevice characteristics, 1602–1604
  nanodevice modeling approaches, 1604–1605
  nanowire electronic structure, 1620–1621
  open boundary conditions, scaling issues with, 1616–1618
  parameter fitting, 1606–1607
  quantum dots, 1620–1621
  quantum transport, 1618–1619
  short channel devices, 1632–1633
  strain, 1607–1608
  surface passivation, 1618–1620
  transfer matrices, transmission calculations with, 1612
Tilted ion implant, 27
Time-dependence, 566
Time dependent dielectric breakdown (TDDB), 208, 227, 938
Time-independent Schrödinger equation, 1561
Time of flight (ToF), 645, 693
Time resolved electric response, 1464
Time-to-failure (TTF), 568
Time-voltage, 621
TiN metal hard mask, 172
TiO_x, 607
Titanium (Ti), 192
Titanium nitride (TiN), 192, 385
Titanium oxide, 1325
Titanium-tungsten, 379
TlBr, 757
TMR, 675
Top electrode (TE), 1044, 1181
Top port, 668
Top-down approach, 890
Top-of-the-barrier (TOB) model, 1622–1623, 1627
TopCon technology, 717
Topography, 195
Topological insulators (TIs), 1150
Topology optimization, 1319, 1320, 1322, 1323, 1325, 1326
  general considerations, 1319
  optimization method, 1322
  variational problem and regularization, 1320
  problem, 1313
Total current densities, 586
Total harmonic distortion (THD), 667
Trajectory split approach, 1270
Transadmittance efficiency, 411–412
Transconductance, 347, 433, 988
  efficiency, 405–407, 409, 412, 1002
  in MOSFETs, 347, 351, 354
Trans-impedance amplifier (TIA), 1013
Transducers, 636
Transfer characteristics, 347, 553, 897
  in MOSFETs, 347, 351
Transfer efficiency, 356
Transfer function, CCD, 359
Transfer inefficiency, CCD, 356, 363
Transfer length, 145
Transfer matrix, 1289, 1295, 1612
Transferred electron devices (TEDs), 810
Transient analysis, 985
Transient diffusion, 1280–1281
Transient electronics, 1027
Transistors, 1029
Transit-time mode Gunn oscillations, 810–811
Transition frequency f_T, 828–834, 836
Transition metal dichalcogenides (TMDs), 312, 372, 384, 790, 890, 1525, 1538, 1539, 1554
Transition rate, 1469
Transitions, inter-trap, 1472–1473
Transmission coefficient, 1473, 1475, 1625
Transmission electron microscope, 888
Transmission electron microscopy (TEM), 266, 1022, 1046, 1075
  definition, 118
  dislocations and stacking faults, 118
  image plane, 118
  material processes, 120
  methods, 118
  micrographs, 120, 121
  schematic illustration, 118
  sketch, 119
  thermionic or field effect, 118
  transmitted electrons, 118, 119
  Z contrast, 118
Transmission gate (TG), 949

Transmission line, 1238
Transmission line model (TLM)
alloyed contacts, 146
end-contact resistance, 146, 147
lateral current crowding, 148
literature data, 148
semiconductor sheet resistance, 145
specific contact resistance, 145
test structures, 145, 146
Transmission probability, 870, 1589, 1590
Transmission rates, 863
Transmon, 1211
Transport factor, 899
Transport model
ab initio quantum, for chalcogenides, 1473–1477
trap-limited, 1461–1463
trap-limited, in a random network, 1469
trap-limited, with dispersive band states, 1464
Transversal electric (TE) polarization, 858
Transversal magnetic (TM) polarization, 858
Transverse energy, 872
Trap level, 1340
Trap-assisted tunneling (TAT), 869, 875, 880, 881, 890
tunneling current, 882
Trap-limited conduction (TLC), 978, 1103, 1460
Trap-limited transport model, 1461–1463
in a random network, 1469
with dispersive band states, 1464
Trapezoidal rule, 1390
Traps (localized states), 1098, 1102
Tree, 1305
Trench CAVET, 549
Trench cell technology, 470
Trench etch process, 173
Trench FET, 111
Trench MOS barrier Schottky (TMBS), 486
Triangles
acute, 1443
obtuse, 1443
Trifluoromethanesulfonic acids, 305
Trimethyl silane, 208
Trimethylaluminium (TMA), 965
Triphenylsulfonium triflate (TPS-tf), 302
Triple patterning, 24
True random number generator (TRNG), 621
Tubes, cathode-ray, 354
Tumble, 665
Tungsten, 192
Tunnel device, 375
Tunnel diode, 376, 380
Tunnel field effect transistors (TFETs), 268, 371, 372, 375, 379, 381–384, 869, 896, 899, 932, 1492, 1498–1505, 1507, 1509, 1510, 1615
ambipolar conduction, 885
BTBT, 870–872
complementary technology platform, TFET inverters for, 1503–1507
complex gate dielectrics, 897
device structures, 1498–1499
GaSb/InAs-based TFET optimization, 1502–1503
heterojunction, 1500, 1501
homojunction, 1499
HTFET, 885–893
n-type TFET, 869
OFF current, 879
ON-current, 875–879
operation principles, 869–870
output characteristics, 883–885
Tunnel magnetoresistance (TMR), 1182
Tunnel-effect, 677
Tunneling, 1492, 1494, 1496, 1497, 1499, 1500, 1502, 1509, 1510
enhancement factor, 882
gap, 887
probability, 870, 872, 875, 882
width, 870
width modulation, 873
Tunneling field-effect transistors (tFETs), 1526, 1546
Tunneling magnetoresistance (TMR), 1145
Turn-off (GTO) thyristors, 448
Turn-off switching waveforms, 545, 547
Turn-on switching waveforms, 545, 547
Turn-on-voltage, 981
Two-dimensional (2D) materials, 372, 384, 1516, 1519, 1524, 1525, 1531–1534, 1538, 1544, 1552–1554
Two-dimensional CCD
frame-transfer, 360
line-transfer, 360
Two-dimensional charge coupling, 492
Two-dimensional electron gas (2DEG), 144, 149, 155
Two-dimensional manifold, 1320
2D Lebesgue measure, 1443
2D materials, 778, 790–795, 890
2D patterning, 177
2D version of secondary ions mass spectrometry (2D-SIMS), 152
Two-diode test method, 376
Two-phase CCD, 355

U

U-centers, 1459
UFSOI/UFPDB/UFDG, 1250
Ultra-dilute sulfuric peroxide (uDSP), 222
Ultrafast spectroscopy, 736
Ultra large scale integration (ULSI) circuits, 309
Ultra-low-k (ULK) materials, 172, 225
Ultrapure, 199
Ultras, 1247
Ultra-shallow p-n junction diode, 376
Ultrathin body (UTB), 371, 372, 376, 377, 379, 380, 383
Ultra-thin body and box (UTBB) fully depleted silicon-on-insulator MOSFET, 392–394
back-biased, 403–407
device cross-section, 395
first-cut analog sizing method, 416
Ultrathin cap, 211
Ultraviolet (UV) irradiation, 183, 279
UMOSFET, 427, 437–438
Uncertainty quantification, 1326
Unclamped inductive switching stress, 512
Uncollimated deposition, 195
Under-the-barrier model, 1623
Uniformity, 195, 197
Unipolar, 343
devices, 343
operation, 375
Schottky type operation, 373
Universal memory, 604–607
Universal screening potential, 1268
Urbach energy, 894, 896
Urbach tails, 159, 160, 893, 1098, 1456
USB power delivery systems, 83
USIM, 1247
UV cure, 183, 185

V
V_{60}, 875
Vacancies, 875, 1267, 1271, 1273, 1280
Vacuum depositions
  atomic layer deposition, 965
  CVD, 965
  sputtering, 964–965
  thermal evaporation, 964
Vacuum level, 332
Vacuum mainframe, 197
Valence-alternation pairs (VAP), 1102, 1456, 1458
Valence band, 373, 906
Valence band effective density of states, 373
Valence-band hole, 853
Valence force field (VFF), 1605
Value, tendential, 1465
Van der Pauw, 144
van der Waals (vdW) gaps, 124
Van der Waals materials, 890
Van Hove singularities, 161
Van Roosbroeck, Willy Werner, 1336
Vanadium dioxide (VO_2), 939
VAP, *see* Valence-alternation pairs (VAP)
Varactor, 1235
Variable range hopping (VRH), 977
Variational methods, 1392
Variational problem, 1320–1323
Variations, systematic and stochastic, 1260
VBIC vertical BJT model, 1242
Vector, 1305
Velocity, 1589
  drift, 352
  saturation, 352
Velocity overshoot, 1359–1361, 1374
  spatial, 1426
  stationary, 1420
Ventilation hole, 668
Verilog, 983
Verilog-A standardization, 1255
Vertical devices architectures, 540
Vertical direction, 1261
Vertical DMOS, 86
Vertical DMOSFET, 427
  blocking characteristics, 428–430
  on-resistance of, 431–433
  P-channel and value for power electronics applications, 436–437
  switching characteristics, 433
  threshold voltage, 430–431
Vertical external cavity surface emitting lasers (VECSELs), 854, 861, 862
Vertical GaN devices modeling, 545
Vertical heterojunction TFET, 887
Vertical hot electron transistor, 915
Vertical MOSFETs, 550
Vertical nanowire HTFETs, 889
Vertical p-n junction, 381–382
Vertical transistors (VFET), 267, 562
Vertical tube furnaces, 12
Vertical-cavity surface-emitting lasers (VCSELs), 861
V-groove formation, 516
Via-first scheme, 173
Vibration modes, 663
Video interlacing, CCD, 361
Vienna *Ab initio* Software Package (VASP), 1516, 1520, 1526, 1532, 1535
Viscosity modifiers, 969
Visual representation, 557
Void formation, 1109, 1113, 1114
Voids, 189, 202
Volatile memory, 40–41
Voltage
  comparison, 535
  drop, 143
  ramp, 1055
  snapback, 1100
  source converter, 424
Voltage transfer characteristics (VTC), 943
Volume constraint, 1321
Volume inversion (VI), 314
Volume-minimized cells, 1107, 1109–1110, 1115
  bridge, 1109
  line, 1109
  pillar, 1109
  self-heating vertical wall, 1109, 1110
von Neumann computer architecture scheme, 40
Voronoi diagram, 1442, 1443, 1445
Voronoi volume, 1443

W
Wafer bonding, 32, 33
Wafer level bonding, 658
Wafers Per Hour (WPH), 284, 290, 299
Ward-Dutton partition, 1246
Waste electrical and electronic equipment (WEEE Directive), 1038
Water-based inks, 968
Water-soluble integrated circuit, 1035
Water-soluble materials, 1034
Water-soluble polymers, 1022
Wave vector, 906
Waveforms, 193
Wavefunction, 1587
Waveguides (WG), 778, 795–797, 1289, 1290
Wavelength, 1324, 1325
Wave packet, Gaussian, 1467
Weak-inversion condition, 335
Wearables, 641–643
Weibull distribution, 1113
Weibull plot, 571
Well-formed channel, 343
Well proximity effect (WPE), 10, 1245
Wenzel, 1323
Wentzel-Kramers-Brillouin (WKB) approximation, 870–872, 882
Wet cleaning/etching, Cu interconnects
  applications, 220
  brush clean, 221
  dissolved oxygen, 225
  HM, 226–229
  patterning, 221, 223–225
  post film deposition clean, 221
  pre-lithography backside clean, 221, 222
  process, 171
  tool, 220
  ULK removal, 226
Wet-etching, 20, 1305
Wettability, 192, 199, 1323
Wetting angles, 199
Wheatstone bridge, 672
Wide band gap (WBG) semiconductors, 111, 142, 143, 371, 383, 891
Wiedemann-Franz law, 1348
Wigner density functional theory, 1576–1577
Wigner formulation, 1560, 1564, 1572

Wigner function, 1212, 1217, 1572
Wigner quasi-distribution function, 1566
Wigner transport equation (WTE), 1561–1563
Wigner-Boltzmann transport equation (WBTE), 1563–1564
Winged edge, 1307
Wire resistance, 192
Wireless sensors networks, 643–645
Word lines (WL), 1069
Work function, 332, 353, 372, 376, 378, 383, 384, 885
Workfunction-induced doping, 372, 375, 377, 378, 380, 385
  charge plasma devices, 378–379
  gated Schottky based ultrathin-body devices, 376–378
  1-D Schottky based devices, 375–376
Wrap-around gates, 890
Write
  bandwidth, 1096
  speed, 1113

X
X-ray absorption spectroscopy (XAS), 130
X-ray analytical techniques
  brilliance, 130
  bulk materials, 130
  epitaxial layers, 130
  nanostructured materials, 128
  polar figure analyses, 131
  reciprocal space, 130
  silicon nanoparticles, 129
  synchrotron radiation, 130
  texturing, 131
  thin films, 131
X-ray attenuation coefficient, 759
X-ray detection, image sensors, 363
X-ray diffraction (XRD), 129–131
  in chalcogenides, 1454
X-ray fluorescence (XRF) technique, 226
X-ray photogeneration efficiency, 751
X-ray reflection (XRR), 135, 183
X-ray sensitivity, 758
X-rays, 747
XRD, *see* X-ray diffraction (XRD)
Xsim, 1247

Y
Young–Dupré equation, 199
Young's modulus, 1061, 1062

Z
Zener tunneling, 869
Zero bandgap, 778
Zero contour, 1320
Zero rate level (ZRL), 661
Zero-field mobility, 1353
Zinc-oxide (ZnO), 371
  nanorods, 615
Zirconium-doped hafnium oxide (HZO), 952
$Zn_{0.35}Te_{0.65}$, 1466